FUJITSU SEMICONDUCTOR
DATA SHEET

DS05-11432-1E

MEMORY Mobile FCRAM™
CMOS

64 M Bit (4 M word×16 bit)
Mobile Phone Application Specific Memory

MB82DBS04163C-70L

■ DESCRIPTION

The FUJITSU MB82DBS04163C is a CMOS Fast Cycle Random Access Memory (FCRAM*) with asynchronous Static Random Access Memory (SRAM) interface containing 67,108,864 storages accessible in a 16-bit format. MB82DBS04163C is utilized using a FUJITSU advanced FCRAM core technology and improved integration in comparison to regular SRAM.
The MB82DBS04163C adopts asynchronous page mode and synchronous burst mode for fast memory access as user configurable options.
This MB82DBS04163C is suited for mobile applications such as Cellular Handset and PDA.

* : FCRAM is a trademark of FUJITSU LIMITED, Japan

■ PRODUCT LINEUP

Parameter		MB82DBS04163C-70L
Access Time (Max) (t_{CE}, t_{AA})		70 ns
Access Time from CLK (Max) (t_{AC})	RL = 6, 5	10 ns
Active Current (Max) (I_{DDA1})		35 mA
Standby Current (Max) (I_{DDS1})	$T_A \leq +40$ °C	90 µA
Power Down Current (Max) (I_{DDPS})		10 µA

■ FEATURES

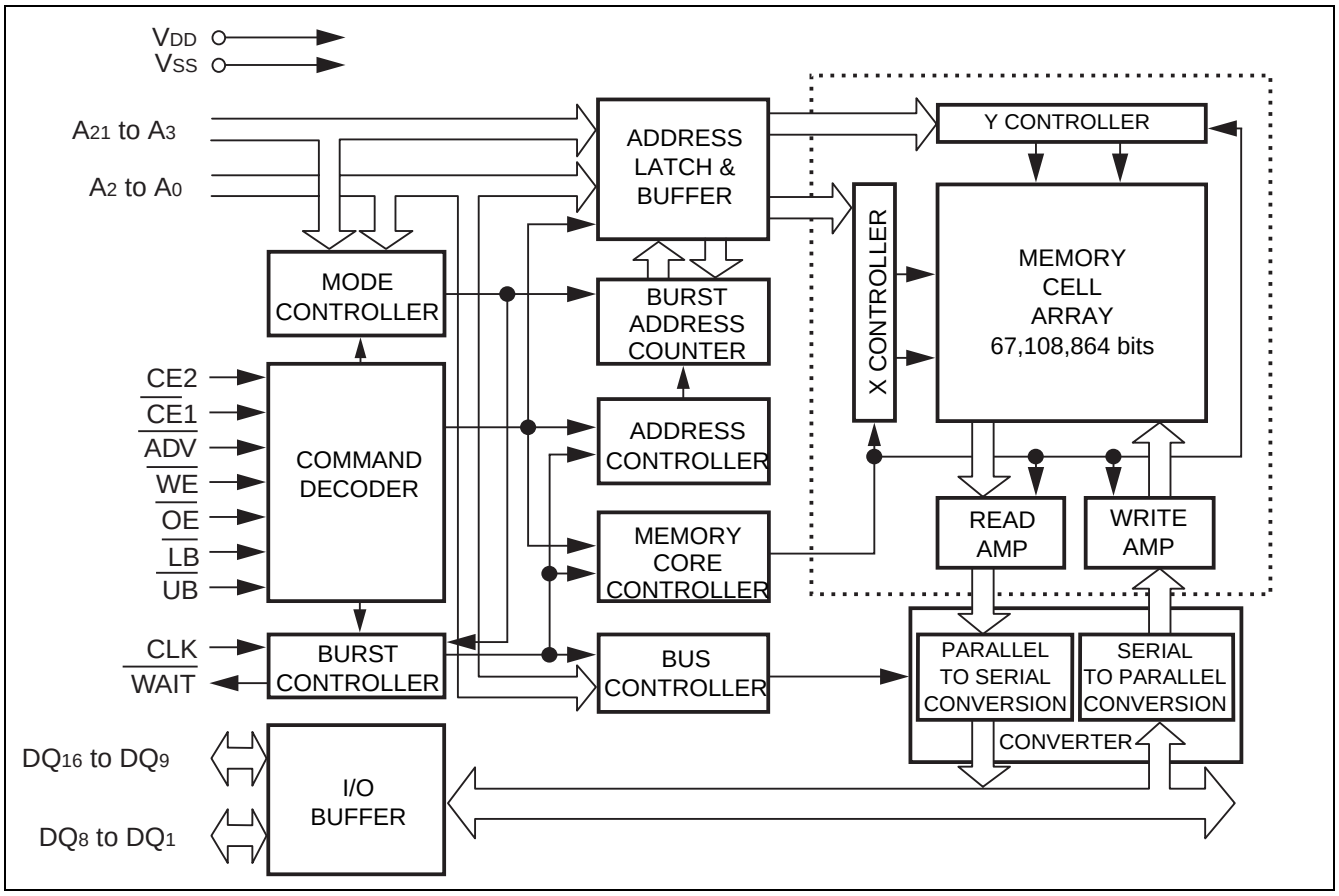
- Asynchronous SRAM Interface
- Fast Access Time : t_{CE} = 70 ns Max
- 8 words Page Access Capability : t_{PAA} = 20 ns Max
- Burst Read/Write Access Capability : t_{AC} = 10 ns Max
- Low Voltage Operating Condition : V_{DD} = 1.7 V to 1.95 V
- Wide Operating Temperature : T_A = -30 °C to +85 °C
- Byte Control by $\overline{LB}$ and $\overline{UB}$
- Low-Power Consumption : I_{DDA1} = 35 mA Max
  I_{DDS1} = 90 µA Max ($T_A \leq +40$°C)
- Various Power Down mode : Sleep
  8 M-bit Partial
  16 M-bit Partial
- Shipping Form : Wafer/Chip

■ PIN DESCRIPTION

Pin Name	Description
A_{21} to A_0	Address Input
$\overline{CE1}$	Chip Enable 1 (Low Active)
CE2	Chip Enable 2(High Active)
$\overline{WE}$	Write Enable (Low Active)
$\overline{OE}$	Output Enable (Low Active)
$\overline{LB}$	Lower Byte Control (Low Active)
$\overline{UB}$	Upper Byte Control (Low Active)
CLK	Clock Input
$\overline{ADV}$	Address Valid Input (Low Active)
$\overline{WAIT}$	Wait Output
DQ_8 to DQ_1	Lower Byte Data Input/Output
DQ_{16} to DQ_9	Upper Byte Data Input/Output
V_{DD}	Power Supply Voltage
V_{SS}	Ground

Note : Refer to "■PACKAGE FOR ENGINEERING SAMPLES" for additional pin descriptions of FBGA package supply.

■ BLOCK DIAGRAM



■ FUNCTION TRUTH TABLE

1. Asynchronous Operation (Page Mode)

Mode	CE2	$\overline{CE}$1	CLK	$\overline{ADV}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	A_{21} to A_0	DQ_8 to DQ_1	DQ_{16} to DQ_9	$\overline{WAIT}$
Standby (Deselect)	H	H	X	X	X	X	X	X	X	High-Z	High-Z	High-Z
Output Disable*1	H	L	X	*3	H	H	X	X	*5	High-Z	High-Z	High-Z
Output Disable (No Read)			X	*3	H	L	H	H	Valid	High-Z	High-Z	High-Z
Read (Upper Byte)			X	*3			H	L	Valid	High-Z	Output Valid	High-Z
Read (Lower Byte)			X	*3			L	H	Valid	Output Valid	High-Z	High-Z
Read (Word)			X	*3			L	L	Valid	Output Valid	Output Valid	High-Z
Page Read			X	*3			L/H	L/H	Valid	*6	*6	High-Z
No Write			X	*3	L	H*4	H	H	Valid	Invalid	Invalid	High-Z
Write (Upper Byte)			X	*3			H	L	Valid	Invalid	Input Valid	High-Z
Write (Lower Byte)			X	*3			L	H	Valid	Input Valid	Invalid	High-Z
Write (Word)			X	*3			L	L	Valid	Input Valid	Input Valid	High-Z
Power Down*2	L	X	X	X	X	X	X	X	X	High-Z	High-Z	High-Z

Note : L = V_{IL}, H = V_{IH}, X can be either V_{IL} or V_{IH}, High-Z = High Impedance

*1 : Should not be kept this logic condition longer than 1 μs.

*2 : Power Down mode can be entered from Standby state and all output are in High-Z state.
Data retention depends on the selection of Partial Size for Power Down Program.
Refer to "Power Down" in "■FUNCTIONAL DESCRIPTION" for the details.

*3 : "L" for address pass through and "H" for address latch on the rising edge of $\overline{ADV}$.

*4 : $\overline{OE}$ can be V_{IL} during write operation if the following conditions are satisfied;
(1) Write pulse is initiated by $\overline{CE}$1. See "(14) Asynchronous Read/Write Timing 1-1 ($\overline{CE}$1 Control)" in "■TIMING DIAGRAMS".
(2) $\overline{OE}$ stays V_{IL} during Write cycle.

*5 : Can be either V_{IL} or V_{IH} but must be valid before Read or Write.

*6 : Output of upper and lower byte data is either Valid or High-Z depending on the level of $\overline{LB}$ and $\overline{UB}$ input.

2. Synchronous Operation (Burst Mode)

Mode	CE2	$\overline{CE1}$	CLK	$\overline{ADV}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	A_{21} to A_0	DQ_8 to DQ_1	DQ_{16} to DQ_9	$\overline{WAIT}$
Standby(Deselect)	H	H	X	X	X	X	X	X	X	High-Z	High-Z	High-Z
Start Address Latch*1		L	↑ *3	↓↑	X*4	X*4	X*6	X*6	Valid*7	High-Z*8	High-Z*8	High-Z*11
Advance Burst Read to Next Address*1			↑ *3	H	H	L			X	Output Valid*9	Output Valid*9	Output Valid
Burst Read Suspend*1			↑ *3			H				High-Z	High-Z	High*12
Advance Burst Write to Next Address*1			↑ *3		L*5	H				Input Valid*10	Input Valid*10	High*13
Burst Write Suspend*1			↑ *3		H*5					Input Invalid	Input Invalid	High*12
Terminate Burst Read		↑	X		H	X				High-Z	High-Z	High-Z
Terminate Burst Write		↑	X		X	H				High-Z	High-Z	High-Z
Power Down*2	L	X	X	X	X	X	X	X	X	High-Z	High-Z	High-Z

Note : L = V_{IL}, H = V_{IH}, X can be either V_{IL} or V_{IH}, ↑ = valid edge, ↓↑ = rising edge of Low pulse, High-Z = High impedance

*1 : Should not be kept this logic condition longer than 4 µs.

*2 : Power Down mode can be entered from Standby state and all output are in High-Z state. Data retention depends on the selection of Partial Size for Power Down Program. Refer to "Power Down" in "■FUNCTIONAL DESCRIPTION" for the details.

*3 : Valid clock edge shall be set on either rising or falling edge through CR set. CLK must be started and stable prior to memory access.

*4 : Can be either V_{IL} or V_{IH} except for the case the both of $\overline{OE}$ and $\overline{WE}$ are V_{IL}. It is prohibited to bring the both of $\overline{OE}$ and $\overline{WE}$ to V_{IL}.

*5 : When device is operating in "$\overline{WE}$ Single Clock Pulse Control" mode, $\overline{WE}$ is don't care once write operation is determined by $\overline{WE}$ Low Pulse at the beginning of write access together with address latching. Burst write suspend feature is not supported in "$\overline{WE}$ Single Clock Pulse Control" mode.

*6 : Can be either V_{IL} or V_{IH} but must be valid before Read or Write is determined. And once $\overline{LB}$ and $\overline{UB}$ input levels are determined, they must not be changed until the end of burst.

*7 : Once valid address is determined, input address must not be changed during $\overline{ADV}$ = L.

*8 : If $\overline{OE}$ = L, output is either Invalid or High-Z depending on the level of $\overline{LB}$ and $\overline{UB}$ input. If $\overline{WE}$ = L, input is Invalid. If $\overline{OE}$ = $\overline{WE}$ = H, output is High-Z.

*9 : Outputs is either Valid or High-Z depending on the level of $\overline{LB}$ and $\overline{UB}$ input.

*10 : Input is either Valid or Invalid depending on the level of $\overline{LB}$ and $\overline{UB}$ input.

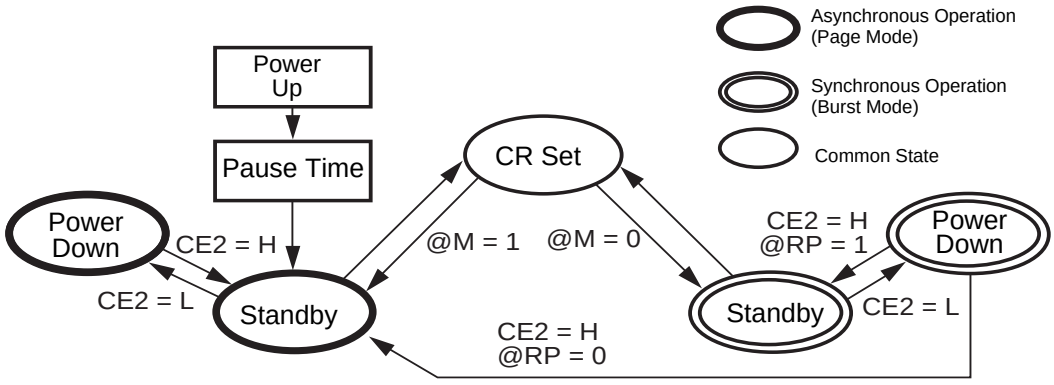
*11 : Output is either High-Z or Invalid depending on the level of $\overline{OE}$ and $\overline{WE}$ input.

*12 : Keep the level from previous cycle except for suspending on last data. Refer to "$\overline{WAIT}$ Output Function" in "■FUNCTIONAL DESCRIPTION" for the details.

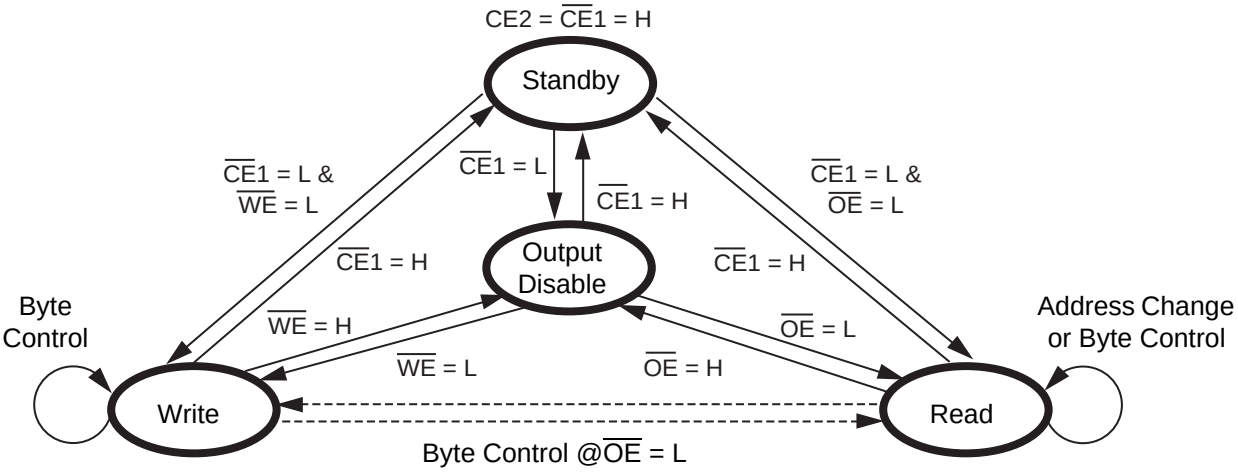
*13 : $\overline{WAIT}$ output is driven in High level during burst write operation.

■ STATE DIAGRAM

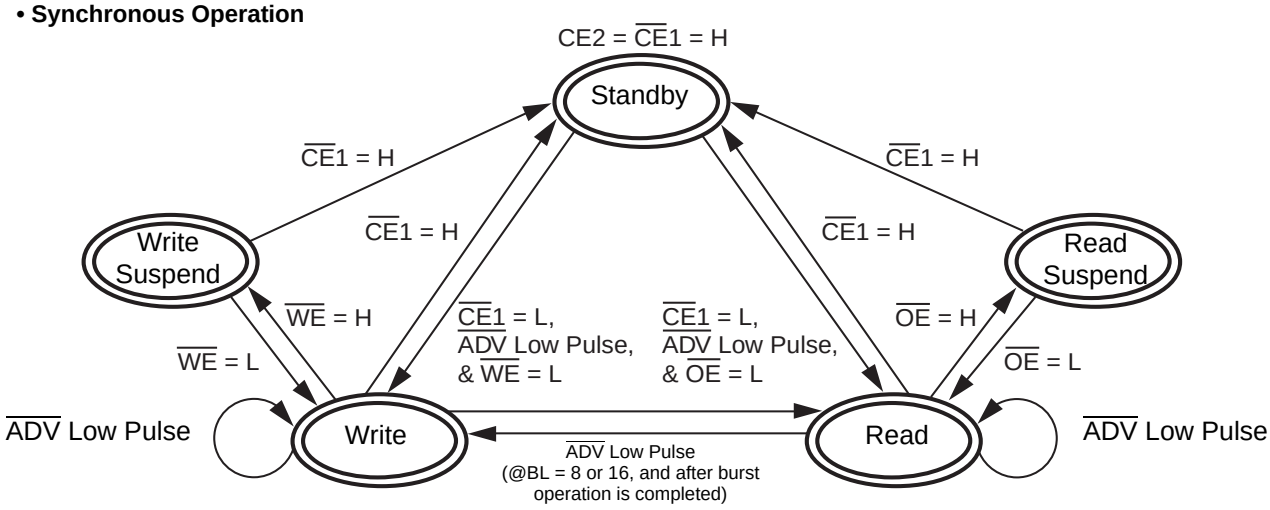
• Initial/Standby State



• Asynchronous Operation



• Synchronous Operation



Note : Assuming all the parameters specified in AC CHARACTERISTICS are satisfied. Refer to the "■FUNCTIONAL DESCRIPTION", "2. AC Characteristics" in "■ELECTRICAL CHARACTERISTICS", and "■TIMING DIAGRAMS" for details.

■ FUNCTIONAL DESCRIPTION

This device supports asynchronous read, page read & normal write operation and synchronous burst read and burst write operation for faster memory access and features three kinds of power down modes for power saving as user configurable option.

• Power-up

It is required to follow the power-up timing to start executing proper device operation. Refer to "Power-up Timing". After Power-up, the device defaults to asynchronous page read & normal write operation mode with sleep power down feature.

• Configuration Register

The Configuration Register(CR) is used to configure the type of device function among optional features. Each selection of features is set through CR set sequence after power-up. If CR set sequence is not performed after power-up, the device is configured for asynchronous operation with sleep power down feature as default configuration.

• CR Set Sequence

The CR set requires total 6 read/write cycles with unique address. Operation other than read/write operation requires that device being in standby mode. Following table shows the detail sequence.

Cycle #	Operation	Address	Data
#1	Read	3FFFFFh (MSB)	Read Data (RDa)
#2	Write	3FFFFFh	RDa
#3	Write	3FFFFFh	RDa
#4	Write	3FFFFFh	X
#5	Write	3FFFFFh	X
#6	Read	Address Key	Read Data (RDb)

The first cycle is to read from most significant address(MSB).
The second and third cycles are to write to MSB. If the second or third cycle is written into the different address, the CR set is cancelled and the data written by the second or third cycle is valid as a normal write operation. It is recommended to write back the data(RDa) read by first cycle to MSB in order to secure the data.
The forth and fifth cycles are to write to MSB. The data of forth and fifth cycles is don't-care. If the forth or fifth cycle is written into different address, the CR set is also cancelled, but write data may not be written as normal write operation.
The last cycle is to read from specific address key for mode selection. And read data(RDb) is invalid.

Once this CR set sequence is performed from an initial CR set to the other new CR set, the written data stored in memory cell array may be lost. So, it should perform the CR set sequence prior to regular read/write operation if necessary to change from default configuration.

• **Address Key**

The address key has the following format.

Address Pin	Register Name	Function	Key	Description	Note
A_{21}	—	—	1	Unused bits must be 1	*1
A_{20}, A_{19}	PS	Partial Size	00	16 M-bit Partial	
			01	8 M-bit Partial	
			10	Reserved for future use	*2
			11	Sleep [Default]	
A_{18} to A_{16}	BL	Burst Length	000	Reserved for future use	*2
			001	Reserved for future use	*2
			010	8 words	
			011	16 words	
			100	Reserved for future use	*2
			101	Reserved for future use	*2
			110	Reserved for future use	*2
			111	Continuous	*3
A_{15}	M	Mode	0	Synchronous Mode (Burst Read / Write)	*4
			1	Asynchronous Mode [Default] (Page Read / Normal Write)	*5
A_{14} to A_{12}	RL	Read Latency	000	Reserved for future use	*2
			001	3 clocks	
			010	4 clocks	
			011	5 clocks	
			1xx	Reserved for future use	*2
A_{11}	BS	Burst Sequence	0	Reserved for future use	*2
			1	Sequential	
A_{10}	SW	Single Write	0	Burst Read & Burst Write	
			1	Burst Read & Single Write	*6
A_9	VE	Valid Clock Edge	0	Falling Clock Edge	
			1	Rising Clock Edge	
A_8	RP	Reset to Page	0	Reset to Page mode	*7
			1	Remain the previous mode	
A_7	WC	Write Control	0	$\overline{WE}$ Single Clock Pulse Control without Write Suspend Function	*6
			1	$\overline{WE}$ Level Control with Write Suspend Function	
A_6 to A_0	—	—	1	Unused bits must be 1	*1

*1: A_{21} and A_6 to A_0 must be all "1" in any cases.

*2: It is prohibited to apply this key.

*3: Please contact local FUJITSU representative for the use of BL = continuous option.

*4: If M = 0, all the registers must be set with appropriate Key input at the same time.

*5: If M = 1, PS must be set with appropriate Key input at the same time. Except for PS, all the other key inputs must be "1".

*6: Burst Read & Single Write is not supported at $\overline{WE}$ Single Clock Pulse Control.

*7: Effective only when PS = 11.

- **Power Down**

  The Power Down is low power idle state controlled by CE2. CE2 Low drives the device in power down mode and maintains low power idle state as long as CE2 is kept Low. CE2 High resumes the device from power down mode.

  This device has three power down modes, Sleep, 8 M-bit Partial, and 16 M-bit Partial.

  The selection of power down mode is set through CR set sequence. Each mode has following data retention features.

Mode	Data Retention Size	Retention Address
Sleep [default]	No	N/A
8 M-bit Partial	8 M bits	000000h to 07FFFFh
16 M-bit Partial	16 M bits	000000h to 0FFFFFh

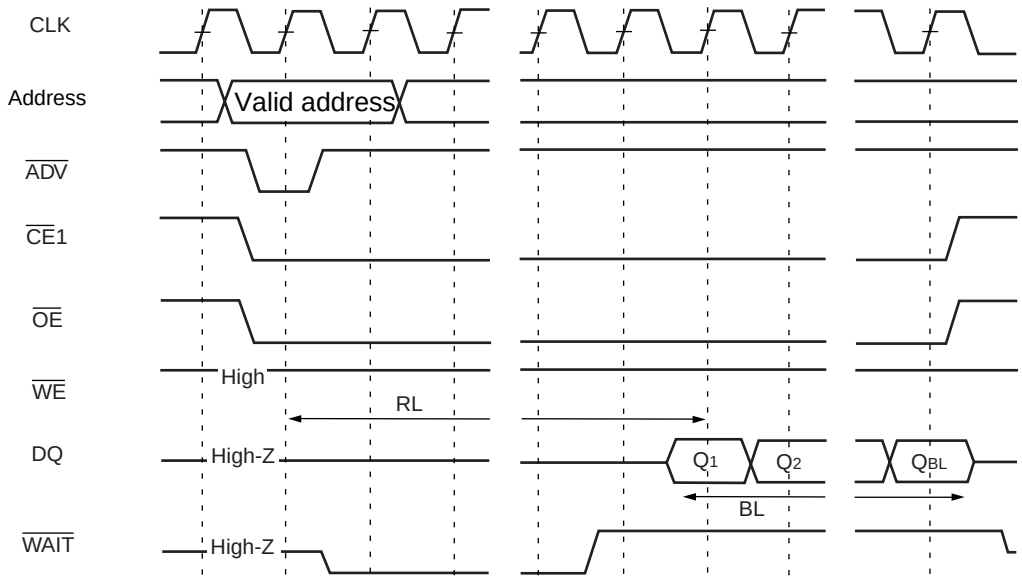
  The default state after power-up is Sleep and it is the lowest power consumption but all data will be lost once CE2 is brought to Low for Power Down. It is not required to perform CR set sequence to set to Sleep mode after power-up in case of asynchronous operation.

  When RP = 0, Power Down comprehends a function to reset the device to default configuration(asynchronous mode). After resuming from power down mode, the device is back in page mode of default configurations. This is effective only when PS is set on sleep mode. When Partial mode is selected, RP = 0 is not effective.

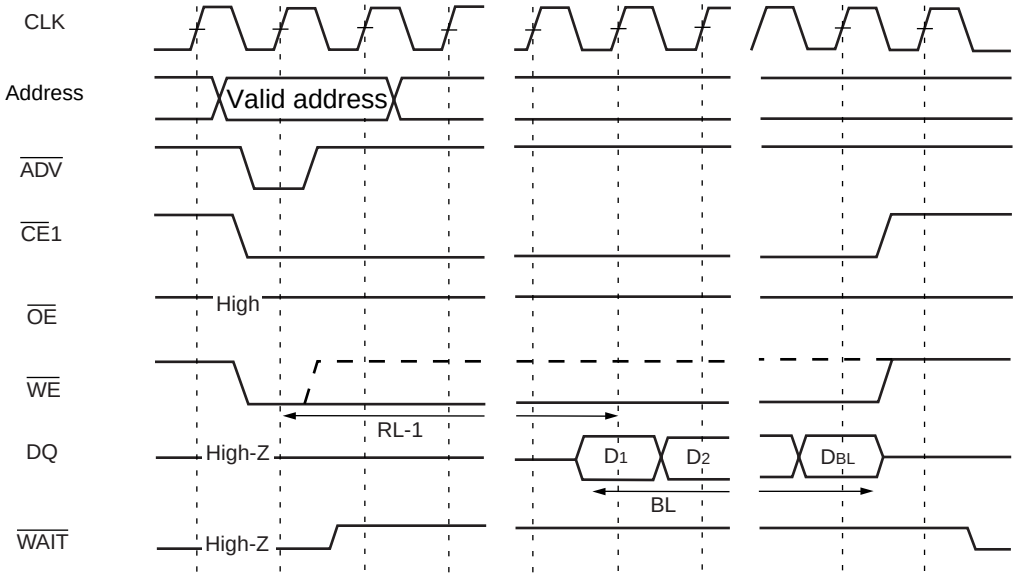
- **Burst Read/Write Operation**

  Synchronous burst read/write operation provides faster memory access that synchronized to microcontroller or system bus frequency. Configuration Register(CR) Set is required to perform burst read & write operation after power-up. Once CR set sequence is performed to select synchronous burst mode, the device is configured to synchronous burst read/write operation mode with corresponding RL and BL that is set through CR set sequence together with operation mode. In order to perform synchronous burst read & write operation, it is required to control new signals, CLK, $\overline{\text{ADV}}$ and $\overline{\text{WAIT}}$ that Low Power SRAMs don't have.

• Burst Read Operation



• Burst Write Operation



• CLK Input Function

The CLK is input signal to synchronize memory to microcontroller or system bus frequency during synchronous burst read & write operation. The CLK input increments device internal address counter and the valid edge of CLK is referred for latency counts from address latch, burst write data latch, and burst read data output. During synchronous operation mode, CLK input must be supplied except for standby state and power down state. CLK is don't care during asynchronous operation.

- **$\overline{\text{ADV}}$ Input Function**

  The $\overline{\text{ADV}}$ is input signal to latch valid address. It is applicable to synchronous operation as well as asynchronous operation. $\overline{\text{ADV}}$ input is active during $\overline{\text{CE}}$1 = L and $\overline{\text{CE}}$1 = H disables $\overline{\text{ADV}}$ input. All addresses are determined on the rising edge of $\overline{\text{ADV}}$.

  During synchronous burst read/write operation, $\overline{\text{ADV}}$ = H disables all address inputs. Once $\overline{\text{ADV}}$ is brought to High after valid address latch, it is inhibited to bring $\overline{\text{ADV}}$ Low until the end of burst or until burst operation is terminated. $\overline{\text{ADV}}$ Low pulse is mandatory for synchronous burst read/write operation mode to latch the valid address input.

  During asynchronous operation, $\overline{\text{ADV}}$ = H also disables all address inputs. $\overline{\text{ADV}}$ can be tied to Low during asynchronous operation and it is not necessary to control $\overline{\text{ADV}}$ to High.

- **$\overline{\text{WAIT}}$ Output Function**

  The $\overline{\text{WAIT}}$ is output signal to indicate data bus status when the device is operating in synchronous burst mode.

  During burst read operation, $\overline{\text{WAIT}}$ output is enabled after specified time duration from $\overline{\text{OE}}$ = L or $\overline{\text{CE}}$1 = L whichever occurs last. $\overline{\text{WAIT}}$ output Low indicates data output at next clock cycle is invalid, and $\overline{\text{WAIT}}$ output becomes High one clock cycle prior to valid data output. During $\overline{\text{OE}}$ read suspend, $\overline{\text{WAIT}}$ output doesn't indicate data bus status but carries the same level from previous clock cycle (kept High) except for burst read suspend on the final data output. If final read data output is suspended, $\overline{\text{WAIT}}$ output becomes high impedance after specified time duration from $\overline{\text{OE}}$ = H.

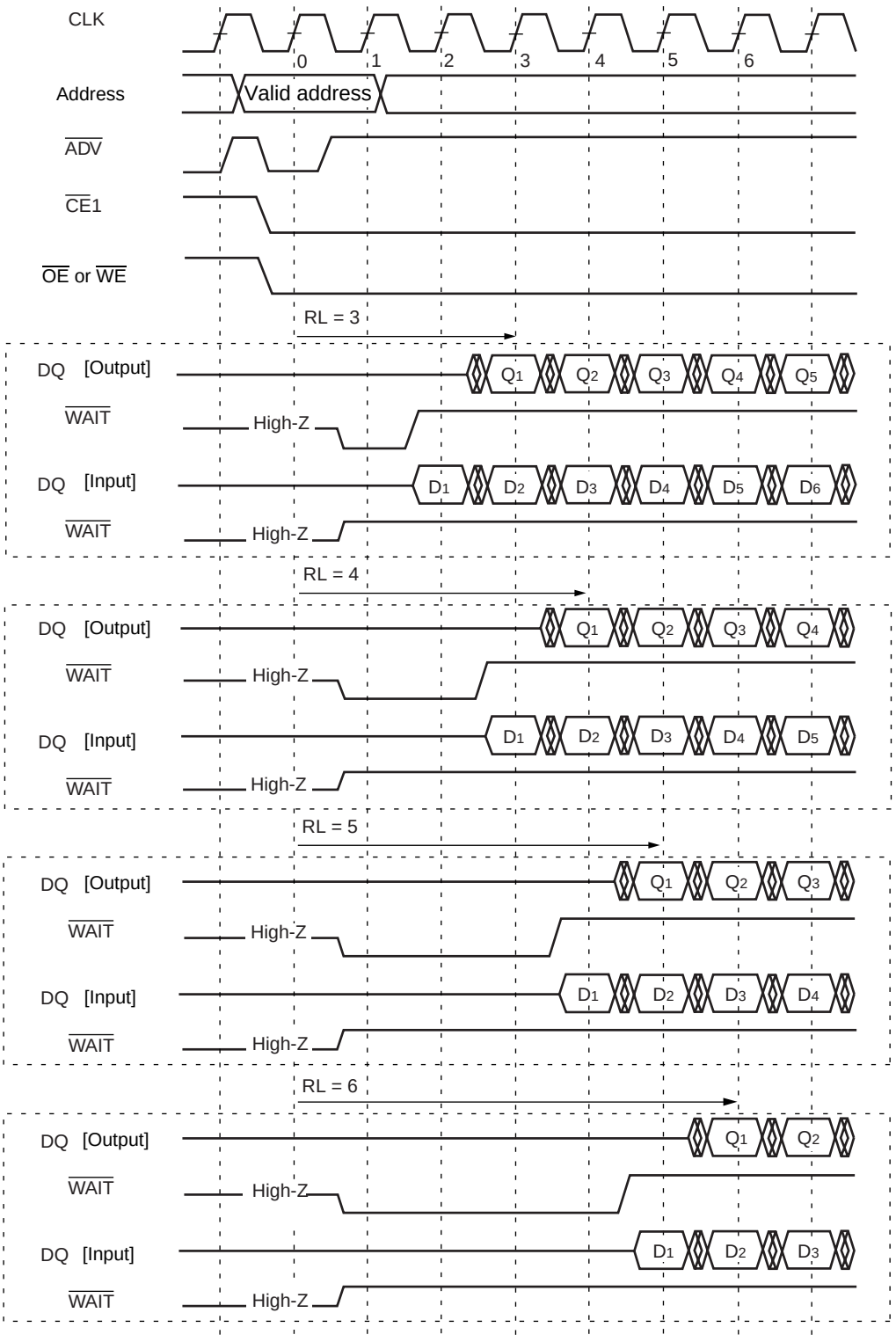
  During burst write operation, $\overline{\text{WAIT}}$ output is valid to High level after specified time duration from $\overline{\text{WE}}$ = L or $\overline{\text{CE}}$1 = L whichever occurs last and kept High for entire write cycles including $\overline{\text{WE}}$ write suspend. The actual write data latching starts on the appropriate clock edge with respect to Valid Clock Edge, Read Latency, and Burst Length. During $\overline{\text{WE}}$ write suspend, $\overline{\text{WAIT}}$ output doesn't indicate data bus status but carries the same level from previous clock cycle (kept High) except for write suspend on the final data input. If final write data input is suspended, $\overline{\text{WAIT}}$ output becomes high impedance after specified time duration from $\overline{\text{WE}}$ = H.

  This device doesn't incur additional output delay against crossing device-row boundary or internal refresh operation. Therefore, the burst operation is always started after fixed latency with respect to read latency. And there is no waiting cycle asserted in the middle of burst operation except for burst read or write suspend by $\overline{\text{OE}}$ brought to High or $\overline{\text{WE}}$ brought to High. Thus, once $\overline{\text{WAIT}}$ output is enabled and brought to High, $\overline{\text{WAIT}}$ output keeps High level until the end of burst or until the burst operation is terminated.

  When the device is operating in asynchronous mode, $\overline{\text{WAIT}}$ output is always in High Impedance.

- **Latency**

  Read Latency (RL) is the number of clock cycles between the address being latched and first read data becoming available during synchronous burst read operation. It is set through CR set sequence after power-up. Once specific RL is set through CR set sequence, write latency, that is the number of clock cycles between address being latched and first write data being latched, is automatically set to RL-1. The burst operation is always started after fixed latency with respect to Read Latency set in CR.


CLK
0
1
2
3
4
5
6
Address
Valid address
ADV
CE1
OE or WE
RL = 3
DQ [Output]
Q1
Q2
Q3
Q4
Q5
WAIT
High-Z
DQ [Input]
D1
D2
D3
D4
D5
D6
WAIT
High-Z
RL = 4
DQ [Output]
Q1
Q2
Q3
Q4
WAIT
High-Z
DQ [Input]
D1
D2
D3
D4
D5
WAIT
High-Z
RL = 5
DQ [Output]
Q1
Q2
Q3
WAIT
High-Z
DQ [Input]
D1
D2
D3
D4
WAIT
High-Z
RL = 6
DQ [Output]
Q1
Q2
WAIT
High-Z
DQ [Input]
D1
D2
D3
WAIT
High-Z

- **Address Latch by $\overline{\text{ADV}}$**

  The $\overline{\text{ADV}}$ latches valid address presence on address inputs. During synchronous burst read/write operation mode, all the address are determined on the rising edge of $\overline{\text{ADV}}$ when $\overline{\text{CE}}$1 = L. The specified minimum value of $\overline{\text{ADV}}$ = L setup time and hold time against valid edge of clock where RL count is begun must be satisfied. Valid address must be determined with specified setup time against either the falling edge of $\overline{\text{ADV}}$ or falling edge of $\overline{\text{CE}}$1 whichever comes late. And the determined valid address must not be changed during $\overline{\text{ADV}}$ = L period.

- **Burst Length**

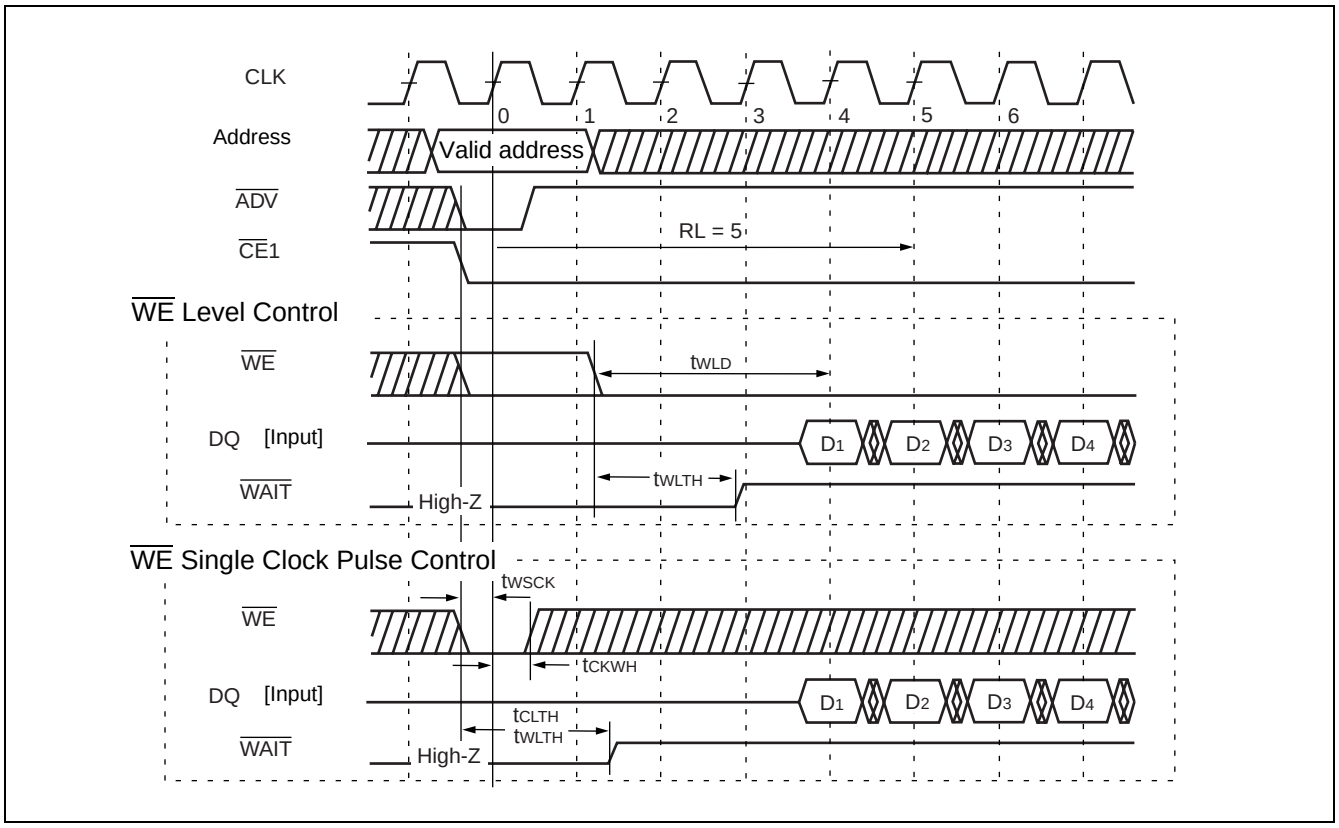
  Burst Length is the number of word to be read or written during synchronous burst read/write operation as the result of a single address latch cycle. It can be set on 8,16 words boundary or continuous for entire address through CR set sequence. The burst type is sequential that is incremental decoding scheme within a boundary address. Starting from initial address being latched, device internal address counter assigns +1 to the previous address until reaching the end of boundary address and then wrap round to least significant address (= 0). After completing read data output or write data latch for the set burst length, operation automatically ended except for continuous burst length. When continuous burst length is set, read/write is endless unless it is terminated by the rising edge of $\overline{\text{CE}}$1.

- **Single Write**

  Single write is synchronous write operation with Burst Length = 1. The device can be configured either to "Burst Read & Single Write" or to "Burst Read & Burst Write" through CR set sequence. Once the device is configured to "Burst Read & Single Write" mode, the burst length for synchronous write operation is always fixed 1 regardless of BL values set in CR, while burst length for read is in accordance with BL values set in CR.

- **Write control**

The device has two types of $\overline{WE}$ signal control method, "$\overline{WE}$ Level Control" and "$\overline{WE}$ Single Clock Pulse Control", for synchronous burst write operation. It is configured through CR set sequence.

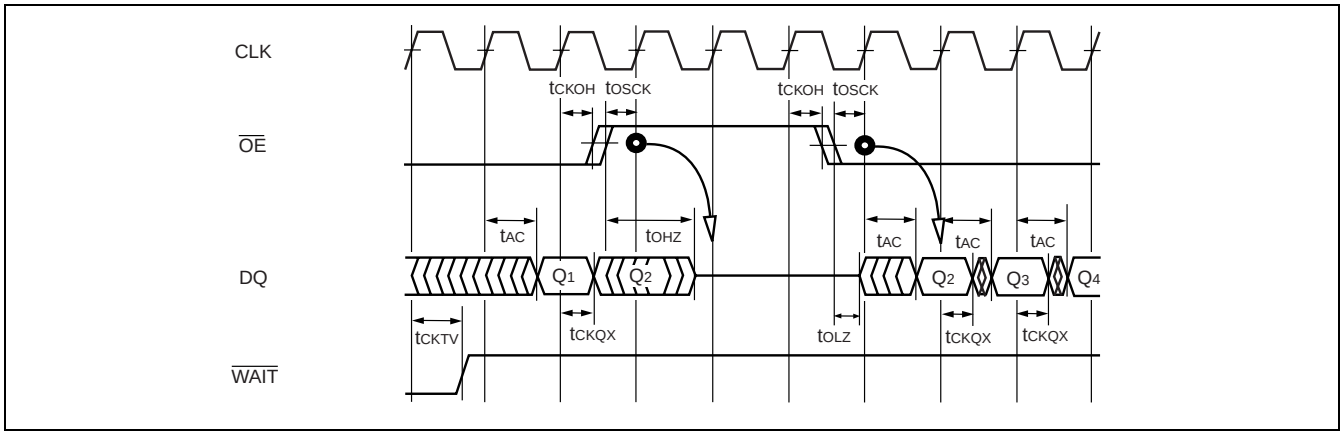


• **Burst Read Suspend**

Burst read operation can be suspended by $\overline{OE}$ High pulse. During burst read operation, $\overline{OE}$ brought to High from Low suspends burst read operation. Once $\overline{OE}$ is brought to High with the specified setup time against clock where the data being suspended, the device internal counter is suspended, and the data output becomes high impedance after specified time duration. It is inhibited to suspend the first data output at the beginning of burst read.

$\overline{OE}$ brought to Low from High resumes burst read operation. Once $\overline{OE}$ is brought to Low, data output becomes valid after specified time duration, and internal address counter is reactivated. The last data output being suspended as the result of $\overline{OE}$ = H and first data output as the result of $\overline{OE}$ = L are from the same address.

In order to guarantee to output last data before suspension and first data after resumption, the specified minimum value of $\overline{OE}$ hold time and setup time against clock edge must be satisfied respectively.



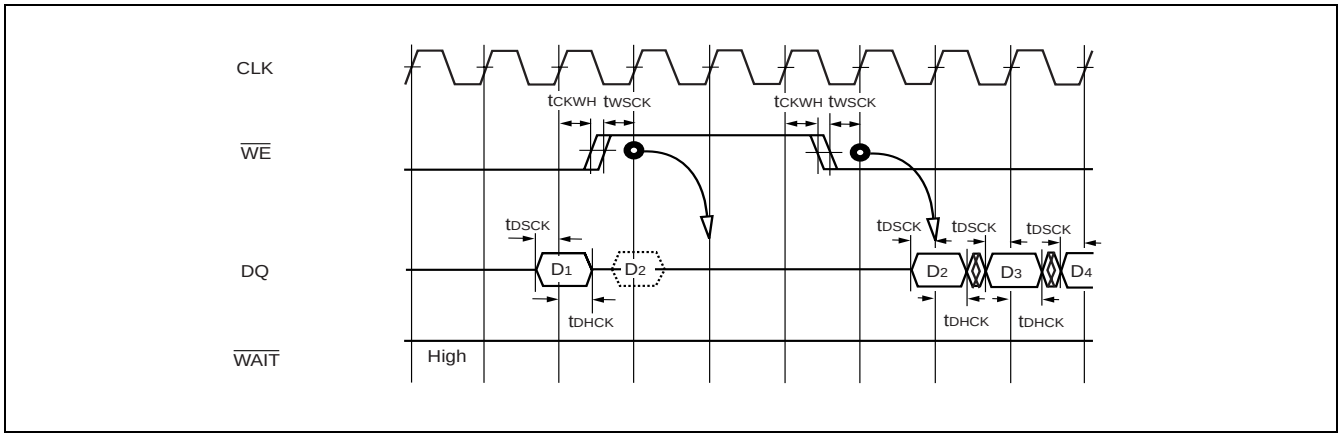
• **Burst Write Suspend**

Burst write operation can be suspended by $\overline{WE}$ High pulse. During burst write operation, $\overline{WE}$ brought to High from Low suspends burst write operation. Once $\overline{WE}$ is brought to High with the specified setup time against clock where the data being suspended, device internal counter is suspended, data input is ignored. It is inhibited to suspend the first data input at the beginning of burst write.

$\overline{WE}$ brought to Low from High resumes burst write operation. Once $\overline{WE}$ is brought to Low, data input becomes valid after specified time duration, and internal address counter is reactivated. The write address of the cycle where data being suspended and the first write address as the result of $\overline{WE}$ = L are the same address.

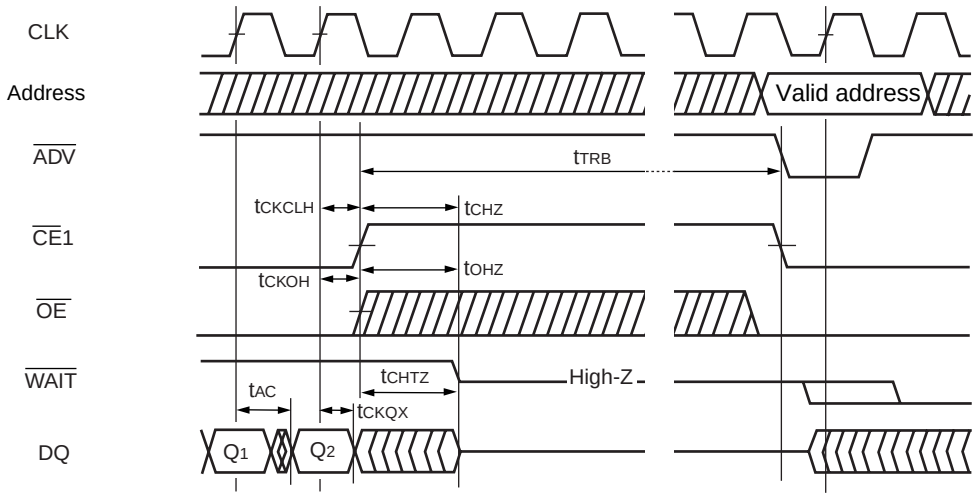
In order to guarantee to latch the last data input before suspension and first data input after resumption, the specified minimum value of $\overline{WE}$ hold time and setup time against clock edge must be satisfied respectively.

Burst write suspend function is available when the device is operating in $\overline{WE}$ level controlled burst write only.



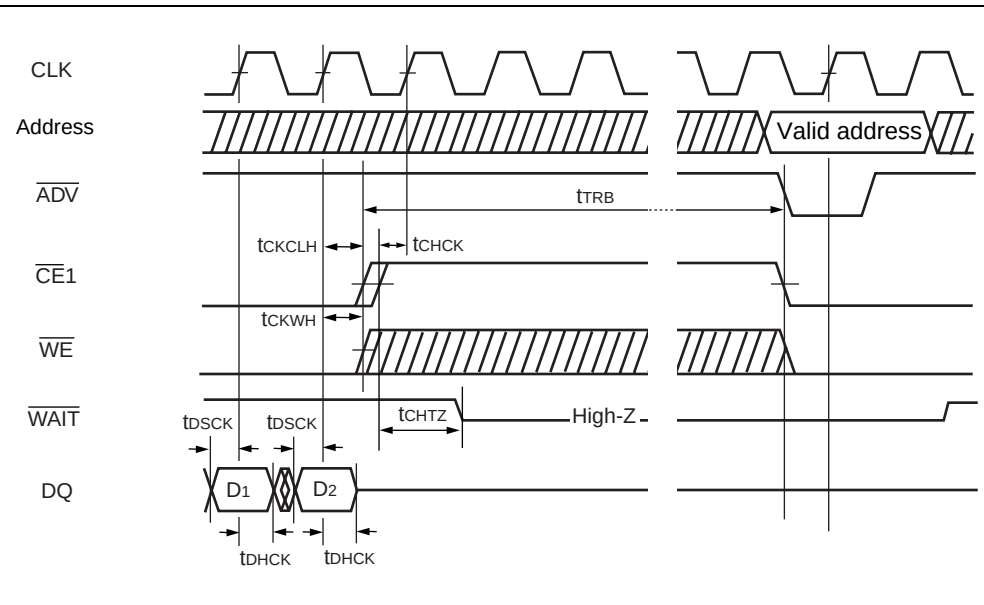
• **Burst Read Termination**

Burst read operation can be terminated by $\overline{CE}1$ brought to High. If BL is set on Continuous, burst read operation is continued endless unless terminated by $\overline{CE}1$ = H. It is inhibited to terminate burst read before first data output is completed. In order to guarantee last data output, the specified minimum value of $\overline{CE}1$ = L hold time from clock edge must be satisfied. After termination, the specified minimum recovery time (t_{TRB}) is required to start new access.



• **Burst Write Termination**

Burst write operation can be terminated by $\overline{CE}1$ brought to High. If BL is set on Continuous, burst write operation is continued endless unless terminated by $\overline{CE}1$ = H. It is inhibited to terminate burst write before first data input is completed. In order to guarantee last data input being latched, the specified minimum values of $\overline{CE}1$ = L hold time from clock edge must be satisfied. After termination, the specified minimum recovery time (t_{TRB}) is required to start new access.



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Voltage of V_{DD} Supply Relative to V_{SS} *	V_{DD}	− 0.5	+ 3.6	V
Voltage at Any Pin Relative to V_{SS} *	V_{IN}, V_{OUT}	− 0.5	+ 3.6	V
Short Circuit Output Current *	I_{OUT}	− 50	+ 50	mA
Storage Temperature	Tstg	− 55	+ 125	°C

* : All voltages are referenced to V_{SS} = 0 V.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value		Unit
		Min	Max	
Power Supply Voltage*1	V_{DD}	1.7	1.95	V
	V_{SS}	0	0	V
High Level Input Voltage*1, *2	V_{IH}	$V_{DD} \times 0.8$	$V_{DD} + 0.2$	V
Low Level Input Voltage*1, *3	V_{IL}	− 0.3	$V_{DD} \times 0.2$	V
Ambient Temperature	T_A	− 30	+ 85	°C

*1 : All voltages are referenced to V_{SS} = 0 V.

*2 : Maximum DC voltage on input and I/O pins is V_{DD} + 0.2 V. During voltage transitions, inputs may overshoot to V_{DD} + 1.0 V for periods of up to 5 ns.

*3 : Minimum DC voltage on input or I/O pins is -0.3 V. During voltage transitions, inputs may undershoot V_{SS} to -1.0 V for periods of up to 5 ns.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

(At recommended operating conditions unless otherwise noted)

Parameter	Symbol	Test Conditions		Value		Unit
				Min	Max	
Input Leakage Current	I_{LI}	$V_{SS} \le V_{IN} \le V_{DD}$		–1.0	+1.0	µA
Output Leakage Current	I_{LO}	0 V ≤ V_{OUT} ≤ V_{DD}, Output High Impedance		–1.0	+1.0	µA
Output High Voltage Level	V_{OH}	$V_{DD} = V_{DD}$ (Min), I_{OH} = –0.5 mA		1.4	—	V
Output Low Voltage Level	V_{OL}	I_{OL} = 1 mA		—	0.4	V
V_{DD} Power Down Current	I_{DDPS}	$V_{DD} = V_{DD}$ (Max), $V_{IN} = V_{IH}$ or V_{IL}, CE2 ≤ 0.2 V	SLEEP	—	10	µA
	I_{DDP8}		8 M-bit Partial	—	80	µA
	I_{DDP16}		16 M-bit Partial	—	100	µA
V_{DD} Standby Current	I_{DDS}	$V_{DD} = V_{DD}$ (Max), V_{IN} (including CLK) = V_{IH} or V_{IL}, $\overline{CE}1$ = CE2 = V_{IH}		—	1.5	mA
	I_{DDS1}	$V_{DD} = V_{DD}$ (Max), V_{IN} (including CLK) ≤ 0.2 V or V_{IN} (including CLK) ≥ V_{DD} – 0.2 V, $\overline{CE}1$ = CE2 ≥ V_{DD} – 0.2 V	$T_A \le +85$ °C	—	170	µA
			$T_A \le +40$ °C	—	90	µA
	I_{DDS2}	$V_{DD} = V_{DD}$ (Max), t_{CK} = Min V_{IN} ≤ 0.2 V or V_{IN} ≥ V_{DD} – 0.2 V, $\overline{CE}1$ = CE2 ≥ V_{DD} – 0.2 V		—	220	µA
V_{DD} Active Current	I_{DDA1}	$V_{DD} = V_{DD}$ (Max), $V_{IN} = V_{IH}$ or V_{IL}, $\overline{CE}1 = V_{IL}$ and CE2 = V_{IH}, I_{OUT} = 0 mA	t_{RC}/t_{WC} = Min	—	35	mA
	I_{DDA2}		t_{RC}/t_{WC} = 1 µs	—	5	mA
V_{DD} Page Read Current	I_{DDA3}	$V_{DD} = V_{DD}$ (Max), $V_{IN} = V_{IH}$ or V_{IL}, $\overline{CE}1 = V_{IL}$ and CE2 = V_{IH}, I_{OUT} = 0 mA, t_{PRC} = Min		—	10	mA
V_{DD} Burst Access Current	I_{DDA4}	$V_{DD} = V_{DD}$ (Max), $V_{IN} = V_{IH}$ or V_{IL}, $\overline{CE}1 = V_{IL}$ and CE2 = V_{IH}, $t_{CK} = t_{CK}$ (Min), BL = Continuous, I_{OUT} = 0 mA		—	25	mA

Notes :
- All voltages are referenced to V_{SS} = 0 V.
- DC characteristics are measured after following Power-up Timing.
- I_{OUT} depends on the output load conditions.

2. AC Characteristics

(1) Asynchronous Read Operation (Page mode)

(At recommended operating conditions unless otherwise noted)

Parameter	Symbol	Value		Unit	Notes
		Min	Max		
Read Cycle Time	t_{RC}	70	1000	ns	*1, *2
$\overline{CE}1$ Access Time	t_{CE}	—	70	ns	*3
$\overline{OE}$ Access Time	t_{OE}	—	40	ns	*3
Address Access Time	t_{AA}	—	70	ns	*3, *5
$\overline{ADV}$ Access Time	t_{AV}	—	70	ns	*3
$\overline{LB}$, $\overline{UB}$ Access Time	t_{BA}	—	30	ns	*3
Page Address Access Time	t_{PAA}	—	20	ns	*3, *6
Page Read Cycle Time	t_{PRC}	20	1000	ns	*1, *6, *7
Output Data Hold Time	t_{OH}	5	—	ns	*3
$\overline{CE}1$ Low to Output Low-Z	t_{CLZ}	5	—	ns	*4
$\overline{OE}$ Low to Output Low-Z	t_{OLZ}	10	—	ns	*4
$\overline{LB}$, $\overline{UB}$ Low to Output Low-Z	t_{BLZ}	0	—	ns	*4
$\overline{CE}1$ High to Output High-Z	t_{CHZ}	—	20	ns	*3
$\overline{OE}$ High to Output High-Z	t_{OHZ}	—	14	ns	*3
$\overline{LB}$, $\overline{UB}$ High to Output High-Z	t_{BHZ}	—	20	ns	*3
Address Setup Time to $\overline{CE}1$ Low	t_{ASC}	–5	—	ns	
Address Setup Time to $\overline{OE}$ Low	t_{ASO}	10	—	ns	
$\overline{ADV}$ Low Pulse Width	t_{VPL}	10	—	ns	*8
$\overline{ADV}$ High Pulse Width	t_{VPH}	15	—	ns	*8
Address Setup Time to $\overline{ADV}$ High	t_{ASV}	5	—	ns	
Address Hold Time from $\overline{ADV}$ High	t_{AHV}	5	—	ns	
Address Invalid Time	t_{AX}	—	10	ns	*5, *9
Address Hold Time from $\overline{CE}1$ High	t_{CHAH}	–5	—	ns	*10
Address Hold Time from $\overline{OE}$ High	t_{OHAH}	–5	—	ns	
$\overline{WE}$ High to $\overline{OE}$ Low Time for Read	t_{WHOL}	25	1000	ns	*11
$\overline{CE}1$ High Pulse Width	t_{CP}	15	—	ns	

*1 : Maximum value is applicable if $\overline{CE}1$ is kept at Low without change of address input of A_{21} to A_3.

*2 : Address should not be changed within minimum t_{RC}.

*3 : The output load 50 pF with 50 Ω termination to $V_{DD} \times 0.5$ V.

*4 : The output load 5 pF without any other load.

*5 : Applicable to A_{21} to A_3 when $\overline{CE}1$ is kept at Low.

*6 : Applicable only to A_2, A_1 and A_0 when $\overline{CE}1$ is kept at Low for the page address access.

(Continued)

(Continued)

*7 : In case Page Read Cycle is continued with keeping $\overline{CE}1$ stays Low, $\overline{CE}1$ must be brought to High within 4 µs. In other words, Page Read Cycle must be closed within 4 µs.

*8 : t_{VPL} is specified from the falling edge of either $\overline{CE}1$ or $\overline{ADV}$ whichever comes late. The sum of t_{VPL} and t_{VPH} must be equal or greater than t_{RC} for each access.

*9 : Applicable to address access when at least two of address inputs are switched from previous state.

*10 : t_{RC} (Min) and t_{PRC} (Min) must be satisfied.

*11 : If actual value of t_{WHOL} is shorter than specified minimum values, the actual t_{AA} of following Read may become longer by the amount of subtracting actual value from specified minimum value.

(2) Asynchronous Write Operation

(At recommended operating conditions unless otherwise noted)

Parameter	Symbol	Value		Unit	Notes
		Min	Max		
Write Cycle Time	t_{WC}	70	1000	ns	*1, *2
Address Setup Time	t_{AS}	0	—	ns	*3
$\overline{ADV}$ Low Pulse Width	t_{VPL}	10	—	ns	*4
$\overline{ADV}$ High Pulse Width	t_{VPH}	15	—	ns	*4
Address Setup Time to $\overline{ADV}$ High	t_{ASV}	5	—	ns	
Address Hold Time from $\overline{ADV}$ High	t_{AHV}	5	—	ns	
$\overline{CE}$1 Write Pulse Width	t_{CW}	45	—	ns	*3
$\overline{WE}$ Write Pulse Width	t_{WP}	45	—	ns	*3
$\overline{LB}$, $\overline{UB}$ Write Pulse Width	t_{BW}	45	—	ns	*3
$\overline{LB}$, $\overline{UB}$ Byte Mask Setup Time	t_{BS}	–5	—	ns	*5
$\overline{LB}$, $\overline{UB}$ Byte Mask Hold Time	t_{BH}	–5	—	ns	*6
Write Recovery Time	t_{WR}	0	—	ns	*7
$\overline{CE}$1 High Pulse Width	t_{CP}	15	—	ns	
$\overline{WE}$ High Pulse Width	t_{WHP}	15	1000	ns	
$\overline{LB}$, $\overline{UB}$ High Pulse Width	t_{BHP}	15	1000	ns	
Data Setup Time	t_{DS}	15	—	ns	
Data Hold Time	t_{DH}	0	—	ns	
$\overline{OE}$ High to $\overline{CE}$1 Low Setup Time for Write	t_{OHCL}	–5	—	ns	*8
$\overline{OE}$ High to Address Setup Time for Write	t_{OES}	0	—	ns	*9
$\overline{LB}$ and $\overline{UB}$ Write Pulse Overlap	t_{BWO}	30	—	ns	

*1 : Maximum value is applicable if $\overline{CE}$1 is kept at Low without any address change.

*2 : Minimum value must be equal or greater than the sum of write pulse width (t_{CW}, t_{WP} or t_{BW}) and write recovery time (t_{WR}).

*3 : Write pulse width is defined from High to Low transition of $\overline{CE}$1, $\overline{WE}$, $\overline{LB}$, or $\overline{UB}$, whichever occurs last.

*4 : t_{VPL} is specified from the falling edge of either $\overline{CE}$1 or $\overline{ADV}$ whichever comes late. The sum of t_{VPL} and t_{VPH} must be equal or greater than t_{WC} for each access.

*5 : Applicable for byte mask only. Byte mask setup time is defined from the High to Low transition of $\overline{CE}$1 or $\overline{WE}$ whichever occurs last.

*6 : Applicable for byte mask only. Byte mask hold time is defined from the Low to High transition of $\overline{CE}$1 or $\overline{WE}$ whichever occurs first.

*7 : Write recovery time is defined from Low to High transition of $\overline{CE}$1, $\overline{WE}$, $\overline{LB}$, or $\overline{UB}$, whichever occurs first.

*8 : If $\overline{OE}$ is Low after minimum t_{OHCL}, read cycle is initiated. In other word, $\overline{OE}$ must be brought to High within 5 ns after $\overline{CE}$1 is brought to Low.

*9 : If $\overline{OE}$ is Low after new address input, read cycle is initiated. In other word, $\overline{OE}$ must be brought to High at the same time or before new address is valid.

(3) Synchronous Operation - Clock Input (Burst mode)

(At recommended operating conditions unless otherwise noted)

Parameter		Symbol	Value		Unit	Notes
			Min	Max		
Clock Period	RL = 6	t_{CK}	13	—	ns	*1
	RL = 5		15	—	ns	*1
	RL = 4		18	—	ns	*1
	RL = 3		30	—	ns	*1
Clock High Pulse Width		t_{CKH}	4	—	ns	
Clock Low Pulse Width		t_{CKL}	4	—	ns	
Clock Transition Time		t_{CKT}	—	3	ns	*2

*1 : Clock period is defined between valid clock edges.

*2 : Clock transition time is defined between V_{IH} (Min) and V_{IL} (Max)

(4) Synchronous Operation - Address Latch (Burst mode)

(At recommended operating conditions unless otherwise noted)

Parameter		Symbol	Value		Unit	Notes
			Min	Max		
Address Setup Time to $\overline{CE}1$ Low		t_{ASCL}	–5	—	ns	*1
Address Setup Time to $\overline{ADV}$ Low		t_{ASVL}	–5	—	ns	*2
Address Hold Time from $\overline{ADV}$ High		t_{AHV}	5	—	ns	
$\overline{ADV}$ Low Pulse Width		t_{VPL}	10	—	ns	*3
$\overline{ADV}$ Low Setup Time to CLK	RL = 6, 5	t_{VSCK}	4	—	ns	*4
	RL = 4, 3	t_{VSCK}	7	—	ns	*4
$\overline{CE}1$ Low Setup Time to CLK	RL = 6, 5	t_{CLCK}	4	—	ns	*4
	RL = 4, 3	t_{CLCK}	7	—	ns	*4
$\overline{ADV}$ Low Hold Time from CLK		t_{CKVH}	1	—	ns	*4
Burst End $\overline{ADV}$ High Hold Time from CLK		t_{VHVL}	13	—	ns	

*1 : t_{ASCL} is applicable if $\overline{CE}1$ is brought to Low after $\overline{ADV}$ is brought to Low.

*2 : t_{ASVL} is applicable if $\overline{ADV}$ is brought to Low after $\overline{CE}1$ is brought to Low.

*3 : t_{VPL} is specified from the falling edge of either $\overline{CE}1$ or $\overline{ADV}$ whichever comes late.

*4 : Applicable to the 1st valid clock edge.

(5) Synchronous Read Operation (Burst mode)

(At recommended operating conditions unless otherwise noted)

Parameter		Symbol	Value		Unit	Notes
			Min	Max		
Burst Read Cycle Time		t_{RCB}	—	4000	ns	
Access Time from CLK	RL = 6, 5	t_{AC}	—	10	ns	*1
	RL = 4, 3	t_{AC}	—	12	ns	*1
Output Hold Time from CLK		t_{CKQX}	3	—	ns	*1
$\overline{CE}1$ Low to $\overline{WAIT}$ Low		t_{CLTL}	5	20	ns	*1
$\overline{OE}$ Low to $\overline{WAIT}$ Low		t_{OLTL}	0	20	ns	*1, *2
$\overline{ADV}$ Low to $\overline{WAIT}$ Low		t_{VLTL}	0	20	ns	*1
CLK to $\overline{WAIT}$ Valid Time		t_{CKTV}	—	10	ns	*1, *3
$\overline{WAIT}$ Valid Hold Time from CLK		t_{CKTX}	3	—	ns	*1
$\overline{CE}1$ Low to Output Low-Z		t_{CLZ}	5	—	ns	*4
$\overline{OE}$ Low to Output Low-Z		t_{OLZ}	10	—	ns	*4
$\overline{LB}$, $\overline{UB}$ Low to Output Low-Z		t_{BLZ}	0	—	ns	*4
$\overline{CE}1$ High to Output High-Z		t_{CHZ}	—	20	ns	*1
$\overline{OE}$ High to Output High-Z		t_{OHZ}	—	14	ns	*1
$\overline{LB}$, $\overline{UB}$ High to Output High-Z		t_{BHZ}	—	20	ns	*1
$\overline{CE}1$ High to $\overline{WAIT}$ High-Z		t_{CHTZ}	—	20	ns	*1
$\overline{OE}$ High to $\overline{WAIT}$ High-Z		t_{OHTZ}	—	20	ns	*1
$\overline{OE}$ Low Setup Time to 1st Data-output		t_{OLQ}	30	—	ns	
$\overline{LB}$, $\overline{UB}$ Setup Time to 1st Data-output		t_{BLQ}	26	—	ns	*5
$\overline{OE}$ Setup Time to CLK		t_{OSCK}	4	—	ns	
$\overline{OE}$ Hold Time from CLK		t_{CKOH}	2	—	ns	
Burst End $\overline{CE}1$ Low Hold Time from CLK		t_{CKCLH}	2	—	ns	
Burst End $\overline{LB}$, $\overline{UB}$ Hold Time from CLK		t_{CKBH}	2	—	ns	
Burst Terminate Recovery Time	BL = 8, 16	t_{TRB}	26	—	ns	*6
	BL = Continuous		70	—	ns	*6

*1 : The output load 50 pF with 50 Ω termination to $V_{DD} \times 0.5$ V.

*2 : $\overline{WAIT}$ drives High at the beginning depending on $\overline{OE}$ falling edge timing.

*3 : t_{CKTV} is guaranteed after t_{OLTL} (Max) from $\overline{OE}$ falling edge and t_{OSCK} must be satisfied.

*4 : The output load 5 pF without any other load.

*5 : Once they are determined, they must not be changed until the end of burst read.

*6 : Defined from the Low to High transition of $\overline{CE}1$ to the High to Low transition of either $\overline{ADV}$ or $\overline{CE}1$ whichever occurs late.

(6) Synchronous Write Operation (Burst mode)

(At recommended operating conditions unless otherwise noted)

Parameter		Symbol	Value		Unit	Notes
			Min	Max		
Burst Write Cycle Time		t_{WCB}	—	4000	ns	
Data Setup Time to CLK		t_{DSCK}	4	—	ns	
Data Hold Time from CLK		t_{DHCK}	2	—	ns	
$\overline{WE}$ Low Setup Time to 1st Data Input		t_{WLD}	30	—	ns	
$\overline{LB}$, $\overline{UB}$ Setup Time for Write		t_{BS}	-5	—	ns	*1
$\overline{WE}$ Setup Time to CLK		t_{WSCK}	4	—	ns	
$\overline{WE}$ Hold Time from CLK		t_{CKWH}	2	—	ns	
$\overline{CE}$1 Low to $\overline{WAIT}$ High		t_{CLTH}	5	20	ns	*2
$\overline{WE}$ Low to $\overline{WAIT}$ High		t_{WLTH}	0	20	ns	*2
$\overline{CE}$1 High to $\overline{WAIT}$ High-Z		t_{CHTZ}	—	20	ns	*2
$\overline{WE}$ High to $\overline{WAIT}$ High-Z		t_{WHTZ}	—	20	ns	*2
Burst End $\overline{CE}$1 Low Hold Time from CLK		t_{CKCLH}	2	—	ns	
Burst End $\overline{CE}$1 High Setup Time to next CLK		t_{CHCK}	4	—	ns	
Burst End $\overline{LB}$, $\overline{UB}$ Hold Time from CLK		t_{CKBH}	2	—	ns	
Burst Write Recovery Time		t_{WRB}	26	—	ns	*3
Burst Terminate Recovery Time	BL = 8, 16	t_{TRB}	26	—	ns	*4
	BL = Continuous	t_{TRB}	70	—	ns	*4

*1 : Defined from the valid input edge to the High to Low transition of either $\overline{ADV}$, $\overline{CE}$1, or $\overline{WE}$, whichever occurs last. And once $\overline{LB}$, $\overline{UB}$ are determined, $\overline{LB}$, $\overline{UB}$ must not be changed until the end of burst write.

*2 : The output load 50 pF with 50 Ω termination to $V_{DD} \times 0.5$ V.

*3 : Defined from the valid clock edge where last data-input being latched at the end of burst write to the High to Low transition of either $\overline{ADV}$ or $\overline{CE}$1 whichever occurs late for the next access.

*4 : Defined from the Low to High transition of $\overline{CE}$1 to the High to Low transition of either $\overline{ADV}$ or $\overline{CE}$1 whichever occurs late for the next access.

(7) Power Down Parameters

(At recommended operating conditions unless otherwise noted)

Parameter	Symbol	Value		Unit	Notes
		Min	Max		
CE2 Low Setup Time for Power Down Entry	t_{CSP}	10	—	ns	
CE2 Low Hold Time after Power Down Entry	t_{C2LP}	70	—	ns	
CE2 Low Hold Time for Reset to Asynchronous mode	t_{C2LPR}	50	—	µs	*1
$\overline{CE}$1 High Hold Time following CE2 High after Power Down Exit [SLEEP mode only]	t_{CHH}	300	—	µs	*2
$\overline{CE}$1 High Hold Time following CE2 High after Power Down Exit [not in SLEEP mode]	t_{CHHP}	70	—	ns	*3
$\overline{CE}$1 High Setup Time following CE2 High after Power Down Exit	t_{CHS}	0	—	ns	*2

*1 : Applicable when CR is set to RP=0 (Reset to Page mode)

*2 : Applicable also to power-up.

*3 : Applicable when 8 M-bit or 16 M-bit Partial mode is set.

(8) Other Timing Parameters

(At recommended operating conditions unless otherwise noted)

Parameter	Symbol	Value		Unit	Notes
		Min	Max		
$\overline{CE}$1 High to $\overline{OE}$ Invalid Time for Standby Entry	t_{CHOX}	10	—	ns	
$\overline{CE}$1 High to $\overline{WE}$ Invalid Time for Standby Entry	t_{CHWX}	10	—	ns	*1
CE2 Low Hold Time after Power-up	t_{C2LH}	50	—	µs	
$\overline{CE}$1 High Hold Time following CE2 High after Power-up	t_{CHH}	300	—	µs	
Input Transition Time (except for CLK)	t_T	1	25	ns	*2, *3

*1 : Some data might be written into any address location if t_{CHWX} (Min) is not satisfied.

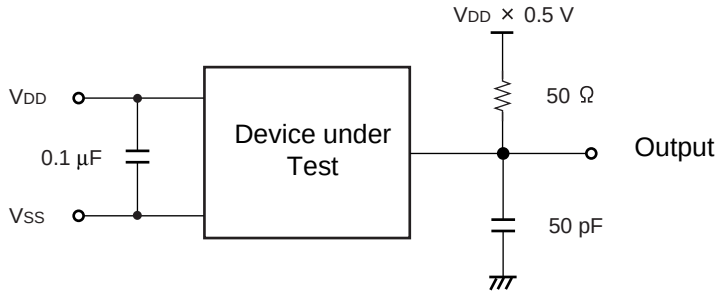
*2 : Except for clock input transition time.

*3 : The Input Transition Time (t_T) at AC testing is 5 ns for Asynchronous operation and 3 ns for Synchronous operation respectively. If actual t_T is longer than 5 ns or 3 ns specified as AC test condition, it may violate AC specification of some timing parameters. See " (9) AC Test Conditions".

(9) AC Test Conditions

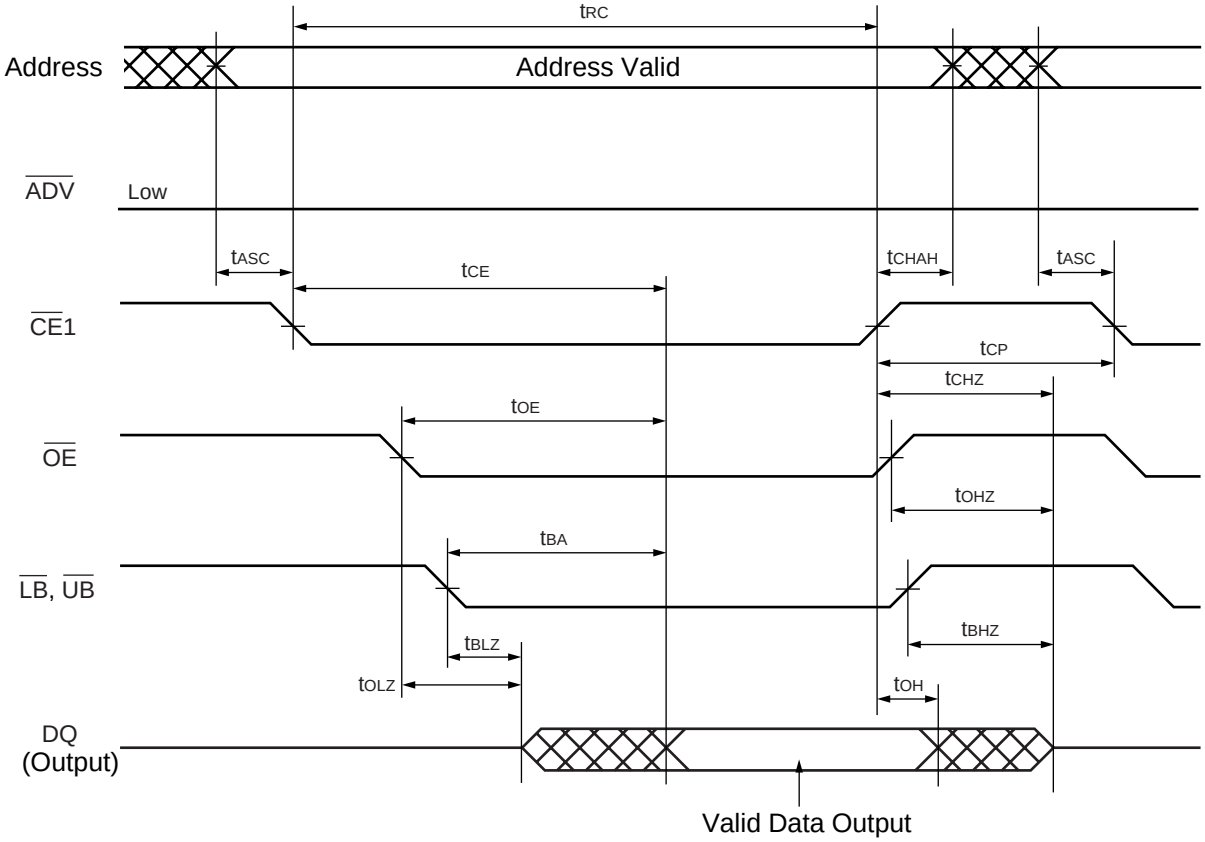
Description		Symbol	Test Setup	Value	Unit	Notes
Input High Level		V_{IH}	—	$V_{DD} \times 0.8$	V	
Input Low Level		V_{IL}	—	$V_{DD} \times 0.2$	V	
Input Timing Measurement Level		V_{REF}	—	$V_{DD} \times 0.5$	V	
Input Transition Time	Async.	t_T	Between V_{IL} and V_{IH}	5	ns	
	Sync.			3	ns	

- AC MEASUREMENT OUTPUT LOAD CIRCUIT



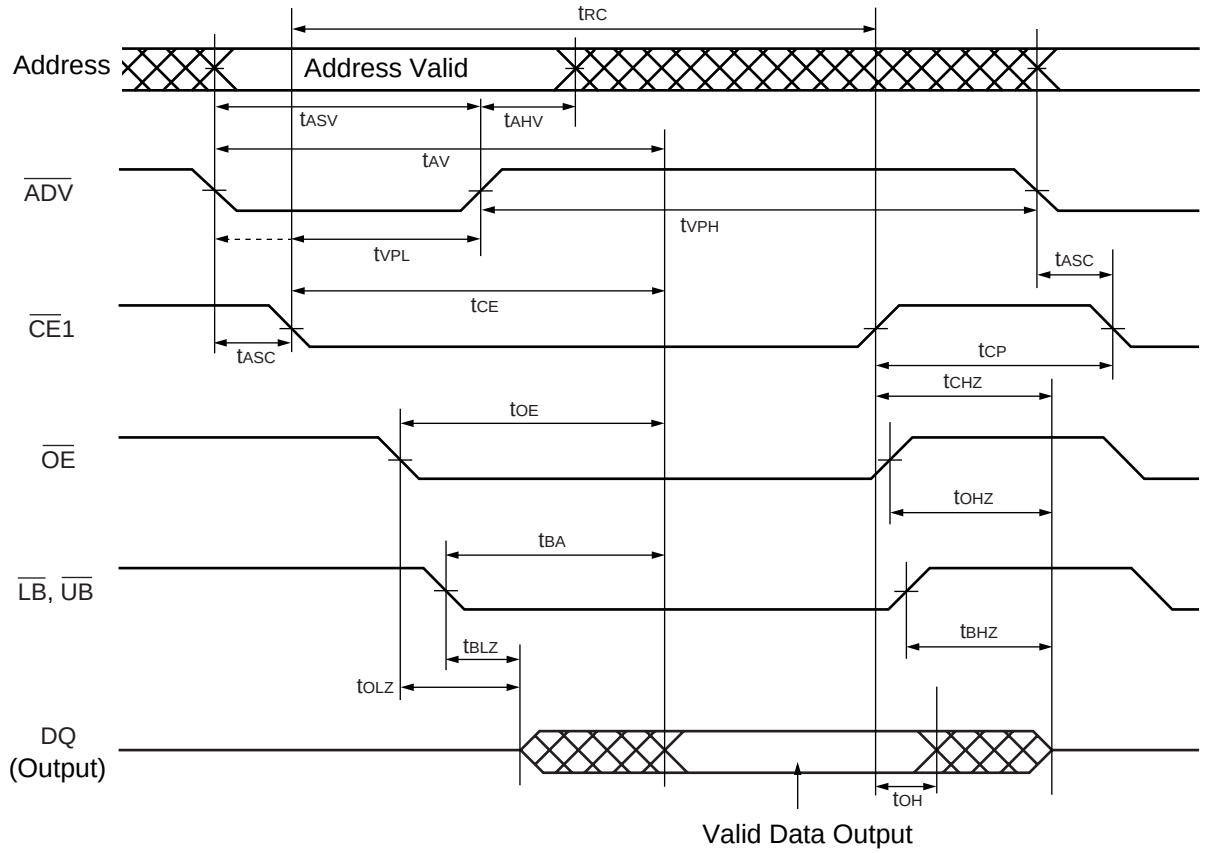
■ TIMING DIAGRAMS

(1) Asynchronous Read Timing 1-1 (Basic Timing)



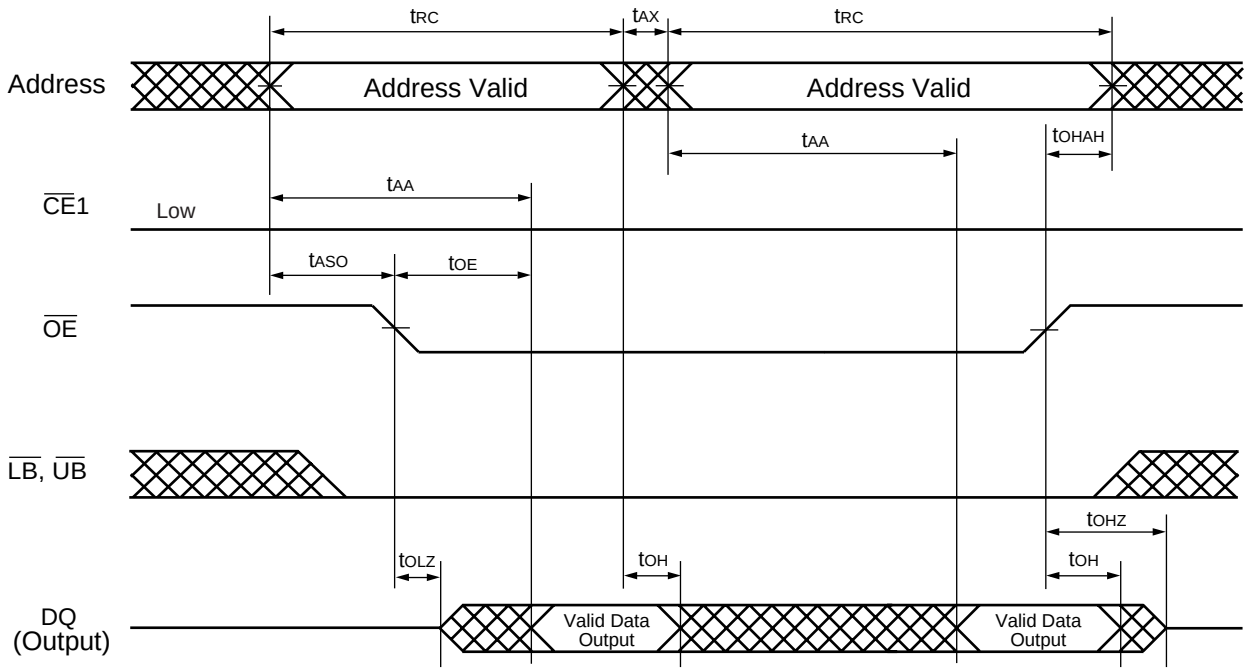
Note : This timing diagram assumes CE2 = H and $\overline{WE}$ = H.

(2) Asynchronous Read Timing 1-2 (Basic Timing)



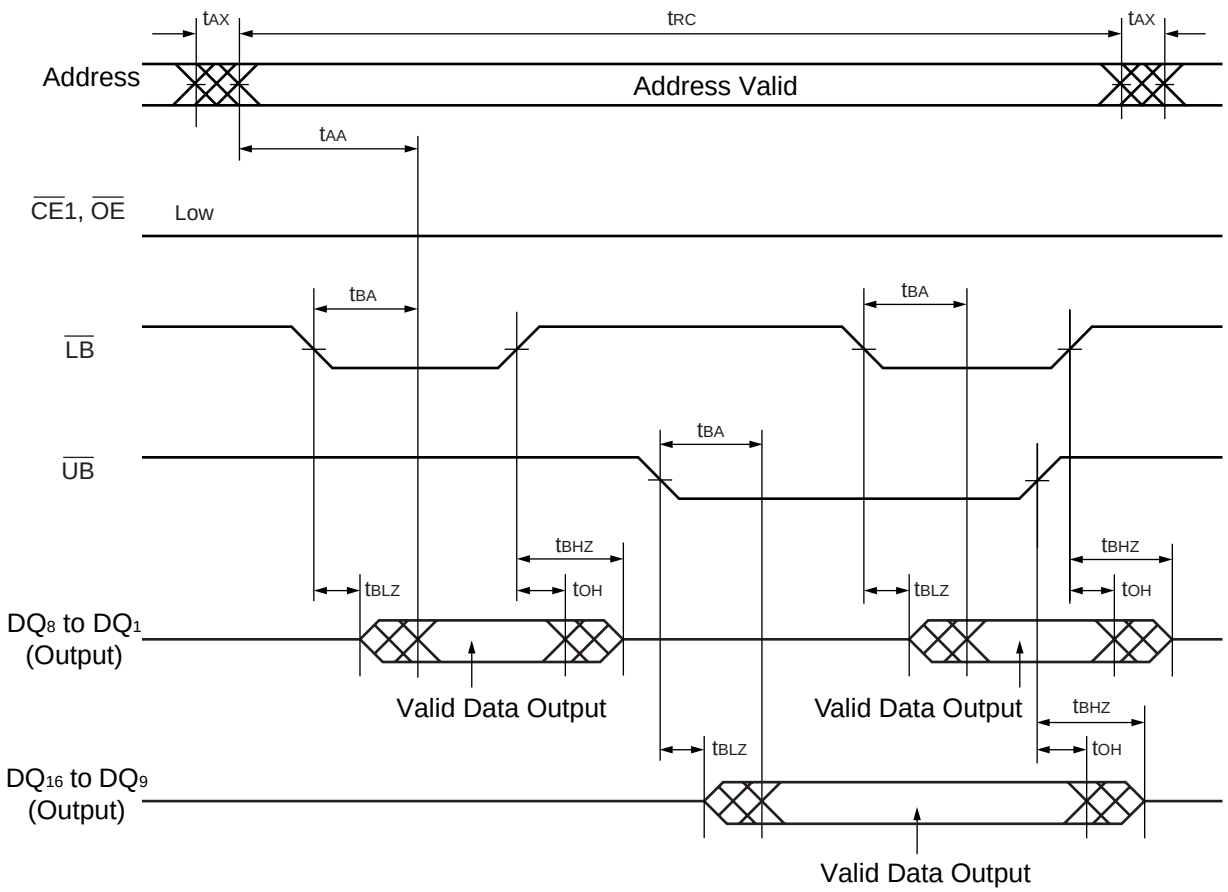
Note : This timing diagram assumes CE2 = H and $\overline{WE}$ = H.

(3) Asynchronous Read Timing 2 ($\overline{OE}$ Control & Address Access)



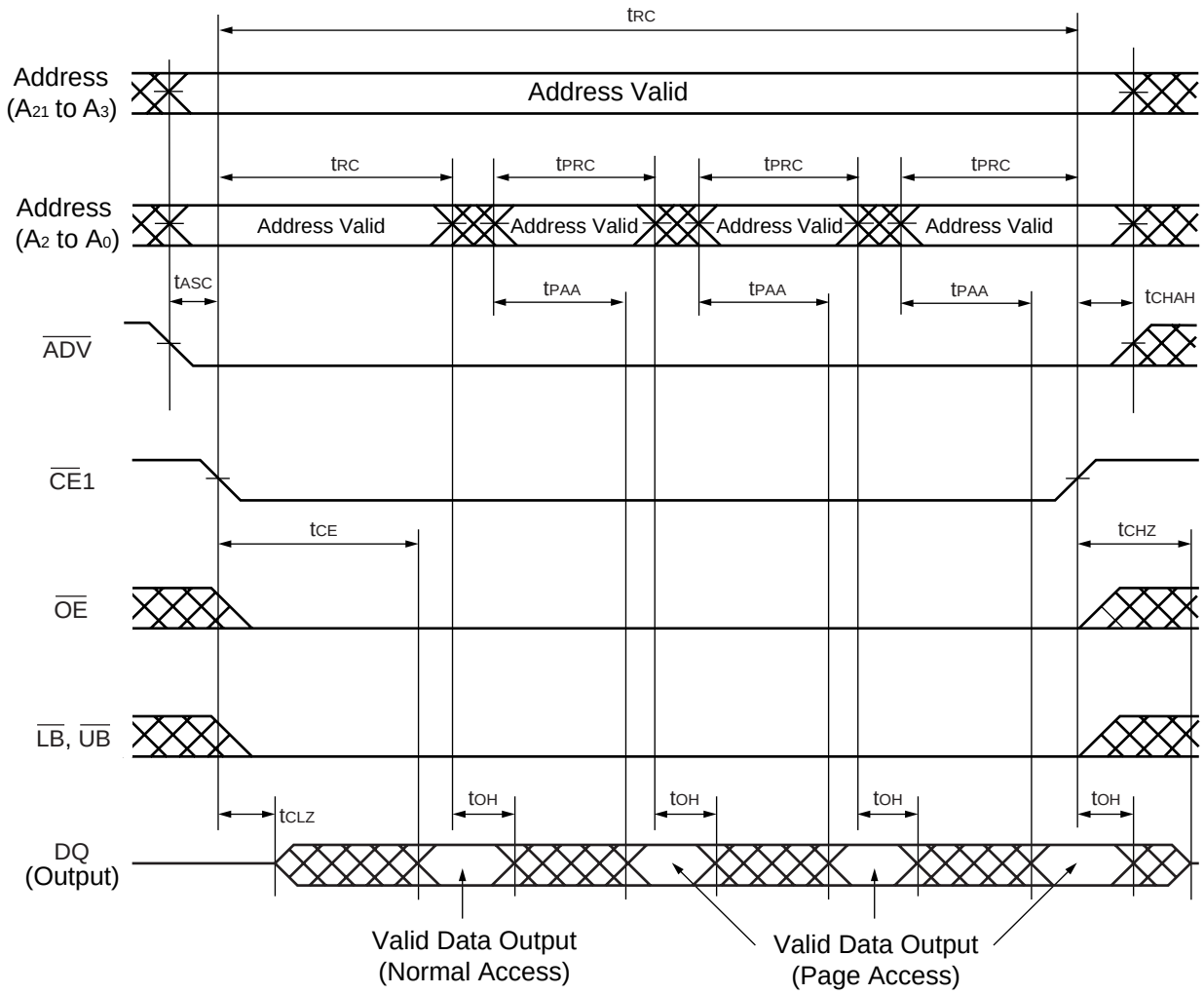
Note : This timing diagram assumes CE2 = H, $\overline{ADV}$ = L and $\overline{WE}$ = H.

(4) Asynchronous Read Timing 3 ($\overline{LB}$, $\overline{UB}$ Byte Control Access)



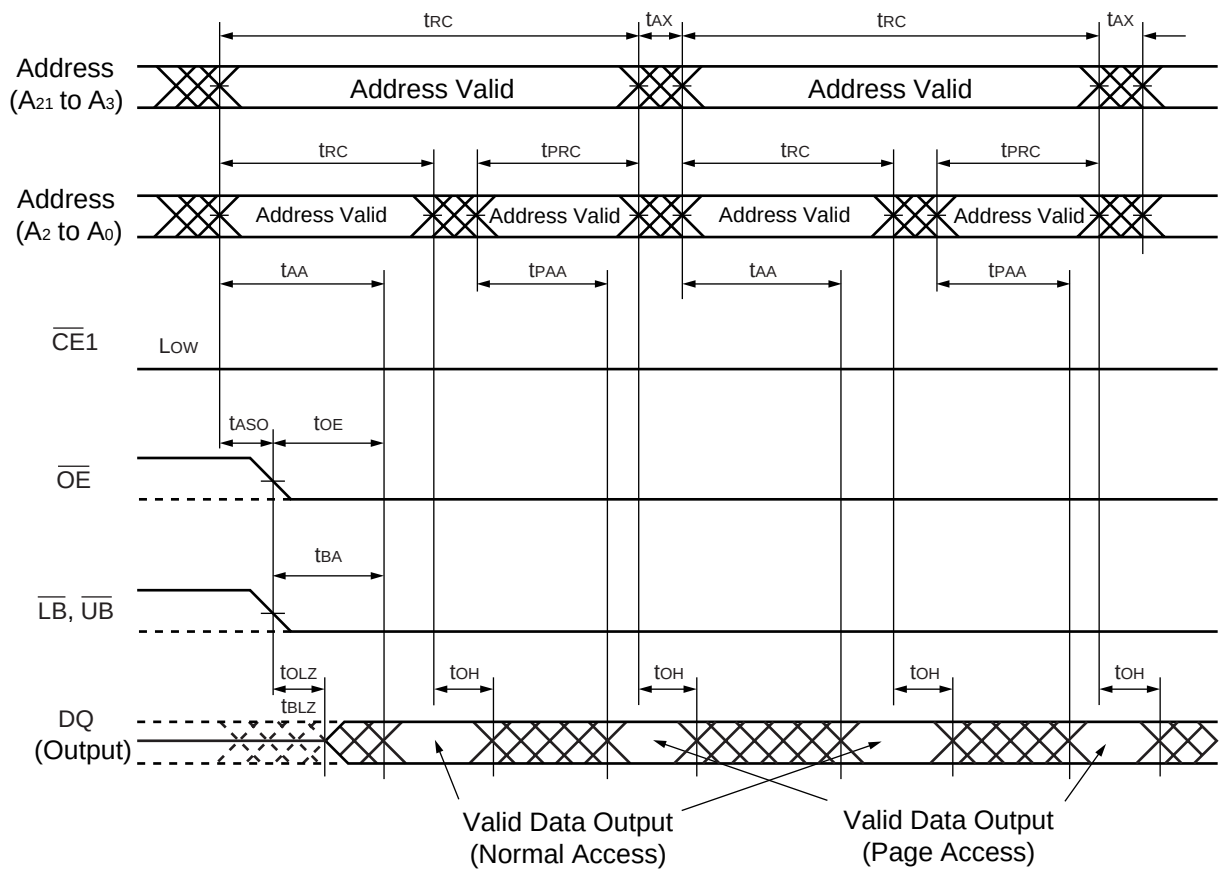
Note : This timing diagram assumes CE2 = H, $\overline{ADV}$ = L and $\overline{WE}$ = H.

(5) Asynchronous Read Timing 4 (Page Address Access after $\overline{CE}$1 Control Access)



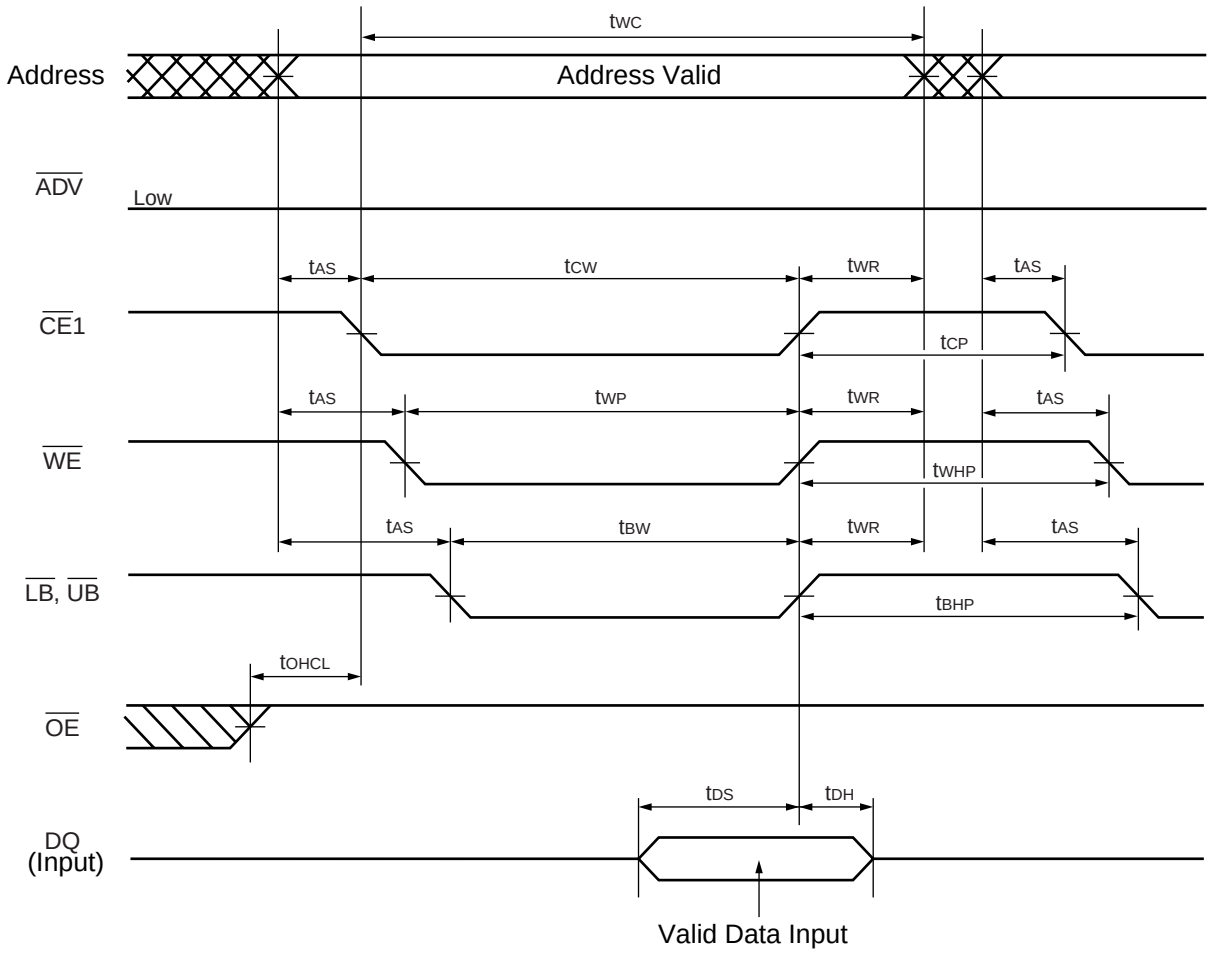
Note : This timing diagram assumes CE2 = H and $\overline{WE}$ = H.

(6) Asynchronous Read Timing 5 (Random and Page Address Access)



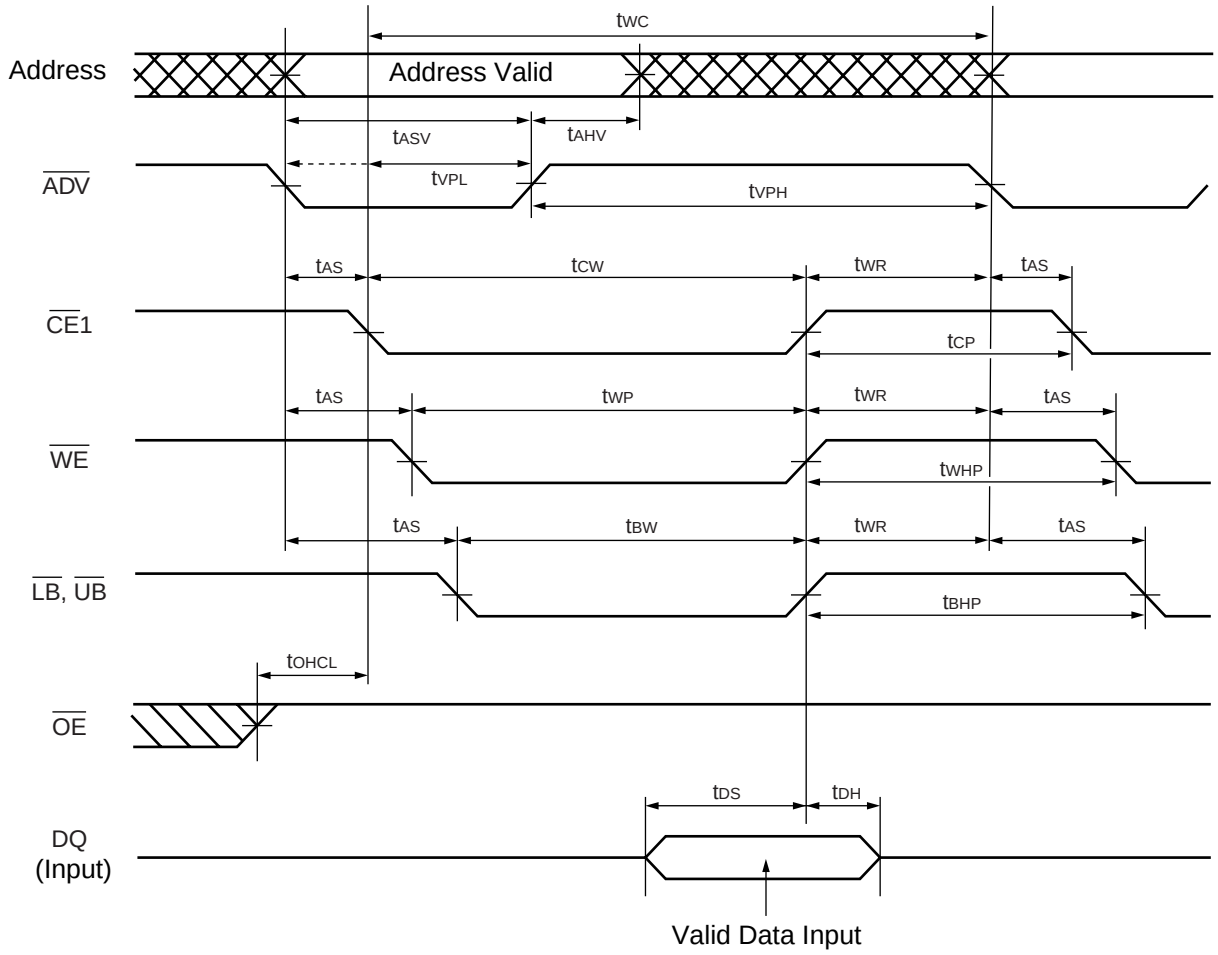
Notes : • This timing diagram assumes CE2 = H, $\overline{ADV}$ = L and $\overline{WE}$ = H.
• Either or both $\overline{LB}$ and $\overline{UB}$ must be Low when both $\overline{CE}$1 and $\overline{OE}$ are Low.

(7) Asynchronous Write Timing 1-1 (Basic Timing)



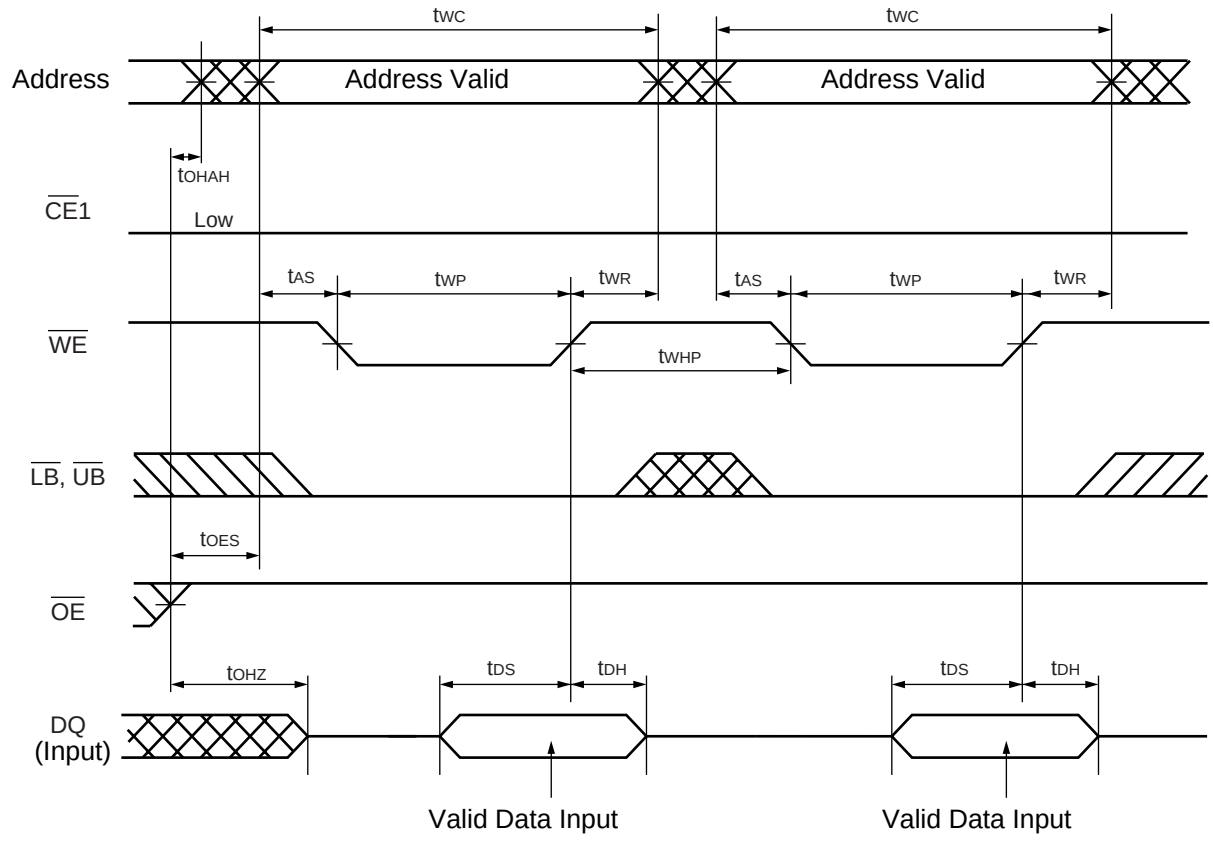
Note : This timing diagram assumes CE2 = H and $\overline{ADV}$ = L.

(8) Asynchronous Write Timing 1-2 (Basic Timing)



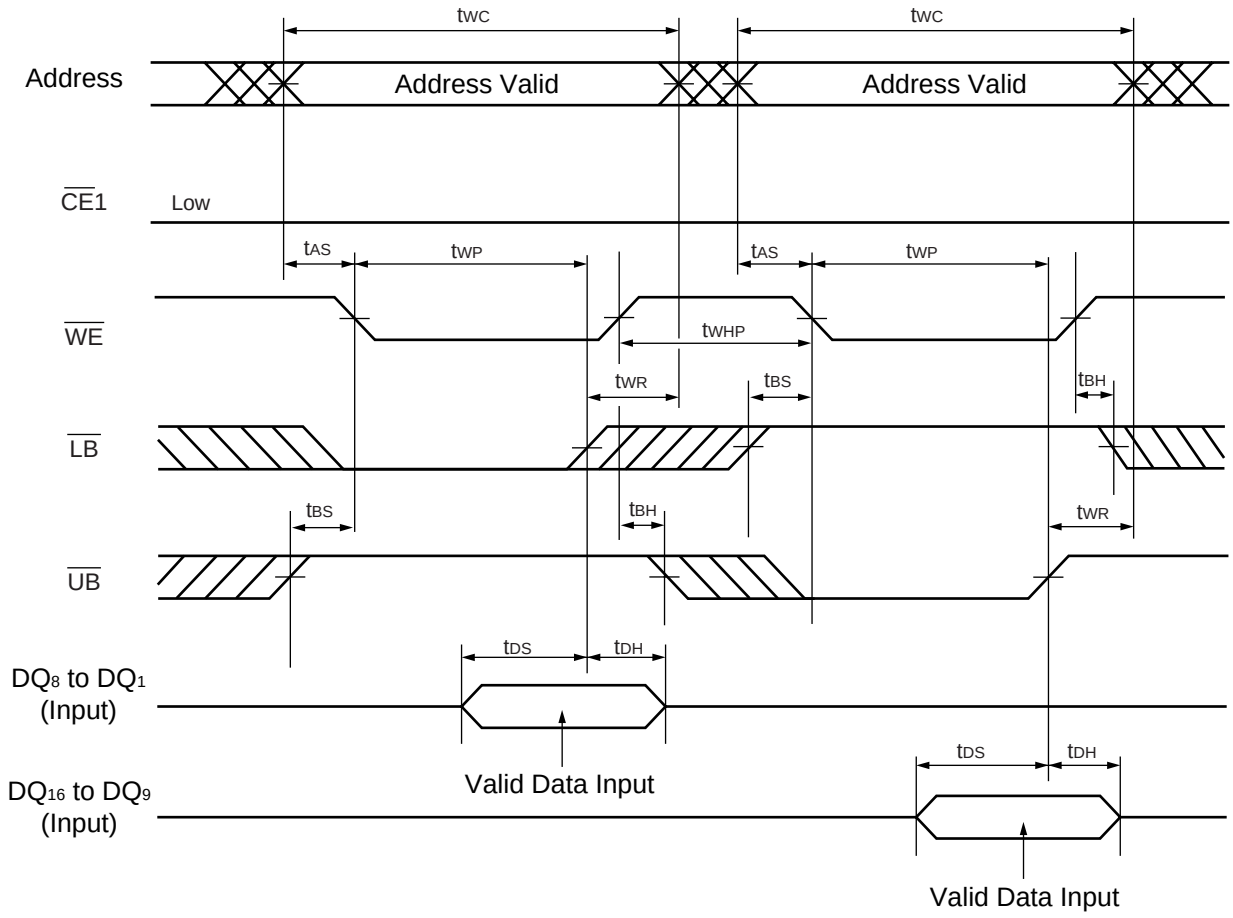
Note : This timing diagram assumes CE2 = H.

(9) Asynchronous Write Timing 2 ($\overline{WE}$ Control)



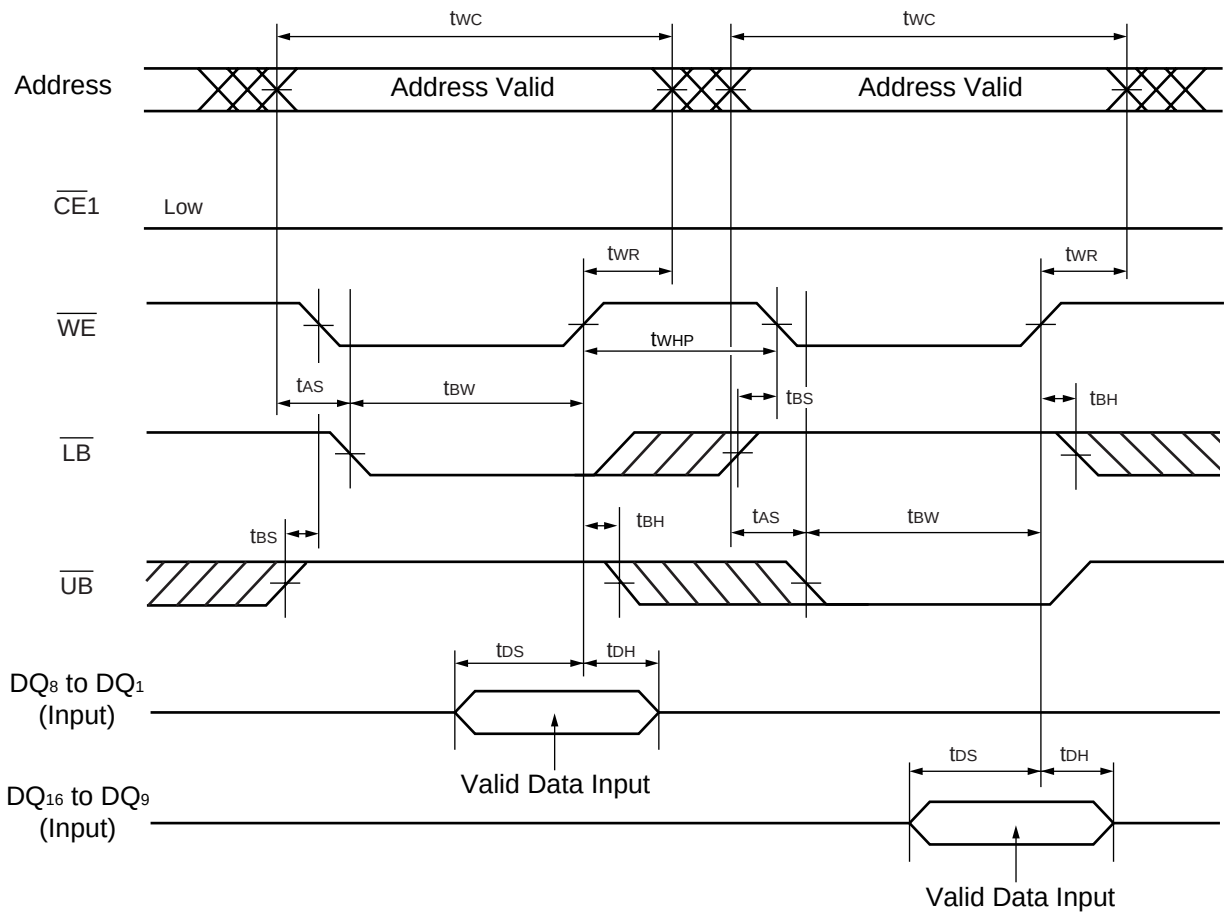
Note : This timing diagram assumes CE2 = H and $\overline{ADV}$ = L.

(10) Asynchronous Write Timing 3-1 ($\overline{WE}$, $\overline{LB}$, $\overline{UB}$ Byte Write Control)



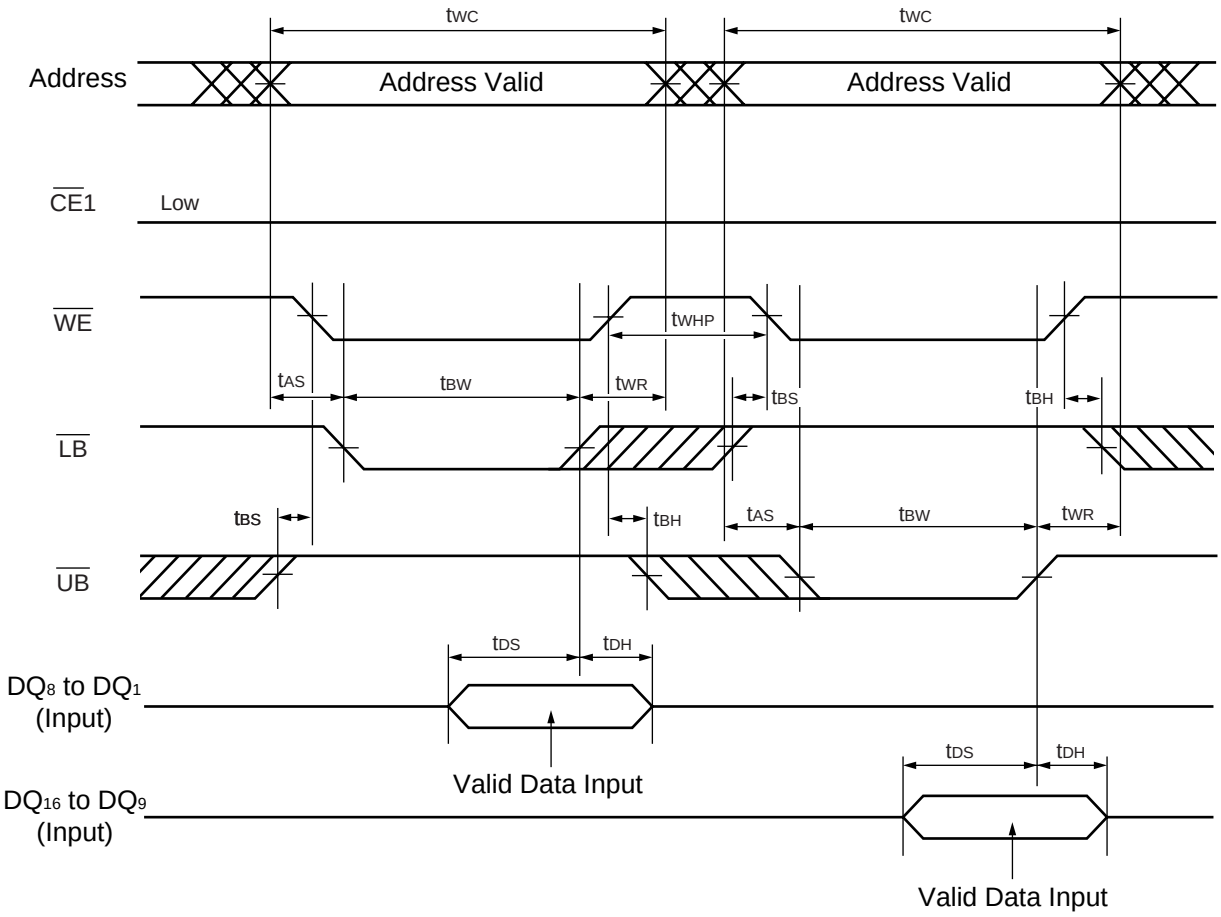
Note : This timing diagram assumes CE2 = H, $\overline{ADV}$ = L and $\overline{OE}$ = H.

(11) Asynchronous Write Timing 3-2 ($\overline{WE}$, $\overline{LB}$, $\overline{UB}$ Byte Write Control)



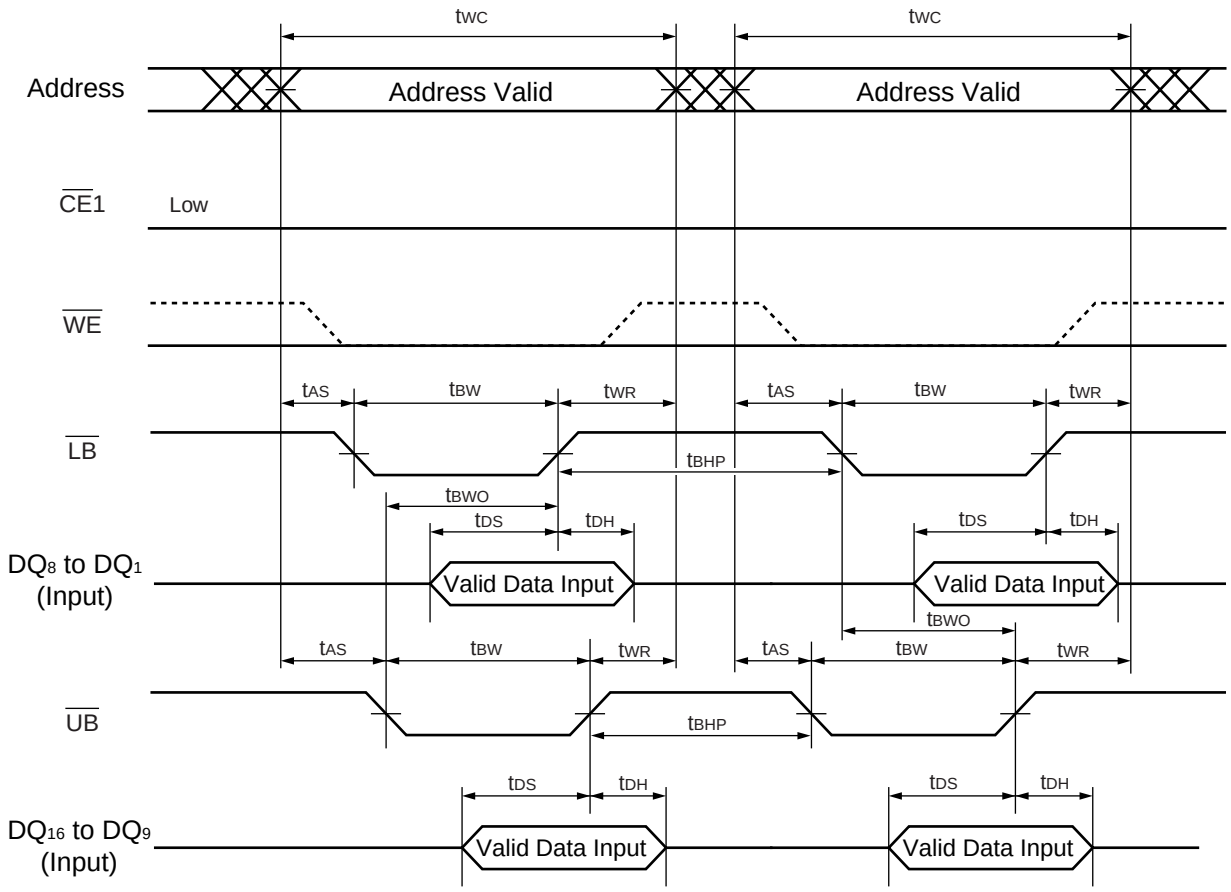
Note : This timing diagram assumes CE2 = H, $\overline{ADV}$ = L and $\overline{OE}$ = H.

(12) Asynchronous Write Timing 3-3 ($\overline{WE}$, $\overline{LB}$, $\overline{UB}$ Byte Write Control)



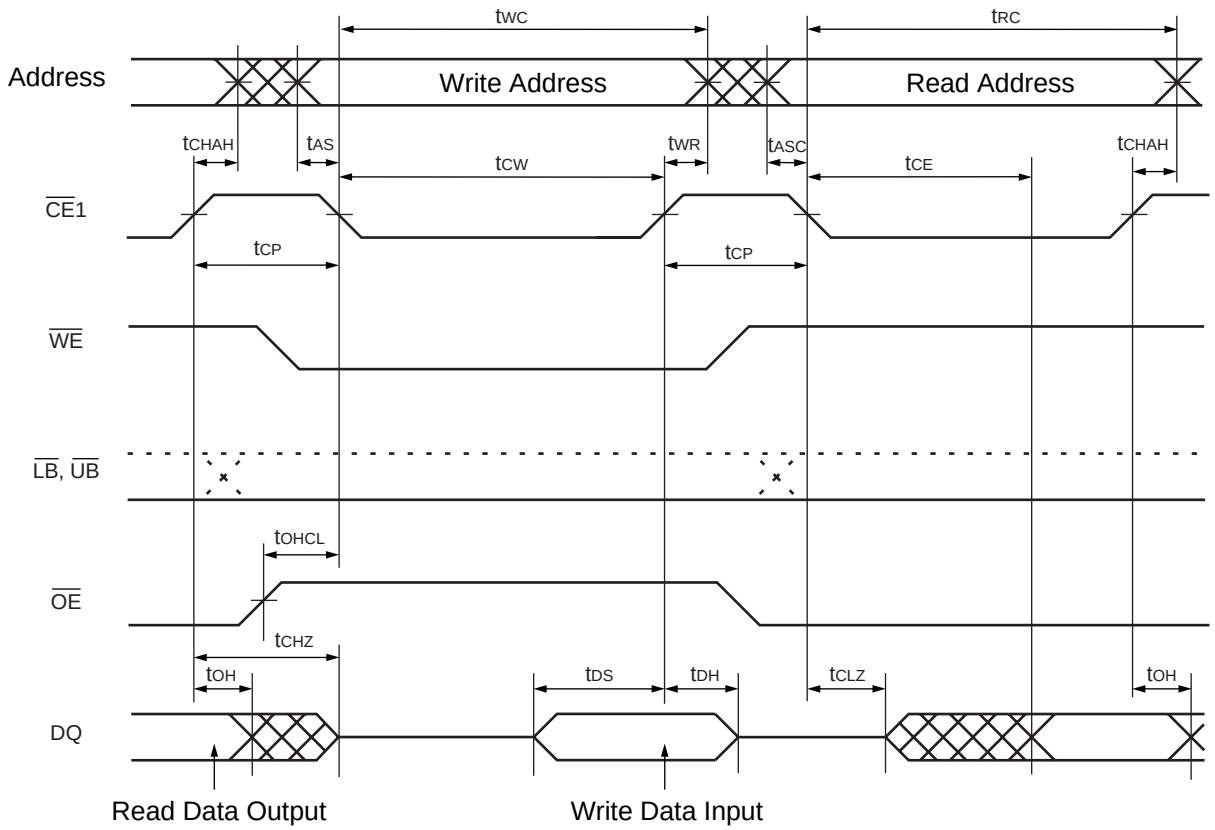
Note : This timing diagram assumes CE2 = H, $\overline{ADV}$ = L and $\overline{OE}$ = H.

(13) Asynchronous Write Timing 3-4 ($\overline{WE}$, $\overline{LB}$, $\overline{UB}$ Byte Write Control)



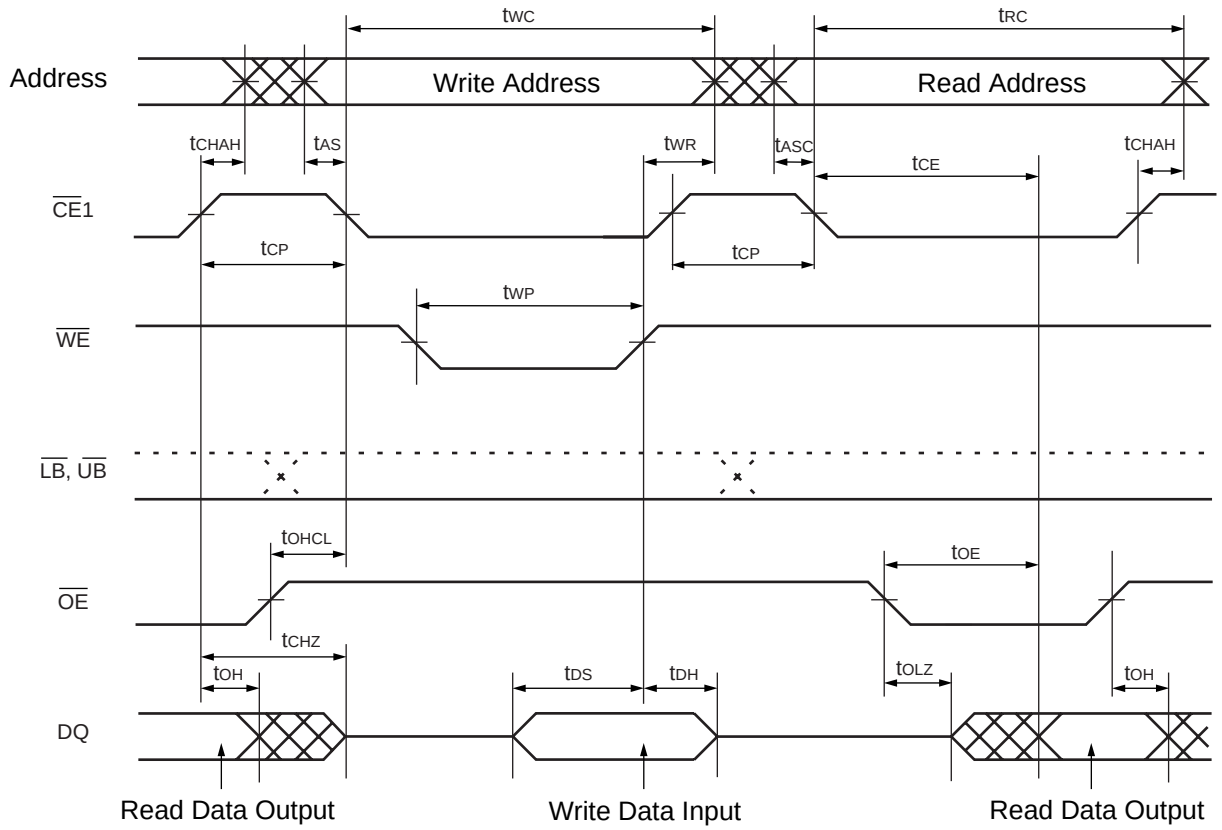
Note : This timing diagram assumes CE2 = H, $\overline{ADV}$ = L and $\overline{OE}$ = H.

(14) Asynchronous Read/Write Timing 1-1 ($\overline{CE}$1 Control)



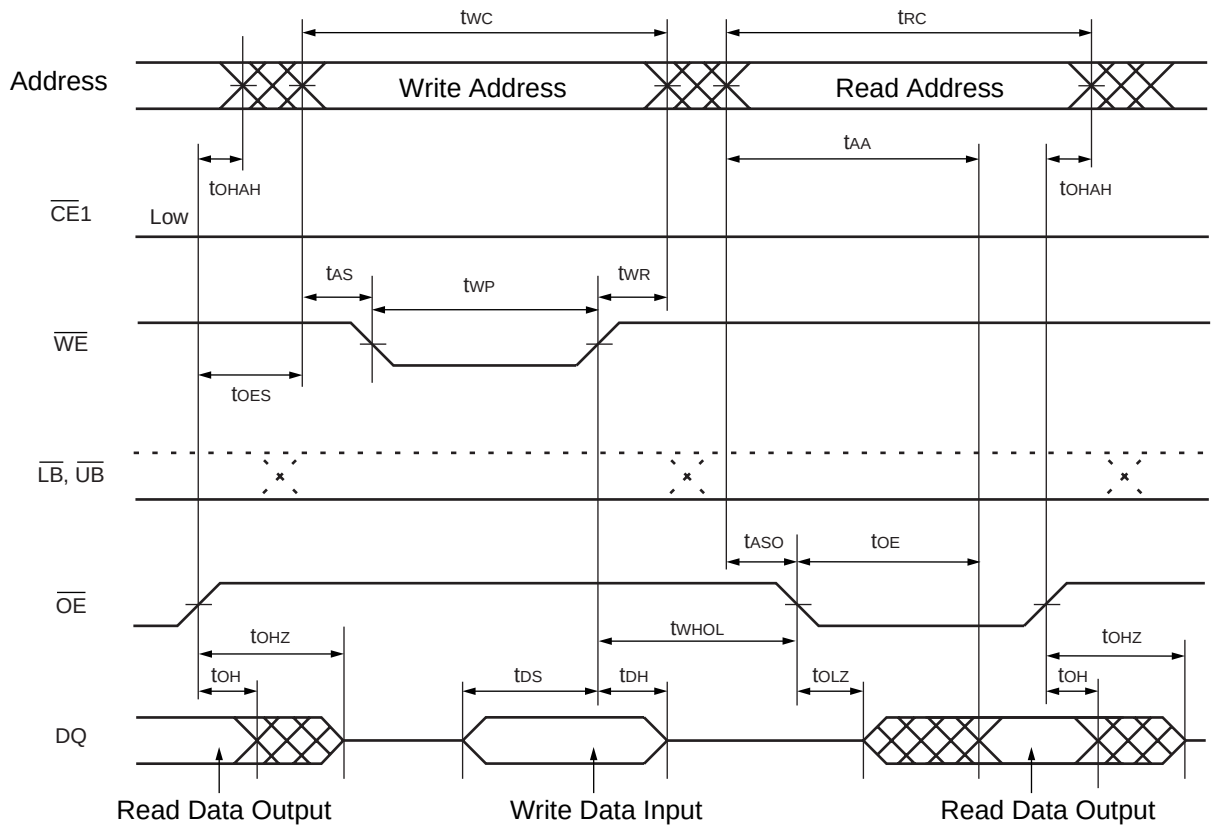
Notes : • This timing diagram assumes CE2 = H and $\overline{ADV}$ = L
• Write address is valid from either $\overline{CE}$1 or $\overline{WE}$ of last falling edge.

(15) Asynchronous Read/Write Timing 1-2 ($\overline{CE}$1, $\overline{WE}$, $\overline{OE}$ Control)



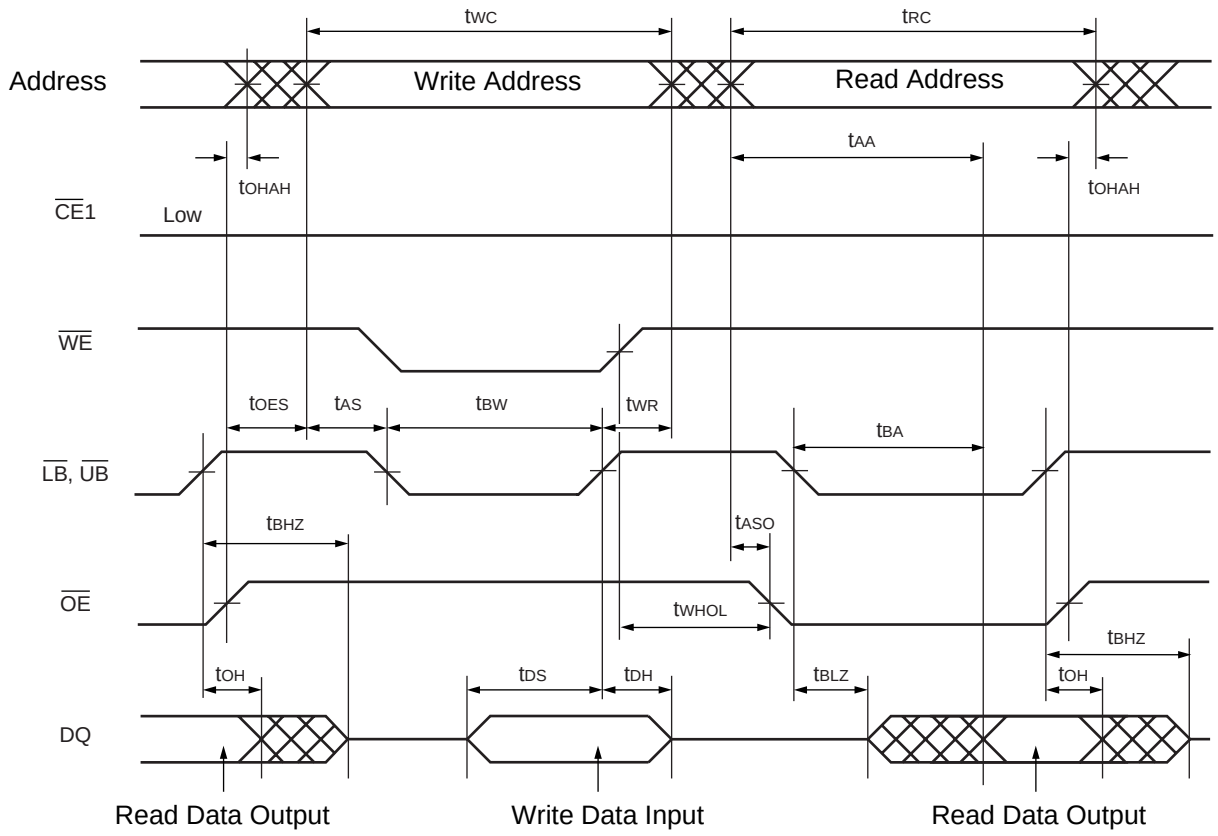
Notes : • This timing diagram assumes CE2 = H and $\overline{ADV}$ = L.
• $\overline{OE}$ can be fixed Low during write operation if it is $\overline{CE}$1 controlled write at Read-Write-Read sequence.

(16) Asynchronous Read/Write Timing 2 ($\overline{OE}$, $\overline{WE}$ Control)



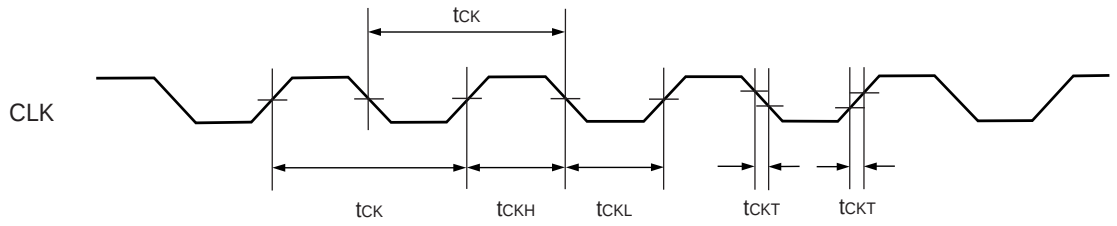
Notes : • This timing diagram assumes CE2 = H and $\overline{ADV}$ = L.
• $\overline{CE}$1 can be tied to Low for $\overline{WE}$ and $\overline{OE}$ controlled operation.

(17) Asynchronous Read/Write Timing 3 ($\overline{OE}$, $\overline{WE}$, $\overline{LB}$, $\overline{UB}$ Control)



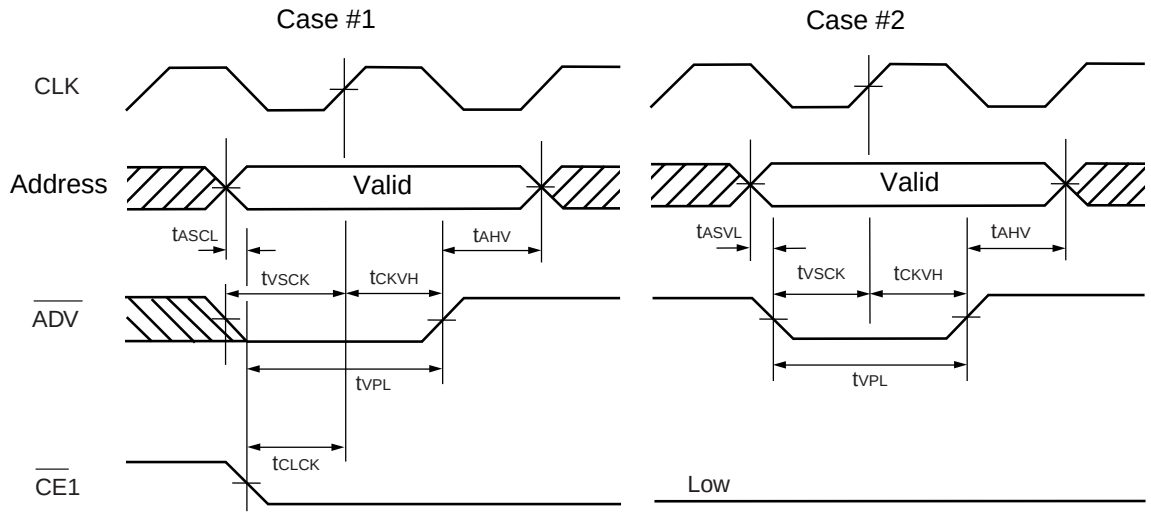
Notes : • This timing diagram assumes CE2 = H and $\overline{ADV}$ = L.
• $\overline{CE}$1 can be tied to Low for $\overline{WE}$ and $\overline{OE}$ controlled operation.

(18) Clock Input Timing



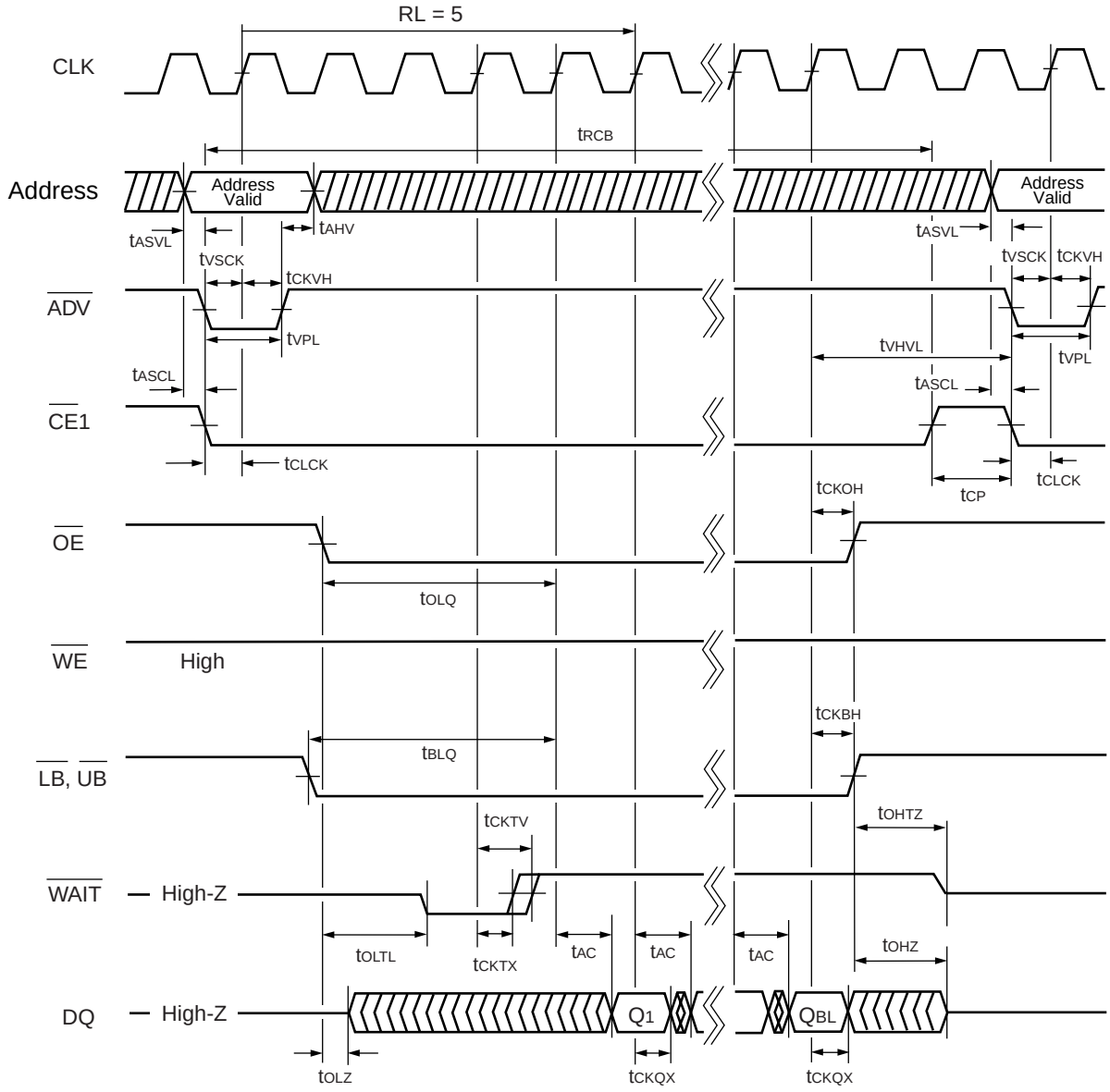
Notes : • Stable clock input must be required during $\overline{CE}1$ = L.
• t_{CK} is defined between valid clock edges.
• t_{CKT} is defined between V_{IH} (Min) and V_{IL} (Max)

(19) Address Latch Timing (Synchronous Mode)



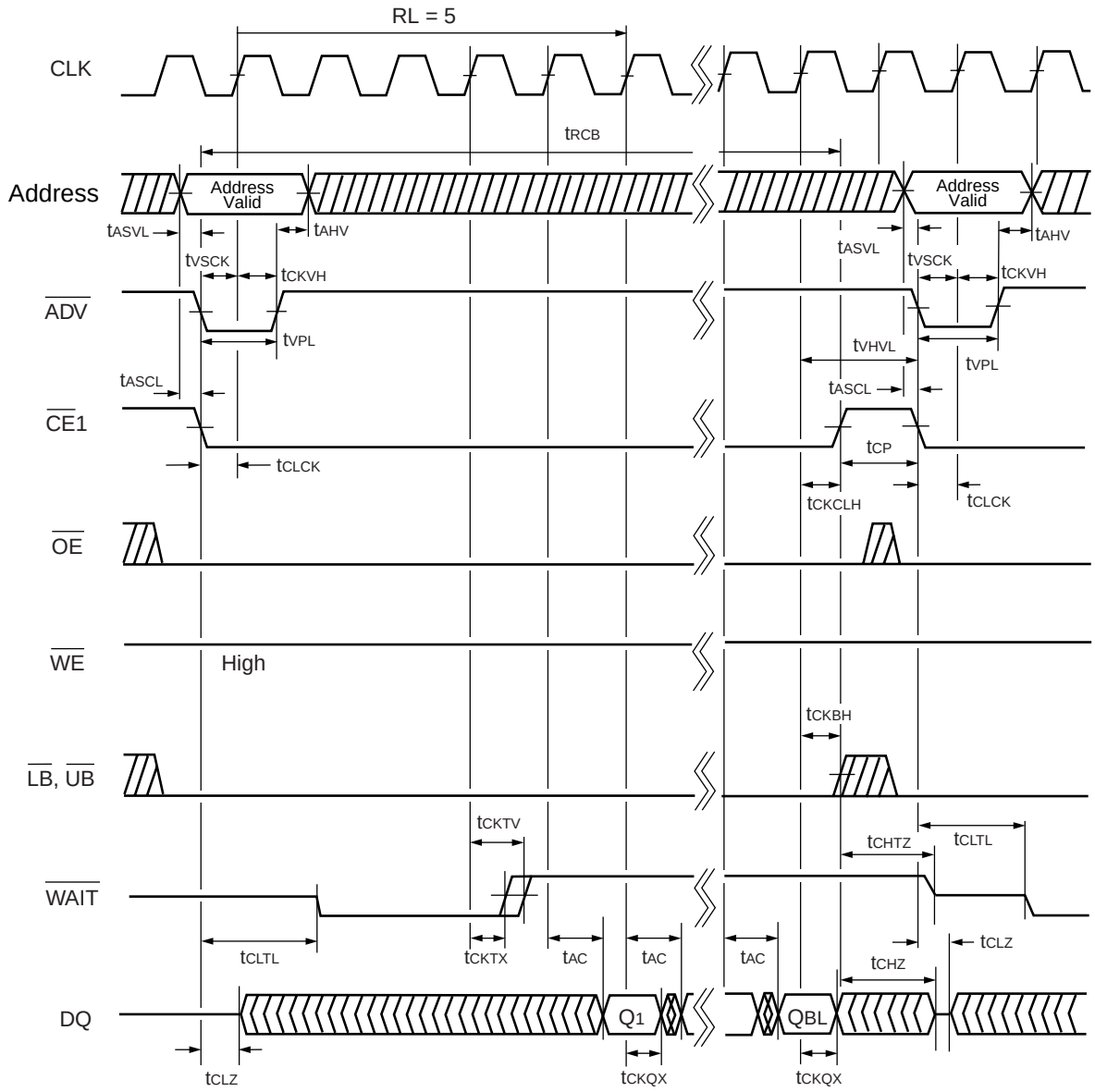
Notes : • Case #1 is the timing when $\overline{CE}1$ is brought to Low after $\overline{ADV}$ is brought to Low.
Case #2 is the timing when $\overline{ADV}$ is brought to Low after $\overline{CE}1$ is brought to Low.
• t_{VPL} is specified from the falling edge of either $\overline{CE}1$ or $\overline{ADV}$ whichever comes late.
At least one valid clock edge must be input during $\overline{ADV}$ = L.
• t_{VSCK} and t_{CLCK} are applied to the 1st valid clock edge during $\overline{ADV}$=L.

(20) Synchronous Read Timing 1 ($\overline{OE}$ Control)



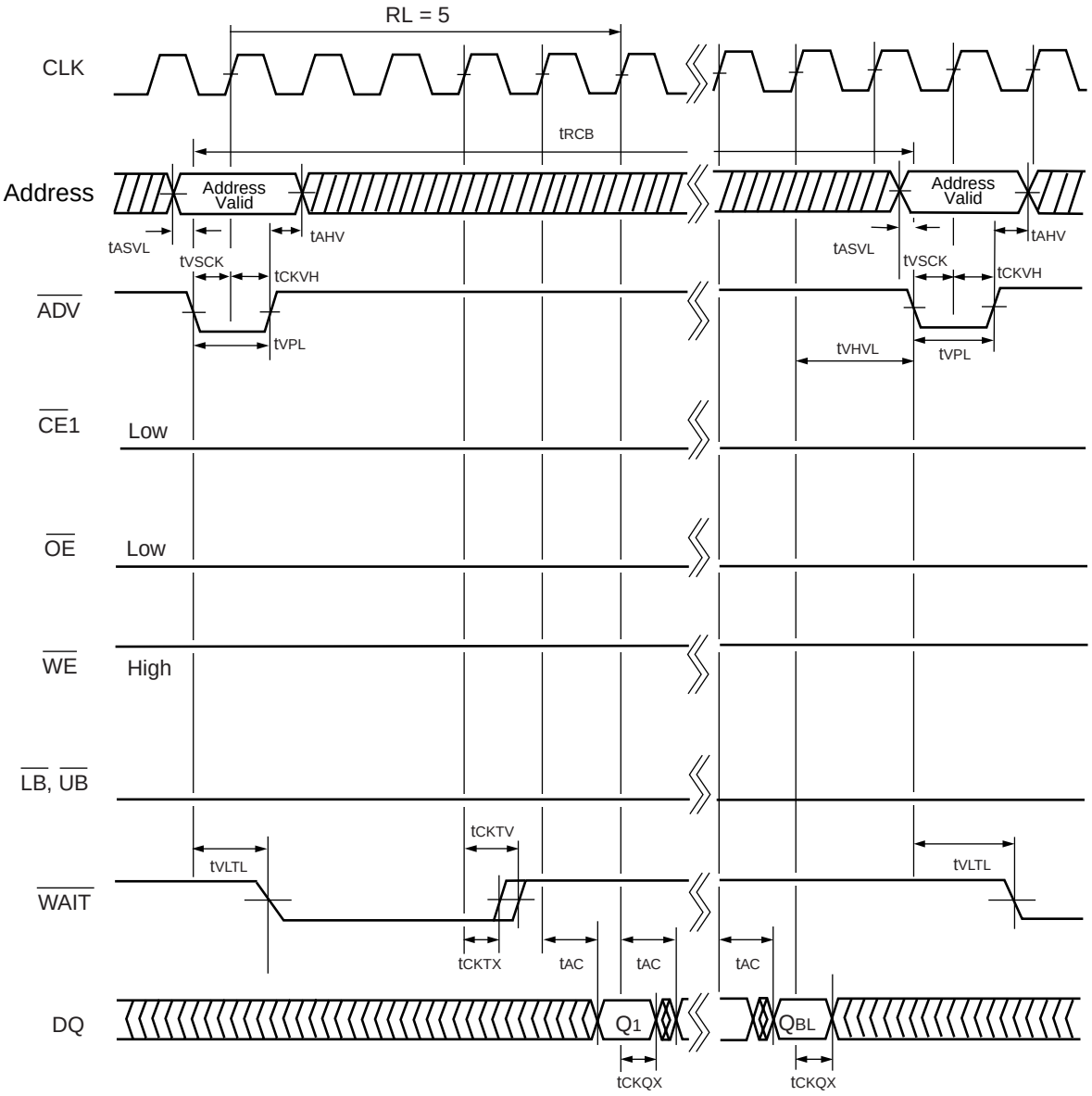
Note : This timing diagram assumes CE2 = H, the valid clock edge on rising edge and BL = 8 or 16.

(21) Synchronous Read Timing 2 ($\overline{CE}$1 Control)



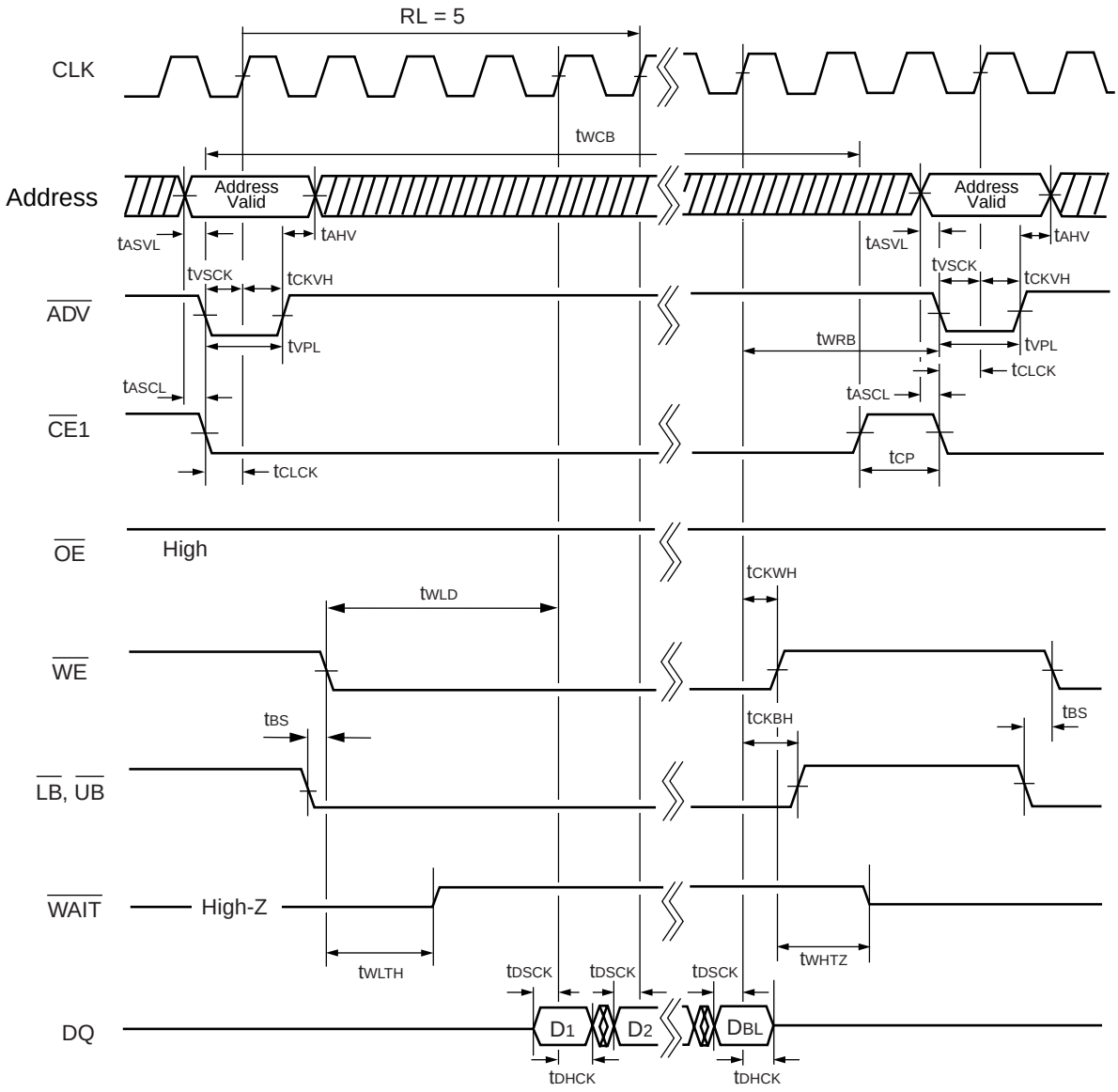
Note : This timing diagram assumes CE2 = H, the valid clock edge on rising edge and BL = 8 or 16.

(22) Synchronous Read Timing 3 ($\overline{\text{ADV}}$ Control)



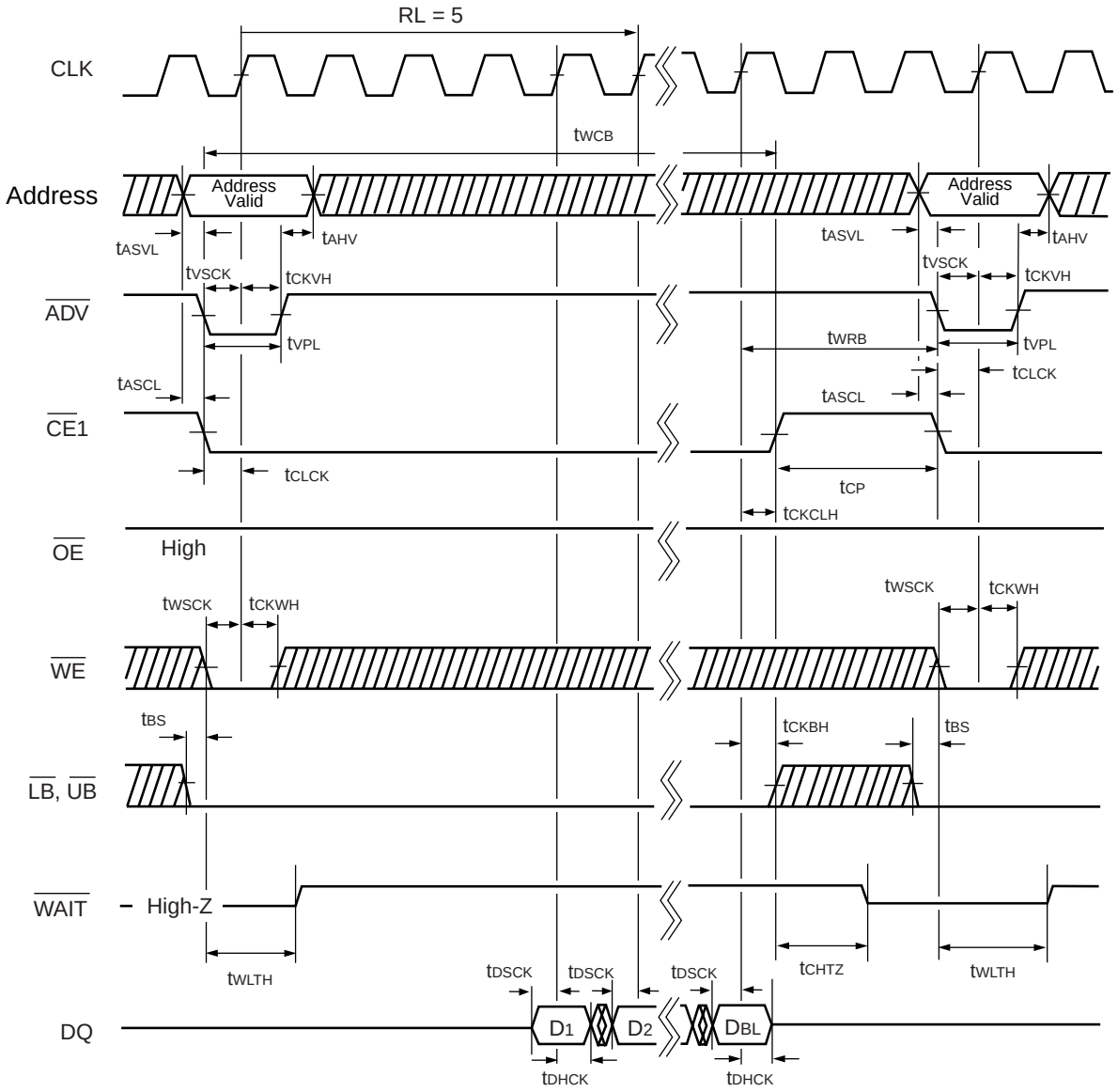
Note : This timing diagram assumes CE2 = H, the valid clock edge on rising edge and BL = 8 or 16.

(23) Synchronous Write Timing 1 ($\overline{WE}$ Level Control)



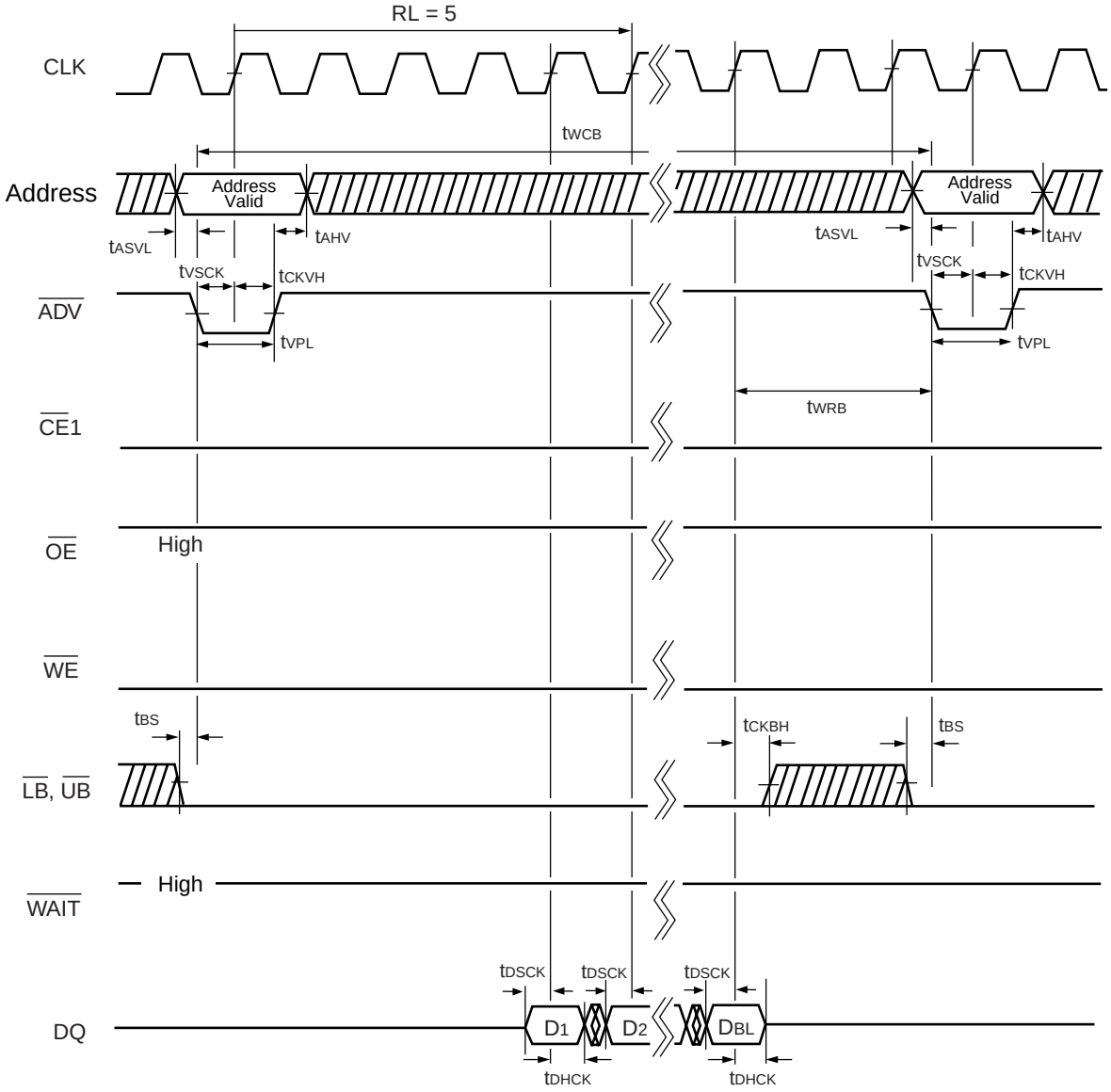
Note : This timing diagram assumes CE2 = H, the valid clock edge on rising edge and BL = 8 or 16.

(24) Synchronous Write Timing 2 ($\overline{WE}$ Single Clock Pulse Timing)



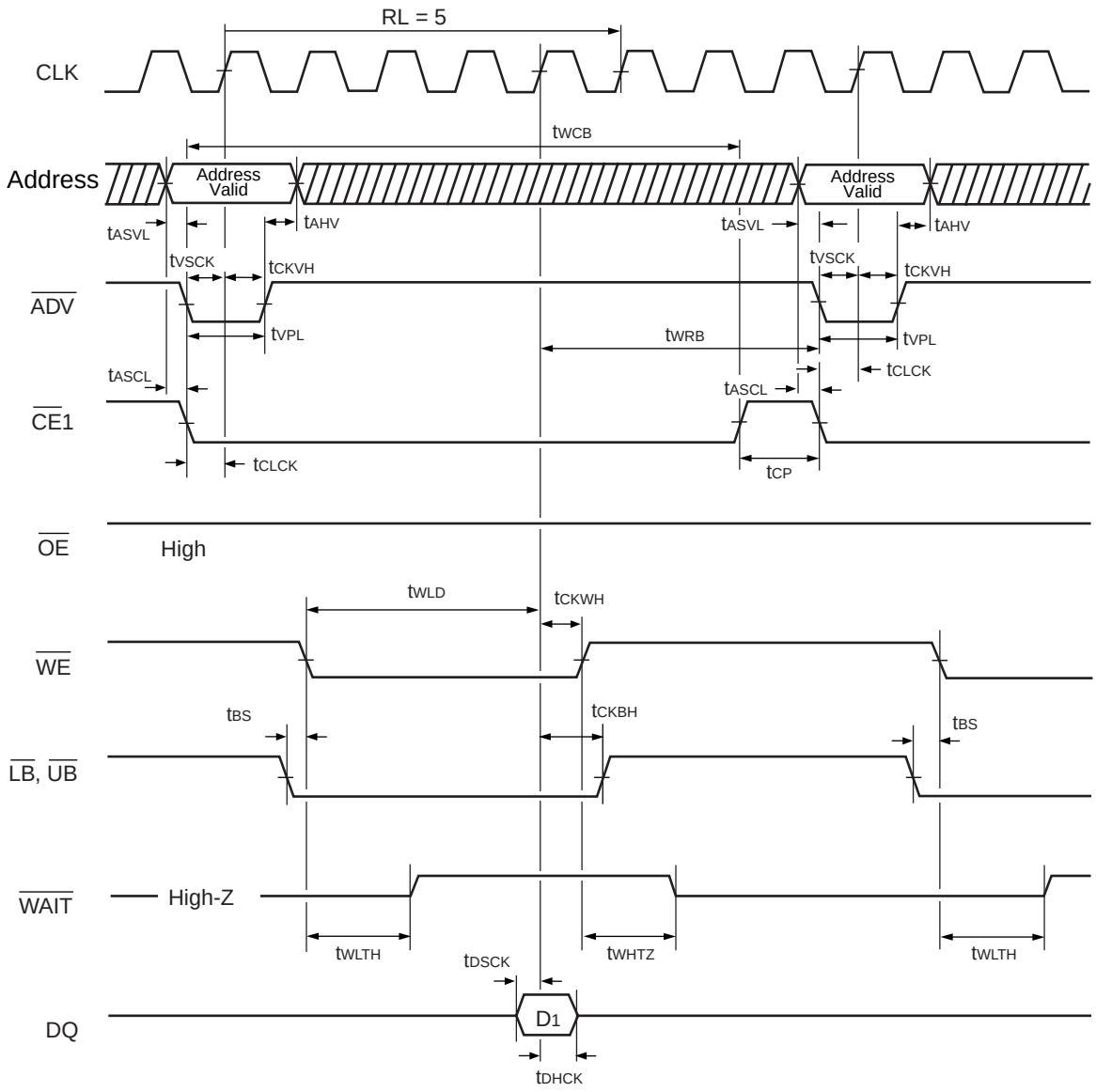
Note : This timing diagram assumes CE2 = H, the valid clock edge on rising edge and BL = 8 or 16.

(25) Synchronous Write Timing 3 ($\overline{\text{ADV}}$ Control)



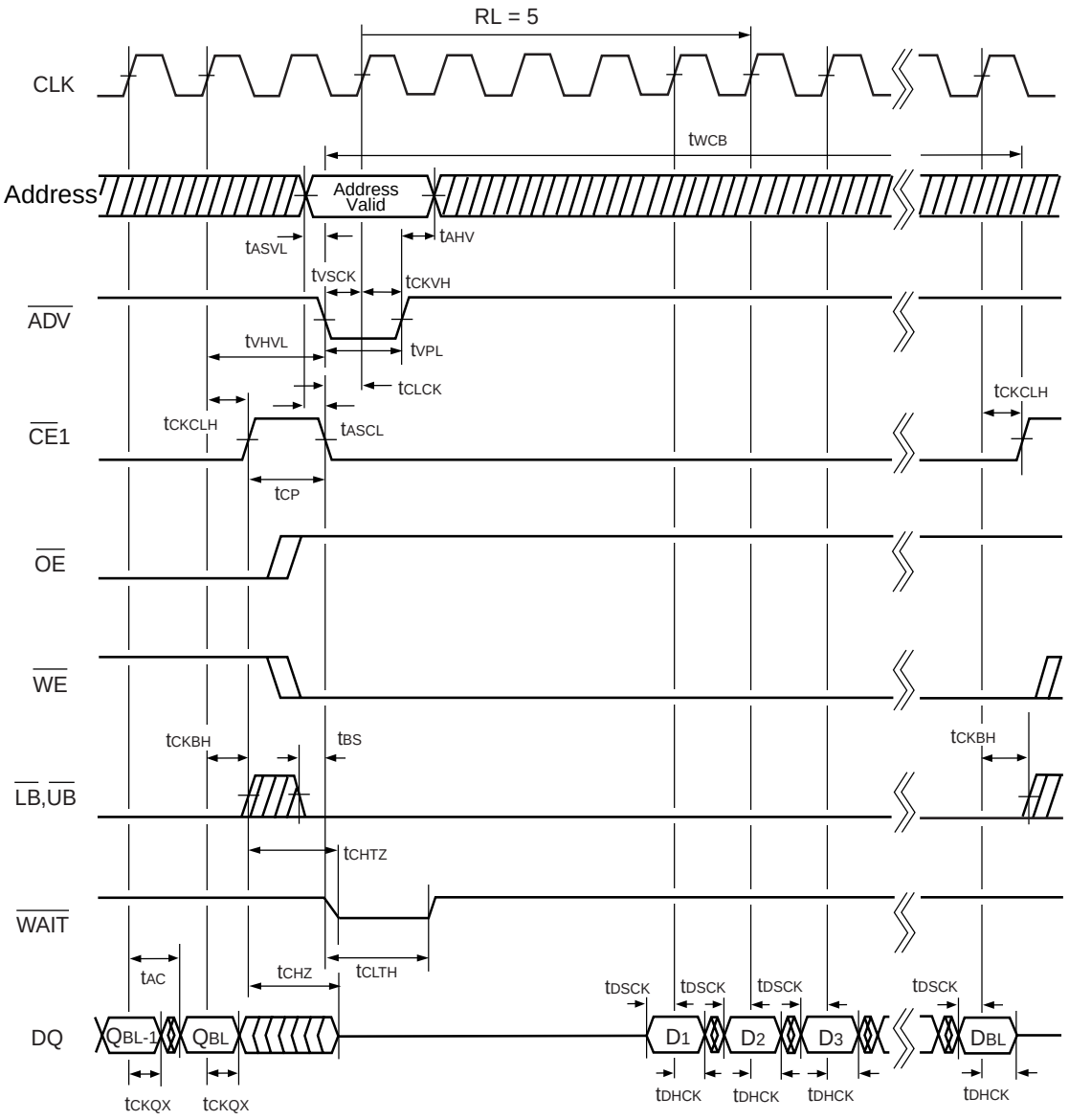
Note : This timing diagram assumes CE2 = H, the valid clock edge on rising edge and BL = 8 or 16.

(26) Synchronous Write Timing 4 ($\overline{WE}$ Level Control, Single Write)



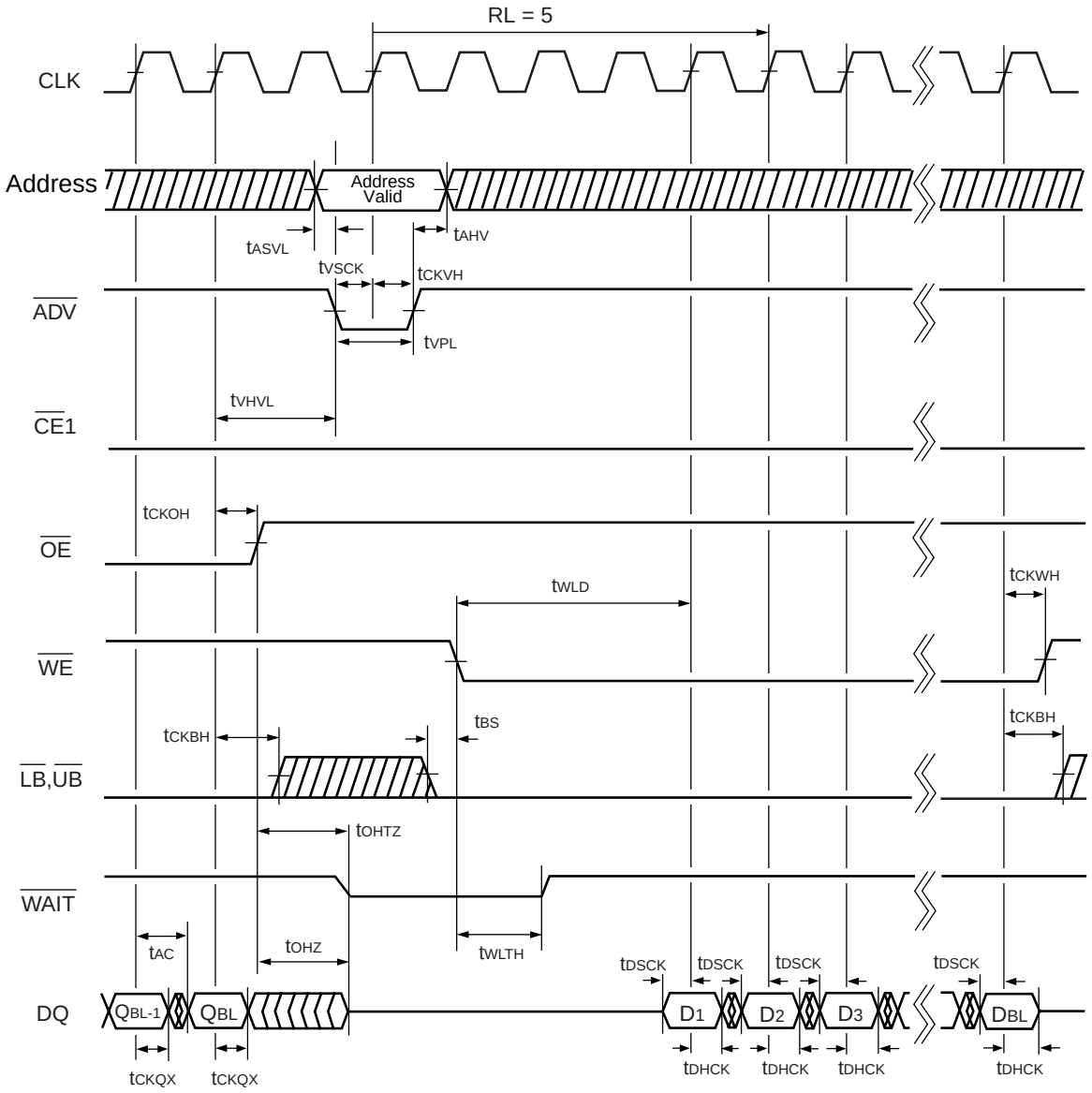
Notes : • This timing diagram assumes CE2 = H, the valid clock edge on rising edge and single write operation.
• Write data is latched on the valid clock edge.

(27) Synchronous Read to Write Timing 1 ($\overline{CE}$1 Control)



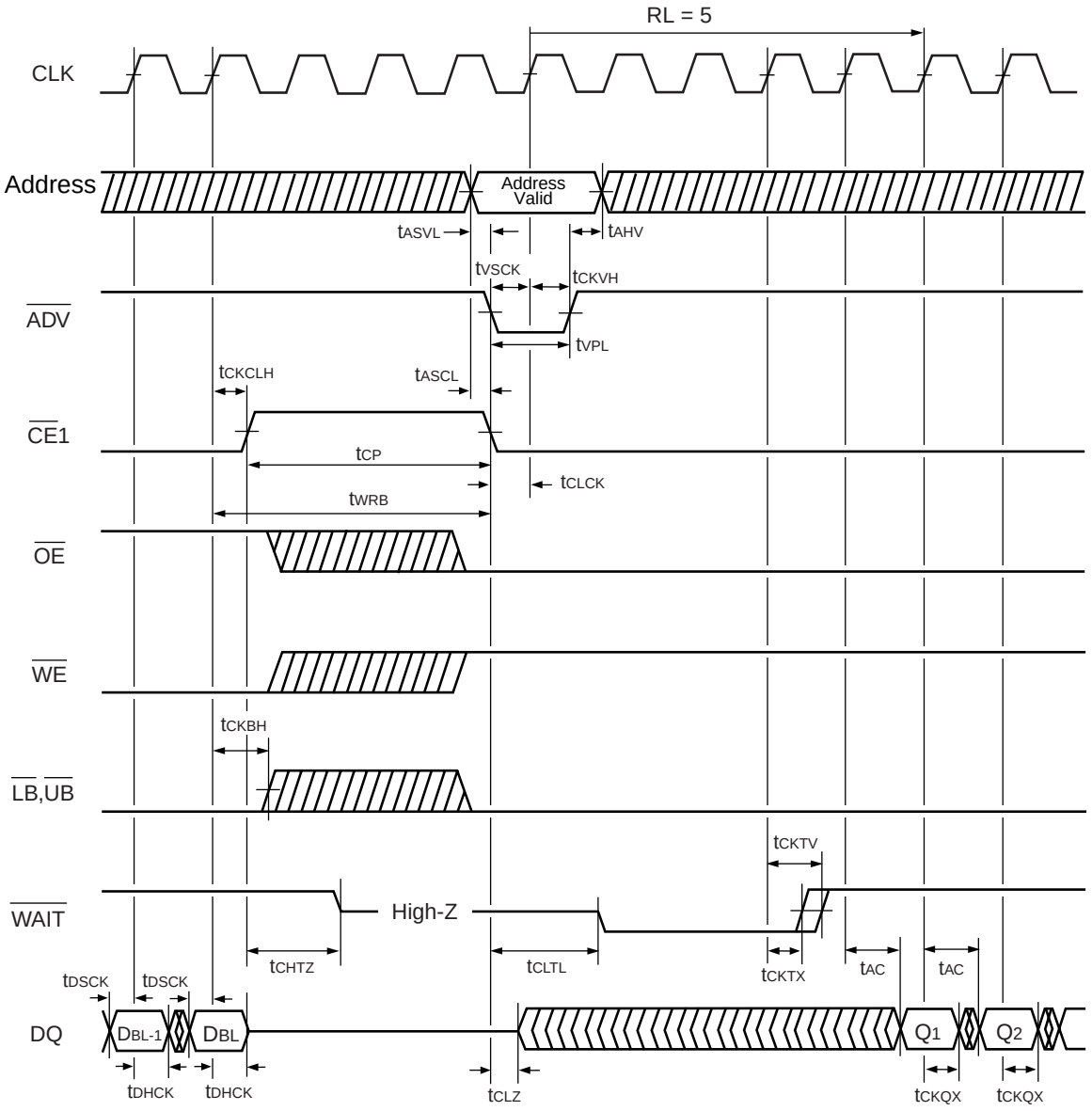
Note : This timing diagram assumes CE2 = H, the valid clock edge on rising edge and BL = 8 or 16.

(28) Synchronous Read to Write Timing 2 ($\overline{ADV}$ Control)



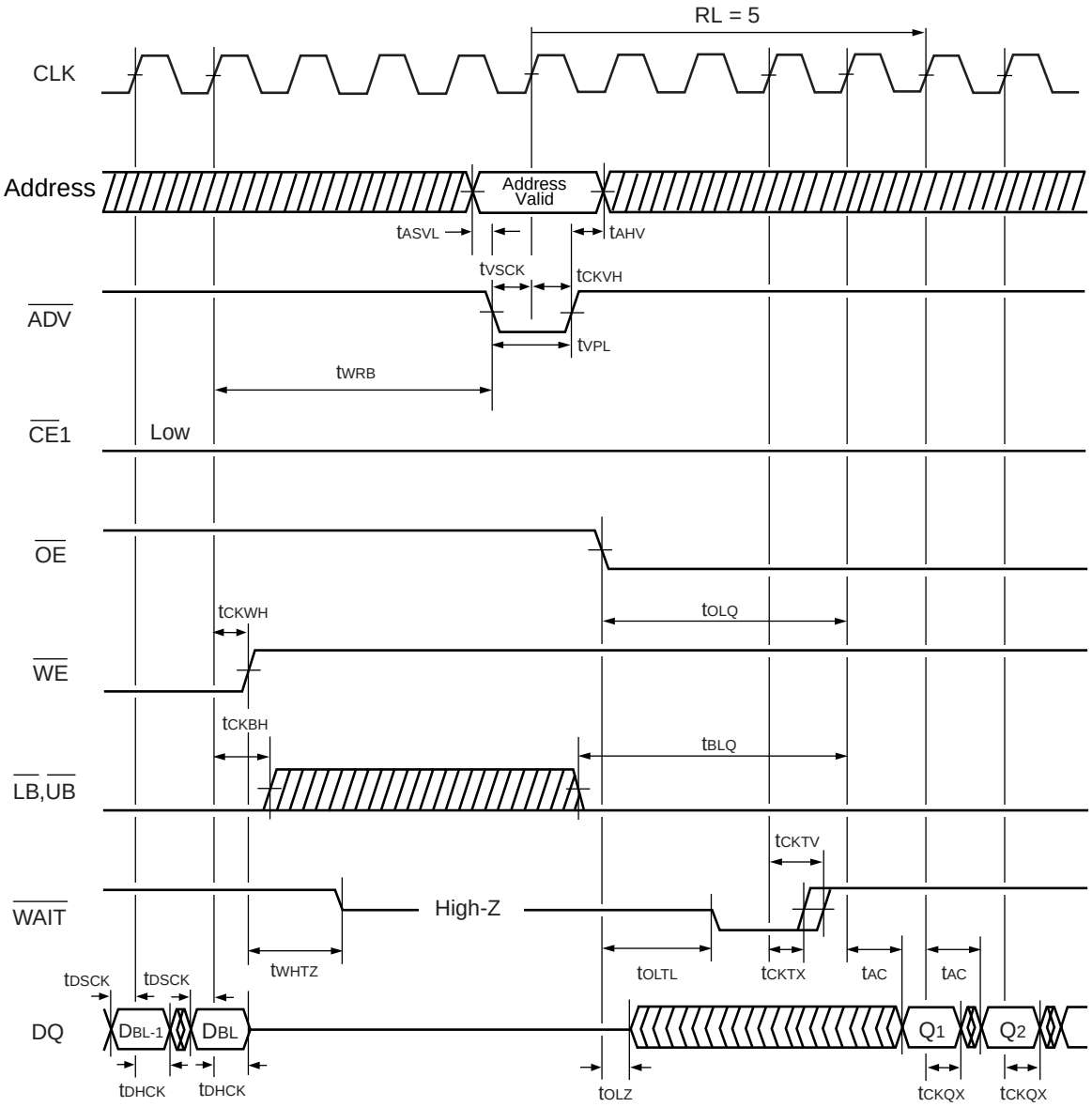
Note : This timing diagram assumes CE2 = H, the valid clock edge on rising edge and BL = 8 or 16.

(29) Synchronous Write to Read Timing 1($\overline{CE}$1 Control)



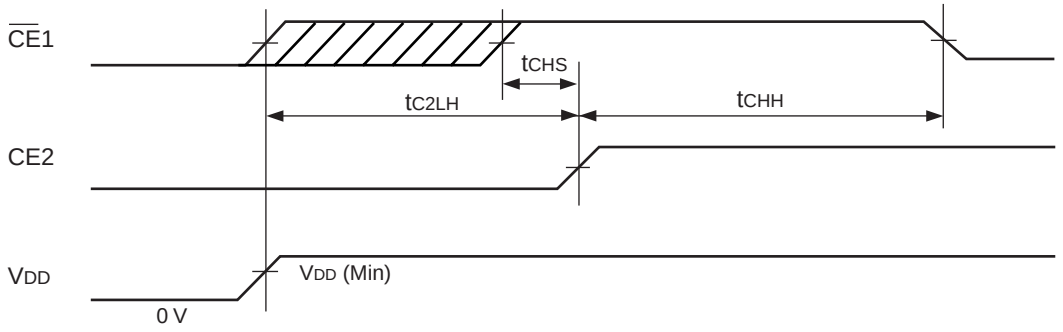
Note : This timing diagram assumes CE2 = H, the valid clock edge on rising edge and BL = 8 or 16.

(30) Synchronous Write to Read Timing 2 ($\overline{ADV}$ Control)



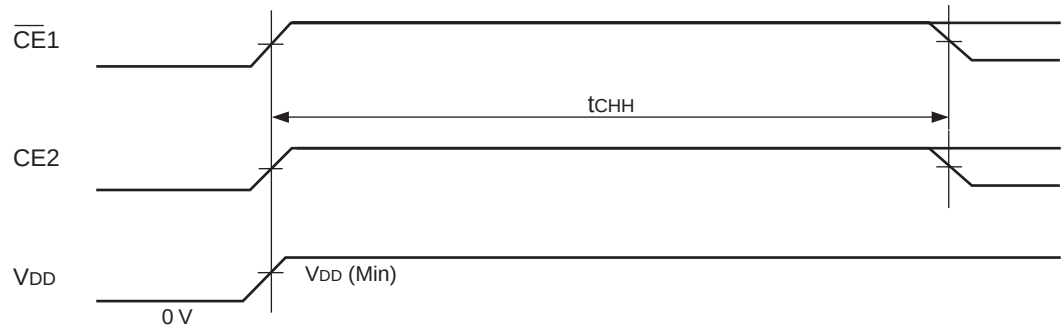
Note : This timing diagram assumes CE2 = H, the valid clock edge on rising edge and BL = 8 or 16.

(31) Power-up Timing 1



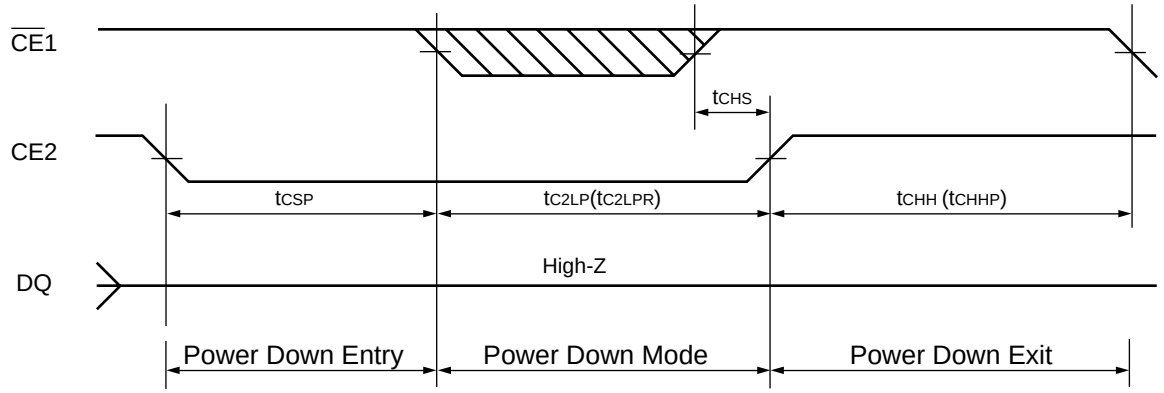
Note : The t_{C2LH} specifies after V_{DD} reaches specified minimum level.

(32) Power-up Timing 2



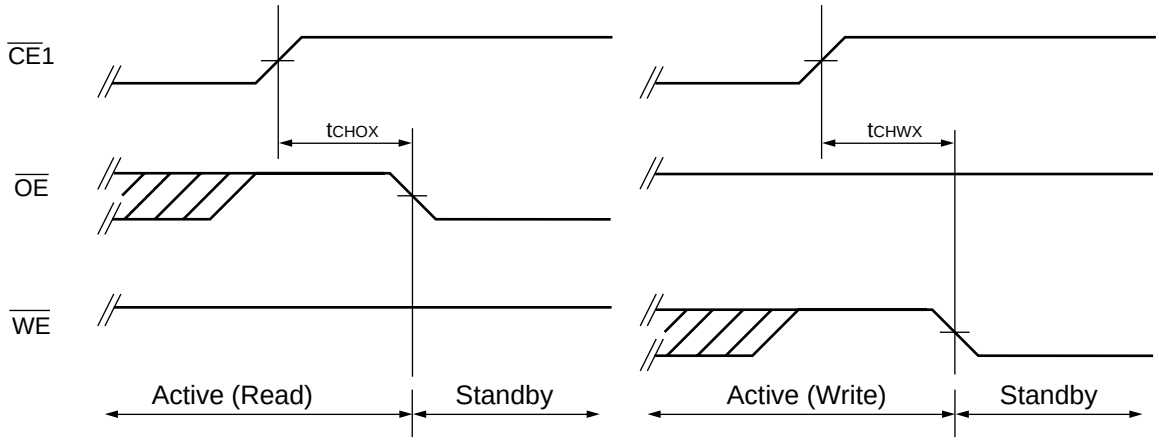
Note : The t_{CHH} specifies after V_{DD} reaches specified minimum level and applicable to both $\overline{CE}1$ and CE2.
If transition time of V_{DD} (from 0 V to V_{DD} (Min)) is longer than 50 ms, "(31) Power-up Timing 1" must be applied.

(33) Power Down Entry and Exit Timing



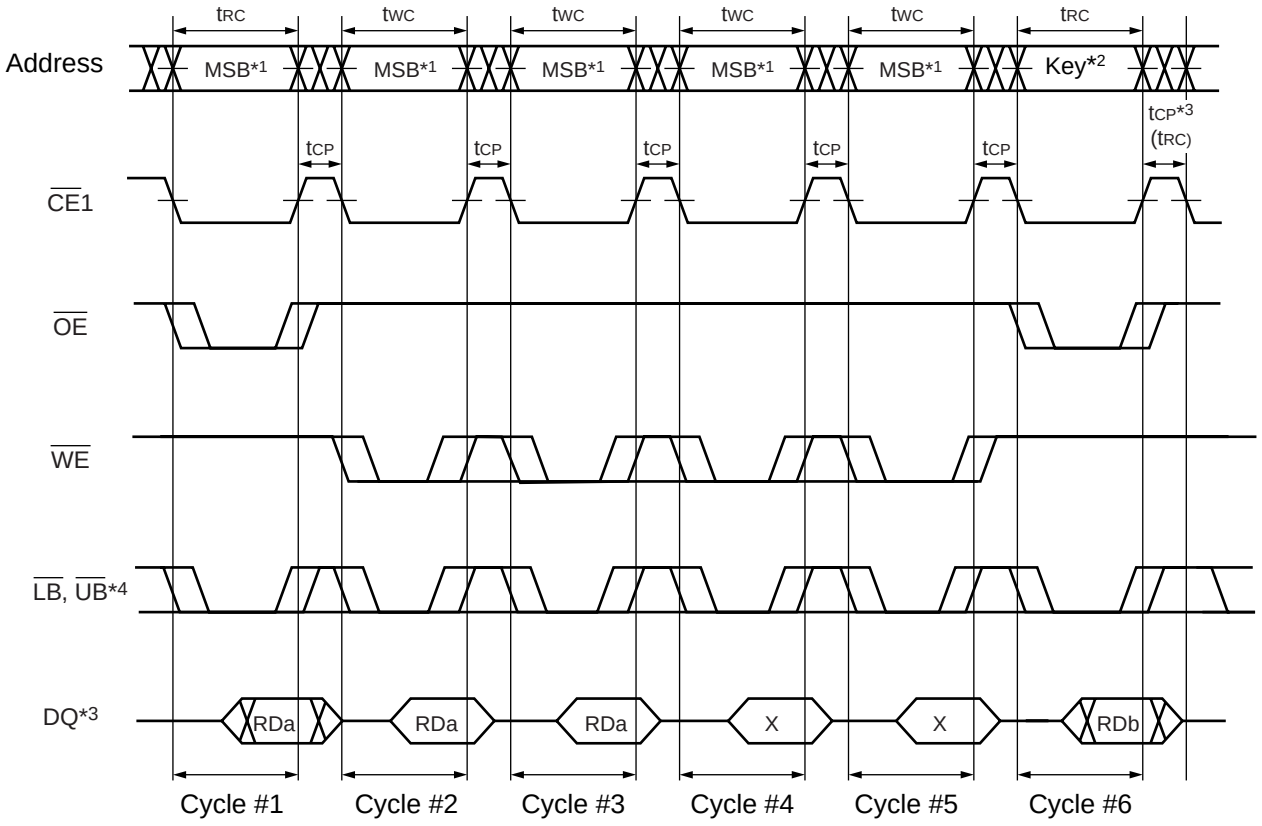
Note : This Power Down mode can be also used as a reset timing if “Power-up timing” above could not be satisfied and Power Down program was not performed prior to this reset.

(34) Standby Entry Timing after Read or Write



Note : Both t_{CHOX} and t_{CHWX} define the earliest entry timing for Standby mode.

(35) Configuration Register Set Timing 1 (Asynchronous Operation)



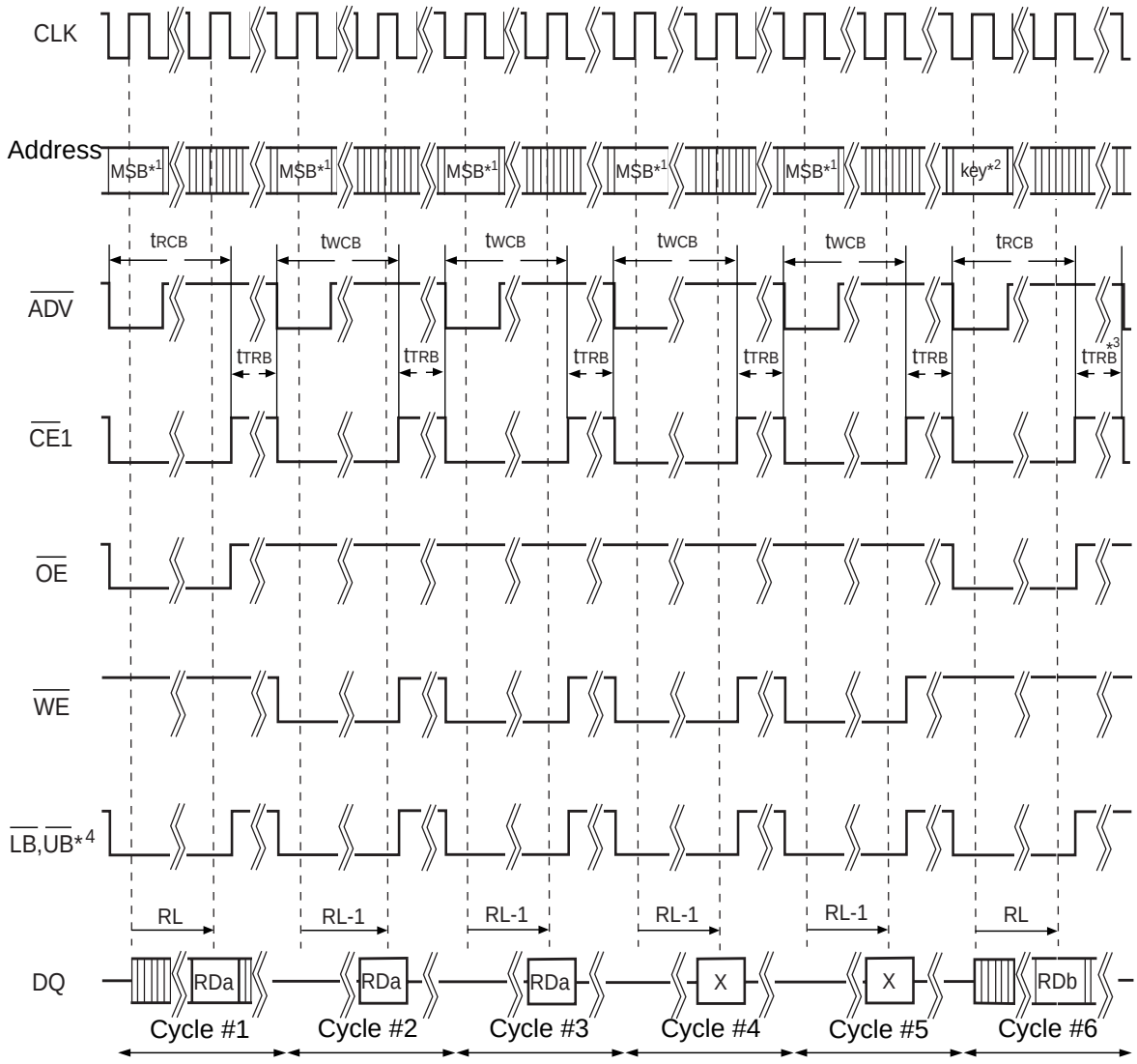
*1 : The all address inputs must be High from Cycle #1 to #5.

*2 : The address key must confirm the format specified in "■FUNCTIONAL DESCRIPTION". If not, the operation and data are not guaranteed.

*3 : After t_{CP} or t_{RC} following Cycle #6, the Configuration Register Set is completed and returned to the normal operation. t_{CP} and t_{RC} are applicable to returning to asynchronous mode and to synchronous mode respectively.

*4 : Byte read or write is available in addition to Word read or write. At least one byte control signal ($\overline{LB}$ or $\overline{UB}$) need to be Low.

(36) Configuration Register Set Timing 2 (Synchronous Operation)



*1 : The all address inputs must be High from Cycle #1 to #5.

*2 : The address key must confirm the format specified in "■FUNCTIONAL DESCRIPTION". If not, the operation and data are not guaranteed.

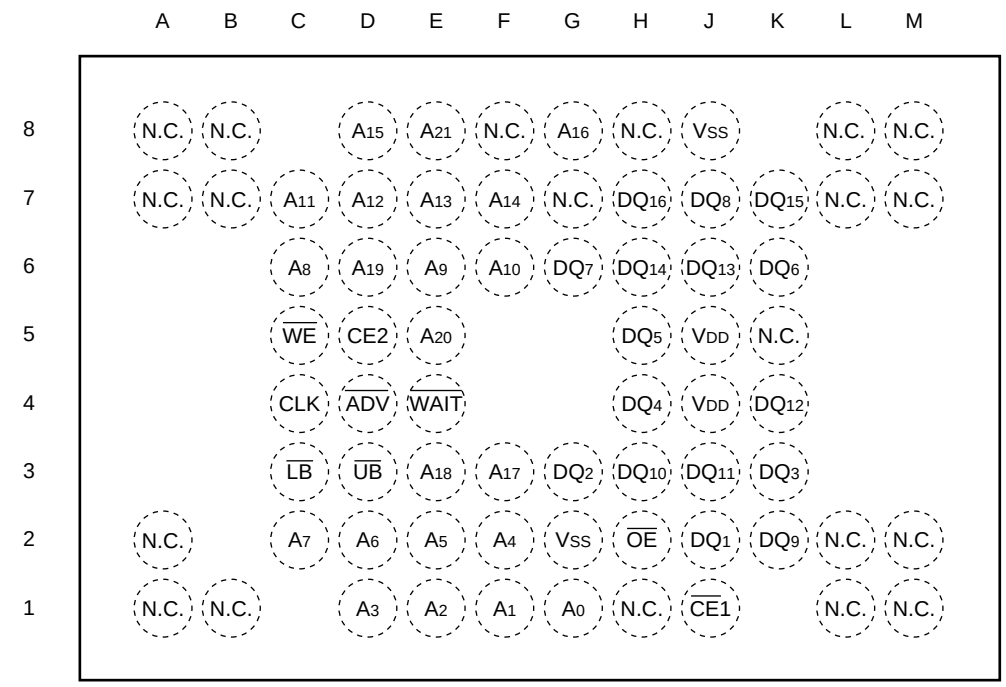
*3 : After t_{TRB} following Cycle #6, the Configuration Register Set is completed and returned to the normal operation.

*4 : Byte read or write is available in addition to Word read or write. At least one byte control signal ($\overline{LB}$ or $\overline{UB}$) need to be Low.

■ PACKAGE FOR ENGINEERING SAMPLES

- **Pin Assignment**

(TOP VIEW)



(BGA-71P-M03)

- **Pin Description**

Pin Name	Description
A_{21} to A_0	Address Input
$\overline{CE}1$	Chip Enable (Low Active)
CE2	Chip Enable (High Active)
$\overline{WE}$	Write Enable (Low Active)
$\overline{OE}$	Output Enable (Low Active)
$\overline{LB}$	Lower Byte Control (Low Active)
$\overline{UB}$	Upper Byte Control (Low Active)
CLK	Clock Input
$\overline{ADV}$	Address Valid Input (Low Active)
$\overline{WAIT}$	Wait Output
DQ_8 to DQ_1	Lower Byte Data Input/Output
DQ_{16} to DQ_9	Upper Byte Data Input/Output
V_{DD}	Power Supply
V_{SS}	Ground
NC	No Conection

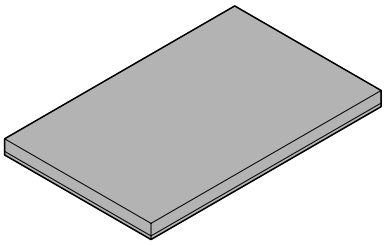
- **Package Capacitance**

(f = 1 MHz, T_A = +25 °C)

Parameter	Symbol	Test conditions	Value			Unit
			Min	Typ	Max	
Address Input Capacitance	C_{IN1}	V_{IN} = 0 V	—	—	5	pF
Control Input Capacitance	C_{IN2}	V_{IN} = 0 V	—	—	5	pF
Data Input/Output Capacitance	$C_{I/O}$	V_{IO} = 0 V	—	—	8	pF

- **Package View**

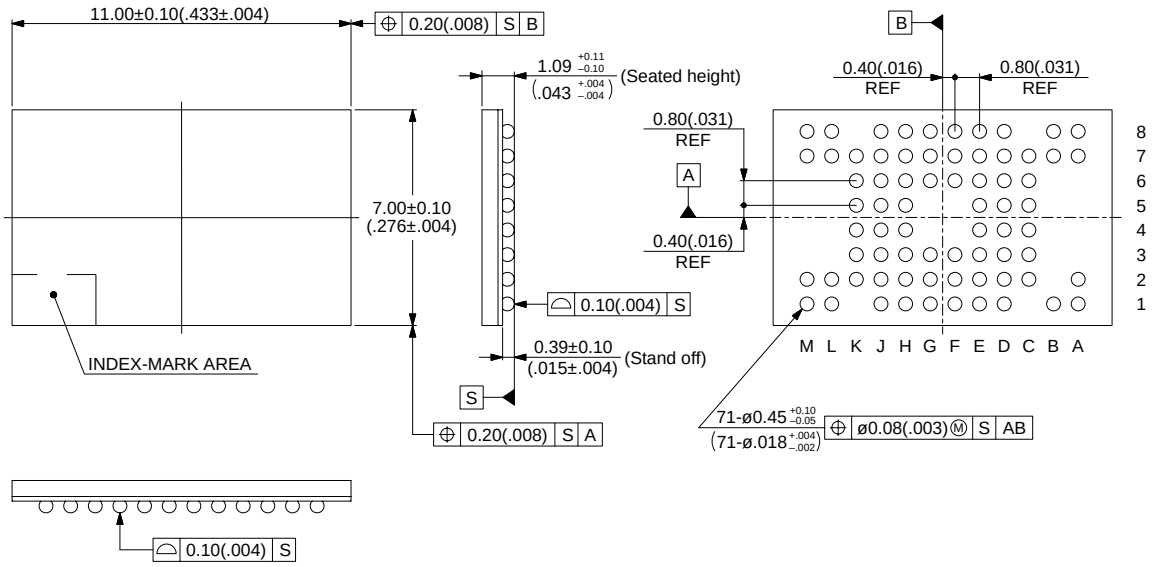
71-pin plastic FBGA



(BGA-71P-M03)

- **Package Dimension**

71-pin plastic FBGA
(BGA-71P-M03)



Dimensions in mm (inches)
Note : The values in parentheses are reference values.

■ ORDERING INFORMATION

Part Number	Shipping Form	Remarks
MB82DBS04163C-70LWFKT	wafer	

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F0601