

# MB834000A/AL

## CMOS 4M-BIT MASK READ ONLY MEMORY

### 512K x 8 CMOS MASK READ ONLY MEMORY

The Fujitsu MB834000A/AL is a CMOS Si-gate mask-programmable static read only memory organized as 524, 288 words by 8 bits.

All pins are TTL-compatible and 3-state output level. The device is fully-static operatable (i.e. no need of clock signal) with a single +5V power supply. Also, the MB834000AL can be used with a single +3V power supply which is required for battery powered applications.

The MB834000A/AL is designed for applications such as character generator and program strage which require large memory capacity and high-speed/low-power operation.

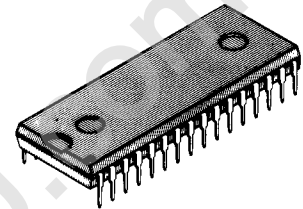
- Organization: 524, 288 words x 8 bits
- Access time: 200ns max. @  $V_{CC} = 5V$  (MB834000A)  
400ns max. @  $V_{CC} = 3V$  (MB834000AL)
- Completely static operation: No clock required
- TTL compatible Input/Output
- Three state output
- Single +5V power supply (MB834000A/AL)  
Single +3V power supply (MB834000AL)
- Power dissipation: 220mW max. (Active) @  $V_{CC} = 5V$  (MB834000A/AL)  
40mW max. (Active) @  $V_{CC} = 3V$  (MB834000AL)
- JEDEC standard 32-pin Plastic DIP: Suffix: P
- 32-pin Plastic Small Outline Package (SOP): Suffix: PF
- 32-pin Plastic Thin Small Outline Package (TSOP):  
Suffix: PFTN(Normal Bend)  
Suffix: PFTR(Reversed Bend)

### ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Supply Voltage	$V_{CC}$	-0.3 to +7.0 *	V
Input Voltage	$V_{IN}$	-0.5 to $V_{CC} + 0.5$ *	V
Output Voltage	$V_{OUT}$	-0.5 to $V_{CC} + 0.5$ *	V
Temperature Under Bias	$T_{BIAS}$	-10 to +85	°C
Storage Temperature Range	$T_{STG}$	-45 to +125	°C

\* Referenced to GND

**NOTE:** Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

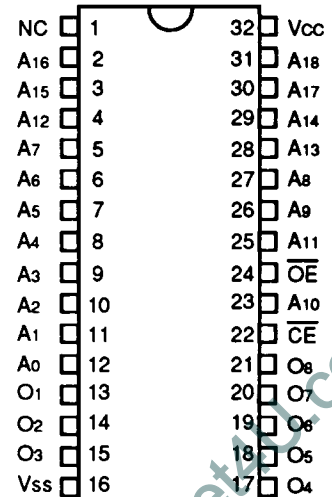


PLASTIC PACKAGE  
DIP-32P-M01

FPT-32P-M03 See Page 6  
FPT-32P-M04 See Page 7  
FPT-32P-M05 See Page 8

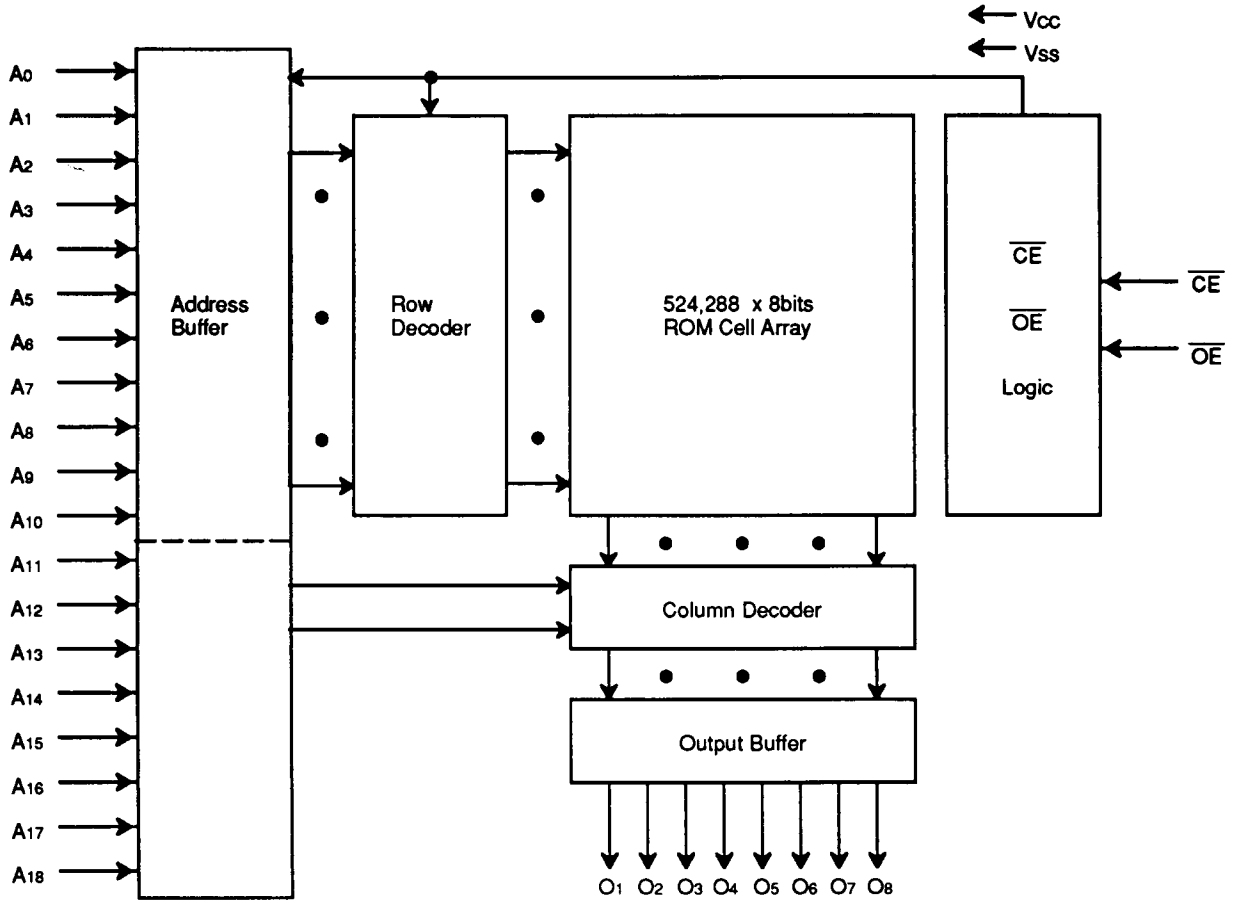
### PIN ASSIGNMENT

(TOP VIEW)



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 — MB834000A/AL BLOCK DIAGRAM



TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	Mode	Output	Power Dissipation Mode
H	X	NOTSELECTED	High-Z	STANDBY
L	H	NOT SELECTED	High-Z	ACTIVE
L	L	SELECTED	Dout	ACTIVE

## CAPACITANCE (TA=25°C, f=1MHz)

Parameter	Symbol	Min	Typ	Max	Unit
Output Capacitance (VOUT=0V)	COUT			15	pF
Input Capacitance (VIN=0V)	CIN			10	pF

## RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	MB834000A/AL			MB834000AL			Unit
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage	V <sub>CC</sub>	4.5	5.0	5.5	2.7	3.0	3.3	V
Ambient Temperature	T <sub>A</sub>	0		70	0		70	°C

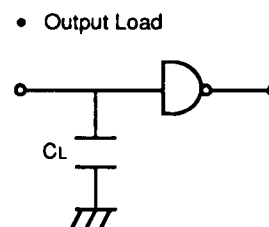
## DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Test Condition	Symbol	MB834000A/AL			MB834000AL			Unit
			Min	Typ	Max	Min	Typ	Max	
Active Supply Current	$\overline{CE}=V_{IL}$ , Minimum Cycle Output = Open	I <sub>CC</sub>			50			12	mA
Standby Supply Current	$\overline{CE}=V_{IH}$	I <sub>SB1</sub>			1			0.5	mA
	$\overline{CE}=V_{CC}=V_{IH}$ , V <sub>IN</sub> =GND or V <sub>CC</sub>	I <sub>SB2</sub>			10			10	μA
Input Leakage Current	V <sub>IN</sub> =0 to V <sub>CC</sub>	I <sub>LI</sub>	-10		10	-5		5	μA
Output Leakage Current	$\overline{CE}=V_{IH}$ $\overline{OE}=V_{IH}$	I <sub>LVO</sub>	-10		10	-5		5	μA
Input Low Voltage		V <sub>IL</sub>	-0.3		0.8	-0.3		0.6	V
Input High Voltage		V <sub>IH</sub>	2.2		V <sub>CC</sub> +0.3	V <sub>CC</sub> ×0.7		V <sub>CC</sub> +0.3	V
Output High Voltage	I <sub>OH</sub> =-400μA	V <sub>OH</sub>	2.4			2.0			V
Output Low Voltage	I <sub>OL</sub> =2.1mA	V <sub>OL</sub>			0.4				V
	I <sub>OL</sub> =1.0mA						0.4		

**Fig. 2 — AC TEST CONDITIONS**

- Input Pulse Level : 0.6 to 2.4V @V<sub>CC</sub> = 5V (MB834000A/AL)  
0.4 to V<sub>CC</sub>×0.8V @V<sub>CC</sub> = 3V(MB834000AL)
- Input Pulse Rise and Fall Time : τ<sub>r</sub>=5ns
- Timing Reference Levels : Input: V<sub>IL</sub>=0.8V, V<sub>IH</sub>=2.2V / Output: V<sub>OL</sub>=0.8V, V<sub>OH</sub>=2.2V  
@V<sub>CC</sub> = 5V (MB834000A/AL)  
: Input: V<sub>IL</sub>=0.6V, V<sub>IH</sub>=V<sub>CC</sub>×0.7V / Output: V<sub>OL</sub>=V<sub>OH</sub>=1.5V  
@V<sub>CC</sub> = 3V (MB834000AL)  
: 1 TTL Gate and 100pF



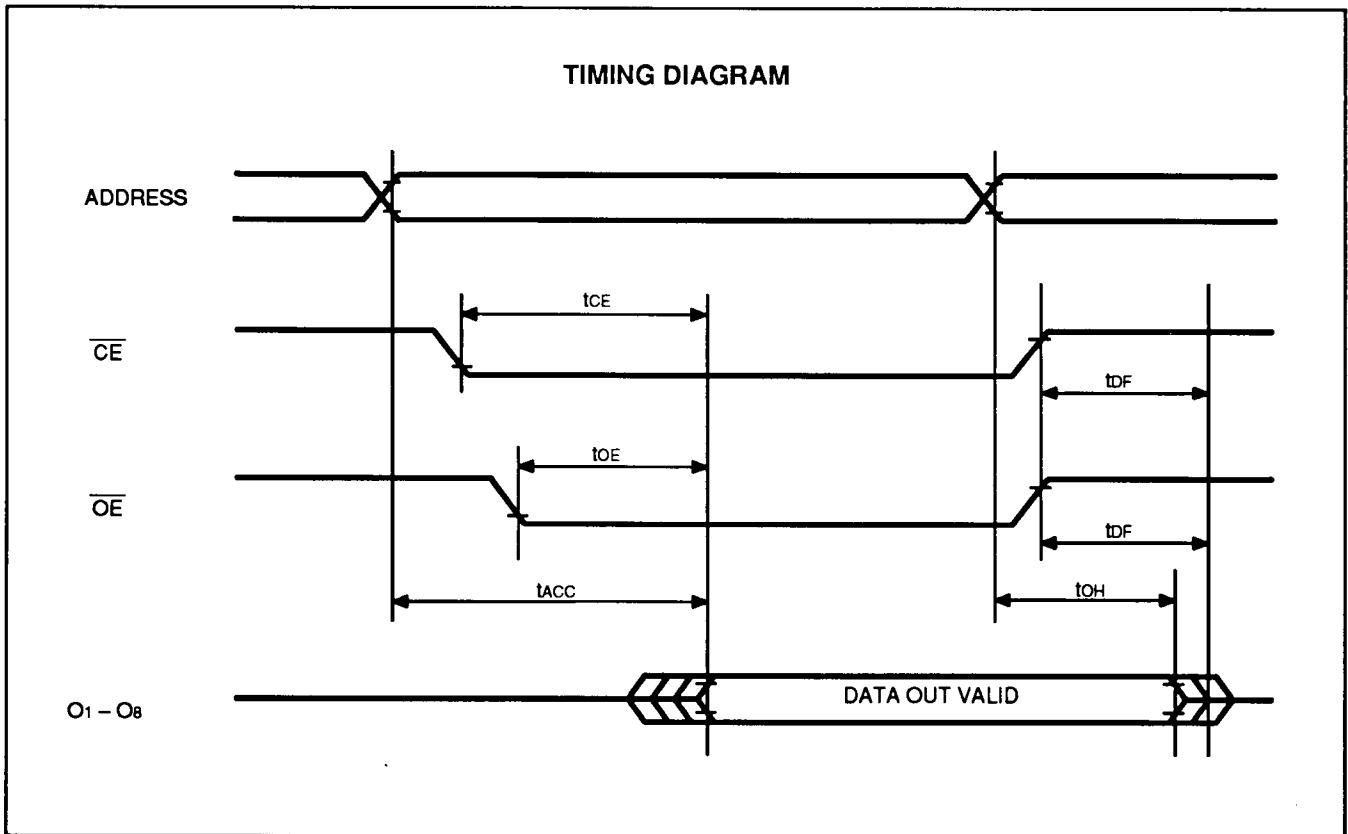
# AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Test Condition	Symbol	MB834000A/AL		MB834000AL		Unit
			Min	Max	Min	Max	
Address Access Time	$\overline{CE}=\overline{OE}=V_{IL}$	tACC		200		400	ns
Chip Enable Access Time	$\overline{OE}=V_{IL}$	tCE		200		400	ns
Output Enable Access Time		tOE		80		200	ns
Output Disable Time *2		tDF		60		120	ns
Output Hold Time	$\overline{CE}=\overline{OE}=V_{IL}$	tOH	0		0		ns

\*1: When continuously switching between 3V operation and 5V operation, during VCC transition the  $\overline{CE}$  should be High state (Standby mode).

\*2: tDF is specified by either of  $\overline{CE}$  or  $\overline{OE}$  changing to High earlier.

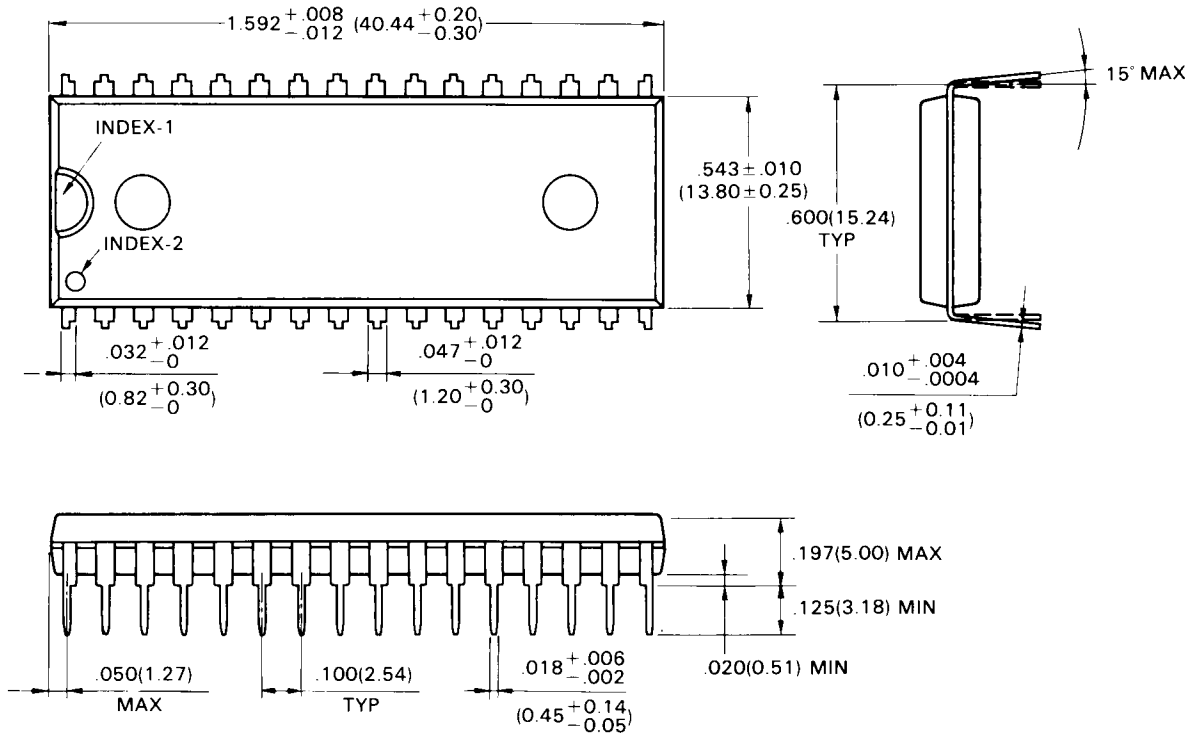


# PACKAGE DIMENSIONS

(Suffix: P)

## 32-LEAD PLASTIC DUAL IN-LINE PACKAGE

(Case No. : DIP-32P-M01)

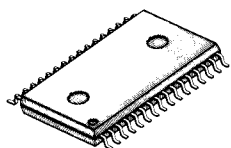


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Dimensions in  
inches (millimeters)

# PACKAGE DIMENSIONS (Continued)

(Suffix: PF)



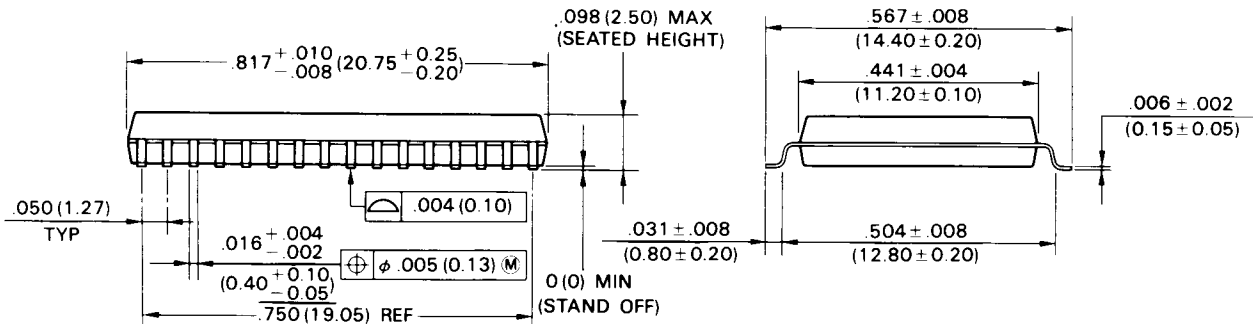
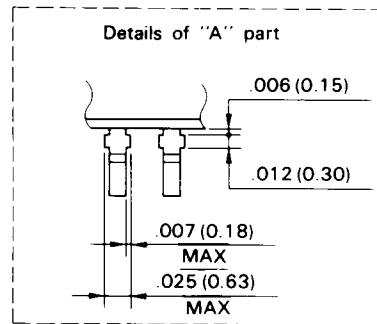
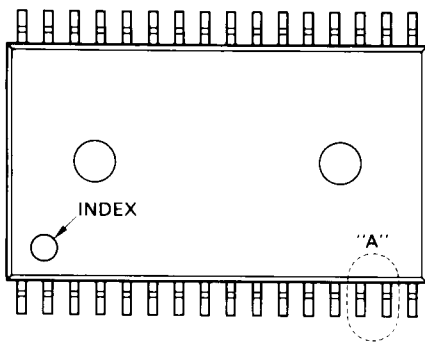
**PLASTIC PACKAGE**  
FPT-32P-M03

**PIN ASSIGNMENT**

NC.	1		32	Vcc
A16	2		31	A18
A15	3		30	A17
A12	4		29	A14
A7	5		28	A13
A6	6		27	A8
A5	7		26	A9
A4	8	( TOP VIEW )	25	A11
A3	9		24	$\overline{OE}$
A2	10		23	A10
A1	11		22	$\overline{CE}$
A0	12		21	O8
O1	13		20	O7
O2	14		19	O6
O3	15		17	O5
Vss	16		18	O4

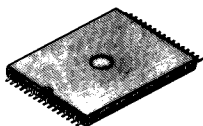
## 32-LEAD PLASTIC FLAT PACKAGE

(Case No. : FPT-32P-M03)



# PACKAGE DIMENSIONS (Continued)

(Suffix: PFTN)



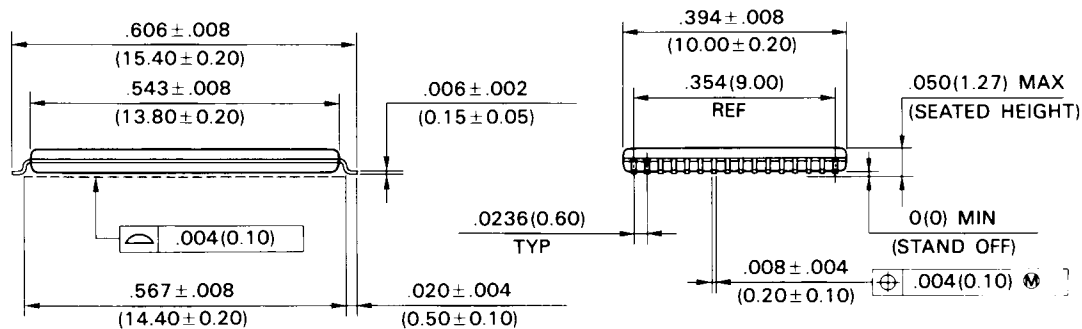
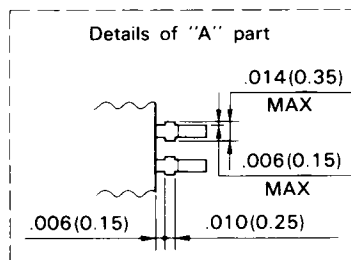
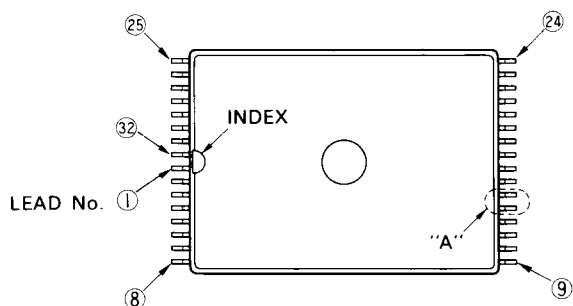
**PLASTIC PACKAGE**  
**FPT-32P-M04**

**PIN ASSIGNMENT**  
(Normal Bend)

A11	25		24	OE
A9	26	( Marking Face )	23	A10
A8	27		22	CE
A13	28		21	O8
A14	29		20	O7
A17	30		19	O6
A18	31		18	O5
VCC	32		17	O4
NC	1		16	VSS
A16	2		15	O3
A15	3		14	O2
A12	4		13	O1
A7	5		12	A0
A6	6		11	A1
A5	7		10	A2
A4	8		9	A3

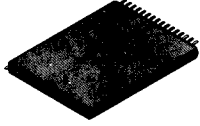
## 32-LEAD PLASTIC FLAT PACKAGE

(Case No. : FPT-32P-M04)



# PACKAGE DIMENSIONS (Continued)

(Suffix: PFTR)



**PLASTIC PACKAGE  
FPT-32P-M05**

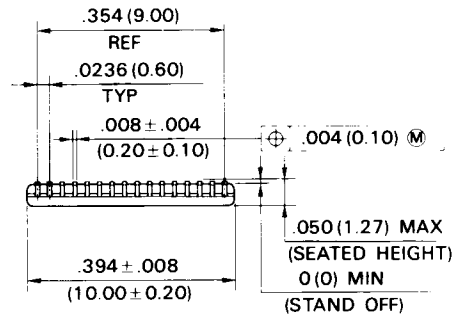
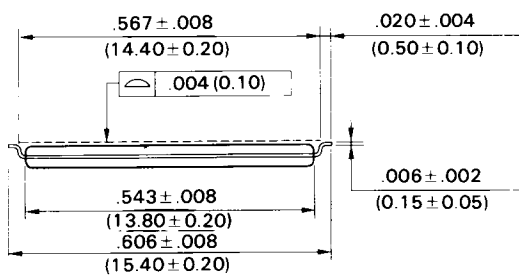
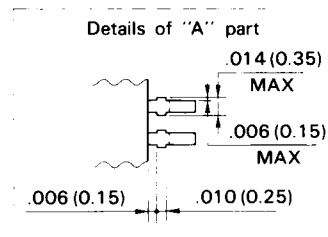
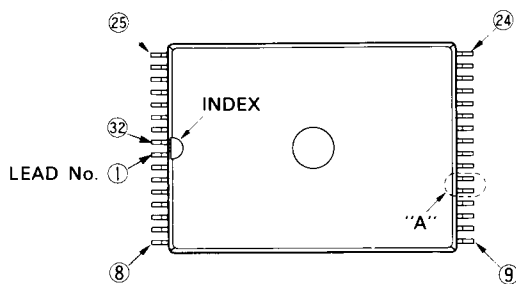
**PIN ASSIGNMENT  
(Reversed Bend)**

( Marking Face )

A4		8		9		A3
A5		7		10		A2
A6		6		11		A1
A7		5		12		A0
A12		4		13		O1
A15		3		14		O2
A16		2		15		O3
NC.		1		16		VSS
VCC		32		17		O4
A18		31		18		O5
A17		30		19		O6
A14		29		20		O7
A13		28		21		O8
A8		27		22		$\overline{CE}$
A9		26		23		A10
A11		25		24		$\overline{OE}$

## 32-LEAD PLASTIC FLAT PACKAGE

(Case No. : FPT-32P-M05)





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