Preliminary

MOS Memories

FUJITSU

MB83512-15

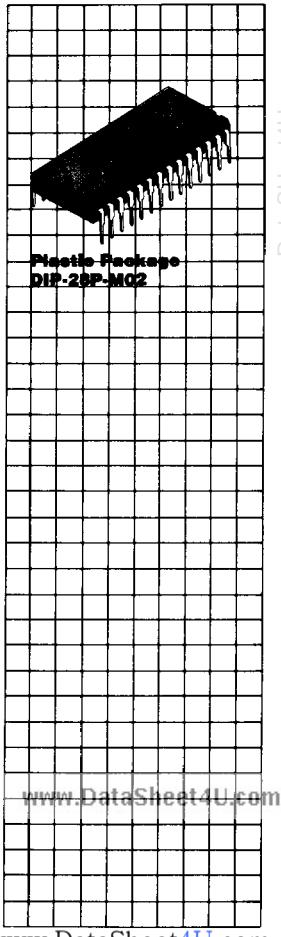
CMOS 524,288-Bit Mask-Programmable Read Only Memory

Description

The Fujitsu MB83512 is a CMOS Si-gate mask-programmable static read only memory organized as 65,536 words by 8-bits.

The MB83512 has TTL-compatible I/O and TRI-state output level with fully-static operation (i.e. no need of clock signal) and single +5V power supply. The device is designed for applications such as character generator or program storage which require large memory capacity and high-speed/low-power operation.

The MB83512 is packaged in a 28-pin dual-in-line package and its pin-out is compatible with standard 28-pin EPROM.



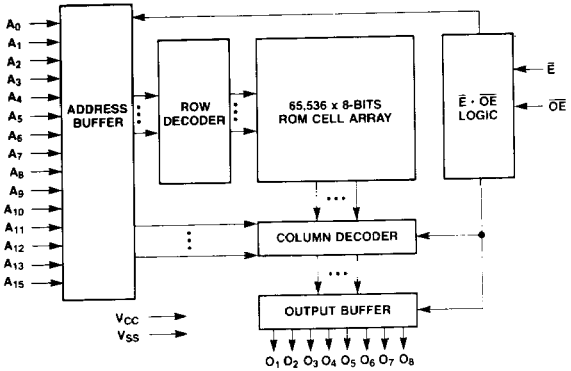
Plastic Package
DIP-28P-M02

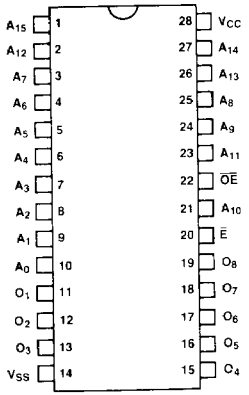
Features

- 65,536 words x 8-bits organization
- Fast access time: 150 ns max.
- Complete static operation: No clock required
- ALL inputs and outputs are TTL compatible
- Three-state outputs
- +5V supply voltage
- Low power consumption: 220 mW (Operation) 16.5 mW (Standby, TTL input level)
- 275 μW (Standby, CMOS input level)
- Standard 28-pin DIP

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this impedance circuit.

MB83512-15 Block Diagram and Pin Assignment





TRUTH TABLE

Ē	$\overline{OE}$	MODE	OUTPUT	POWER CONSUMPTION MODE
H	X	NON-SELECTED	HIGH-Z	STANDBY
L	H	NON-SELECTED	HIGH-Z	ACTIVE
L	L	SELECTED	OUTPUT	ACTIVE

Absolute Maximum Ratings
(See Note)

Rating	Symbol	Value	Unit
Storage temperature range	T_{STG}	−45 to +125	°C
Temperature under bias	T_{BIAS}	−10 to +85	°C
Supply voltage	V_{CC}	−0.3 to +7.0	V
Input voltage	V_{IN}	−0.5 to V_{CC} + 0.5	V
Output voltage	V_{OUT}	−0.5 to V_{CC} + 0.5	V

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance
(T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit
Output Capacitance (V_{OUT} = 0V)	C_{OUT}			10	pF
Input Capacitance (V_{IN} = 0V)	C_{IN}			7	pF

Recommended Operating Conditions
(Reference to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input low voltage	V_{IL}	−0.3		0.8	V
Input high voltage	V_{IH}	2.2		V_{CC} + 0.3	V
Ambient temperature	T_A	0		70	°C

DC Characteristics

(Recommended operating conditions unless otherwise noted.)

Parameter	Test Conditions	Symbol	MB83512-15 Min	MB83512-15 Max	Unit
Standby supply current	$\overline{E} = V_{IH}$	I_{SB1}		3	mA
	$\overline{E} = V_{CC}$, V_{IN} = GND or V_{CC}	I_{SB2}		50	μA
Active supply current	$\overline{E} = V_{IL}$, minimum cycle	I_{CC}		40	mA
Input leakage current	V_{IN} = 0V to V_{CC}	I_{LI}	−10	10	μA
Output leakage current	$\overline{E} = V_{IH}$, or $\overline{OE} = V_{IH}$	I_{LO}	−10	10	μA
Output high voltage	I_{OH} = −400 μA	V_{OH}	2.4		V
Output low voltage	I_{OL} = 2.1 mA	V_{OL}		0.4	V

AC Characteristics

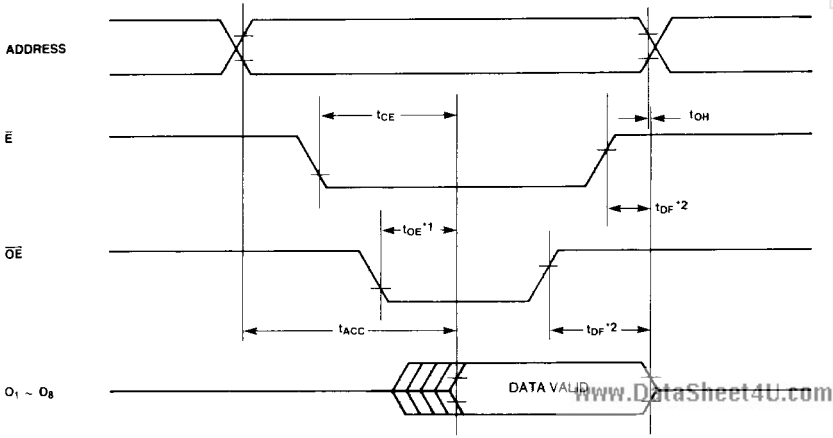
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB83512-15 Min	Typ	Max	Unit
Address access time ($\overline{E} = \overline{OE} = V_{IL}$)	t_{ACC}			150	ns
Chip enable access time ($\overline{OE} = V_{IL}$)	t_E			150	ns
Output enable access time*1	t_{OE}			80	ns
Output disable time*2	T_{DF}			60	ns
Output hold time	t_{OH}	0			ns

Notes: *1 $\overline{OE}$ may be delayed up to ($t_{ACC} - t_{OE}$) after the falling edge of $\overline{E}$ without impact on t_{ACC}.

*2 t_{DF} is specified from $\overline{OE}$ or $\overline{E}$, whichever occurs earlier.

Timing Diagram

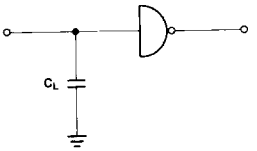


NOTES: *1 $\overline{OE}$ MAY BE DELAYED UP TO ($t_{ACC} - t_{OE}$) AFTER THE FALLING EDGE OF $\overline{E}$ WITHOUT IMPACT ON t_{ACC}.

*2 t_{DF} IS SPECIFIED FROM $\overline{OE}$ OR $\overline{E}$, WHICHEVER OCCURS EARLIER.

AC Test Conditions

Input Pulse Levels:	0.6V to 2.4V
Input Pulse Rise and Fall Time:	t_T = 5 ns
Timing Reference Levels:	Input: V_{IL} = 0.8V, V_{IH} = 2.2V
	Output: V_{OL} = 0.8V, V_{OH} = 2.2V
Output Load:	1 TTL Gate and C_L = 100 pF



Package Dimensions

Dimensions in inches
(millimeters)

28-Lead Plastic Dual In-Line Package
(Case No.: DIP-28P-M02)