July 1990
Edition 2.0

FUJITSU

DATA SHEET

MB841000-80/-80L/-10/-10L/-12/-12L
CMOS 1M LOW POWER SRAM

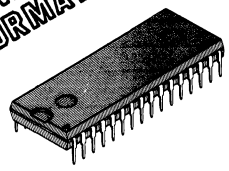
128K Words x 8 Bits CMOS Static Random Access Memory with Data Retention

The Fujitsu MB841000 is a 131,072 words x 8 bits static random access memory fabricated with a CMOS silicon gate process. The memory uses asynchronous circuitry and it may be maintained in any state for an indefinite period of time. All pins are TTL compatible and a single +5 V power supply is required.

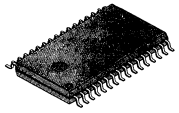
The MB841000 has low power dissipation, low cost, and high performance, and it is ideally suited for use in microprocessor systems and other applications where fast access time and ease of use are required.

- Organization: 131,072 words x 8 bits
- Access time: 80 ns max. (MB841000-80/80L)
  100 ns max. (MB841000-10/10L)
  120 ns max. (MB841000-12/12L)
- Static operation: no clock required
- TTL compatible inputs and outputs
- Three-state outputs
- Single +5 V power supply ±10% tolerance
- Low power standby:
  CMOS level 5.5 mW max. (MB841000-80/-10/-12)
  1.1 mW max. (MB841000-80L/-10L/-12L)
  TTL level 16.5 mW max. (MB841000-80/-80L,-10/-10L,-12/12L)
- Data retention voltage: 2.0 V min.
- Standard 32-pin Plastic Packages:
  DIP (600 mil) MB841000-xx(L)P
  SOP (525 mil) MB841000-xx(L)PF

ADVANCE INFORMATION



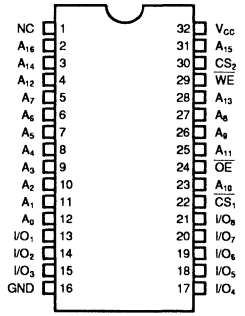
PLASTIC PACKAGE
(DIP-32P-M01)



PLASTIC PACKAGE
(FPT-32P-M03)

PIN ASSIGNMENT

TOP VIEW



Absolute Maximum Ratings (See Note)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7.0	V
Input Voltage	V_{IN}	−0.5 to V_{CC} +0.5	V
Output Voltage	$V_{I/O}$	−0.5 to V_{CC} +0.5	V
Temperature Under Bias	T_{BIAS}	−10 to +85	°C
Storage Temperature Range	T_{STG}	−40 to +125	°C

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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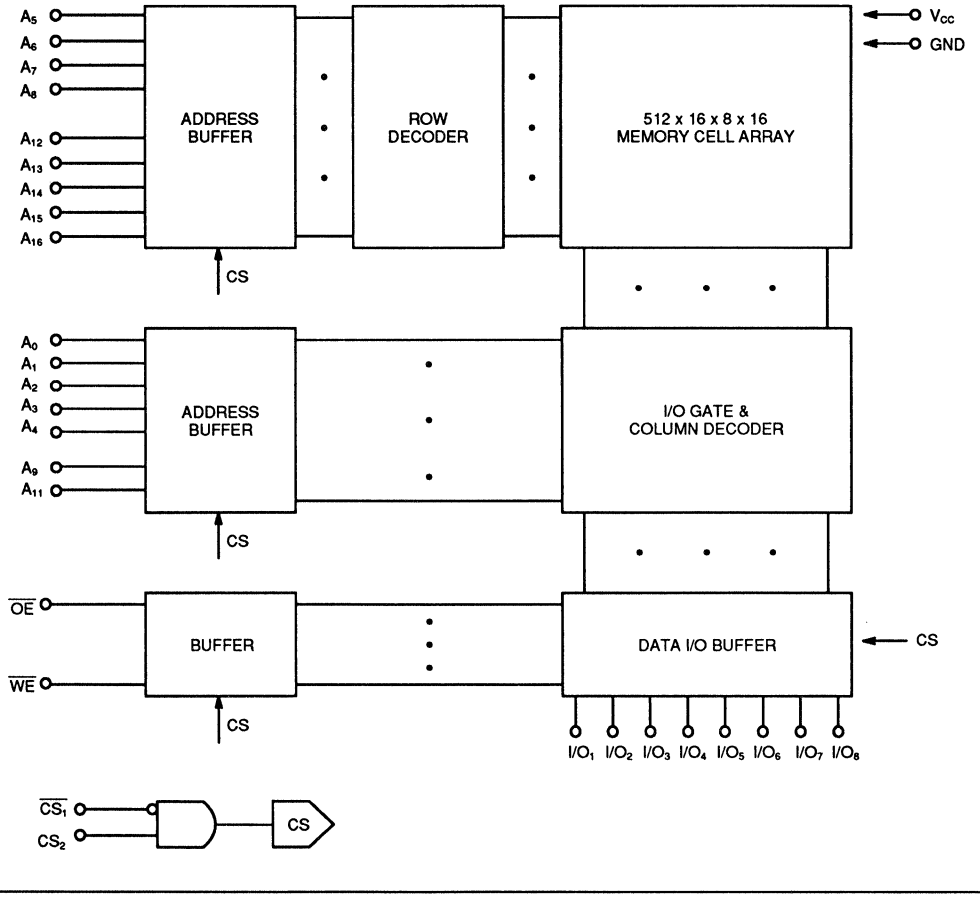
Fig. 1 — MB841000 BLOCK DIAGRAM



CAPACITANCE (T_A= 25° C, f = 1MHz)

Parameter	Symbol	Min	Typ	Max	Unit
I/O Capacitance ($V_{I/O}$=0V)	$C_{I/O}$			10	pF
Input Capacitance (V_{IN}=0V)	C_{IN}			8	pF

PIN DESCRIPTION

Symbol	Pin name	Symbol	Pin name
A_0 to A_{16}	Address Input	$\overline{WE}$	Write Enable
I/O_1 to I/O_8	Data Input/Output	V_{CC}	Power Supply (50±10%)
$\overline{OE}$	Output Enable	GND	Ground
$\overline{CS_1}$	Chip Select 1	NC	No Connect
CS_2	Chip Select 2		

FUNCTION TRUTH TABLE

$\overline{CS_1}$	CS_2	$\overline{OE}$	$\overline{WE}$	MODE	SUPPLY CURRENT	I/O PIN
H	X	X	X	Not Selected	I_{SB}	High–Z
X	L	X	X	Not Selected	I_{SB}	High–Z
L	H	H	H	D_{OUT} Disable	I_{CC}	High–Z
L	H	L	H	Read	I_{CC}	D_{OUT}
L	H	X	L	Write	I_{CC}	D_{IN}

RECOMMENDED OPERATING CONDITION

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ambient Temperature	T_A	0		70	°C

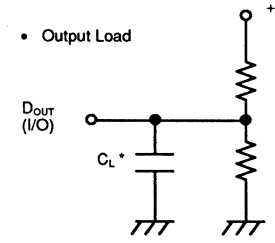
DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Test Condition	Symbol	MB841000 -80/10/12		MB841000 -80L/10L/12L		Unit
			Min	Max	Min	Max	
Standby Supply Current	$CS_2 \leq 0.2V$ or $\overline{CS_1} \geq V_{CC}-0.2V$ ($CS_2 \leq 0.2V$ or $CS_2 \geq V_{CC}-0.2V$)	I_{SB1}		1		0.2	mA
	$\overline{CS_1}=V_{IH}$ or $CS_2=V_{IL}$	I_{SB2}		3		3	mA
Active Supply Current	$V_{IN}=V_{IH}$ or V_{IL}, $\overline{CS_1}=V_{IL}$, $CS_2=V_{IH}$ $I_{OUT}=0mA$	I_{CC1}		5		5	mA
Operating Supply Current	Cycle=Min. Duty=100%, $I_{OUT}=0mA$	I_{CC2}		80		80	mA
Input Leakage Current	$V_{IN}=0V$ to V_{CC}	I_{LI}	–1	1	–1	1	µA
Output Leakage Current	$V_{I/O}=0V$ to V_{CC} $\overline{CS_1}=V_{IH}$ or $CS_2=V_{IL}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$	$I_{LI/O}$	–2	2	–2	2	µA
Input High Voltage		V_{IH}	2.2	V_{CC} +0.3	2.2	V_{CC} +0.3	V
Input Low Voltage		V_{IL}	–0.3*	0.8	–0.3*	0.8	V
Output High Voltage	$I_{OH}=-1.0mA$	V_{OH}	2.4		2.4		V
Output Low Voltage	$I_{OL}=2.1mA$	V_{OL}		0.4		0.4	V

Note : All voltages are referenced to GND.
*** :** –3.0V min. for pulse width less than 20 ns. (V_{IL} min. = –0.3V at DC level.)

Fig.2 – AC TEST CONDITIONS



- Output Load
- Input Pulse Levels: 0.6V to 2.4V
- Input Pulse Rise & Fall Times: 5ns (Transient between 0.8V and 2.2V)
- Timing Reference Levels: Input : $V_{IL}=0.8V, V_{IH}=2.2V$
  Output : $V_{OL}=0.8V, V_{OH}=2.0V$

* Including Jig and stray capacitance

	R_1	R_2	C_L	Parameters Measured
Load I	1.8KΩ	990Ω	100pF	except t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WLZ} and t_{WHZ}
Load II	1.8KΩ	990Ω	5pF	t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WLZ} and t_{WHZ}

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

READ CYCLE *1

Parameter	Symbol	MB841000–80/80L		MB841000–10/10L		MBM841000–12/12L		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	80		100		120		ns
Address Access Time *2	t_{AA}		80		100		120	ns
$\overline{CS_1}$ Access Time *3	t_{AC1}		80		100		120	ns
CS_2 Access Time *3	t_{AC2}		80		100		120	ns
Output Enable to Output Valid	t_{OE}		35		40		50	ns
Output Hold from Address Change	t_{OH}	10		10		10		ns
Chip Select to Output Low–Z *4	t_{CLZ}	10		10		10		ns
Output Enable to Output Low–Z *4	t_{OLZ}	5		5		5		ns
Chip Select to Output High–Z *4	t_{CHZ}		30		35		40	ns
Output Enable to Output High–Z *4	t_{OHZ}		30		35		40	ns

Note: *1 $\overline{WE}$ is high for Read cycle.

*2 Device is continuously selected, $\overline{CS_1}$=$\overline{OE}$=V_{IL}, CS_2=V_{IH}.

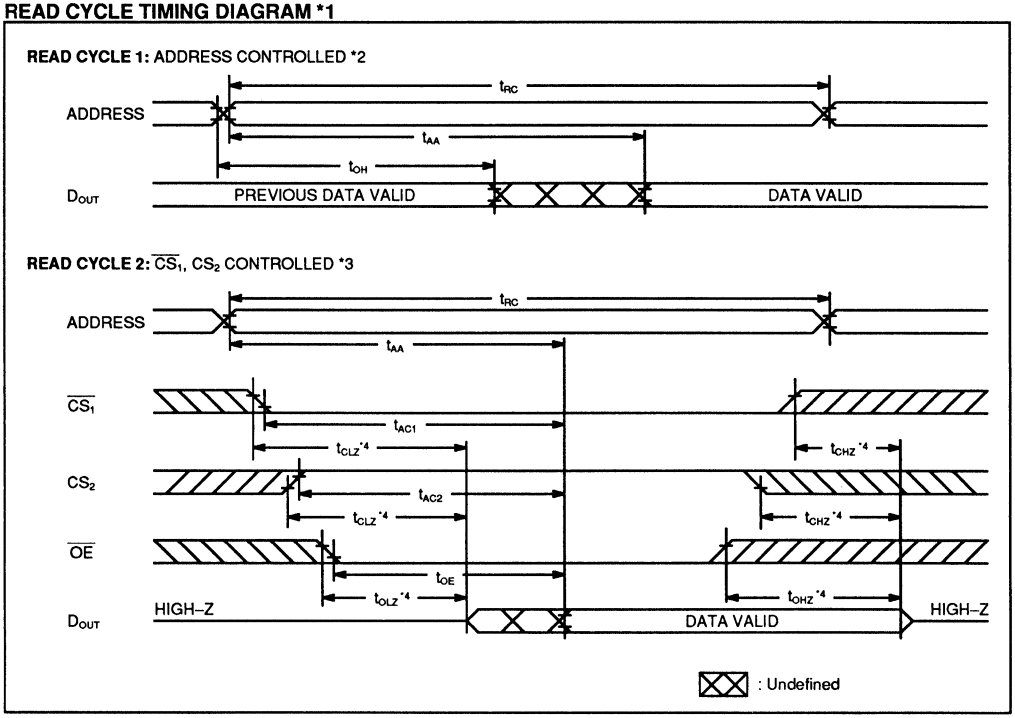
*3 Address valid prior to or coincident with $\overline{CS_1}$ transition low, CS_2 transition high.

*4 Transition is measured at the point of ±500mV from steady state voltage with specified Load II in Fig.2.

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

READ CYCLE TIMING DIAGRAM *1



Note: *1 $\overline{WE}$ is high for Read Cycle.

*2 Device is continuously selected, $\overline{CS_1}$=$\overline{OE}$=V_{IL}, CS_2=V_{IH}.

*3 Address valid prior to or coincident with $\overline{CS_1}$ transition low, CS_2 transition high.

*4 Transition is measured at the point of ±500mV from steady state voltage with specified load II in Fig. 2.

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

WRITE CYCLE *1*2

Parameter	Symbol	MB841000–80/80L		MB841000–10/10L		MBM841000–12/12L		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time *3	t_{WC}	80		100		120		ns
Address Valid to End of Write	t_{AW}	60		80		85		ns
Chip Select to End of Write	t_{CW}	60		80		85		ns
Data Valid to End of Write	t_{DW}	30		40		45		ns
Data Hold Time	t_{DH}	0		0		0		ns
Write Pulse Width	t_{WP}	50		60		70		ns
Address Setup Time	t_{AS}	0		0		0		ns
Write Recovery Time *4	t_{WR}	5		5		5		ns
Write Enable to Output Low–Z *5	t_{WLZ}	5		5		5		ns
Write Enable to Output High–Z *5	t_{WHZ}		30		35		40	ns

Note: *1 If $\overline{OE}$, $\overline{CS_1}$ and CS_2 are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

*2 If $\overline{CS_1}$ goes high or CS_2 goes low simultaneously with $\overline{WE}$ high, the output remains in high impedance state.

*3 All write cycle are determined from last address transition to the first address transition of the next address.

*4 t_{WR} is defined from the end point of WRITE Mode.

*5 Transition is measured at the point of ±500mV from steady state voltage with specified Load II in Fig.2.

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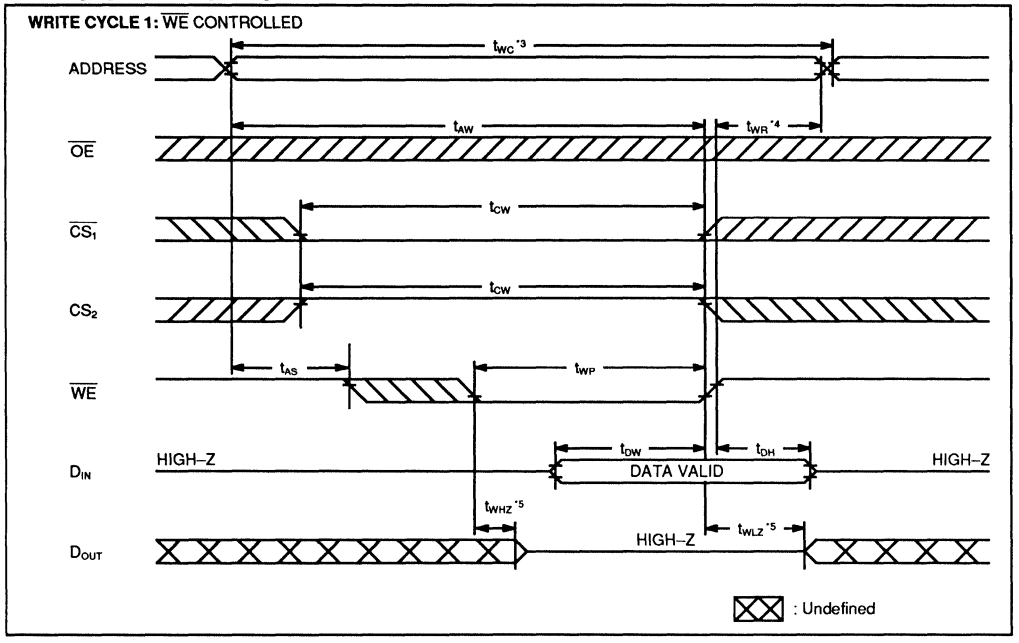
AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

WRITE CYCLE TIMING DIAGRAM *1 *2



Note: *1 If $\overline{OE}$, $\overline{CS_1}$ and CS_2 are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

*2 If $\overline{CS_1}$ goes high or CS_2 goes low simultaneously with $\overline{WE}$ high, the output remains in high impedance state.

*3 All write cycle are determined from last address transition to the first address transition of the next address.

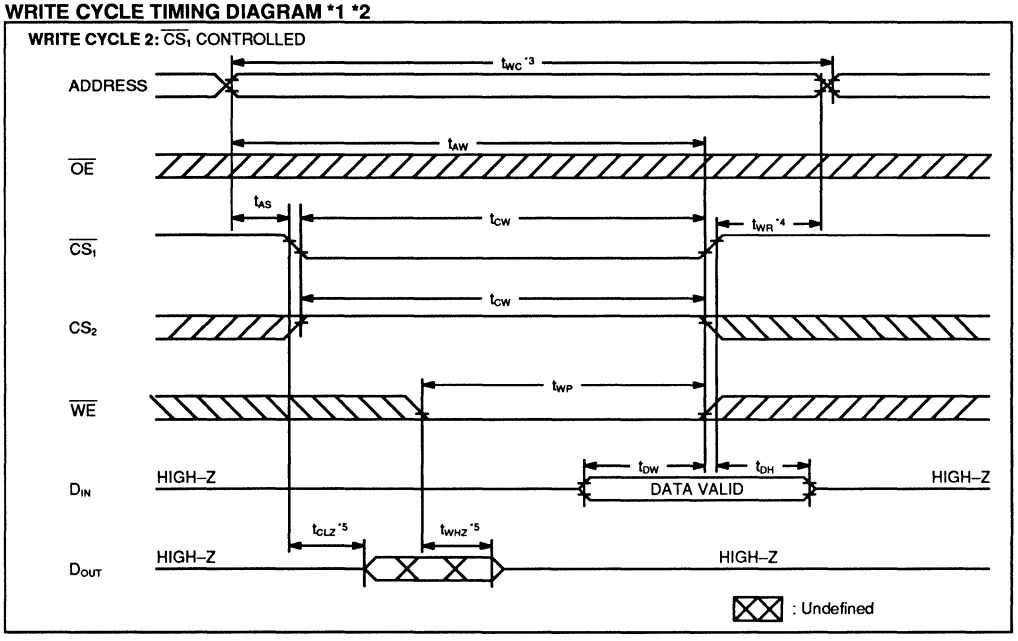
*4 t_{WR} is defined from the end point of WRITE Mode.

*5 Transition is measured at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

WRITE CYCLE TIMING DIAGRAM *1 *2



Note: *1 If $\overline{OE}$, $\overline{CS_1}$ and CS_2 are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

*2 If $\overline{CS_1}$ goes high or CS_2 goes low simultaneously with $\overline{WE}$ high, the output remains in high impedance state.

*3 All write cycle are determined from last address transition to the first address transition of the next address.

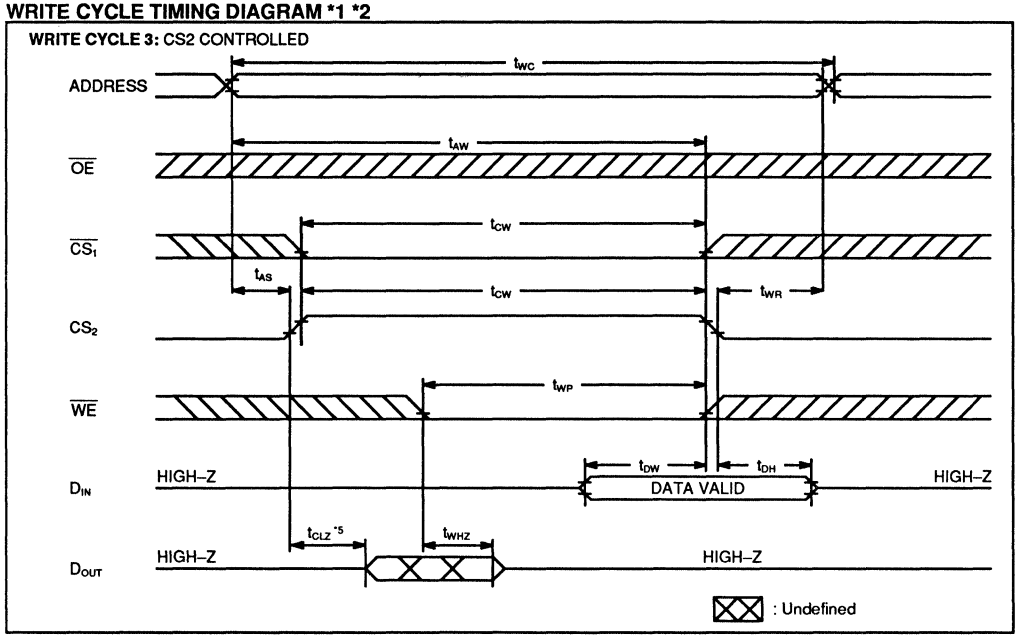
*4 t_{WR} is defined from the end point of WRITE Mode.

*5 Transition is measured at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

WRITE CYCLE TIMING DIAGRAM *1 *2



Note: *1 If $\overline{OE}$, $\overline{CS_1}$ and CS_2 are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

*2 If $\overline{CS_1}$ goes high or CS_2 goes low simultaneously with $\overline{WE}$ high, the output remains in high impedance state.

*3 All write cycle are determined from last address transition to the first address transition of the next address.

*4 t_{WR} is defined from the end point of WRITE Mode.

*5 Transition is measured at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

DATA RETENTION CHARACTERISTICS

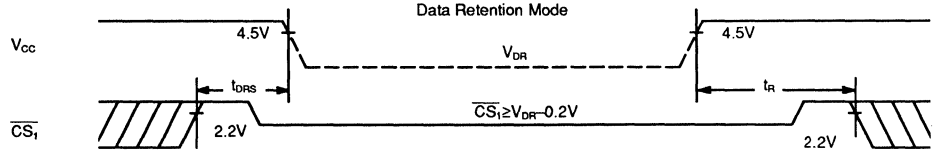
(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Typ	Max	Unit
Data Retention Supply Voltage		V_{DR}	2.0		5.5	V
Data Retention Supply Current *1	Standard	I_{DR}			0.5	mA
	L-Version				0.1 *2	mA
Data Retention Setup Time		t_{DRS}	0			ns
Operation Recovery Time *2		t_R	t_{RC}			ns

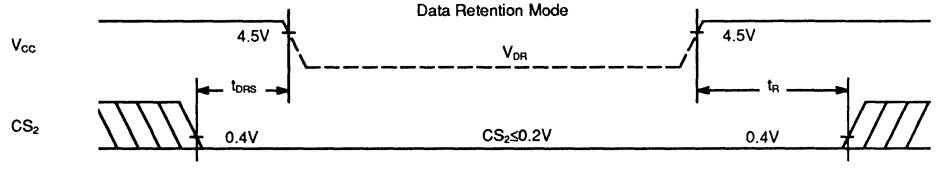
Note: *1 V_{CC}=V_{DR}=3.0V
$\overline{CS_1} \geq V_{DR} - 0.2V$, $CS_2 \geq V_{DR} - 0.2V$ or $CS_2 \leq 0.2V$ (at $\overline{CS_1}$ CONTROLLED)
$CS_2 \leq 0.2V$ (at CS_2 CONTROLLED)
*2 t_{RC}: Read Cycle Time

DATA RETENTION TIMING

$\overline{CS_1}$ CONTROLLED



CS_2 CONTROLLED

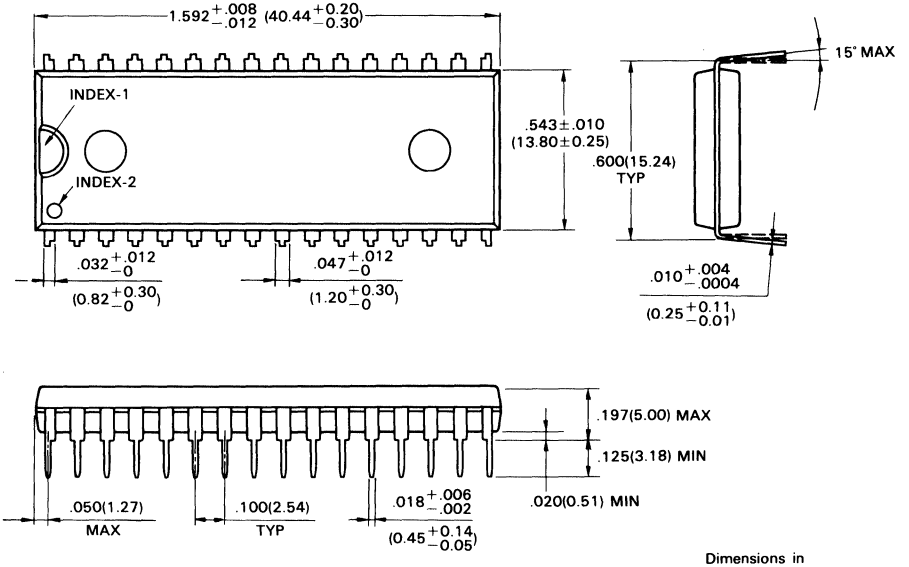


PACKAGE DIMENSIONS

(Suffix: P)

32-LEAD PLASTIC DUAL IN-LINE PACKAGE

(Case No. : DIP-32P-M01)

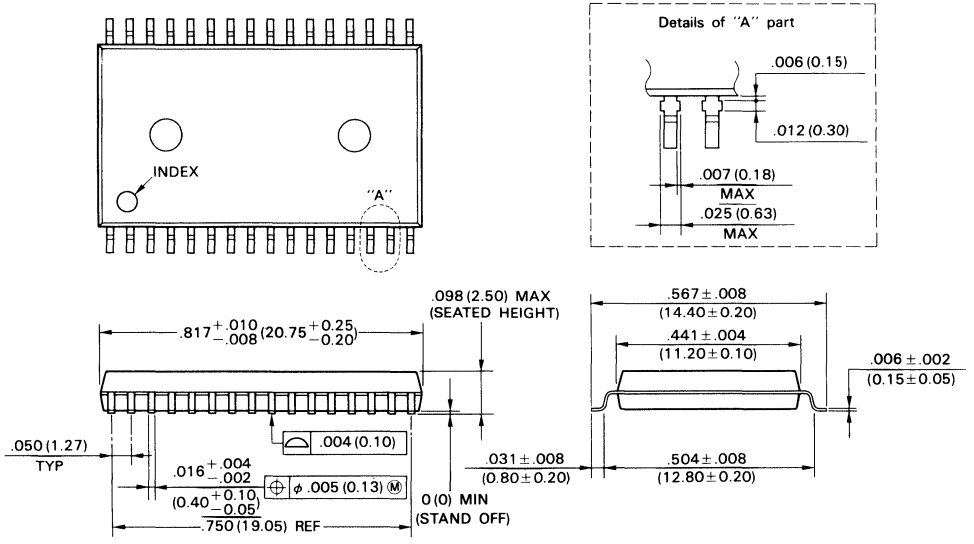


Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS

(Suffix: PF)

32-LEAD PLASTIC FLAT PACKAGE
(Case No. : FPT-32P-M03)



Dimensions in
inches (millimeters)

3