

MCP (Multi-Chip Package) FLASH MEMORY & SRAM CMOS

8M (× 8/× 16) FLASH MEMORY & 1M (× 8) STATIC RAM

MB84VA2006-10/MB84VA2007-10

■ FEATURES

- Power supply voltage of 2.7 to 3.6 V
- High performance
100 ns maximum access time
- Operating Temperature
-20 to +85°C

— FLASH MEMORY

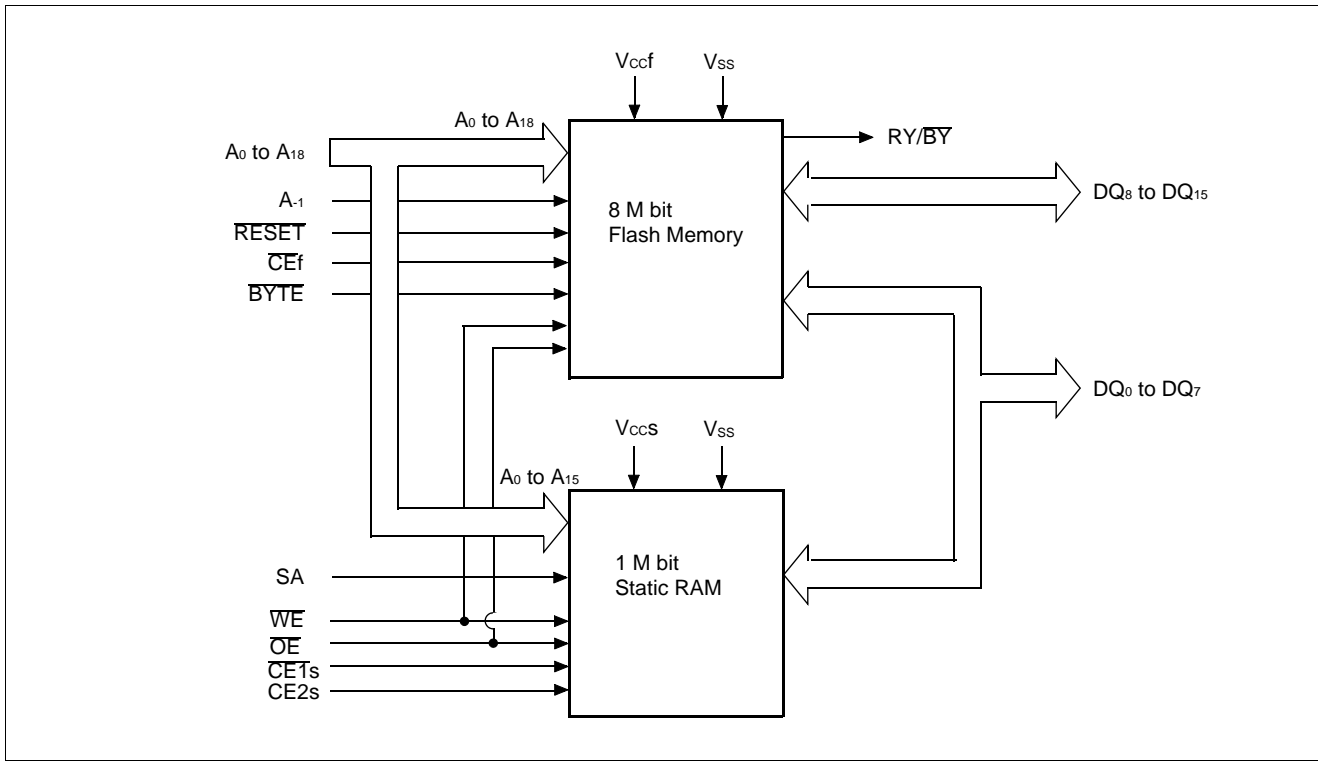
- Minimum 100,000 write/erase cycles
- Sector erase architecture
One 16 K byte, two 8 K bytes, one 32 K byte, and fifteen 64 K bytes.
Any combination of sectors can be concurrently erased. Also supports full chip erase.
- Boot Code Sector Architecture
MB84VA2006: Top sector
MB84VA2007: Bottom sector
- Embedded Erase™ Algorithms
Automatically pre-programs and erases the chip or any sector
- Embedded Program™ Algorithms
Automatically writes and verifies data at specified address
- Data Polling and Toggle Bit feature for detection of program or erase cycle completion
- Ready-Busy output (RY/BY)
Hardware method for detection of program or erase cycle completion
- Automatic sleep mode
When addresses remain stable, automatically switch themselves to low power mode.
- Low V_{cc} write inhibit ≤ 2.5 V
- Erase Suspend/Resume
Suspends the erase operation to allow a read in another sector within the same device
- Please refer to "MBM29LV800TA/BA" data sheet in detailed function

— SRAM

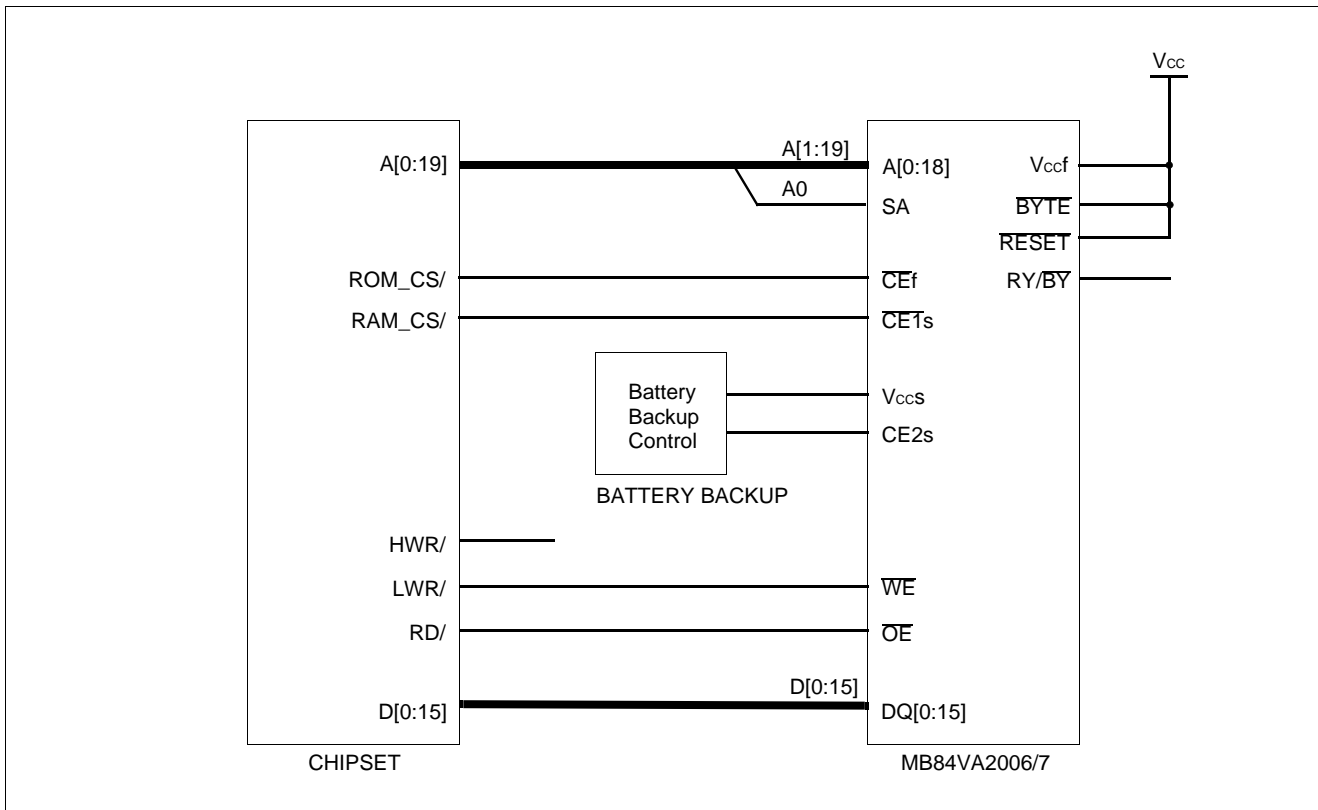
- Power dissipation
Operating : 35 mA max.
Standby : 30 μA max.
- Power down features using $\overline{CE1}$ s and CE2s
- Data retention supply voltage: 2.0 V to 3.6 V

MB84VA2006-10/MB84VA2007-10

■ BLOCK DIAGRAM



■ EXAMPLE OF CONNECTION WITH CHIPSET



■ PIN ASSIGNMENTS

(Top View)

| | A | B | C | D | E | F | G | H |
|---|-------------------|------------------|-----------------|------------------|------------------|------------------|---------------------|-----------------------------------|
| 6 | $\overline{CE}1s$ | V _{SS} | DQ ₁ | A ₁ | A ₂ | A ₄ | CE2s | A ₉ |
| 5 | A ₁₀ | DQ ₅ | DQ ₂ | A ₀ | A ₃ | A ₇ | RY/ \overline{BY} | A ₁₄ |
| 4 | \overline{OE} | DQ ₇ | DQ ₄ | DQ ₀ | A ₆ | A ₁₈ | RESET | A ₁₅ |
| 3 | A ₁₁ | A ₈ | A ₅ | DQ ₈ | DQ ₃ | DQ ₁₂ | A ₁₂ | BYTE |
| 2 | A ₁₃ | A ₁₇ | SA* | $\overline{CE}f$ | DQ ₁₀ | V _{ccf} | DQ ₆ | DQ ₁₅ /A ₋₁ |
| 1 | \overline{WE} | V _{CCS} | A ₁₆ | V _{SS} | DQ ₉ | DQ ₁₁ | DQ ₁₃ | DQ ₁₄ |

*: A₁₆ for SRAM

Table 1 Pin Configuration

| Pin | Function | Input/ Output |
|--|---|------------------|
| A ₀ to A ₁₅ | Address Inputs (Common) | I |
| A ₋₁ , A ₁₆ to A ₁₈ | Address Input (Flash) | I |
| SA | Address Input (SRAM) | I |
| DQ ₀ to DQ ₇ | Data Inputs/Outputs (Common) | I/O |
| DQ ₈ to DQ ₁₅ | Data Inputs/Outputs (Flash) | I/O |
| $\overline{CE}f$ | Chip Enable (Flash) | I |
| $\overline{CE}1s$ | Chip Enable (SRAM) | I |
| CE2s | Chip Enable (SRAM) | I |
| \overline{OE} | Output Enable (Common) | I |
| \overline{WE} | Write Enable (Common) | I |
| RY/ \overline{BY} | Ready/Busy Outputs (Flash) | O |
| BYTE | Selects 8-bit or 16-bit mode (Flash) | I |
| RESET | Hardware Reset Pin/Sector Protection Unlock (Flash) | I |
| N.C. | No Internal Connection | — |
| V _{SS} | Device Ground (Common) | Power |
| V _{ccf} | Device Power Supply (Flash) | Power |
| V _{CCS} | Device Power Supply (SRAM) | Power |

MB84VA2006-10/MB84VA2007-10

■ PRODUCT LINE UP

| | | Flash Memory | SRAM |
|---------------------------------------|--|-----------------------------|------|
| Ordering Part No. | $V_{CC} = 3.0\text{ V} \begin{smallmatrix} +0.6\text{ V} \\ -0.3\text{ V} \end{smallmatrix}$ | MB84VA2006-10/MB84VA2007-10 | |
| Max. Address Access Time (ns) | | 100 | 100 |
| Max. \overline{CE} Access Time (ns) | | 100 | 100 |
| Max. \overline{OE} Access Time (ns) | | 40 | 50 |

■ BUS OPERATIONS

Table 2 User Bus Operations (BYTE= V_{IL})

| Operation (1), (3) | \overline{CEf} | $\overline{CE1s}$ | $\overline{CE2s}$ | \overline{OE} | \overline{WE} | DQ ₀ to DQ ₇ | DQ ₈ to DQ ₁₅ | RESET |
|----------------------|------------------|-------------------|-------------------|-----------------|-----------------|------------------------------------|-------------------------------------|-------|
| Full Standby | H | H | X | X | X | HIGH-Z | HIGH-Z | H |
| | | X | L | | | | | |
| Output Disable | X | X | X | H | H | HIGH-Z | HIGH-Z | H |
| Read from Flash (2) | L | H | X | L | H | D _{OUT} | HIGH-Z | H |
| | | X | L | | | | | |
| Write to Flash | L | H | X | H | L | D _{IN} | HIGH-Z | H |
| | | X | L | | | | | |
| Read from SRAM | H | L | H | L | H | D _{OUT} | HIGH-Z | H |
| Write to SRAM | H | L | H | X | L | D _{IN} | HIGH-Z | H |
| Flash Hardware Reset | X | H | X | X | X | HIGH-Z | HIGH-Z | L |
| | | X | L | | | | | |

Table 3 User Bus Operations (BYTE= V_{IH})

| Operation (1), (3) | \overline{CEf} | $\overline{CE1s}$ | $\overline{CE2s}$ | \overline{OE} | \overline{WE} | DQ ₀ to DQ ₇ | DQ ₈ to DQ ₁₅ | RESET |
|----------------------|------------------|-------------------|-------------------|-----------------|-----------------|------------------------------------|-------------------------------------|-------|
| Full Standby | H | H | X | X | X | HIGH-Z | HIGH-Z | H |
| | | X | L | | | | | |
| Output Disable | X | X | X | H | H | HIGH-Z | HIGH-Z | H |
| Read from Flash (2) | L | H | X | L | H | D _{OUT} | D _{OUT} | H |
| | | X | L | | | | | |
| Write to Flash | L | H | X | H | L | D _{IN} | D _{IN} | H |
| | | X | L | | | | | |
| Read from SRAM | H | L | H | L | H | D _{OUT} | HIGH-Z | H |
| Write to SRAM | H | L | H | X | L | D _{IN} | HIGH-Z | H |
| Flash Hardware Reset | X | H | X | X | X | HIGH-Z | HIGH-Z | L |
| | | X | L | | | | | |

Legend: L = V_{IL} , H = V_{IH} , X = V_{IL} or V_{IH} . See DC Characteristics for voltage levels.

- Notes:**
1. Other operations except for indicated this column are inhibited.
 2. \overline{WE} can be V_{IL} if \overline{OE} is V_{IL} , \overline{OE} at V_{IH} initiates the write operations.
 4. Do not apply $\overline{CEf} = V_{IL}$, $\overline{CE1s} = V_{IL}$ and $\overline{CE2s} = V_{IH}$ at a time.

MB84VA2006-10/MB84VA2007-10

■ FLEXIBLE SECTOR-ERASE ARCHITECTURE on FLASH MEMORY

- One 16 K byte, two 8 K bytes, one 32 K byte, and fifteen 64 K bytes.
- Individual-sector, multiple-sector, or bulk-erase capability.

| | (×8) | (×16) | | (×8) | (×16) |
|----------|--------|--------|----------|--------|--------|
| 16K byte | FFFFFH | 7FFFFH | 64K byte | FFFFFH | 7FFFFH |
| 8K byte | FC000H | 7E000H | 64K byte | F0000H | 78000H |
| 8K byte | FA000H | 7D000H | 64K byte | E0000H | 70000H |
| 32K byte | F8000H | 7C000H | 64K byte | D0000H | 68000H |
| 64K byte | F0000H | 78000H | 64K byte | C0000H | 60000H |
| 64K byte | E0000H | 70000H | 64K byte | B0000H | 58000H |
| 64K byte | D0000H | 68000H | 64K byte | A0000H | 50000H |
| 64K byte | C0000H | 60000H | 64K byte | 90000H | 48000H |
| 64K byte | B0000H | 58000H | 64K byte | 80000H | 40000H |
| 64K byte | A0000H | 50000H | 64K byte | 70000H | 38000H |
| 64K byte | 90000H | 48000H | 64K byte | 60000H | 30000H |
| 64K byte | 80000H | 40000H | 64K byte | 50000H | 28000H |
| 64K byte | 70000H | 38000H | 64K byte | 40000H | 20000H |
| 64K byte | 60000H | 30000H | 64K byte | 30000H | 18000H |
| 64K byte | 50000H | 28000H | 64K byte | 20000H | 10000H |
| 64K byte | 40000H | 20000H | 32K byte | 10000H | 08000H |
| 64K byte | 30000H | 18000H | 8K byte | 08000H | 04000H |
| 64K byte | 20000H | 10000H | 8K byte | 06000H | 03000H |
| 64K byte | 10000H | 08000H | 16K byte | 04000H | 02000H |
| 64K byte | 00000H | 00000H | | 00000H | 00000H |

MB84VA2006 Sector Architecture

MB84VA2007 Sector Architecture

MB84VA2006-10/MB84VA2007-10

Table 4 Sector Address Tables (MB84VA2006)

| Sector Address | A ₁₈ | A ₁₇ | A ₁₆ | A ₁₅ | A ₁₄ | A ₁₃ | A ₁₂ | Address Range (×8) | Address Range (×16) |
|----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|--------------------|---------------------|
| SA0 | 0 | 0 | 0 | 0 | X | X | X | 00000H to 0FFFFH | 00000H to 07FFFFH |
| SA1 | 0 | 0 | 0 | 1 | X | X | X | 10000H to 1FFFFH | 08000H to 0FFFFH |
| SA2 | 0 | 0 | 1 | 0 | X | X | X | 20000H to 2FFFFH | 10000H to 17FFFFH |
| SA3 | 0 | 0 | 1 | 1 | X | X | X | 30000H to 3FFFFH | 18000H to 1FFFFH |
| SA4 | 0 | 1 | 0 | 0 | X | X | X | 40000H to 4FFFFH | 20000H to 27FFFFH |
| SA5 | 0 | 1 | 0 | 1 | X | X | X | 50000H to 5FFFFH | 28000H to 2FFFFH |
| SA6 | 0 | 1 | 1 | 0 | X | X | X | 60000H to 6FFFFH | 30000H to 37FFFFH |
| SA7 | 0 | 1 | 1 | 1 | X | X | X | 70000H to 7FFFFH | 38000H to 3FFFFH |
| SA8 | 1 | 0 | 0 | 0 | X | X | X | 80000H to 8FFFFH | 40000H to 47FFFFH |
| SA9 | 1 | 0 | 0 | 1 | X | X | X | 90000H to 9FFFFH | 48000H to 4FFFFH |
| SA10 | 1 | 0 | 1 | 0 | X | X | X | A0000H to AFFFFH | 50000H to 57FFFFH |
| SA11 | 1 | 0 | 1 | 1 | X | X | X | B0000H to BFFFFH | 58000H to 5FFFFH |
| SA12 | 1 | 1 | 0 | 0 | X | X | X | C0000H to CFFFFH | 60000H to 67FFFFH |
| SA13 | 1 | 1 | 0 | 1 | X | X | X | D0000H to DFFFFH | 68000H to 6FFFFH |
| SA14 | 1 | 1 | 1 | 0 | X | X | X | E0000H to EFFFFH | 70000H to 77FFFFH |
| SA15 | 1 | 1 | 1 | 1 | 0 | X | X | F0000H to F7FFFFH | 78000H to 7BFFFFH |
| SA16 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | F8000H to F9FFFFH | 7C000H to 7CFFFFH |
| SA17 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | FA000H to FBFFFFH | 7D000H to 7DFFFFH |
| SA18 | 1 | 1 | 1 | 1 | 1 | 1 | X | FC000H to FFFFFH | 7E000H to 7FFFFH |

MB84VA2006-10/MB84VA2007-10

Table 5 Sector Address Tables (MB84VA2007)

| Sector Address | A ₁₈ | A ₁₇ | A ₁₆ | A ₁₅ | A ₁₄ | A ₁₃ | A ₁₂ | Address Range (×8) | Address Range (×16) |
|----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|--------------------|---------------------|
| SA0 | 0 | 0 | 0 | 0 | 0 | 0 | X | 00000H to 03FFFFH | 00000H to 01FFFFH |
| SA1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 04000H to 05FFFFH | 02000H to 02FFFFH |
| SA2 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 06000H to 07FFFFH | 03000H to 03FFFFH |
| SA3 | 0 | 0 | 0 | 0 | 1 | X | X | 08000H to 0FFFFH | 04000H to 07FFFFH |
| SA4 | 0 | 0 | 0 | 1 | X | X | X | 10000H to 1FFFFH | 08000H to 0FFFFH |
| SA5 | 0 | 0 | 1 | 0 | X | X | X | 20000H to 2FFFFH | 10000H to 17FFFFH |
| SA6 | 0 | 0 | 1 | 1 | X | X | X | 30000H to 3FFFFH | 18000H to 1FFFFH |
| SA7 | 0 | 1 | 0 | 0 | X | X | X | 40000H to 4FFFFH | 20000H to 27FFFFH |
| SA8 | 0 | 1 | 0 | 1 | X | X | X | 50000H to 5FFFFH | 28000H to 2FFFFH |
| SA9 | 0 | 1 | 1 | 0 | X | X | X | 60000H to 6FFFFH | 30000H to 37FFFFH |
| SA10 | 0 | 1 | 1 | 1 | X | X | X | 70000H to 7FFFFH | 38000H to 3FFFFH |
| SA11 | 1 | 0 | 0 | 0 | X | X | X | 80000H to 8FFFFH | 40000H to 47FFFFH |
| SA12 | 1 | 0 | 0 | 1 | X | X | X | 90000H to 9FFFFH | 48000H to 4FFFFH |
| SA13 | 1 | 0 | 1 | 0 | X | X | X | A0000H to AFFFFH | 50000H to 57FFFFH |
| SA14 | 1 | 0 | 1 | 1 | X | X | X | B0000H to BFFFFH | 58000H to 5FFFFH |
| SA15 | 1 | 1 | 0 | 0 | X | X | X | C0000H to CFFFFH | 60000H to 67FFFFH |
| SA16 | 1 | 1 | 0 | 1 | X | X | X | D0000H to DFFFFH | 68000H to 6FFFFH |
| SA17 | 1 | 1 | 1 | 0 | X | X | X | E0000H to EFFFFH | 70000H to 77FFFFH |
| SA18 | 1 | 1 | 1 | 1 | X | X | X | F0000H to FFFFFH | 78000H to 7FFFFH |

MB84VA2006-10/MB84VA2007-10

Table 6.1 Flash Memory Autoselect Codes

| Type | | A ₆ | A ₁ | A ₀ | A ₋₁ ^{*1} | Code (HEX) |
|---------------------|------------|-----------------|-----------------|-----------------|-------------------------------|------------|
| Manufacturer's Code | | V _{IL} | V _{IL} | V _{IL} | V _{IL} | 04H |
| Device Code | MB84VA2006 | V _{IL} | V _{IL} | V _{IH} | V _{IL} | DAH |
| | | | | | X | 22DAH |
| | MB84VA2007 | V _{IL} | V _{IL} | V _{IH} | V _{IL} | 5BH |
| | | | | | X | 225BH |

*1: A₋₁ is for Byte mode.

Table 6.2 Expanded Autoselect Code Table

| Type | | Code | DQ ₁₅ | DQ ₁₄ | DQ ₁₃ | DQ ₁₂ | DQ ₁₁ | DQ ₁₀ | DQ ₉ | DQ ₈ | DQ ₇ | DQ ₆ | DQ ₅ | DQ ₄ | DQ ₃ | DQ ₂ | DQ ₁ | DQ ₀ |
|---------------------|-----------------------|-------|------------------|------------------|------------------|------------------|------------------|------------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| Manufacturer's Code | | 04H | A-1/0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| Device Code | MB84VA2006 (B) (W) | DAH | A-1 | HI-Z | HI-Z | HI-Z | HI-Z | HI-Z | HI-Z | HI-Z | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 |
| | | 22DAH | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 |
| | MB84VA2007 (B) (W) | 5BH | A-1 | HI-Z | HI-Z | HI-Z | HI-Z | HI-Z | HI-Z | HI-Z | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 |
| | | 225BH | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 |

(B): Byte mode

(W): Word mode

MB84VA2006-10/MB84VA2007-10

Table 7 Flash Memory Command Definitions

| Command Sequence | | Bus Write Cycles Req'd | First Bus Write Cycle | | Second Bus Write Cycle | | Third Bus Write Cycle | | Fourth Bus Read/Write Cycle | | Fifth Bus Write Cycle | | Sixth Bus Write Cycle | |
|-------------------------|--------------|---|-----------------------|------|------------------------|------|-----------------------|------|-----------------------------|------|-----------------------|------|-----------------------|------|
| | | | Addr. | Data | Addr. | Data | Addr. | Data | Addr. | Data | Addr. | Data | Addr. | Data |
| Read/Reset | word Byte | 1 | XXXH | F0H | — | — | — | — | — | — | — | — | — | — |
| Read/Reset | word Byte | 3 | 555H AAAH | AAH | 2AAH 555H | 55H | 555H AAAH | F0H | RA | RD | — | — | — | — |
| Autoselect | word Byte | 3 | 555H AAAH | AAH | 2AAH 555H | 55H | 555H AAAH | 90H | — | — | — | — | — | — |
| Program | word Byte | 4 | 555H AAAH | AAH | 2AAH 555H | 55H | 555H AAAH | A0H | PA | PD | — | — | — | — |
| Chip Erase | word Byte | 6 | 555H AAAH | AAH | 2AAH 555H | 55H | 555H AAAH | 80H | 555H AAAH | AAH | 2AAH 555H | 55H | 555H AAAH | 10H |
| Sector Erase | word Byte | 6 | 555H AAAH | AAH | 2AAH 555H | 55H | 555H AAAH | 80H | 555H AAAH | AAH | 2AAH 555H | 55H | SA | 30H |
| Sector Erase Suspend | | Erase can be suspended during sector erase with Addr ("H" or "L"). Data (B0H) | | | | | | | | | | | | |
| Sector Erase Resume | | Erase can be resumed after suspend with Addr ("H" or "L"). Data (30H) | | | | | | | | | | | | |
| Set to Fast Mode | word Byte | 3 | 555H AAAH | AAH | 2AAH 555H | 55H | 555H AAAH | 20H | — | — | — | — | — | — |
| Fast Program (Note) | word Byte | 2 | XXXH XXXH | A0H | PA | PD | — | — | — | — | — | — | — | — |
| Reset from Fast Mode | word Byte | 2 | XXXH XXXH | 90H | XXXH XXXH | F0H | — | — | — | — | — | — | — | — |
| Extended Sector Protect | word Byte | 4 | XXXH | 60H | SPA | 60H | SPA | 40H | SPA | SD | — | — | — | — |

Address bits A₁₁ to A₂₀ = X = "H" or "L" for all address commands except for Program Address (PA) and Sector Address (SA).

Bus operations are defined in Table 2.

Both Read/Reset commands are functionally equivalent, resetting the device to the read mode.

RA =Address of the memory location to be read.

PA =Address of the memory location to be programmed. Addresses are latched on the falling edge of the write pulse.

SA =Address of the sector to be erased. The combination of A₂₀, A₁₉, A₁₈, A₁₇, A₁₆, A₁₅, A₁₄, and A₁₃ will uniquely select any sector.

RD =Data read from location RA during read operation.

PD =Data to be programmed at location PA.

SPA =Sector address to be protected. Set sector address (SA) and (A₆, A₁, A₀) = (0, 1, 0).

SD =Sector protection verify data. Output 01H at protected sector addresses and output 00H at unprotected sector addresses.

Note:This command is valid while Fast Mode.

MB84VA2006-10/MB84VA2007-10

■ ABSOLUTE MAXIMUM RATINGS

| | |
|--|-----------------------------|
| Storage Temperature | -55°C to +125°C |
| Ambient Temperature with Power Applied | -25°C to +85°C |
| Voltage with Respect to Ground All pins (Note) | -0.3 V to $V_{ccf} + 0.5$ V |
| | -0.3 V to $V_{ccs} + 0.5$ V |
| V_{ccf}/V_{ccs} Supply (Note) | -0.3 V to +4.6 V |

Note: Minimum DC voltage on input or I/O pins are -0.5 V. During voltage transitions, inputs may negativeovershoot V_{ss} to -2.0 V for periods of up to 20 ns. Maximum DC voltage on output and I/O pins are $V_{ccf} + 0.5$ V or $V_{ccs} + 0.5$ V. During voltage transitions, outputs may positive overshoot to $V_{cc} + 2.0$ V for periods of up to 20 ns.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING RANGES

Commercial Devices

Ambient Temperature (T_A)

| | |
|-------|----------------|
| | -20°C to +85°C |
|-------|----------------|

V_{ccf}/V_{ccs} Supply Voltages.....+2.7 V to +3.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

WARNING: Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representative beforehand.

MB84VA2006-10/MB84VA2007-10

■ DC CHARACTERISTICS

| Parameter Symbol | Parameter Description | Test Conditions | | Min. | Typ. | Max. | Unit | |
|---------------------|--|---|---------------------------------|-------------------------------|------|-----------------------|------|----|
| I _{LI} | Input Leakage Current | — | | -1.0 | — | +1.0 | μA | |
| I _{LO} | Output Leakage Current | — | | -1.0 | — | +1.0 | μA | |
| I _{CC1f} | Flash V _{CC} Active Current (Read) | V _{CCf} = V _{CC} Max., $\overline{CE}f = V_{IL}$ OE = V _{IH} | Byte | t _{CYCLE} = 10 MHz | — | — | 22 | mA |
| | | | Word | | — | — | 25 | |
| | | | Byte | t _{CYCLE} = 5 MHz | — | — | 12 | |
| | | | Word | | — | — | 15 | |
| I _{CC2f} | Flash V _{CC} Active Current (Program/Erase) | V _{CCf} = V _{CC} Max., $\overline{CE}f = V_{IL}$, OE = V _{IH} | | — | — | 35 | mA | |
| I _{CC1S} | SRAM V _{CC} Active Current | V _{CCS} = V _{CC} Max., CE1s = V _{IL} , CE2s = V _{IH} | t _{CYCLE} = 10 MHz | — | — | 40 | mA | |
| | | | t _{CYCLE} = 1 MHz | — | — | 12 | mA | |
| I _{CC2S} | SRAM V _{CC} Active Current | CE1s = 0.2 V, CE2s = V _{CCS} - 0.2 V, WE = V _{CCS} - 0.2 V | t _{CYCLE} = 10 MHz | — | — | 35 | mA | |
| | | | t _{CYCLE} = 1 MHz | — | — | 8 | mA | |
| I _{SB1f} | Flash V _{CC} Standby Current | V _{CCf} = V _{CC} Max., $\overline{CE}f = V_{CCf} \pm 0.3$ V RESET = V _{CCf} ± 0.3 V | | — | — | 5 | μA | |
| I _{SB2f} | Flash V _{CC} Standby Current (RESET) | V _{CCf} = V _{CC} Max., RESET = V _{SS} ± 0.3 V | | — | — | 5 | μA | |
| I _{SB1S} | SRAM V _{CC} Standby Current | CE1s = V _{IH} or CE2s = V _{IL} | | — | — | 2 | mA | |
| I _{SB2S**} | SRAM V _{CC} Standby Current | CE1s = V _{CC} - 0.2 V or CE2s = 0.2 V | V _{CCS} = 3.0 V ±10% | T _A = 25°C | — | 1 | 2 | μA |
| | | | | T _A = -20 to +85°C | — | — | 35 | μA |
| | | | V _{CCS} = 3.3 V ±0.3 V | T _A = 25°C | — | 2 | 3 | μA |
| | | | | T _A = -20 to +85°C | — | — | 40 | μA |
| | | | V _{CCS} = 3.0 V | T _A = 25°C | — | — | 1 | μA |
| | | | | T _A = -20 to +85°C | — | — | 30 | μA |
| V _{IL} | Input Low Level | — | | -0.3 | — | 0.6 | V | |
| V _{IH} | Input High Level | — | | 2.2 | — | V _{CC} +0.3* | V | |
| V _{OL} | Output Low Voltage Level | I _{OL} = 2.1 mA, V _{CCf} = V _{CCS} = V _{CC} Min. | | — | — | 0.4 | V | |
| V _{OH} | Output High Voltage Level | I _{OH} = -500 μA, V _{CCf} = V _{CCS} = V _{CC} Min. | | V _{CC} -0.5 | — | — | V | |
| V _{LKO} | Flash Low V _{CC} Lock-Out Voltage | — | | 2.3 | — | 2.5 | V | |

* : V_{CC} indicate lower of V_{CCf} or V_{CCS}

** : During standby mode with CE1s = V_{CCS} - 0.2 V, CE2s should be CE2s < 0.2V or CE2s > V_{CCS} - 0.2V

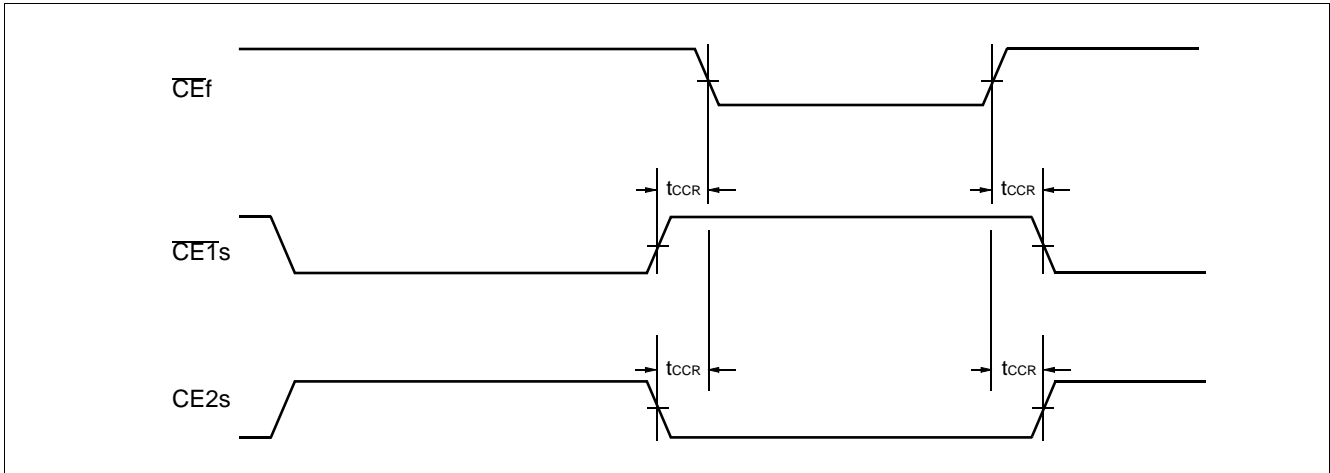
MB84VA2006-10/MB84VA2007-10

■ AC CHARACTERISTICS

• CE Timing

| Parameter Symbols | | Description | Test Setup | | -10 | Unit |
|-------------------|------------------|-----------------|------------|------|-----|------|
| JEDEC | Standard | | | | | |
| — | t _{CCR} | CE Recover Time | — | Min. | 0 | ns |

• Timing Diagram for alternating SRAM to Flash



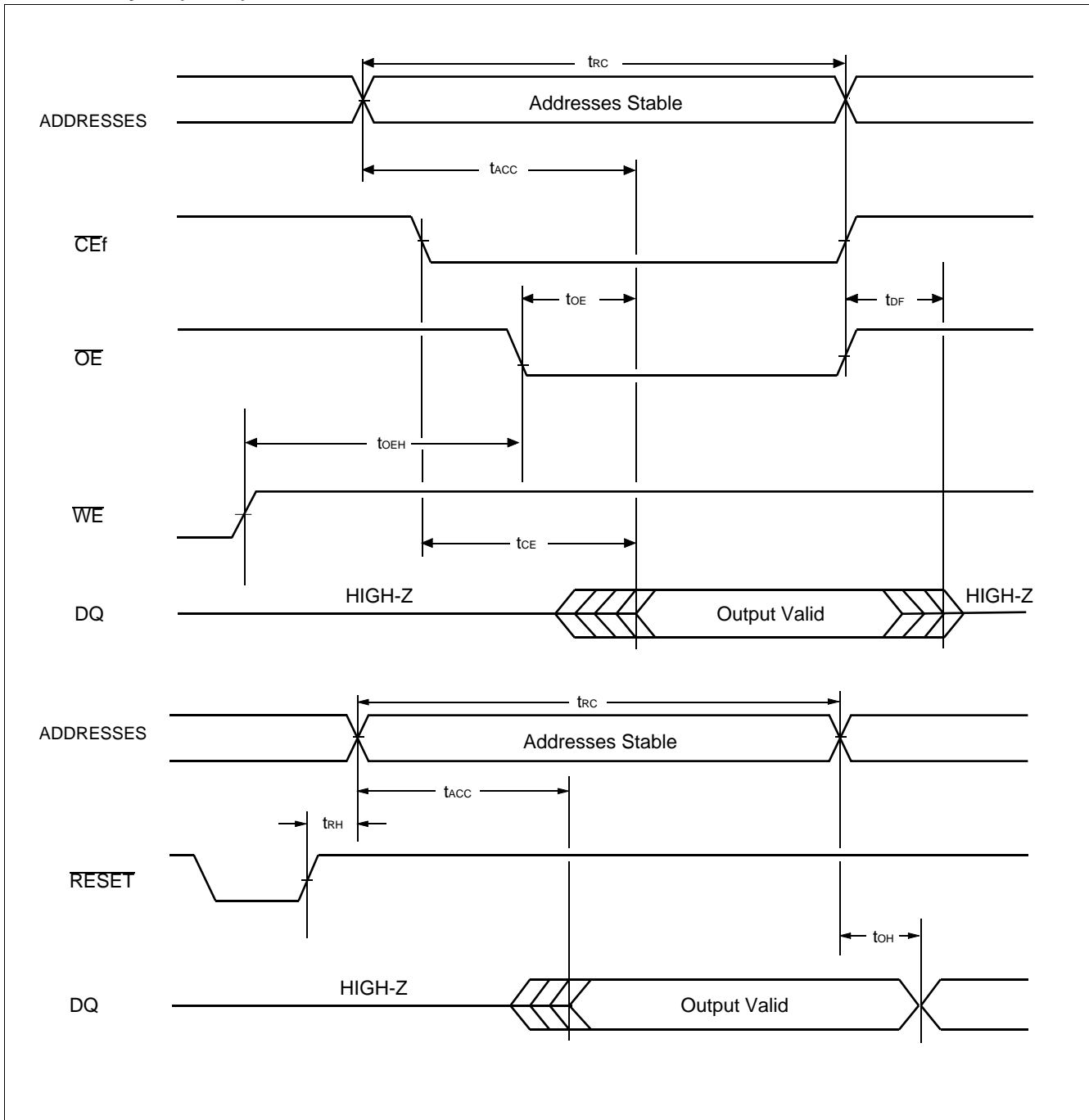
• Read Only Operations Characteristics (Flash)

| Parameter Symbols | | Description | Test Setup | -10 (Note) | | Unit |
|-------------------|--|--|--|------------|------|------|
| JEDEC | Standard | | | Min. | Max. | |
| t _{AVAV} | t _{RC} | Read Cycle Time | — | 100 | — | ns |
| t _{AVQV} | t _{ACC} | Address to Output Delay | $\overline{CE}_f = V_{IL}$ $\overline{OE} = V_{IL}$ | — | 100 | ns |
| t _{ELQV} | t _{CEf} | Chip Enable to Output Delay | $\overline{OE} = V_{IL}$ | — | 100 | ns |
| t _{GLQV} | t _{OE} | Output Enable to Output Delay | — | — | 40 | ns |
| t _{EHQZ} | t _{DF} | Chip Enable to Output High-Z | — | — | 30 | ns |
| t _{GHQZ} | t _{DF} | Output Enable to Output High-Z | — | — | 30 | ns |
| t _{AXQX} | t _{OH} | Output Hold Time From Addresses, \overline{CE}_f or \overline{OE} , Whichever Occurs First | — | 0 | — | ns |
| — | t _{READY} | RESET Pin Low to Read Mode | — | — | 20 | μs |
| — | t _{ELFL} t _{ELFH} | CE or BYTE Switching Low or High | — | — | 5 | ns |

Note: Test Conditions—Output Load: 1 TTL gate and 30 pF
 Input rise and fall times: 5 ns
 Input pulse levels: 0.0 V to 3.0 V
 Timing measurement reference level
 Input: 1.5 V
 Output: 1.5 V

MB84VA2006-10/MB84VA2007-10

• Read Cycle (Flash)



MB84VA2006-10/MB84VA2007-10

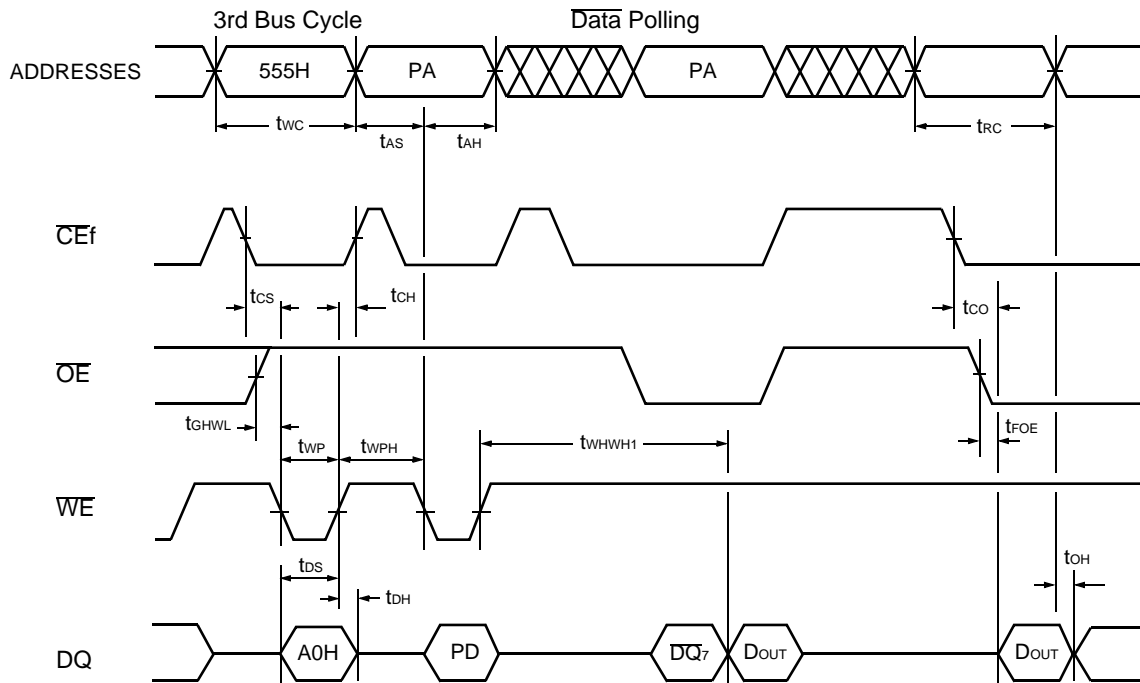
• Erase/Program Operations (Flash)

| Parameter Symbols | | Description | -10 | | | Unit |
|--------------------|--------------------|--|------|------|------|------|
| JEDEC | Standard | | Min. | Typ. | Max. | |
| t _{AVAV} | t _{WC} | Write Cycle Time | 100 | — | — | ns |
| t _{AVWL} | t _{AS} | Address Setup Time (\overline{WE} to Addr.) | 0 | — | — | ns |
| t _{AVEL} | t _{AS} | Address Setup Time (\overline{CEf} to Addr.) | 0 | — | — | ns |
| t _{WLAX} | t _{AH} | Address Hold Time (\overline{WE} to Addr.) | 50 | — | — | ns |
| t _{ELAX} | t _{AH} | Address Hold Time (\overline{CEf} to Addr.) | 50 | — | — | ns |
| t _{DVWH} | t _{DS} | Data Setup Time | 50 | — | — | ns |
| t _{WHDX} | t _{DH} | Data Hold Time | 0 | — | — | ns |
| — | t _{OES} | Output Enable Setup Time | 0 | — | — | ns |
| — | t _{OEH} | Output Enable Hold Time | 0 | — | — | ns |
| | | Toggle and Data Polling | 10 | — | — | ns |
| t _{GHEL} | t _{GHEL} | Read Recover Time Before Write (\overline{OE} to \overline{CEf}) | 0 | — | — | ns |
| t _{GHWL} | t _{GHWL} | Read Recover Time Before Write (\overline{OE} to \overline{WE}) | 0 | — | — | ns |
| t _{WLEL} | t _{WS} | \overline{WE} Setup Time (\overline{CEf} to \overline{WE}) | 0 | — | — | ns |
| t _{ELWL} | t _{CS} | \overline{CEf} Setup Time (\overline{WE} to \overline{CEf}) | 0 | — | — | ns |
| t _{EHWH} | t _{WH} | \overline{WE} Hold Time (\overline{CEf} to \overline{WE}) | 0 | — | — | ns |
| t _{WHEH} | t _{CH} | \overline{CEf} Hold Time (\overline{WE} to \overline{CEf}) | 0 | — | — | ns |
| t _{WLWH} | t _{WP} | Write Pulse Width | 50 | — | — | ns |
| t _{ELEH} | t _{CP} | \overline{CEf} Pulse Width | 50 | — | — | ns |
| t _{WHWL} | t _{WPH} | Write Pulse Width High | 30 | — | — | ns |
| t _{EHEL} | t _{CPH} | \overline{CEf} Pulse Width High | 30 | — | — | ns |
| t _{WHWH1} | t _{WHWH1} | Byte Programming Operation | — | 8 | — | μs |
| t _{WHWH2} | t _{WHWH2} | Sector Erase Operation (Note 1) | — | 1 | — | sec |
| | | | — | — | 15 | sec |
| — | t _{VCS} | V _{ccf} Setup Time | 50 | — | — | μs |
| — | t _{VLHT} | Voltage Transition Time (Note 2) | 4 | — | — | μs |
| — | t _{VIDR} | Rise Time to V _{ID} (Note 2) | 500 | — | — | ns |
| — | t _{RB} | Recover Time from RY/BY | 0 | — | — | ns |
| — | t _{RP} | RESET Pulse Width | 500 | — | — | ns |
| — | t _{RH} | RESET Hold Time Before Read | 200 | — | — | ns |
| — | t _{EOE} | Delay Time from Embedded Output Enable | — | — | 100 | ns |
| — | t _{BUSY} | Program/Erase Valid to RY/BY Delay | — | — | 90 | ns |
| — | t _{FLQZ} | BYTE Switching Low to Output High-Z | — | — | 30 | ns |
| — | t _{FLQV} | BYTE Switching High to Output Active | 30 | — | — | ns |

Note : 1. This does not include the preprogramming time.

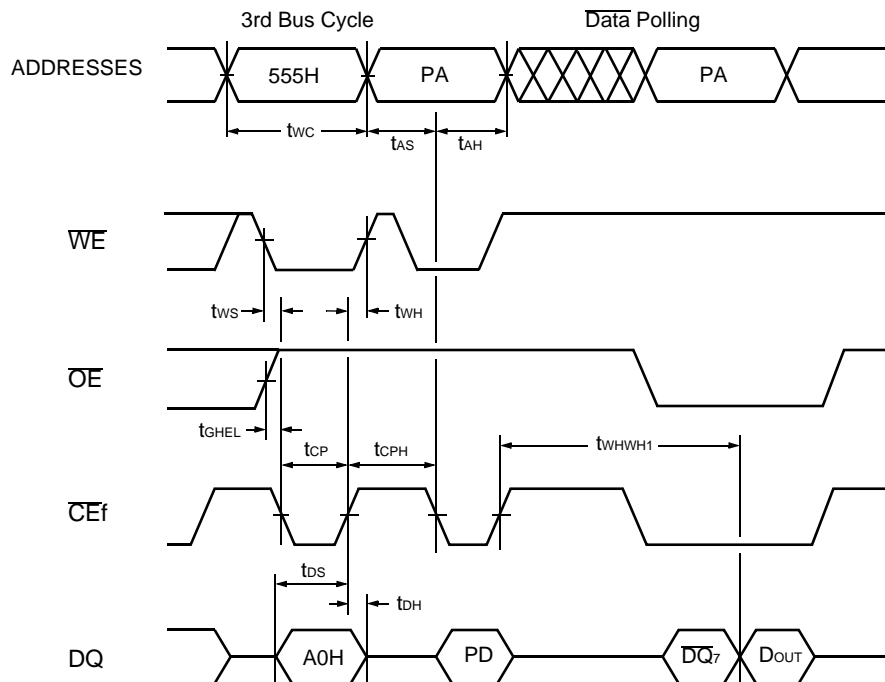
2. This timing is for Sector Protection Operation.

• Write Cycle (WE control) (Flash)



- Notes:**
1. PA is address of the memory location to be programmed.
 2. PD is data to be programmed at byte address.
 3. \overline{DQ}_7 is the output of the complement of the data written to the device.
 4. DOUT is the output of the data written to the device.
 5. Figure indicates last two bus cycles out of four cycle sequence
 6. These waveforms are for the x16 mode. The addresses differ from x8 mode.

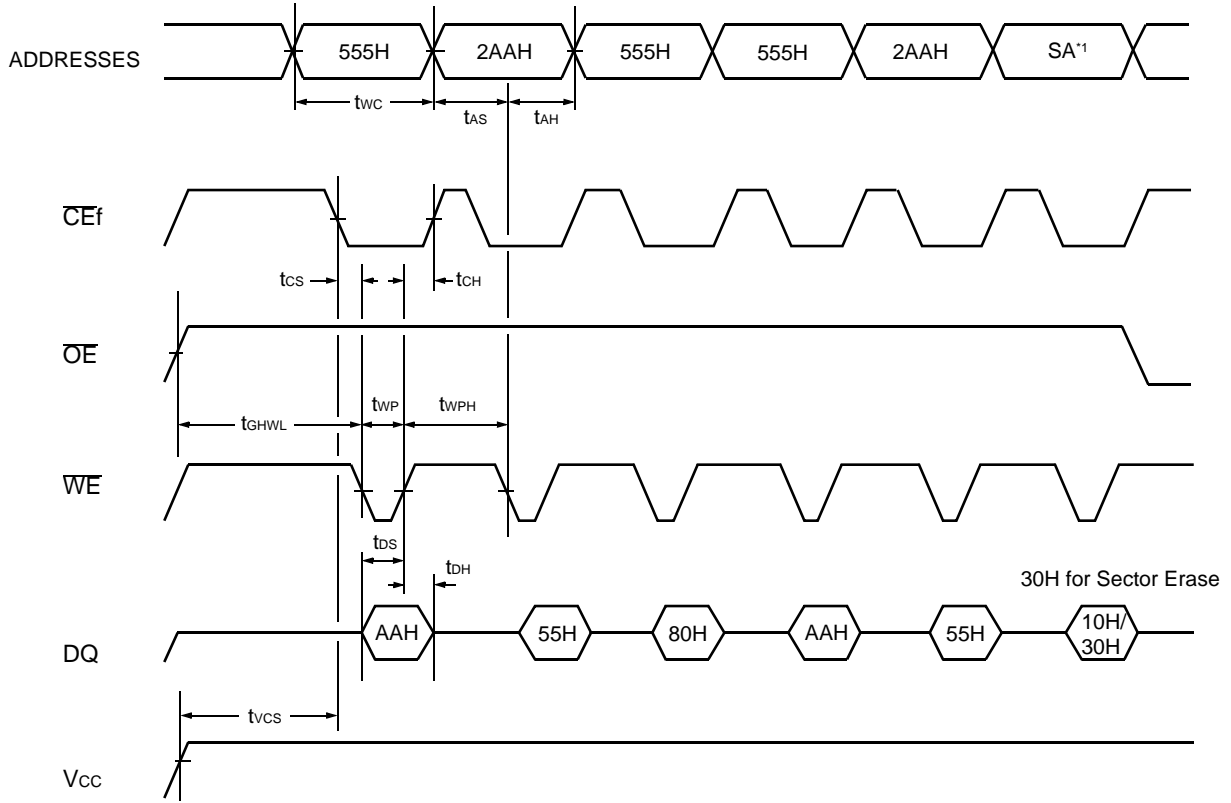
• Write Cycle (\overline{CEf} control) (Flash)



- Notes:**
1. PA is address of the memory location to be programmed.
 2. PD is data to be programmed at byte address.
 3. \overline{DQ}_7 is the output of the complement of the data written to the device.
 4. D_{OUT} is the output of the data written to the device.
 5. Figure indicates last two bus cycles out of four bus cycle sequence
 6. These waveforms are for the x16 mode. The addresses differ from x8 mode.

MB84VA2006-10/MB84VA2007-10

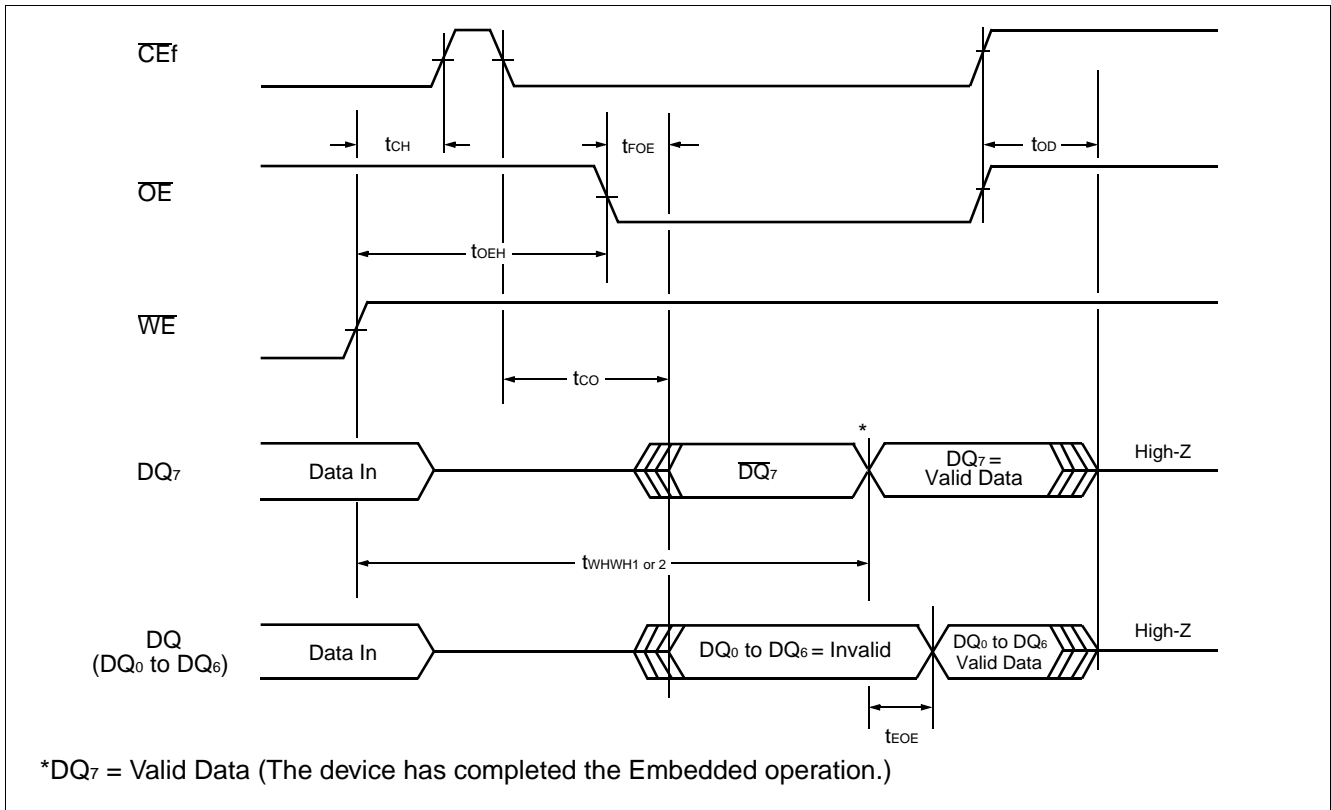
• AC Waveforms Chip/Sector Erase Operations (Flash)



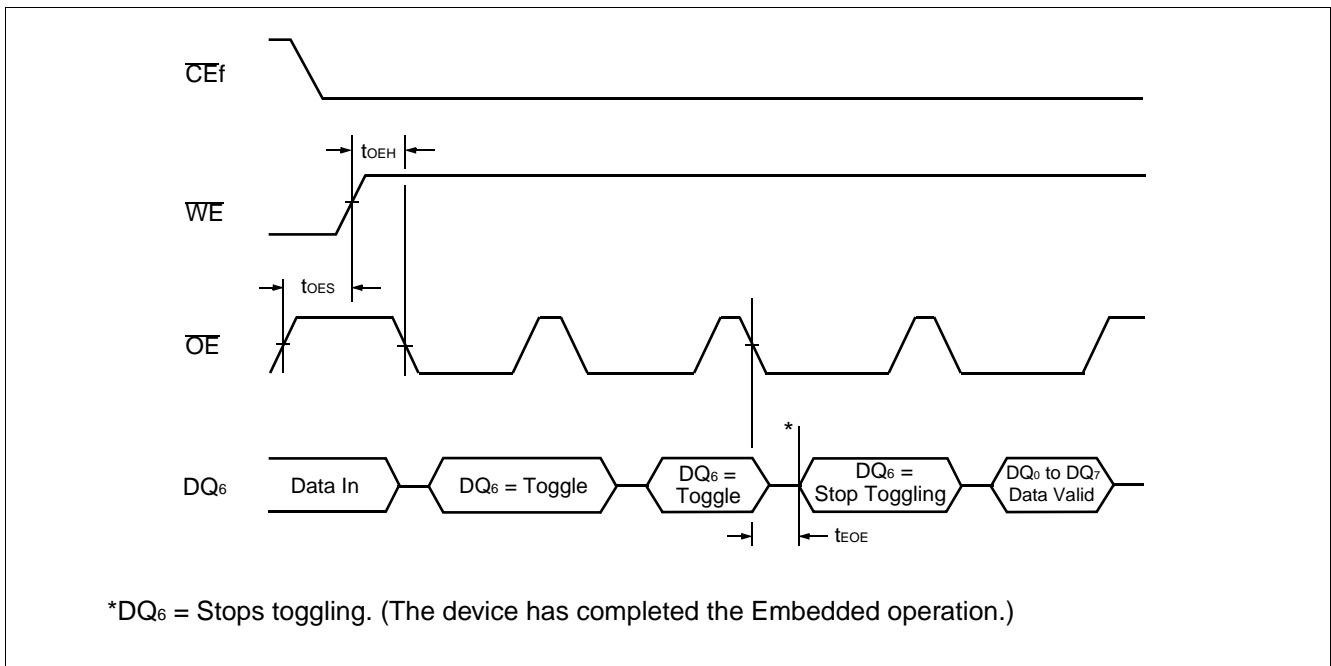
- Notes:**
1. SA is the sector address for Sector Erase. Addresses = 555H for Chip Erase.
 2. These waveforms are for the x16 mode. The addresses differ from x8 mode.

MB84VA2006-10/MB84VA2007-10

• AC Waveforms for Data Polling during Embedded Algorithm Operations (Flash)

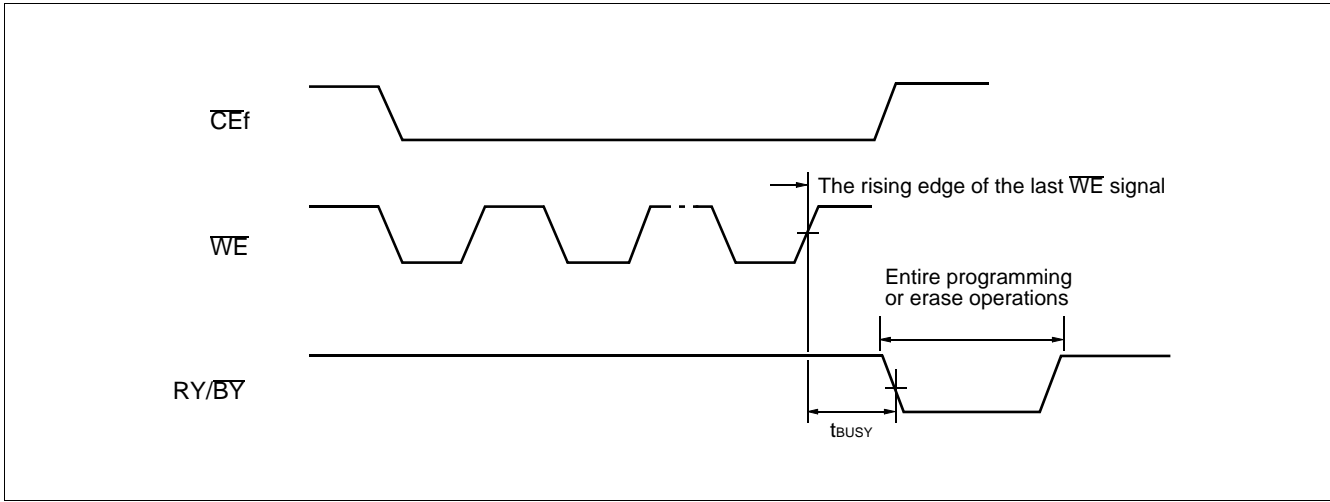


• AC Waveforms for Taggle Bit during Embedded Algorithm Operations (Flash)

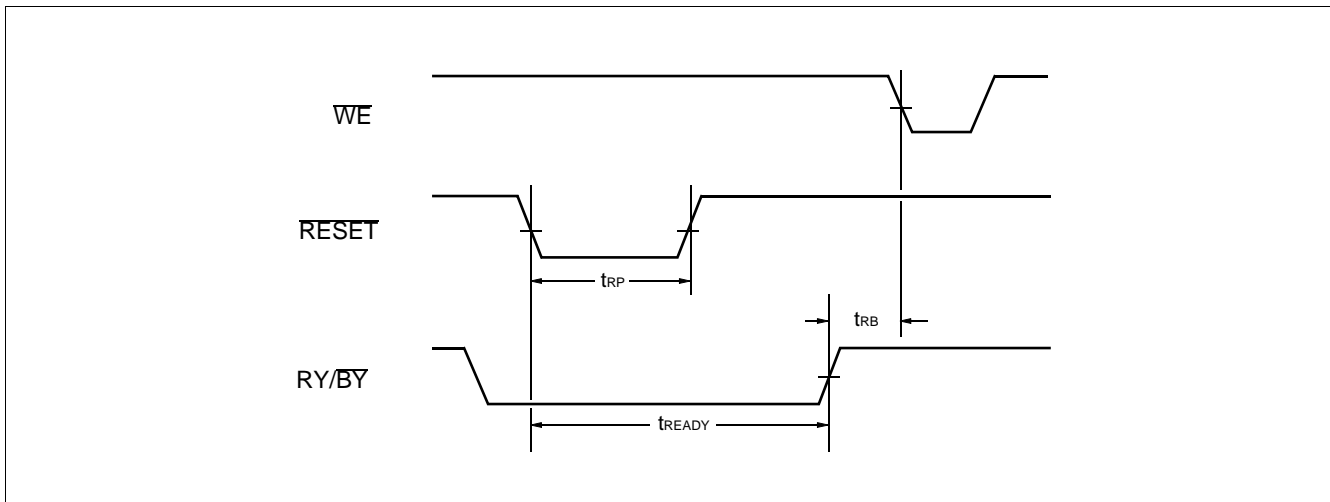


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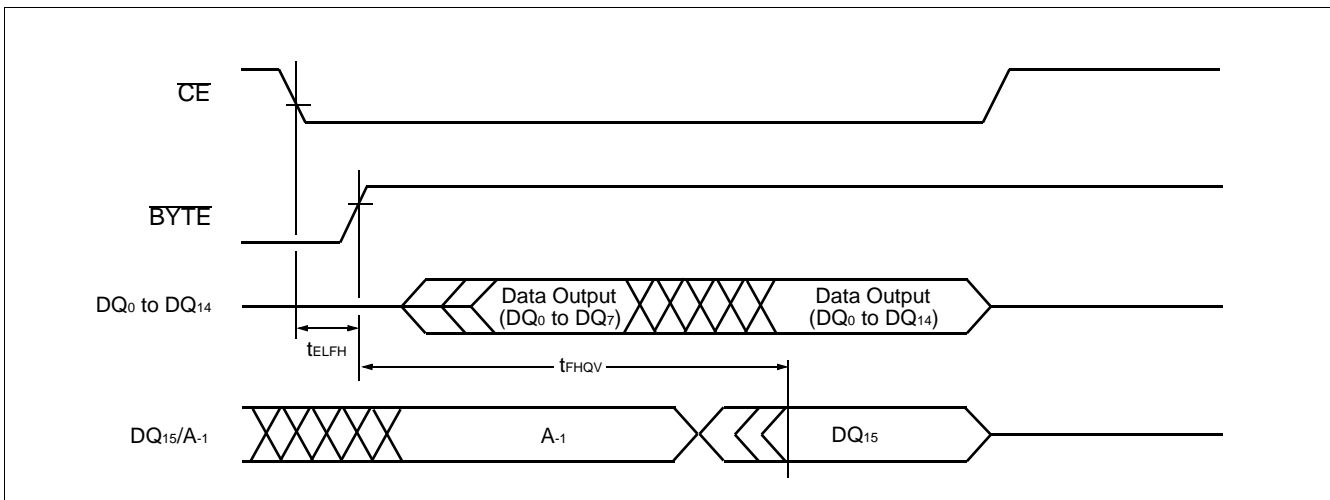
• RY/BY Timing Diagram during Write/Erase Operations (Flash)



• RESET, RY/BY Timing Diagram (Flash)

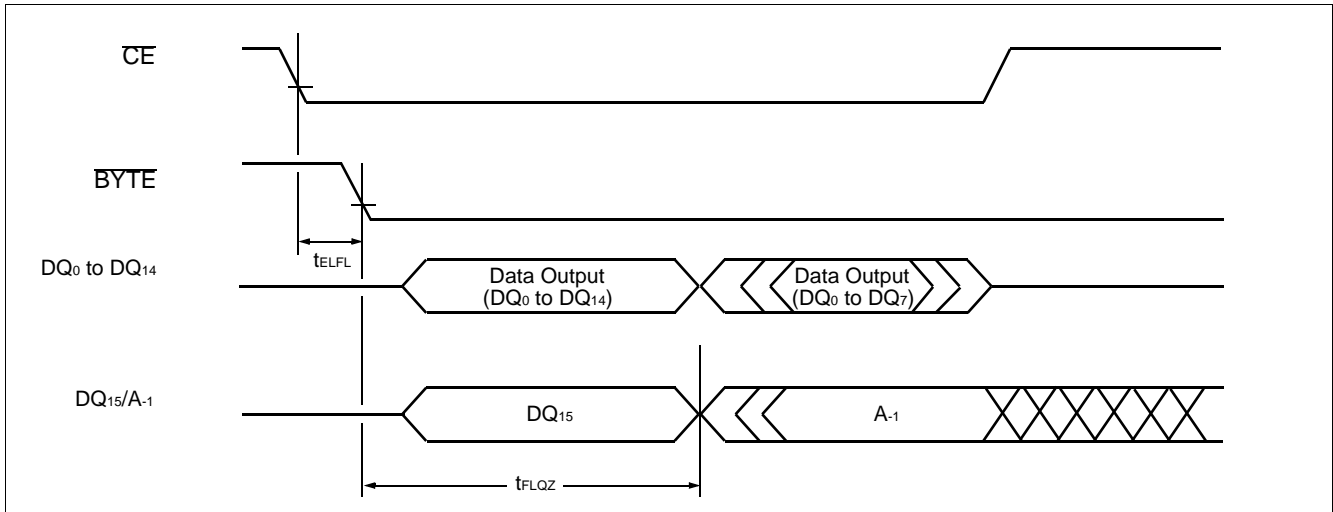


• Timing Diagram for Word Mode Configuration (Flash)

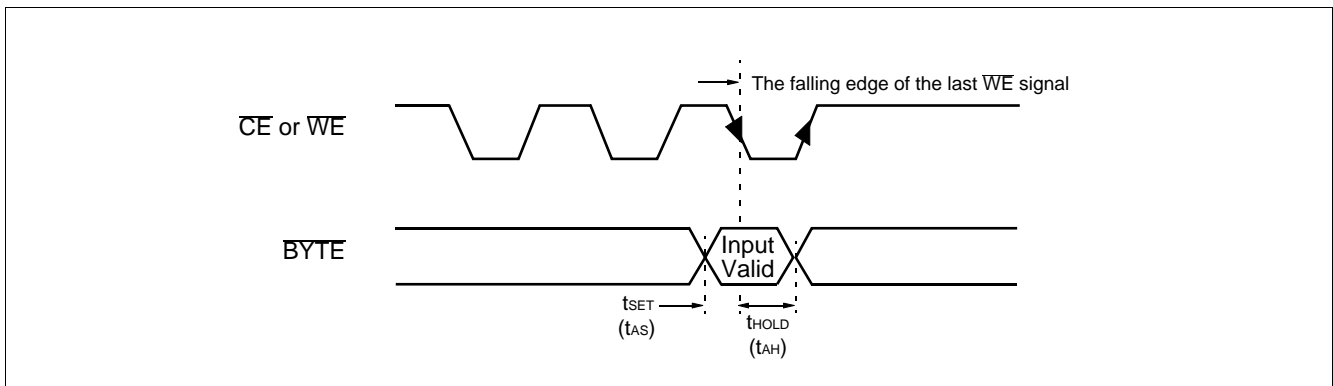


MB84VA2006-10/MB84VA2007-10

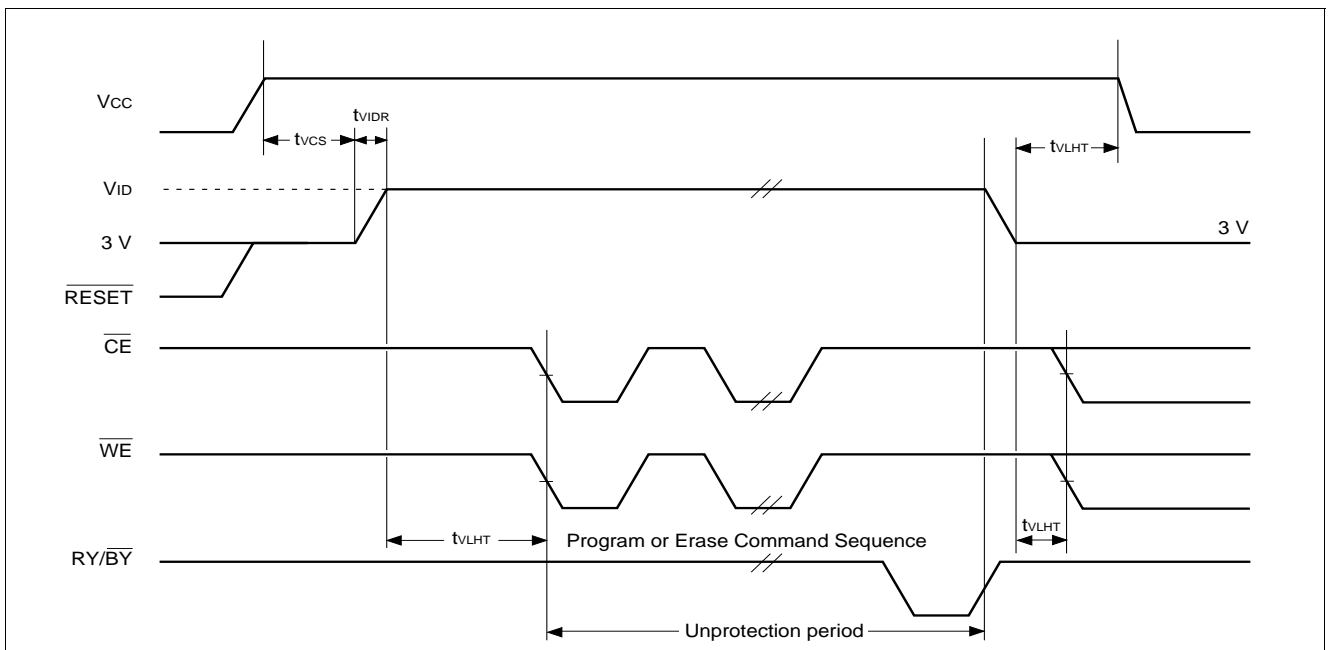
• Timing Diagram for Byte Mode Configuration (Flash)



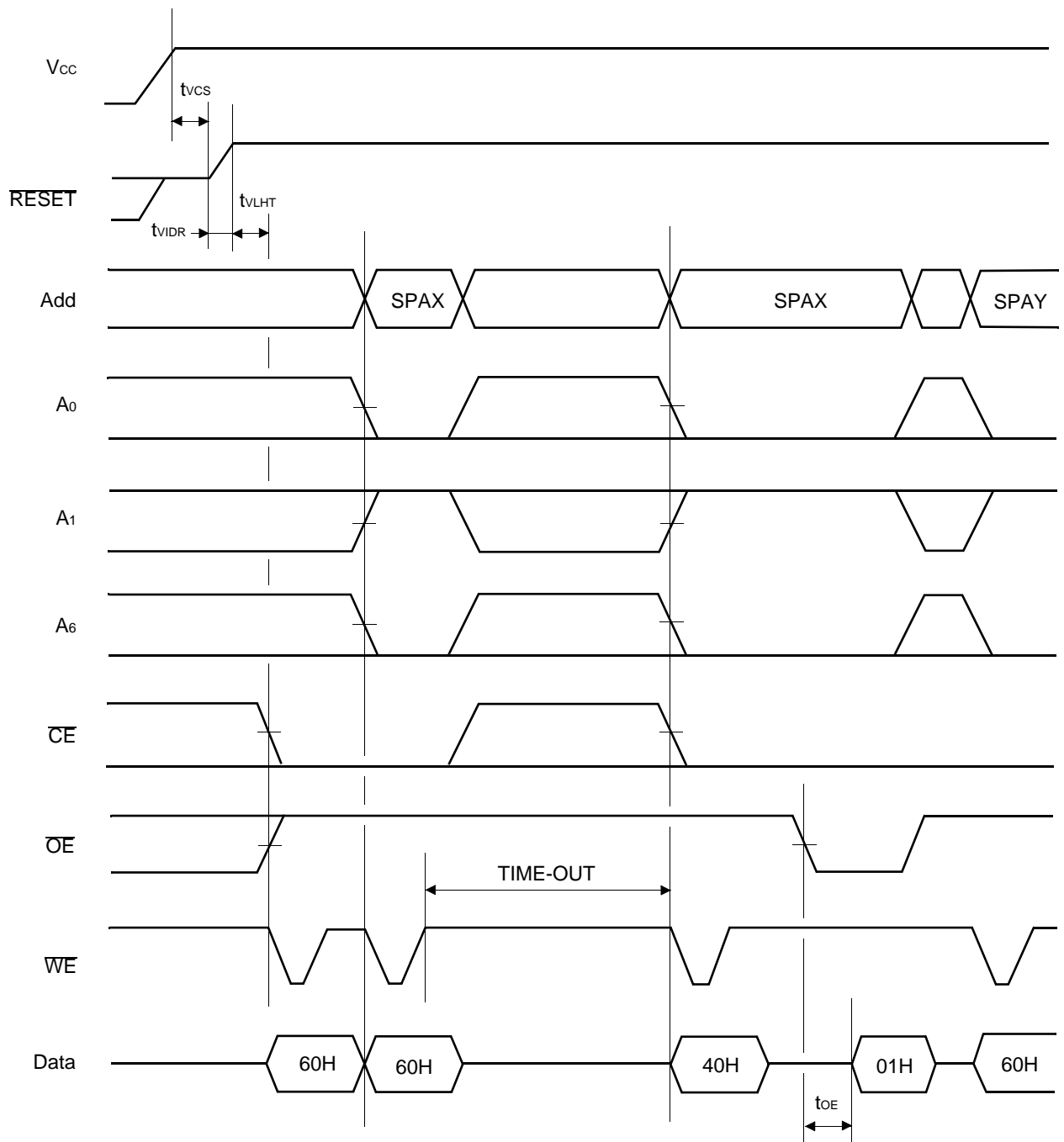
• BYTE Timing Diagram for Write Operations (Flash)



• Temporary Sector Unprotection (Flash)



• Extended Sector Protection (Flash)



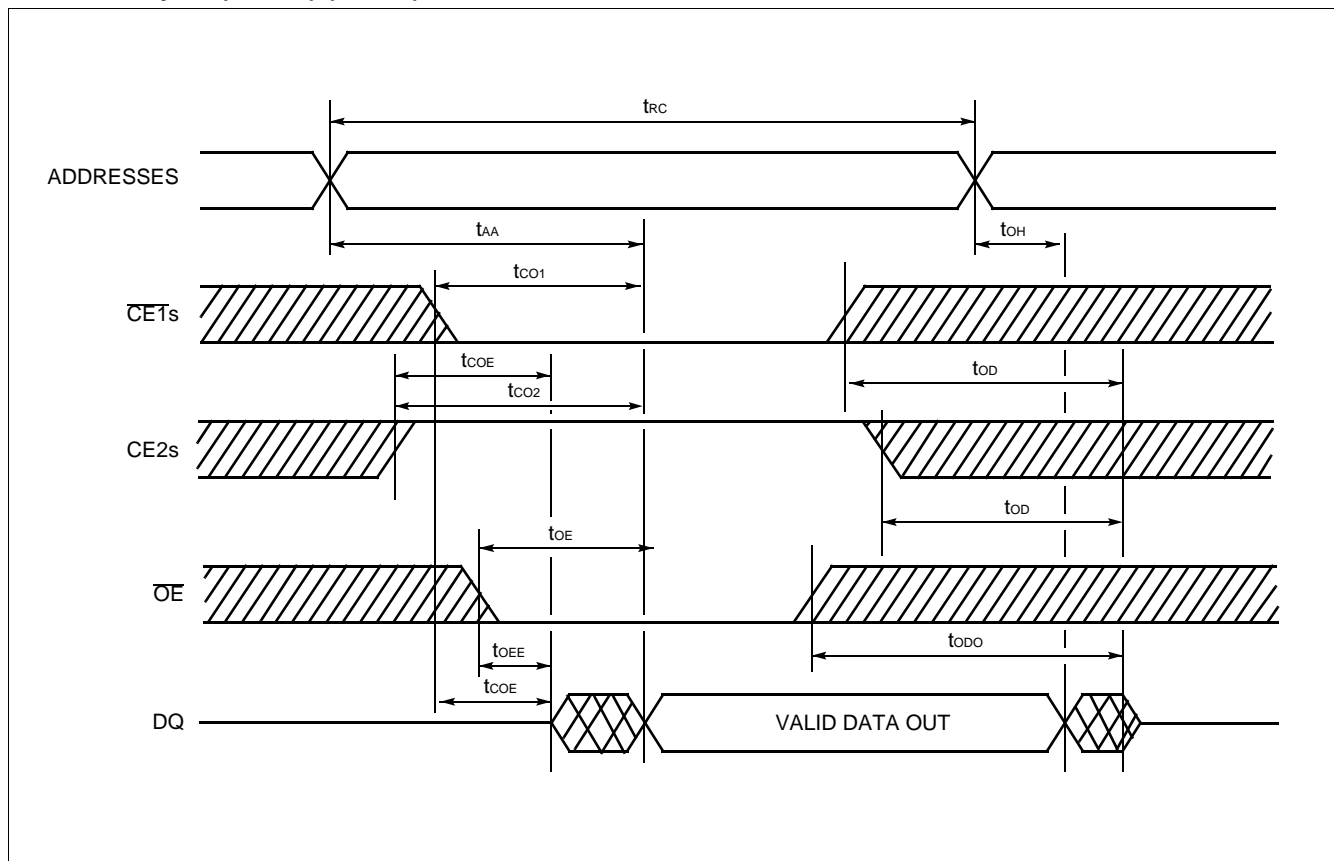
SPAX : Sector Address to be protected
 SPAY : Next Sector Address to be protected
 TIME-OUT : Time-Out window = 150 μ s (min)

MB84VA2006-10/MB84VA2007-10

• Read Cycle (SRAM)

| Parameter Symbol | Parameter Description | Min. | Max. | Unit |
|------------------|---|------|------|------|
| t_{RC} | Read Cycle Time | 100 | — | ns |
| t_{AA} | Address Access Time | — | 100 | ns |
| t_{CO1} | Chip Enable ($\overline{CE1s}$) Access Time | — | 100 | ns |
| t_{CO2} | Chip Enable ($CE2s$) Access Time | — | 100 | ns |
| t_{OE} | Output Enable Access Time | — | 50 | ns |
| t_{COE} | Chip Enable ($\overline{CE1s}$ Low and $CE2s$ High) to Output Active | 5 | — | ns |
| t_{OEE} | Output Enable Low to Output Active | 0 | — | ns |
| t_{OD} | Chip Enable ($\overline{CE1s}$ High or $CE2s$ Low) to Output High-Z | — | 40 | ns |
| t_{ODO} | Output Enable High to Output High-Z | — | 40 | ns |
| t_{OH} | Output Data Hold Time | 10 | — | ns |

• Read Cycle (Note 1) (SRAM)

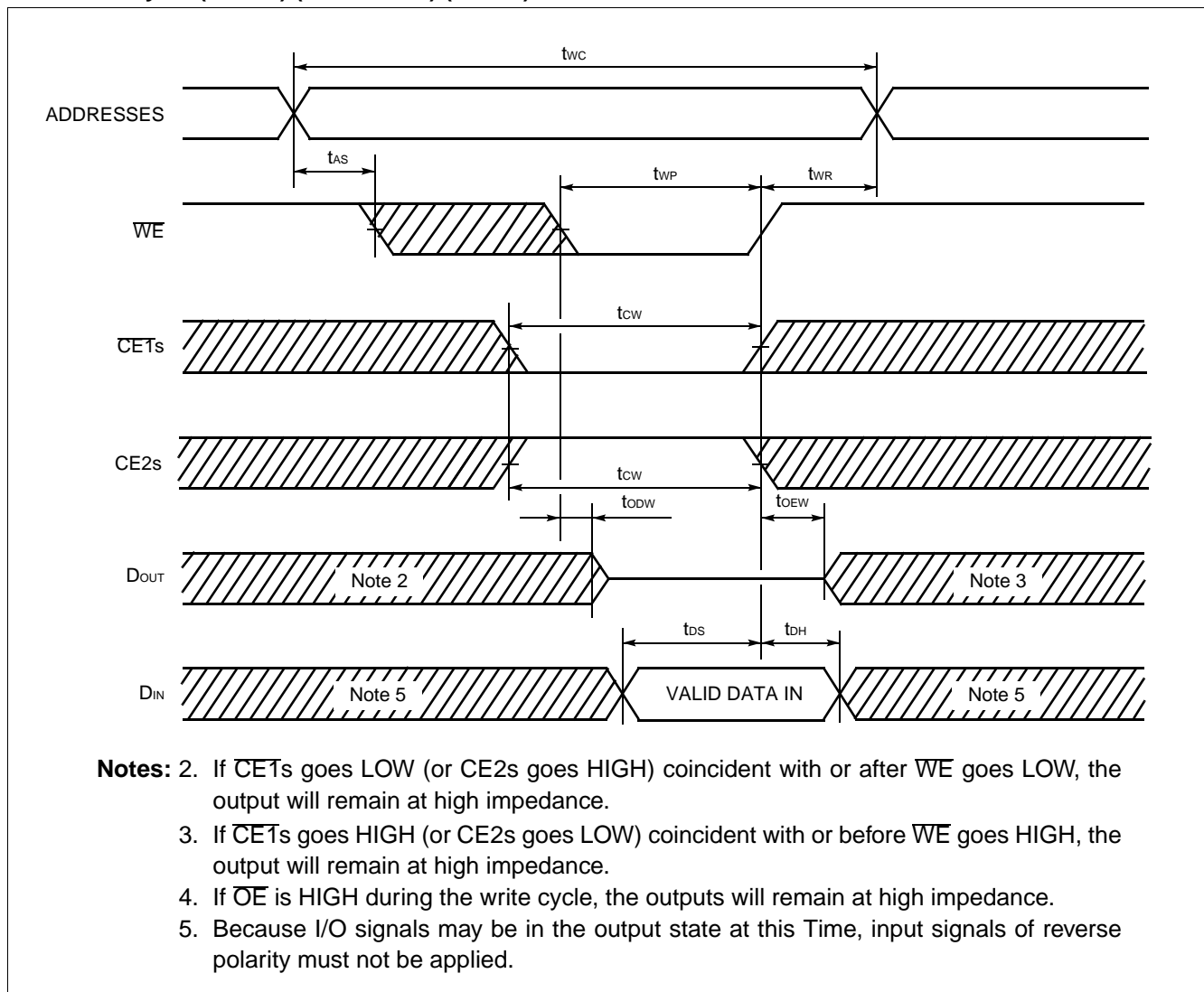


Note: 1. \overline{WE} remains HIGH for the read cycle.

• Write Cycle (SRAM)

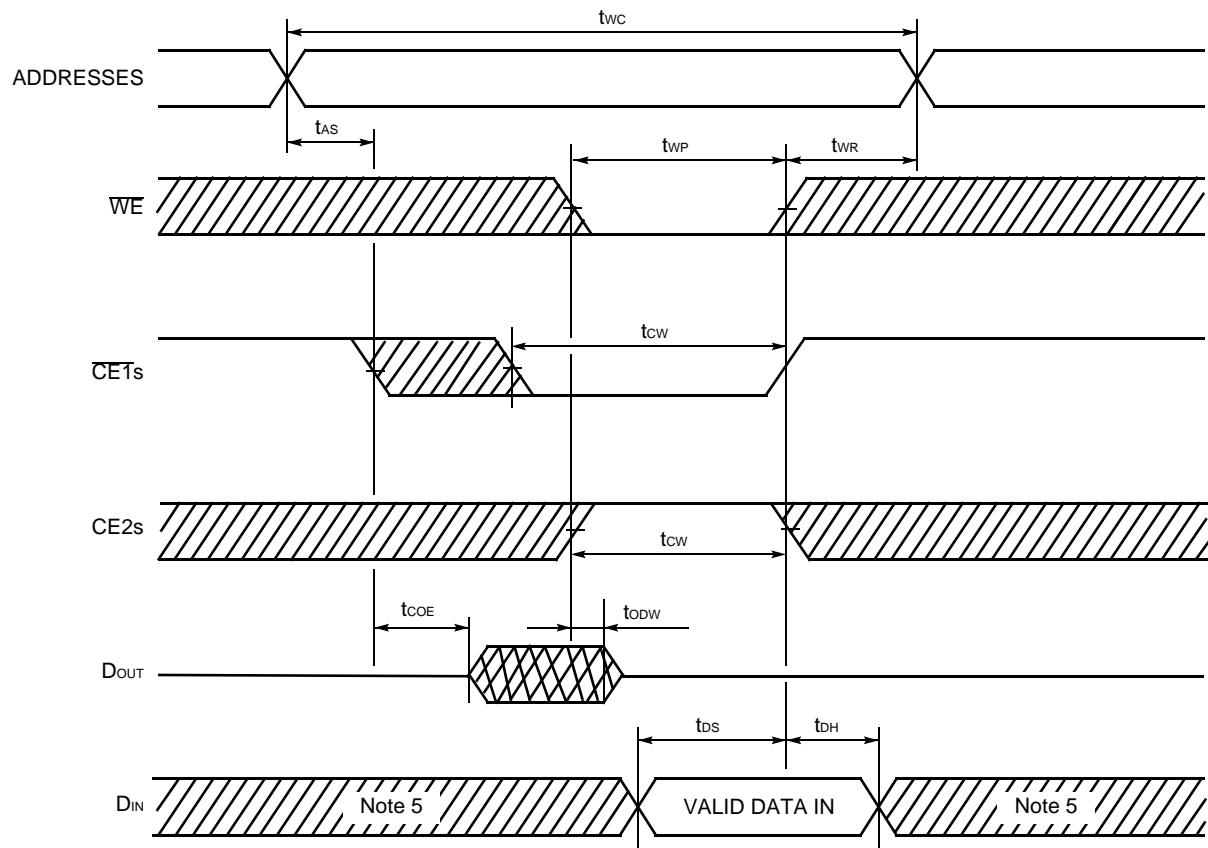
| Parameter Symbol | Parameter Description | Min. | Max. | Unit |
|------------------|---------------------------------------|------|------|------|
| t_{WC} | Write Cycle Time | 100 | — | ns |
| t_{WP} | Write Pulse Width | 60 | — | ns |
| t_{CW} | Chip Enable to End of Write | 80 | — | ns |
| t_{AS} | Address Setup Time | 0 | — | ns |
| t_{WR} | Write Recovery Time | 0 | — | ns |
| t_{ODW} | \overline{WE} Low to Output High-Z | — | 40 | ns |
| t_{OEW} | \overline{WE} High to Output Active | 0 | — | ns |
| t_{DS} | Data Setup Time | 60 | — | ns |
| t_{DH} | Data Hold Time | 0 | — | ns |

• Write Cycle (Note 4) (\overline{WE} control) (SRAM)



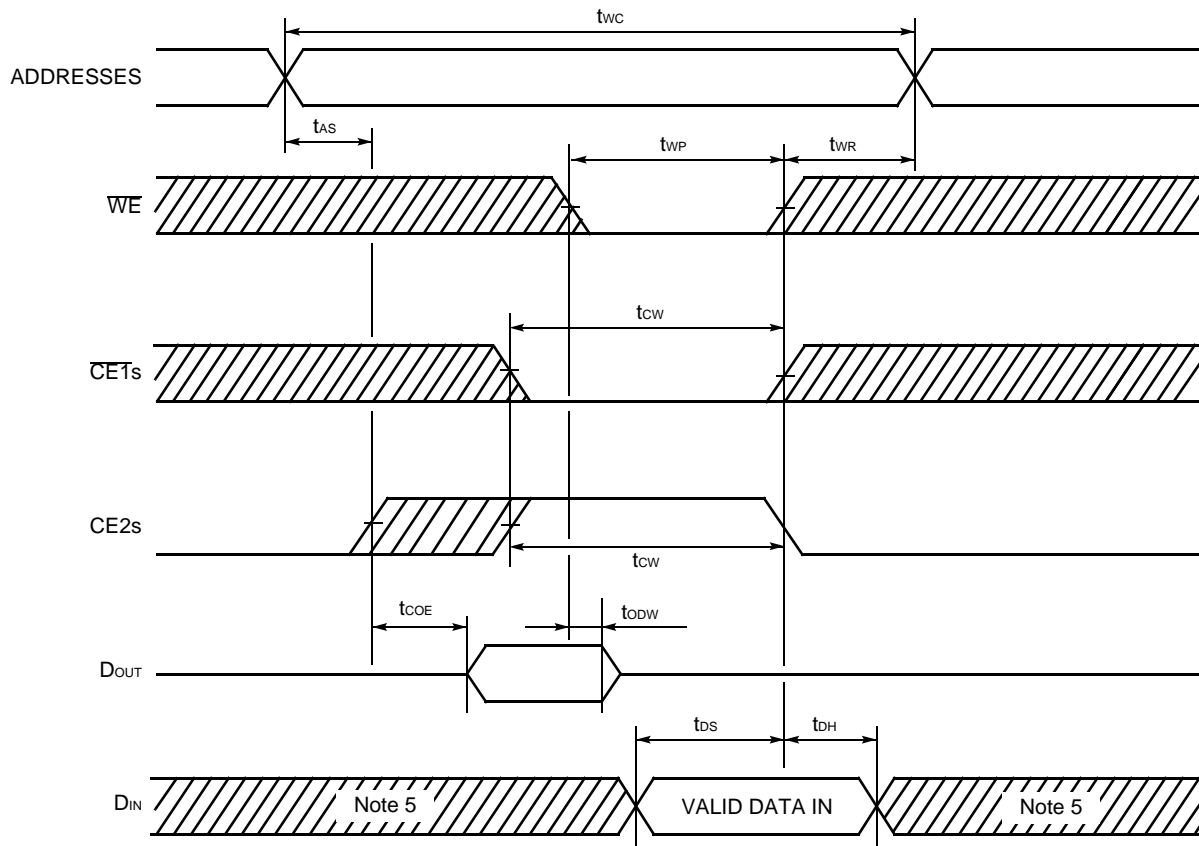
MB84VA2006-10/MB84VA2007-10

• Write Cycle (Note 4) ($\overline{CE1s}$ control) (SRAM)



- Notes:**
2. If $\overline{CE1s}$ goes LOW (or CE2s goes HIGH) coincident with or after \overline{WE} goes LOW, the output will remain at high impedance.
 3. If $\overline{CE1s}$ goes HIGH (or CE2s goes LOW) coincident with or before \overline{WE} goes HIGH, the output will remain at high impedance.
 4. If \overline{OE} is HIGH during the write cycle, the outputs will remain at high impedance.
 5. Because I/O signals may be in the output state at this Time, input signals of reverse polarity must not be applied.

• Write Cycle (Note 4) (CE2s Control) (SRAM)



- Notes:**
2. If $\overline{CE1s}$ goes LOW (or CE2s goes HIGH) coincident with or after \overline{WE} goes LOW, the output will remain at high impedance.
 3. If $\overline{CE1s}$ goes HIGH (or CE2s goes LOW) coincident with or before \overline{WE} goes HIGH, the output will remain at high impedance.
 4. If \overline{OE} is HIGH during the write cycle, the outputs will remain at high impedance.
 5. Because I/O signals may be in the output state at this Time, input signals of reverse polarity must not be applied.

MB84VA2006-10/MB84VA2007-10

■ ERASE AND PROGRAMMING PERFORMANCE (Flash)

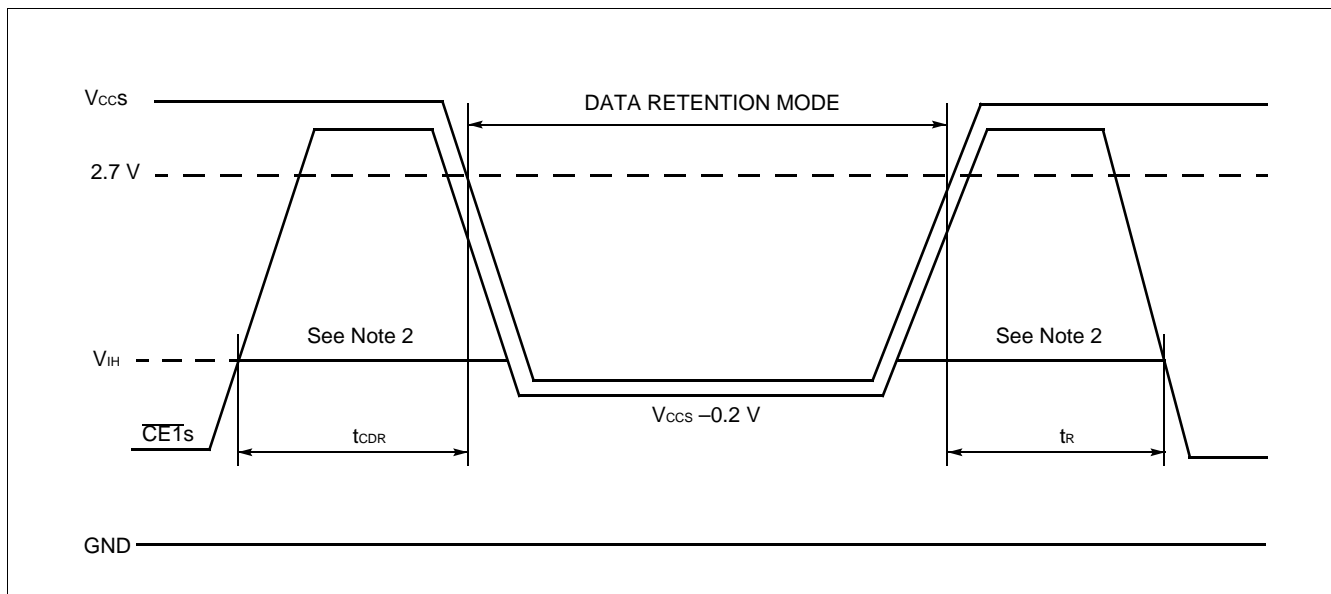
| Parameter | Limits | | | Unit | Comment |
|-----------------------|---------|------|-------|--------|--|
| | Min. | Typ. | Max. | | |
| Sector Erase Time | — | 1 | 15 | sec | Excludes programming time prior to erasure |
| Byte Programming Time | — | 8 | 3,600 | μs | Excludes system-level overhead |
| Chip Programming Time | — | 12 | 50 | sec | Excludes system-level overhead |
| Erase/Program Cycle | 100,000 | — | — | cycles | |

■ DATA RETENTION CHARACTERISTICS (SRAM)

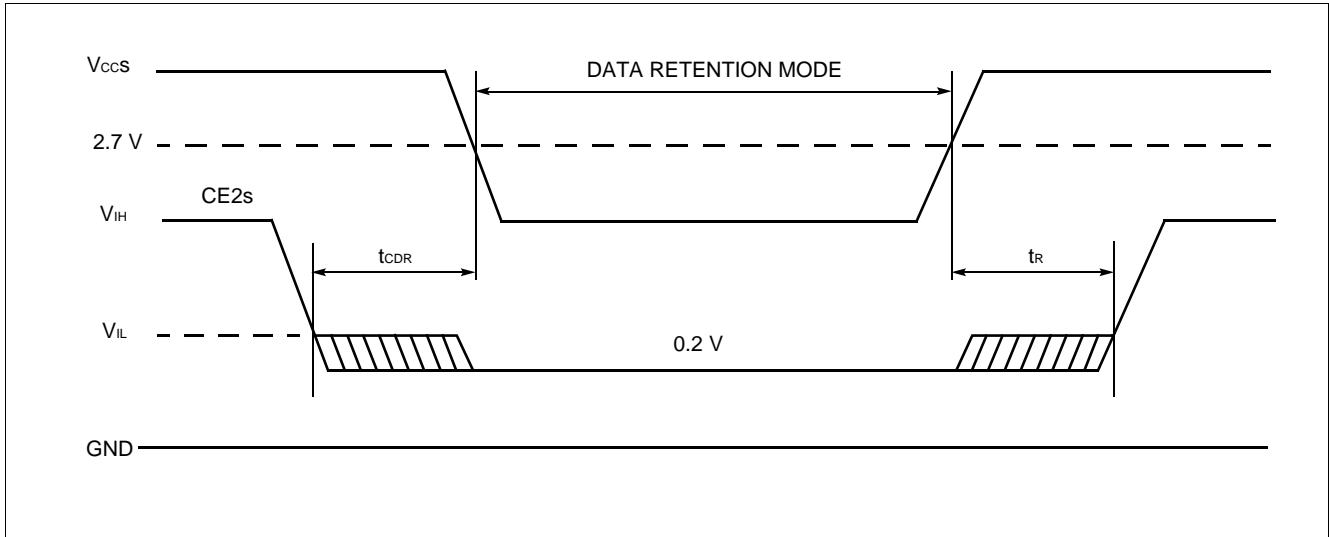
| Parameter Symbol | Parameter Description | Min. | Typ. | Max. | Unit |
|-------------------|---|-------------------------|------|------|------|
| V _{DH} | Data Retention Supply Voltage | 2.0 | — | 3.6 | V |
| I _{DDs2} | Standby Current | V _{DH} = 3.0 V | — | 30* | μA |
| | | V _{DH} = 3.6 V | — | 40 | μA |
| t _{CDR} | Chip Deselect to Data Retention Mode Time | 0 | — | — | ns |
| t _R | Recovery Time | 5 | — | — | ms |

* : 5 μA (Max.) at T_A = -20°C to +40°C

• $\overline{CE1}$ s Controlled Data Retention Mode (Note 1)



• **CE2s Controlled Data Retention Mode (Note 3)**



- Notes:**
1. In $\overline{CE1}$ s controlled data retention mode, input level of CE2s should be fixed Vccs to Vccs-0.2V or Vss to 0.2V during data retention mode. Other input and input/output pins can be used between -0.3V to Vccs+0.3V.
 2. When $\overline{CE1}$ s is operating at the VIH min. level (2.2 V), the standby current is given by ISB1s during the transition of Vccs from 3.6 to 2.2 V.
 3. In CE2s controlled data retention mode, input and input/output pins can be used between between -0.3V to Vccs+0.3V.

■ **PIN CAPACITANCE**

| Parameter Symbol | Parameter Description | Test Setup | Typ. | Max. | Unit |
|------------------|-------------------------|----------------------|-------|-------|------|
| C _{IN} | Input Capacitance | V _{IN} = 0 | T.B.D | T.B.D | pF |
| C _{OUT} | Output Capacitance | V _{OUT} = 0 | T.B.D | T.B.D | pF |
| C _{IN2} | Control Pin Capacitance | V _{IN} = 0 | T.B.D | T.B.D | pF |

Note: Test conditions T_A = 25°C, f = 1.0 MHz

■ **HANDLING OF PACKAGE**

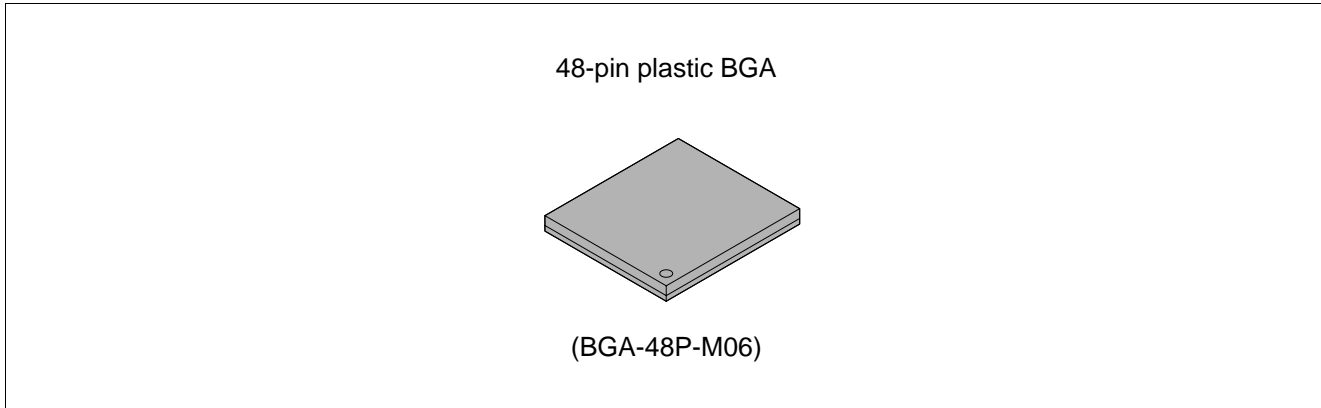
Please handle this package carefully since the sides of packages are right angle.

■ **CAUTION**

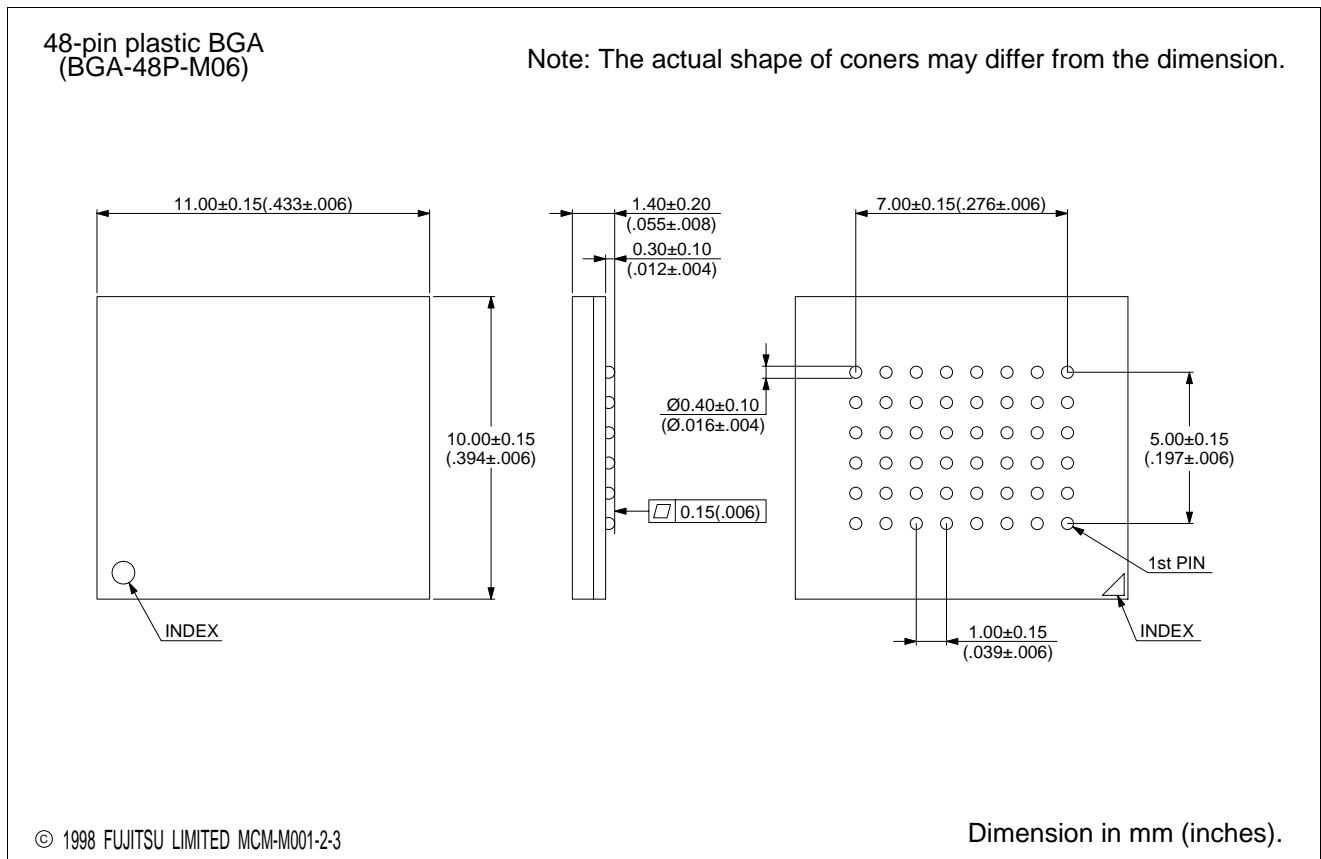
- 1.)The high voltage (VID) can not apply to address pins and control pins except \overline{RESET} . Therefore, it can not use autoselect and sector protect function by applying the high voltage (VID) to specific pins.
- 2.)For the sector protection, since the high voltage (VID) can be applied to the \overline{RESET} , it can be protected the sector using "Extended sector protect" command.

MB84VA2006-10/MB84VA2007-10

■ PACKAGE



■ PACKAGE DIMENSIONS



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