

Stacked MCP (Multi-Chip Package) FLASH MEMORY & SRAM CMOS

32M (× 8/×16) FLASH MEMORY & 4M (× 8/×16) STATIC RAM

MB84VD2218XEC-90/MB84VD2219XEC-90
MB84VD2218XEE-90/MB84VD2219XEE-90

■ FEATURES

- Power supply voltage of 2.7 V to 3.3 V
- High performance
 - 90 ns maximum access time (Flash)
 - 85 ns maximum access time (SRAM)
- Operating Temperature
 - 25 °C to +85 °C
- Package 73-ball BGA

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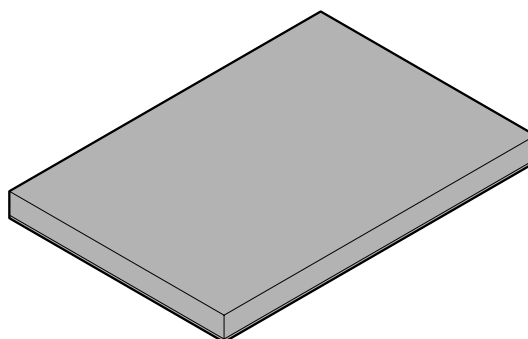
■ PRODUCT LINE UP

		Flash Memory	SRAM
Ordering Part No.	$V_{ccf}^*, V_{ccs}^* = 3.0 V \begin{matrix} +0.3 V \\ -0.3 V \end{matrix}$	MB84VD2218XEC/EE-90/MB84VD2219XEC/EE-90	
Max. Address Access Time (ns)		90	85
Max. \overline{CE} Access Time (ns)		90	85
Max. \overline{OE} Access Time (ns)		40	45

* : Both V_{ccf} and V_{ccs} must be in recommended operation range when either part is being accessed.

■ PACKAGE

73-ball plastic BGA



(BGA-73P-M01)

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1.FLASH MEMORY

- **Simultaneous Read/Write operations (dual bank)**
Multiple devices available with different bank sizes
Host system can program or erase in one bank, then immediately and simultaneously read from the other bank
Zero latency between read and write operations
Read-while-erase
Read-while-program
- **Minimum 100,000 write/erase cycles**
- **Sector erase architecture**
Eight 4 K words and sixty three 32 K words.
Any combination of sectors can be concurrently erased. Also supports full chip erase.
- **Boot Code Sector Architecture**
MB84VD2218X: Top sector
MB84VD2219X: Bottom sector
- **Embedded Erase™ Algorithms**
Automatically pre-programs and erases the chip or any sector
- **Embedded Program™ Algorithms**
Automatically writes and verifies data at specified address
- **Data Polling and Toggle Bit feature for detection of program or erase cycle completion**
- **Ready-Busy output (RY/BY)**
Hardware method for detection of program or erase cycle completion
- **Automatic sleep mode**
When addresses remain stable, automatically switch themselves to low power mode.
- **Low V_{ccf} write inhibit ≤ 2.5 V**
- **Hidden ROM (Hi-ROM) region**
64K byte of Hi-ROM, accessible through a new “Hi-ROM Enable” command sequence
Factory serialized and protected to provide a secure electronic serial number (ESN)
- **WP/ACC input pin**
At V_{IL}, allows protection of boot sectors, regardless of sector protection/unprotection status (MB84VD2218XEC/EE:SA69,SA70 MB84VD2219XEC/EE:SA0,SA1)
At V_{IH}, allows removal of boot sector protection
At V_{ACC}, program time will reduce by 40%.
- **Erase Suspend/Resume**
Suspends the erase operation to allow a read in another sector within the same device
- **Please refer to “MBM29DL32XTE/BE” data sheet in detailed function**

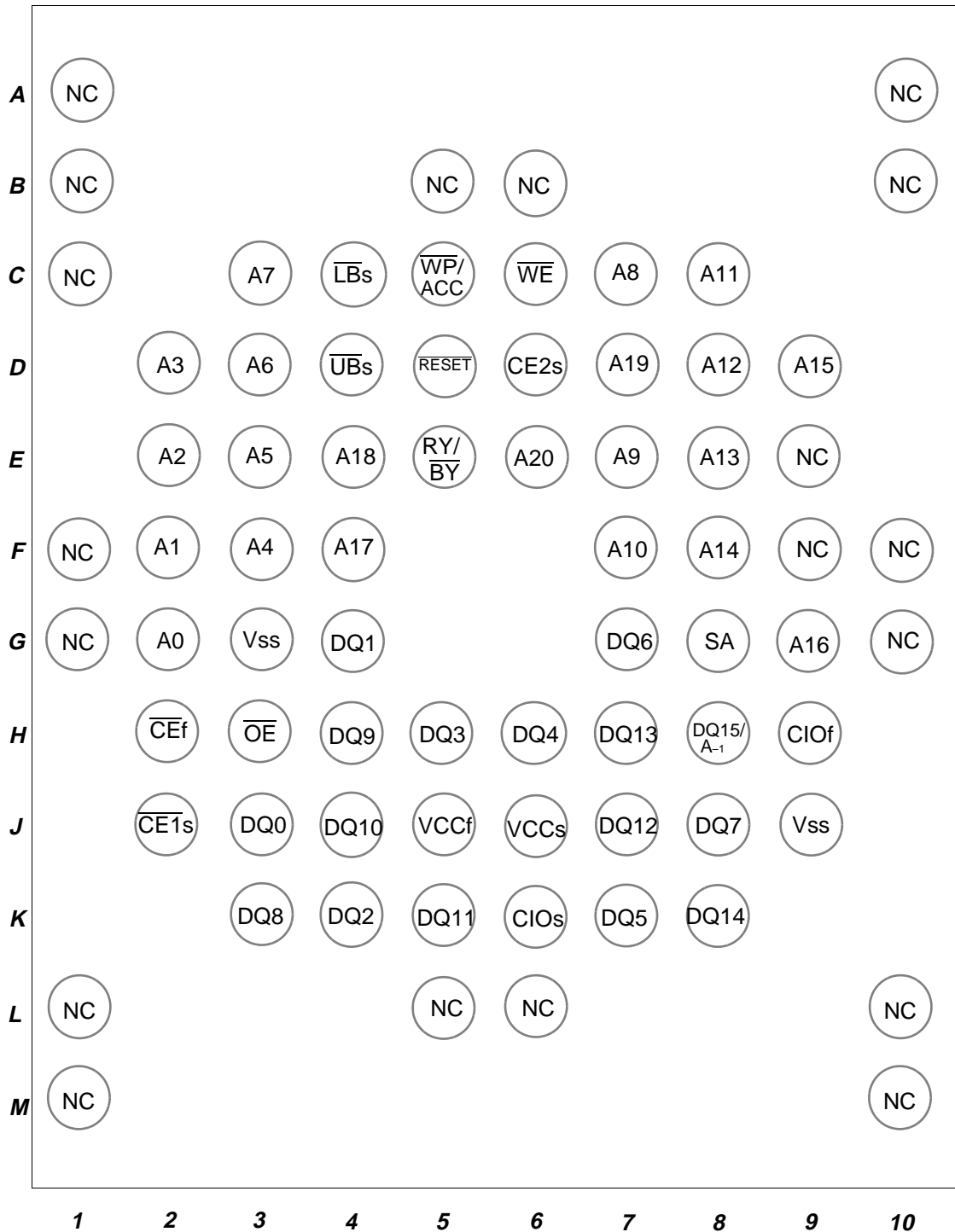
2.SRAM

- **Power dissipation**
Operating : 50 mA Max.
Standby : 15 μA Max.
- **Power down features using $\overline{CE1}$ s and CE2s**
- **Data retention supply voltage: 1.5 V to 3.3 V**
- **$\overline{CE1}$ s and CE2s Chip Select**
- **Byte data control: \overline{LB} s(DQ₀-DQ₇), \overline{UB} s(DQ₈-DQ₁₅)**

MB84VD2218XEC/EE/2219XEC/EE-90

■ PIN ASSIGNMENT

(Top View)



(BGA-73P-M01)

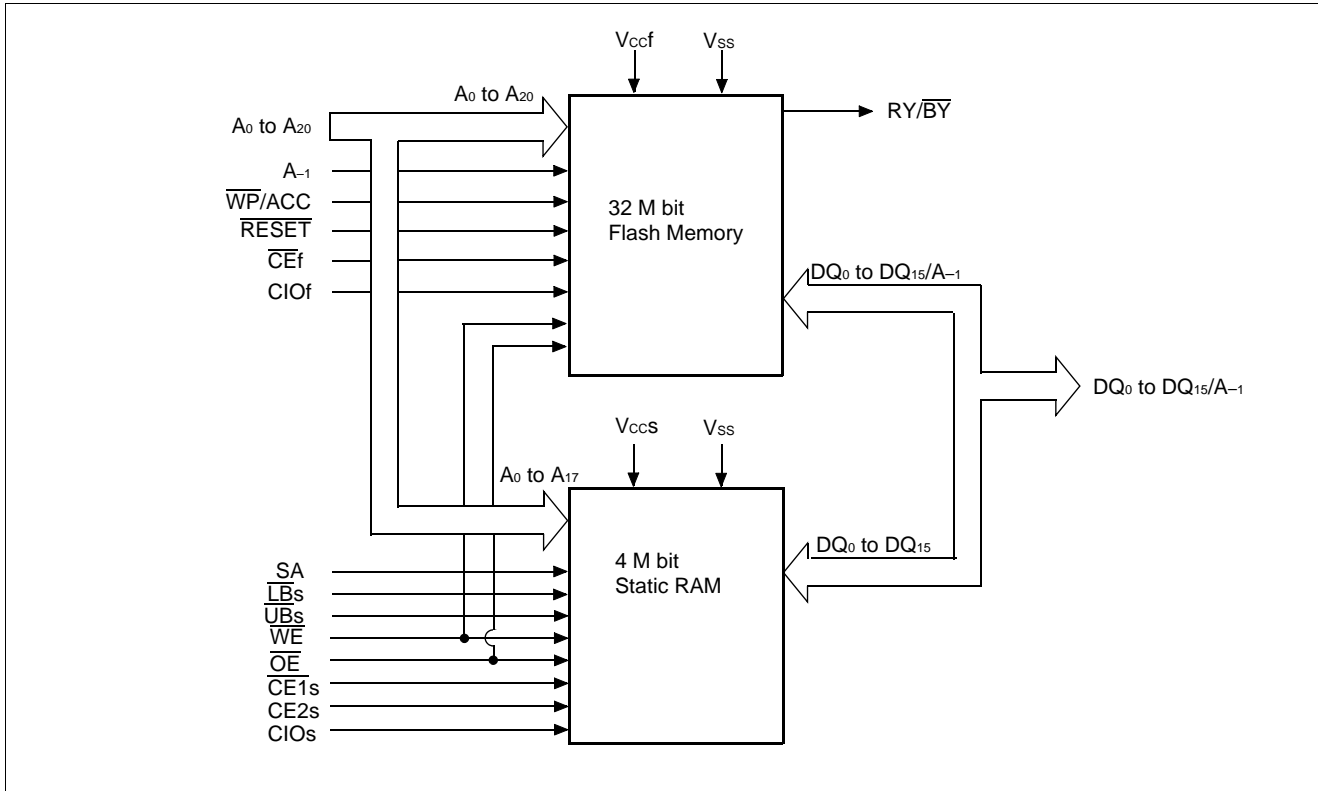
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■ PIN DESCRIPTION

Pin Name	Function	Input/Output
A ₀ to A ₁₇	Address Inputs (Common)	I
A ₋₁ , A ₁₈ to A ₂₀	Address Input (Flash)	I
SA	Address Input (SRAM)	I
DQ ₀ to DQ ₁₅	Data Inputs/Outputs (Common)	I/O
$\overline{\text{CE}}_f$	Chip Enable (Flash)	I
$\overline{\text{CE}}_{1s}$	Chip Enable (SRAM)	I
CE _{2s}	Chip Enable (SRAM)	I
$\overline{\text{OE}}$	Output Enable (Common)	I
$\overline{\text{WE}}$	Write Enable (Common)	I
RY/ $\overline{\text{BY}}$	Ready/Busy Outputs (Flash) Open Drain Output	O
$\overline{\text{UB}}_s$	Upper Byte Control (SRAM)	I
$\overline{\text{LB}}_s$	Lower Byte Control (SRAM)	I
CIO _f	I/O Configuration (Flash) CIO _f = V _{ccf} is Word mode (x16), CIO _f = V _{ss} is Byte mode (x8)	I
CIO _s	I/O Configuration (SRAM) CIO _s = V _{ccs} is Word mode (x16), CIO _s = V _{ss} is Byte mode (x8)	I
$\overline{\text{RESET}}$	Hardware Reset Pin/Sector Protection Unlock (Flash)	I
$\overline{\text{WP/ACC}}$	Write Protect / Acceleration (Flash)	I
N.C.	No Internal Connection	—
V _{ss}	Device Ground (Common)	Power
V _{ccf}	Device Power Supply (Flash)	Power
V _{ccs}	Device Power Supply (SRAM)	Power

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■ BLOCK DIAGRAM



MB84VD2218XEC/EE/2219XEC/EE-90

■ DEVICE BUS OPERATIONS

Table 1.1 User Bus Operations (Flash=Word mode; CIOf=V_{ccf}, SRAM=Word mode; CIOs=V_{ccs})

Operation *1,*3	$\overline{CE}f$	$\overline{CE}1s$	$CE2s$	\overline{OE}	\overline{WE}	SA *6	$\overline{LB}s$	$\overline{UB}s$	DQ ₀ to DQ ₇	DQ ₈ to DQ ₁₅	\overline{RESET}	$\overline{WP}/$ ACC *5
Full Standby	H	H	X	X	X	X	X	X	High-Z	High-Z	H	X
		X	L									
Output Disable	H	L	H	H	H	X	X	X	High-Z	High-Z	H	X
				X	X	X	H	H	High-Z	High-Z		
	L	H	X	H	H	X	X	X	High-Z	High-Z		
		X	L									
Read from Flash *2	L	H	X	L	H	X	X	X	D _{OUT}	D _{OUT}	H	X
		X	L									
Write to Flash	L	H	X	H	L	X	X	X	D _{IN}	D _{IN}	H	X
		X	L									
Read from SRAM	H	L	H	L	H	X	L	L	D _{OUT}	D _{OUT}	H	X
							H	L	High-Z	D _{OUT}		
							L	H	D _{OUT}	High-Z		
Write to SRAM	H	L	H	X	L	X	L	L	D _{IN}	D _{IN}	H	X
							H	L	High-Z	D _{IN}		
							L	H	D _{IN}	High-Z		
Temporary Sector Group Unprotection *4	X	X	X	X	X	X	X	X	X	X	V _{ID}	X
Flash Hardware Reset	X	H	X	X	X	X	X	X	High-Z	High-Z	L	X
		X	L									
Boot Block Sector Write Protection	X	X	X	X	X	X	X	X	X	X	X	L

Legend: L = V_{IL}, H = V_{IH}, X = V_{IL} or V_{IH}. See DC Characteristics for voltage levels.

*1 : Other operations except for indicated this column are inhibited.

*2 : \overline{WE} can be V_{IL} if \overline{OE} is V_{IL}, \overline{OE} at V_{IH} initiates the write operations.

*3 : Do not apply $\overline{CE}f = V_{IL}$, $\overline{CE}1s = V_{IL}$ and $CE2s = V_{IH}$ at a time.

*4 : It is also used for the extended sector group protections.

*5 : $\overline{WP}/ACC = V_{IL}$; protection of boot sectors.

$\overline{WP}/ACC = V_{IH}$; removal of boot sectors protection.

$\overline{WP}/ACC = V_{ACC}$ (9V); Program time will reduce by 40%.

*6 : SA; Don't care or Open.

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Table 1.2 User Bus Operations (Flash=Word mode; CIOf=V_{ccf}, SRAM=Byte mode; CIOs=V_{ss})

Operation *1,*3	$\overline{CE}f$	$\overline{CE}1s$	CE2s	\overline{OE}	\overline{WE}	SA	$\overline{LB}s$ *6	$\overline{UB}s$ *6	DQ ₀ to DQ ₇	DQ ₈ to DQ ₁₅	\overline{RESET}	$\overline{WP}/$ ACC *5
Full Standby	H	H	X	X	X	X	X	X	High-Z	High-Z	H	X
		X	L									
Output Disable	H	L	H	H	H	X	X	X	High-Z	High-Z	H	X
		X	X	X	H	H	High-Z	High-Z				
	L	H	X	H	H	X	X	X	High-Z	High-Z		
		X	L									
Read from Flash *2	L	H	X	L	H	X	X	X	D _{OUT}	D _{OUT}	H	X
		X	L									
Write to Flash	L	H	X	H	L	X	X	X	D _{IN}	D _{IN}	H	X
		X	L									
Read from SRAM	H	L	H	L	H	SA	X	X	D _{OUT}	High-Z	H	X
Write to SRAM	H	L	H	X	L	SA	X	X	D _{IN}	High-Z	H	X
Temporary Sector Group Unprotection*4	X	X	X	X	X	X	X	X	X	X	V _{ID}	X
Flash Hardware Reset	X	H	X	X	X	X	X	X	High-Z	High-Z	L	X
		X	L									
Boot Block Sector Write Protection	X	X	X	X	X	X	X	X	X	X	X	L

Legend: L = V_{IL}, H = V_{IH}, X = V_{IL} or V_{IH}. See DC Characteristics for voltage levels.

*1 : Other operations except for indicated this column are inhibited.

*2 : \overline{WE} can be V_{IL} if \overline{OE} is V_{IL}, \overline{OE} at V_{IH} initiates the write operations.

*3 : Do not apply $\overline{CE}f = V_{IL}$, $\overline{CE}1s = V_{IL}$ and CE2s = V_{IH} at a time.

*4 : It is also used for the extended sector group protections.

*5 : $\overline{WP}/ACC = V_{IL}$; protection of boot sectors.

$\overline{WP}/ACC = V_{IH}$; removal of boot sectors protection.

$\overline{WP}/ACC = V_{ACC}$ (9V); Program time will reduce by 40%.

*6 : $\overline{LB}s$, $\overline{UB}s$; Don't care or Open.

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Table 1.3 User Bus Operations (Flash=Byte mode; CIOf=V_{ss}, SRAM=Byte mode; CIOs=V_{ss})

Operation *1,*3	\overline{CEf}	$\overline{CE1s}$	$\overline{CE2s}$	DQ _{15/A-1}	\overline{OE}	\overline{WE}	SA	\overline{LBs} *6	\overline{UBs} *6	DQ ₀ to DQ ₇	DQ ₈ to DQ ₁₄	\overline{RESET}	$\overline{WP/ACC}$ *5
Full Standby	H	H	X	X	X	X	X	X	X	High-Z	High-Z	H	X
		X	L										
Output Disable	H	L	H	X	H	H	X	X	X	High-Z	High-Z	H	X
		X	L	X	X	X	H	H	High-Z	High-Z			
	L	H	X	A-1	H	H	X	X	X	High-Z	High-Z		
		X	L										
Read from Flash *2	L	H	X	A-1	L	H	X	X	X	D _{OUT}	X	H	X
		X	L										
Write to Flash	L	H	X	A-1	H	L	X	X	X	D _{IN}	X	H	X
		X	L										
Read from SRAM	H	L	H	X	L	H	SA	X	X	D _{OUT}	High-Z	H	X
Write to SRAM	H	L	H	X	X	L	SA	X	X	D _{IN}	High-Z	H	X
Temporary Sector Group Unprotection*4	X	X	X	X	X	X	X	X	X	X	X	V _{ID}	X
Flash Hardware Reset	X	H	X	X	X	X	X	X	X	High-Z	High-Z	L	X
		X	L										
Boot Block Sector Write Protection	X	X	X	X	X	X	X	X	X	X	X	X	L

Legend: L = V_{IL}, H = V_{IH}, X = V_{IL} or V_{IH}. See DC Characteristics for voltage levels.

*1 : Other operations except for indicated this column are inhibited.

*2 : \overline{WE} can be V_{IL} if \overline{OE} is V_{IL}, \overline{OE} at V_{IH} initiates the write operations.

*3 : Do not apply $\overline{CEf} = V_{IL}$, $\overline{CE1s} = V_{IL}$ and $\overline{CE2s} = V_{IH}$ at a time.

*4 : It is also used for the extended sector group protections.

*5 : $\overline{WP/ACC} = V_{IL}$; protection of boot sectors.

$\overline{WP/ACC} = V_{IH}$; removal of boot sectors protection.

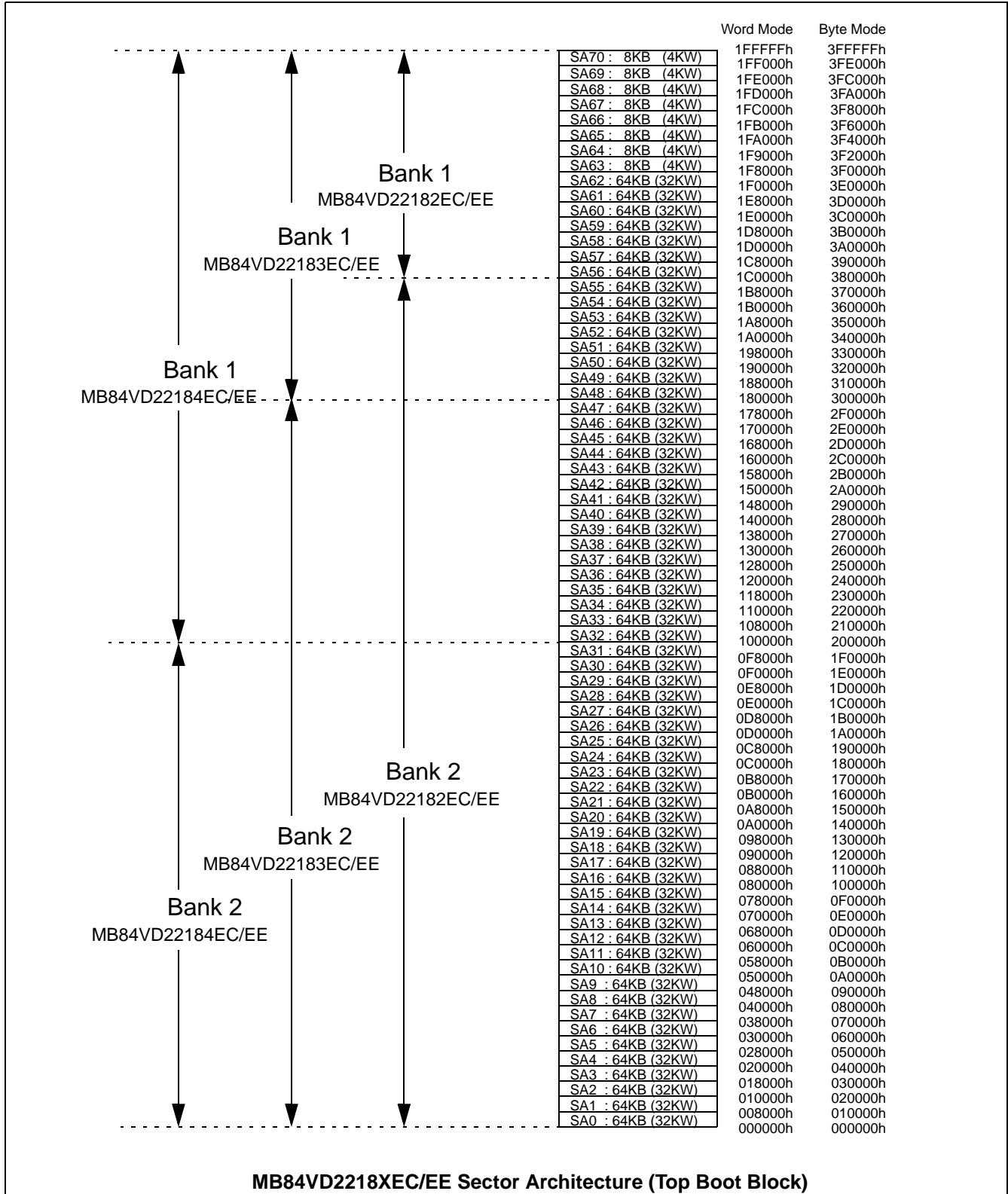
$\overline{WP/ACC} = V_{ACC}$ (9V); Program time will reduce by 40%.

*6 : \overline{LBs} , \overline{UBs} ; Don't care or Open.

MB84VD2218XEC/EE/2219XEC/EE-90

■ FLEXIBLE SECTOR-ERASE ARCHITECTURE on FLASH MEMORY

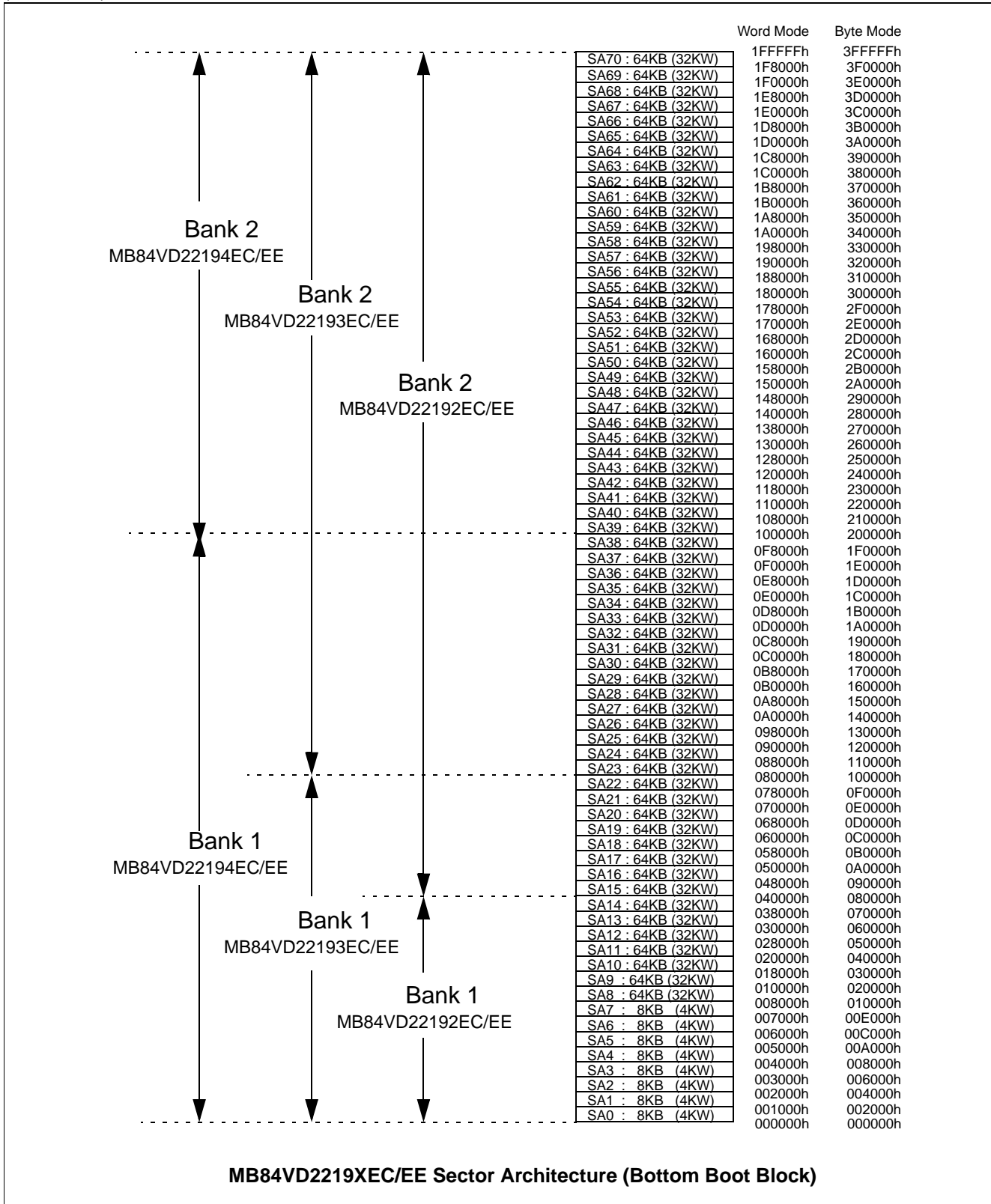
- Eight 4 K words, and sixty three 32 K words.
- Individual-sector, multiple-sector, or bulk-erase capability.



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MB84VD2218XEC/EE/2219XEC/EE-90

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MB84VD2218XEC/EE/2219XEC/EE-90

Table 2.1 Sector Address Tables (MB84VD22182EC/EE)

Bank	Sector	Sector Address										Address Range (BYTE mode)	Address Range (WORD mode)
		Bank Address											
		A20	A19	A18	A17	A16	A15	A14	A13	A12	A11		
Bank 2	SA0	0	0	0	0	0	0	X	X	X	X	000000h to 00FFFFh	000000h to 007FFFh
	SA1	0	0	0	0	0	1	X	X	X	X	010000h to 01FFFFh	008000h to 00FFFFh
	SA2	0	0	0	0	1	0	X	X	X	X	020000h to 02FFFFh	010000h to 017FFFh
	SA3	0	0	0	0	1	1	X	X	X	X	030000h to 03FFFFh	018000h to 01FFFFh
	SA4	0	0	0	1	0	0	X	X	X	X	040000h to 04FFFFh	020000h to 027FFFh
	SA5	0	0	0	1	0	1	X	X	X	X	050000h to 05FFFFh	028000h to 02FFFFh
	SA6	0	0	0	1	1	0	X	X	X	X	060000h to 06FFFFh	030000h to 037FFFh
	SA7	0	0	0	1	1	1	X	X	X	X	070000h to 07FFFFh	038000h to 03FFFFh
	SA8	0	0	1	0	0	0	X	X	X	X	080000h to 08FFFFh	040000h to 047FFFh
	SA9	0	0	1	0	0	1	X	X	X	X	090000h to 09FFFFh	048000h to 04FFFFh
	SA10	0	0	1	0	1	0	X	X	X	X	0A0000h to 0AFFFFh	050000h to 057FFFh
	SA11	0	0	1	0	1	1	X	X	X	X	0B0000h to 0BFFFFh	058000h to 05FFFFh
	SA12	0	0	1	1	0	0	X	X	X	X	0C0000h to 0CFFFFh	060000h to 067FFFh
	SA13	0	0	1	1	0	1	X	X	X	X	0D0000h to 0DFFFFh	068000h to 06FFFFh
	SA14	0	0	1	1	1	0	X	X	X	X	0E0000h to 0EFFFFh	070000h to 077FFFh
	SA15	0	0	1	1	1	1	X	X	X	X	0F0000h to 0FFFFh	078000h to 07FFFFh
	SA16	0	1	0	0	0	0	X	X	X	X	100000h to 10FFFFh	080000h to 087FFFh
	SA17	0	1	0	0	0	1	X	X	X	X	110000h to 11FFFFh	088000h to 08FFFFh
	SA18	0	1	0	0	1	0	X	X	X	X	120000h to 12FFFFh	090000h to 097FFFh
	SA19	0	1	0	0	1	1	X	X	X	X	130000h to 13FFFFh	098000h to 09FFFFh
	SA20	0	1	0	1	0	0	X	X	X	X	140000h to 14FFFFh	0A0000h to 0A7FFFh
	SA21	0	1	0	1	0	1	X	X	X	X	150000h to 15FFFFh	0A8000h to 0AFFFFh
	SA22	0	1	0	1	1	0	X	X	X	X	160000h to 16FFFFh	0B0000h to 0B7FFFh
	SA23	0	1	0	1	1	1	X	X	X	X	170000h to 17FFFFh	0B8000h to 0BFFFFh
	SA24	0	1	1	0	0	0	X	X	X	X	180000h to 18FFFFh	0C0000h to 0C7FFFh
	SA25	0	1	1	0	0	1	X	X	X	X	190000h to 19FFFFh	0C8000h to 0CFFFFh
	SA26	0	1	1	0	1	0	X	X	X	X	1A0000h to 1AFFFFh	0D0000h to 0D7FFFh
	SA27	0	1	1	0	1	1	X	X	X	X	1B0000h to 1BFFFFh	0D8000h to 0DFFFFh
	SA28	0	1	1	1	0	0	X	X	X	X	1C0000h to 1CFFFFh	0E0000h to 0E7FFFh
	SA29	0	1	1	1	0	1	X	X	X	X	1D0000h to 1DFFFFh	0E8000h to 0EFFFFh
	SA30	0	1	1	1	1	0	X	X	X	X	1E0000h to 1EFFFFh	0F0000h to 0F7FFFh
	SA31	0	1	1	1	1	1	X	X	X	X	1F0000h to 1FFFFh	0F8000h to 0FFFFh

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MB84VD2218XEC/EE/2219XEC/EE-90

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Bank	Sector	Sector Address										Address Range (BYTE mode)	Address Range (WORD mode)
		Bank Address											
		A20	A19	A18	A17	A16	A15	A14	A13	A12	A11		
Bank 2	SA32	1	0	0	0	0	0	X	X	X	X	200000h to 20FFFFh	100000h to 107FFFh
	SA33	1	0	0	0	0	1	X	X	X	X	210000h to 21FFFFh	108000h to 10FFFFh
	SA34	1	0	0	0	1	0	X	X	X	X	220000h to 22FFFFh	110000h to 117FFFh
	SA35	1	0	0	0	1	1	X	X	X	X	230000h to 23FFFFh	118000h to 11FFFFh
	SA36	1	0	0	1	0	0	X	X	X	X	240000h to 24FFFFh	120000h to 127FFFh
	SA37	1	0	0	1	0	1	X	X	X	X	250000h to 25FFFFh	128000h to 12FFFFh
	SA38	1	0	0	1	1	0	X	X	X	X	260000h to 26FFFFh	130000h to 137FFFh
	SA39	1	0	0	1	1	1	X	X	X	X	270000h to 27FFFFh	138000h to 13FFFFh
	SA40	1	0	1	0	0	0	X	X	X	X	280000h to 28FFFFh	140000h to 147FFFh
	SA41	1	0	1	0	0	1	X	X	X	X	290000h to 29FFFFh	148000h to 14FFFFh
	SA42	1	0	1	0	1	0	X	X	X	X	2A0000h to 2AFFFFh	150000h to 157FFFh
	SA43	1	0	1	0	1	1	X	X	X	X	2B0000h to 2BFFFFh	158000h to 15FFFFh
	SA44	1	0	1	1	0	0	X	X	X	X	2C0000h to 2CFFFFh	160000h to 167FFFh
	SA45	1	0	1	1	0	1	X	X	X	X	2D0000h to 2DFFFFh	168000h to 16FFFFh
	SA46	1	0	1	1	1	0	X	X	X	X	2E0000h to 2EFFFFh	170000h to 177FFFh
	SA47	1	0	1	1	1	1	X	X	X	X	2F0000h to 2FFFFh	178000h to 17FFFFh
	SA48	1	1	0	0	0	0	X	X	X	X	300000h to 30FFFFh	180000h to 187FFFh
	SA49	1	1	0	0	0	1	X	X	X	X	310000h to 31FFFFh	188000h to 18FFFFh
	SA50	1	1	0	0	1	0	X	X	X	X	320000h to 32FFFFh	190000h to 197FFFh
	SA51	1	1	0	0	1	1	X	X	X	X	330000h to 33FFFFh	198000h to 19FFFFh
SA52	1	1	0	1	0	0	X	X	X	X	340000h to 34FFFFh	1A0000h to 1A7FFFh	
SA53	1	1	0	1	0	1	X	X	X	X	350000h to 35FFFFh	1A8000h to 1AFFFFh	
SA54	1	1	0	1	1	0	X	X	X	X	360000h to 36FFFFh	1B0000h to 1B7FFFh	
SA55	1	1	0	1	1	1	X	X	X	X	370000h to 37FFFFh	1B8000h to 1BFFFFh	
Bank 1	SA56	1	1	1	0	0	0	X	X	X	X	380000h to 38FFFFh	1C0000h to 1C7FFFh
	SA57	1	1	1	0	0	1	X	X	X	X	390000h to 39FFFFh	1C8000h to 1CFFFFh
	SA58	1	1	1	0	1	0	X	X	X	X	3A0000h to 3AFFFFh	1D0000h to 1D7FFFh
	SA59	1	1	1	0	1	1	X	X	X	X	3B0000h to 3BFFFFh	1D8000h to 1DFFFFh
	SA60	1	1	1	1	0	0	X	X	X	X	3C0000h to 3CFFFFh	1E0000h to 1E7FFFh
	SA61	1	1	1	1	0	1	X	X	X	X	3D0000h to 3DFFFFh	1E8000h to 1EFFFFh
	SA62	1	1	1	1	1	0	X	X	X	X	3E0000h to 3EFFFFh	1F0000h to 1F7FFFh
	SA63	1	1	1	1	1	1	0	0	0	X	3F0000h to 3F1FFFh	1F8000h to 1F8FFFh
	SA64	1	1	1	1	1	1	0	0	1	X	3F2000h to 3F3FFFh	1F9000h to 1F9FFFh
	SA65	1	1	1	1	1	1	0	1	0	X	3F4000h to 3F5FFFh	1FA000h to 1FAFFFh
	SA66	1	1	1	1	1	1	0	1	1	X	3F6000h to 3F7FFFh	1FB000h to 1FBFFFh
	SA67	1	1	1	1	1	1	1	0	0	X	3F8000h to 3F9FFFh	1FC000h to 1FCFFFh
	SA68	1	1	1	1	1	1	1	0	1	X	3FA000h to 3FAFFFh	1FD000h to 1FDFFFh
	SA69	1	1	1	1	1	1	1	1	0	X	3FC000h to 3FCFFFh	1FE000h to 1FEFFFh
SA70	1	1	1	1	1	1	1	1	1	X	3FE000h to 3FFFFh	1FF000h to 1FFFFh	

MB84VD2218XEC/EE/2219XEC/EE-90

Table 2.2 Sector Address Tables (MB84VD22192EC/EE)

Bank	Sector	Sector Address										Address Range (BYTE mode)	Address Range (WORD mode)	
		Bank Address												
		A20	A19	A18	A17	A16	A15	A14	A13	A12	A11			
Bank 1	SA0	0	0	0	0	0	0	0	0	0	X	000000h to 001FFFh	000000h to 000FFFh	
	SA1	0	0	0	0	0	0	0	0	0	1	X	002000h to 003FFFh	001000h to 001FFFh
	SA2	0	0	0	0	0	0	0	0	1	0	X	004000h to 005FFFh	002000h to 002FFFh
	SA3	0	0	0	0	0	0	0	0	1	1	X	006000h to 007FFFh	003000h to 003FFFh
	SA4	0	0	0	0	0	0	0	1	0	0	X	008000h to 009FFFh	004000h to 004FFFh
	SA5	0	0	0	0	0	0	0	1	0	1	X	00A000h to 00BFFFh	005000h to 005FFFh
	SA6	0	0	0	0	0	0	0	1	1	0	X	00C000h to 00DFFFh	006000h to 006FFFh
	SA7	0	0	0	0	0	0	0	1	1	1	X	00E000h to 00FFFFh	007000h to 007FFFh
	SA8	0	0	0	0	0	0	1	X	X	X	X	010000h to 01FFFFh	008000h to 00FFFFh
	SA9	0	0	0	0	0	1	0	X	X	X	X	020000h to 02FFFFh	010000h to 017FFFh
	SA10	0	0	0	0	0	1	1	X	X	X	X	030000h to 03FFFFh	018000h to 01FFFFh
	SA11	0	0	0	0	1	0	0	X	X	X	X	040000h to 04FFFFh	020000h to 027FFFh
	SA12	0	0	0	0	1	0	1	X	X	X	X	050000h to 05FFFFh	028000h to 02FFFFh
	SA13	0	0	0	0	1	1	0	X	X	X	X	060000h to 06FFFFh	030000h to 037FFFh
SA14	0	0	0	0	1	1	1	X	X	X	X	070000h to 07FFFFh	038000h to 03FFFFh	
Bank 2	SA15	0	0	1	0	0	0	X	X	X	X	080000h to 08FFFFh	040000h to 047FFFh	
	SA16	0	0	1	0	0	1	X	X	X	X	090000h to 09FFFFh	048000h to 04FFFFh	
	SA17	0	0	1	0	1	0	X	X	X	X	0A0000h to 0AFFFFh	050000h to 057FFFh	
	SA18	0	0	1	0	1	1	X	X	X	X	0B0000h to 0BFFFFh	058000h to 05FFFFh	
	SA19	0	0	1	1	0	0	X	X	X	X	0C0000h to 0CFFFFh	060000h to 067FFFh	
	SA20	0	0	1	1	0	1	X	X	X	X	0D0000h to 0DFFFFh	068000h to 06FFFFh	
	SA21	0	0	1	1	1	0	X	X	X	X	0E0000h to 0EFFFFh	070000h to 077FFFh	
	SA22	0	0	1	1	1	1	X	X	X	X	0F0000h to 0FFFFFh	078000h to 07FFFFh	
	SA23	0	1	0	0	0	0	X	X	X	X	100000h to 10FFFFh	080000h to 087FFFh	
	SA24	0	1	0	0	0	1	X	X	X	X	110000h to 11FFFFh	088000h to 08FFFFh	
	SA25	0	1	0	0	1	0	X	X	X	X	120000h to 12FFFFh	090000h to 097FFFh	
	SA26	0	1	0	0	1	1	X	X	X	X	130000h to 13FFFFh	098000h to 09FFFFh	
	SA27	0	1	0	1	0	0	X	X	X	X	140000h to 14FFFFh	0A0000h to 0A7FFFh	
	SA28	0	1	0	1	0	1	X	X	X	X	150000h to 15FFFFh	0A8000h to 0AFFFFh	
	SA29	0	1	0	1	1	0	X	X	X	X	160000h to 16FFFFh	0B0000h to 0B7FFFh	
	SA30	0	1	0	1	1	1	X	X	X	X	170000h to 17FFFFh	0B8000h to 0BFFFFh	
	SA31	0	1	1	0	0	0	X	X	X	X	180000h to 18FFFFh	0C0000h to 0C7FFFh	
	SA32	0	1	1	0	0	1	X	X	X	X	190000h to 19FFFFh	0C8000h to 0CFFFFh	
	SA33	0	1	1	0	1	0	X	X	X	X	1A0000h to 1AFFFFh	0D0000h to 0D7FFFh	
	SA34	0	1	1	0	1	1	X	X	X	X	1B0000h to 1BFFFFh	0D8000h to 0DFFFFh	
	SA35	0	1	1	1	0	0	X	X	X	X	1C0000h to 1CFFFFh	0E0000h to 0E7FFFh	

(Continued)

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(Continued)

Bank	Sector	Sector Address										Address Range (BYTE mode)	Address Range (WORD mode)
		Bank Address											
		A20	A19	A18	A17	A16	A15	A14	A13	A12	A11		
Bank 2	SA36	0	1	1	1	0	1	X	X	X	X	1D0000h to 1DFFFFh	0E8000h to 0EFFFFh
	SA37	0	1	1	1	1	0	X	X	X	X	1E0000h to 1EFFFFh	0F0000h to 0F7FFFh
	SA38	0	1	1	1	1	1	X	X	X	X	1F0000h to 1FFFFFh	0F8000h to 0FFFFFFh
	SA39	1	0	0	0	0	0	X	X	X	X	200000h to 20FFFFh	100000h to 107FFFh
	SA40	1	0	0	0	0	1	X	X	X	X	210000h to 21FFFFh	108000h to 10FFFFh
	SA41	1	0	0	0	1	0	X	X	X	X	220000h to 22FFFFh	110000h to 117FFFh
	SA42	1	0	0	0	1	1	X	X	X	X	230000h to 23FFFFh	118000h to 11FFFFh
	SA43	1	0	0	1	0	0	X	X	X	X	240000h to 24FFFFh	120000h to 127FFFh
	SA44	1	0	0	1	0	1	X	X	X	X	250000h to 25FFFFh	128000h to 12FFFFh
	SA45	1	0	0	1	1	0	X	X	X	X	260000h to 26FFFFh	130000h to 137FFFh
	SA46	1	0	0	1	1	1	X	X	X	X	270000h to 27FFFFh	138000h to 13FFFFh
	SA47	1	0	1	0	0	0	X	X	X	X	280000h to 28FFFFh	140000h to 147FFFh
	SA48	1	0	1	0	0	1	X	X	X	X	290000h to 29FFFFh	148000h to 14FFFFh
	SA49	1	0	1	0	1	0	X	X	X	X	2A0000h to 2AFFFFh	150000h to 157FFFh
	SA50	1	0	1	0	1	1	X	X	X	X	2B0000h to 2BFFFFh	158000h to 15FFFFh
	SA51	1	0	1	1	0	0	X	X	X	X	2C0000h to 2CFFFFh	160000h to 167FFFh
	SA52	1	0	1	1	0	1	X	X	X	X	2D0000h to 2DFFFFh	168000h to 16FFFFh
	SA53	1	0	1	1	1	0	X	X	X	X	2E0000h to 2EFFFFh	170000h to 177FFFh
	SA54	1	0	1	1	1	1	X	X	X	X	2F0000h to 2FFFFFh	178000h to 17FFFFh
	SA55	1	1	0	0	0	0	X	X	X	X	300000h to 30FFFFh	180000h to 187FFFh
	SA56	1	1	0	0	0	1	X	X	X	X	310000h to 31FFFFh	188000h to 18FFFFh
	SA57	1	1	0	0	1	0	X	X	X	X	320000h to 32FFFFh	190000h to 197FFFh
	SA58	1	1	0	0	1	1	X	X	X	X	330000h to 33FFFFh	198000h to 19FFFFh
	SA59	1	1	0	1	0	0	X	X	X	X	340000h to 34FFFFh	1A0000h to 1A7FFFh
	SA60	1	1	0	1	0	1	X	X	X	X	350000h to 35FFFFh	1A8000h to 1AFFFFh
	SA61	1	1	0	1	1	0	X	X	X	X	360000h to 36FFFFh	1B0000h to 1B7FFFh
	SA62	1	1	0	1	1	1	X	X	X	X	370000h to 37FFFFh	1B8000h to 1BFFFFh
	SA63	1	1	1	0	0	0	X	X	X	X	380000h to 38FFFFh	1C0000h to 1C7FFFh
	SA64	1	1	1	0	0	1	X	X	X	X	390000h to 39FFFFh	1C8000h to 1CFFFFh
	SA65	1	1	1	0	1	0	X	X	X	X	3A0000h to 3AFFFFh	1D0000h to 1D7FFFh
	SA66	1	1	1	0	1	1	X	X	X	X	3B0000h to 3BFFFFh	1D8000h to 1DFFFFh
	SA67	1	1	1	1	0	0	X	X	X	X	3C0000h to 3CFFFFh	1E0000h to 1E7FFFh
SA68	1	1	1	1	0	1	X	X	X	X	3D0000h to 3DFFFFh	1E8000h to 1EFFFFh	
SA69	1	1	1	1	1	0	X	X	X	X	3E0000h to 3EFFFFh	1F0000h to 1F7FFFh	
SA70	1	1	1	1	1	1	X	X	X	X	3F0000h to 3FFFFFFh	1F8000h to 1FFFFFFh	

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Table 2.3 Sector Address Tables (MB84VD22183EC/EE)

Bank	Sector	Sector Address										Address Range (BYTE mode)	Address Range (WORD mode)
		Bank Address											
		A20	A19	A18	A17	A16	A15	A14	A13	A12	A11		
Bank 2	SA0	0	0	0	0	0	0	X	X	X	X	000000h to 00FFFFh	000000h to 007FFFh
	SA1	0	0	0	0	0	1	X	X	X	X	010000h to 01FFFFh	008000h to 00FFFFh
	SA2	0	0	0	0	1	0	X	X	X	X	020000h to 02FFFFh	010000h to 017FFFh
	SA3	0	0	0	0	1	1	X	X	X	X	030000h to 03FFFFh	018000h to 01FFFFh
	SA4	0	0	0	1	0	0	X	X	X	X	040000h to 04FFFFh	020000h to 027FFFh
	SA5	0	0	0	1	0	1	X	X	X	X	050000h to 05FFFFh	028000h to 02FFFFh
	SA6	0	0	0	1	1	0	X	X	X	X	060000h to 06FFFFh	030000h to 037FFFh
	SA7	0	0	0	1	1	1	X	X	X	X	070000h to 07FFFFh	038000h to 03FFFFh
	SA8	0	0	1	0	0	0	X	X	X	X	080000h to 08FFFFh	040000h to 047FFFh
	SA9	0	0	1	0	0	1	X	X	X	X	090000h to 09FFFFh	048000h to 04FFFFh
	SA10	0	0	1	0	1	0	X	X	X	X	0A0000h to 0AFFFFh	050000h to 057FFFh
	SA11	0	0	1	0	1	1	X	X	X	X	0B0000h to 0BFFFFh	058000h to 05FFFFh
	SA12	0	0	1	1	0	0	X	X	X	X	0C0000h to 0CFFFFh	060000h to 067FFFh
	SA13	0	0	1	1	0	1	X	X	X	X	0D0000h to 0DFFFFh	068000h to 06FFFFh
	SA14	0	0	1	1	1	0	X	X	X	X	0E0000h to 0EFFFFh	070000h to 077FFFh
	SA15	0	0	1	1	1	1	X	X	X	X	0F0000h to 0FFFFFh	078000h to 07FFFFh
	SA16	0	1	0	0	0	0	X	X	X	X	100000h to 10FFFFh	080000h to 087FFFh
	SA17	0	1	0	0	0	1	X	X	X	X	110000h to 11FFFFh	088000h to 08FFFFh
	SA18	0	1	0	0	1	0	X	X	X	X	120000h to 12FFFFh	090000h to 097FFFh
	SA19	0	1	0	0	1	1	X	X	X	X	130000h to 13FFFFh	098000h to 09FFFFh
	SA20	0	1	0	1	0	0	X	X	X	X	140000h to 14FFFFh	0A0000h to 0A7FFFh
	SA21	0	1	0	1	0	1	X	X	X	X	150000h to 15FFFFh	0A8000h to 0AFFFFh
	SA22	0	1	0	1	1	0	X	X	X	X	160000h to 16FFFFh	0B0000h to 0B7FFFh
	SA23	0	1	0	1	1	1	X	X	X	X	170000h to 17FFFFh	0B8000h to 0BFFFFh
	SA24	0	1	1	0	0	0	X	X	X	X	180000h to 18FFFFh	0C0000h to 0C7FFFh
	SA25	0	1	1	0	0	1	X	X	X	X	190000h to 19FFFFh	0C8000h to 0CFFFFh
	SA26	0	1	1	0	1	0	X	X	X	X	1A0000h to 1AFFFFh	0D0000h to 0D7FFFh
	SA27	0	1	1	0	1	1	X	X	X	X	1B0000h to 1BFFFFh	0D8000h to 0DFFFFh
	SA28	0	1	1	1	0	0	X	X	X	X	1C0000h to 1CFFFFh	0E0000h to 0E7FFFh
	SA29	0	1	1	1	0	1	X	X	X	X	1D0000h to 1DFFFFh	0E8000h to 0EFFFFh
	SA30	0	1	1	1	1	0	X	X	X	X	1E0000h to 1EFFFFh	0F0000h to 0F7FFFh
	SA31	0	1	1	1	1	1	X	X	X	X	1F0000h to 1FFFFFh	0F8000h to 0FFFFFh

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(Continued)

Bank	Sector	Sector Address										Address Range (BYTE mode)	Address Range (WORD mode)
		Bank Address											
		A20	A19	A18	A17	A16	A15	A14	A13	A12	A11		
Bank 2	SA32	1	0	0	0	0	0	X	X	X	X	200000h to 20FFFFh	100000h to 107FFFh
	SA33	1	0	0	0	0	1	X	X	X	X	210000h to 21FFFFh	108000h to 10FFFFh
	SA34	1	0	0	0	1	0	X	X	X	X	220000h to 22FFFFh	110000h to 117FFFh
	SA35	1	0	0	0	1	1	X	X	X	X	230000h to 23FFFFh	118000h to 11FFFFh
	SA36	1	0	0	1	0	0	X	X	X	X	240000h to 24FFFFh	120000h to 127FFFh
	SA37	1	0	0	1	0	1	X	X	X	X	250000h to 25FFFFh	128000h to 12FFFFh
	SA38	1	0	0	1	1	0	X	X	X	X	260000h to 26FFFFh	130000h to 137FFFh
	SA39	1	0	0	1	1	1	X	X	X	X	270000h to 27FFFFh	138000h to 13FFFFh
	SA40	1	0	1	0	0	0	X	X	X	X	280000h to 28FFFFh	140000h to 147FFFh
	SA41	1	0	1	0	0	1	X	X	X	X	290000h to 29FFFFh	148000h to 14FFFFh
	SA42	1	0	1	0	1	0	X	X	X	X	2A0000h to 2AFFFFh	150000h to 157FFFh
	SA43	1	0	1	0	1	1	X	X	X	X	2B0000h to 2BFFFFh	158000h to 15FFFFh
	SA44	1	0	1	1	0	0	X	X	X	X	2C0000h to 2CFFFFh	160000h to 167FFFh
	SA45	1	0	1	1	0	1	X	X	X	X	2D0000h to 2DFFFFh	168000h to 16FFFFh
	SA46	1	0	1	1	1	0	X	X	X	X	2E0000h to 2EFFFFh	170000h to 177FFFh
SA47	1	0	1	1	1	1	X	X	X	X	2F0000h to 2FFFFFh	178000h to 17FFFFh	
Bank 1	SA48	1	1	0	0	0	0	X	X	X	X	300000h to 30FFFFh	180000h to 187FFFh
	SA49	1	1	0	0	0	1	X	X	X	X	310000h to 31FFFFh	188000h to 18FFFFh
	SA50	1	1	0	0	1	0	X	X	X	X	320000h to 32FFFFh	190000h to 197FFFh
	SA51	1	1	0	0	1	1	X	X	X	X	330000h to 33FFFFh	198000h to 19FFFFh
	SA52	1	1	0	1	0	0	X	X	X	X	340000h to 34FFFFh	1A0000h to 1A7FFFh
	SA53	1	1	0	1	0	1	X	X	X	X	350000h to 35FFFFh	1A8000h to 1AFFFFh
	SA54	1	1	0	1	1	0	X	X	X	X	360000h to 36FFFFh	1B0000h to 1B7FFFh
	SA55	1	1	0	1	1	1	X	X	X	X	370000h to 37FFFFh	1B8000h to 1BFFFFh
	SA56	1	1	1	0	0	0	X	X	X	X	380000h to 38FFFFh	1C0000h to 1C7FFFh
	SA57	1	1	1	0	0	1	X	X	X	X	390000h to 39FFFFh	1C8000h to 1CFFFFh
	SA58	1	1	1	0	1	0	X	X	X	X	3A0000h to 3AFFFFh	1D0000h to 1D7FFFh
	SA59	1	1	1	0	1	1	X	X	X	X	3B0000h to 3BFFFFh	1D8000h to 1DFFFFh
	SA60	1	1	1	1	0	0	X	X	X	X	3C0000h to 3CFFFFh	1E0000h to 1E7FFFh
	SA61	1	1	1	1	0	1	X	X	X	X	3D0000h to 3DFFFFh	1E8000h to 1EFFFFh
	SA62	1	1	1	1	1	0	X	X	X	X	3E0000h to 3EFFFFh	1F0000h to 1F7FFFh
	SA63	1	1	1	1	1	1	0	0	0	X	3F0000h to 3F1FFFh	1F8000h to 1F8FFFh
	SA64	1	1	1	1	1	1	0	0	1	X	3F2000h to 3F3FFFh	1F9000h to 1F9FFFh
	SA65	1	1	1	1	1	1	0	1	0	X	3F4000h to 3F5FFFh	1FA000h to 1FAFFFh
	SA66	1	1	1	1	1	1	0	1	1	X	3F6000h to 3F7FFFh	1FB000h to 1FBFFFh
	SA67	1	1	1	1	1	1	1	0	0	X	3F8000h to 3F9FFFh	1FC000h to 1FCFFFh
	SA68	1	1	1	1	1	1	1	0	1	X	3FA000h to 3FAFFFh	1FD000h to 1FDFFFh
SA69	1	1	1	1	1	1	1	1	0	X	3FC000h to 3FCFFFh	1FE000h to 1FEFFFh	
SA70	1	1	1	1	1	1	1	1	1	X	3FE000h to 3FFFFFh	1FF000h to 1FFFFFh	

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Table 2.4 Sector Address Tables (MB84VD22193EC/EE)

Bank	Sector	Sector Address										Address Range (BYTE mode)	Address Range (WORD mode)	
		Bank Address												
		A20	A19	A18	A17	A16	A15	A14	A13	A12	A11			
Bank 1	SA0	0	0	0	0	0	0	0	0	0	X	000000h to 001FFFh	000000h to 000FFFh	
	SA1	0	0	0	0	0	0	0	0	0	1	X	002000h to 003FFFh	001000h to 001FFFh
	SA2	0	0	0	0	0	0	0	0	1	0	X	004000h to 005FFFh	002000h to 002FFFh
	SA3	0	0	0	0	0	0	0	0	1	1	X	006000h to 007FFFh	003000h to 003FFFh
	SA4	0	0	0	0	0	0	0	1	0	0	X	008000h to 009FFFh	004000h to 004FFFh
	SA5	0	0	0	0	0	0	0	1	0	1	X	00A000h to 00BFFFh	005000h to 005FFFh
	SA6	0	0	0	0	0	0	0	1	1	0	X	00C000h to 00DFFFh	006000h to 006FFFh
	SA7	0	0	0	0	0	0	0	1	1	1	X	00E000h to 00FFFFh	007000h to 007FFFh
	SA8	0	0	0	0	0	0	1	X	X	X	X	010000h to 01FFFFh	008000h to 00FFFFh
	SA9	0	0	0	0	1	0	X	X	X	X	X	020000h to 02FFFFh	010000h to 017FFFh
	SA10	0	0	0	0	1	1	X	X	X	X	X	030000h to 03FFFFh	018000h to 01FFFFh
	SA11	0	0	0	1	0	0	X	X	X	X	X	040000h to 04FFFFh	020000h to 027FFFh
	SA12	0	0	0	1	0	1	X	X	X	X	X	050000h to 05FFFFh	028000h to 02FFFFh
	SA13	0	0	0	1	1	0	X	X	X	X	X	060000h to 06FFFFh	030000h to 037FFFh
	SA14	0	0	0	1	1	1	X	X	X	X	X	070000h to 07FFFFh	038000h to 03FFFFh
	SA15	0	0	1	0	0	0	X	X	X	X	X	080000h to 08FFFFh	040000h to 047FFFh
	SA16	0	0	1	0	0	1	X	X	X	X	X	090000h to 09FFFFh	048000h to 04FFFFh
	SA17	0	0	1	0	1	0	X	X	X	X	X	0A0000h to 0AFFFFh	050000h to 057FFFh
	SA18	0	0	1	0	1	1	X	X	X	X	X	0B0000h to 0BFFFFh	058000h to 05FFFFh
	SA19	0	0	1	1	0	0	X	X	X	X	X	0C0000h to 0CFFFFh	060000h to 067FFFh
	SA20	0	0	1	1	0	1	X	X	X	X	X	0D0000h to 0DFFFFh	068000h to 06FFFFh
	SA21	0	0	1	1	1	0	X	X	X	X	X	0E0000h to 0EFFFFh	070000h to 077FFFh
SA22	0	0	1	1	1	1	X	X	X	X	X	0F0000h to 0FFFFFh	078000h to 07FFFFh	
Bank 2	SA23	0	1	0	0	0	0	X	X	X	X	100000h to 10FFFFh	080000h to 087FFFh	
	SA24	0	1	0	0	0	1	X	X	X	X	110000h to 11FFFFh	088000h to 08FFFFh	
	SA25	0	1	0	0	1	0	X	X	X	X	120000h to 12FFFFh	090000h to 097FFFh	
	SA26	0	1	0	0	1	1	X	X	X	X	130000h to 13FFFFh	098000h to 09FFFFh	
	SA27	0	1	0	1	0	0	X	X	X	X	140000h to 14FFFFh	0A0000h to 0A7FFFh	
	SA28	0	1	0	1	0	1	X	X	X	X	150000h to 15FFFFh	0A8000h to 0AFFFFh	
	SA29	0	1	0	1	1	0	X	X	X	X	160000h to 16FFFFh	0B0000h to 0B7FFFh	
	SA30	0	1	0	1	1	1	X	X	X	X	170000h to 17FFFFh	0B8000h to 0BFFFFh	
	SA31	0	1	1	0	0	0	X	X	X	X	180000h to 18FFFFh	0C0000h to 0C7FFFh	
	SA32	0	1	1	0	0	1	X	X	X	X	190000h to 19FFFFh	0C8000h to 0CFFFFh	
	SA33	0	1	1	0	1	0	X	X	X	X	1A0000h to 1AFFFFh	0D0000h to 0D7FFFh	
	SA34	0	1	1	0	1	1	X	X	X	X	1B0000h to 1BFFFFh	0D8000h to 0DFFFFh	
	SA35	0	1	1	1	0	0	X	X	X	X	1C0000h to 1CFFFFh	0E0000h to 0E7FFFh	

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(Continued)

Bank	Sector	Sector Address										Address Range (BYTE mode)	Address Range (WORD mode)
		Bank Address											
		A20	A19	A18	A17	A16	A15	A14	A13	A12	A11		
Bank 2	SA36	0	1	1	1	0	1	X	X	X	X	1D0000h to 1DFFFFh	0E8000h to 0EFFFFh
	SA37	0	1	1	1	1	0	X	X	X	X	1E0000h to 1EFFFFh	0F0000h to 0F7FFFh
	SA38	0	1	1	1	1	1	X	X	X	X	1F0000h to 1FFFFFh	0F8000h to 0FFFFFFh
	SA39	1	0	0	0	0	0	X	X	X	X	200000h to 20FFFFh	100000h to 107FFFh
	SA40	1	0	0	0	0	1	X	X	X	X	210000h to 21FFFFh	108000h to 10FFFFh
	SA41	1	0	0	0	1	0	X	X	X	X	220000h to 22FFFFh	110000h to 117FFFh
	SA42	1	0	0	0	1	1	X	X	X	X	230000h to 23FFFFh	118000h to 11FFFFh
	SA43	1	0	0	1	0	0	X	X	X	X	240000h to 24FFFFh	120000h to 127FFFh
	SA44	1	0	0	1	0	1	X	X	X	X	250000h to 25FFFFh	128000h to 12FFFFh
	SA45	1	0	0	1	1	0	X	X	X	X	260000h to 26FFFFh	130000h to 137FFFh
	SA46	1	0	0	1	1	1	X	X	X	X	270000h to 27FFFFh	138000h to 13FFFFh
	SA47	1	0	1	0	0	0	X	X	X	X	280000h to 28FFFFh	140000h to 147FFFh
	SA48	1	0	1	0	0	1	X	X	X	X	290000h to 29FFFFh	148000h to 14FFFFh
	SA49	1	0	1	0	1	0	X	X	X	X	2A0000h to 2AFFFFh	150000h to 157FFFh
	SA50	1	0	1	0	1	1	X	X	X	X	2B0000h to 2BFFFFh	158000h to 15FFFFh
	SA51	1	0	1	1	0	0	X	X	X	X	2C0000h to 2CFFFFh	160000h to 167FFFh
	SA52	1	0	1	1	0	1	X	X	X	X	2D0000h to 2DFFFFh	168000h to 16FFFFh
	SA53	1	0	1	1	1	0	X	X	X	X	2E0000h to 2EFFFFh	170000h to 177FFFh
	SA54	1	0	1	1	1	1	X	X	X	X	2F0000h to 2FFFFFh	178000h to 17FFFFh
	SA55	1	1	0	0	0	0	X	X	X	X	300000h to 30FFFFh	180000h to 187FFFh
	SA56	1	1	0	0	0	1	X	X	X	X	310000h to 31FFFFh	188000h to 18FFFFh
	SA57	1	1	0	0	1	0	X	X	X	X	320000h to 32FFFFh	190000h to 197FFFh
	SA58	1	1	0	0	1	1	X	X	X	X	330000h to 33FFFFh	198000h to 19FFFFh
	SA59	1	1	0	1	0	0	X	X	X	X	340000h to 34FFFFh	1A0000h to 1A7FFFh
	SA60	1	1	0	1	0	1	X	X	X	X	350000h to 35FFFFh	1A8000h to 1AFFFFh
	SA61	1	1	0	1	1	0	X	X	X	X	360000h to 36FFFFh	1B0000h to 1B7FFFh
	SA62	1	1	0	1	1	1	X	X	X	X	370000h to 37FFFFh	1B8000h to 1BFFFFh
	SA63	1	1	1	0	0	0	X	X	X	X	380000h to 38FFFFh	1C0000h to 1C7FFFh
	SA64	1	1	1	0	0	1	X	X	X	X	390000h to 39FFFFh	1C8000h to 1CFFFFh
	SA65	1	1	1	0	1	0	X	X	X	X	3A0000h to 3AFFFFh	1D0000h to 1D7FFFh
SA66	1	1	1	0	1	1	X	X	X	X	3B0000h to 3BFFFFh	1D8000h to 1DFFFFh	
SA67	1	1	1	1	0	0	X	X	X	X	3C0000h to 3CFFFFh	1E0000h to 1E7FFFh	
SA68	1	1	1	1	0	1	X	X	X	X	3D0000h to 3DFFFFh	1E8000h to 1EFFFFh	
SA69	1	1	1	1	1	0	X	X	X	X	3E0000h to 3EFFFFh	1F0000h to 1F7FFFh	
SA70	1	1	1	1	1	1	X	X	X	X	3F0000h to 3FFFFFh	1F8000h to 1FFFFFFh	

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Table 2.5 Sector Address Tables (MB84VD22184EC/EE)

Bank	Sector	Sector Address										Address Range (BYTE mode)	Address Range (WORD mode)
		Bank Address											
		A20	A19	A18	A17	A16	A15	A14	A13	A12	A11		
Bank 2	SA0	0	0	0	0	0	0	X	X	X	X	000000h to 00FFFFh	000000h to 007FFFh
	SA1	0	0	0	0	0	1	X	X	X	X	010000h to 01FFFFh	008000h to 00FFFFh
	SA2	0	0	0	0	1	0	X	X	X	X	020000h to 02FFFFh	010000h to 017FFFh
	SA3	0	0	0	0	1	1	X	X	X	X	030000h to 03FFFFh	018000h to 01FFFFh
	SA4	0	0	0	1	0	0	X	X	X	X	040000h to 04FFFFh	020000h to 027FFFh
	SA5	0	0	0	1	0	1	X	X	X	X	050000h to 05FFFFh	028000h to 02FFFFh
	SA6	0	0	0	1	1	0	X	X	X	X	060000h to 06FFFFh	030000h to 037FFFh
	SA7	0	0	0	1	1	1	X	X	X	X	070000h to 07FFFFh	038000h to 03FFFFh
	SA8	0	0	1	0	0	0	X	X	X	X	080000h to 08FFFFh	040000h to 047FFFh
	SA9	0	0	1	0	0	1	X	X	X	X	090000h to 09FFFFh	048000h to 04FFFFh
	SA10	0	0	1	0	1	0	X	X	X	X	0A0000h to 0AFFFFh	050000h to 057FFFh
	SA11	0	0	1	0	1	1	X	X	X	X	0B0000h to 0BFFFFh	058000h to 05FFFFh
	SA12	0	0	1	1	0	0	X	X	X	X	0C0000h to 0CFFFFh	060000h to 067FFFh
	SA13	0	0	1	1	0	1	X	X	X	X	0D0000h to 0DFFFFh	068000h to 06FFFFh
	SA14	0	0	1	1	1	0	X	X	X	X	0E0000h to 0EFFFFh	070000h to 077FFFh
	SA15	0	0	1	1	1	1	X	X	X	X	0F0000h to 0FFFFFh	078000h to 07FFFFh
	SA16	0	1	0	0	0	0	X	X	X	X	100000h to 10FFFFh	080000h to 087FFFh
	SA17	0	1	0	0	0	1	X	X	X	X	110000h to 11FFFFh	088000h to 08FFFFh
	SA18	0	1	0	0	1	0	X	X	X	X	120000h to 12FFFFh	090000h to 097FFFh
	SA19	0	1	0	0	1	1	X	X	X	X	130000h to 13FFFFh	098000h to 09FFFFh
	SA20	0	1	0	1	0	0	X	X	X	X	140000h to 14FFFFh	0A0000h to 0A7FFFh
	SA21	0	1	0	1	0	1	X	X	X	X	150000h to 15FFFFh	0A8000h to 0AFFFFh
	SA22	0	1	0	1	1	0	X	X	X	X	160000h to 16FFFFh	0B0000h to 0B7FFFh
	SA23	0	1	0	1	1	1	X	X	X	X	170000h to 17FFFFh	0B8000h to 0BFFFFh
	SA24	0	1	1	0	0	0	X	X	X	X	180000h to 18FFFFh	0C0000h to 0C7FFFh
	SA25	0	1	1	0	0	1	X	X	X	X	190000h to 19FFFFh	0C8000h to 0CFFFFh
	SA26	0	1	1	0	1	0	X	X	X	X	1A0000h to 1AFFFFh	0D0000h to 0D7FFFh
	SA27	0	1	1	0	1	1	X	X	X	X	1B0000h to 1BFFFFh	0D8000h to 0DFFFFh
	SA28	0	1	1	1	0	0	X	X	X	X	1C0000h to 1CFFFFh	0E0000h to 0E7FFFh
	SA29	0	1	1	1	0	1	X	X	X	X	1D0000h to 1DFFFFh	0E8000h to 0EFFFFh
	SA30	0	1	1	1	1	0	X	X	X	X	1E0000h to 1EFFFFh	0F0000h to 0F7FFFh
	SA31	0	1	1	1	1	1	X	X	X	X	1F0000h to 1FFFFFh	0F8000h to 0FFFFFh

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(Continued)

Bank	Sector	Sector Address										Address Range (BYTE mode)	Address Range (WORD mode)
		Bank Address											
		A20	A19	A18	A17	A16	A15	A14	A13	A12	A11		
Bank 1	SA32	1	0	0	0	0	0	X	X	X	X	200000h to 20FFFFh	100000h to 107FFFh
	SA33	1	0	0	0	0	1	X	X	X	X	210000h to 21FFFFh	108000h to 10FFFFh
	SA34	1	0	0	0	1	0	X	X	X	X	220000h to 22FFFFh	110000h to 117FFFh
	SA35	1	0	0	0	1	1	X	X	X	X	230000h to 23FFFFh	118000h to 11FFFFh
	SA36	1	0	0	1	0	0	X	X	X	X	240000h to 24FFFFh	120000h to 127FFFh
	SA37	1	0	0	1	0	1	X	X	X	X	250000h to 25FFFFh	128000h to 12FFFFh
	SA38	1	0	0	1	1	0	X	X	X	X	260000h to 26FFFFh	130000h to 137FFFh
	SA39	1	0	0	1	1	1	X	X	X	X	270000h to 27FFFFh	138000h to 13FFFFh
	SA40	1	0	1	0	0	0	X	X	X	X	280000h to 28FFFFh	140000h to 147FFFh
	SA41	1	0	1	0	0	1	X	X	X	X	290000h to 29FFFFh	148000h to 14FFFFh
	SA42	1	0	1	0	1	0	X	X	X	X	2A0000h to 2AFFFFh	150000h to 157FFFh
	SA43	1	0	1	0	1	1	X	X	X	X	2B0000h to 2BFFFFh	158000h to 15FFFFh
	SA44	1	0	1	1	0	0	X	X	X	X	2C0000h to 2CFFFFh	160000h to 167FFFh
	SA45	1	0	1	1	0	1	X	X	X	X	2D0000h to 2DFFFFh	168000h to 16FFFFh
	SA46	1	0	1	1	1	0	X	X	X	X	2E0000h to 2EFFFFh	170000h to 177FFFh
	SA47	1	0	1	1	1	1	X	X	X	X	2F0000h to 2FFFFh	178000h to 17FFFFh
	SA48	1	1	0	0	0	0	X	X	X	X	300000h to 30FFFFh	180000h to 187FFFh
	SA49	1	1	0	0	0	1	X	X	X	X	310000h to 31FFFFh	188000h to 18FFFFh
	SA50	1	1	0	0	1	0	X	X	X	X	320000h to 32FFFFh	190000h to 197FFFh
	SA51	1	1	0	0	1	1	X	X	X	X	330000h to 33FFFFh	198000h to 19FFFFh
	SA52	1	1	0	1	0	0	X	X	X	X	340000h to 34FFFFh	1A0000h to 1A7FFFh
	SA53	1	1	0	1	0	1	X	X	X	X	350000h to 35FFFFh	1A8000h to 1AFFFFh
	SA54	1	1	0	1	1	0	X	X	X	X	360000h to 36FFFFh	1B0000h to 1B7FFFh
	SA55	1	1	0	1	1	1	X	X	X	X	370000h to 37FFFFh	1B8000h to 1BFFFFh
	SA56	1	1	1	0	0	0	X	X	X	X	380000h to 38FFFFh	1C0000h to 1C7FFFh
	SA57	1	1	1	0	0	1	X	X	X	X	390000h to 39FFFFh	1C8000h to 1CFFFFh
	SA58	1	1	1	0	1	0	X	X	X	X	3A0000h to 3AFFFFh	1D0000h to 1D7FFFh
	SA59	1	1	1	0	1	1	X	X	X	X	3B0000h to 3BFFFFh	1D8000h to 1DFFFFh
	SA60	1	1	1	1	0	0	X	X	X	X	3C0000h to 3CFFFFh	1E0000h to 1E7FFFh
	SA61	1	1	1	1	0	1	X	X	X	X	3D0000h to 3DFFFFh	1E8000h to 1EFFFFh
SA62	1	1	1	1	1	0	X	X	X	X	3E0000h to 3EFFFFh	1F0000h to 1F7FFFh	
SA63	1	1	1	1	1	1	0	0	0	X	3F0000h to 3F1FFFh	1F8000h to 1F8FFFh	
SA64	1	1	1	1	1	1	0	0	1	X	3F2000h to 3F3FFFh	1F9000h to 1F9FFFh	
SA65	1	1	1	1	1	1	0	1	0	X	3F4000h to 3F5FFFh	1FA000h to 1FAFFFh	
SA66	1	1	1	1	1	1	0	1	1	X	3F6000h to 3F7FFFh	1FB000h to 1FBFFFh	
SA67	1	1	1	1	1	1	1	0	0	X	3F8000h to 3F9FFFh	1FC000h to 1FCFFFh	
SA68	1	1	1	1	1	1	1	0	1	X	3FA000h to 3FAFFFh	1FD000h to 1FDFFFh	
SA69	1	1	1	1	1	1	1	1	0	X	3FC000h to 3FCFFFh	1FE000h to 1FEFFFh	
SA70	1	1	1	1	1	1	1	1	1	X	3FE000h to 3FFFFFFh	1FF000h to 1FFFFFFh	

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Table 2.6 Sector Address Tables (MB84VD22194EC/EE)

Bank	Sector	Sector Address										Address Range (BYTE mode)	Address Range (WORD mode)	
		Bank Address												
		A20	A19	A18	A17	A16	A15	A14	A13	A12	A11			
Bank 1	SA0	0	0	0	0	0	0	0	0	0	X	000000h to 001FFFh	000000h to 000FFFh	
	SA1	0	0	0	0	0	0	0	0	0	1	X	002000h to 003FFFh	001000h to 001FFFh
	SA2	0	0	0	0	0	0	0	0	1	0	X	004000h to 005FFFh	002000h to 002FFFh
	SA3	0	0	0	0	0	0	0	0	1	1	X	006000h to 007FFFh	003000h to 003FFFh
	SA4	0	0	0	0	0	0	0	1	0	0	X	008000h to 009FFFh	004000h to 004FFFh
	SA5	0	0	0	0	0	0	0	1	0	1	X	00A000h to 00BFFFh	005000h to 005FFFh
	SA6	0	0	0	0	0	0	0	1	1	0	X	00C000h to 00DFFFh	006000h to 006FFFh
	SA7	0	0	0	0	0	0	0	1	1	1	X	00E000h to 00FFFFh	007000h to 007FFFh
	SA8	0	0	0	0	0	0	1	X	X	X	X	010000h to 01FFFFh	008000h to 00FFFFh
	SA9	0	0	0	0	0	1	0	X	X	X	X	020000h to 02FFFFh	010000h to 017FFFh
	SA10	0	0	0	0	0	1	1	X	X	X	X	030000h to 03FFFFh	018000h to 01FFFFh
	SA11	0	0	0	0	1	0	0	X	X	X	X	040000h to 04FFFFh	020000h to 027FFFh
	SA12	0	0	0	0	1	0	1	X	X	X	X	050000h to 05FFFFh	028000h to 02FFFFh
	SA13	0	0	0	0	1	1	0	X	X	X	X	060000h to 06FFFFh	030000h to 037FFFh
	SA14	0	0	0	0	1	1	1	X	X	X	X	070000h to 07FFFFh	038000h to 03FFFFh
	SA15	0	0	1	0	0	0	0	X	X	X	X	080000h to 08FFFFh	040000h to 047FFFh
	SA16	0	0	1	0	0	0	1	X	X	X	X	090000h to 09FFFFh	048000h to 04FFFFh
	SA17	0	0	1	0	0	1	0	X	X	X	X	0A0000h to 0AFFFFh	050000h to 057FFFh
	SA18	0	0	1	0	0	1	1	X	X	X	X	0B0000h to 0BFFFFh	058000h to 05FFFFh
	SA19	0	0	1	1	0	0	0	X	X	X	X	0C0000h to 0CFFFFh	060000h to 067FFFh
	SA20	0	0	1	1	0	0	1	X	X	X	X	0D0000h to 0DFFFFh	068000h to 06FFFFh
	SA21	0	0	1	1	1	0	0	X	X	X	X	0E0000h to 0EFFFFh	070000h to 077FFFh
	SA22	0	0	1	1	1	1	1	X	X	X	X	0F0000h to 0FFFFFh	078000h to 07FFFFh
	SA23	0	1	0	0	0	0	0	X	X	X	X	100000h to 10FFFFh	080000h to 087FFFh
	SA24	0	1	0	0	0	0	1	X	X	X	X	110000h to 11FFFFh	088000h to 08FFFFh
	SA25	0	1	0	0	0	1	0	X	X	X	X	120000h to 12FFFFh	090000h to 097FFFh
	SA26	0	1	0	0	0	1	1	X	X	X	X	130000h to 13FFFFh	098000h to 09FFFFh
	SA27	0	1	0	0	0	0	0	X	X	X	X	140000h to 14FFFFh	0A0000h to 0A7FFFh
	SA28	0	1	0	0	0	1	0	X	X	X	X	150000h to 15FFFFh	0A8000h to 0AFFFFh
	SA29	0	1	0	0	1	0	0	X	X	X	X	160000h to 16FFFFh	0B0000h to 0B7FFFh
	SA30	0	1	0	0	1	1	1	X	X	X	X	170000h to 17FFFFh	0B8000h to 0BFFFFh
	SA31	0	1	1	0	0	0	0	X	X	X	X	180000h to 18FFFFh	0C0000h to 0C7FFFh
	SA32	0	1	1	0	0	0	1	X	X	X	X	190000h to 19FFFFh	0C8000h to 0CFFFFh
	SA33	0	1	1	0	0	1	0	X	X	X	X	1A0000h to 1AFFFFh	0D0000h to 0D7FFFh
SA34	0	1	1	0	0	1	1	X	X	X	X	1B0000h to 1BFFFFh	0D8000h to 0DFFFFh	

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(Continued)

Bank	Sector	Sector Address										Address Range (BYTE mode)	Address Range (WORD mode)
		Bank Address											
		A20	A19	A18	A17	A16	A15	A14	A13	A12	A11		
Bank 1	SA35	0	1	1	1	0	0	X	X	X	X	1C0000h to 1CFFFFh	0E0000h to 0E7FFFh
	SA36	0	1	1	1	0	1	X	X	X	X	1D0000h to 1DFFFFh	0E8000h to 0EFFFFh
	SA37	0	1	1	1	1	0	X	X	X	X	1E0000h to 1EFFFFh	0F0000h to 0F7FFFh
	SA38	0	1	1	1	1	1	X	X	X	X	1F0000h to 1FFFFFh	0F8000h to 0FFFFFh
Bank 2	SA39	1	0	0	0	0	0	X	X	X	X	200000h to 20FFFFh	100000h to 107FFFh
	SA40	1	0	0	0	0	1	X	X	X	X	210000h to 21FFFFh	108000h to 10FFFFh
	SA41	1	0	0	0	1	0	X	X	X	X	220000h to 22FFFFh	110000h to 117FFFh
	SA42	1	0	0	0	1	1	X	X	X	X	230000h to 23FFFFh	118000h to 11FFFFh
	SA43	1	0	0	1	0	0	X	X	X	X	240000h to 24FFFFh	120000h to 127FFFh
	SA44	1	0	0	1	0	1	X	X	X	X	250000h to 25FFFFh	128000h to 12FFFFh
	SA45	1	0	0	1	1	0	X	X	X	X	260000h to 26FFFFh	130000h to 137FFFh
	SA46	1	0	0	1	1	1	X	X	X	X	270000h to 27FFFFh	138000h to 13FFFFh
	SA47	1	0	1	0	0	0	X	X	X	X	280000h to 28FFFFh	140000h to 147FFFh
	SA48	1	0	1	0	0	1	X	X	X	X	290000h to 29FFFFh	148000h to 14FFFFh
	SA49	1	0	1	0	1	0	X	X	X	X	2A0000h to 2AFFFFh	150000h to 157FFFh
	SA50	1	0	1	0	1	1	X	X	X	X	2B0000h to 2BFFFFh	158000h to 15FFFFh
	SA51	1	0	1	1	0	0	X	X	X	X	2C0000h to 2CFFFFh	160000h to 167FFFh
	SA52	1	0	1	1	0	1	X	X	X	X	2D0000h to 2DFFFFh	168000h to 16FFFFh
	SA53	1	0	1	1	1	0	X	X	X	X	2E0000h to 2EFFFFh	170000h to 177FFFh
	SA54	1	0	1	1	1	1	X	X	X	X	2F0000h to 2FFFFFh	178000h to 17FFFFh
	SA55	1	1	0	0	0	0	X	X	X	X	300000h to 30FFFFh	180000h to 187FFFh
	SA56	1	1	0	0	0	1	X	X	X	X	310000h to 31FFFFh	188000h to 18FFFFh
	SA57	1	1	0	0	1	0	X	X	X	X	320000h to 32FFFFh	190000h to 197FFFh
	SA58	1	1	0	0	1	1	X	X	X	X	330000h to 33FFFFh	198000h to 19FFFFh
	SA59	1	1	0	1	0	0	X	X	X	X	340000h to 34FFFFh	1A0000h to 1A7FFFh
	SA60	1	1	0	1	0	1	X	X	X	X	350000h to 35FFFFh	1A8000h to 1AFFFFh
	SA61	1	1	0	1	1	0	X	X	X	X	360000h to 36FFFFh	1B0000h to 1B7FFFh
	SA62	1	1	0	1	1	1	X	X	X	X	370000h to 37FFFFh	1B8000h to 1BFFFFh
	SA63	1	1	1	0	0	0	X	X	X	X	380000h to 38FFFFh	1C0000h to 1C7FFFh
	SA64	1	1	1	0	0	1	X	X	X	X	390000h to 39FFFFh	1C8000h to 1CFFFFh
	SA65	1	1	1	0	1	0	X	X	X	X	3A0000h to 3AFFFFh	1D0000h to 1D7FFFh
	SA66	1	1	1	0	1	1	X	X	X	X	3B0000h to 3BFFFFh	1D8000h to 1DFFFFh
SA67	1	1	1	1	0	0	X	X	X	X	3C0000h to 3CFFFFh	1E0000h to 1E7FFFh	
SA68	1	1	1	1	0	1	X	X	X	X	3D0000h to 3DFFFFh	1E8000h to 1EFFFFh	
SA69	1	1	1	1	1	0	X	X	X	X	3E0000h to 3EFFFFh	1F0000h to 1F7FFFh	
SA70	1	1	1	1	1	1	X	X	X	X	3F0000h to 3FFFFFh	1F8000h to 1FFFFFh	

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**Table 3.1 Sector Group Address (MB84VD2218XEC/EE)
(Top Boot Block)**

Sector Group	A ₂₀	A ₁₉	A ₁₈	A ₁₇	A ₁₆	A ₁₅	A ₁₄	A ₁₃	A ₁₂	Sectors
SGA0	0	0	0	0	0	0	X	X	X	SA0
SGA1	0	0	0	0	0	1	X	X	X	SA1 to SA3
					1	0				
					1	1				
SGA2	0	0	0	1	X	X	X	X	X	SA4 to SA7
SGA3	0	0	1	0	X	X	X	X	X	SA8 to SA11
SGA4	0	0	1	1	X	X	X	X	X	SA12 to SA15
SGA5	0	1	0	0	X	X	X	X	X	SA16 to SA19
SGA6	0	1	0	1	X	X	X	X	X	SA20 to SA23
SGA7	0	1	1	0	X	X	X	X	X	SA24 to SA27
SGA8	0	1	1	1	X	X	X	X	X	SA28 to SA31
SGA9	1	0	0	0	X	X	X	X	X	SA32 to SA35
SGA10	1	0	0	1	X	X	X	X	X	SA36 to SA39
SGA11	1	0	1	0	X	X	X	X	X	SA40 to SA43
SGA12	1	0	1	1	X	X	X	X	X	SA44 to SA47
SGA13	1	1	0	0	X	X	X	X	X	SA48 to SA51
SGA14	1	1	0	1	X	X	X	X	X	SA52 to SA55
SGA15	1	1	1	0	X	X	X	X	X	SA56 to SA59
SGA16	1	1	1	1	0	0	X	X	X	SA60 to SA62
					0	1				
					1	0				
SGA17	1	1	1	1	1	1	0	0	0	SA63
SGA18	1	1	1	1	1	1	0	0	1	SA64
SGA19	1	1	1	1	1	1	0	1	0	SA65
SGA20	1	1	1	1	1	1	0	1	1	SA66
SGA21	1	1	1	1	1	1	1	0	0	SA67
SGA22	1	1	1	1	1	1	1	0	1	SA68
SGA23	1	1	1	1	1	1	1	1	0	SA69
SGA24	1	1	1	1	1	1	1	1	1	SA70

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**Table 3.2 Sector Group Address (MB84VD2219XEC/EE)
(Bottom Boot Block)**

Sector Group	A ₂₀	A ₁₉	A ₁₈	A ₁₇	A ₁₆	A ₁₅	A ₁₄	A ₁₃	A ₁₂	Sectors
SGA0	0	0	0	0	0	0	0	0	0	SA0
SGA1	0	0	0	0	0	0	0	0	1	SA1
SGA2	0	0	0	0	0	0	0	1	0	SA2
SGA3	0	0	0	0	0	0	0	1	1	SA3
SGA4	0	0	0	0	0	0	1	0	0	SA4
SGA5	0	0	0	0	0	0	1	0	1	SA5
SGA6	0	0	0	0	0	0	1	1	0	SA6
SGA7	0	0	0	0	0	0	1	1	1	SA7
SGA8	0	0	0	0	0	1	X	X	X	SA8 to SA10
					1	0				
					1	1				
SGA9	0	0	0	1	X	X	X	X	X	SA11 to SA14
SGA10	0	0	1	0	X	X	X	X	X	SA15 to SA18
SGA11	0	0	1	1	X	X	X	X	X	SA19 to SA22
SGA12	0	1	0	0	X	X	X	X	X	SA23 to SA26
SGA13	0	1	0	1	X	X	X	X	X	SA27 to SA30
SGA14	0	1	1	0	X	X	X	X	X	SA31 to SA34
SGA15	0	1	1	1	X	X	X	X	X	SA35 to SA38
SGA16	1	0	0	0	X	X	X	X	X	SA39 to SA42
SGA17	1	0	0	1	X	X	X	X	X	SA43 to SA46
SGA18	1	0	1	0	X	X	X	X	X	SA47 to SA50
SGA19	1	0	1	1	X	X	X	X	X	SA51 to SA54
SGA20	1	1	0	0	X	X	X	X	X	SA55 to SA58
SGA21	1	1	0	1	X	X	X	X	X	SA59 to SA62
SGA22	1	1	1	0	X	X	X	X	X	SA63 to SA66
SGA23	1	1	1	1	0	0	X	X	X	SA67 to SA69
					0	1				
					1	0				
SGA24	1	1	1	1	1	1	X	X	X	SA70

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Table 4 Flash Memory Autoselect Codes

Type		A ₁₂ to A ₁₉	A ₆	A ₁	A ₀	A ₋₁ *1	Code (HEX)	
Manufacturer's Code		X	V _{IL}	V _{IL}	V _{IL}	V _{IL}	04h	
Device Code	MB84VD22182EC MB84VD22182EE	Byte	X	V _{IL}	V _{IL}	V _{IH}	V _{IL}	55h
		Word					X	2255h
	MB84VD22192EC MB84VD22192EE	Byte	X	V _{IL}	V _{IL}	V _{IH}	V _{IL}	56h
		Word					X	2256h
	MB84VD22183EC MB84VD22183EE	Byte	X	V _{IL}	V _{IL}	V _{IH}	V _{IL}	50h
		Word					X	2250h
	MB84VD22193EC MB84VD22193EE	Byte	X	V _{IL}	V _{IL}	V _{IH}	V _{IL}	53h
		Word					X	2253h
	MB84VD22184EC MB84VD22184EE	Byte	X	V _{IL}	V _{IL}	V _{IH}	V _{IL}	5Ch
		Word					X	225Ch
	MB84VD22194EC MB84VD22194EE	Byte	X	V _{IL}	V _{IL}	V _{IH}	V _{IL}	5Fh
		Word					X	225Fh
	Sector Group protect		Sector Group Address	V _{IL}	V _{IH}	V _{IL}	V _{IL}	01h*2

*1: A₋₁ is for Byte mode.

*2: Output 01h at protected sector address and output 00h at unprotected sector address.

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Table 5 Flash Memory Command Definitions

Command Sequence	Bus Write Cycles Req'd	First Bus Write Cycle		Second Bus Write Cycle		Third Bus Write Cycle		Fourth Bus Read/Write Cycle		Fifth Bus Write Cycle		Sixth Bus Write Cycle		
		Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	
Read/Reset *1	1	XXXh	F0h	—	—	—	—	—	—	—	—	—	—	
Read/Reset*1	Word	3	555h	AAh	2AAh	55h	555h	F0h	RA	RD	—	—	—	—
	Byte		AAAh											
Autoselect	Word	3	555h	AAh	2AAh	55h	(BA) 555h	90h	—	—	—	—	—	—
	Byte		AAAh											
Program	Word	4	555h	AAh	2AAh	55h	555h	A0h	PA	PD	—	—	—	—
	Byte		AAAh											
Chip Erase	Word	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	555h	10h
	Byte		AAAh											
Sector Erase	Word	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	SA	30h
	Byte		AAAh											
Sector Erase Suspend	1	BA	B0h	—	—	—	—	—	—	—	—	—	—	
Sector Erase Resume	1	BA	30h	—	—	—	—	—	—	—	—	—	—	
Set to Fast Mode	Word	3	555h	AAh	2AAh	55h	555h	20h	—	—	—	—	—	—
	Byte		AAAh											
Fast Program *2	Word	2	XXXh	A0h	PA	PD	—	—	—	—	—	—	—	—
	Byte		—	—	—	—	—	—	—	—	—	—	—	—
Reset from Fast Mode*2	Word	2	BA	90h	XXXh	F0h*6	—	—	—	—	—	—	—	—
	Byte		—	—	—	—	—	—	—	—	—	—	—	—
Extended Sector Group Protection*3	Word	4	XXXh	60h	SPA	60h	SPA	40h	SPA	SD	—	—	—	—
	Byte		—	—	—	—	—	—	—	—	—	—	—	—
Query*4	Word	1	55h	98h	—	—	—	—	—	—	—	—	—	—
	Byte		AAh											
Hi-ROM Entry	Word	3	555h	AAh	2AAh	55h	555h	88h	—	—	—	—	—	—
	Byte		AAAh											
Hi-ROM Program*5	Word	4	555h	AAh	2AAh	55h	555h	A0h	PA	PD	—	—	—	—
	Byte		AAAh											
Hi-ROM Erase*5	Word	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	HRA	30h
	Byte		AAAh											
Hi-ROM Exit*5	Word	4	555h	AAh	2AAh	55h	(HRBA) 555h	90h	XXXh	00h	—	—	—	—
	Byte		AAAh											

*1 : Both Read/Reset commands are functionally equivalent, resetting the device to the read mode.

*2 : This command is valid while Fast Mode.

*3 : This command is valid while $\overline{\text{RESET}} = V_{\text{ID}}$.

*4 : The valid Address is A₀ to A₆.

*5 : This command is valid while Hi-ROM mode.

*6 : The data "00h" is also acceptable.

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Address bits A_{11} to $A_{20} = X = "H"$ or $"L"$ for all address commands except for Program Address (PA), Sector Address (SA), and Bank Address (BA).

Bus operations are defined in Table 2 "User Bus Operations".

RA = Address of the memory location to be read.

PA = Address of the memory location to be programmed.

Addresses are latched on the falling edge of the write pulse.

SA = Address of the sector to be erased. The combination of A_{20} , A_{19} , A_{18} , A_{17} , A_{16} , A_{15} , A_{14} , A_{13} , and A_{12} will uniquely select any sector.

BA = Bank address (A_{15} to A_{20})

SPA = Sector group address to be protected. Set sector group address (SGA) and $(A_6, A_1, A_0) = (0, 1, 0)$.

HRA = Address of the Hidden-ROM area.

MB84VD2218XEC/EE (Top Boot Type) Word mode: 1F8000h to 1FFFFFFh

Byte mode: 3F0000h to 3FFFFFFh

MB84VD2219XEC/EE (Bottom Boot Type) Word mode: 000000h to 007FFFh

Byte mode: 000000h to 00FFFFh

HRBA = Bank address of the Hidden-ROM area

MB84VD2218XEC/EE (Top Boot Type) : $A_{15} = A_{16} = A_{17} = A_{18} = A_{19} = A_{20} = 1$

MB84VD2219XEC/EE (Bottom Boot Type) : $A_{15} = A_{16} = A_{17} = A_{18} = A_{19} = A_{20} = 0$

RD = Data read from location RA during read operation.

PD = Data to be programmed at location PA.

SD = Sector protection verify data. Output 01h at protected sector addresses and output 00h at unprotected sector addresses.

The system should generate the following address patterns;

Word mode : 555h or 2AAh to addresses A_0 to A_{10}

Byte mode : AAh or 55h to addresses A_{-1} and A_0 to A_{10}

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■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min.	Max.	
Storage Temperature	T _{stg}	-55	+125	°C
Ambient Temperature with Power Applied	T _A	-25	+85	°C
Voltage with Respect to Ground All pins *1 except $\overline{\text{RESET}}$ and $\overline{\text{WP/ACC}}$	V _{IN} , V _{OUT}	-0.3	V _{ccf} +0.4	V
			V _{ccs} +0.4	V
V _{ccf} /V _{ccs} Supply *1	V _{ccf} , V _{ccs}	-0.3	+4.0	V
$\overline{\text{RESET}}$ *2	V _{IN}	-0.5	+ 13.0	V
$\overline{\text{WP/ACC}}$ *3	V _{IN}	-0.5	+10.5	V

*1 : Minimum DC voltage on input or I/O pins is -0.3 V. During voltage transitions, input or I/O pins may undershoot V_{SS} to -2.0 V for periods of up to 20 ns. Maximum DC voltage on input or I/O pins is V_{ccf} +0.4 V or V_{ccs} +0.4 V. During voltage transitions, input or I/O pins may overshoot to V_{ccf} +2.0 V or V_{ccs} +2.0 V for periods of up to 20 ns.

*2 : Minimum DC input voltage on $\overline{\text{RESET}}$ pin is -0.5 V. During voltage transitions, $\overline{\text{RESET}}$ pins may undershoot V_{SS} to -2.0 V for periods of up to 20 ns.
Voltage difference between input and supply voltage (V_{IN}-V_{ccf} or V_{ccs}) does not exceed 9.0 V.
Maximum DC input voltage on $\overline{\text{RESET}}$ pin is +13.0 V which may overshoot to 14.0 V for periods of up to 20 ns.

*3 : Minimum DC input voltage on $\overline{\text{WP/ACC}}$ pin is -0.5 V. During voltage transitions, $\overline{\text{WP/ACC}}$ pin may undershoot V_{SS} to -2.0 V for periods of up to 20 ns. Maximum DC input voltage on $\overline{\text{WP/ACC}}$ pin is +10.5 V which may overshoot to 12.0 V for periods of up to 20 ns, when V_{ccf} is applied.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value		Unit
		Min.	Max.	
Ambient Temperature	T _A	-25	+85	°C
V _{ccf} /V _{ccs} Supply Voltages	V _{ccf} , V _{ccs}	+2.7	+3.3	V

Note: Operating ranges define those limits between which the functionality of the device is guaranteed.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

Parameter	Symbol	Test Conditions	Value			Unit		
			Min.	Typ.	Max.			
Input Leakage Current	I_{LI}	$V_{IN} = V_{SS}$ to V_{CCf} , V_{CCS}	-1.0	—	+1.0	μA		
Output Leakage Current	I_{LO}	$V_{OUT} = V_{SS}$ to V_{CCf} , V_{CCS}	-1.0	—	+1.0	μA		
RESET Inputs Leakage Current	I_{LIT}	$V_{CCf} = V_{CCf}$ Max., $V_{CCS} = V_{CCS}$ Max, $\overline{RESET} = 12.5V$	—	—	35	μA		
ACC Input Leakage Current	I_{LIA}	$V_{CCf} = V_{CCf}$ Max., $V_{CCS} = V_{CCS}$ Max, $WP/ACC = V_{ACC}$ Max	—	—	20	mA		
Flash V_{CC} Active Current (Read)* ¹	I_{CC1f}	$\overline{CEf} = V_{IL}$, $\overline{OE} = V_{IH}$	$t_{CYCLE} = 5$ MHz	Byte	—	—	16	mA
			$t_{CYCLE} = 5$ MHz	Word	—	—	18	
			$t_{CYCLE} = 1$ MHz	Byte	—	—	7	mA
			$t_{CYCLE} = 1$ MHz	Word	—	—	7	
Flash V_{CC} Active Current (Program / Erase) * ²	I_{CC2f}	$\overline{CEf} = V_{IL}$, $\overline{OE} = V_{IH}$	—	—	35	mA		
Flash V_{CC} Active Current (Read-While-Program)* ⁵	I_{CC3f}	$\overline{CEf} = V_{IL}$, $\overline{OE} = V_{IH}$	Byte	—	—	51	mA	
			Word	—	—	53		
Flash V_{CC} Active Current (Read-While-Erase)* ⁵	I_{CC4f}	$\overline{CEf} = V_{IL}$, $\overline{OE} = V_{IH}$	Byte	—	—	51	mA	
			Word	—	—	53		
Flash V_{CC} Active Current (Erase-Suspend-Program)	I_{CC5f}	$\overline{CEf} = V_{IL}$, $\overline{OE} = V_{IH}$	—	—	35	mA		
SRAM V_{CC} Active Current	I_{CC1S}	$V_{CCS} = V_{CC}$ Max., $\overline{CE1s} = V_{IL}$, $\overline{CE2s} = V_{IH}$	$t_{CYCLE} = 10$ MHz		—	—	50	mA
SRAM V_{CC} Active Current	I_{CC2S}	$\overline{CE1s} = 0.2$ V, $\overline{CE2s} = V_{CCS} - 0.2$ V,	$t_{CYCLE} = 10$ MHz		—	—	50	mA
			$t_{CYCLE} = 1$ MHz		—	—	8	mA
Flash V_{CC} Standby Current	I_{SB1f}	$V_{CCf} = V_{CC}$ Max., $\overline{CEf} = V_{CCf} \pm 0.3$ V $\overline{RESET} = V_{CCf} \pm 0.3$ V, $WP/ACC = V_{CCf} \pm 0.3$ V	—	1	5	μA		
Flash V_{CC} Standby Current (RESET)	I_{SB2f}	$V_{CCf} = V_{CC}$ Max., $\overline{RESET} = V_{SS} \pm 0.3$ V, $WP/ACC = V_{CCf} \pm 0.3$ V	—	1	5	μA		
Flash V_{CC} Current (Automatic Sleep Mode)* ³	I_{SB3f}	$V_{CCf} = V_{CC}$ Max., $\overline{CEf} = V_{SS} \pm 0.3$ V $\overline{RESET} = V_{CCf} \pm 0.3$ V, $WP/ACC = V_{CCf} \pm 0.3$ V $V_{IN} = V_{CCf} \pm 0.3$ V or $V_{SS} \pm 0.3$ V	—	1	5	μA		
SRAM V_{CC} Standby Current	I_{SB1S}	$\overline{CE1s} \geq V_{CCS} - 0.2$ V, $\overline{CE2s} \geq V_{CCS} - 0.2$ V	—	—	15	μA		
SRAM V_{CC} Standby Current	I_{SB2S}	$\overline{CE2s} \leq 0.2$ V	—	—	15	μA		

(Continued)

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(Continued)

Parameter	Symbol	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
Input Low Level	V _{IL}	—	-0.3	—	0.5	V
Input High Level	V _{IH}	—	2.4	—	V _{CC} +0.3 ^{*6}	V
Voltage for Sector Protection, and Temporary Sector Unprotection (RESET) ^{*4}	V _{ID}	—	11.5	—	12.5	V
Voltage for Program Acceleration (WP/ACC) ^{*4}	V _{ACC}	—	8.5	9.0	9.5	V
Output Low Voltage Level	V _{OL}	V _{ccf} = V _{ccf} Min., V _{ccs} = V _{ccs} Min., I _{OL} =1.0 mA	—	—	0.4	V
Output High Voltage Level	V _{OH}	V _{ccf} = V _{ccf} Min., V _{ccs} = V _{ccs} Min., I _{OH} =-0.5 mA	2.4	—	—	V
Flash Low V _{ccf} Lock-Out Voltage	V _{LKO}	—	2.3	—	2.5	V

*1 : The I_{cc} current listed includes both the DC operating current and the frequency dependent component.

*2 : I_{cc} active while Embedded Algorithm (program or erase) is in progress.

*3 : Automatic sleep mode enables the low power mode when address remain stable for 150 ns.

*4 : Applicable for only V_{ccf} applying.

*5 : Embedded Alogorithm (program or erase) is in progress. (@5 MHz)

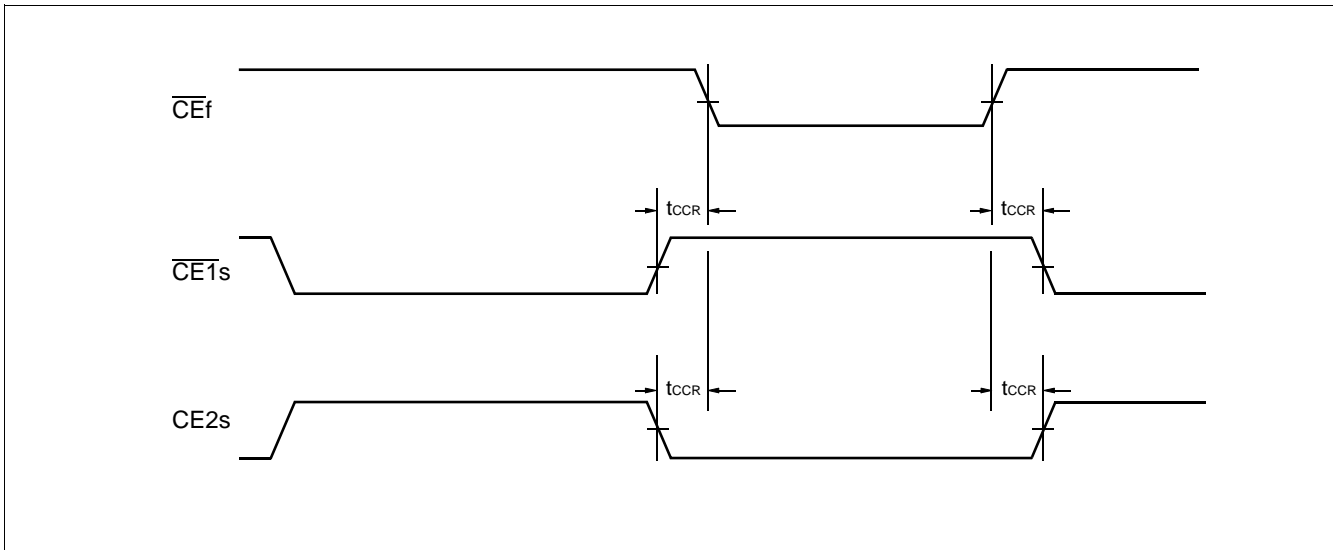
*6 : V_{CC} indicates lower of V_{ccf} or V_{ccs}

2. AC Characteristics

• \overline{CE} Timing

Parameter	Symbol		Test Setup	Value	Unit
	JEDEC	Standard		Min.	
\overline{CE} Recover Time	—	t_{CCR}	—	0	ns

• Timing Diagram for alternating SRAM to Flash



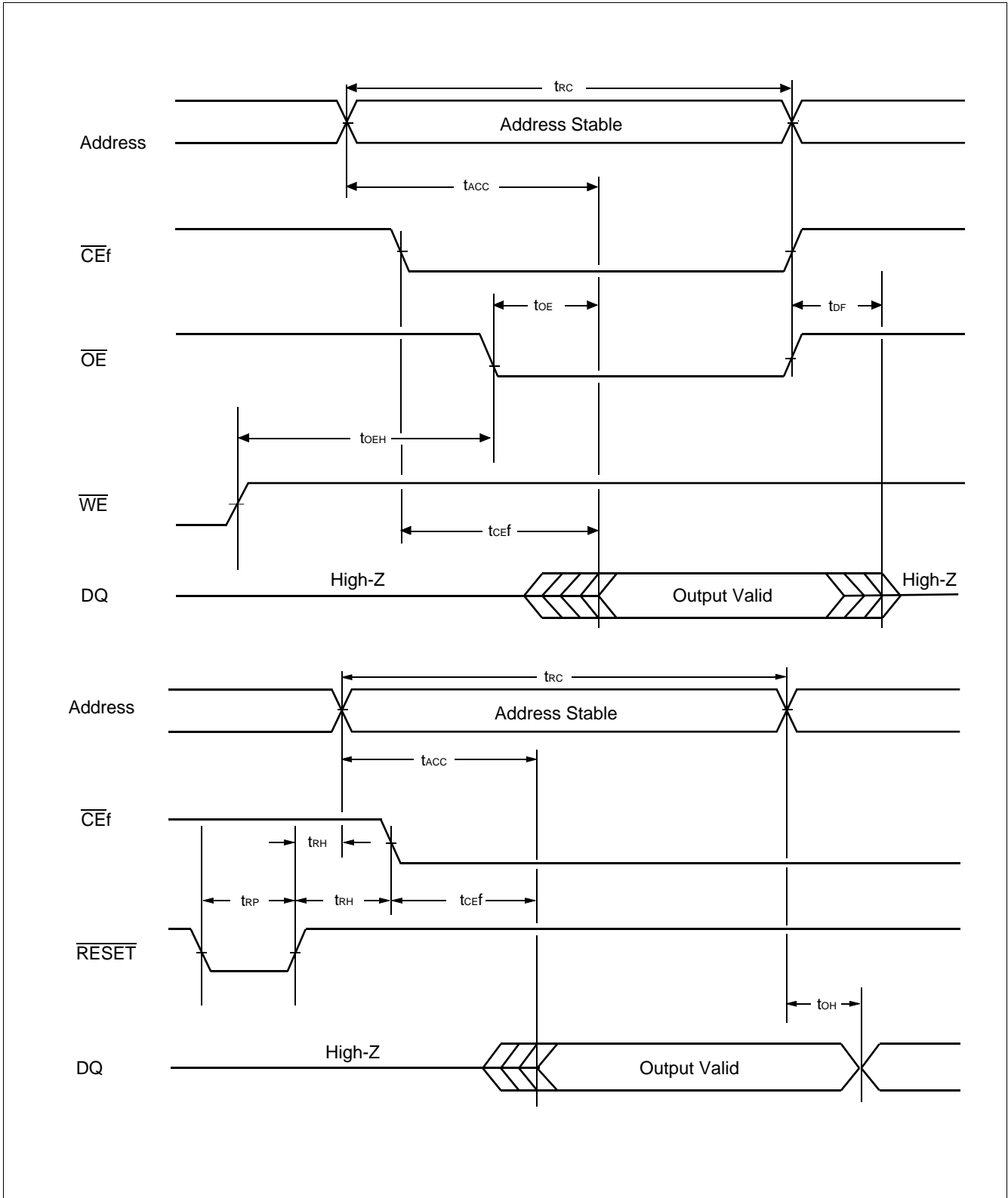
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• Read Only Operations Characteristics (Flash)

Parameter	Symbol		Test Setup	Value (Note)		Unit
	JEDEC	Standard		Min.	Max.	
Read Cycle Time	t_{AVAV}	t_{RC}	—	90	—	ns
Address to Output Delay	t_{AVQV}	t_{ACC}	$\overline{CE}f = V_{IL}$ $\overline{OE} = V_{IL}$	—	90	ns
Chip Enable to Output Delay	t_{ELQV}	t_{cef}	$\overline{OE} = V_{IL}$	—	90	ns
Output Enable to Output Delay	t_{GLQV}	t_{OE}	—	—	40	ns
Chip Enable to Output High-Z	t_{EHQZ}	t_{DF}	—	—	30	ns
Output Enable to Output High-Z	t_{GHQZ}	t_{DF}	—	—	30	ns
Output Hold Time From Addresses, $\overline{CE}f$ or \overline{OE} , Whichever Occurs First	t_{AXQX}	t_{OH}	—	0	—	ns
\overline{RESET} Pin Low to Read Mode	—	t_{READY}	—	—	20	μs

Note: Test Conditions—Output Load: 1 TTL gate and 30 pF
 Input rise and fall times: 5 ns
 Input pulse levels: 0.0 V to 3.0 V
 Timing measurement reference level
 Input: 1.5 V
 Output: 1.5 V

• Read Cycle (Flash)



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• Erase/Program Operations (Flash)

Parameter	Symbol		Value			Unit
	JEDEC	Standard	Min.	Typ.	Max.	
Write Cycle Time	t _{AVAV}	t _{WC}	90	—	—	ns
Address Setup Time (\overline{WE} to Addr.)	t _{AVWL}	t _{AS}	0	—	—	ns
Address Setup Time to \overline{CEf} Low During Toggle Bit Polling	—	t _{ASO}	15	—	—	ns
Address Hold Time (\overline{WE} to Addr.)	t _{WLAX}	t _{AH}	45	—	—	ns
Address Hold Time from \overline{CE} or \overline{OE} High During Toggle Bit Polling	—	t _{AHT}	0	—	—	ns
Data Setup Time	t _{DVWH}	t _{DS}	35	—	—	ns
Data Hold Time	t _{WDHX}	t _{DH}	0	—	—	ns
Output Enable Setup Time	—	t _{OES}	0	—	—	ns
Output Enable Hold Time	Read	t _{OEH}	0	—	—	ns
	Toggle and Data Polling		10	—	—	ns
\overline{CEf} High During Toggle Bit Polling	—	t _{CEPH}	20	—	—	ns
\overline{OE} High During Toggle Bit Polling	—	t _{OEPH}	20	—	—	ns
Read Recover Time Before Write (\overline{OE} to \overline{CEf})	t _{GHEL}	t _{GHEL}	0	—	—	ns
Read Recover Time Before Write (\overline{OE} to \overline{WE})	t _{GHWL}	t _{GHWL}	0	—	—	ns
\overline{WE} Setup Time (\overline{CEf} to \overline{WE})	t _{WLEL}	t _{WS}	0	—	—	ns
\overline{CEf} Setup Time (\overline{WE} to \overline{CEf})	t _{ELWL}	t _{CS}	0	—	—	ns
\overline{WE} Hold Time (\overline{CEf} to \overline{WE})	t _{EHWH}	t _{WH}	0	—	—	ns
\overline{CEf} Hold Time (\overline{WE} to \overline{CEf})	t _{WHEH}	t _{CH}	0	—	—	ns
Write Pulse Width	t _{WLWH}	t _{WP}	35	—	—	ns
\overline{CEf} Pulse Width	t _{ELEH}	t _{CP}	35	—	—	ns
Write Pulse Width High	t _{WHWL}	t _{WPH}	30	—	—	ns
\overline{CEf} Pulse Width High	t _{EHEL}	t _{CPH}	30	—	—	ns
Byte Programming Operation	t _{WHWH1}	t _{WHWH1}	—	8	—	μs
Word Programming Operation			—	16	—	μs
Sector Erase Operation *1	t _{WHWH2}	t _{WHWH2}	—	1	—	s

(Continued)

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(Continued)

Parameter	Symbol		Value			Unit
	JEDEC	Standard	Min.	Typ.	Max.	
V _{ccf} Setup Time	—	t _{VCS}	50	—	—	μs
Voltage Transition Time *2	—	t _{VLHT}	4	—	—	μs
Rise Time to V _D *2	—	t _{VIDR}	500	—	—	ns
Rise Time to V _{ACC}	—	t _{VACCR}	500	—	—	ns
Recover Time from RY/ $\overline{\text{BY}}$	—	t _{RB}	0	—	—	ns
$\overline{\text{RESET}}$ Pulse Width	—	t _{RP}	500	—	—	ns
Delay Time from Embedded Output Enable	—	t _{EOE}	—	—	90	ns
$\overline{\text{RESET}}$ High Level Period Before Read	—	t _{RH}	200	—	—	ns
Program/Erase Valid to RY/ $\overline{\text{BY}}$ Delay	—	t _{BUSY}	—	—	90	ns
Erase Time-out Time *3	—	t _{TOW}	50	—	—	μs
Erase Suspend Transition Time *4	—	t _{SPD}	—	—	20	μs

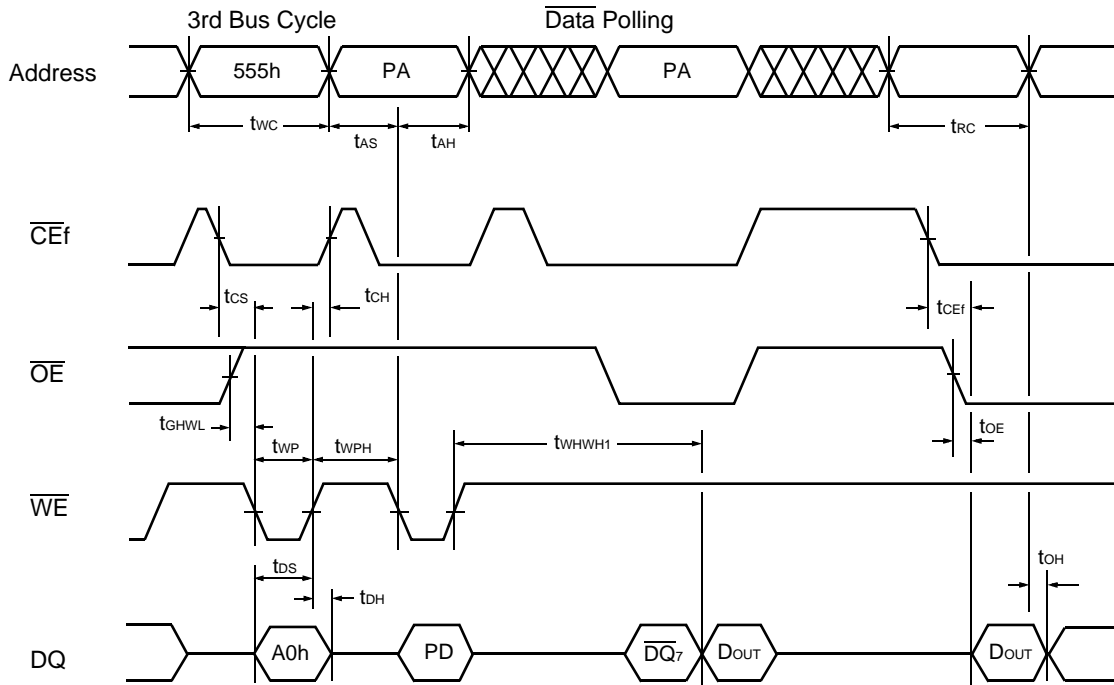
*1 : This does not include the preprogramming time.

*2 : This timing is for Sector Protection Operation.

*3 : The time between writes must be less than “t_{TOW}” otherwise that command will not be accepted and erasure will start. A time-out or “t_{TOW}” from the rising edge of last $\overline{\text{CE}}$ or $\overline{\text{WE}}$ whichever happens first will initiate the execution of the Sector Erase command(s).

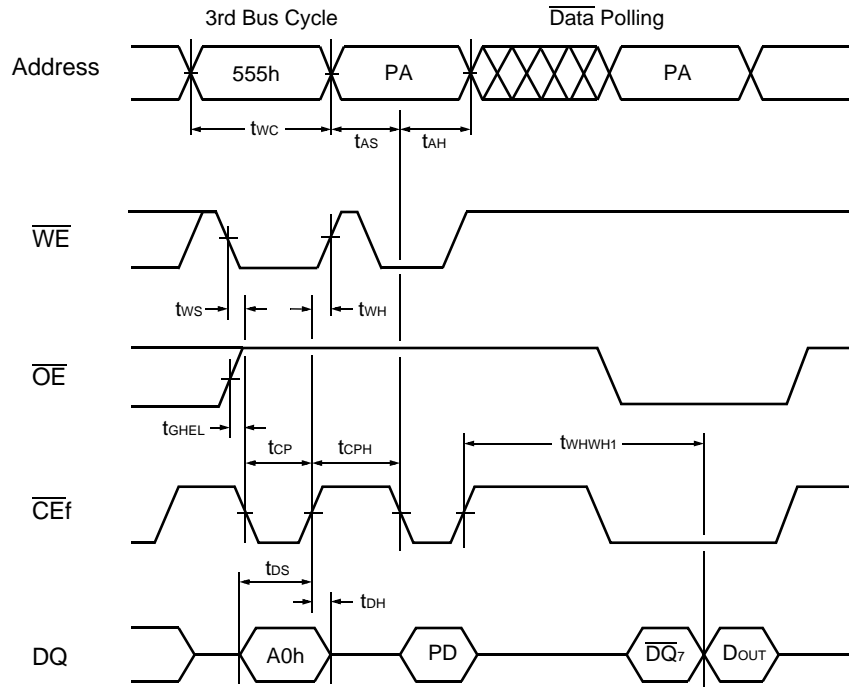
*4 : When the Erase Suspend command is written during the Sector Erase operation, the device will take a maximum of “t_{SPD}” to suspend the erase operation.

• Write Cycle (\overline{WE} control) (Flash)



- Notes:
1. PA is address of the memory location to be programmed.
 2. PD is data to be programmed at byte address.
 3. \overline{DQ}_7 is the output of the complement of the data written to the device.
 4. D_{OUT} is the output of the data written to the device.
 5. Figure indicates last two bus cycles out of four bus cycle sequence.
 6. These waveforms are for the x16 mode. (The addresses differ from x8 mode.)

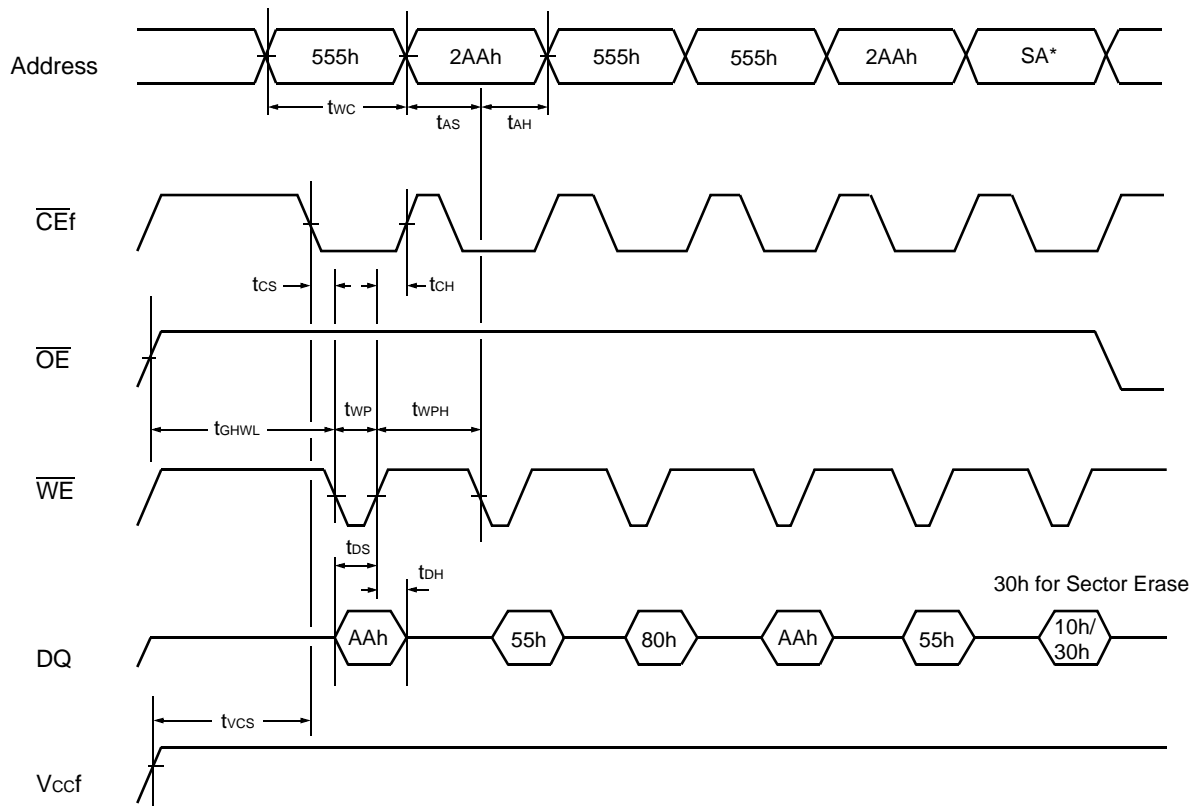
• Write Cycle ($\overline{\text{CEf}}$ control) (Flash)



- Notes:
1. PA is address of the memory location to be programmed.
 2. PD is data to be programmed at byte address.
 3. $\overline{\text{DQ}}_7$ is the output of the complement of the data written to the device.
 4. D_{OUT} is the output of the data written to the device.
 5. Figure indicates last two bus cycles out of four bus cycle sequence.
 6. These waveforms are for the x16 mode. (The addresses differ from x8 mode.)

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• AC Waveforms Chip/Sector Erase Operations (Flash)

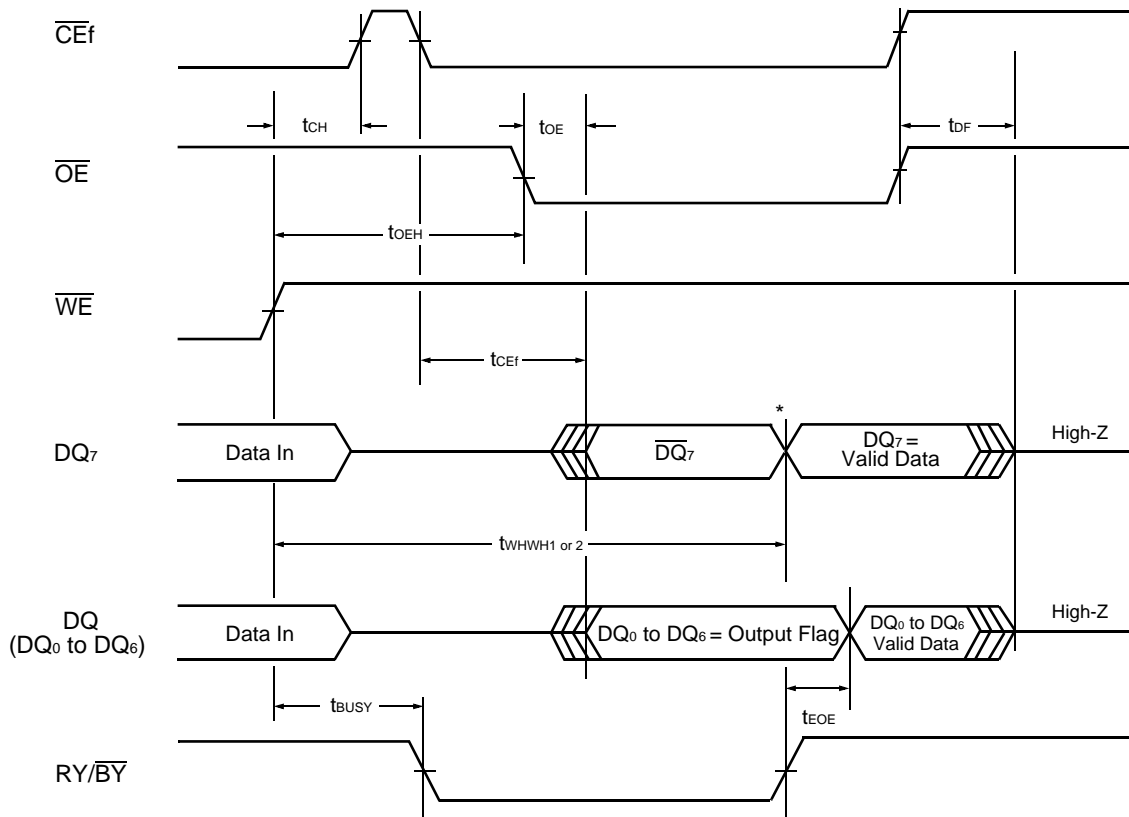


*: SA is the sector address for Sector Erase. Address = 555h for Chip Erase.

Note: These waveform are for the $\times 16$ mode. (The addresses differ from $\times 8$ mode.)

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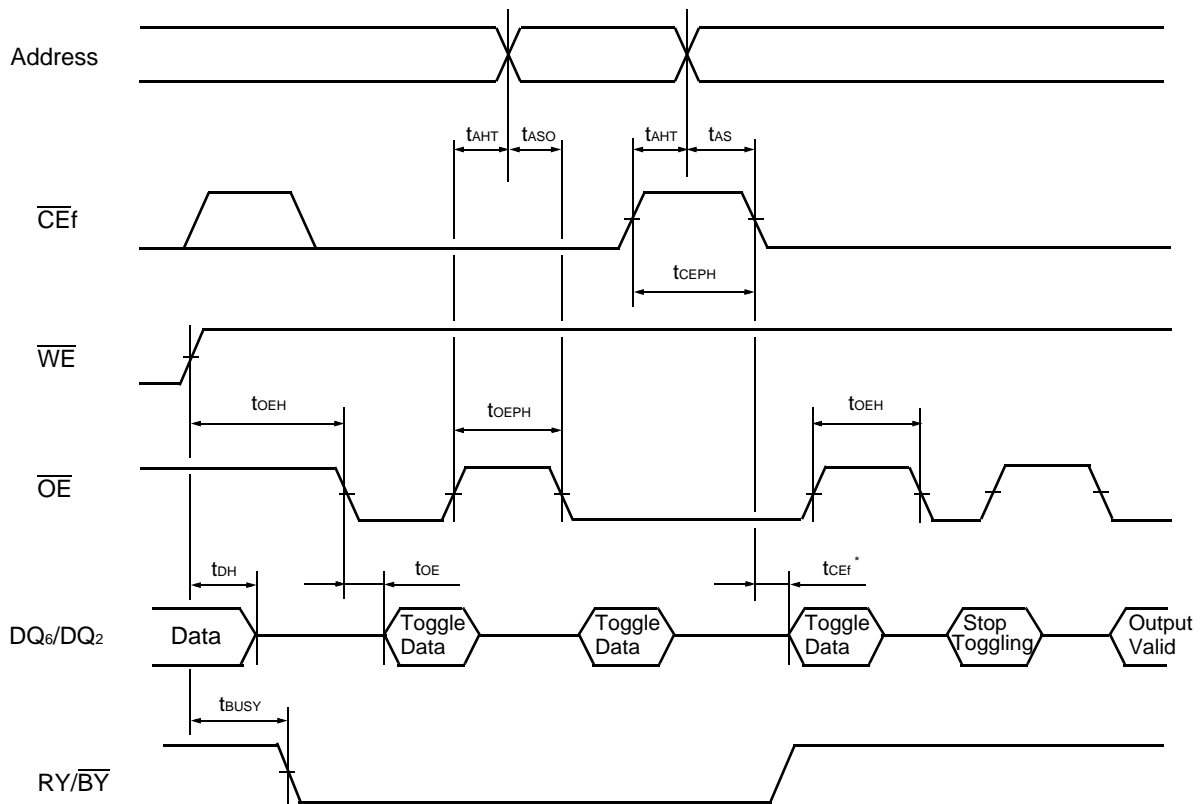
• AC Waveforms for $\overline{\text{Data Polling}}$ during Embedded Algorithm Operations (Flash)



*: DQ_7 = Valid Data (The device has completed the Embedded operation.)

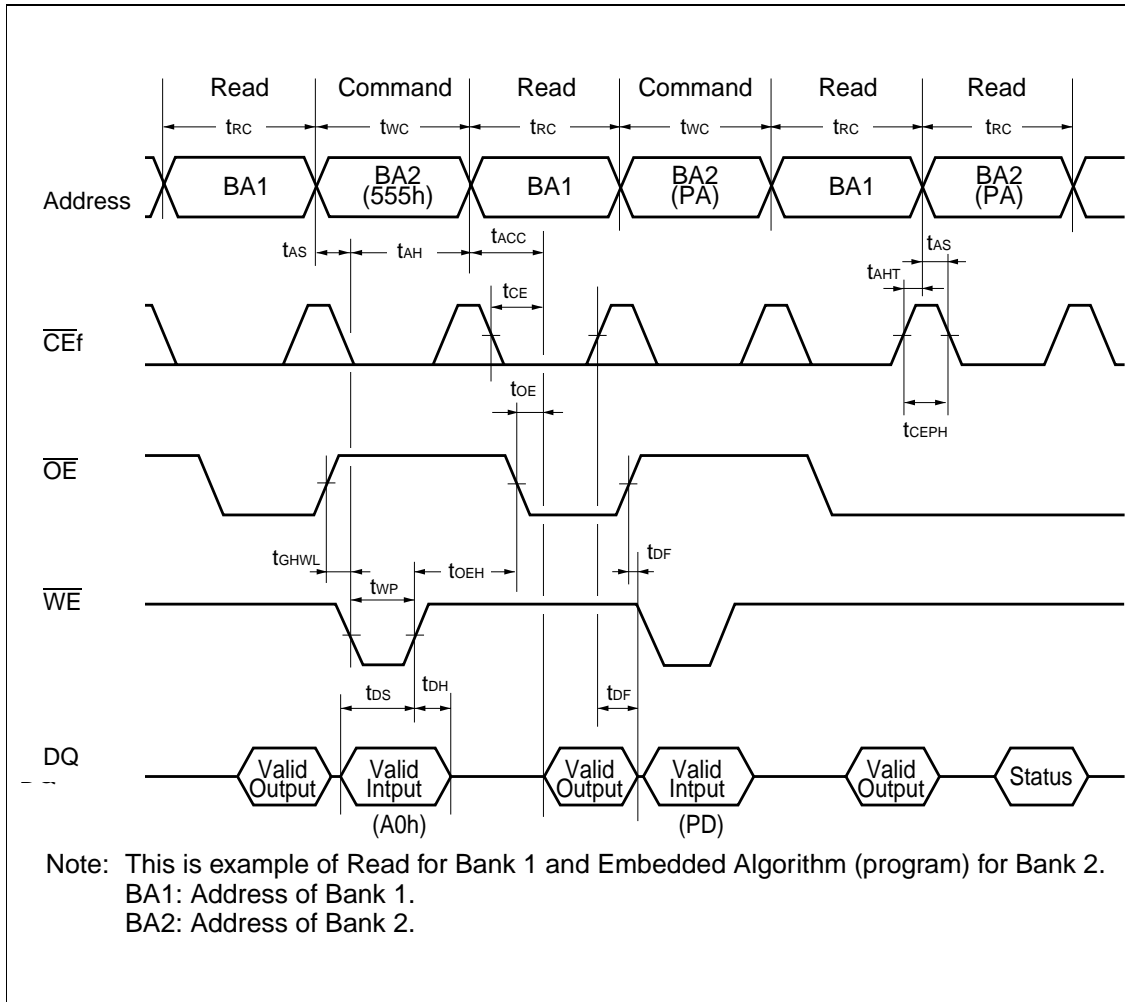
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• AC Waveforms for Toggle Bit during Embedded Algorithm Operations (Flash)

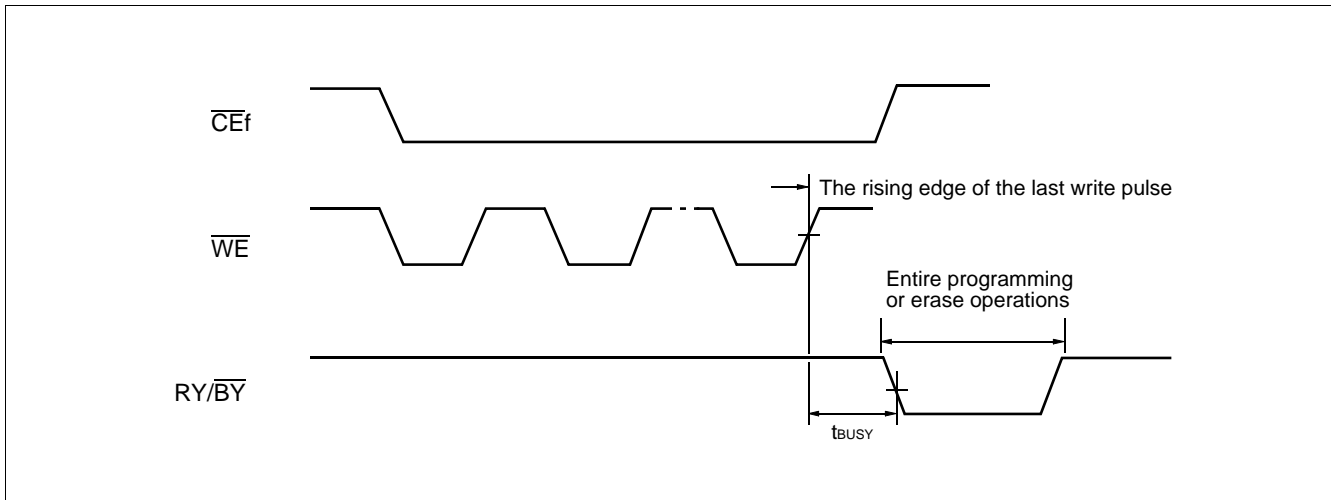


* : DQ₆ stops toggling (The device has completed the Embedded operation).

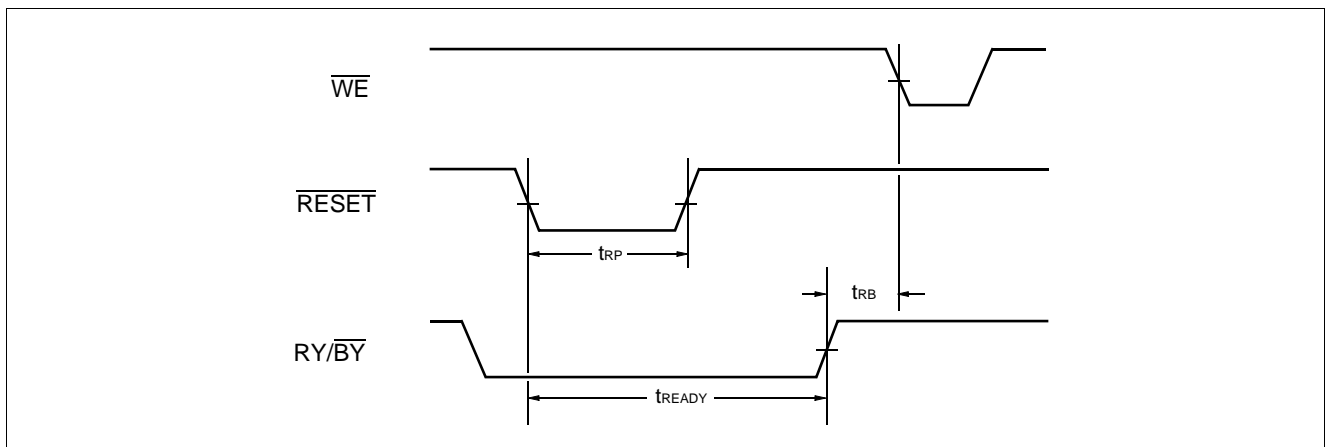
• Back-to-back Read/Write Timing Diagram (Flash)



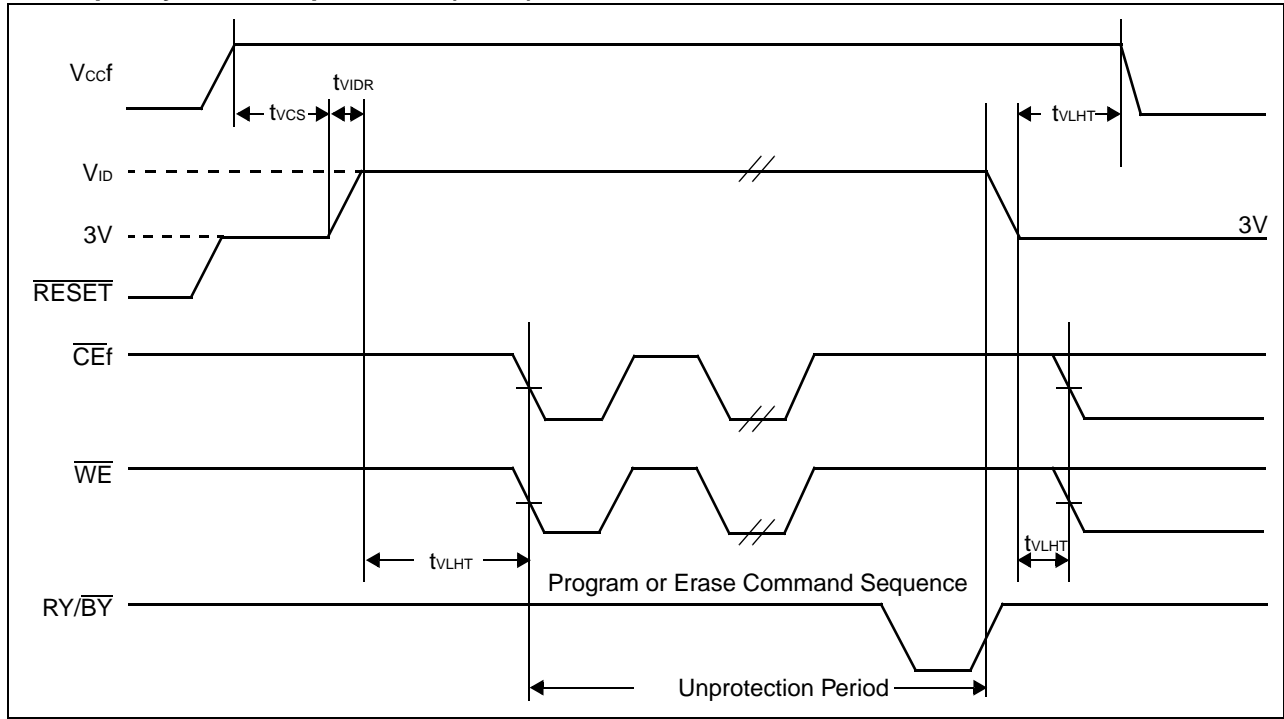
- RY/ $\overline{\text{BY}}$ Timing Diagram during Write/Erase Operations (Flash)



- $\overline{\text{RESET}}$, $\text{RY}/\overline{\text{BY}}$ Timing Diagram (Flash)

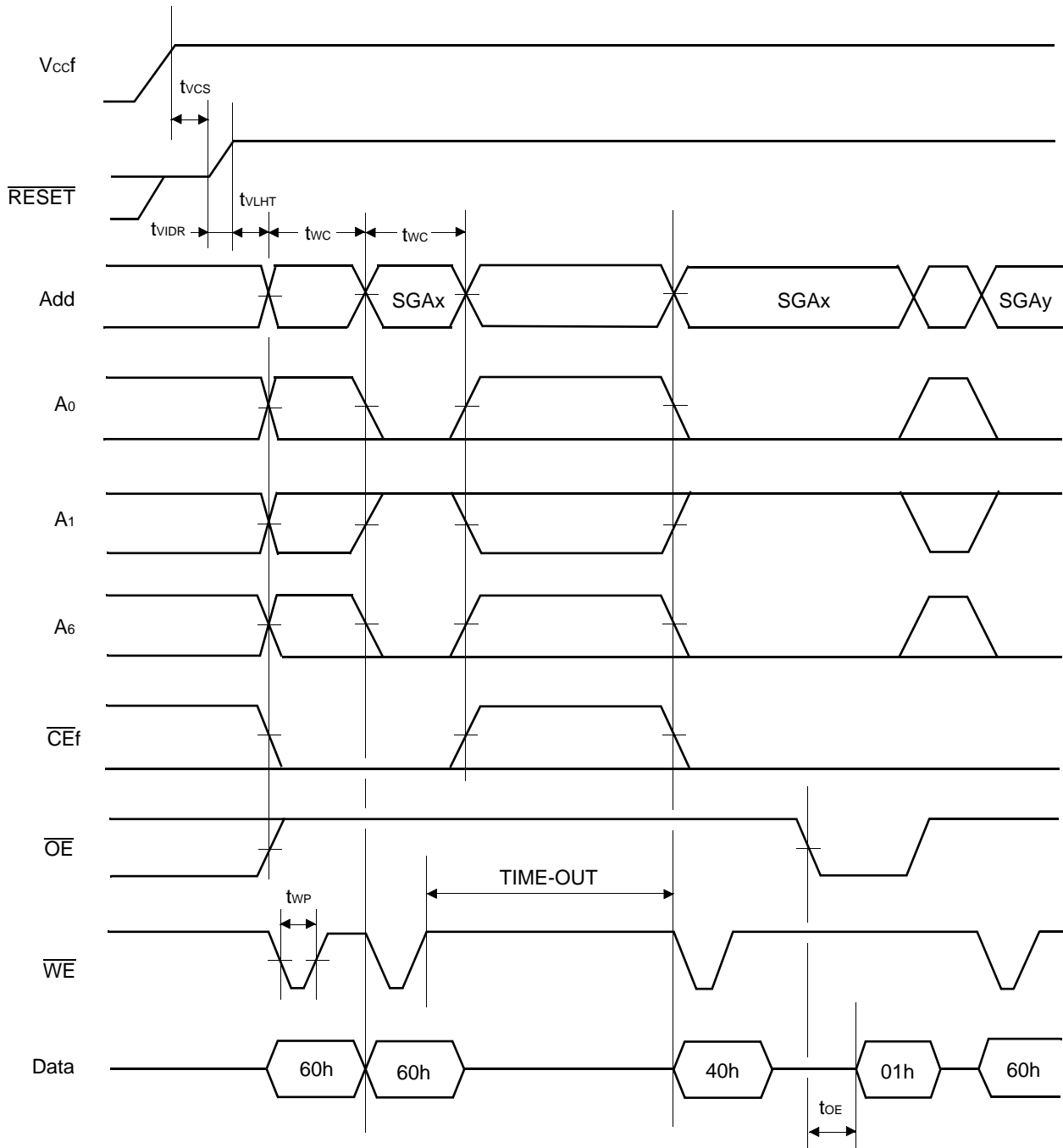


• Temporary Sector Unprotection (Flash)



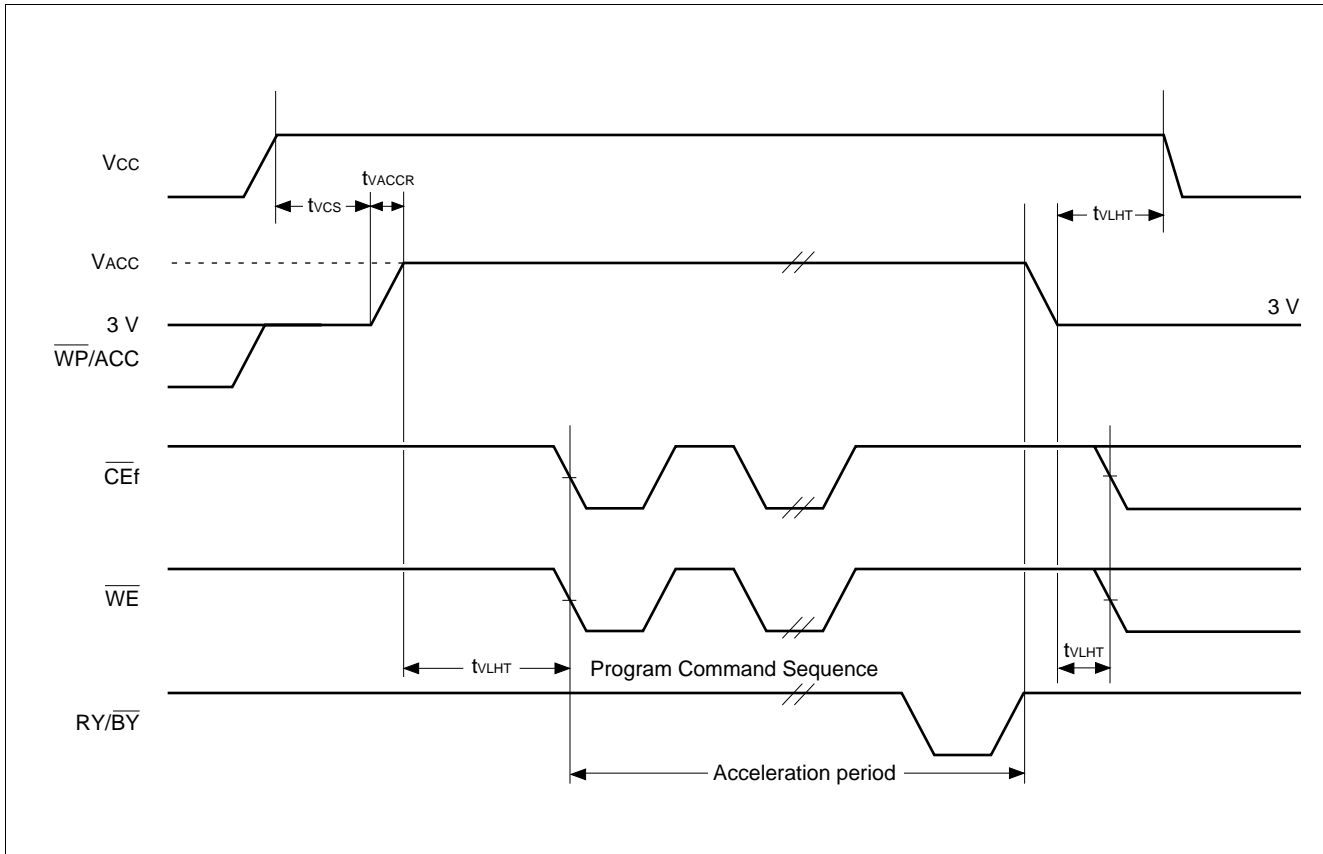
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• Extended Sector Protection (Flash)



SGAx: Sector Group Address to be protected
 SGAY : Next Group Sector Address to be protected
 TIME-OUT : Time-Out window = 250 μs (Min.)

• Accelerated Program (Flash)



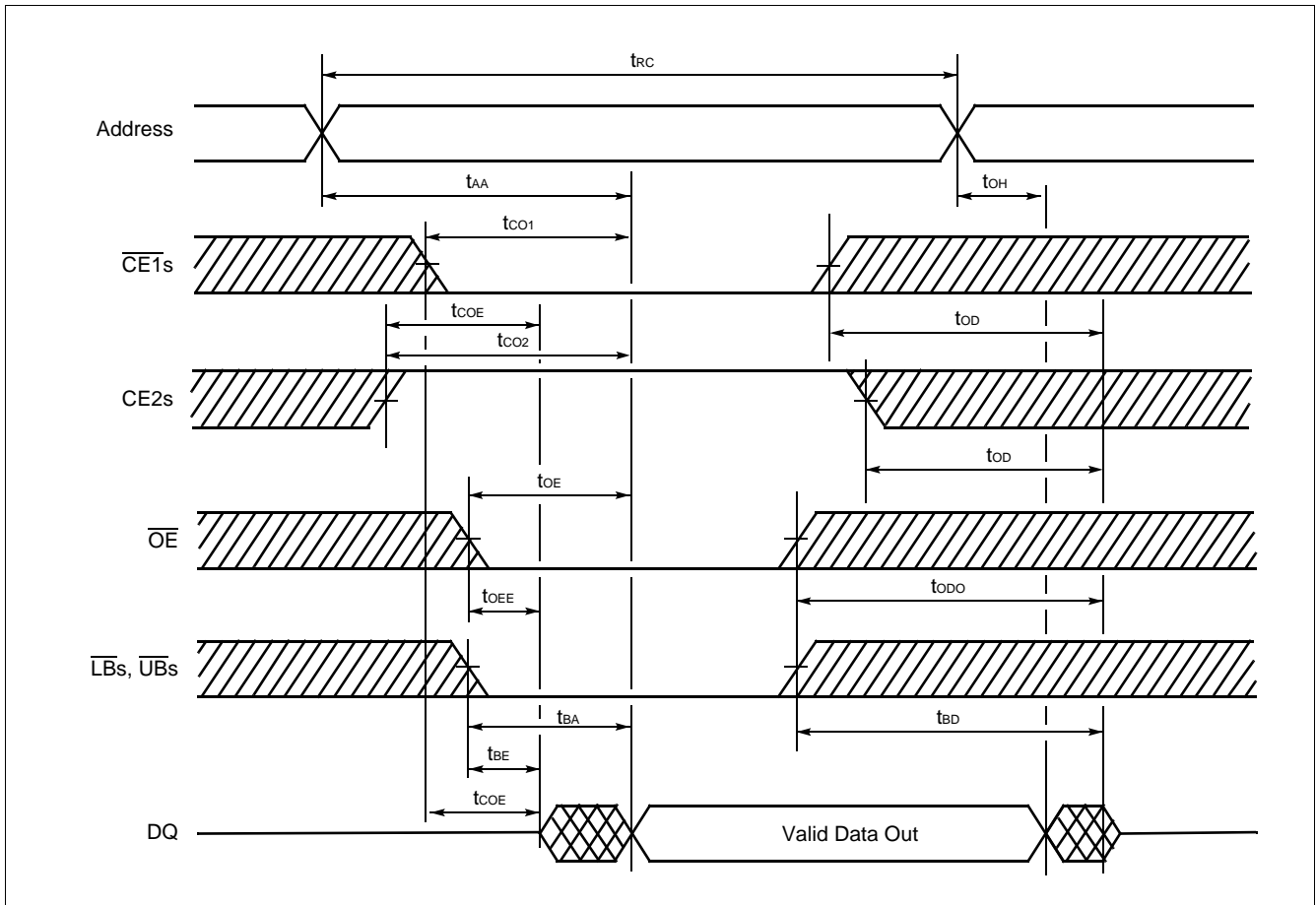
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• Read Cycle (SRAM)

Parameter	Symbol	Value		Unit
		Min.	Max.	
Read Cycle Time	t_{RC}	85	—	ns
Address Access Time	t_{AA}	—	85	ns
Chip Enable ($\overline{CE1}$ s) Access Time	t_{CO1}	—	85	ns
Chip Enable (CE2s) Access Time	t_{CO2}	—	85	ns
Output Enable Access Time	t_{OE}	—	45	ns
\overline{LB} s, \overline{UB} s to Output Valid	t_{BA}	—	85	ns
Chip Enable ($\overline{CE1}$ s Low and CE2s High) to Output Active	t_{COE}	5	—	ns
Output Enable Low to Output Active	t_{OEE}	0	—	ns
\overline{LB} s, \overline{UB} s Enable Low to Output Active	t_{BE}	0	—	ns
Chip Enable ($\overline{CE1}$ s High or CE2s Low) to Output High-Z	t_{OD}	—	35	ns
Output Enable High to Output High-Z	t_{ODO}	—	35	ns
\overline{LB} s, \overline{UB} s Output Enable to Output High-Z	t_{BD}	—	35	ns
Output Data Hold Time	t_{OH}	10	—	ns

Note : Test Conditions — Out put load : 1TTL gate and 30 pF
 Input rise and fall times : 5 ns
 Input pulse levels : 0.0 V to V_{CCS}
 Timing measurement reference level
 Input : $0.5 \times V_{CCS}$
 Output : $0.5 \times V_{CCS}$

• Read Cycle (Note 1) (SRAM)

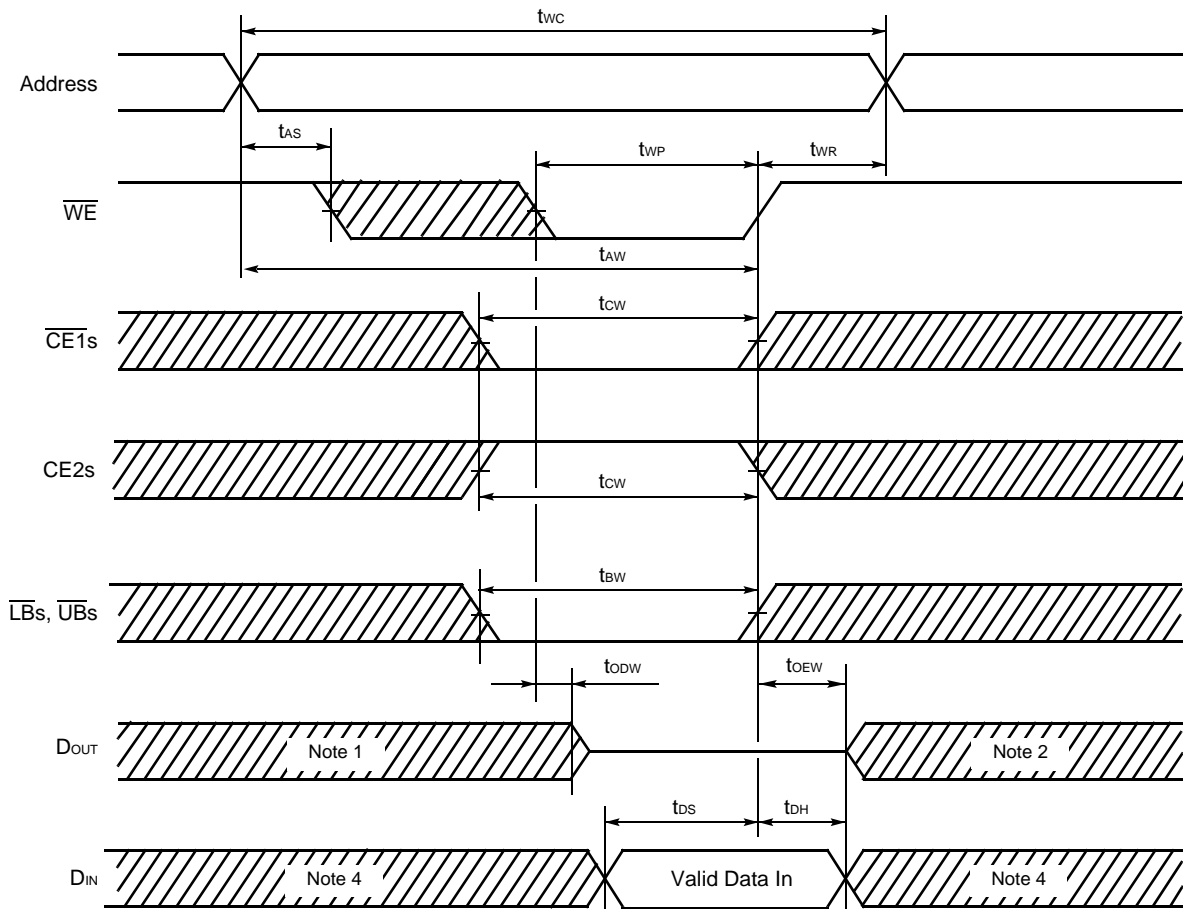


Note : \overline{WE} remains "H" for the read cycle.

• Write Cycle (SRAM)

Parameter	Symbol	Value		Unit
		Min.	Max.	
Write Cycle Time	t _{WC}	85	—	ns
Write Pulse Width	t _{WP}	60	—	ns
Chip Enable to End of Write	t _{CW}	70	—	ns
Address valid to End of Write	t _{AW}	70	—	ns
\overline{UB} s, \overline{LB} s to End of Write	t _{BW}	70	—	ns
Address Setup Time	t _{AS}	0	—	ns
Write Recovery Time	t _{WR}	0	—	ns
\overline{WE} Low to Output High-Z	t _{ODW}	—	35	ns
\overline{WE} High to Output Active	t _{OEW}	0	—	ns
Data Setup Time	t _{DS}	35	—	ns
Data Hold Time	t _{DH}	0	—	ns

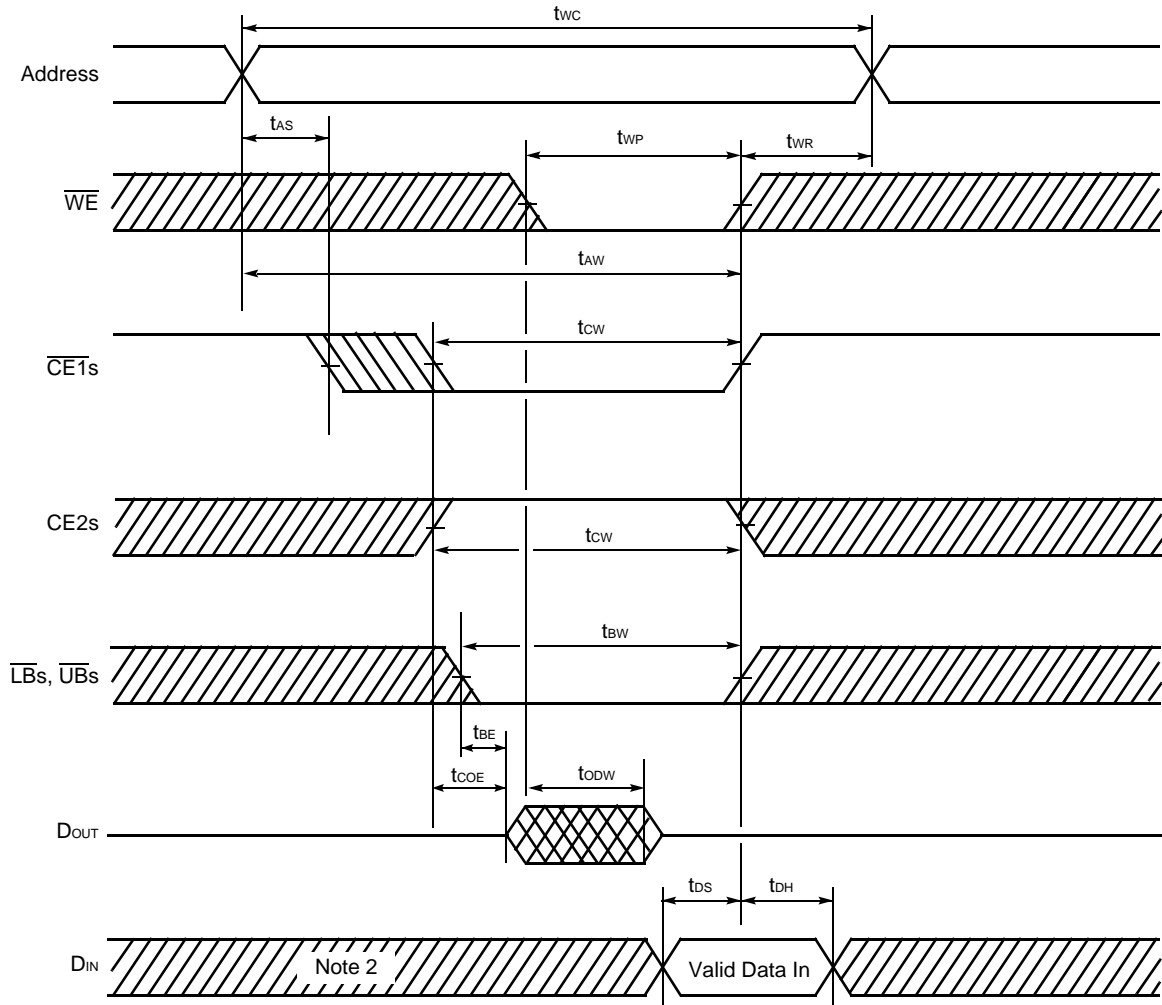
• Write Cycle(Note 3) (\overline{WE} control) (SRAM)



- Notes:
- 1.If $\overline{CE1s}$ goes "L" (or $\overline{CE2s}$ goes "H") coincident with or after \overline{WE} goes "L", the output will remain at High-Z.
 - 2.If $\overline{CE1s}$ goes "H" (or $\overline{CE2s}$ goes "L") coincident with or before \overline{WE} goes "H", the output will remain at High-Z.
 - 3.If \overline{OE} is "H" during the write cycle, the outputs will remain at High-Z.
 - 4.Because I/O signals may be in the output state at this Time, input signals of reverse polarity must not be applied.

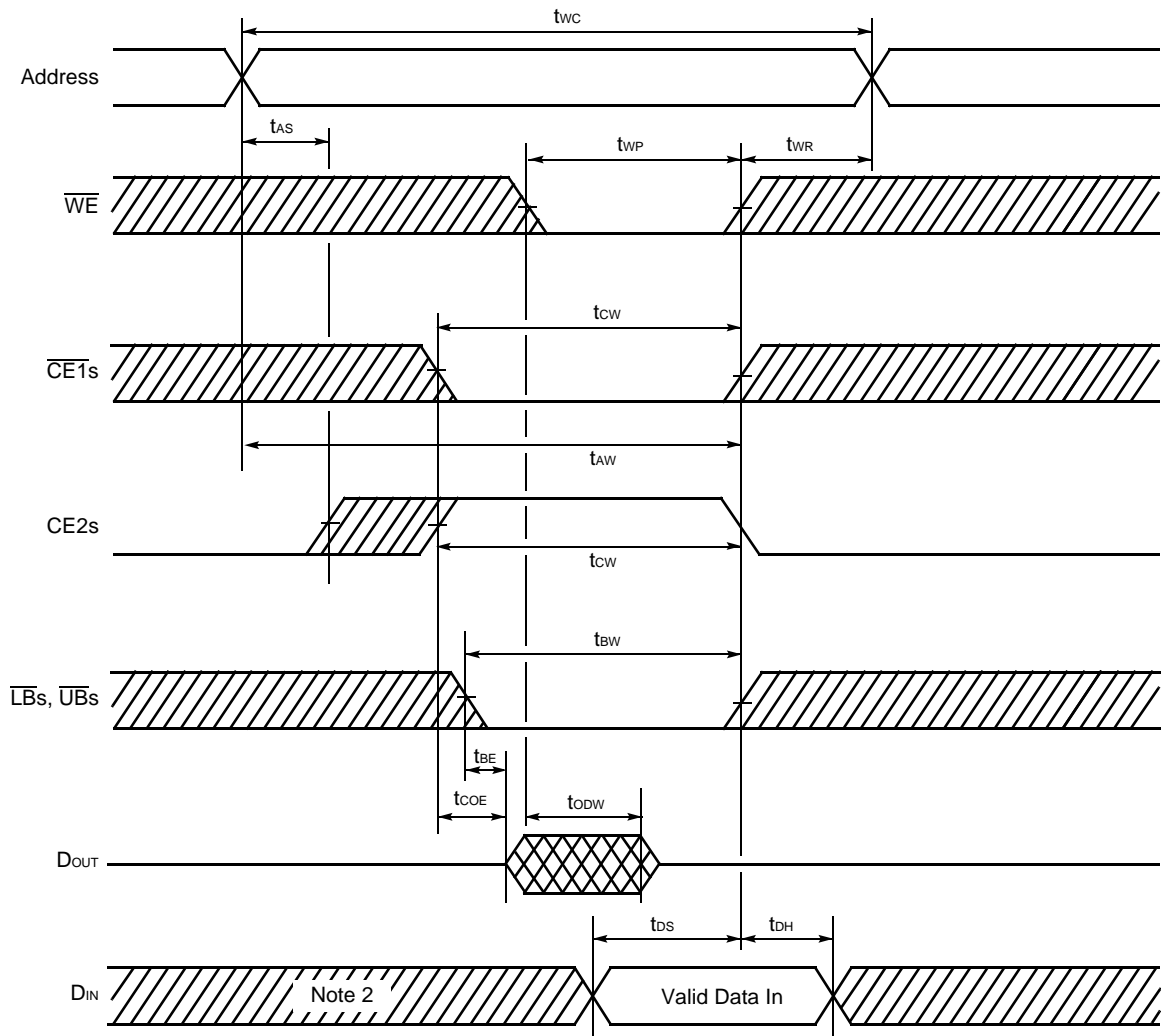
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• Write Cycle (Note 1) ($\overline{CE1s}$ control) (SRAM)



- Notes: 1. If \overline{OE} is "H" during the write cycle, the outputs will remain at High-Z.
 2. Because I/O signals may be in the output state at this Time, input signals of reverse polarity must not be applied.

• Write Cycle (Note 1) (CE2s Control) (SRAM)

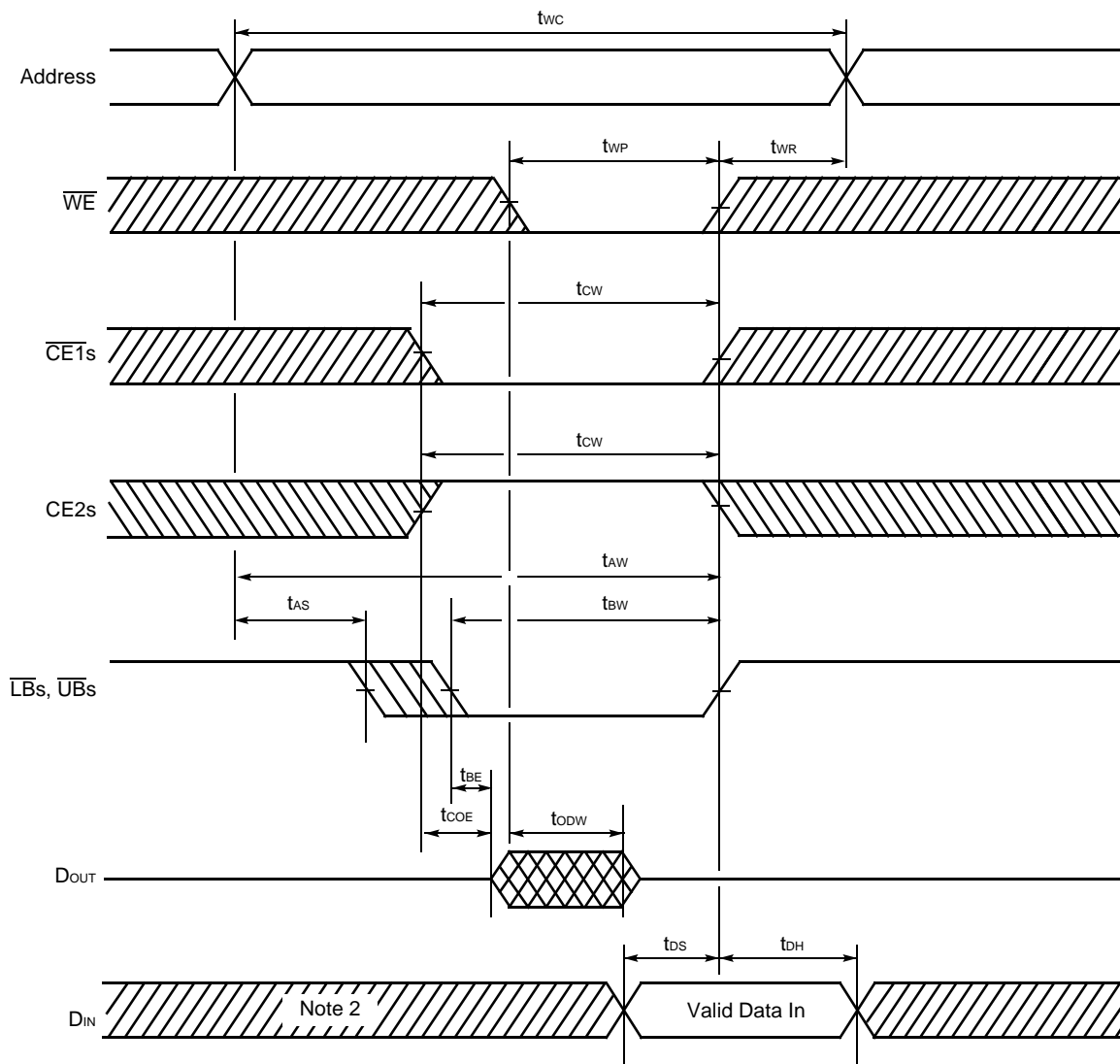


Notes: 1. If \overline{OE} is "H" during the write cycle, the outputs will remain at High-Z.

2. Because I/O signals may be in the output state at this Time, input signals of reverse polarity must not be applied.

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• Write Cycle (Note 1) ($\overline{\text{LBs}}$, $\overline{\text{UBs}}$ Control) (SRAM)



Notes: 1. If $\overline{\text{OE}}$ is "H" during the write cycle, the outputs will remain at High-Z.

2. Because I/O signals may be in the output state at this Time, input signals of reverse polarity must not be applied.

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■ ERASE AND PROGRAMMING PERFORMANCE (Flash)

Parameter	Limits			Unit	Comment
	Min.	Typ.	Max.		
Sector Erase Time	—	1	10	s	Excludes programming time prior to erasure
Byte Programming Time	—	8	300	μ s	Excludes system-level overhead
Word Programming Time	—	16	360	μ s	Excludes system-level overhead
Chip Programming Time	—	—	100	s	Excludes system-level overhead
Erase/Program Cycle	100,000	—	—	cycle	

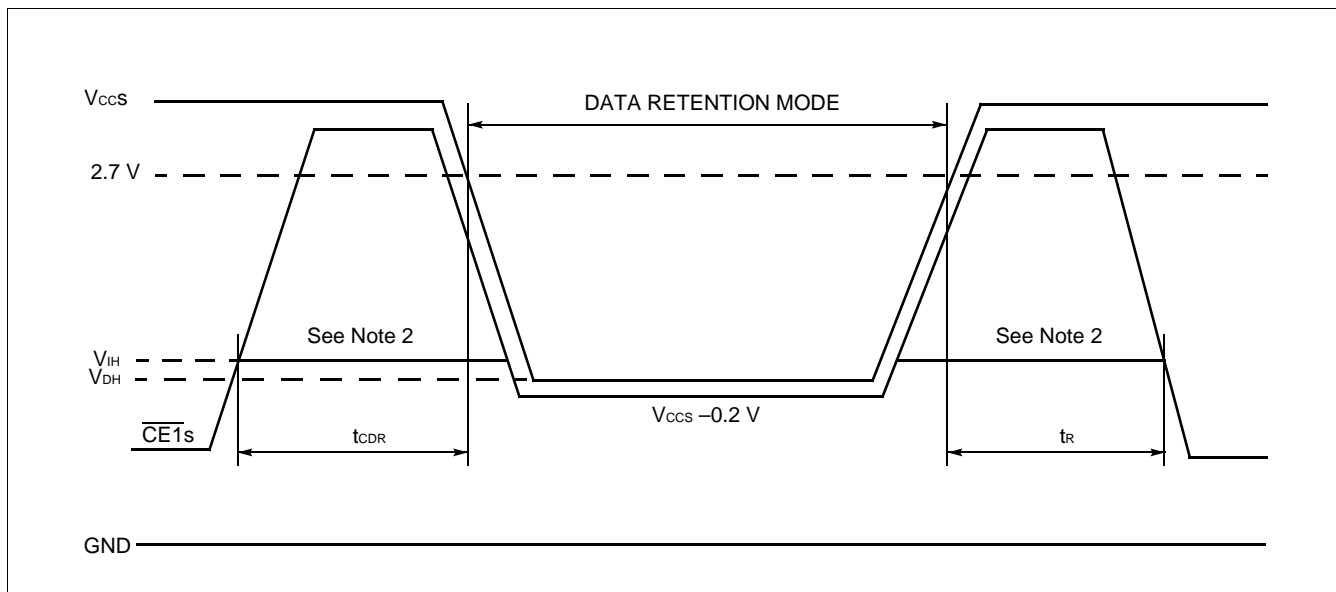
■ DATA RETENTION CHARACTERISTICS (SRAM)

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Data Retention Supply Voltage	V_{DH}	1.5	—	3.3	V
Standby Current	I_{DDs2}	—	1.5	12*	μ A
Chip Deselect to Data Retention Mode Time	t_{CDR}	0	—	—	ns
Recovery Time	t_r	t_{RC}	—	—	ns

*: $T_A=70^\circ\text{C}$

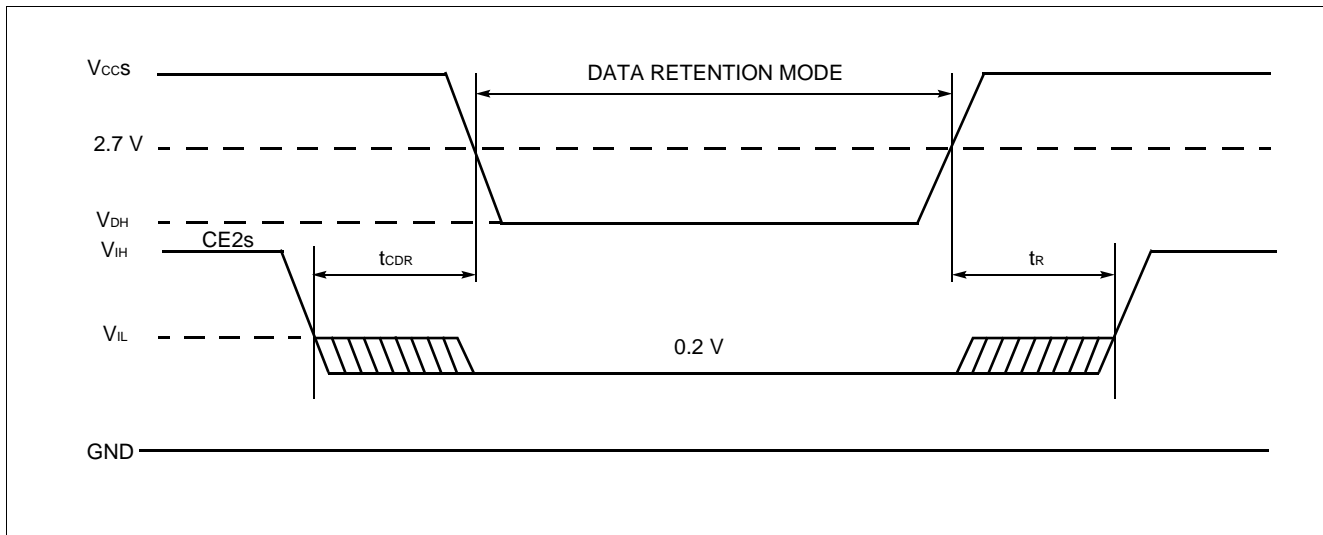
Note: t_{RC} : Read cycle time

• $\overline{\text{CE1}}$ s Controlled Data Retention Mode (Note 1)



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• CE2s Controlled Data Retention Mode (Note 3)



- Notes:
1. In $\overline{CE1}$ s controlled data retention mode, input level of CE2s should be fixed V_{CCS} to V_{CCS}-0.2 V or V_{SS} to 0.2 V during data retention mode. Other input and input/output pins can be used between -0.3 V to V_{CCS}+0.3 V.
 2. When $\overline{CE1}$ s is operating at the V_{IH} Min. level (2.2 V), the standby current is given by I_{SB1S} during the transition of V_{CCS} from 3.6 to 2.2 V.
 3. In CE2s controlled data retention mode, input and input/output pins can be used between -0.3 V to V_{CCS}+0.3 V.

■ PIN CAPACITANCE

Parameter	Symbol	Test Setup	Value		Unit
			Typ.	Max.	
Input Capacitance	C _{IN}	V _{IN} = 0	11	14	pF
Output Capacitance	C _{OUT}	V _{OUT} = 0	12	16	pF
Control Pin Capacitance	C _{IN2}	V _{IN} = 0	14	16	pF
\overline{WP}/ACC Pin Capacitance	C _{IN3}	V _{IN} = 0	21.5	26	pF

Note: Test conditions T_A = 25°C, f = 1.0 MHz

■ HANDLING OF PACKAGE

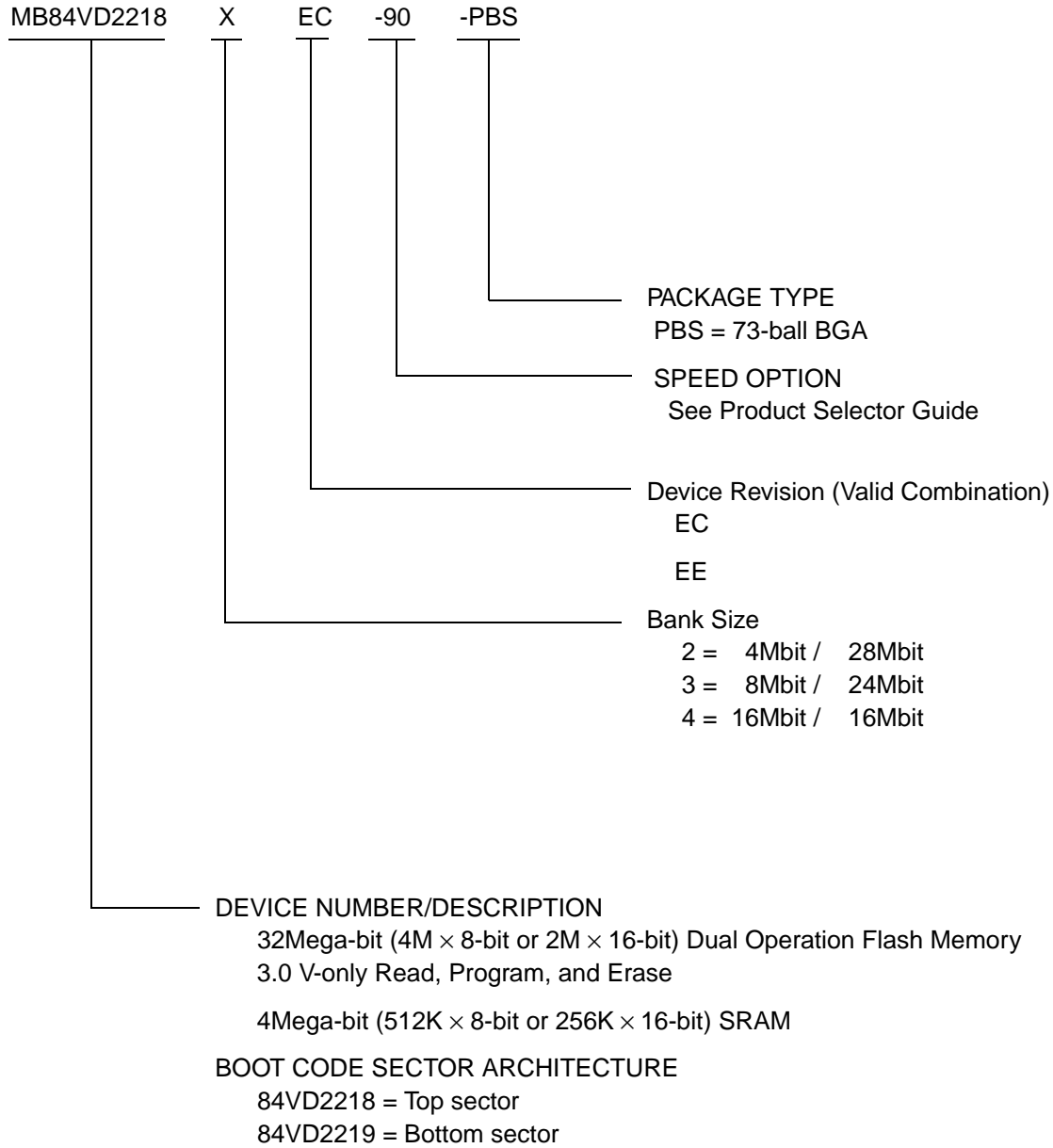
Please handle this package carefully since the sides of packages are right angle.

■ CAUTION

- 1) The high voltage (V_{ID}) can not apply to address pins and control pins except \overline{RESET} . Therefore, it can not use autoselect and sector protect function by applying the high voltage (V_{ID}) to specific pins.
- 2) For the sector protection, since the high voltage (V_{ID}) can be applied to the \overline{RESET} , it can be protected the sector using "Extended sector protect" command.

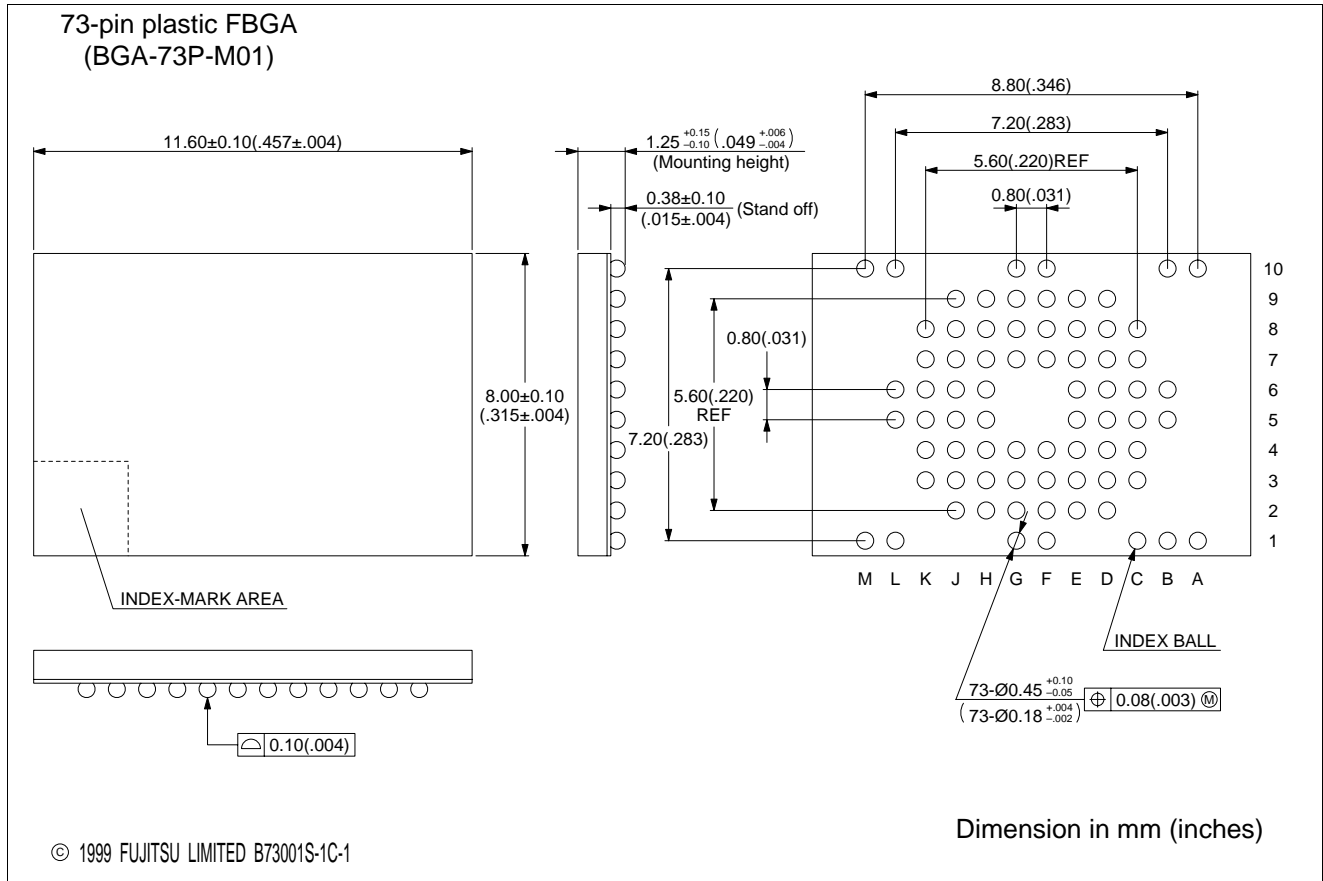
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■ ORDERING INFORMATION



MB84VD2218XEC/EE/2219XEC/EE-90

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