FUJITSU SEMICONDUCTOR
DATA SHEET

DS05-50301-1E

Stacked MCP (Multi-Chip Package) FLASH MEMORY & FCRAM

CMOS

64 M (×16) FLASH MEMORY & 16 M (×16) Mobile FCRAM™

MB84VD23381EF-85

■ FEATURES

- **Power Supply Voltage of 2.7 V to 3.0 V for FCRAM**
- **Power Supply Voltage of 2.7 V to 3.3 V for Flash**
- **High Performance**
  85 ns maximum access time (Flash)
  85 ns maximum access time (FCRAM)

(Continued)

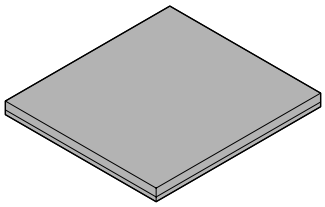
■ PRODUCT LINE UP

	Flash Memory **$V_{CC}f$ = 2.7 V to 3.3 V**	**FCRAM*** **$V_{CC}s$ = 2.7 V to 3.0 V**
Max Address Access Time (ns)	85	85
Max $\overline{CE}$ Access Time (ns)	85	85
Max $\overline{OE}$ Access Time (ns)	35	60

* : Both $V_{CC}f$ and $V_{CC}s$ must be the same level when either part is being accessed and $V_{CC}f$ can be 2.4 V during standby state.

■ PACKAGE

101-ball plastic FBGA



(BGA-101P-M01)

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- **Operating Temperature**
  –30 °C to +85 °C
- **Package 101-ball FBGA**

– FLASH MEMORY

- **Simultaneous Read/Write Operations (FlexBank™)**
  Two virtual Banks are chosen from the combination of four physical banks
  Host system can program or erase in one bank, then read immediately and simultaneously read from the other bank Zero latency between read and write operations
  Read-while-erase
  Read-while-program
- **Minimum 100,000 Write/Erase Cycles**
- **Sector Erase Architecture**
  Sixteen 4 K words and one hundred twenty-six 32 K word sectors.
  Any combination of sectors can be concurrently erased. Also supports full chip erase.
- **Embedded Erase™ Algorithms**
  Automatically pre-programs and erases the chip or any sector
- **Embedded Program™ Algorithms**
  Automatically writes and verifies data at specified address
- **$\overline{\text{Data}}$ Polling and Toggle Bit feature for detection of program or erase cycle completion**
- **Ready-Busy Output (RY/$\overline{\text{BY}}$)**
  Hardware method for detection of program or erase cycle completion
- **Automatic Sleep Mode**
  When addresses remain stable, automatically switch themselves to low power mode.
- **Low V_{CC} Write Inhibit ≤ 2.5 V**
- **Hidden ROM (Hi-ROM) Region**
  256 byte of Hi-ROM, accessible through a new “Hi-ROM Enable” command sequence
  Factory serialized and protected to provide a secure electronic serial number (ESN)
- **$\overline{\text{WP}}$/ACC Input Pin**
  At V_{IL}, allows protection of “outermost” 2 × 8 K bytes on both ends of boot secctors, regardless of sector protection/unprotection status.
  At V_{IH}, allows removal of boot sector protection
  At V_{ACC}, program time will be reduced by 40 %.
- **Program Suspend/Resume**
  Suspends the program operation to allow a read in another byte
- **Erase Suspend/Resume**
  Suspends the erase operation to allow a read in another sector within the same device
- **Please refer to “MBM29DL640E” datasheet in detailed function**

– FCRAM™

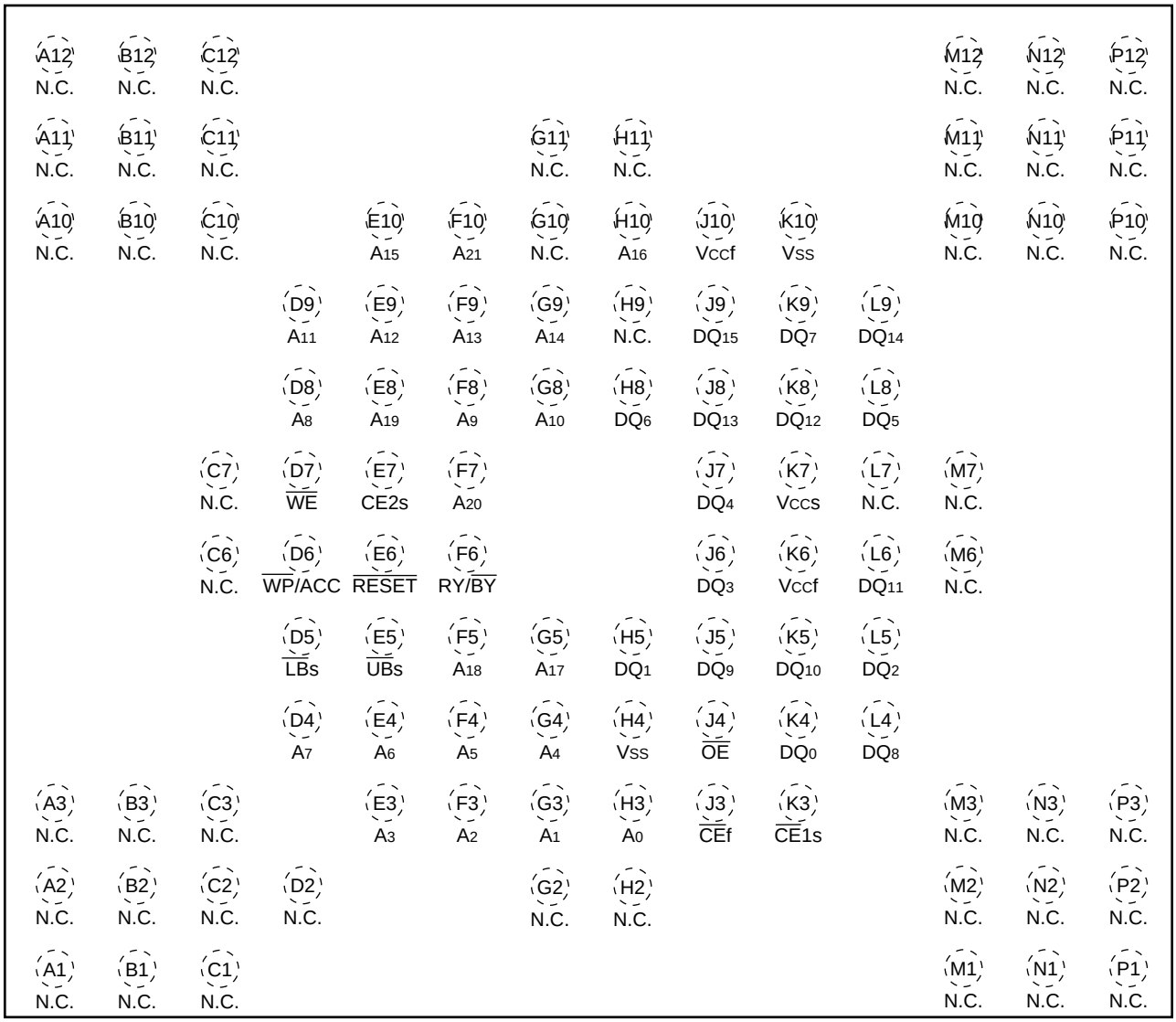
- **Power Dissipation**
  Operating : 20 mA Max
  Standby : 100 µA Max
  Power Down : 10 µA Max
- **Power Down Control by CE2s**
- **Byte Write Control : $\overline{\text{LB}}$s (DQ_7-DQ_0) , $\overline{\text{UB}}$s (DQ_{15}-DQ_8)**

FlexBank™ is a trademark of Fujitsu Limited, Japan.

FCRAMTM™ is a trademark of Fujitsu Limited, Japan.

■ PIN ASSIGNMENT

FBGA
(TOP VIEW)
Marking side



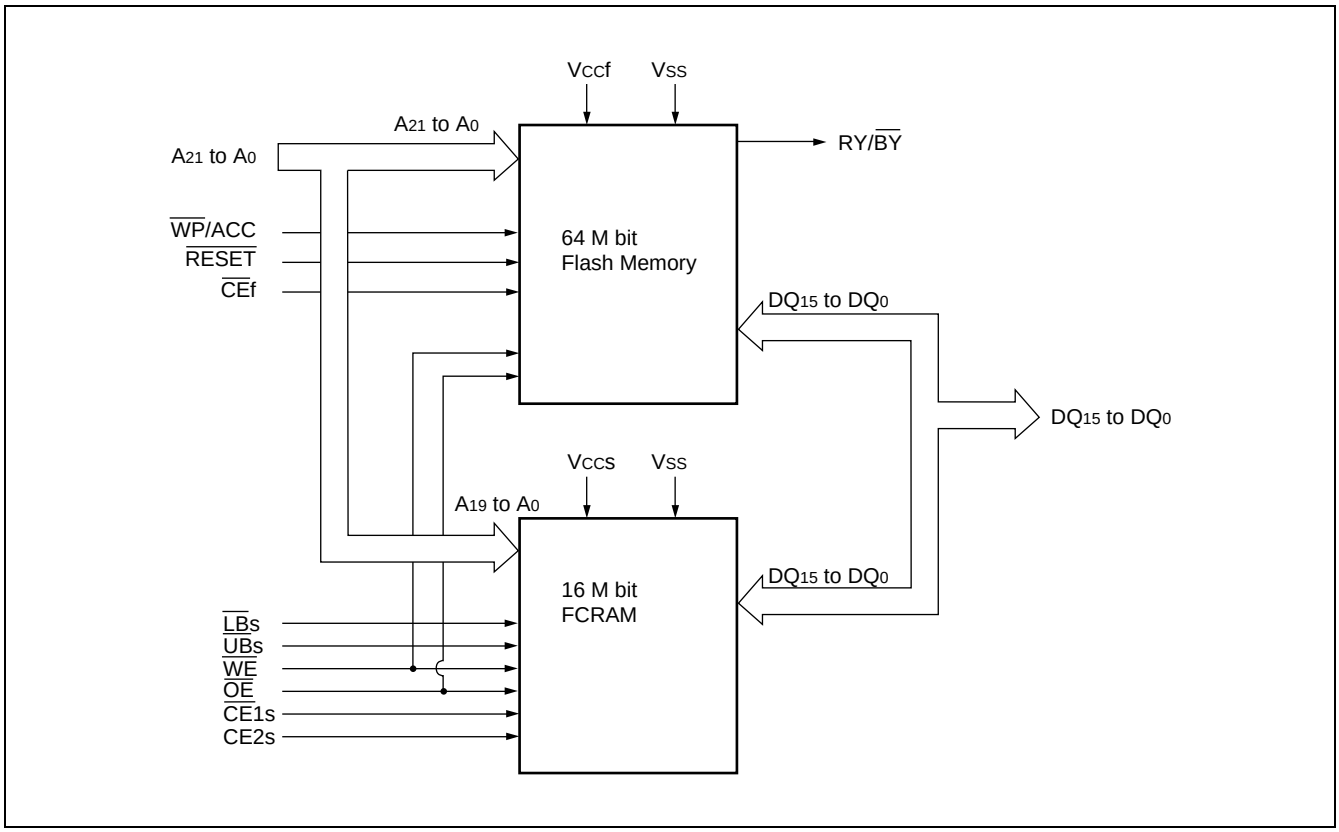
(BGA-101P-M01)

■ PIN DESCRIPTION

Pin Configuration

Pin	Function	Input/Output
A_{19} to A_0	Address Inputs (Common)	I
A_{21}, A_{20}	Address Input (Flash)	I
DQ_{15} to DQ_0	Data Inputs/Outputs (Common)	I/O
$\overline{CE}$f	Chip Enable (Flash)	I
$\overline{CE}$1s	Chip Enable (FCRAM)	I
CE2s	Chip Enable (FCRAM)	I
$\overline{OE}$	Output Enable (Common)	I
$\overline{WE}$	Write Enable (Common)	I
RY/$\overline{BY}$	Ready/Busy Outputs (Flash) Open Drain Output	O
$\overline{UB}$s	Upper Byte Control (FCRAM)	I
$\overline{LB}$s	Lower Byte Control (FCRAM)	I
$\overline{RESET}$	Hardware Reset Pin/Sector Protection Unlock (Flash)	I
$\overline{WP}$/ACC	Write Protect/Acceleration (Flash)	I
N.C.	No Internal Connection	—
V_{SS}	Device Ground (Common)	Power
V_{CC}f	Device Power Supply (Flash)	Power
V_{CC}s	Device Power Supply (FCRAM)	Power

■ BLOCK DIAGRAM



■ DEVICE BUS OPERATIONS

User Bus Operations

Operation*1, *2	$\overline{CE}$f	$\overline{CE}$1s	CE2s	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$s	$\overline{UB}$s	DQ_7 to DQ_0	DQ_{15} to DQ_8	$\overline{RESET}$	$\overline{WP}$/ ACC*5
Full Standby	H	H	X	X	X	X	X	High-Z	High-Z	H	X
Output Disable*3	H	L	H	H	H	X	X	High-Z	High-Z	H	X
	L	H	H	H	H	X	X	High-Z	High-Z		
Read from Flash*4	L	H	H	L	H	X	X	D_{OUT}	D_{OUT}	H	X
Write to Flash	L	H	H	H	L	X	X	D_{IN}	D_{IN}	H	X
Read from FCRAM*5	H	L	H	L	H	X	X	D_{OUT}	D_{OUT}	H	X
Write to FCRAM	H	L	H	H	L	L	L	D_{IN}	D_{IN}	H	X
						H	L	High-Z	D_{IN}		
						L	H	D_{IN}	High-Z		
Temporary Sector Group Unprotection*6	X	X	X	X	X	X	X	X	X	V_{ID}	X
Flash Hardware Reset	X	H	H	X	X	X	X	High-Z	High-Z	L	X
Boot Block Sector Write Protection	X	X	X	X	X	X	X	X	X	X	L
FCRAM Power Down	X	L	L	X	X	X	X	X	X	X	X

Legend : L = V_{IL}, H = V_{IH}, X = V_{IL} or V_{IH}. See "■ DC CHARACTERISTICS" for voltage levels.

*1 : Other operations not indicated in this column are prohibited.

*2 : Do not apply $\overline{CE}$f = V_{IL}, $\overline{CE}$1s = V_{IL} and CE2s = V_{IH} all at once.

*3 : FCRAM Output Disable condition should not be kept longer than 1 μs.

*4 : $\overline{WE}$ can be V_{IL} if $\overline{OE}$ is V_{IL}, $\overline{OE}$ at V_{IH} initiates the write operations.

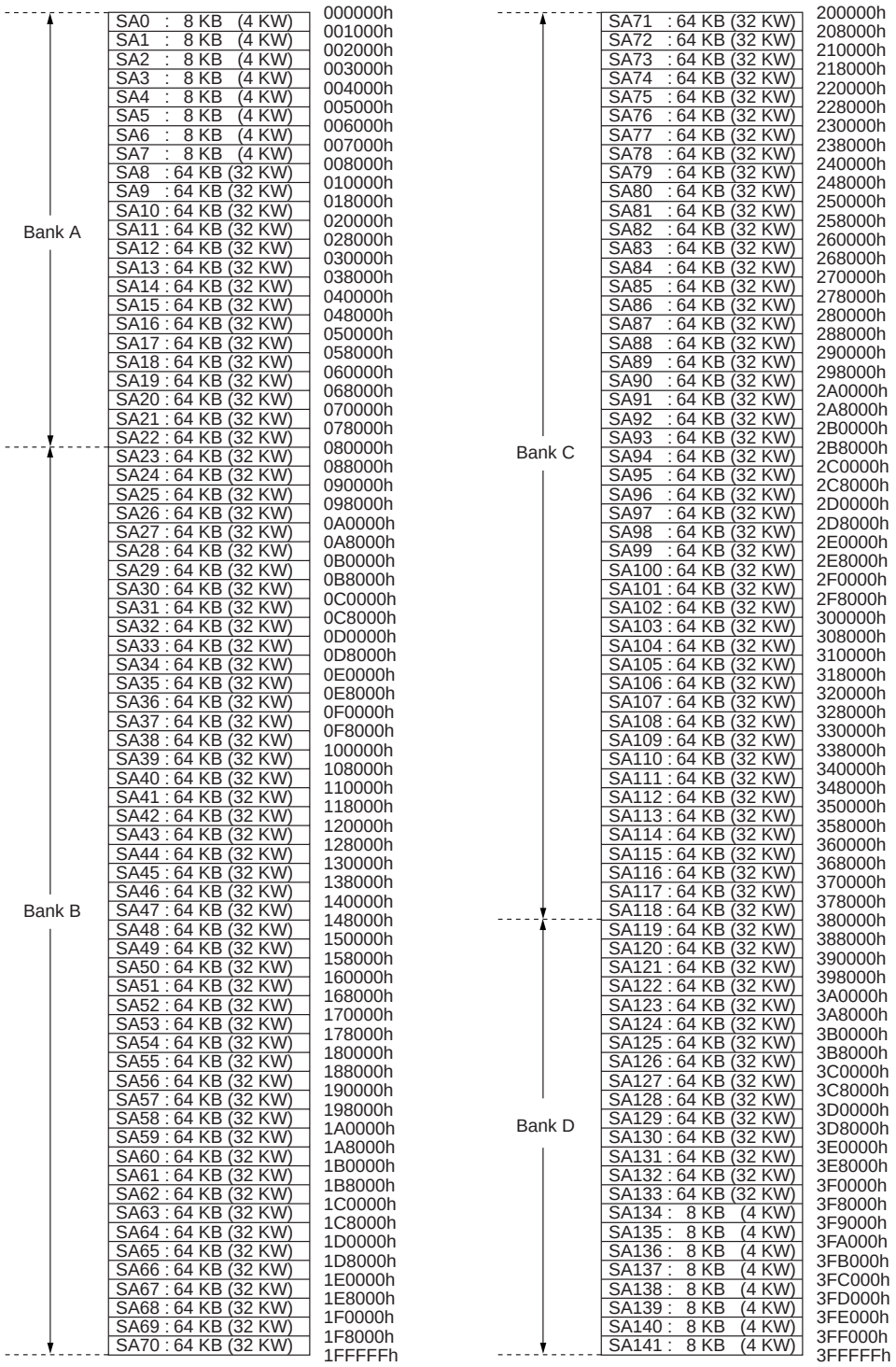
*5 : FCRAM Byte control at Read operation is not supported.

*6 : Also used for the extended sector group protections.

Note : Protect "outermost" 2 × 8 K bytes (4 words) on both ends of the boot block sectors.

■ FLEXIBLE SECTOR-ERASE ARCHITECTURE on FLASH MEMORY

- Sixteen 4 K words, and one hundred twenty-six 32 K words.
- Individual-sector, multiple sector, or bulk-erase capability.



MB84VD23381EF Sector Architecture

Example of Virtual Banks Combination

Bank Splits	Bank 1				Bank 2			
	Mega bits	Combination of Memory Bank	Sectors		Mega bits	Combination of Memory Bank	Sectors	
			8 K byte/ 4 K word	64 K byte/ 32 K word			8 K byte/ 4 K word	64 K byte/ 32 K word
1	8 M bits	Bank A	8	15	56 Mbits	Bank B Bank C Bank D	8	111
2	16 Mbits	Bank A Bank D	16	30	48 Mbits	Bank B Bank C	0	96
3	24 Mbits	Bank B	0	48	40 Mbits	Bank A Bank C Bank D	16	78
4	32 Mbits	Bank A Bank B	8	63	32 Mbits	Bank C Bank D	8	63

BankA : Address 000000h to 07FFFFh
BankB : Address 080000h to 1FFFFFh
BankC : Address 200000h to 37FFFFh
BankD : Address 380000h to 3FFFFFh

Sector Address Tables

Bank	Sector	Sector Address										Address Range
		Bank Address										
		A_{21}	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	
Bank A	SA0	0	0	0	0	0	0	0	0	0	0	000000h to 000FFFh
	SA1	0	0	0	0	0	0	0	0	0	1	001000h to 001FFFh
	SA2	0	0	0	0	0	0	0	0	1	0	002000h to 002FFFh
	SA3	0	0	0	0	0	0	0	0	1	1	003000h to 003FFFh
	SA4	0	0	0	0	0	0	0	1	0	0	004000h to 004FFFh
	SA5	0	0	0	0	0	0	0	1	0	1	005000h to 005FFFh
	SA6	0	0	0	0	0	0	0	1	1	0	006000h to 006FFFh
	SA7	0	0	0	0	0	0	0	1	1	1	007000h to 007FFFh
	SA8	0	0	0	0	0	0	1	X	X	X	008000h to 00FFFFh
	SA9	0	0	0	0	0	1	0	X	X	X	010000h to 017FFFh
	SA10	0	0	0	0	0	1	1	X	X	X	018000h to 01FFFFh
	SA11	0	0	0	0	1	0	0	X	X	X	020000h to 027FFFh
	SA12	0	0	0	0	1	0	1	X	X	X	028000h to 02FFFFh
	SA13	0	0	0	0	1	1	0	X	X	X	030000h to 037FFFh
	SA14	0	0	0	0	1	1	1	X	X	X	038000h to 03FFFFh
	SA15	0	0	0	1	0	0	0	X	X	X	040000h to 047FFFh

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Bank	Sector	Sector Address										Address Range
		Bank Address										
		A_{21}	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	
Bank A	SA16	0	0	0	1	0	0	1	X	X	X	048000h to 04FFFFh
	SA17	0	0	0	1	0	1	0	X	X	X	050000h to 057FFFh
	SA18	0	0	0	1	0	1	1	X	X	X	058000h to 05FFFFh
	SA19	0	0	0	1	1	0	0	X	X	X	060000h to 067FFFh
	SA20	0	0	0	1	1	0	1	X	X	X	068000h to 06FFFFh
	SA21	0	0	0	1	1	1	0	X	X	X	070000h to 077FFFh
	SA22	0	0	0	1	1	1	1	X	X	X	078000h to 07FFFFh
Bank B	SA23	0	0	1	0	0	0	0	X	X	X	080000h to 087FFFh
	SA24	0	0	1	0	0	0	1	X	X	X	088000h to 08FFFFh
	SA25	0	0	1	0	0	1	0	X	X	X	090000h to 097FFFh
	SA26	0	0	1	0	0	1	1	X	X	X	098000h to 09FFFFh
	SA27	0	0	1	0	1	0	0	X	X	X	0A0000h to 0A7FFFh
	SA28	0	0	1	0	1	0	1	X	X	X	0A8000h to 0AFFFFh
	SA29	0	0	1	0	1	1	0	X	X	X	0B0000h to 0B7FFFh
	SA30	0	0	1	0	1	1	1	X	X	X	0B8000h to 0BFFFFh
	SA31	0	0	1	1	0	0	0	X	X	X	0C0000h to 0C7FFFh
	SA32	0	0	1	1	0	0	1	X	X	X	0C8000h to 0CFFFFh
	SA33	0	0	1	1	0	1	0	X	X	X	0D0000h to 0D7FFFh
	SA34	0	0	1	1	0	1	1	X	X	X	0D8000h to 0DFFFFh
	SA35	0	0	1	1	1	0	0	X	X	X	0E0000h to 0E7FFFh
	SA36	0	0	1	1	1	0	1	X	X	X	0E8000h to 0EFFFFh
	SA37	0	0	1	1	1	1	0	X	X	X	0F0000h to 0F7FFFh
	SA38	0	0	1	1	1	1	1	X	X	X	0F8000h to 0FFFFFh
	SA39	0	1	0	0	0	0	0	X	X	X	100000h to 107FFFh
	SA40	0	1	0	0	0	0	1	X	X	X	108000h to 10FFFFh
	SA41	0	1	0	0	0	1	0	X	X	X	110000h to 117FFFh
	SA42	0	1	0	0	0	1	1	X	X	X	118000h to 11FFFFh
	SA43	0	1	0	0	1	0	0	X	X	X	120000h to 127FFFh
	SA44	0	1	0	0	1	0	1	X	X	X	128000h to 12FFFFh
	SA45	0	1	0	0	1	1	0	X	X	X	130000h to 137FFFh
	SA46	0	1	0	0	1	1	1	X	X	X	138000h to 13FFFFh
	SA47	0	1	0	1	0	0	0	X	X	X	140000h to 147FFFh
	SA48	0	1	0	1	0	0	1	X	X	X	148000h to 14FFFFh

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Bank	Sector	Sector Address										Address Range
		Bank Address										
		A_{21}	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	
Bank B	SA49	0	1	0	1	0	1	0	X	X	X	150000h to 157FFFh
	SA50	0	1	0	1	0	1	1	X	X	X	158000h to 15FFFFh
	SA51	0	1	0	1	1	0	0	X	X	X	160000h to 167FFFh
	SA52	0	1	0	1	1	0	1	X	X	X	168000h to 16FFFFh
	SA53	0	1	0	1	1	1	0	X	X	X	170000h to 177FFFh
	SA54	0	1	0	1	1	1	1	X	X	X	178000h to 17FFFFh
	SA55	0	1	1	0	0	0	0	X	X	X	180000h to 187FFFh
	SA56	0	1	1	0	0	0	1	X	X	X	188000h to 18FFFFh
	SA57	0	1	1	0	0	1	0	X	X	X	190000h to 197FFFh
	SA58	0	1	1	0	0	1	1	X	X	X	198000h to 19FFFFh
	SA59	0	1	1	0	1	0	0	X	X	X	1A0000h to 1A7FFFh
	SA60	0	1	1	0	1	0	1	X	X	X	1A8000h to 1AFFFFh
	SA61	0	1	1	0	1	1	0	X	X	X	1B0000h to 1B7FFFh
	SA62	0	1	1	0	1	1	1	X	X	X	1B8000h to 1BFFFFh
	SA63	0	1	1	1	0	0	0	X	X	X	1C0000h to 1C7FFFh
	SA64	0	1	1	1	0	0	1	X	X	X	1C8000h to 1CFFFFh
	SA65	0	1	1	1	0	1	0	X	X	X	1D0000h to 1D7FFFh
	SA66	0	1	1	1	0	1	1	X	X	X	1D8000h to 1DFFFFh
	SA67	0	1	1	1	1	0	0	X	X	X	1E0000h to 1E7FFFh
	SA68	0	1	1	1	1	0	1	X	X	X	1E8000h to 1EFFFFh
	SA69	0	1	1	1	1	1	0	X	X	X	1F0000h to 1F7FFFh
	SA70	0	1	1	1	1	1	1	X	X	X	1F8000h to 1FFFFFh
Bank C	SA71	1	0	0	0	0	0	0	X	X	X	200000h to 207FFFh
	SA72	1	0	0	0	0	0	1	X	X	X	208000h to 20FFFFh
	SA73	1	0	0	0	0	1	0	X	X	X	210000h to 217FFFh
	SA74	1	0	0	0	0	1	1	X	X	X	218000h to 21FFFFh
	SA75	1	0	0	0	1	0	0	X	X	X	220000h to 227FFFh
	SA76	1	0	0	0	1	0	1	X	X	X	228000h to 22FFFFh
	SA77	1	0	0	0	1	1	0	X	X	X	230000h to 237FFFh
	SA78	1	0	0	0	1	1	1	X	X	X	238000h to 23FFFFh
	SA79	1	0	0	1	0	0	0	X	X	X	240000h to 247FFFh
	SA80	1	0	0	1	0	0	1	X	X	X	248000h to 24FFFFh
	SA81	1	0	0	1	0	1	0	X	X	X	250000h to 257FFFh

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Bank	Sector	Sector Address										Address Range
		Bank Address										
		A_{21}	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	
Bank C	SA82	1	0	0	1	0	1	1	X	X	X	258000h to 25FFFFh
	SA83	1	0	0	1	1	0	0	X	X	X	260000h to 267FFFh
	SA84	1	0	0	1	1	0	1	X	X	X	268000h to 26FFFFh
	SA85	1	0	0	1	1	1	0	X	X	X	270000h to 277FFFh
	SA86	1	0	0	1	1	1	1	X	X	X	278000h to 27FFFFh
	SA87	1	0	1	0	0	0	0	X	X	X	280000h to 287FFFh
	SA88	1	0	1	0	0	0	1	X	X	X	288000h to 28FFFFh
	SA89	1	0	1	0	0	1	0	X	X	X	290000h to 297FFFh
	SA90	1	0	1	0	0	1	1	X	X	X	298000h to 29FFFFh
	SA91	1	0	1	0	1	0	0	X	X	X	2A0000h to 2A7FFFh
	SA92	1	0	1	0	1	0	1	X	X	X	2A8000h to 2AFFFFh
	SA93	1	0	1	0	1	1	0	X	X	X	2B0000h to 2B7FFFh
	SA94	1	0	1	0	1	1	1	X	X	X	2B8000h to 2BFFFFh
	SA95	1	0	1	1	0	0	0	X	X	X	2C0000h to 2C7FFFh
	SA96	1	0	1	1	0	0	1	X	X	X	2C8000h to 2CFFFFh
	SA97	1	0	1	1	0	1	0	X	X	X	2D0000h to 2D7FFFh
	SA98	1	0	1	1	0	1	1	X	X	X	2D8000h to 2DFFFFh
	SA99	1	0	1	1	1	0	0	X	X	X	2E0000h to 2E7FFFh
	SA100	1	0	1	1	1	0	1	X	X	X	2E8000h to 2EFFFFh
	SA101	1	0	1	1	1	1	0	X	X	X	2F0000h to 2F7FFFh
	SA102	1	0	1	1	1	1	1	X	X	X	2F8000h to 2FFFFFh
	SA103	1	1	0	0	0	0	0	X	X	X	300000h to 307FFFh
	SA104	1	1	0	0	0	0	1	X	X	X	308000h to 30FFFFh
	SA105	1	1	0	0	0	1	0	X	X	X	310000h to 317FFFh
	SA106	1	1	0	0	0	1	1	X	X	X	318000h to 31FFFFh
	SA107	1	1	0	0	1	0	0	X	X	X	320000h to 327FFFh
	SA108	1	1	0	0	1	0	1	X	X	X	328000h to 32FFFFh
	SA109	1	1	0	0	1	1	0	X	X	X	330000h to 337FFFh
	SA110	1	1	0	0	1	1	1	X	X	X	338000h to 33FFFFh
	SA111	1	1	0	1	0	0	0	X	X	X	340000h to 347FFFh
	SA112	1	1	0	1	0	0	1	X	X	X	348000h to 34FFFFh
	SA113	1	1	0	1	0	1	0	X	X	X	350000h to 357FFFh
	SA114	1	1	0	1	0	1	1	X	X	X	358000h to 35FFFFh

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Bank	Sector	Sector Address										Address Range
		Bank Address										
		A_{21}	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	
Bank C	SA115	1	1	0	1	1	0	0	X	X	X	360000h to 367FFFh
	SA116	1	1	0	1	1	0	1	X	X	X	368000h to 36FFFFh
	SA117	1	1	0	1	1	1	0	X	X	X	370000h to 377FFFh
	SA118	1	1	0	1	1	1	1	X	X	X	378000h to 37FFFFh
Bank D	SA119	1	1	1	0	0	0	0	X	X	X	380000h to 387FFFh
	SA120	1	1	1	0	0	0	1	X	X	X	388000h to 38FFFFh
	SA121	1	1	1	0	0	1	0	X	X	X	390000h to 397FFFh
	SA122	1	1	1	0	0	1	1	X	X	X	398000h to 39FFFFh
	SA123	1	1	1	0	1	0	0	X	X	X	3A0000h to 3A7FFFh
	SA124	1	1	1	0	1	0	1	X	X	X	3A8000h to 3AFFFFh
	SA125	1	1	1	0	1	1	0	X	X	X	3B0000h to 3B7FFFh
	SA126	1	1	1	0	1	1	1	X	X	X	3B8000h to 3BFFFFh
	SA127	1	1	1	1	0	0	0	X	X	X	3C0000h to 3C7FFFh
	SA128	1	1	1	1	0	0	1	X	X	X	3C8000h to 3CFFFFh
	SA129	1	1	1	1	0	1	0	X	X	X	3D0000h to 3D7FFFh
	SA130	1	1	1	1	0	1	1	X	X	X	3D8000h to 3DFFFFh
	SA131	1	1	1	1	1	0	0	X	X	X	3E0000h to 3E7FFFh
	SA132	1	1	1	1	1	0	1	X	X	X	3E8000h to 3EFFFFh
	SA133	1	1	1	1	1	1	0	X	X	X	3F0000h to 3F7FFFh
	SA134	1	1	1	1	1	1	1	0	0	0	3F8000h to 3F8FFFh
	SA135	1	1	1	1	1	1	1	0	0	1	3F9000h to 3F9FFFh
	SA136	1	1	1	1	1	1	1	0	1	0	3FA000h to 3FAFFFh
	SA137	1	1	1	1	1	1	1	0	1	1	3FB000h to 3FBFFFh
	SA138	1	1	1	1	1	1	1	1	0	0	3FC000h to 3FCFFFh
	SA139	1	1	1	1	1	1	1	1	0	1	3FD000h to 3FDFFFh
	SA140	1	1	1	1	1	1	1	1	1	0	3FE000h to 3FEFFFh
	SA141	1	1	1	1	1	1	1	1	1	1	3FF000h to 3FFFFFh

Sector Group Addresses (MB84VD23381EF)

Sector Group	A_{21}	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	Sectors
SGA0	0	0	0	0	0	0	0	0	0	0	SA0
SGA1	0	0	0	0	0	0	0	0	0	1	SA1
SGA2	0	0	0	0	0	0	0	0	1	0	SA2
SGA3	0	0	0	0	0	0	0	0	1	1	SA3
SGA4	0	0	0	0	0	0	0	1	0	0	SA4
SGA5	0	0	0	0	0	0	0	1	0	1	SA5
SGA6	0	0	0	0	0	0	0	1	1	0	SA6
SGA7	0	0	0	0	0	0	0	1	1	1	SA7
SGA8	0	0	0	0	0	0	0	X	X	X	SA8 to SA10
						0	1				
						1	0				
SGA9	0	0	0	0	1	X	X	X	X	X	SA11 to SA14
SGA10	0	0	0	1	0	X	X	X	X	X	SA15 to SA18
SGA11	0	0	0	1	1	X	X	X	X	X	SA19 to SA22
SGA12	0	0	1	0	0	X	X	X	X	X	SA23 to SA26
SGA13	0	0	1	0	1	X	X	X	X	X	SA24 to SA30
SGA14	0	0	1	1	0	X	X	X	X	X	SA31 to SA34
SGA15	0	0	1	1	1	X	X	X	X	X	SA35 to SA38
SGA16	0	1	0	0	0	X	X	X	X	X	SA39 to SA42
SGA17	0	1	0	0	1	X	X	X	X	X	SA43 to SA46
SGA18	0	1	0	1	0	X	X	X	X	X	SA47 to SA50
SGA19	0	1	0	1	1	X	X	X	X	X	SA51 to SA54
SGA20	0	1	1	0	0	X	X	X	X	X	SA55 to SA58
SGA21	0	1	1	0	1	X	X	X	X	X	SA59 to SA62
SGA22	0	1	1	1	0	X	X	X	X	X	SA63 to SA66
SGA23	0	1	1	1	1	X	X	X	X	X	SA67 to SA70
SGA24	1	0	0	0	0	X	X	X	X	X	SA71 to SA74
SGA25	1	0	0	0	1	X	X	X	X	X	SA75 to SA78
SGA26	1	0	0	1	0	X	X	X	X	X	SA79 to SA82
SGA27	1	0	0	1	1	X	X	X	X	X	SA83 to SA86
SGA28	1	0	1	0	0	X	X	X	X	X	SA87 to SA90
SGA29	1	0	1	0	1	X	X	X	X	X	SA91 to SA94
SGA30	1	0	1	1	0	X	X	X	X	X	SA95 to SA98
SGA31	1	0	1	1	1	X	X	X	X	X	SA99 to SA102
SGA32	1	1	0	0	0	X	X	X	X	X	SA103 to SA106

(Continued)

(Continued)

Sector Group	A_{21}	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	Sectors
SGA33	1	1	0	0	1	X	X	X	X	X	SA107 to SA110
SGA34	1	1	0	1	0	X	X	X	X	X	SA111 to SA114
SGA35	1	1	0	1	1	X	X	X	X	X	SA115 to SA118
SGA36	1	1	1	0	0	X	X	X	X	X	SA119 to SA122
SGA37	1	1	1	0	1	X	X	X	X	X	SA123 to SA126
SGA38	1	1	1	1	0	X	X	X	X	X	SA127 to SA130
SGA39	1	1	1	1	1	0	0	X	X	X	SA131 to SA133
						0	1				
						1	0				
SGA40	1	1	1	1	1	1	1	0	0	0	SA134
SGA41	1	1	1	1	1	1	1	0	0	1	SA135
SGA42	1	1	1	1	1	1	1	0	1	0	SA136
SGA43	1	1	1	1	1	1	1	0	1	1	SA137
SGA44	1	1	1	1	1	1	1	1	0	0	SA138
SGA45	1	1	1	1	1	1	1	1	0	1	SA139
SGA46	1	1	1	1	1	1	1	1	1	0	SA140
SGA47	1	1	1	1	1	1	1	1	1	1	SA141

Flash Memory Autoselect Codes

Type	A_{21} to A_{12}	A_6	A_3	A_2	A_1	A_0	Code (HEX)
Manufacture's Code	BA*2	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	04h
Device Code	BA*2	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	227Eh
Extended Device Code	BA*2	V_{IL}	V_{IH}	V_{IH}	V_{IH}	V_{IL}	2202h
	BA*2	V_{IL}	V_{IH}	V_{IH}	V_{IH}	V_{IH}	2201h
Sector Group Protection	Sector Group Addresses	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	01h*1

*1 : Outputs 01h at protected sector group addresses and outputs 00h at unprotected sector group addresses.

*2 : BA is Bank Address which is needed only in Command Autoselect mode.

Flash Memory Command Definitions

Command Sequence	Bus Write Cycles Req'd	First Bus Write Cycle		Second Bus Write Cycle		Third Bus Write Cycle		Fourth Bus Read/Write Cycle		Fifth Bus Write Cycle		Sixth Bus Write Cycle	
		Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data
Read/Reset*1	1	XXXh	F0h	—	—	—	—	—	—	—	—	—	—
Read/Reset*1	3	555h	AAh	2AAh	55h	555h	F0h	RA	RD	—	—	—	—
Autoselect	3	555h	AAh	2AAh	55h	(BA) 555h	90h	—	—	—	—	—	—
Program	4	555h	AAh	2AAh	55h	555h	A0h	PA	PD	—	—	—	—
Chip Erase	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	555h	10h
Sector Erase	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	SA	30h
Sector Erase Suspend	1	BA	B0h	—	—	—	—	—	—	—	—	—	—
Sector Erase Resume	1	BA	30h	—	—	—	—	—	—	—	—	—	—
Program Suspend	1	BA	B0h	—	—	—	—	—	—	—	—	—	—
Program Resume	1	BA	30h	—	—	—	—	—	—	—	—	—	—
Set to Fast Mode	3	555h	AAh	2AAh	55h	555h	20h	—	—	—	—	—	—
Fast Program *2	2	XXXh	A0h	PA	PD	—	—	—	—	—	—	—	—
Reset from Fast Mode*2	2	BA	90h	XXXh	F0h *6	—	—	—	—	—	—	—	—
Extended Sector Group Protection *3	4	XXXh	60h	SPA	60h	SPA	40h	SPA	SD	—	—	—	—
Query *4	1	(BA) 55h	98h	—	—	—	—	—	—	—	—	—	—
Hi-ROM Entry	3	555h	AAh	2AAh	55h	555h	88h	—	—	—	—	—	—
Hi-ROM Program *5	4	555h	AAh	2AAh	55h	555h	A0h	(HRA) PA	PD	—	—	—	—
Hi-ROM Exit *5	4	555h	AAh	2AAh	55h	(HRBA) 555h	90h	XXXh	00h	—	—	—	—

(Continued)

(Continued)

*1 : Both Read/Reset commands are functionally equivalent, resetting the device to the read mode.

*2 : This command is valid during Fast Mode.

*3 : This command is valid while $\overline{RESET} = V_{ID}$.

*4 : The valid addresses are A_6 to A_0.

*5 : This command is valid during Hi-ROM mode.

*6 : The data “00h” is also acceptable.

Notes :
- Address bits A_{21} to A_{11} = X = “H” or “L” for all address commands except for Program Address (PA) , Sector Address (SA) , and Bank Address (BA) .
- Bus operations are defined in “User Bus Operation” in “■ DEVICE BUS OPERATIONS”.
- RA = Address of the memory location to be read.
  PA = Address of the memory location to be programmed.
  Addresses are latched on the falling edge of the write pulse.
  SA = Address of the sector to be erased. The combination of A_{21}, A_{20}, A_{19}, A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13}, and A_{12} will uniquely select any sector.
  BA = Bank address (A_{21} to A_{19})
- RD = Data read from location RA during read operation.
  PD = Data to be programmed at location PA. Data is latched on the rising edge of write pulse.
- SPA = Sector group address to be protected. Set sector group address (SGA) and (A_6, A_3, A_2, A_1, A_0) = (0, 0, 0, 1, 0) .
  SD = Sector group protection verify data. Output 01h at protected sector group addresses and output 00h at unprotected sector group addresses.
- HRA = Address of the Hi-ROM area (000000h to 00007Fh)
- HRBA = Bank Address of the Hi-ROM area ($A_{21} = A_{20} = A_{19} = V_{IL}$)
- The system should generate the following address patterns: 555h or 2AAh to addresses (A_{10} to A_0) .
- Both Read/Reset commands are functionally equivalent, resetting the device to the read mode.
- The Command combinations not described in “Flash Memory Command Definitions” table are illegal.

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Storage Temperature	Tstg	–55	+125	°C
Ambient Temperature with Power Applied	T_A	–30	+85	°C
Voltage with Respect to Ground All pins*1	V_{IN}	–0.3	$V_{CC}f$ + 0.3	V
	V_{OUT}	–0.3	$V_{CC}s$ + 0.3	V
$V_{CC}f$ Supply*1, *2	$V_{CC}f$	–0.2	+3.6	V
$V_{CC}s$ Supply*1	$V_{CC}s$	–0.2	+3.3	V
$\overline{RESET}$*1, *3	V_{IN}	–0.5	+13.0	V
$\overline{WP}$/ACC*1, *4	V_{ACC}	–0.5	+10.5	V

*1 : Voltage is defined on the basis of V_{SS} = GND = 0 V.

*2 : Minimum DC voltage on input or I/O pins is –0.3 V. During voltage transitions, input or I/O pins may undershoot V_{SS} to –1.0 V for periods of up to 20 ns. Maximum DC voltage on input or I/O pins is $V_{CC}f$ + 0.3 V or $V_{CC}s$ + 0.3 V. During voltage transitions, input or I/O pins may overshoot to $V_{CC}f$ + 1.0 V or $V_{CC}s$ + 1.0 V for periods of up to 5 ns.

*3 : Minimum DC input voltage on $\overline{RESET}$ pin is –0.5 V. During voltage transitions, $\overline{RESET}$ pin may undershoot V_{SS} to –2.0 V for periods of up to 20 ns.
Voltage difference between input and supply voltage (V_{IN}-$V_{CC}f$ or $V_{CC}s$) does not exceed 9.0 V.
Maximum DC input voltage on $\overline{RESET}$ pin is +13.0 V which may overshoot to +14.0 V for periods of up to 20 ns.

*4 : Minimum DC input voltage on $\overline{WP}$/ACC pin is –0.5 V. During voltage transitions, $\overline{WP}$/ACC pin may undershoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC input voltage on $\overline{WP}$/ACC pin is +10.5 V which may overshoot to +10.5 V for periods of up to 20 ns, When $V_{CC}f$ is applied.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value		Unit
		Min	Max	
Ambient Temperature	T_A	–30	+85	°C
$V_{CC}f$ Supply Voltages	$V_{CC}f$	+2.7	+3.3	V
$V_{CC}s$ Supply Voltages	$V_{CC}s$	+2.7	+3.0	V

Notes : • Voltage is defined on the basis of V_{SS} = GND = 0 V.
• Operating ranges define those limits between which the functionality of the device is guaranteed.
• $V_{CC}s$ can be 2.4 V minimum during standby state.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ DC CHARACTERISTICS

Parameter	Symbol	Test Conditions		Value			Unit
				Min	Typ	Max	
Input Leakage Current	I_{LI}	V_{IN} = V_{SS} to V_{CC}, V_{CC} = V_{CC} Max		–1.0	—	+1.0	µA
Output Leakage Current	I_{LO}	V_{OUT} = V_{SS} to V_{CC}, V_{CC} = V_{CC} Max		–1.0	—	+1.0	µA
$\overline{RESET}$ Inputs Leakage Current	I_{LIT}	V_{CC} = V_{CC} Max, $\overline{RESET}$ = 12.5 V		—	—	35	µA
Flash V_{CC} Active Current (Read) *1	$I_{CC1}f$	$\overline{CE}f$ = V_{IL}, $\overline{OE}$ = V_{IH}	t_{CYCLE} = 5 MHz	—	—	18	mA
			t_{CYCLE} = 1 MHz	—	—	7	mA
Flash V_{CC} Active Current (Program/Erase) *2	$I_{CC2}f$	$\overline{CE}f$ = V_{IL}, $\overline{OE}$ = V_{IH}		—	—	40	mA
Flash V_{CC} Active Current (Read-While-Program) *5	$I_{CC3}f$	$\overline{CE}f$ = V_{IL}, $\overline{OE}$ = V_{IH}		—	—	58	mA
Flash V_{CC} Active Current (Read-While-Erase) *5	$I_{CC4}f$	$\overline{CE}f$ = V_{IL}, $\overline{OE}$ = V_{IH}		—	—	58	mA
Flash V_{CC} Active Current (Erase-Suspend-Program)	$I_{CC5}f$	$\overline{CE}f$ = V_{IL}, $\overline{OE}$ = V_{IH}		—	—	40	mA
FCRAM V_{CC} Active Current	$I_{CC1}s$	$V_{CC}s$ = $V_{CC}s$ Max, $\overline{CE}1s$ = V_{IL}, CE2s = V_{IH}, V_{IN} = V_{IH} or V_{IL}, I_{OUT} = 0 mA	t_{RC}/t_{WC} = Min	—	15	20	mA
			t_{RC}/t_{WC} = Max	—	2.5	3.0	
Flash V_{CC} Standby Current	$I_{SB1}f$	$V_{CC}f$ = V_{CC} Max, $\overline{CE}f$ = $V_{CC}f$ ± 0.3 V $\overline{RESET}$ = $V_{CC}f$ ± 0.3 V, $\overline{WP}$/A_{CC} = $V_{CC}f$ ± 0.3 V		—	1	5	µA
Flash V_{CC} Standby Current ($\overline{RESET}$)	$I_{SB2}f$	$V_{CC}f$ = V_{CC} Max, $\overline{RESET}$ = V_{SS} ± 0.3 V, $\overline{WP}$/A_{CC} = $V_{CC}f$ ± 0.3 V		—	1	5	µA
Flash V_{CC} Current (Automatic Sleep Mode) *3	$I_{SB3}f$	$V_{CC}f$ = V_{CC} Max, $\overline{CE}f$ = V_{SS} ± 0.3 V $\overline{RESET}$ = $V_{CC}f$ ± 0.3 V, $\overline{WP}$/A_{CC} = $V_{CC}f$ ± 0.3 V V_{IN} = $V_{CC}f$ ± 0.3 V or V_{SS} ± 0.3 V		—	1	5	µA
FCRAM V_{CC} Standby Current	$I_{SB}s$	$V_{CC}s$ = $V_{CC}s$ Max, $\overline{CE}1s$ ≥ $V_{CC}s$ – 0.2 V, CE2s ≥ $V_{CC}s$ – 0.2V, V_{IN} ≤ 0.2 V or $V_{CC}s$ – 0.2 V		—	80	100	µA
FCRAM V_{CC} Power Down Current	$I_{PD}s$	$V_{CC}s$ = $V_{CC}s$ Max, V_{IN} ≥ $V_{CC}f$ – 0.2 V or V_{IN} ≤ 0.2 V $\overline{CE}1s$ ≤ 0.2V, CE2s ≤ 0.2V, I_{OUT} = 0 mA		—	—	10	µA

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Parameter	Symbol	Test Conditions		Value			Unit
				Min	Typ	Max	
Input Low Level	V_{IL}	—		–0.3	—	0.4	V
Input High Level	V_{IH}	—	Flash	2.0	—	V_{CC} + 0.3	V
			FCRAM	2.3			
Voltage for Autoselect and Sector Protection ($\overline{RESET}$) *4	V_{ID}	—		11.5	—	12.5	V
Voltage for $\overline{WP}$/ACC Sector Protection/Unprotection and Program Acceleration	V_{ACC}	—		8.5	9.0	9.5	V
FCRAM Output Low Level	V_{OL}	V_{CCS} = V_{CCS} Min, I_{OL} = 1.0 mA		—	—	0.4	V
FCRAM Output High Level	V_{OH}	V_{CCS} = V_{CCS} Min, I_{OH} = –0.5 mA		1.8	—	—	V
Flash Output Low Level	V_{OL}	V_{CCf} = V_{CCf} Min, I_{OL} = 4.0 mA		—	—	0.45	V
Flash Output High Level	V_{OH}	V_{CCf} = V_{CCf} Min, I_{OH} = –0.1 mA		V_{CCf} – 0.4	—	—	V
Low V_{CC} Lock-Out Voltage	V_{LKO}	—		2.3	—	2.5	V

*1 : The I_{CC} current listed includes both the DC operating current and the frequency dependent component.

*2 : I_{CC} active while Embedded Algorithm (program or erase) is in progress.

*3 : Automatic sleep mode enables the low power mode when the address remains stable for 150 ns.

*4 : Applicable for only V_{CC} applying.

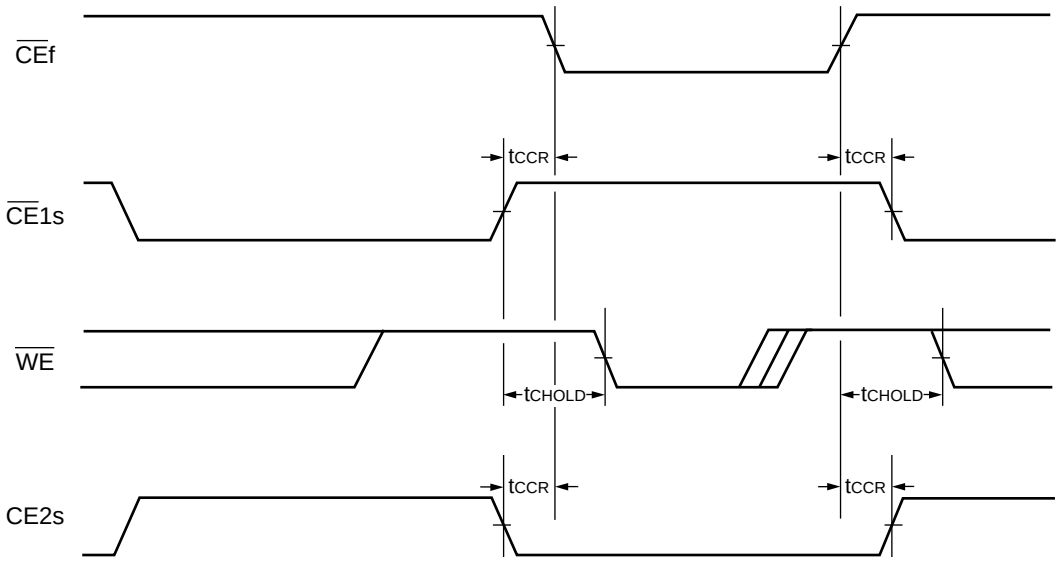
*5 : Embedded Algorithm (program or erase) is in progress. (@5 MHz)

■ AC CHARACTERISTICS

- **$\overline{CE}$ Timing**

Parameter	Symbol		Test Setup	Value	Unit
	JEDEC	Standard		Min	
$\overline{CE}$ Recover Time	—	t_{CCR}	—	0	ns
$\overline{CE}$ Hold Time	—	t_{CHOLD}	—	3	ns

- **Timing Diagram for alternating FCRAM to Flash**

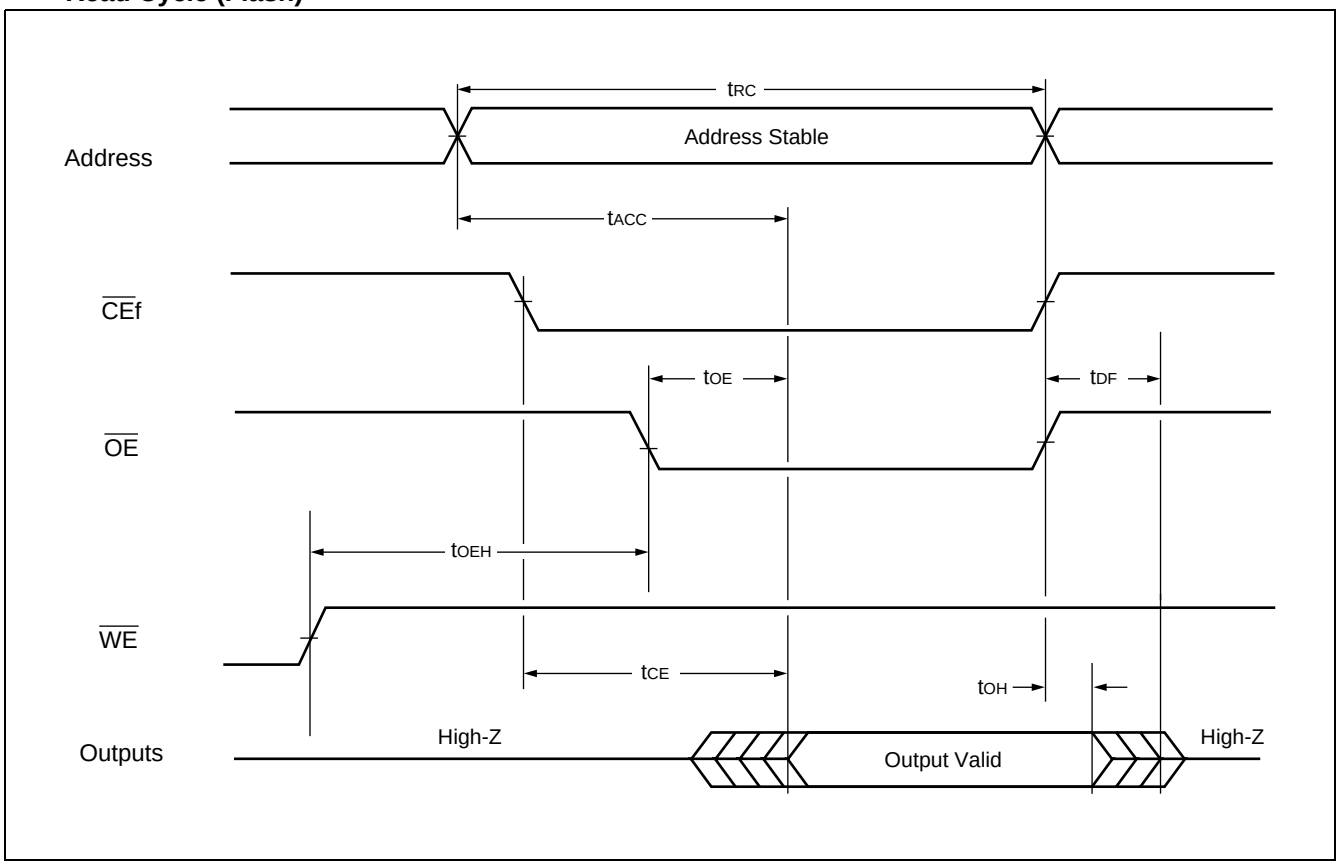


- **Read Only Operations Characteristics (Flash)**

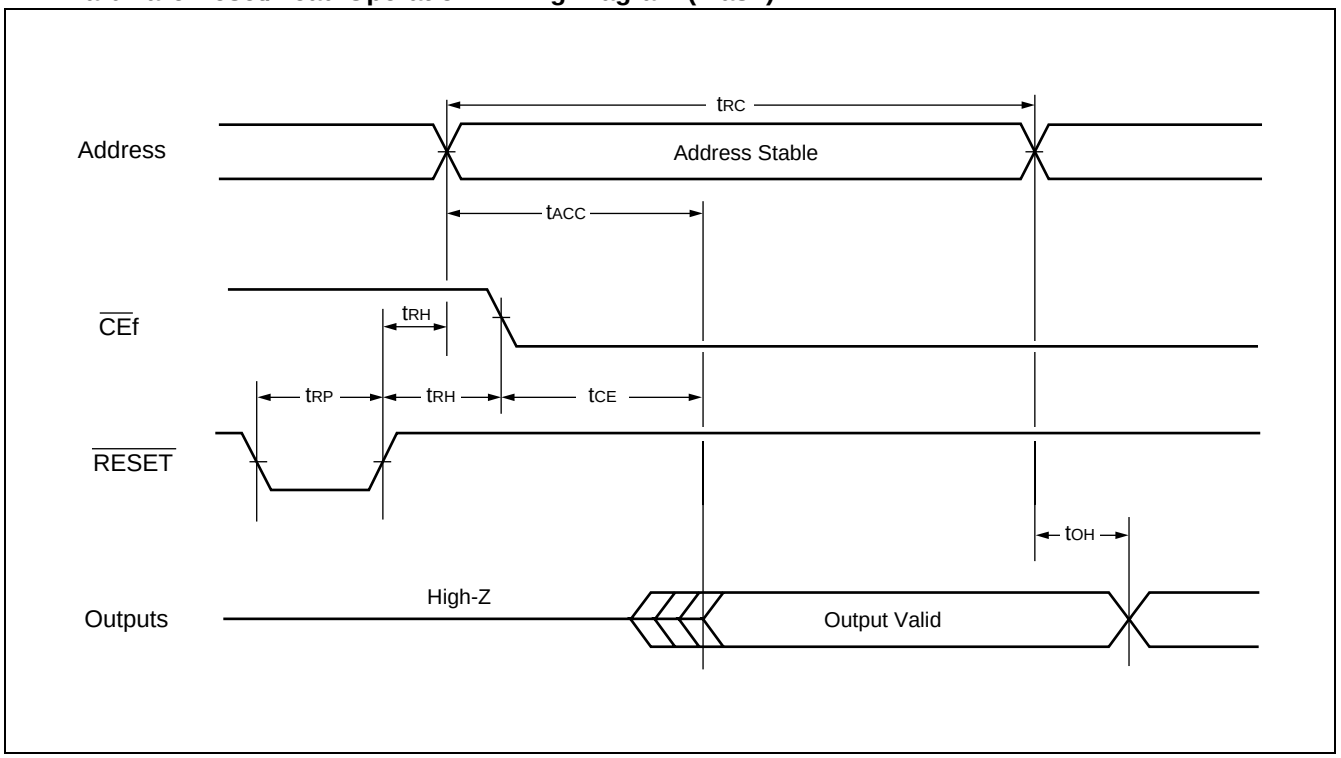
Parameter	Symbol		Test Setup	-85		Unit
	JEDEC	Standard		Min	Max	
Read Cycle Time	t_{AVAV}	t_{RC}	—	85	—	ns
Address to Output Delay	t_{AVQV}	t_{ACC}	$\overline{CE}f = V_{IL}$ $\overline{OE} = V_{IL}$	—	85	ns
Chip Enable to Output Delay	t_{ELQV}	t_{CE}	$\overline{OE} = V_{IL}$	—	85	ns
Output Enable to Output Delay	t_{GLQV}	t_{OE}	—	—	35	ns
Chip Enable to Output High-Z	t_{EHQZ}	t_{DF}	—	—	30	ns
Output Enable to Output High-Z	t_{GHQZ}	t_{DF}	—	—	30	ns
Output Hold Time From Addresses, $\overline{CE}f$ or $\overline{OE}$, Whichever Occurs First	t_{AXQX}	t_{OH}	—	0	—	ns
$\overline{RESET}$ Pin Low to Read Mode	—	t_{READY}	—	—	20	µs
$\overline{CE}f$ Switching Low or High	—	t_{ELFL} t_{ELFH}	—	—	5	ns

Test Conditions : Output Load : 1 TTL gate and 30 pF
Input rise and fall times : 5 ns
Input pulse levels : 0.0 V or $V_{CC}f$
Timing measurement reference level
Input : $0.5 \times V_{CC}f$
Output : $0.5 \times V_{CC}f$

- **Read Cycle (Flash)**



- **Hardware Reset/Read Operation Timing Diagram (Flash)**



- **Erase/Program Operations (Flash)**

Parameter		Symbol		Value			Unit
				-85			
		JEDEC	Standard	Min	Typ	Max	
Write Cycle Time		t_{AVAV}	t_{WC}	85	—	—	ns
Address Setup Time ($\overline{WE}$ to Addr.)		t_{AVWL}	t_{AS}	0	—	—	ns
Address Setup Time to $\overline{CE}$f Low During Toggle Bit Polling		—	t_{ASO}	15	—	—	ns
Address Hold Time ($\overline{WE}$ to Addr.)		t_{WLAX}	t_{AH}	45	—	—	ns
Address Hold Time from $\overline{CE}$f or $\overline{OE}$ High During Toggle Bit Polling		—	t_{AHT}	0	—	—	ns
Data Setup Time		t_{DVWH}	t_{DS}	35	—	—	ns
Data Hold Time		t_{WHDX}	t_{DH}	0	—	—	ns
Output Enable Hold Time	Read	—	t_{OEH}	0	—	—	ns
	Toggle and $\overline{Data}$ Polling			10	—	—	ns
$\overline{CE}$f High During Toggle Bit Polling		—	t_{CEPH}	20	—	—	ns
$\overline{OE}$ High During Toggle Bit Polling		—	t_{OEPH}	20	—	—	ns
Read Recover Time Before Write ($\overline{OE}$ to $\overline{CE}$f)		t_{GHEL}	t_{GHEL}	0	—	—	ns
Read Recover Time Before Write ($\overline{OE}$ to $\overline{WE}$)		t_{GHWL}	t_{GHWL}	0	—	—	ns
$\overline{WE}$ Setup Time ($\overline{CE}$f to $\overline{WE}$)		t_{WLEL}	t_{WS}	0	—	—	ns
$\overline{CE}$f Setup Time ($\overline{WE}$ to $\overline{CE}$f)		t_{ELWL}	t_{CS}	0	—	—	ns
$\overline{WE}$ Hold Time ($\overline{CE}$f to $\overline{WE}$)		t_{EHWH}	t_{WH}	0	—	—	ns
$\overline{CE}$f Hold Time ($\overline{WE}$ to $\overline{CE}$f)		t_{WHEH}	t_{CH}	0	—	—	ns
Write Pulse Width		t_{WLWH}	t_{WP}	35	—	—	ns
$\overline{CE}$f Pulse Width		t_{ELEH}	t_{CP}	35	—	—	ns
Write Pulse Width High		t_{WHWL}	t_{WPH}	30	—	—	ns
$\overline{CE}$f Pulse Width High		t_{EHEL}	t_{CPH}	30	—	—	ns
Word Programming Operation		t_{WHWH1}	t_{WHWH1}	—	16	—	µs
Sector Erase Operation*1		t_{WHWH2}	t_{WHWH2}	—	1	—	s
V_{CC}f Setup Time		—	t_{VCS}	50	—	—	µs
Voltage Transition Time*2		—	t_{VLHT}	4	—	—	µs
Rise Time to V_{ID}*2		—	t_{VIDR}	500	—	—	ns
Rise Time to V_{ACC}		—	t_{VACCR}	500	—	—	ns
Recover Time from RY/$\overline{BY}$		—	t_{RB}	0	—	—	ns
$\overline{RESET}$ Pulse Width		—	t_{RP}	500	—	—	ns
Delay Time from Embedded Output Enable		—	t_{EOE}	—	—	85	ns
$\overline{RESET}$ High Level Period Before Read		—	t_{RH}	200	—	—	ns
Program/Erase Valid to RY/$\overline{BY}$ Delay		—	t_{BUSY}	—	—	90	ns
Erase Time-out Time*3		—	t_{TOW}	50	—	—	µs
Erase Suspend Transition Time*4		—	t_{SPD}	—	—	20	µs

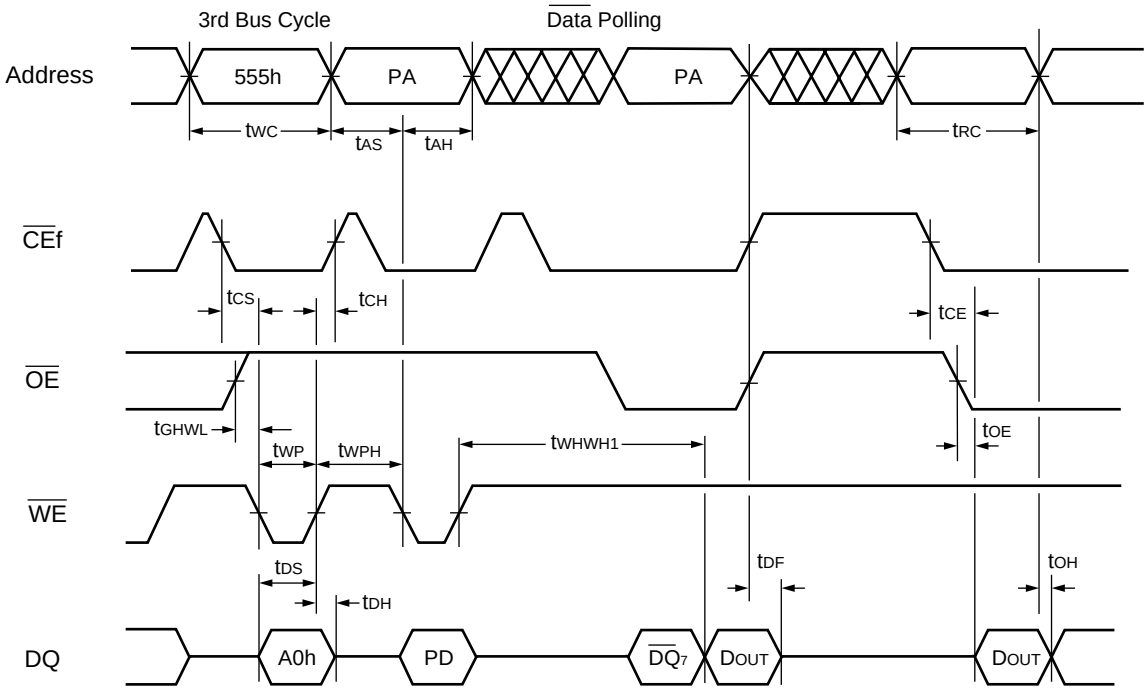
*1 : Does not include the preprogramming time.

*2 : For Sector Group Protection Operation.

*3 : The time between writes must be less than “t_{TOW}” otherwise that command will not be accepted and erasure will start. A time-out or “t_{TOW}” from the rising edge of last $\overline{CE}$f or $\overline{WE}$ whichever happens first will initiate the execution of the Sector Erase command (s) .

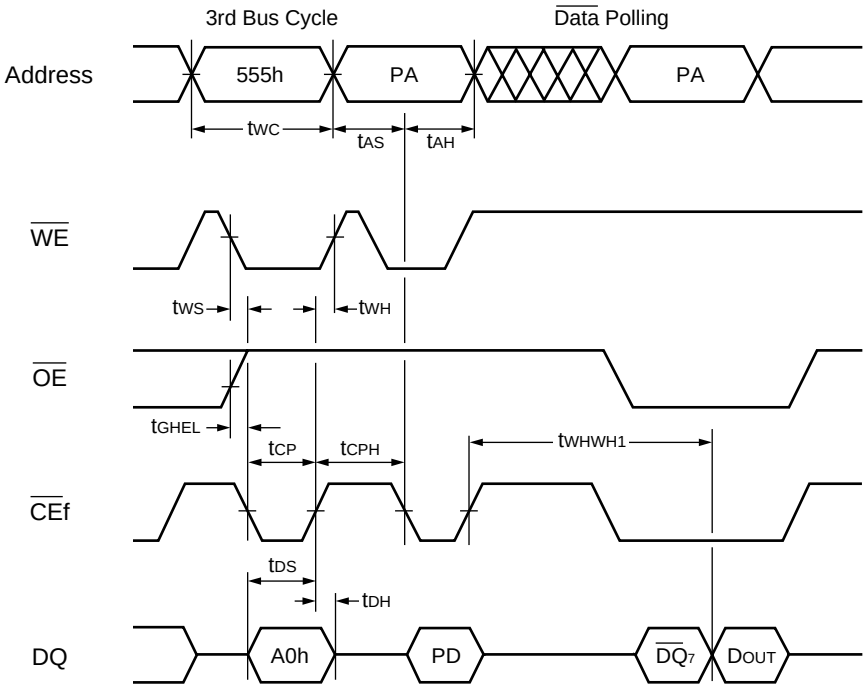
*4 : When the Erase Suspend command is written during the Sector Erase operation, the device will take maximum of “t_{SPD}” to suspend the erase operation.

- **Write Cycle ($\overline{WE}$ control) (Flash)**



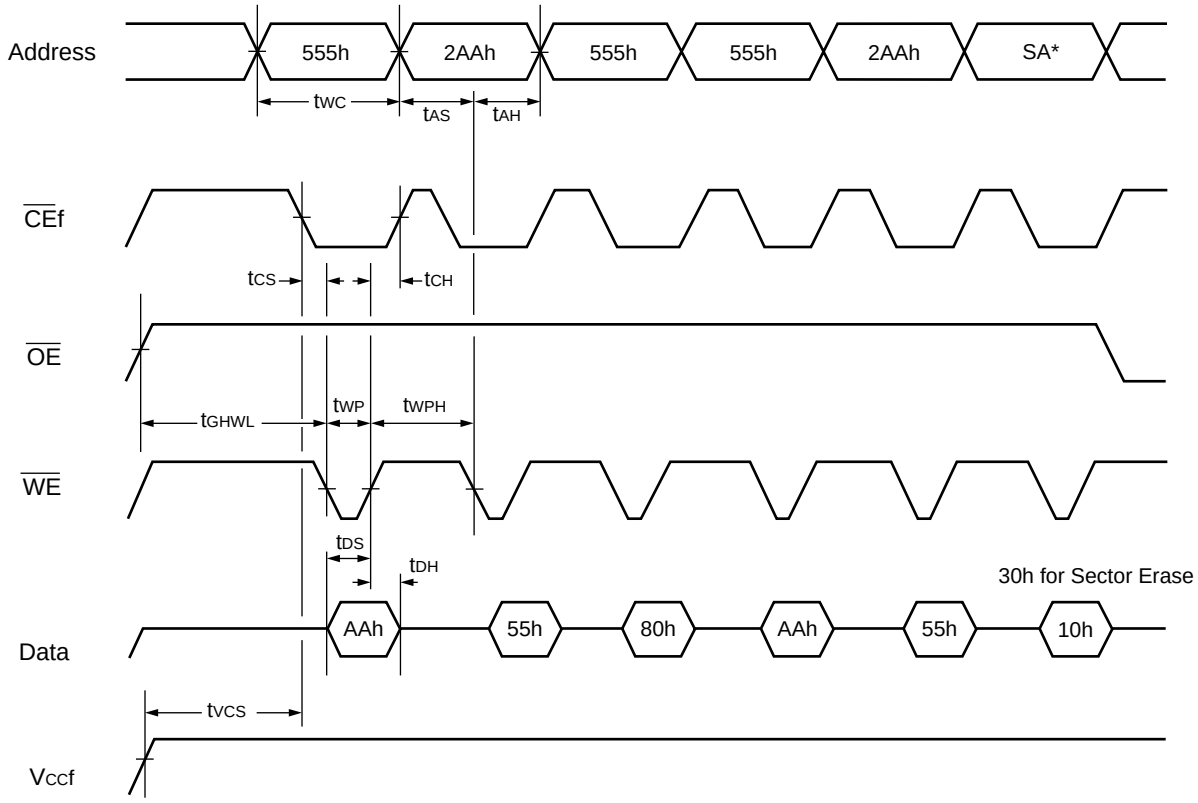
Notes :
- PA is address of the memory location to be programmed.
- PD is data to be programmed at word address.
- $\overline{DQ_7}$ is the output of the complement of the data written to the device.
- D_{OUT} is the output of the data written to the device.
- Figure indicates the last two bus cycles out of four bus cycle sequence.

- **Write Cycle ($\overline{CE}$f control) (Flash)**



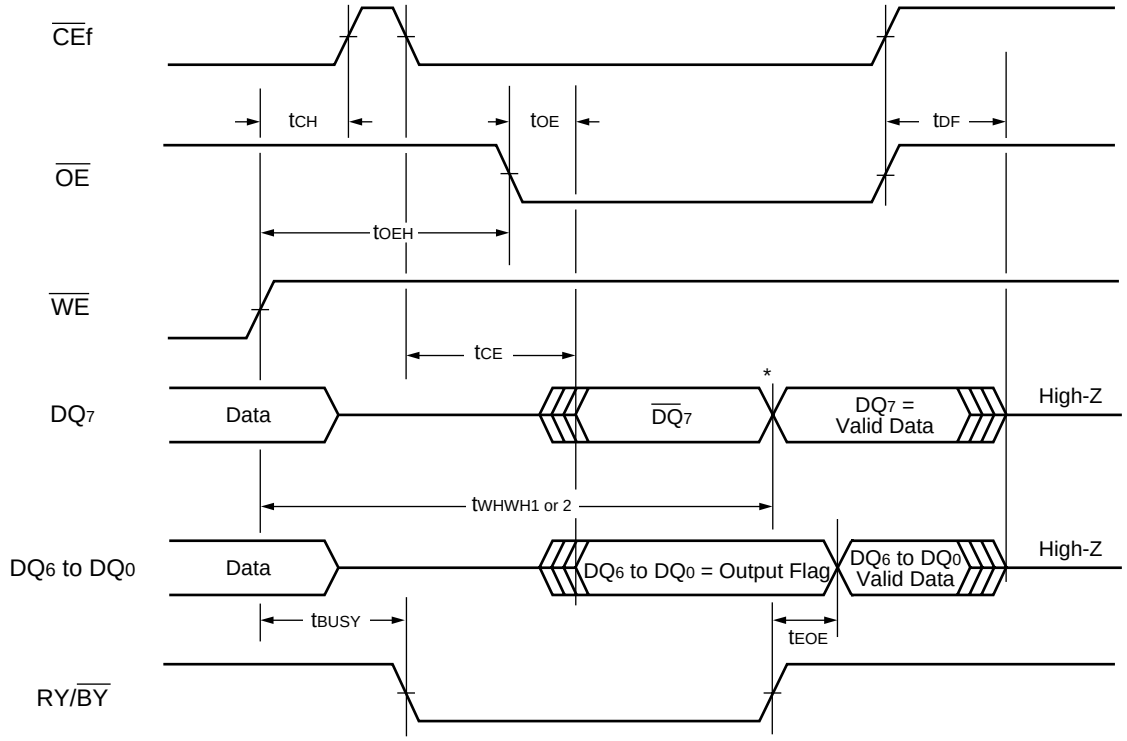
Notes :
- PA is address of the memory location to be programmed.
- PD is data to be programmed at word address.
- $\overline{DQ}_7$ is the output of the complement of the data written to the device.
- D_{OUT} is the output of the data written to the device.
- Figure indicates the last two bus cycles out of four bus cycle sequence.

- **AC Waveforms Chip/Sector Erase Operations (Flash)**



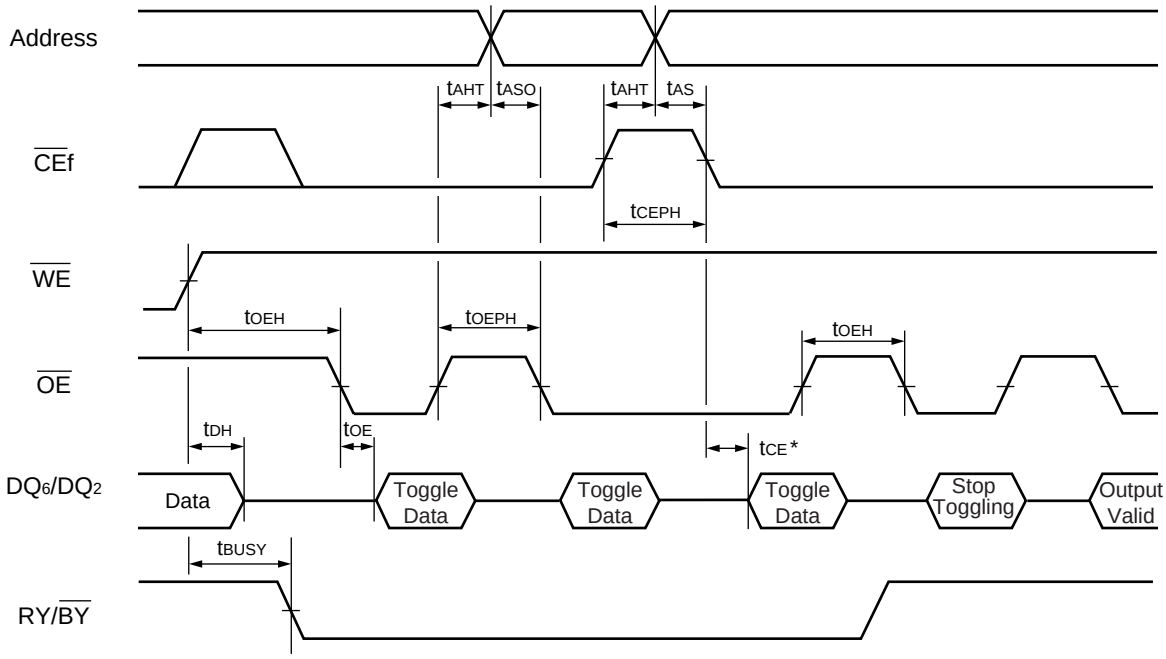
* : SA is the sector address for Sector Erase. Addresses = 555h for Chip Erase.

- **AC Waveforms for $\overline{\text{Data}}$ Polling during Embedded Algorithm Operations (Flash)**



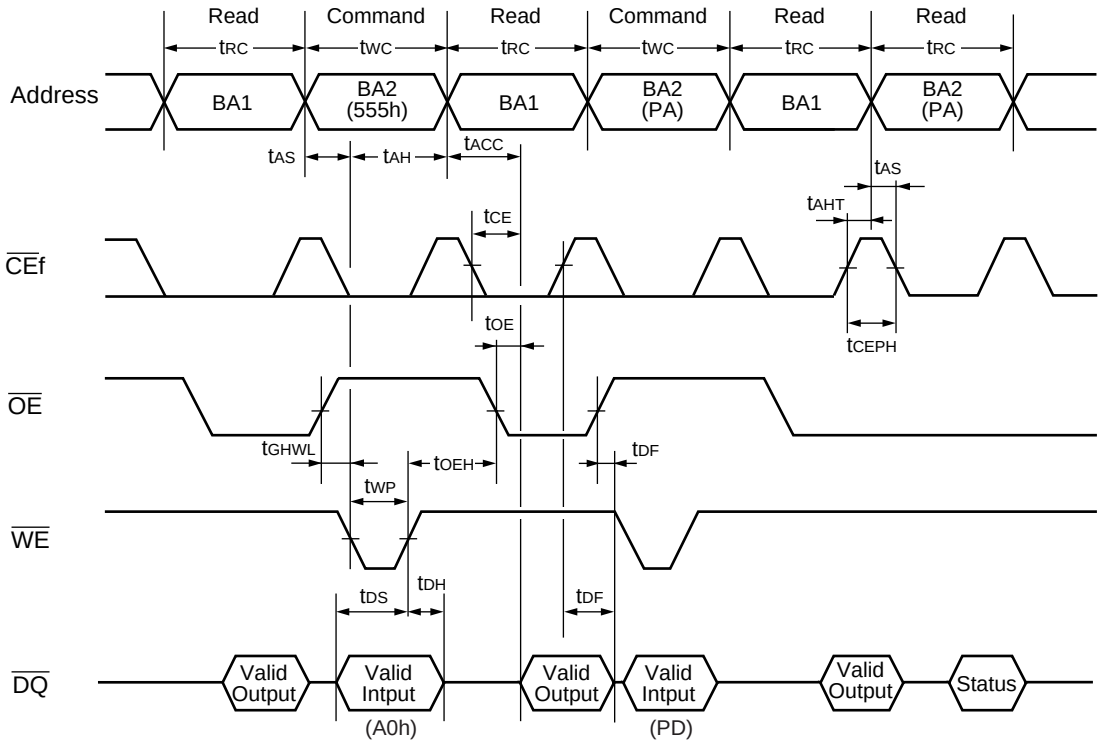
* : DQ_7 = Valid Data (the device has completed the Embedded operation) .

- **AC Waveforms for Toggle Bit during Embedded Algorithm Operations (Flash)**



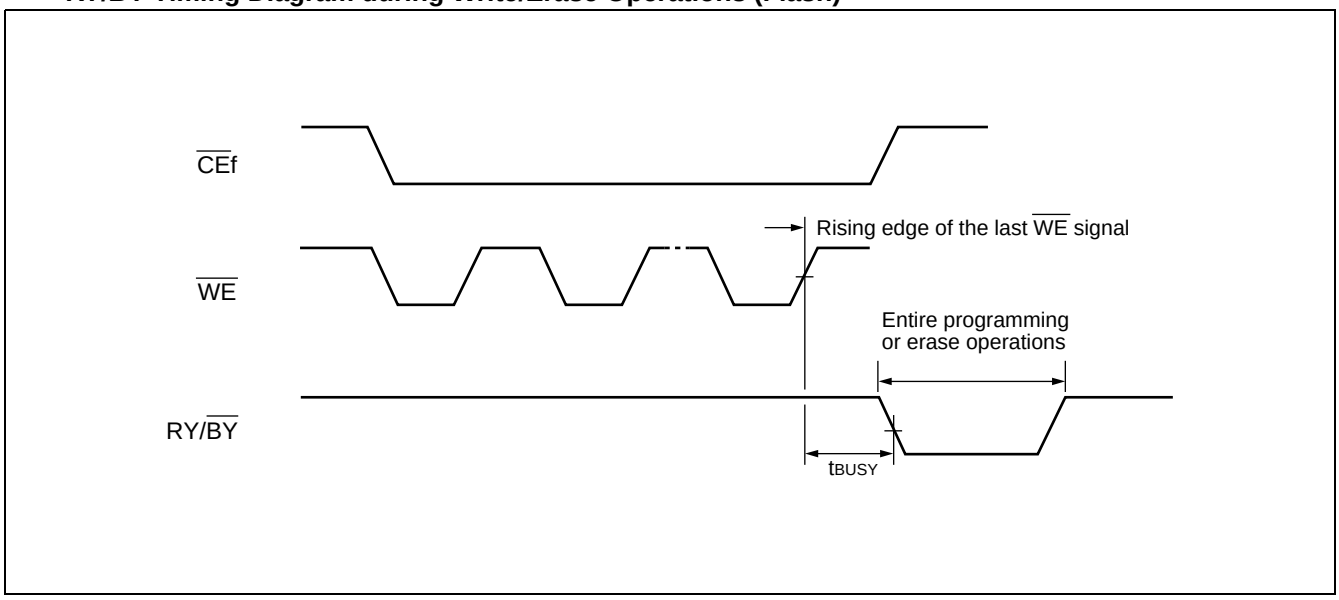
* : DQ_6 stops toggling (the device has completed the Embedded operation) .

- **Bank-to-Bank Read/Write Timing Diagram (Flash)**

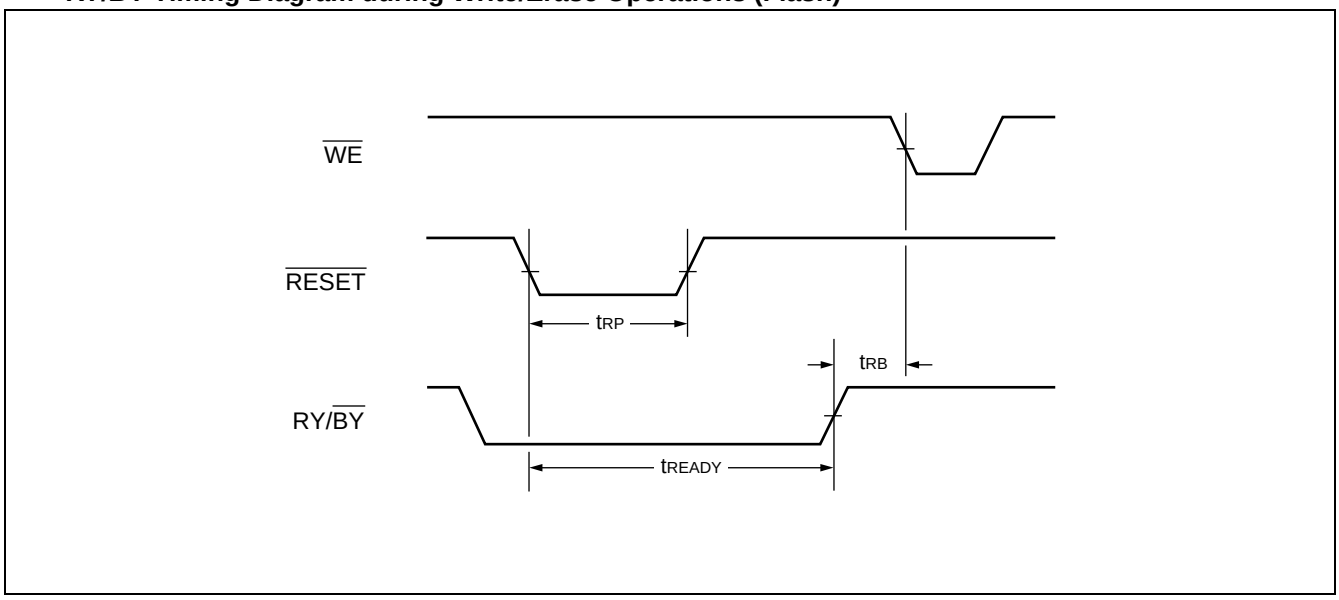


Note : This is example of Read for Bank 1 and Embedded Algorithm (program) for Bank 2.
BA1 : Address corresponding to Bank 1.
BA2 : Address corresponding to Bank 2.

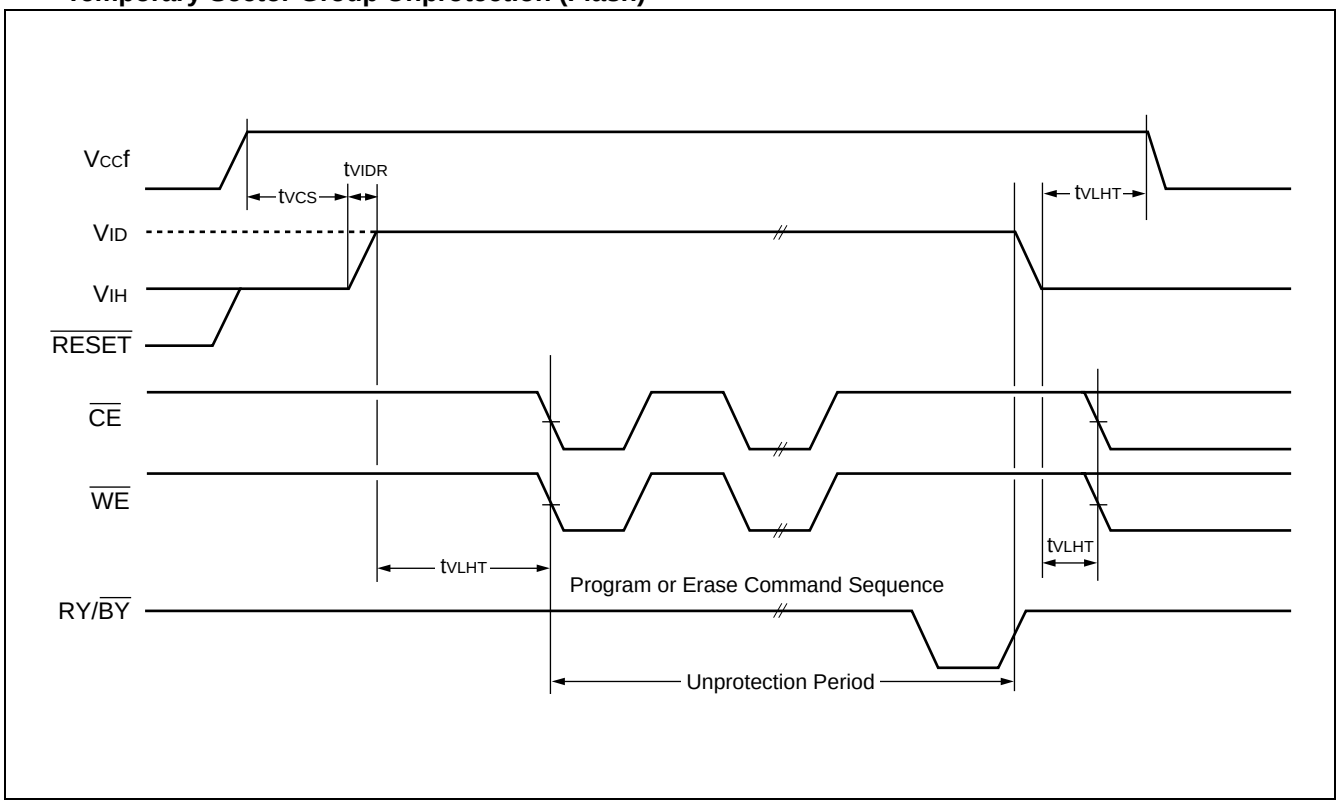
- **RY/$\overline{BY}$ Timing Diagram during Write/Erase Operations (Flash)**



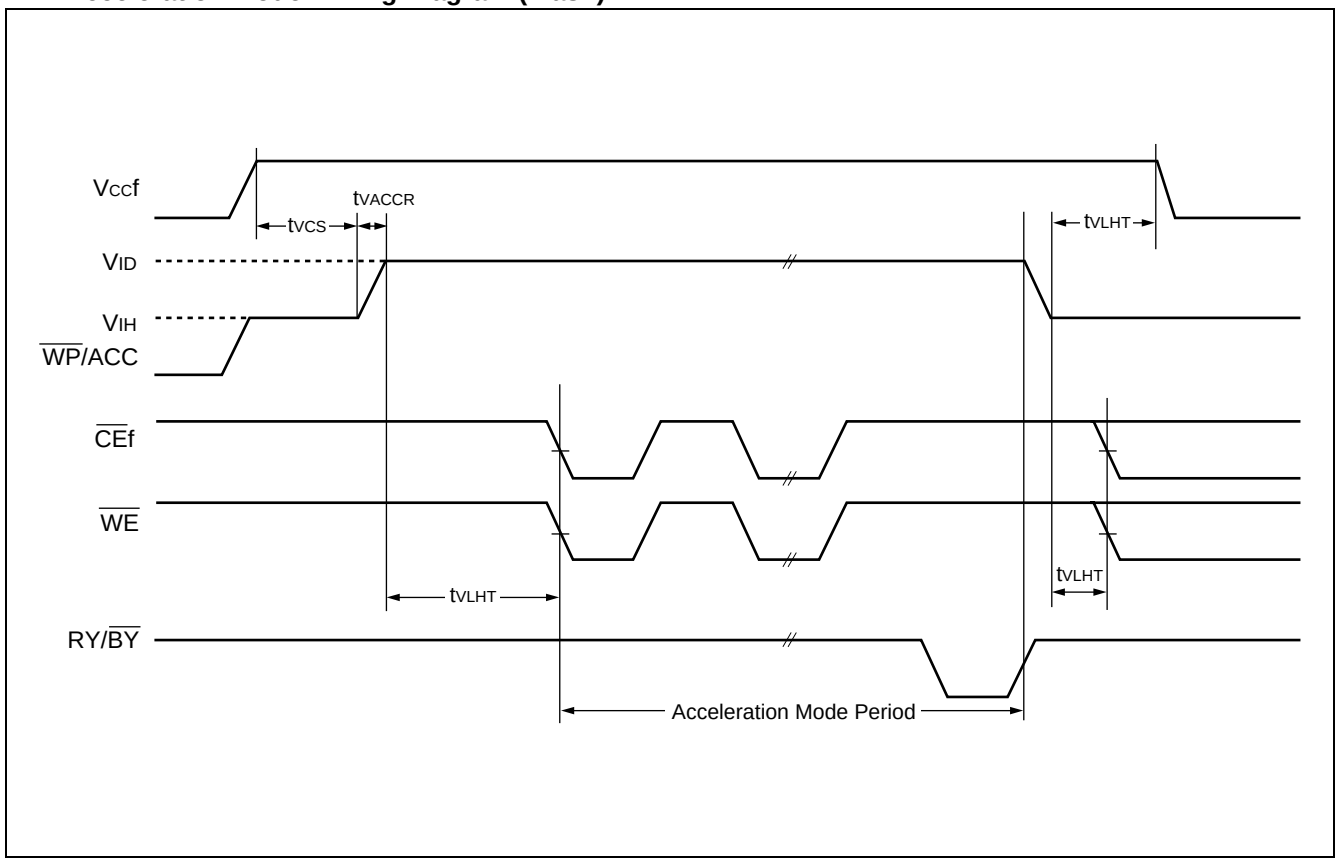
- **RY/$\overline{BY}$ Timing Diagram during Write/Erase Operations (Flash)**



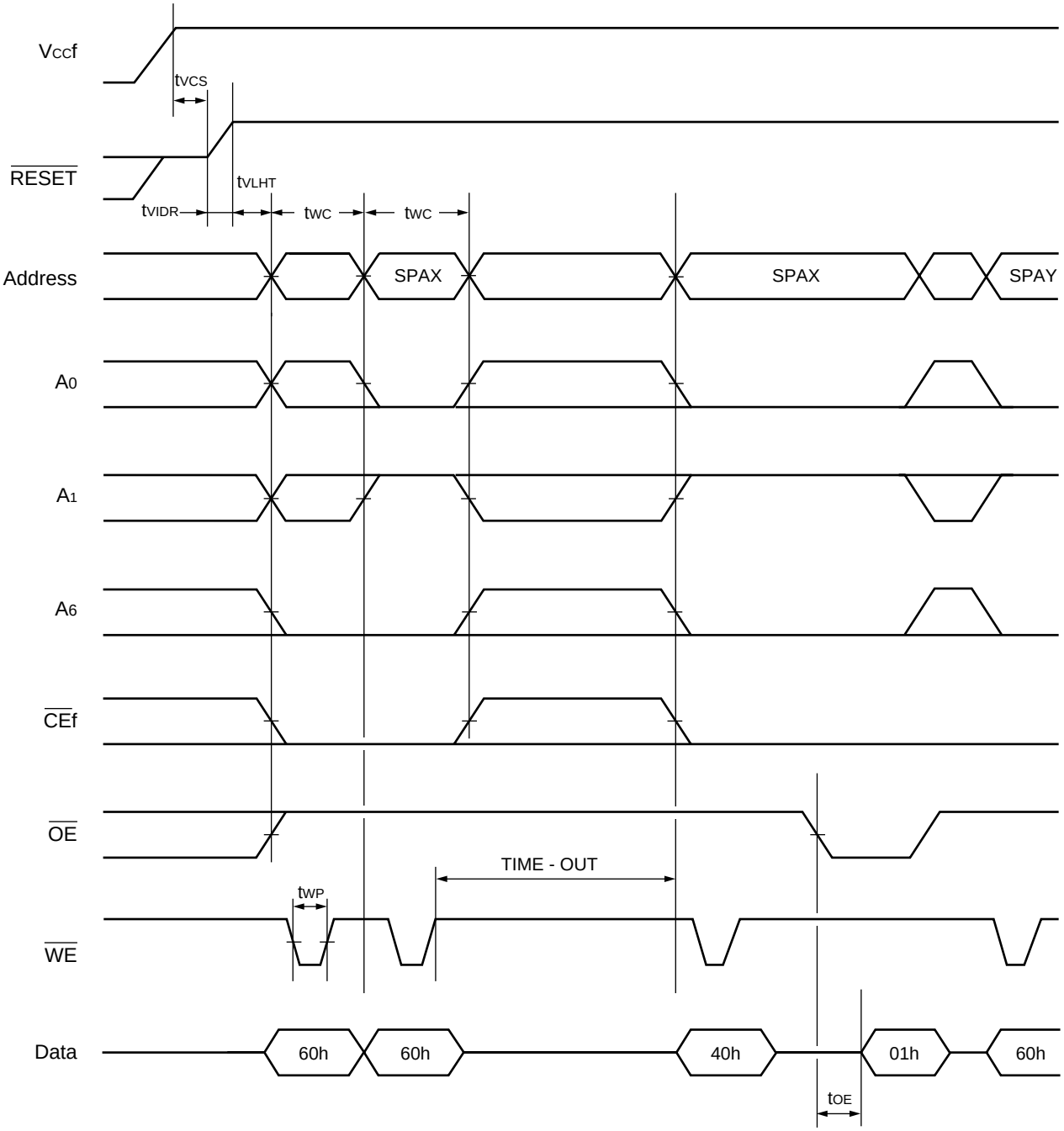
• **Temporary Sector Group Unprotection (Flash)**



• **Acceleration Mode Timing Diagram (Flash)**



- **Extended Sector Group Protection (Flash)**



SPAX : Sector Group Address to be protected
SPAY : Next Sector Group Address to be protected
TIME-OUT : Time-Out window = 250 µs (Min)

- **READ Cycle (FCRAM)**

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Read Cycle Time	t_{RC}	90	1000	ns	*1
Address Setup Time at $\overline{CE}$1s High to Low Transition	t_{ASC}	–5	—	ns	
Address Hold Time during $\overline{CE}$1s Low	t_{AHC}	90	—	ns	*2
Address Access Time	t_{AA}	—	85	ns	*3
Chip Enable Access Time	t_{CE}	—	85	ns	*3
Output Enable Access Time	t_{OE}	—	60	ns	*3
Output Data Hold Time	t_{OH}	5	—	ns	*3
$\overline{CE}$1s Low to Output Low-Z	t_{CLZ}	10	—	ns	*4
$\overline{OE}$ Low to Output Low-Z	t_{OLZ}	0	—	ns	*4
$\overline{CE}$1s High to Output High-Z	t_{CHZ}	—	25	ns	*4
$\overline{OE}$ High to Output High-Z	t_{OHZ}	—	15	ns	*4
$\overline{CE}$1s High Pulse Width	t_{CP}	10	—	ns	
$\overline{CE}$1s High to Address Hold Time	t_{CHAH}	–5	—	ns	*5
Address Invalid Time during Read ($\overline{CE}$1s = Low)	t_{AX}	—	10	ns	

*1 : Maximum value is a reference and is applied to Output Disable condition.

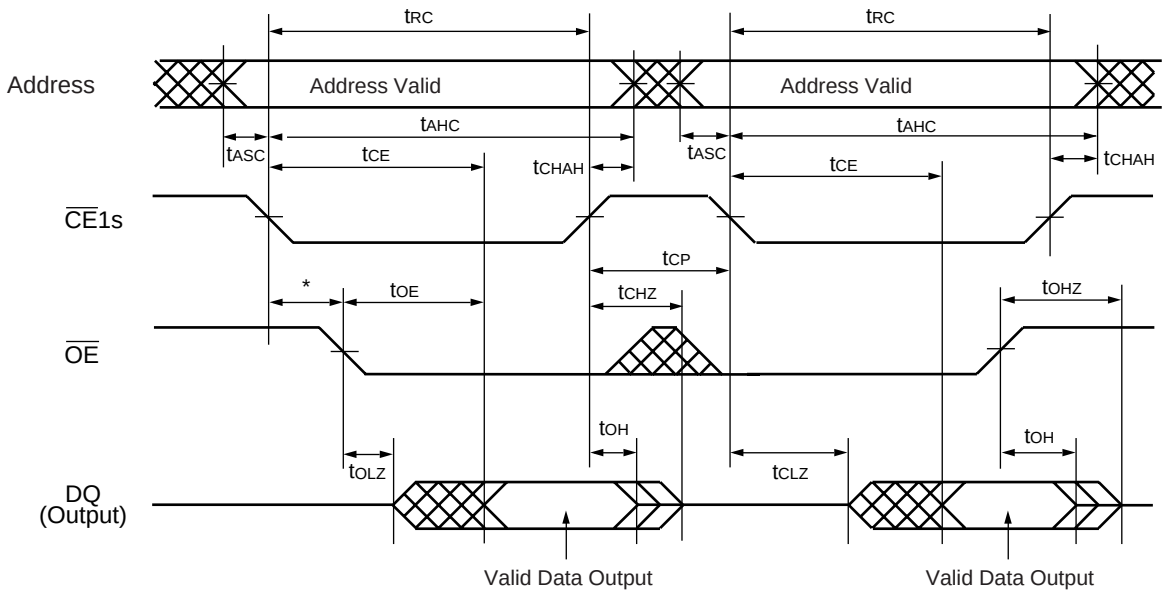
*2 : t_{AHC} must be satisfied every address valid state after t_{AX} during $\overline{CE}$1s = Low.

*3 : Output load is 30 pF.

*4 : Output load is 5 pF.

*5 : If actual address change before $\overline{CE}$1s High transition is earlier than t_{CHAH} (min) , t_{CP} ($\overline{CE}$1s High period) should be kept at least t_{RC} (min) period.

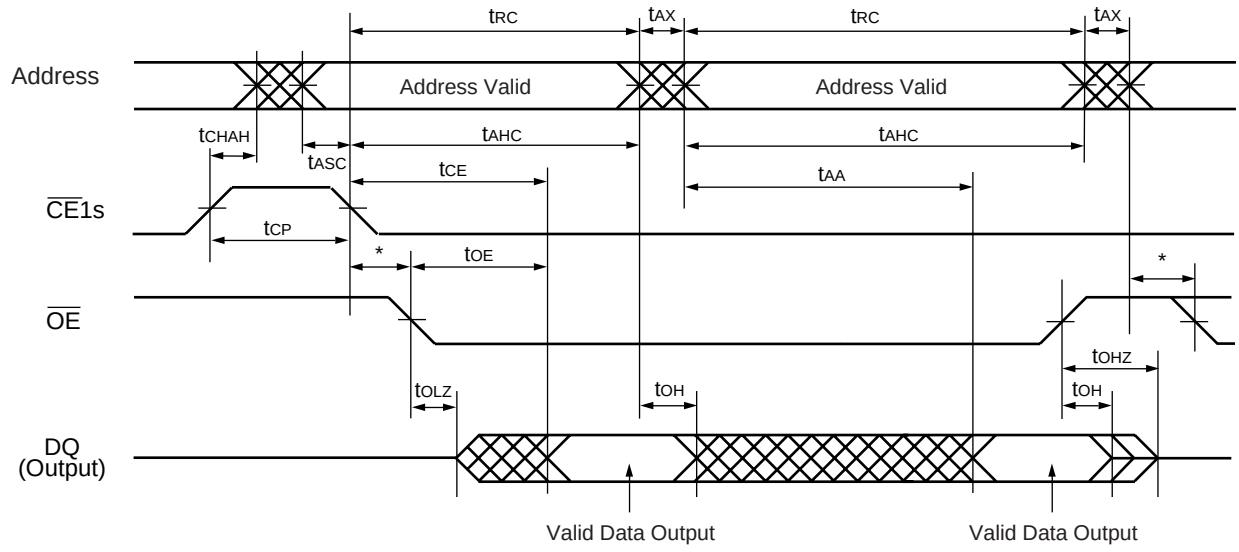
- **READ Timing 1 ($\overline{CE}$1s Control) (FCRAM)**



Note : CE2s and $\overline{WE}$ must be HIGH for entire read cycle.

* : Output Disable condition before new Read data valid should not be kept longer than 1 µs.

- **READ Timing 2 (Address Access) (FCRAM)**



Note : CE2s and $\overline{WE}$ must be HIGH for entire read cycle.

* : Output Disable condition before new Read data valid should not be kept longer than 1 µs.

- **WRITE Cycle (FCRAM)**

Parameter	Symbol	Value		Unit	Re-marks
		Min	Max		
Write Cycle Time	t_{WC}	90	1000	ns	*1
Address Setup Time	t_{AS}	0	—	ns	
Address Hold Time	t_{AH}	40	—	ns	
$\overline{CE}$1s Write Setup Time	t_{CS}	0	1000	ns	*2
$\overline{CE}$1s Write Hold Time	t_{CH}	0	1000	ns	*2
$\overline{WE}$, $\overline{LB}$s, $\overline{UB}$s Setup Time	t_{BS}	0	—	ns	
$\overline{WE}$, $\overline{LB}$s, $\overline{UB}$s Hold Time	t_{BH}	0	—	ns	
$\overline{OE}$ Setup Time	t_{OES}	0	—	ns	
$\overline{OE}$ Hold Time	t_{OEH}	15	—	ns	
$\overline{OE}$ High to $\overline{CE}$1s Low Setup Time	t_{OHCL}	–5	—	ns	*3
$\overline{OE}$ High to Address Hold Time	t_{OHAH}	0	—	ns	*4
$\overline{CE}$1s Write Pulse Width	t_{CW}	60	—	ns	*5, *6
$\overline{WE}$ Write Pulse Width	t_{WP}	60	—	ns	*5, *6
$\overline{CE}$1s Write Recovery Time	t_{WRC}	15	—	ns	*7
$\overline{WE}$ Write Recovery Time	t_{WR}	15	1000	ns	*2, *7
Data Setup Time	t_{DS}	20	—	ns	
Data Hold Time	t_{DH}	10	—	ns	
$\overline{CE}$1s Low to Output in Low-Z	t_{CLZ}	10	—	ns	*8
$\overline{OE}$ Low to Output in Low-Z	t_{OLZ}	0	—	ns	*8

*1 : Maximum value is a reference and applied to Output Disable condition.

*2 : Maximum value is applied to Output Disable condition.

*3 : t_{OHCL} (min) must be satisfied if read operation is not performed prior to write operation.
In case $\overline{OE}$ is disabled after t_{OHCL} (min), $\overline{WE}$ Low must be asserted after t_{RC} (min) from $\overline{CE}$1s Low.

*4 : Applicable if $\overline{CE}$1s stays Low after read operation.

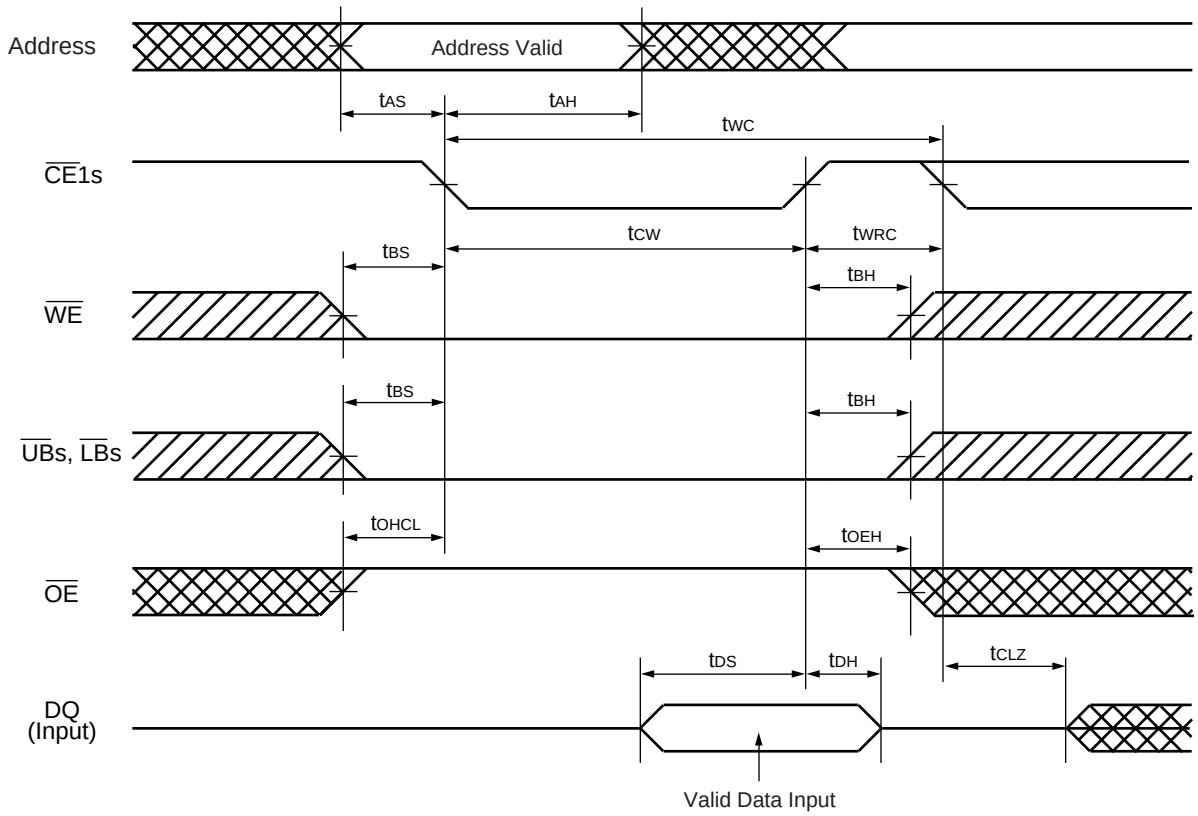
*5 : t_{WHP} (max) must be satisfied for the high pulse noise.

*6 : t_{CW} and t_{WP} are applied if write operation is initiated by $\overline{CE}$1s and $\overline{WE}$, respectively.

*7 : t_{WRC} and t_{WR} are applied if write pulse is terminated by $\overline{CE}$1s and $\overline{WE}$, respectively.

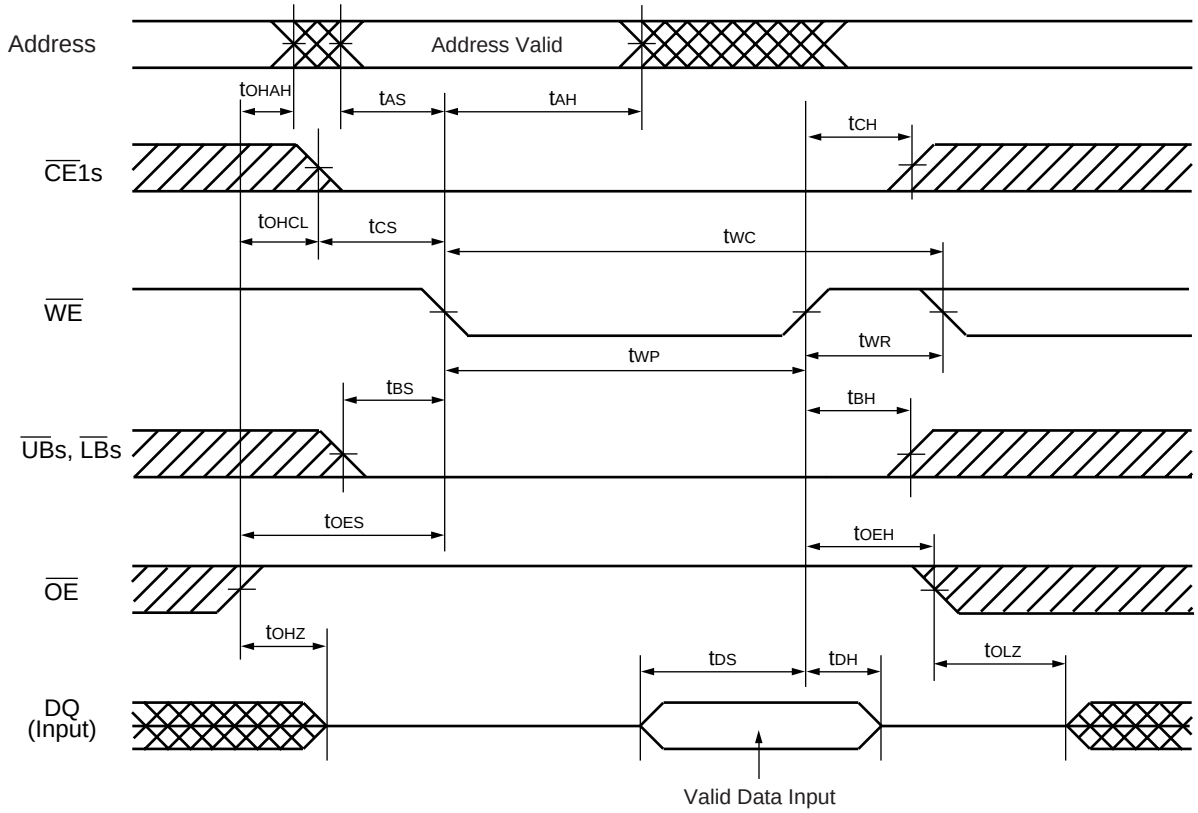
*8 : Output load is 5 pF.

- **WRITE Timing 1 ($\overline{CE}$1s Control) (FCRAM)**



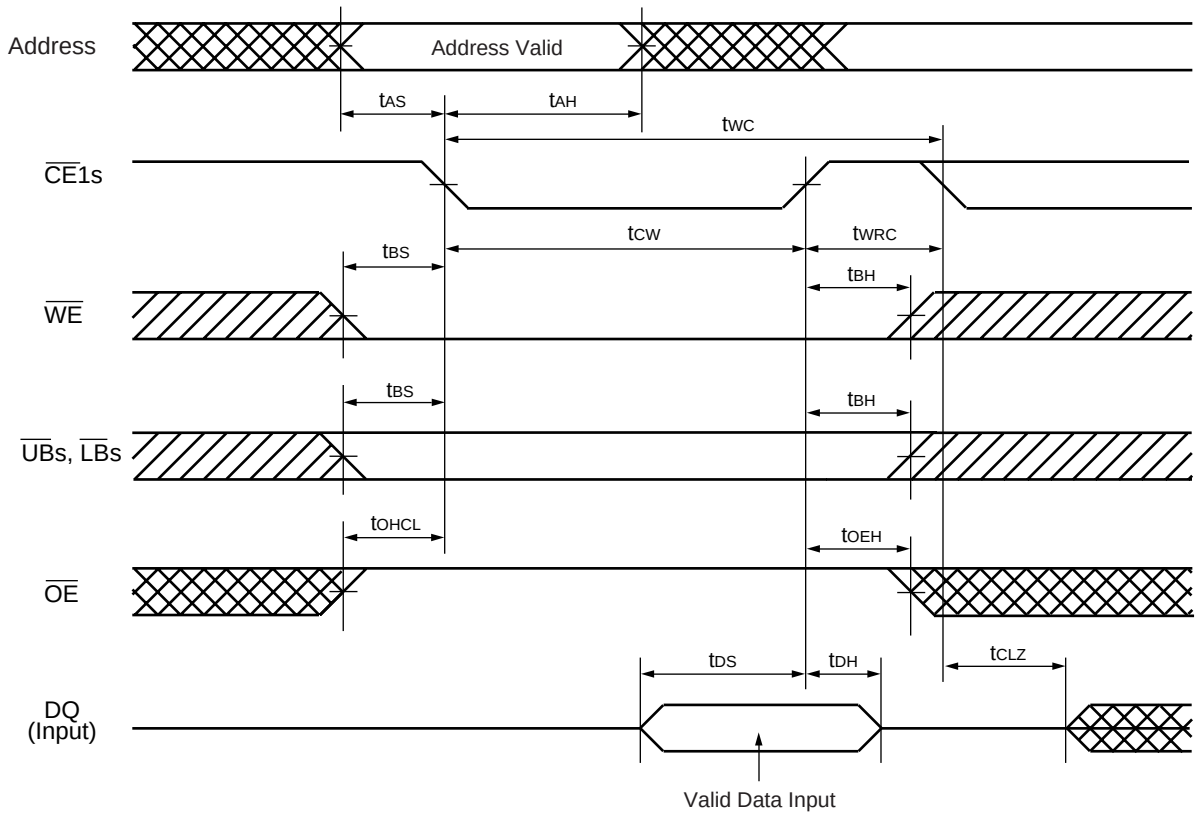
Note : CE2s must be HIGH during the write cycle.

- **WRITE Timing 2 ($\overline{WE}$ Control) (FCRAM)**



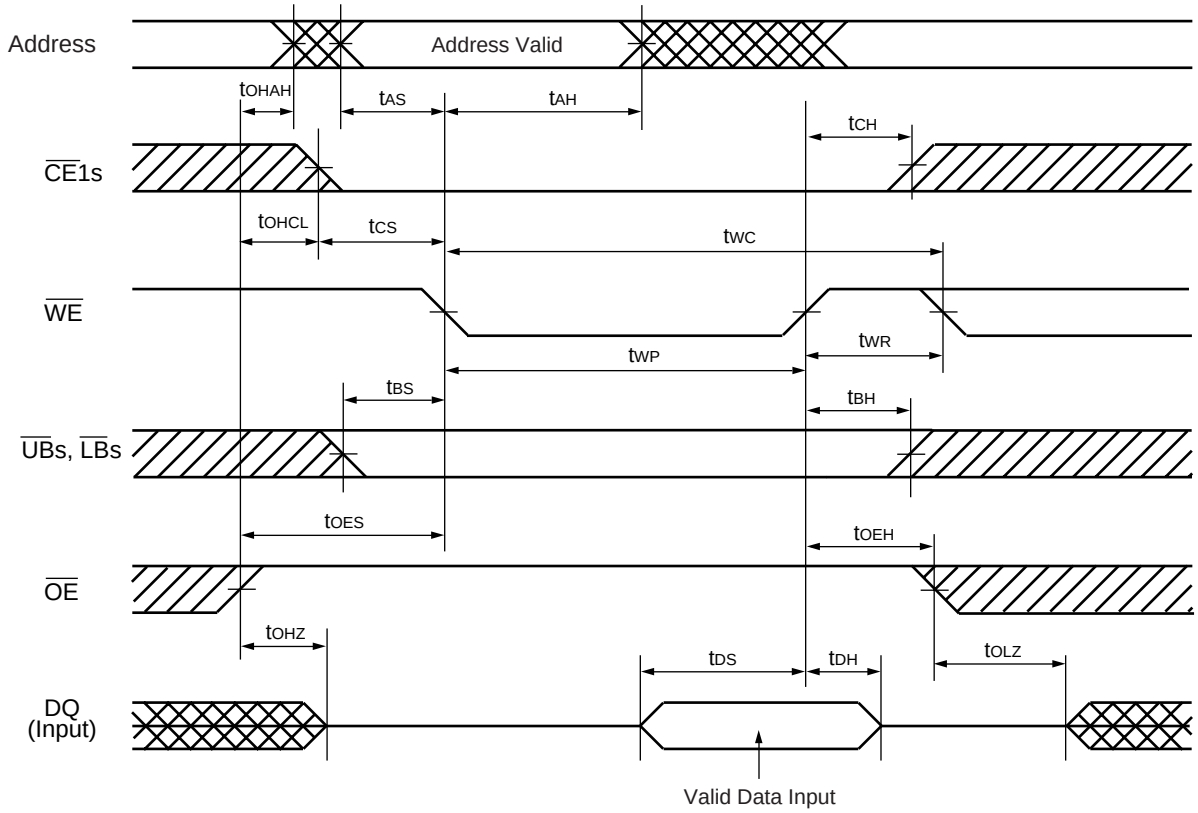
Note : CE2s must be HIGH during the write cycle.

- **BYTE WRITE Timing 1 ($\overline{CE}$1s Control) (FCRAM)**



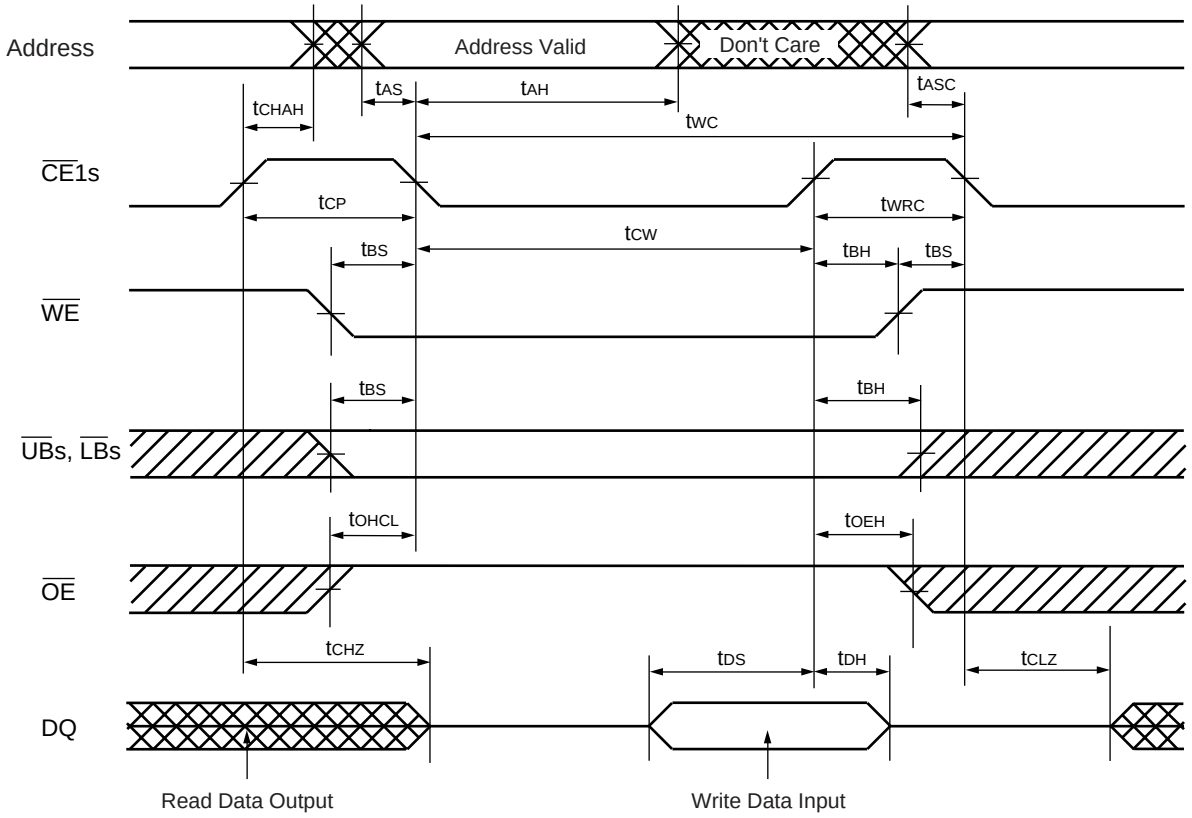
Note : CE2s must be HIGH and either $\overline{LB}$s or $\overline{UB}$s must be LOW during byte write cycle.

- **BYTE WRITE Timing 2 ($\overline{WE}$ Control) (FCRAM)**



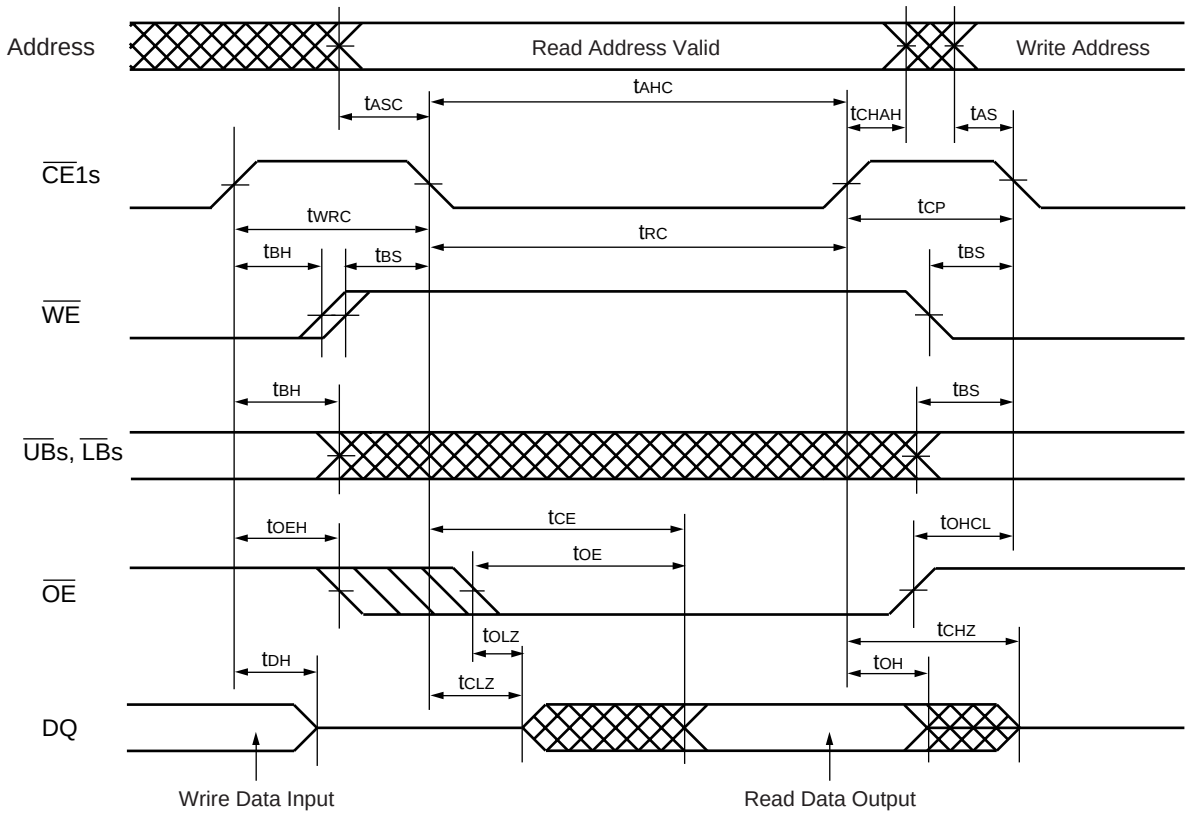
Note : CE2s must be HIGH and either $\overline{LB}$s or $\overline{UB}$s must be LOW during the byte write cycle.

- **READ/WRITE Timing 1-1 ($\overline{CE}$1s Control) (FCRAM)**



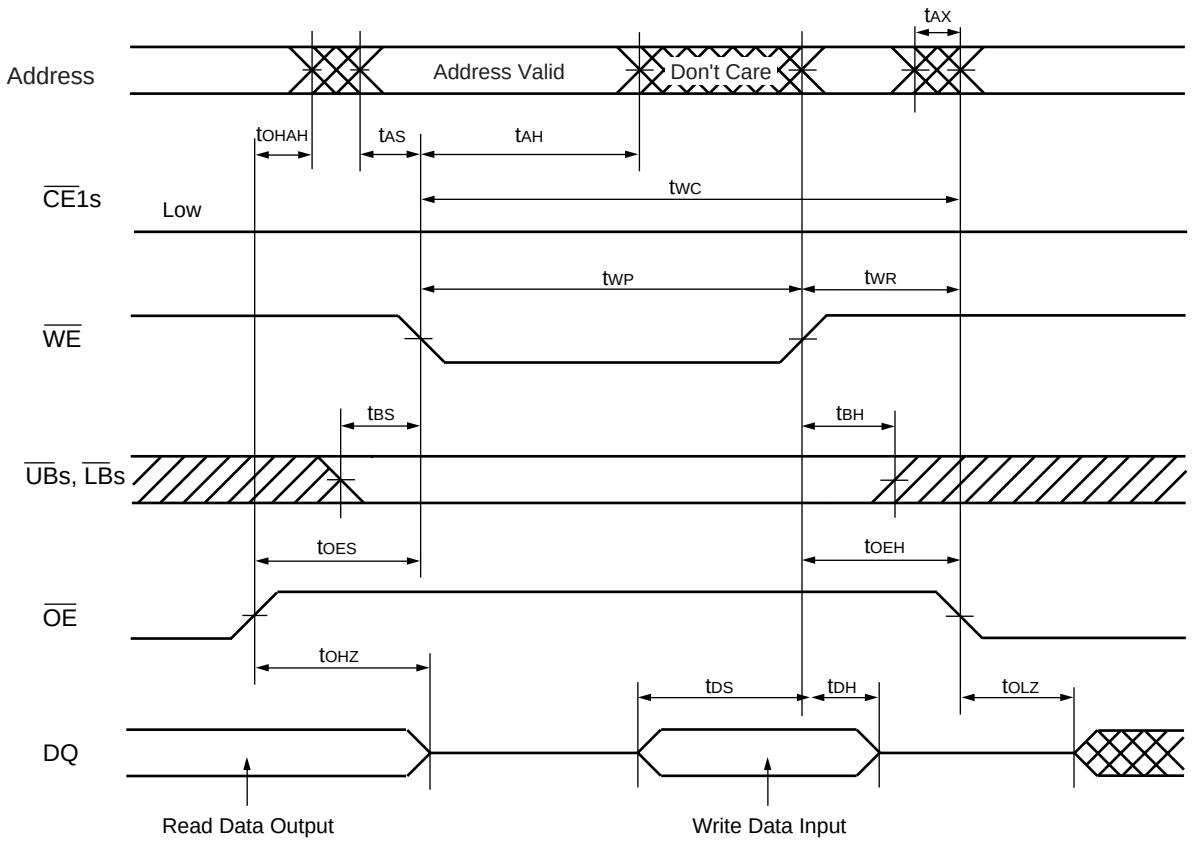
Note : Write address is edge trigger of either $\overline{CE}$1s or $\overline{WE}$ falling edge.

- **READ/WRITE Timing 1-2 ($\overline{CE}$1s Control) (FCRAM)**



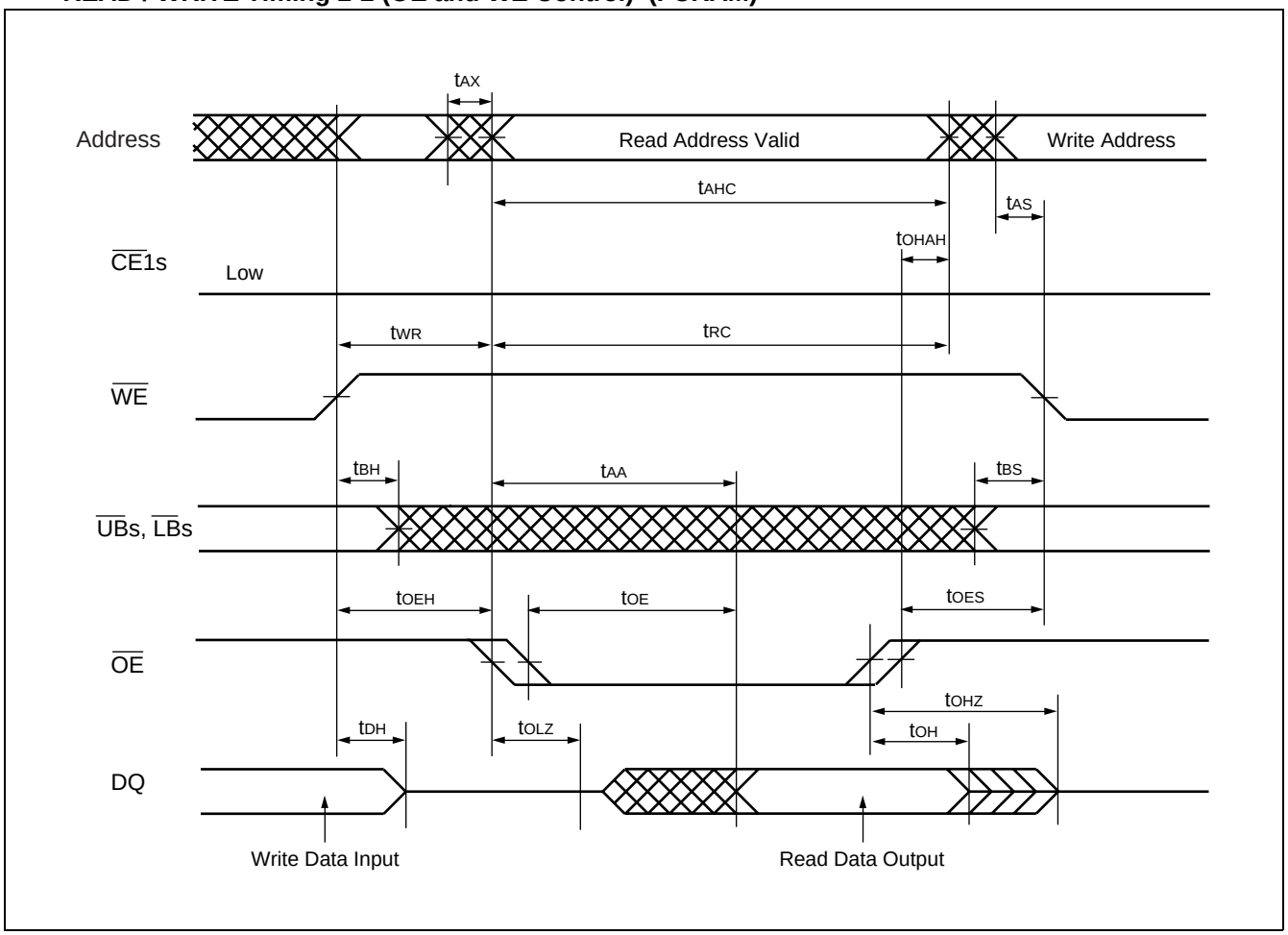
Note : $\overline{WE}$ must be HIGH during the read cycle.

- **READ/WRITE Timing 2-1 ($\overline{OE}$ and $\overline{WE}$ Control) (FCRAM)**



Note : $\overline{CE}$1s can be tied to LOW for $\overline{WE}$ and $\overline{OE}$ controlled operation.
When $\overline{CE}$1s is tied to LOW, output is exclusively controlled by $\overline{OE}$ and read address can be issued after $\overline{WE}$ is brought to High.
WARNING : The read address following write operation must be changed if $\overline{CE}$1s stays LOW.

- **READ / WRITE Timing 2-2 ($\overline{OE}$ and $\overline{WE}$ Control) (FCRAM)**



• **POWER DOWN PARAMETER (FCRAM)**

Parameter	Symbol	Value		Unit	Note
		Min	Max		
CE2s Low Setup Time for Power Down Entry	t_{CSP}	100	—	ns	
$\overline{CE}$1s Low Pulse Width during Power Down Mode	t_{CPP}	100	—	ns	
CE2s Low Hold Time after Power Down Exit ($\overline{CE}$1s = High)	t_{C2LP}	350	—	µs	*1
$\overline{CE}$1s High Hold Time following CE2s High after Power Down Exit	t_{C1HP}	300	—	µs	*2

*1 : Requires at least two dummy read cycles.

*2 : Required when dummy read cycles are not performed.

• **OTHER TIMING PARAMETER (FCRAM)**

Parameter	Symbol	Value		Unit	Note
		Min	Max		
$\overline{CE}$1s High to $\overline{OE}$ Invalid Time for Standby Entry	t_{CHOX}	10	—	ns	
$\overline{CE}$1s High to $\overline{WE}$ Invalid Time for Standby Entry	t_{CHWX}	20	—	ns	
$\overline{CE}$1s and CE2s Active Glitch Pulse Width	t_{CAP}	—	5	ns	*1
$\overline{CE}$1s or $\overline{WE}$ High Glitch Pulse Width during Write Cycle	t_{WHP}	—	5	ns	*2
CE2s Low Hold Time after Power-up	t_{C2LP}	350	—	µs	*3
$\overline{CE}$1s High Hold Time following CE2s High after Power-up	t_{C1HP}	300	—	µs	*4

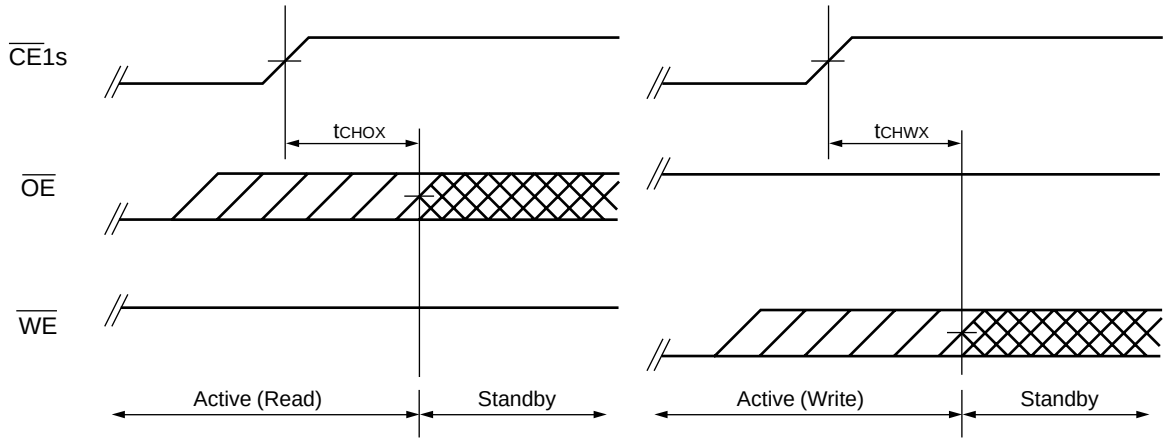
*1 : Active means a condition where $\overline{CE}$1s = V_{IL} and CE2s = V_{IH}.

*2 : Specified to the one time high pulse width during t_{CW} or t_{WP} and excluded 10 ns from beginning and end of the write cycle.

*3 : Requires at least two dummy read cycles.

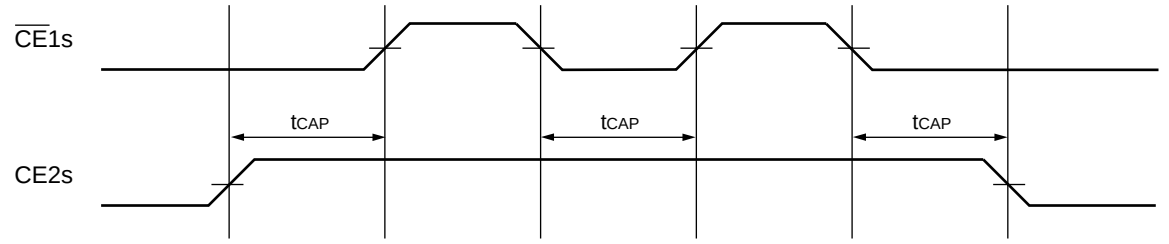
*4 : Required when dummy read cycles are not performed.

- **Standby Entry Timing after Read or Write (FCRAM)**



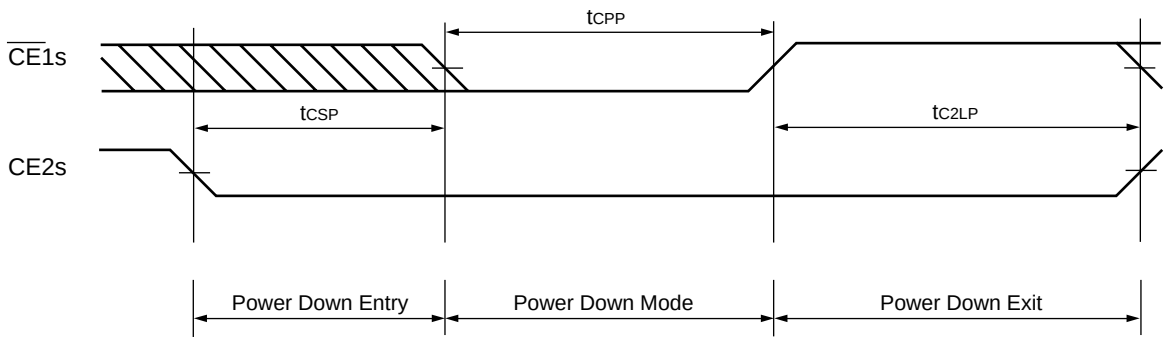
Note : Both t_{CHOX} and t_{CHWX} define the earliest entry timing for Standby mode. If either of timing is not satisfied, it takes t_{RC} (min) period from either last address transition or $\overline{CE}$1s Low to High transition.

- **Chip Enable Timing (FCRAM)**



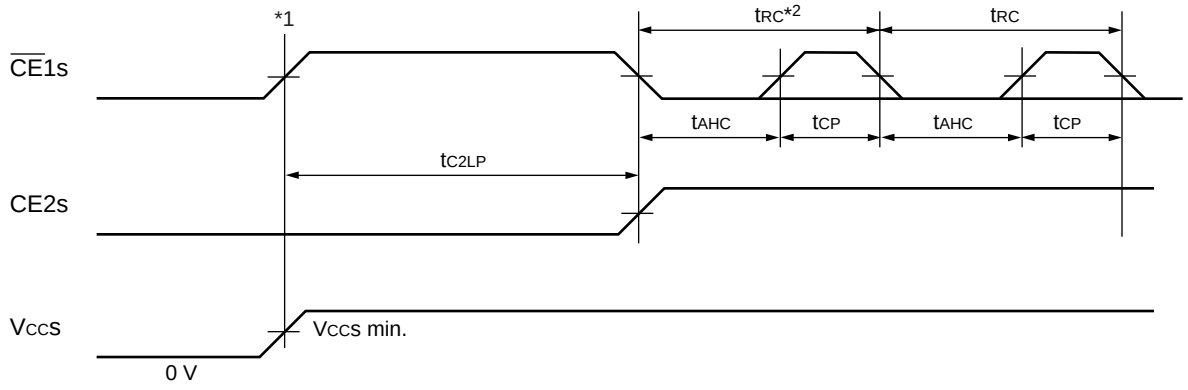
Note : t_{CAP} is not applicable CE2s HIGH pulse width while $\overline{CE}$1s stays LOW and CE2s should not use as a read and write timing control signal in stead of $\overline{CE}$1s.

- **POWER DOWN Timing (FCRAM)**



Note : A minimum of two dummy read cycle must be performed prior to regular read and write operation after t_{C2LP}. Otherwise $\overline{CE}$1s must kept High for t_{C1HP} period after t_{C2LP}.

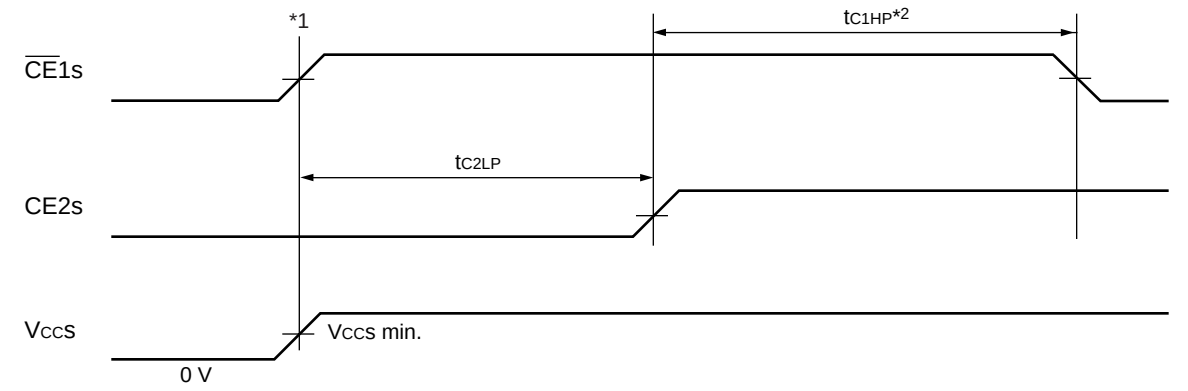
- **Power-Up Timing 1 (FCRAM)**



*1 : It is recommended $\overline{CE}$1s to track V_{CC}s. The t_{C2LP} specifies from valid state of $\overline{CE}$1s = High and CE2s = Low after V_{CC}s reaches specified minimum level.

*2 : 2A minimum of two dummy read cycle must be performed prior to regular read and write operation after t_{C2LP}.

- **Power-Up Timing 2 (No dummy cycle) (FCRAM)**



*1 : It is recommended $\overline{CE}$1s to track V_{CC}s. The t_{C2LP} specifies from valid state of $\overline{CE}$1s = High and CE2s = Low after V_{CC}s reaches specified minimum level.

*2 : No dummy read cycle is required if t_{C1HP} is satisfied.

■ ERASE AND PROGRAMMING PERFORMANCE (FLASH)

Parameter	Limits			Unit	Comments
	Min	Typ	Max		
Sector Erase Time	—	1	10	s	Excludes programming time prior to erasure
Word Programming Time	—	16	360	µs	Excludes system-level overhead
Chip Programming Time	—	—	200	s	Excludes system-level overhead
Erase/Program Cycle	100,000	—	—	cycle	—

■ PACKAGE PIN CAPACITANCE

Parameter	Symbol	Test Setup	Value		Unit
			Typ	Max	
Input Capacitance	C_{IN}	V_{IN} = 0 V	11	14	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0 V	12	16	pF
Control Pin Capacitance	C_{IN2}	V_{IN} = 0 V	14	16	pF
$\overline{WP}$/ACC Pin Capacitance	C_{IN3}	V_{IN} = 0 V	21.5	26	pF

Note : Test conditions T_A = +25 °C, f = 1.0 MHz

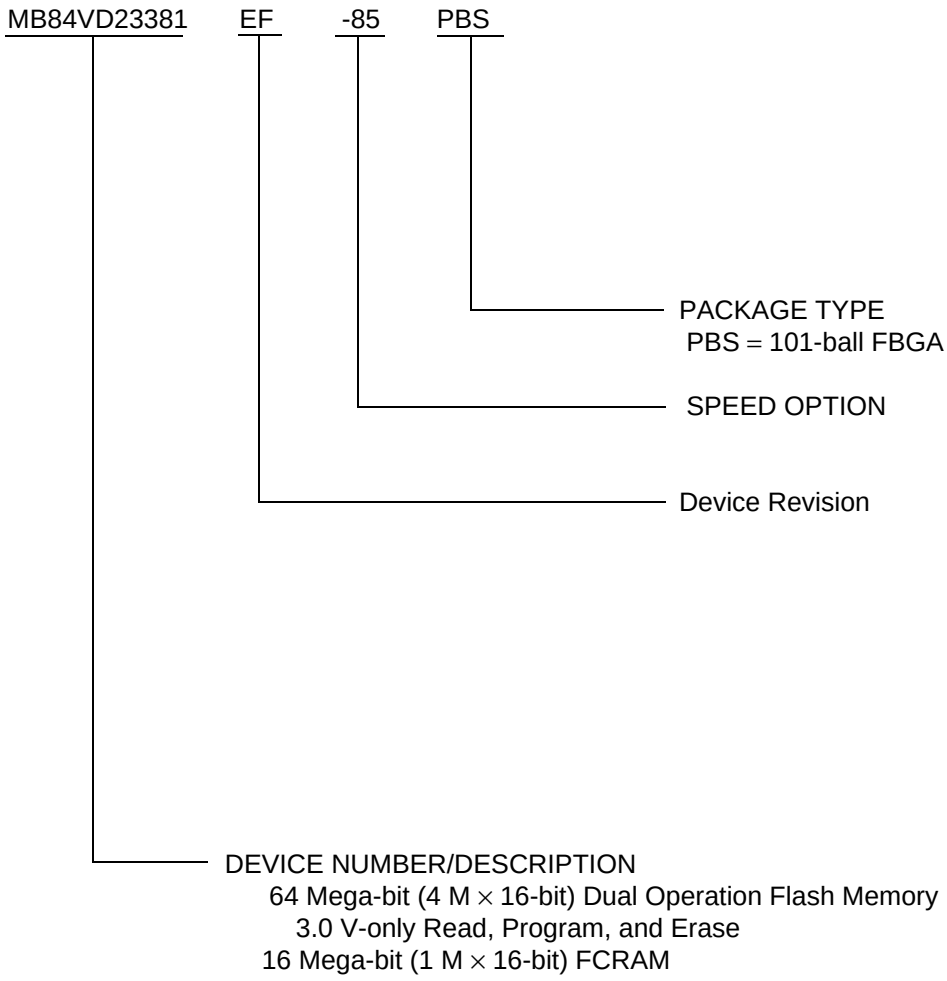
■ HANDLING OF PACKAGE

Please handle this package carefully since the sides of package are created with acute angles.

■ CAUTION

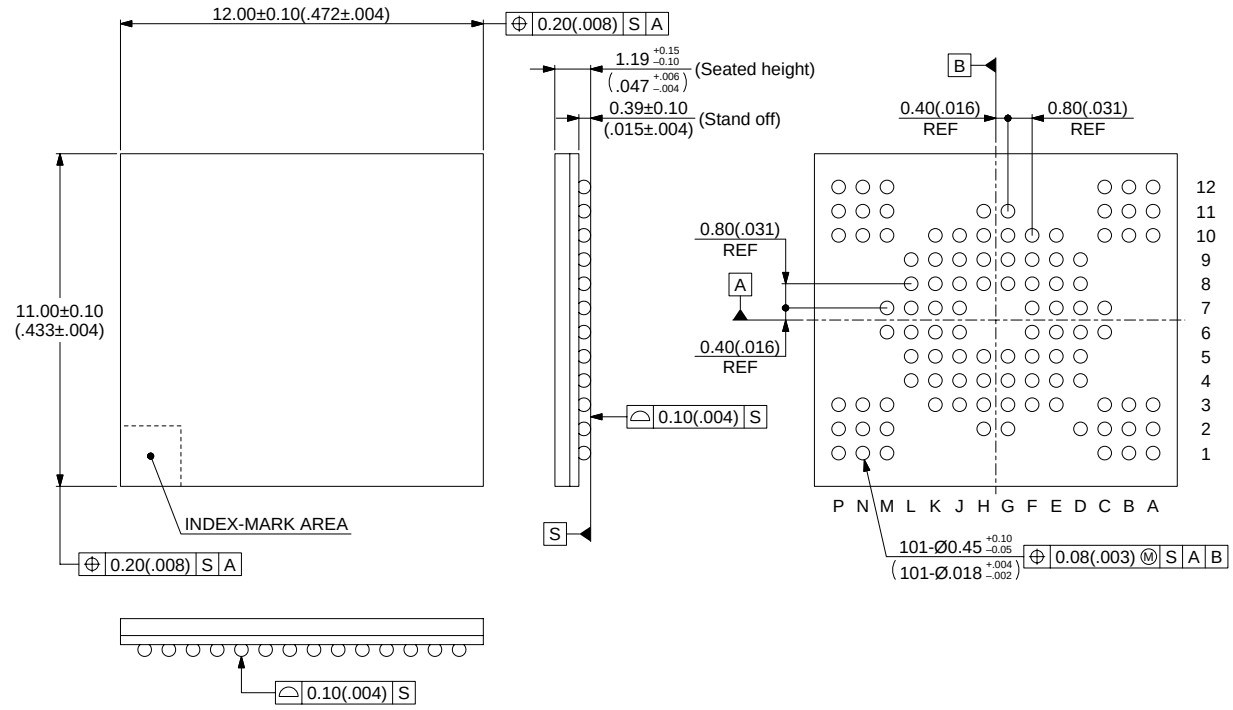
- The high voltage (V_{ID}) cannot be applied to address pins and control pins except $\overline{RESET}$. Exception is when autoselect and Sector Group Protection function are used. Then the high voltage (V_{ID}) can be applied to $\overline{RESET}$.
- Without the high voltage (V_{ID}) , Sector Group Protection can be achieved by using “Extended Sector Group Protection” command.

■ ORDERING INFORMATION



■ PACKAGE DIMENSION

101-ball plastic FBGA
(BGA-101P-M01)



Dimensions in mm (inches)

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