

Stacked MCP (Multi-Chip Package) FLASH MEMORY & FCRAM
CMOS

**64 M (×16) FLASH MEMORY &
32 M (×16) Mobile FCRAM™**

MB84VD23481FJ-70

■ FEATURES

- **Power Supply Voltage of 2.7 V to 3.1 V**
- **High Performance**
70 ns maximum access time (Flash)
70 ns maximum access time (FCRAM)
- **Operating Temperature**
-30 °C to +85 °C
- **Package 65-ball FBGA**

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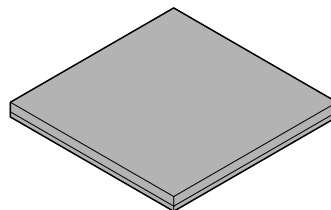
■ PRODUCT LINE-UP

	Flash Memory	FCRAM
Power Supply Voltage (V)	$V_{ccf}^* = 2.7 \text{ V to } 3.1 \text{ V}$	$V_{ccr}^* = 2.7 \text{ V to } 3.1 \text{ V}$
Max Address Access Time (ns)	70	65
Max $\overline{\text{CE}}$ Access Time (ns)	70	65
Max $\overline{\text{OE}}$ Access Time (ns)	30	40

*: Both V_{ccf} and V_{ccr} must be the same level when either part is being accessed.

■ PACKAGE

65-ball plastic FBGA



(BGA-65P-M01)

(Continued)

• FLASH MEMORY

• 0.17 μm Process Technology

• Simultaneous Read/Write Operations (Dual Bank)

• FlexBank™ *1

Bank A : 8 Mbit (8 KB \times 8 and 64 KB \times 15)

Bank B : 24 Mbit (64 KB \times 48)

Bank C : 24 Mbit (64 KB \times 48)

Bank D : 8 Mbit (8 KB \times 8 and 64 KB \times 15)

Two virtual Banks are chosen from the combination of four physical banks. Host system can program or erase in one bank, and then read immediately and simultaneously from the other bank with zero latency between read and write operations.

Read-while-erase

Read-while-program

• Single 3.0 V Read, Program, and Erase

Minimized system level power requirements

• Minimum 100,000 Program/Erase Cycles

• Sector Erase Architecture

Sixteen 4 Kword and one hundred twenty-six 32 Kword sectors in word.

Any combination of sectors can be concurrently erased. It also supports full chip erase.

• HiddenROM Region

256 byte of HiddenROM, accessible through a new "HiddenROM Enable" command sequence

Factory serialized and protected to provide a secure electronic serial number (ESN)

• WP/ACC Input Pin

At V_{IL} , allows protection of "outermost" 2×8 Kbytes on both ends of boot sectors, regardless of sector protection/unprotection status

At V_{IH} , allows removal of boot sector protection

At V_{ACC} , increases program performance

• Embedded Erase™ *2 Algorithms

Automatically preprograms and erases the chip or any sector

• Embedded Program™ *2 Algorithms

Automatically writes and verifies data at specified address

• Data Polling and Toggle Bit Feature for Detection of Program or Erase Cycle Completion

• Ready/Busy Output (RY/BY)

Hardware method for detection of program or erase cycle completion

• Automatic Sleep Mode

When addresses remain stable, the device automatically switches itself to low power mode.

• Low V_{ccf} Write Inhibit ≤ 2.5 V

• Program Suspend/Resume

Suspends the program operation to allow a read in another byte

• Erase Suspend/Resume

Suspends the erase operation to allow a read data and/or program in another sector within the same device

• Please Refer to "MBM29DL64DF" Datasheet in Detailed Function

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- **FCRAM™** *3

- **Power Dissipation**

Operating : 25 mA Max

Standby : 100 μ A Max

- **Power Down Mode**

Sleep : 10 μ A Max

NAP : 60 μ A Max

8M Partial : 70 μ A Max

- **Power Down Control by CE2r**

- **Byte Write Control:** $\overline{\text{LB}}$ (DQ₇ to DQ₀), $\overline{\text{UB}}$ (DQ₁₅ to DQ₈)

- **8 words Address Access Capability**

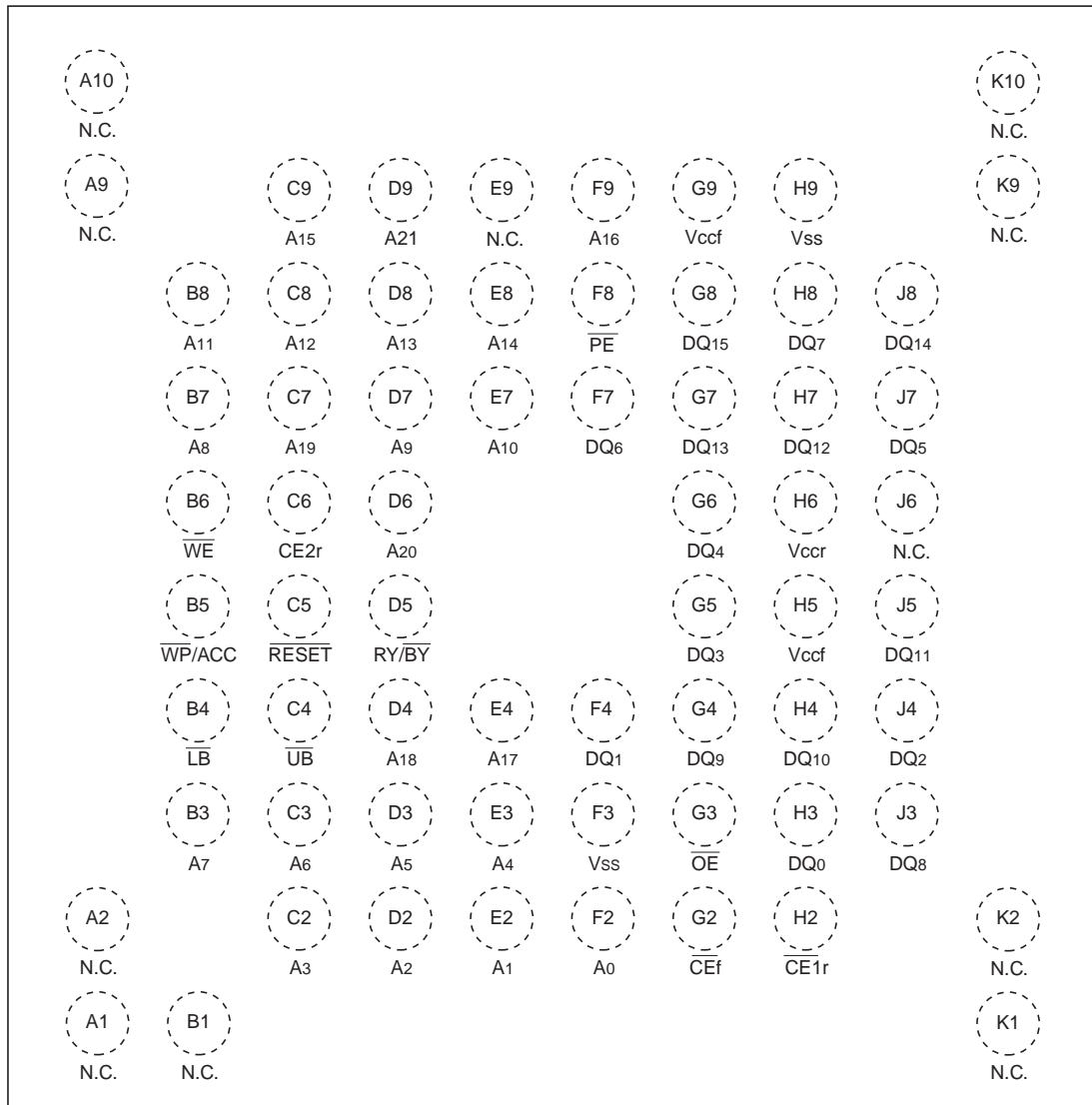
*1 : FlexBank™ is a trademark of Fujitsu Limited, Japan.

*2 : Embedded Erase™ and Embedded Program™ are trademarks of Advanced Micro Devices, Inc.

*3 : FCRAM™ is a trademark of Fujitsu Limited, Japan.

■ PIN ASSIGNMENT

FBGA
(TOP VIEW)
Marking side

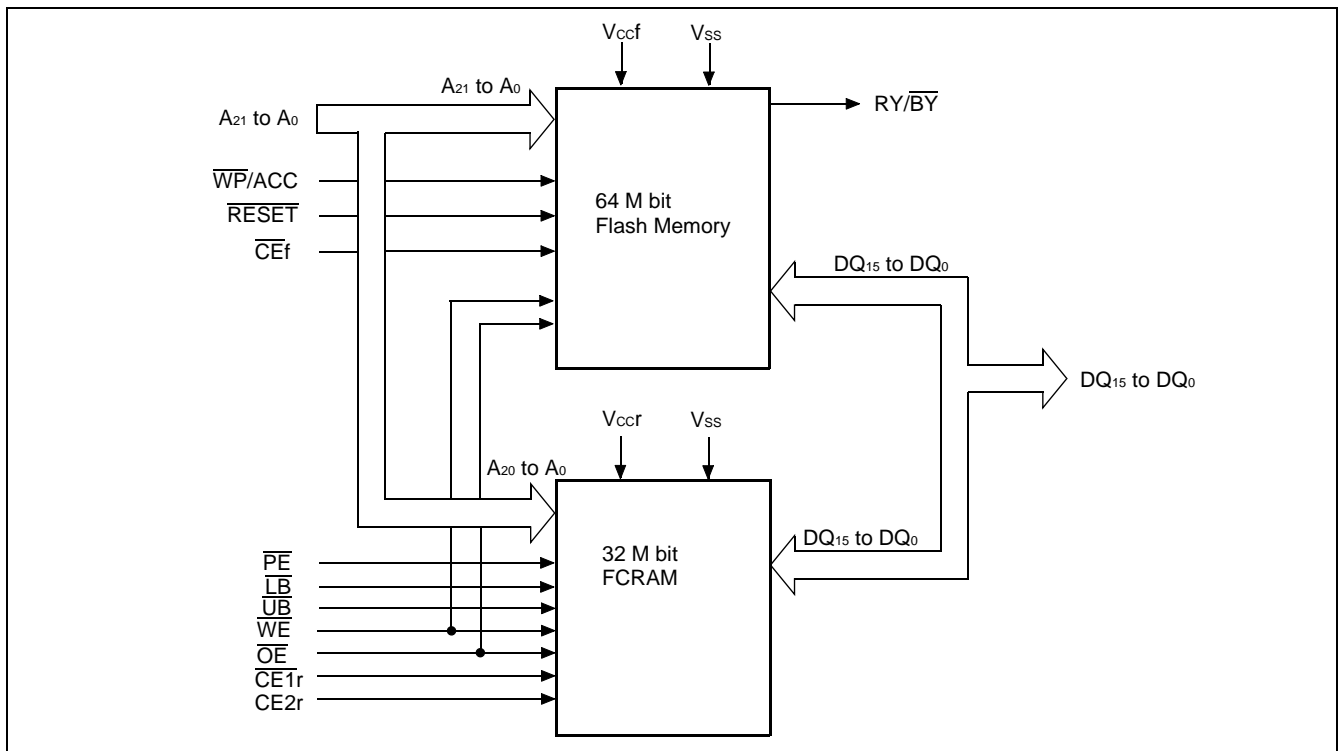


(BGA-65P-M01)

■ PIN DESCRIPTION

Pin Name	Function	Input/Output
A ₂₀ to A ₀	Address Inputs (Common)	I
A ₂₁	Address Input (Flash)	I
DQ ₁₅ to DQ ₀	Data Inputs/Outputs (Common)	I/O
$\overline{\text{CE}}\text{f}$	Chip Enable (Flash)	I
$\overline{\text{CE}}\text{1r}$	Chip Enable (FCRAM)	I
CE2r	Chip Enable (FCRAM)	I
$\overline{\text{OE}}$	Output Enable (Common)	I
$\overline{\text{WE}}$	Write Enable (Common)	I
RY/ $\overline{\text{BY}}$	Ready/Busy Outputs (Flash) Open Drain Output	O
$\overline{\text{UB}}$	Upper Byte Control (FCRAM)	I
$\overline{\text{LB}}$	Lower Byte Control (FCRAM)	I
$\overline{\text{RESET}}$	Hardware Reset Pin/Sector Protection Unlock (Flash)	I
$\overline{\text{WP}}/\text{ACC}$	Write Protect/Acceleration (Flash)	I
$\overline{\text{PE}}$	Partial Enable (FCRAM)	I
N.C.	No Internal Connection	—
V _{ss}	Device Ground (Common)	Power
V _{ccf}	Device Power Supply (Flash)	Power
V _{ccr}	Device Power Supply (FCRAM)	Power

■ BLOCK DIAGRAM



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■ DEVICE BUS OPERATIONS

Operation *1,*2	\overline{CEf}	$\overline{CE1r}$	$CE2r$	\overline{OE}	\overline{WE}	\overline{LB}	\overline{UB}	\overline{PE}	A ₂₁ to A ₀	DQ ₇ to DQ ₀	DQ ₁₅ to DQ ₈	RESET	$\overline{WP/ACC}$ *12
Full Standby	H	H	H	X	X	X	X	H	X	High-Z	High-Z	H	X
Output Disable *3	H	L	H	H	H	X	X	H	X *10	High-Z	High-Z	H	X
	L	H	H	H	H	X	X	H	X	High-Z	High-Z	H	X
Read from Flash *4	L	H	H	L	H	X	X	H	Vaild	D _{OUT}	D _{OUT}	H	X
Write to Flash	L	H	H	H	L	X	X	H	Vaild	D _{IN}	D _{IN}	H	X
Read from FCRAM *5	H	L	H	L	H	L*9	L*9	H	Vaild	D _{OUT}	D _{OUT}	H	X
Write to FCRAM	H	L	H	H	L	L	L	H	Vaild	D _{IN}	D _{IN}	H	X
						H	L			High-Z	D _{IN}		
						L	H			D _{IN}	High-Z		
Temporary Sector Group Unprotection*6	X	X	X	X	X	X	X	X	X	X	X	V _{ID}	X
Flash Hardware Reset	X	H	H	X	X	X	X	X	X	High-Z	High-Z	L	X
Boot Block Sector Write Protection	X	X	X	X	X	X	X	X	X	X	X	X	L
FCRAM Power Down Program *7	H	H	H	X	X	X	X	L	KEY*11	High-Z	High-Z	H	X
FCRAM No Read	H	L	H	L	H	H	H	H	Vaild	High-Z	High-Z	H	X
FCRAM Power Down *8	X	X	L	X	X	X	X	X	X	X	X	X	X

Legend: L = V_{IL}, H = V_{IH}, X = V_{IL} or V_{IH}. See DC Characteristics for voltage levels.

*1 : Other operations except for indicated this column are prohibited.

*2 : Do not apply $\overline{CEf} = V_{IL}$, $\overline{CE1r} = V_{IL}$ and $CE2r = V_{IH}$ all at once.

*3 : FCRAM Output Disable condition should not be kept longer than 1 ms.

*4 : \overline{WE} can be V_{IL} if \overline{OE} is V_{IL}, \overline{OE} at V_{IH} initiates the write operations.

*5 : FCRAM \overline{LB} , \overline{UB} control at Read operation is not supported.

*6 : It is also used for the extended sector group protections.

*7 : The FCRAM Power Down Program can be performed one time after compliance of Power-UP timings and it should not be re-programmed after regular Read or Write.

*8 : FCRAM Power Down mode can be entered from Standby state and all DQ pins are in High-Z state. I_{PDF} current and data retention depends on the selection of Power Down Program.

*9 : Either or both \overline{LB} and \overline{UB} must be Low for FCRAM Read Operation.

*10 : Can be either V_{IL} or V_{IH} but must be valid before Read or Write.

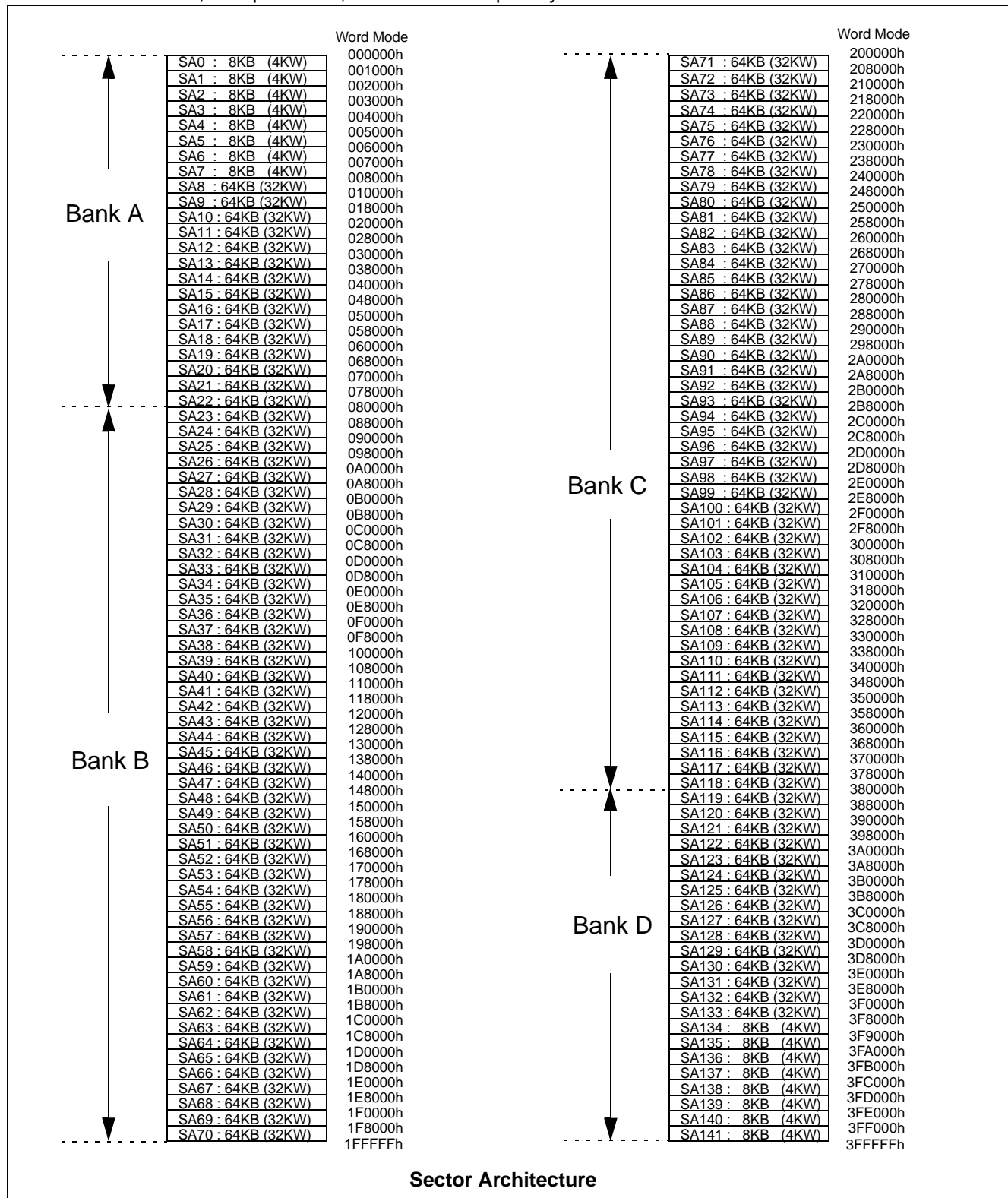
*11 : See “FCRAM Power Down Program Key Table”.

*12 : Protect “outer most” 2x8K bytes (4 words) on both ends of the boot block sectors.

■ 64M FRASH MEMORY CHARACTERISTICS for MCP

1. FLEXIBLE SECTOR-ERASE ARCHITECTURE on FLASH MEMORY

- Sixteen 4K words, and one hundred twenty-six 32 K words.
- Individual-sector, multiple-sector, or bulk-erase capability.



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FlexBank™ Architecture

Bank Splits	Bank 1		Bank 2	
	Volume	Combination	Volume	Combination
1	8 Mbit	Bank A	56 Mbit	Remainder (Bank B, C, D)
2	24 Mbit	Bank B	40 Mbit	Remainder (Bank A, C, D)
3	24 Mbit	Bank C	40 Mbit	Remainder (Bank A, B, D)
4	8 Mbit	Bank D	56 Mbit	Remainder (Bank A, B, C)

Example of Virtual Banks Combination

Bank Splits	Bank 1			Bank 2		
	Volume	Combination	Sector Size	Volume	Combination	Sector Size
1	8 Mbit	Bank A	8 × 8 Kbyte/4 Kword + 15 × 64 Kbyte/32 Kword	56 Mbit	Bank B + Bank C + Bank D	8 × 8 Kbyte/4 Kword + 111 × 64 Kbyte/32 Kword
2	16 Mbit	Bank A + Bank D	16 × 8 Kbyte/4 Kword + 30 × 64 Kbyte/32 Kword	48 Mbit	Bank B + Bank C	96 × 64 Kbyte/32 Kword
3	24 Mbit	Bank B	48 × 64 Kbyte/32 Kword	40 Mbit	Bank A + Bank C + Bank D	16 × 8 Kbyte/4 Kword + 78 × 64 Kbyte/32 Kword
4	32 Mbit	Bank A + Bank B	8 × 8 Kbyte/4 Kword + 63 × 64 Kbyte/32 Kword	32 Mbit	Bank C + Bank D	8 × 8 Kbyte/4 Kword + 63 × 64 Kbyte/32 Kword

Note : When multiple sector erase over several banks is operated, the system cannot read out of the bank to which a sector being erased belongs. For example, suppose that erasing is taking place at both Bank A and Bank B, neither Bank A nor Bank B is read out (they would output the sequence flag once they were selected.) Meanwhile the system would get to read from either Bank C or Bank D.

Simultaneous Operation

Case	Bank 1 Status	Bank 2 Status
1	Read mode	Read mode
2	Read mode	Autoselect mode
3	Read mode	Program mode
4	Read mode	Erase mode *
5	Autoselect mode	Read mode
6	Program mode	Read mode
7	Erase mode *	Read mode

* : By writing erase suspend command on the bank address of sector being erased, the erase operation gets suspended so that it enables reading from or programming the remaining sectors.

Note: Bank 1 and Bank 2 are divided for the sake of convenience at Simultaneous Operation. Actually, the Bank consists of 4 banks, Bank A, Bank B, Bank C and Bank D. Bank Address (BA) meant to specify each of the Banks.

Sector Address Tables

Bank	Sector	Sector Address										Address Range	
		Bank Address										Word Mode	
		A ₂₁	A ₂₀	A ₁₉	A ₁₈	A ₁₇	A ₁₆	A ₁₅	A ₁₄	A ₁₃	A ₁₂		
Bank A	SA0	0	0	0	0	0	0	0	0	0	0	0	000000h to 000FFFh
	SA1	0	0	0	0	0	0	0	0	0	0	1	001000h to 001FFFh
	SA2	0	0	0	0	0	0	0	0	0	1	0	002000h to 002FFFh
	SA3	0	0	0	0	0	0	0	0	0	1	1	003000h to 003FFFh
	SA4	0	0	0	0	0	0	0	0	1	0	0	004000h to 004FFFh
	SA5	0	0	0	0	0	0	0	0	1	0	1	005000h to 005FFFh
	SA6	0	0	0	0	0	0	0	0	1	1	0	006000h to 006FFFh
	SA7	0	0	0	0	0	0	0	0	1	1	1	007000h to 007FFFh
	SA8	0	0	0	0	0	0	0	1	X	X	X	008000h to 00FFFFh
	SA9	0	0	0	0	0	0	1	0	X	X	X	010000h to 017FFFh
	SA10	0	0	0	0	0	0	1	1	X	X	X	018000h to 01FFFFh
	SA11	0	0	0	0	0	1	0	0	X	X	X	020000h to 027FFFh
	SA12	0	0	0	0	0	1	0	1	X	X	X	028000h to 02FFFFh
	SA13	0	0	0	0	0	1	1	0	X	X	X	030000h to 037FFFh
	SA14	0	0	0	0	0	1	1	1	X	X	X	038000h to 03FFFFh
	SA15	0	0	0	0	1	0	0	0	X	X	X	040000h to 047FFFh
	SA16	0	0	0	0	1	0	0	1	X	X	X	048000h to 04FFFFh
	SA17	0	0	0	0	1	0	1	0	X	X	X	050000h to 057FFFh
	SA18	0	0	0	0	1	0	1	1	X	X	X	058000h to 05FFFFh
	SA19	0	0	0	0	1	1	0	0	X	X	X	060000h to 067FFFh
	SA20	0	0	0	0	1	1	0	1	X	X	X	068000h to 06FFFFh
	SA21	0	0	0	0	1	1	1	0	X	X	X	070000h to 077FFFh
SA22	0	0	0	0	1	1	1	1	X	X	X	078000h to 07FFFFh	

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Bank	Sector	Sector Address										Address Range
		Bank Address			Word Mode							Address Range
		A ₂₁	A ₂₀	A ₁₉	A ₁₈	A ₁₇	A ₁₆	A ₁₅	A ₁₄	A ₁₃	A ₁₂	
Bank B	SA23	0	0	1	0	0	0	0	X	X	X	08000h to 087FFFh
	SA24	0	0	1	0	0	0	1	X	X	X	08800h to 08FFFFh
	SA25	0	0	1	0	0	1	0	X	X	X	09000h to 097FFFh
	SA26	0	0	1	0	0	1	1	X	X	X	09800h to 09FFFFh
	SA27	0	0	1	0	1	0	0	X	X	X	0A000h to 0A7FFFh
	SA28	0	0	1	0	1	0	1	X	X	X	0A800h to 0AFFFFh
	SA29	0	0	1	0	1	1	0	X	X	X	0B000h to 0B7FFFh
	SA30	0	0	1	0	1	1	1	X	X	X	0B800h to 0BFFFFh
	SA31	0	0	1	1	0	0	0	X	X	X	0C000h to 0C7FFFh
	SA32	0	0	1	1	0	0	1	X	X	X	0C800h to 0CFFFFh
	SA33	0	0	1	1	0	1	0	X	X	X	0D000h to 0D7FFFh
	SA34	0	0	1	1	0	1	1	X	X	X	0D800h to 0DFFFFh
	SA35	0	0	1	1	1	0	0	X	X	X	0E000h to 0E7FFFh
	SA36	0	0	1	1	1	0	1	X	X	X	0E800h to 0EFFFFh
	SA37	0	0	1	1	1	1	0	X	X	X	0F000h to 0F7FFFh
	SA38	0	0	1	1	1	1	1	X	X	X	0F800h to 0FFFFh
	SA39	0	1	0	0	0	0	0	X	X	X	10000h to 107FFFh
	SA40	0	1	0	0	0	0	1	X	X	X	10800h to 10FFFFh
	SA41	0	1	0	0	0	1	0	X	X	X	11000h to 117FFFh
	SA42	0	1	0	0	0	1	1	X	X	X	11800h to 11FFFFh
	SA43	0	1	0	0	1	0	0	X	X	X	12000h to 127FFFh
	SA44	0	1	0	0	1	0	1	X	X	X	12800h to 12FFFFh
	SA45	0	1	0	0	1	1	0	X	X	X	13000h to 137FFFh
	SA46	0	1	0	0	1	1	1	X	X	X	13800h to 13FFFFh
	SA47	0	1	0	1	0	0	0	X	X	X	14000h to 147FFFh
	SA48	0	1	0	1	0	0	1	X	X	X	14800h to 14FFFFh
	SA49	0	1	0	1	0	1	0	X	X	X	15000h to 157FFFh
	SA50	0	1	0	1	0	1	1	X	X	X	15800h to 15FFFFh
	SA51	0	1	0	1	1	0	0	X	X	X	16000h to 167FFFh
	SA52	0	1	0	1	1	0	1	X	X	X	16800h to 16FFFFh
	SA53	0	1	0	1	1	1	0	X	X	X	17000h to 177FFFh
	SA54	0	1	0	1	1	1	1	X	X	X	17800h to 17FFFFh
SA55	0	1	1	0	0	0	0	X	X	X	18000h to 187FFFh	
SA56	0	1	1	0	0	0	1	X	X	X	18800h to 18FFFFh	
SA57	0	1	1	0	0	1	0	X	X	X	19000h to 197FFFh	
SA58	0	1	1	0	0	1	1	X	X	X	19800h to 19FFFFh	
SA59	0	1	1	0	1	0	0	X	X	X	1A000h to 1A7FFFh	
SA60	0	1	1	0	1	0	1	X	X	X	1A800h to 1AFFFFh	
SA61	0	1	1	0	1	1	0	X	X	X	1B000h to 1B7FFFh	
SA62	0	1	1	0	1	1	1	X	X	X	1B800h to 1BFFFFh	
SA63	0	1	1	1	0	0	0	X	X	X	1C000h to 1C7FFFh	
SA64	0	1	1	1	0	0	1	X	X	X	1C800h to 1CFFFFh	
SA65	0	1	1	1	0	1	0	X	X	X	1D000h to 1D7FFFh	
SA66	0	1	1	1	0	1	1	X	X	X	1D800h to 1DFFFFh	
SA67	0	1	1	1	1	0	0	X	X	X	1E000h to 1E7FFFh	
SA68	0	1	1	1	1	0	1	X	X	X	1E800h to 1EFFFFh	
SA69	0	1	1	1	1	1	0	X	X	X	1F000h to 1F7FFFh	
SA70	0	1	1	1	1	1	1	X	X	X	1F800h to 1FFFFh	

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Bank	Sector	Sector Address										Address Range	
		Bank Address			Sector Address							Word Mode	
		A ₂₁	A ₂₀	A ₁₉	A ₁₈	A ₁₇	A ₁₆	A ₁₅	A ₁₄	A ₁₃	A ₁₂		
Bank C	SA71	1	0	0	0	0	0	0	0	X	X	X	200000h to 207FFFh
	SA72	1	0	0	0	0	0	1	X	X	X	208000h to 20FFFFh	
	SA73	1	0	0	0	0	1	0	X	X	X	210000h to 217FFFh	
	SA74	1	0	0	0	0	1	1	X	X	X	218000h to 21FFFFh	
	SA75	1	0	0	0	1	0	0	X	X	X	220000h to 227FFFh	
	SA76	1	0	0	0	1	0	1	X	X	X	228000h to 22FFFFh	
	SA77	1	0	0	0	1	1	0	X	X	X	230000h to 237FFFh	
	SA78	1	0	0	0	1	1	1	X	X	X	238000h to 23FFFFh	
	SA79	1	0	0	1	0	0	0	X	X	X	240000h to 247FFFh	
	SA80	1	0	0	1	0	0	1	X	X	X	248000h to 24FFFFh	
	SA81	1	0	0	1	0	1	0	X	X	X	250000h to 257FFFh	
	SA82	1	0	0	1	0	1	1	X	X	X	258000h to 25FFFFh	
	SA83	1	0	0	1	1	0	0	X	X	X	260000h to 267FFFh	
	SA84	1	0	0	1	1	0	1	X	X	X	268000h to 26FFFFh	
	SA85	1	0	0	1	1	1	0	X	X	X	270000h to 277FFFh	
	SA86	1	0	0	1	1	1	1	X	X	X	278000h to 27FFFFh	
	SA87	1	0	1	0	0	0	0	X	X	X	280000h to 287FFFh	
	SA88	1	0	1	0	0	0	1	X	X	X	288000h to 28FFFFh	
	SA89	1	0	1	0	0	1	0	X	X	X	290000h to 297FFFh	
	SA90	1	0	1	0	0	1	1	X	X	X	298000h to 29FFFFh	
	SA91	1	0	1	0	1	0	0	X	X	X	2A0000h to 2A7FFFh	
	SA92	1	0	1	0	1	0	1	X	X	X	2A8000h to 2AFFFFh	
	SA93	1	0	1	0	1	1	0	X	X	X	2B0000h to 2B7FFFh	
	SA94	1	0	1	0	1	1	1	X	X	X	2B8000h to 2BFFFFh	
	SA95	1	0	1	1	0	0	0	X	X	X	2C0000h to 2C7FFFh	
	SA96	1	0	1	1	0	0	1	X	X	X	2C8000h to 2CFFFFh	
	SA97	1	0	1	1	0	1	0	X	X	X	2D0000h to 2D7FFFh	
	SA98	1	0	1	1	0	1	1	X	X	X	2D8000h to 2DFFFFh	
SA99	1	0	1	1	1	0	0	X	X	X	2E0000h to 2E7FFFh		
SA100	1	0	1	1	1	0	1	X	X	X	2E8000h to 2EFFFFh		
SA101	1	0	1	1	1	1	0	X	X	X	2F0000h to 2F7FFFh		
SA102	1	0	1	1	1	1	1	X	X	X	2F8000h to 2FFFFh		
SA103	1	1	0	0	0	0	0	X	X	X	300000h to 307FFFh		
SA104	1	1	0	0	0	0	1	X	X	X	308000h to 30FFFFh		
SA105	1	1	0	0	0	1	0	X	X	X	310000h to 317FFFh		
SA106	1	1	0	0	0	1	1	X	X	X	318000h to 31FFFFh		
SA107	1	1	0	0	1	0	0	X	X	X	320000h to 327FFFh		
SA108	1	1	0	0	1	0	1	X	X	X	328000h to 32FFFFh		
SA109	1	1	0	0	1	1	0	X	X	X	330000h to 337FFFh		
SA110	1	1	0	0	1	1	1	X	X	X	338000h to 33FFFFh		
SA111	1	1	0	1	0	0	0	X	X	X	340000h to 347FFFh		
SA112	1	1	0	1	0	0	1	X	X	X	348000h to 34FFFFh		
SA113	1	1	0	1	0	1	0	X	X	X	350000h to 357FFFh		
SA114	1	1	0	1	0	1	1	X	X	X	358000h to 35FFFFh		
SA115	1	1	0	1	1	0	0	X	X	X	360000h to 367FFFh		
SA116	1	1	0	1	1	0	1	X	X	X	368000h to 36FFFFh		
SA117	1	1	0	1	1	1	0	X	X	X	370000h to 377FFFh		
SA118	1	1	0	1	1	1	1	X	X	X	378000h to 37FFFFh		

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(Continued)

Bank	Sector	Sector Address										Address Range
		Bank Address										Word Mode
		A ₂₁	A ₂₀	A ₁₉	A ₁₈	A ₁₇	A ₁₆	A ₁₅	A ₁₄	A ₁₃	A ₁₂	
Bank D	SA119	1	1	1	0	0	0	0	X	X	X	380000h to 387FFFh
	SA120	1	1	1	0	0	0	1	X	X	X	388000h to 38FFFFh
	SA121	1	1	1	0	0	1	0	X	X	X	390000h to 397FFFh
	SA122	1	1	1	0	0	1	1	X	X	X	398000h to 39FFFFh
	SA123	1	1	1	0	1	0	0	X	X	X	3A0000h to 3A7FFFh
	SA124	1	1	1	0	1	0	1	X	X	X	3A8000h to 3AFFFFh
	SA125	1	1	1	0	1	1	0	X	X	X	3B0000h to 3B7FFFh
	SA126	1	1	1	0	1	1	1	X	X	X	3B8000h to 3BFFFFh
	SA127	1	1	1	1	0	0	0	X	X	X	3C0000h to 3C7FFFh
	SA128	1	1	1	1	0	0	1	X	X	X	3C8000h to 3CFFFFh
	SA129	1	1	1	1	0	1	0	X	X	X	3D0000h to 3D7FFFh
	SA130	1	1	1	1	0	1	1	X	X	X	3D8000h to 3DFFFFh
	SA131	1	1	1	1	1	0	0	X	X	X	3E0000h to 3E7FFFh
	SA132	1	1	1	1	1	0	1	X	X	X	3E8000h to 3EFFFFh
	SA133	1	1	1	1	1	1	0	X	X	X	3F0000h to 3F7FFFh
	SA134	1	1	1	1	1	1	1	0	0	0	3F8000h to 3F8FFFh
	SA135	1	1	1	1	1	1	1	0	0	1	3F9000h to 3F9FFFh
SA136	1	1	1	1	1	1	1	0	1	0	3FA000h to 3FAFFFh	
SA137	1	1	1	1	1	1	1	0	1	1	3FB000h to 3FBFFFh	
SA138	1	1	1	1	1	1	1	1	0	0	3FC000h to 3FCFFFh	
SA139	1	1	1	1	1	1	1	1	0	1	3FD000h to 3FDFFFh	
SA140	1	1	1	1	1	1	1	1	1	0	3FE000h to 3FEFFFh	
SA141	1	1	1	1	1	1	1	1	1	1	3FF000h to 3FFFFFh	

Sector Group Addresses

Sector Group	A ₂₁	A ₂₀	A ₁₉	A ₁₈	A ₁₇	A ₁₆	A ₁₅	A ₁₄	A ₁₃	A ₁₂	Sectors
SGA0	0	0	0	0	0	0	0	0	0	0	SA0
SGA1	0	0	0	0	0	0	0	0	0	1	SA1
SGA2	0	0	0	0	0	0	0	0	1	0	SA2
SGA3	0	0	0	0	0	0	0	0	1	1	SA3
SGA4	0	0	0	0	0	0	0	1	0	0	SA4
SGA5	0	0	0	0	0	0	0	1	0	1	SA5
SGA6	0	0	0	0	0	0	0	1	1	0	SA6
SGA7	0	0	0	0	0	0	0	1	1	1	SA7
SGA8	0	0	0	0	0	0	1	X	X	X	SA8 to SA10
						1	0				
						1	1				
SGA9	0	0	0	0	1	X	X	X	X	X	SA11 to SA14
SGA10	0	0	0	1	0	X	X	X	X	X	SA15 to SA18
SGA11	0	0	0	1	1	X	X	X	X	X	SA19 to SA22
SGA12	0	0	1	0	0	X	X	X	X	X	SA23 to SA26
SGA13	0	0	1	0	1	X	X	X	X	X	SA27 to SA30
SGA14	0	0	1	1	0	X	X	X	X	X	SA31 to SA34
SGA15	0	0	1	1	1	X	X	X	X	X	SA35 to SA38
SGA16	0	1	0	0	0	X	X	X	X	X	SA39 to SA42
SGA17	0	1	0	0	1	X	X	X	X	X	SA43 to SA46
SGA18	0	1	0	1	0	X	X	X	X	X	SA47 to SA50
SGA19	0	1	0	1	1	X	X	X	X	X	SA51 to SA54
SGA20	0	1	1	0	0	X	X	X	X	X	SA55 to SA58
SGA21	0	1	1	0	1	X	X	X	X	X	SA59 to SA62
SGA22	0	1	1	1	0	X	X	X	X	X	SA63 to SA66
SGA23	0	1	1	1	1	X	X	X	X	X	SA67 to SA70
SGA24	1	0	0	0	0	X	X	X	X	X	SA71 to SA74
SGA25	1	0	0	0	1	X	X	X	X	X	SA75 to SA78
SGA26	1	0	0	1	0	X	X	X	X	X	SA79 to SA82
SGA27	1	0	0	1	1	X	X	X	X	X	SA83 to SA86
SGA28	1	0	1	0	0	X	X	X	X	X	SA87 to SA90
SGA29	1	0	1	0	1	X	X	X	X	X	SA91 to SA94
SGA30	1	0	1	1	0	X	X	X	X	X	SA95 to SA98
SGA31	1	0	1	1	1	X	X	X	X	X	SA99 to SA102
SGA32	1	1	0	0	0	X	X	X	X	X	SA103 to SA106
SGA33	1	1	0	0	1	X	X	X	X	X	SA107 to SA110
SGA34	1	1	0	1	0	X	X	X	X	X	SA111 to SA114
SGA35	1	1	0	1	1	X	X	X	X	X	SA115 to SA118
SGA36	1	1	1	0	0	X	X	X	X	X	SA119 to SA122
SGA37	1	1	1	0	1	X	X	X	X	X	SA123 to SA126
SGA38	1	1	1	1	0	X	X	X	X	X	SA127 to SA130
SGA39	1	1	1	1	1	0	0	X	X	X	SA131 to SA133
						0	1				
						1	0				
SGA40	1	1	1	1	1	1	1	0	0	0	SA134
SGA41	1	1	1	1	1	1	1	0	0	1	SA135
SGA42	1	1	1	1	1	1	1	0	1	0	SA136
SGA43	1	1	1	1	1	1	1	0	1	1	SA137
SGA44	1	1	1	1	1	1	1	1	0	0	SA138
SGA45	1	1	1	1	1	1	1	1	0	1	SA139
SGA46	1	1	1	1	1	1	1	1	1	0	SA140
SGA47	1	1	1	1	1	1	1	1	1	1	SA141

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Flash Memory Autoselect Codes

Type	A ₂₁ to A ₁₂	A ₆	A ₃	A ₂	A ₁	A ₀	Code (HEX)
Manufacture's Code	BA	L	L	L	L	L	04h
Device Code	BA	L	L	L	L	H	227Eh
Extended Device Code *2	BA	L	H	H	H	L	2202h
	BA	L	H	H	H	H	2201h
Sector Group Protection	Sector Group Addresses	L	L	L	H	L	01h*1

Legend: L = V_{IL}, H = V_{IH}. See DC Characteristics for voltage levels.

*1 : Outputs 01h at protected sector group addresses and outputs 00h at unprotected sector group addresses.

*2 : A read cycle at address (BA) 01h outputs device code. When 227Eh was output, this indicates that there will require two additional codes, called Extended Device Codes. Therefore the system may continue reading out these Extended Device Codes at the address of (BA) 0Eh, as well as at (BA) 0Fh.

Flash Memory Command Definitions

Command Sequence	Bus Write Cycles Req'd	First Bus Write Cycle		Second Bus Write Cycle		Third Bus Write Cycle		Fourth Bus Read/Write Cycle		Fifth Bus Write Cycle		Sixth Bus Write Cycle	
		Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data
Read/Reset	1	XXXh	F0h	—	—	—	—	—	—	—	—	—	—
Read/Reset	3	555h	AAh	2AAh	55h	555h	F0h	RA*5	RD*9	—	—	—	—
Autoselect	3	555h	AAh	2AAh	55h	(BA*8) 555h	90h	—	—	—	—	—	—
Program	4	555h	AAh	2AAh	55h	555h	A0h	PA*6	PD*10	—	—	—	—
Program Suspend	1	BA*8	B0h	—	—	—	—	—	—	—	—	—	—
Program Resume	1	BA*8	30h	—	—	—	—	—	—	—	—	—	—
Chip Erase	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	555h	10h
Sector Erase	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	SA*7	30h
Erase Suspend	1	BA*8	B0h	—	—	—	—	—	—	—	—	—	—
Erase Resume	1	BA*8	30h	—	—	—	—	—	—	—	—	—	—
Extended Sector Group Protection *2	4	XXXh	60h	SPA*11	60h	SPA*11	40h	SPA*11	SD*12	—	—	—	—
Set to Fast Mode	3	555h	AAh	2AAh	55h	555h	20h	—	—	—	—	—	—
Fast Program *1	2	XXXh	A0h	PA*6	PD*10	—	—	—	—	—	—	—	—
Reset from Fast Mode *1	2	BA*8	90h	XXXh	F0h*4	—	—	—	—	—	—	—	—
Query	1	(BA*8) 55h	98h	—	—	—	—	—	—	—	—	—	—
HiddenROM Entry	3	555h	AAh	2AAh	55h	555h	88h	—	—	—	—	—	—
HiddenROM Program *3	4	555h	AAh	2AAh	55h	555h	A0h	(HRA*13) PA*6	PD*10	—	—	—	—
HiddenROM Exit *3	4	555h	AAh	2AAh	55h	(HRBA*14) 555h	90h	XXXh	00h	—	—	—	—

(Continued)

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(Continued)

- *1: This command is valid during Fast Mode.
- *2: This command is valid while $\overline{\text{RESET}} = V_{\text{DD}}$.
- *3: This command is valid during HiddenROM mode.
- *4: The data "00h" is also acceptable.
- *5: RA = Address of the memory location to be read
- *6: PA = Address of the memory location to be programmed
Addresses are latched on the falling edge of the write pulse.
- *7: SA = Address of the sector to be erased. The combination of A_{21} , A_{20} , A_{19} , A_{18} , A_{17} , A_{16} , A_{15} , A_{14} , A_{13} , and A_{12} will uniquely select any sector.
- *8: BA = Bank Address (A_{21} , A_{20} , A_{19})
- *9: RD = Data read from location RA during read operation.
- *10:PD = Data to be programmed at location PA. Data is latched on the rising edge of write pulse.
- *11:SPA = Sector group address to be protected. Set sector group address and (A_6 , A_3 , A_2 , A_1 , A_0) = (0, 0, 0, 1, 0).
- *12:SD = Sector group protection verify data. Output 01h at protected sector group addresses and output 00h at unprotected sector group addresses.
- *13:HRA = Address of the HiddenROM area: 000000h to 00007Fh
- *14: HRBA = Bank Address of the HiddenROM area ($A_{21} = A_{20} = A_{19} = V_{\text{IL}}$)

- Notes :
- Address bits A_{21} to $A_{11} = X = \text{"H"}$ or "L" for all address commands except or Program Address (PA), Sector Address (SA), and Bank Address (BA), and Sector Group Address (SPA).
 - Bus operations are defined in "■ DEVICE BUS OPERATION".
 - The system should generate the following address patterns: 555h or 2AAh to addresses A_{10} to A_0
 - Both Read/Reset commands are functionally equivalent, resetting the device to the read mode.
 - The command combinations not described in this table are illegal.

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Storage Temperature	T _{stg}	-55	+125	°C
Ambient Temperature with Power Applied	T _A	-30	+85	°C
Voltage with Respect to Ground All pins *1	V _{IN}	-0.3	V _{ccf} + 0.3	V
	V _{OUT}	-0.3	V _{ccf} + 0.3	V
V _{ccf} Supply *1	V _{ccf}	-0.2	+3.6	V
V _{ccr} Supply *1	V _{ccr}	-0.2	+3.6	V
$\overline{\text{RESET}}$ *2	V _{IN}	-0.5	+13.0	V
$\overline{\text{WP/ACC}}$ *3	V _{IN}	-0.5	+10.5	V

*1: Minimum DC voltage on input or I/O pins is -0.3 V. During voltage transitions, input or I/O pins may undershoot V_{SS} to -1.0 V for periods of up to 20 ns. Maximum DC voltage on input or I/O pins is V_{ccf}+0.3 V or V_{ccr}+0.3 V. During voltage transitions, input or I/O pins may overshoot to V_{ccf}+1.0 V or V_{ccr}+1.0 V for periods of up to 5 ns.

*2: Minimum DC input voltage on $\overline{\text{RESET}}$ pin is -0.5 V. During voltage transitions, $\overline{\text{RESET}}$ pin may undershoot V_{SS} to -2.0 V for periods of up to 20 ns.
Voltage difference between input and supply voltage (V_{IN}-V_{ccf} or V_{ccr}) does not exceed 9.0 V.
Maximum DC input voltage on $\overline{\text{RESET}}$ pin is +13.0 V which may overshoot to +14.0 V for periods of up to 20 ns.

*3: Minimum DC input voltage on $\overline{\text{WP/ACC}}$ pin is -0.5 V. During voltage transitions, $\overline{\text{WP/ACC}}$ pin may undershoot V_{SS} to -2.0 V for periods of up to 20 ns. Maximum DC input voltage on $\overline{\text{WP/ACC}}$ pin is +10.5 V which may overshoot to +10.5 V for periods of up to 20 ns, when V_{ccf} is applied.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value		Unit
		Min	Max	
Ambient Temperature	T _A	-30	+85	°C
V _{ccf} Supply Voltages	V _{ccf}	+2.7	+3.1	V
V _{ccr} Supply Voltages	V _{ccr}	+2.7	+3.1	V

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

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■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics*1,*2,*3

Parameter	Symbol	Test Conditions	Value			Unit	
			Min	Typ	Max		
Input Leakage Current	I_{LI}	$V_{IN} = V_{SS}$ to V_{CCf} , V_{CCr}	-1.0	—	+1.0	μA	
Output Leakage Current	I_{LO}	$V_{OUT} = V_{SS}$ to V_{CCf} , V_{CCr}	-1.0	—	+1.0	μA	
\overline{RESET} Inputs Leakage Current	I_{LIT}	$V_{CCf} = V_{CCf Max}$, $\overline{RESET} = 12.5 V$	—	—	35	μA	
Flash V_{CC} Active Current (Read) *4	I_{CC1f}	$\overline{CE}f = V_{IL}$, $\overline{OE} = V_{IH}$	$t_{CYCLE} = 5 MHz$	—	—	18	mA
			$t_{CYCLE} = 1 MHz$	—	—	4	mA
Flash V_{CC} Active Current (Program/Erase) *5	I_{CC2f}	$\overline{CE}f = V_{IL}$, $\overline{OE} = V_{IH}$	—	—	30	mA	
Flash V_{CC} Active Current (Read-While-Program) *8	I_{CC3f}	$\overline{CE}f = V_{IL}$, $\overline{OE} = V_{IH}$	—	—	48	mA	
Flash V_{CC} Active Current (Read-While-Erase) *8	I_{CC4f}	$\overline{CE}f = V_{IL}$, $\overline{OE} = V_{IH}$	—	—	48	mA	
Flash V_{CC} Active Current (Erase-Suspend-Program)	I_{CC5f}	$\overline{CE}f = V_{IL}$, $\overline{OE} = V_{IH}$	—	—	30	mA	
\overline{WP}/ACC Acceleration Program Current	I_{ACC}	$V_{CCf} = V_{CCf Max}$, $\overline{WP}/ACC = V_{ACC Max}$	—	—	20	mA	
FCRAM V_{CC} Active Current	I_{CC1r}	$V_{CCf} = V_{CCf Max}$, $\overline{CE}1r = V_{IL}$, $\overline{CE}2r = V_{IH}$, $V_{IN} = V_{IH}$ or V_{IL} , $I_{OUT} = 0 mA$	$t_{RC} / t_{WC} = Min$	—	—	25	mA
			$t_{RC} / t_{WC} = 1 \mu s$	—	—	3	
Flash V_{CC} Standby Current	I_{SB1f}	$V_{CCf} = V_{CCf Max}$, $\overline{CE}f = V_{CCf} \pm 0.3 V$ $\overline{RESET} = V_{CCf} \pm 0.3 V$, $\overline{WP}/ACC = V_{CCf} \pm 0.3 V$	—	1	5	μA	
Flash V_{CC} Standby Current (RESET)	I_{SB2f}	$V_{CCf} = V_{CCf Max}$, $\overline{RESET} = V_{SS} \pm 0.3 V$, $\overline{WP}/ACC = V_{CCf} \pm 0.3 V$	—	1	5	μA	
Flash V_{CC} Current (Automatic Sleep Mode)*6	I_{SB3f}	$V_{CCf} = V_{CCf Max}$, $\overline{CE}f = V_{SS} \pm 0.3 V$ $\overline{RESET} = V_{CCf} \pm 0.3 V$, $\overline{WP}/ACC = V_{CCf} \pm 0.3 V$ $V_{IN} = V_{CCf} \pm 0.3 V$ or $V_{SS} \pm 0.3 V$	—	1	5	μA	
FCRAM V_{CC} Standby Current	I_{SB1r}	$V_{CCr} = V_{CCr Max}$, $\overline{CE}1r \geq V_{CCr} - 0.2 V$, $\overline{CE}2r \geq V_{CCr} - 0.2 V$, $V_{IN} \leq 0.2 V$ or $V_{CCr} - 0.2 V$	—	—	100	μA	
FCRAM V_{CC} Power Down Current	I_{PDSf}	$V_{CCf} = V_{CCf Max}$, $\overline{CE}1r \geq V_{CCf} - 0.2 V$, $\overline{CE}2r \leq 0.2 V$	Sleep	—	—	10	μA
	I_{PDNf}		NAP	—	—	60	μA
	I_{PD8f}		8M Partial	—	—	70	μA

(Continued)

(Continued)

Parameter	Symbol	Test Conditions	Value			Unit
			Min	Typ	Max	
Input Low Level	V_{IL}	—	-0.3	—	0.5	V
Input High Level	V_{IH}	—	Flash	2.0	—	$V_{ccf}+0.3$
			FCRAM	2.2		$V_{ccr}+0.3$
Voltage for Autoselect and Sector Protection (RESET)*7	V_{ID}	—	11.5	—	12.5	V
Voltage for \overline{WP}/ACC Sector Protection/Unprotection and Program Acceleration	V_{ACC}	—	8.5	9.0	9.5	V
FCRAM Output Low Level	V_{OL}	$V_{ccr} = V_{ccr} \text{ Min}, I_{oL} = 1.0 \text{ mA}$	—	—	0.4	V
FCRAM Output High Level	V_{OH}	$V_{ccr} = V_{ccr} \text{ Min}, I_{oH} = -0.5 \text{ mA}$	2.2	—	—	V
Flash Output Low Level	V_{OL}	$V_{ccf} = V_{ccf} \text{ Min}, I_{oL} = 4.0 \text{ mA}$	—	—	0.45	V
Flash Output High Level	V_{OH}	$V_{ccf} = V_{ccf} \text{ Min}, I_{oH} = -0.1 \text{ mA}$	$V_{ccf}-0.4$	—	—	V
Flash Low V_{CC} Lock-Out Voltage	V_{LKO}	—	2.3	2.4	2.5	V

*1 : All voltage are referenced to V_{SS} .

*2 : FCRAM DC characteristics are measured after following POWER-UP timing.

*3 : I_{OUT} depends on the output load conditions.

*4 : The I_{CC} current listed includes both the DC operating current and the frequency dependent component.

*5 : I_{CC} active while Embedded Algorithm (program or erase) is in progress.

*6 : Automatic sleep mode enables the low power mode when address remain stable for 150 ns.

*7 : Applicable for only V_{CC} applying.

*8 : Embedded Alogorithm (program or erase) is in progress. (@5MHz)

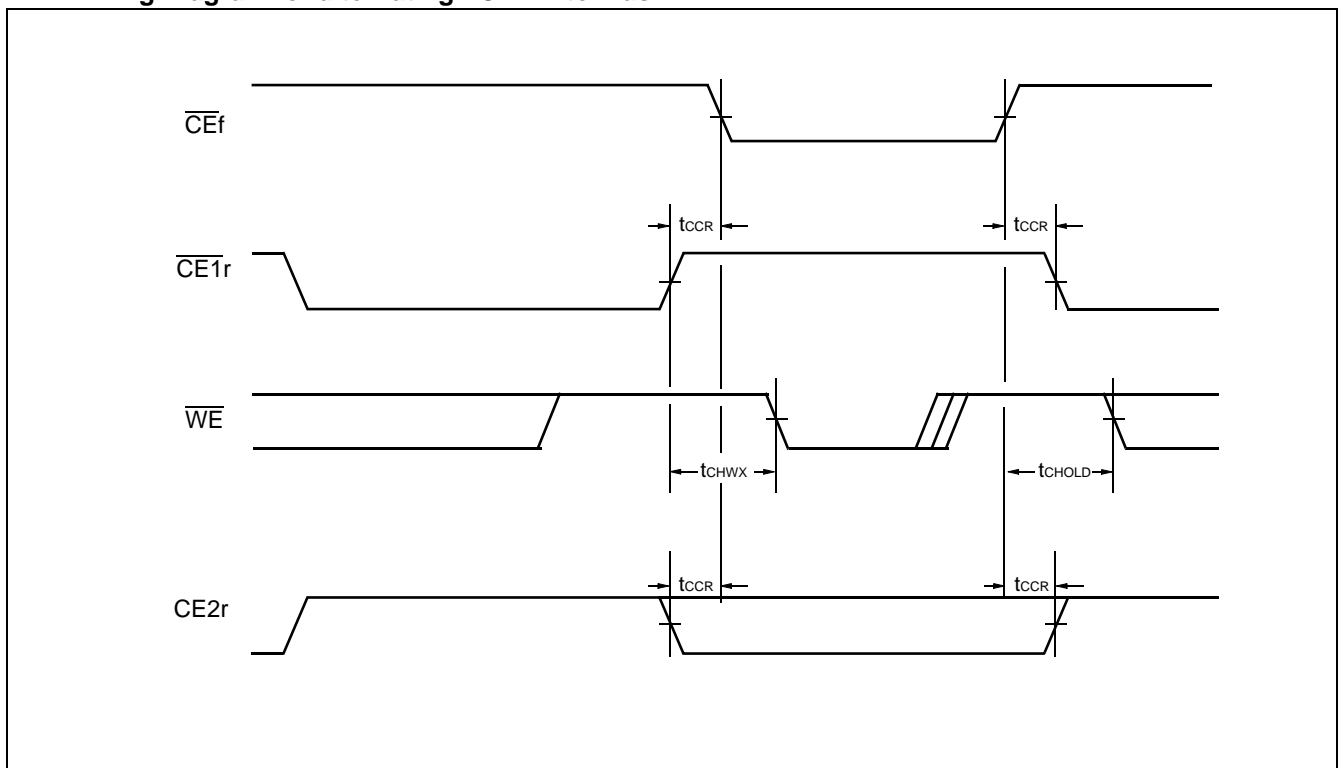
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2. AC Characteristics

• CE Timing

Parameter	Symbol		Condition	Value	Unit
	JEDEC	Standard		Min	
$\overline{\text{CE}}$ Recover Time	—	t_{CCR}	—	0	ns
$\overline{\text{CE}}$ Hold Time	—	t_{CHOLD}	—	3	ns
$\overline{\text{CE1r}}$ High to $\overline{\text{WE}}$ Invalid time for Standby Entry	—	t_{CHWX}	—	10	ns

• Timing Diagram for alternating FCRAM to Flash



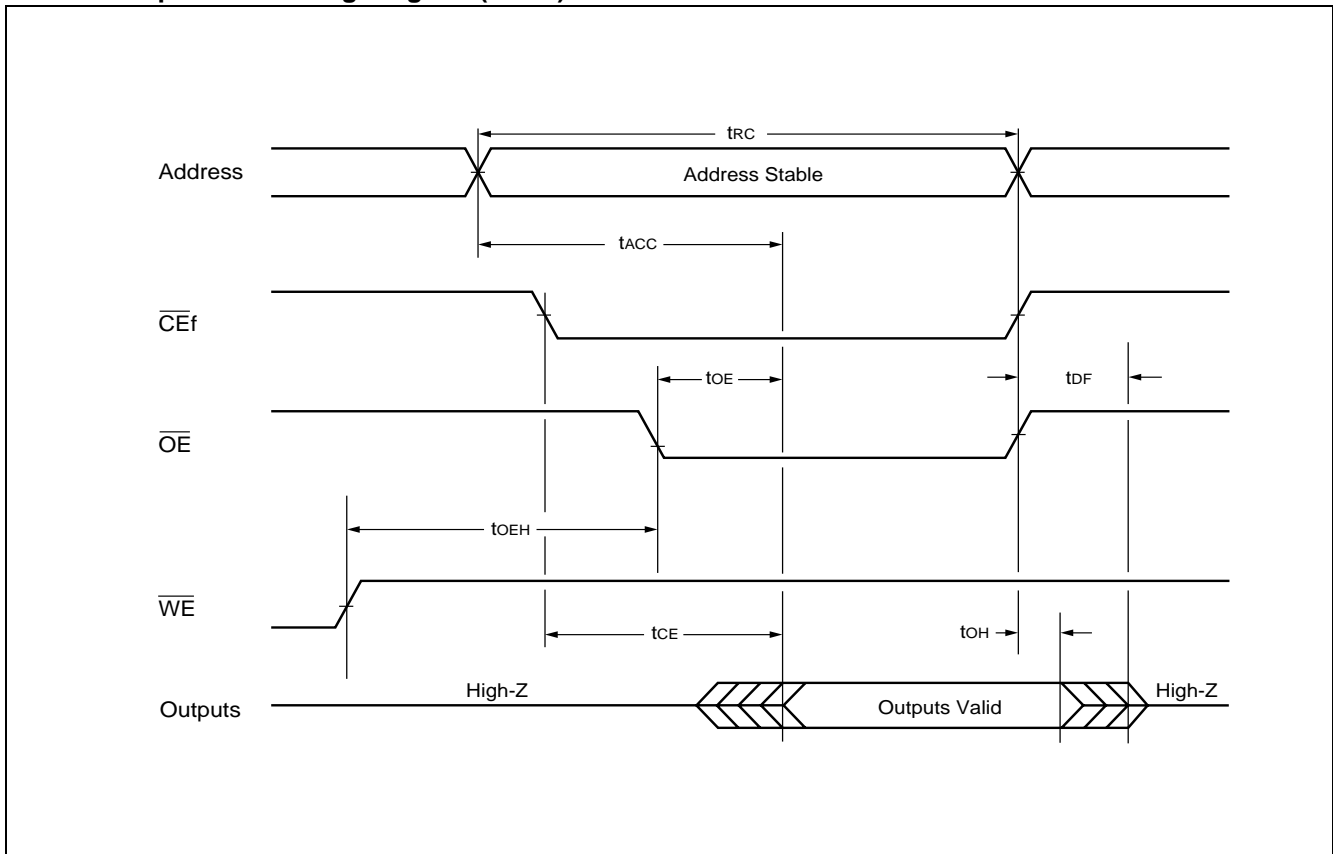
• Read Only Operations Characteristics (Flash)

Parameter	Symbol		Condition	Value *		Unit
	JEDEC	Standard		Min	Max	
Read Cycle Time	t_{AVAV}	t_{RC}	—	70	—	ns
Address to Output Delay	t_{AVQV}	t_{ACC}	$\overline{CE}f = V_{IL}$ $\overline{OE} = V_{IL}$	—	70	ns
Chip Enable to Output Delay	t_{ELQV}	t_{CEf}	$\overline{OE} = V_{IL}$	—	70	ns
Output Enable to Output Delay	t_{GLQV}	t_{OE}	—	—	30	ns
Chip Enable to Output High-Z	t_{EHQZ}	t_{DF}	—	—	25	ns
Output Enable to Output High-Z	t_{GHQZ}	t_{DF}	—	—	25	ns
Output Hold Time From Addresses, $\overline{CE}f$ or \overline{OE} , Whichever Occurs First	t_{AXQX}	t_{OH}	—	0	—	ns
\overline{RESET} Pin Low to Read Mode	—	t_{READY}	—	—	20	μs

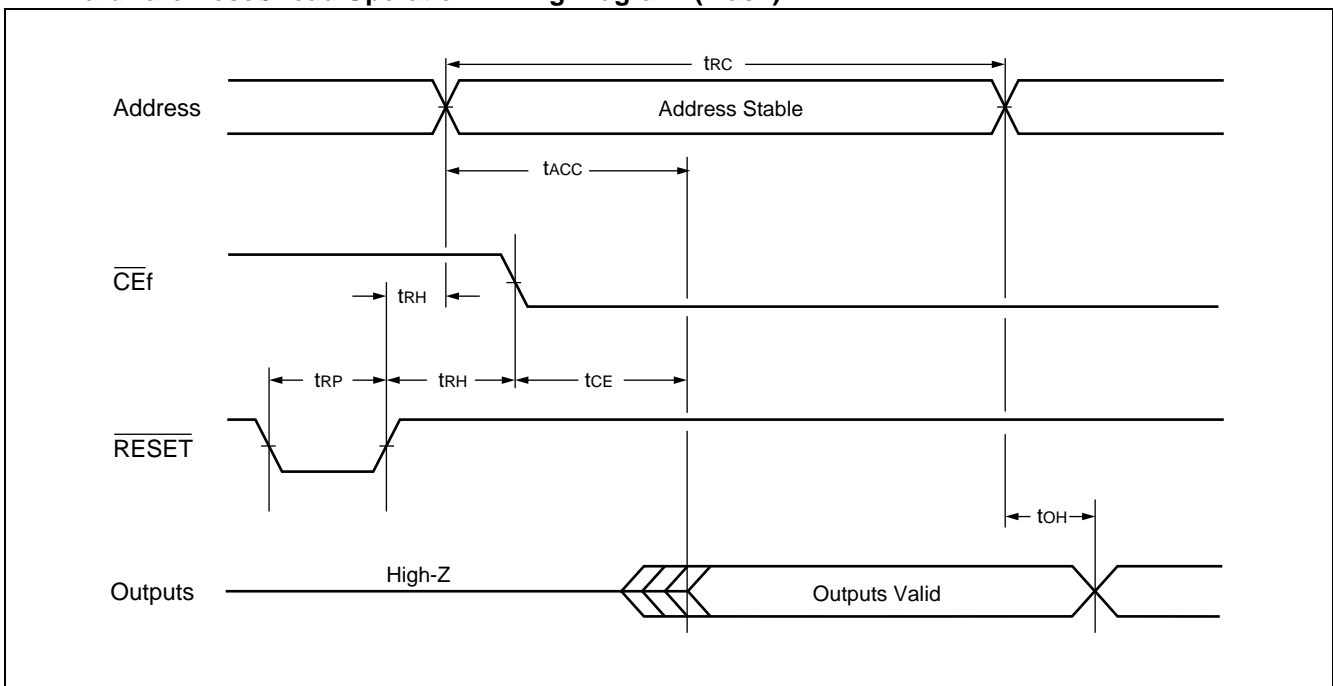
*: Test Conditions— Output Load: 1 TTL gate and 30 pF
 Input rise and fall times: 5 ns
 Input pulse levels: 0.0 V or V_{CCf}
 Timing measurement reference level
 Input: $0.5 \times V_{CCf}$
 Output: $0.5 \times V_{CCf}$

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• Read Operation Timing Diagram (Flash)



• Hardware Reset/Read Operation Timing Diagram (Flash)



• Write/Erase/Program Operations (Flash)

Parameter		Symbol		Value			Unit
		JEDEC	Standard	Min	Typ	Max	
Write Cycle Time		t _{AVAV}	t _{WC}	70	—	—	ns
Address Setup Time		t _{AVWL}	t _{AS}	0	—	—	ns
Address Setup Time to \overline{OE} Low During Toggle Bit Polling		—	t _{ASO}	12	—	—	ns
Address Hold Time		t _{WLAX}	t _{AH}	45	—	—	ns
Address Hold Time from \overline{CEf} or \overline{OE} High During Toggle Bit Polling		—	t _{AHT}	0	—	—	ns
Data Setup Time		t _{DVWH}	t _{DS}	30	—	—	ns
Data Hold Time		t _{WHDX}	t _{DH}	0	—	—	ns
Output Enable Hold Time	Read	—	t _{OEHL}	0	—	—	ns
	Toggle and \overline{Data} Polling			10	—	—	ns
\overline{CEf} High During Toggle Bit Polling		—	t _{CEPH}	20	—	—	ns
\overline{OE} High During Toggle Bit Polling		—	t _{OEHL}	20	—	—	ns
Read Recover Time Before Write		t _{GHWL}	t _{GHWL}	0	—	—	ns
Read Recover Time Before Write		t _{GHEL}	t _{GHEL}	0	—	—	ns
\overline{CEf} Setup Time		t _{ELWL}	t _{CS}	0	—	—	ns
\overline{WE} Setup Time		t _{WLEL}	t _{WS}	0	—	—	ns
\overline{CEf} Hold Time		t _{WHEH}	t _{CH}	0	—	—	ns
\overline{WE} Hold Time		t _{EHWH}	t _{WH}	0	—	—	ns
Write Pulse Width		t _{WLWH}	t _{WP}	35	—	—	ns
\overline{CEf} Pulse Width		t _{ELEH}	t _{CP}	35	—	—	ns
Write Pulse Width High		t _{WHWL}	t _{WPH}	25	—	—	ns
\overline{CEf} Pulse Width High		t _{EHEL}	t _{CPH}	25	—	—	ns
Programming Operation		t _{WHWH1}	t _{WHWH1}	—	6	—	μs
Sector Erase Operation *1		t _{WHWH2}	t _{WHWH2}	—	0.5	—	s
V _{ccf} Setup Time		—	t _{VCS}	50	—	—	μs
Rise Time to V _{ID} *2		—	t _{VIDR}	500	—	—	ns
Rise Time to V _{ACC} *3		—	t _{VACCR}	500	—	—	ns
Voltage Transition Time *2		—	t _{VLHT}	4	—	—	μs
Write Pulse Width *2		—	t _{WPP}	100	—	—	μs

(Continued)

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(Continued)

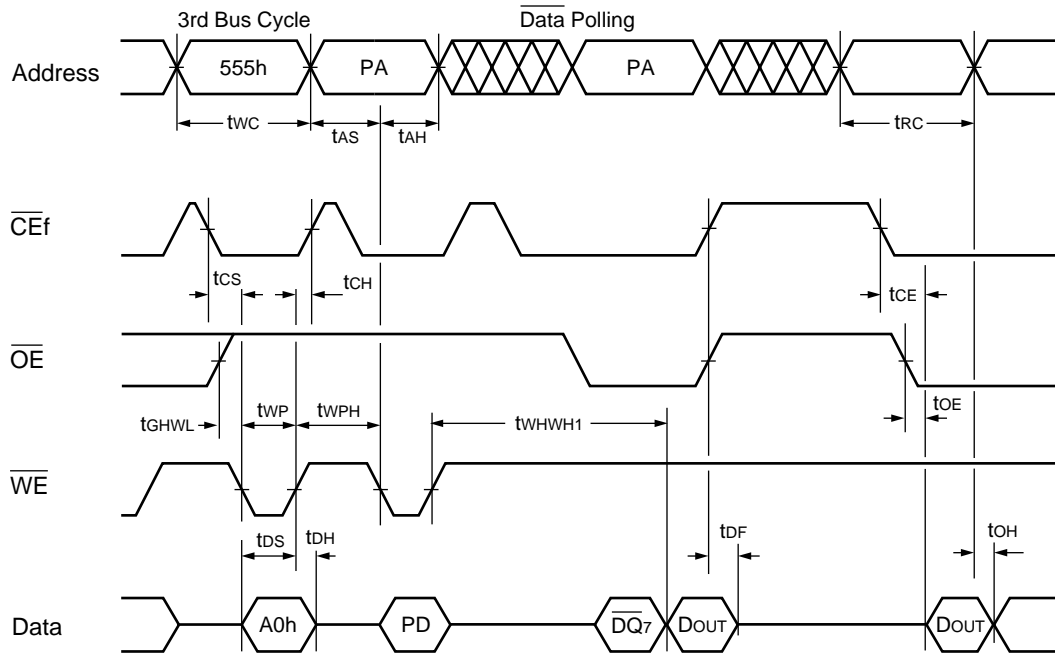
Parameter	Symbol		Value			Unit
	JEDEC	Standard	Min	Typ	Max	
\overline{OE} Setup Time to \overline{WE} Active *2	—	tOESP	4	—	—	μs
\overline{CEf} Setup Time to \overline{WE} Active *2	—	tCSP	4	—	—	μs
Recover Time from RY/ \overline{BY}	—	tRB	0	—	—	ns
\overline{RESET} Pulse Width	—	tRP	500	—	—	ns
\overline{RESET} High Level Period Before Read	—	tRH	200	—	—	ns
Program/Erase Valid to RY/ \overline{BY} Delay	—	tBUSY	—	—	90	ns
Delay Time from Embedded Output Enable	—	tEOE	—	—	70	ns
Erase Time-out Time	—	tTOW	50	—	—	μs
Erase Suspend Transition Time	—	tSPD	—	—	20	μs

*1: This does not include preprogramming time.

*2: This timing is for Sector Group Protection operation.

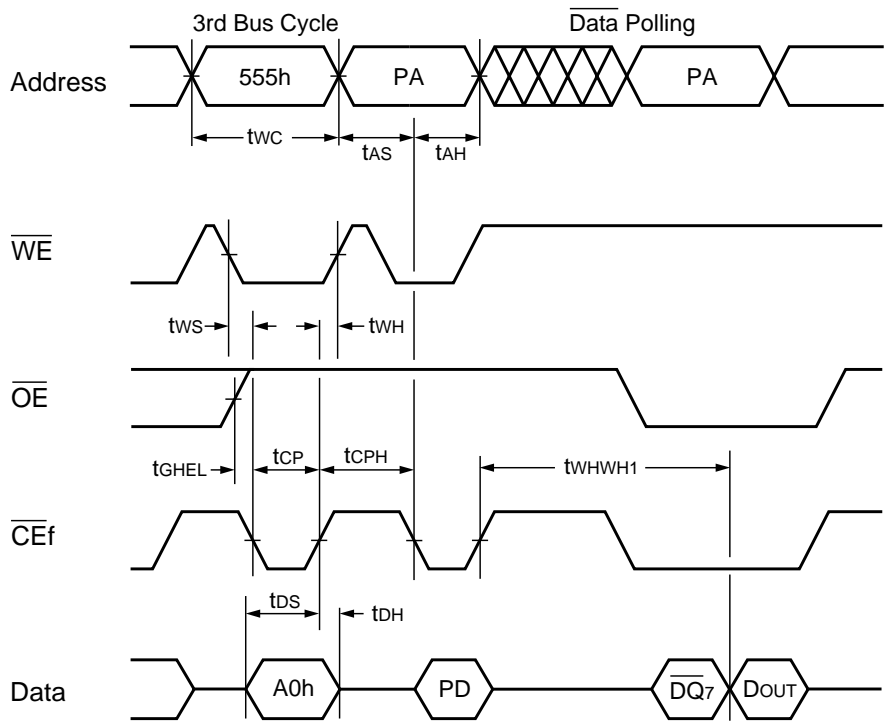
*3: This timing is for Accelerated Program operation.

• Write Cycle (\overline{WE} control) (Flash)



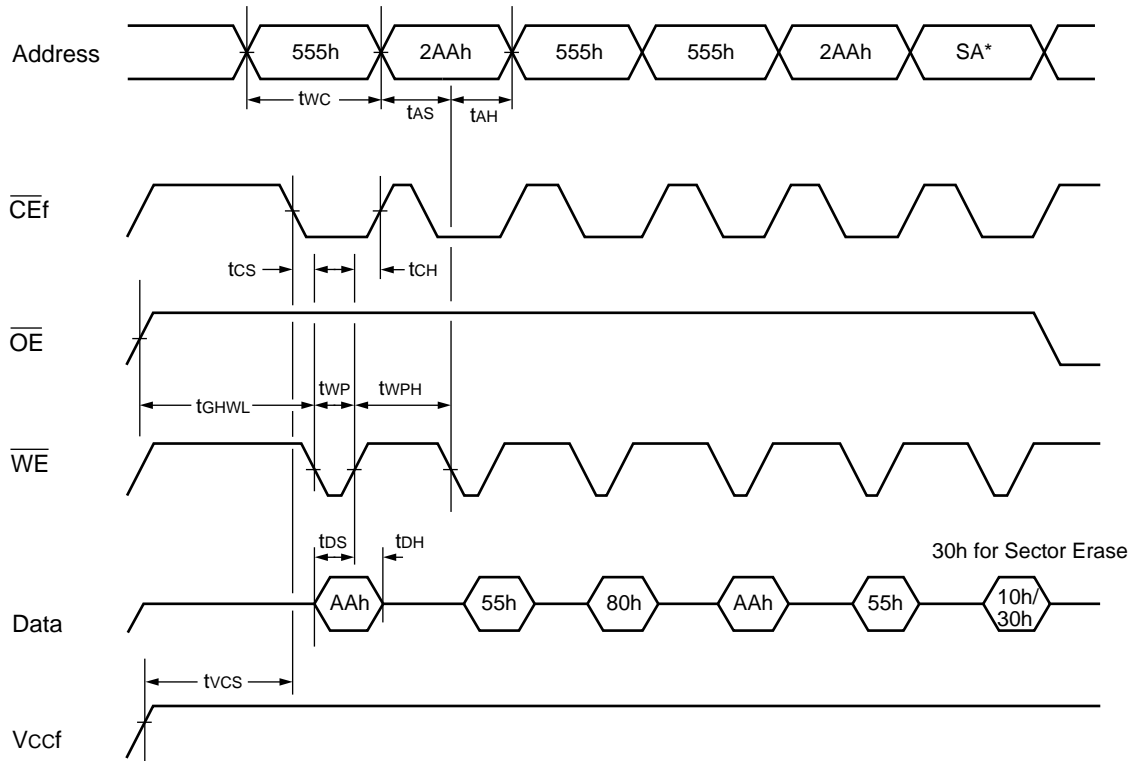
- Notes :
- PA is address of the memory location to be programmed.
 - PD is data to be programmed at word address.
 - \overline{DQ}_7 is the output of the complement of the data written to the device.
 - D_{OUT} is the output of the data written to the device.
 - Figure indicates last two bus cycles out of four bus cycle sequence.

• Write Cycle ($\overline{\text{CEf}}$ control) (Flash)



- Notes :
- PA is address of the memory location to be programmed.
 - PD is data to be programmed at word address.
 - $\overline{\text{DQ7}}$ is the output of the complement of the data written to the device.
 - DOUT is the output of the data written to the device.
 - Figure indicates last two bus cycles out of four bus cycle sequence.

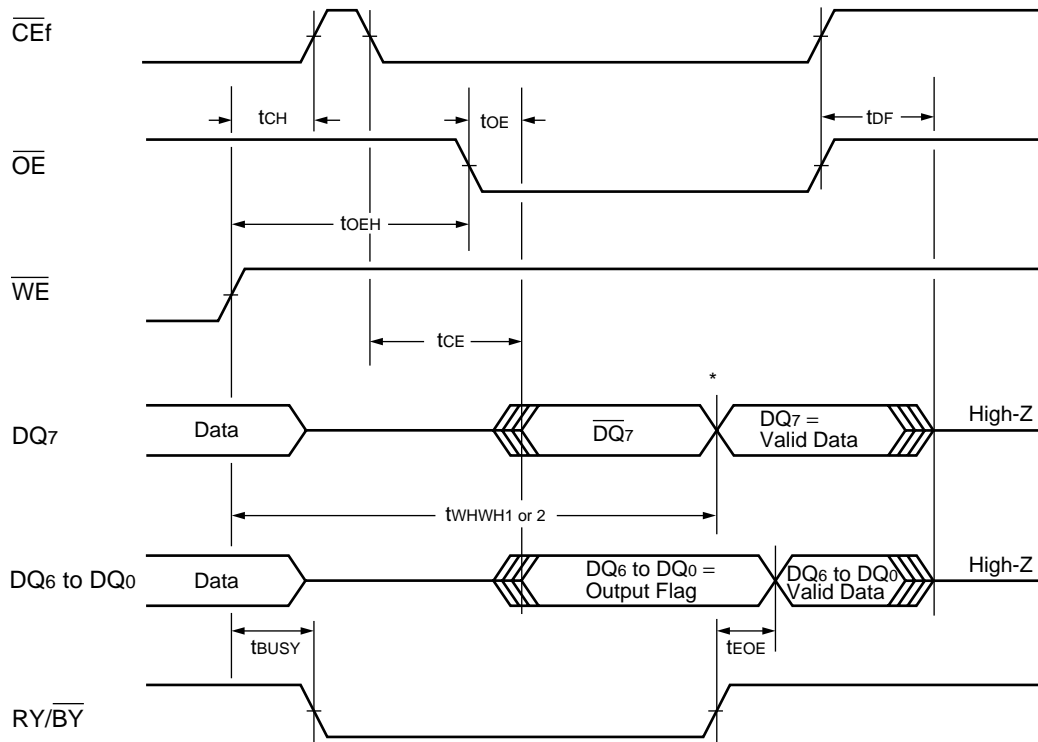
• AC Waveforms Chip/Sector Erase Operations (Flash)



* : SA is the sector address for Sector Erase. Addresses = 555h (Word) for Chip Erase.

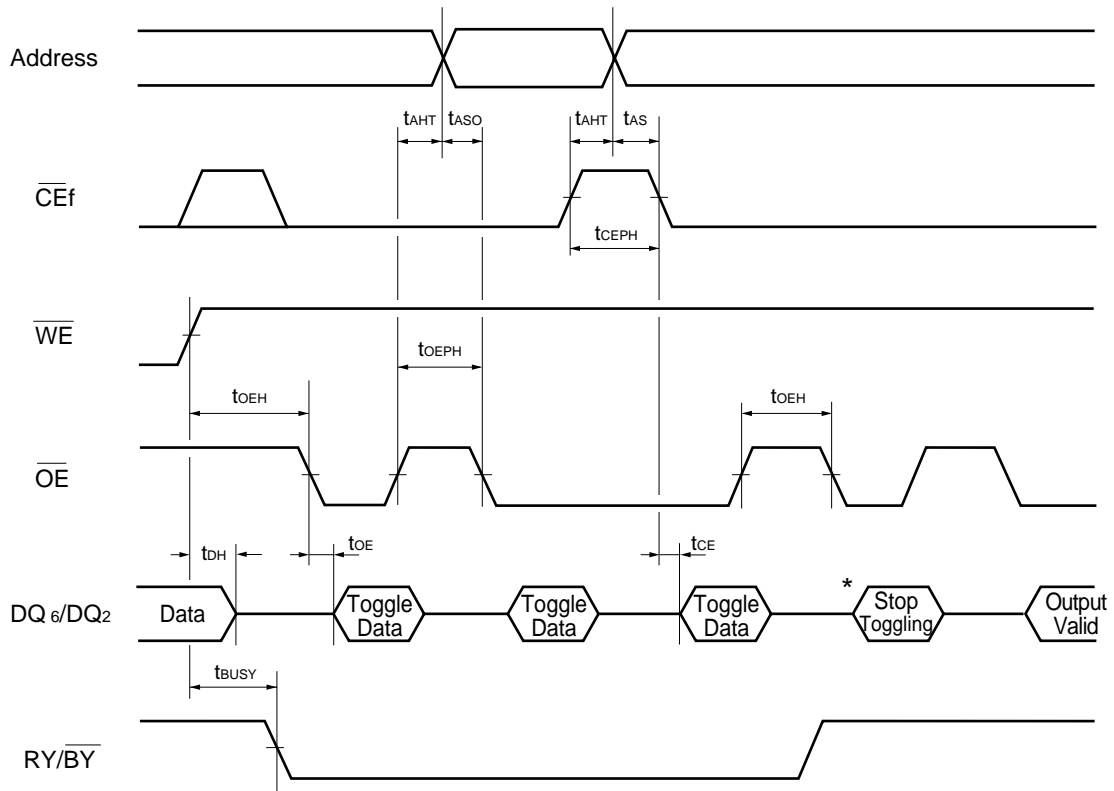
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• AC Waveforms for Data Polling during Embedded Algorithm Operations (Flash)



* : $DQ7 = \text{Valid Data}$ (the device has completed the Embedded operation) .

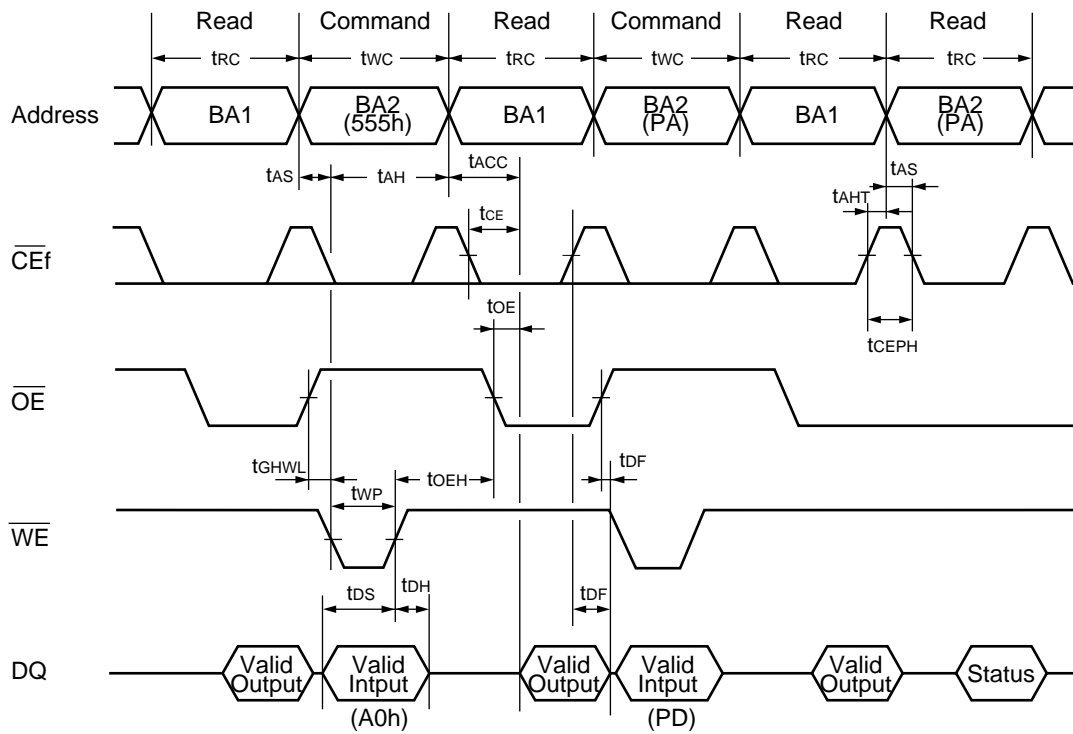
• AC Waveforms for Toggle Bit during Embedded Algorithm Operations (Flash)



* : DQ₆ stops toggling (the device has completed the Embedded operation).

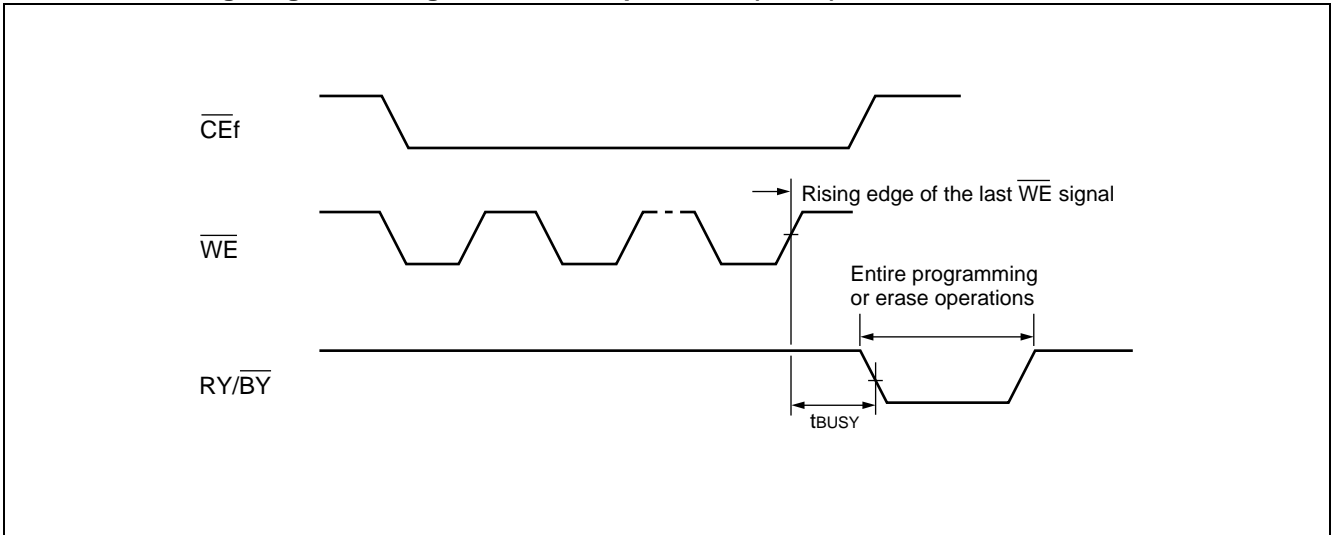
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• Back-to-back Read/Write Timing Diagram (Flash)

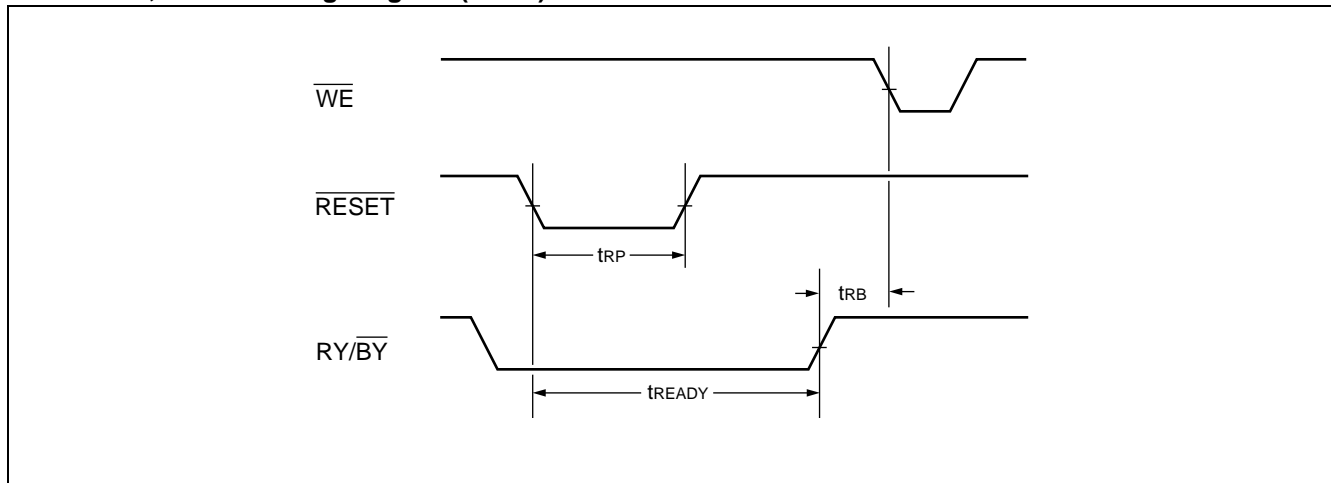


Note : This is example of Read for Bank 1 and Embedded Algorithm (program) for Bank 2.
 BA1 : Address corresponding to Bank 1
 BA2 : Address corresponding to Bank 2

• RY/BY Timing Diagram during Write/Erase Operations (Flash)

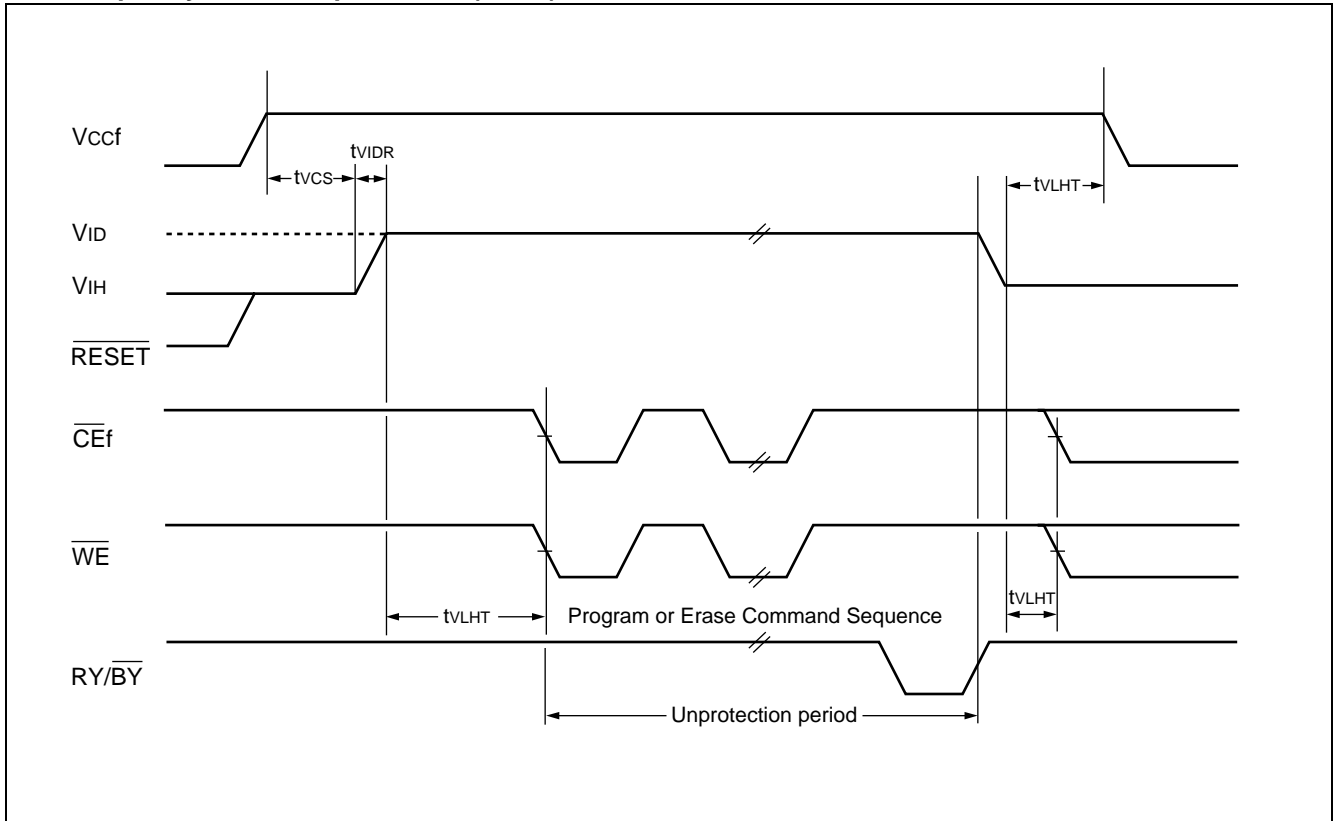


• RESET, RY/BY Timing Diagram (Flash)

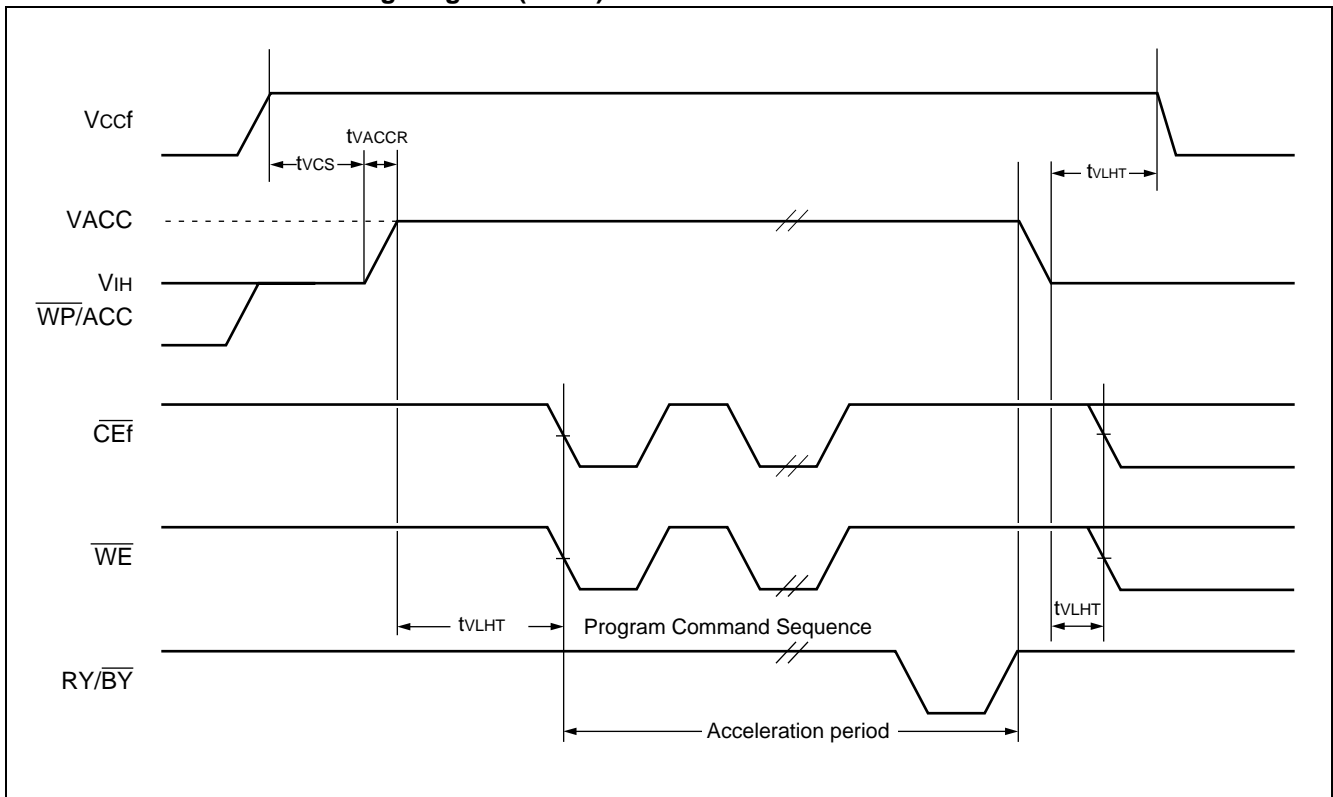


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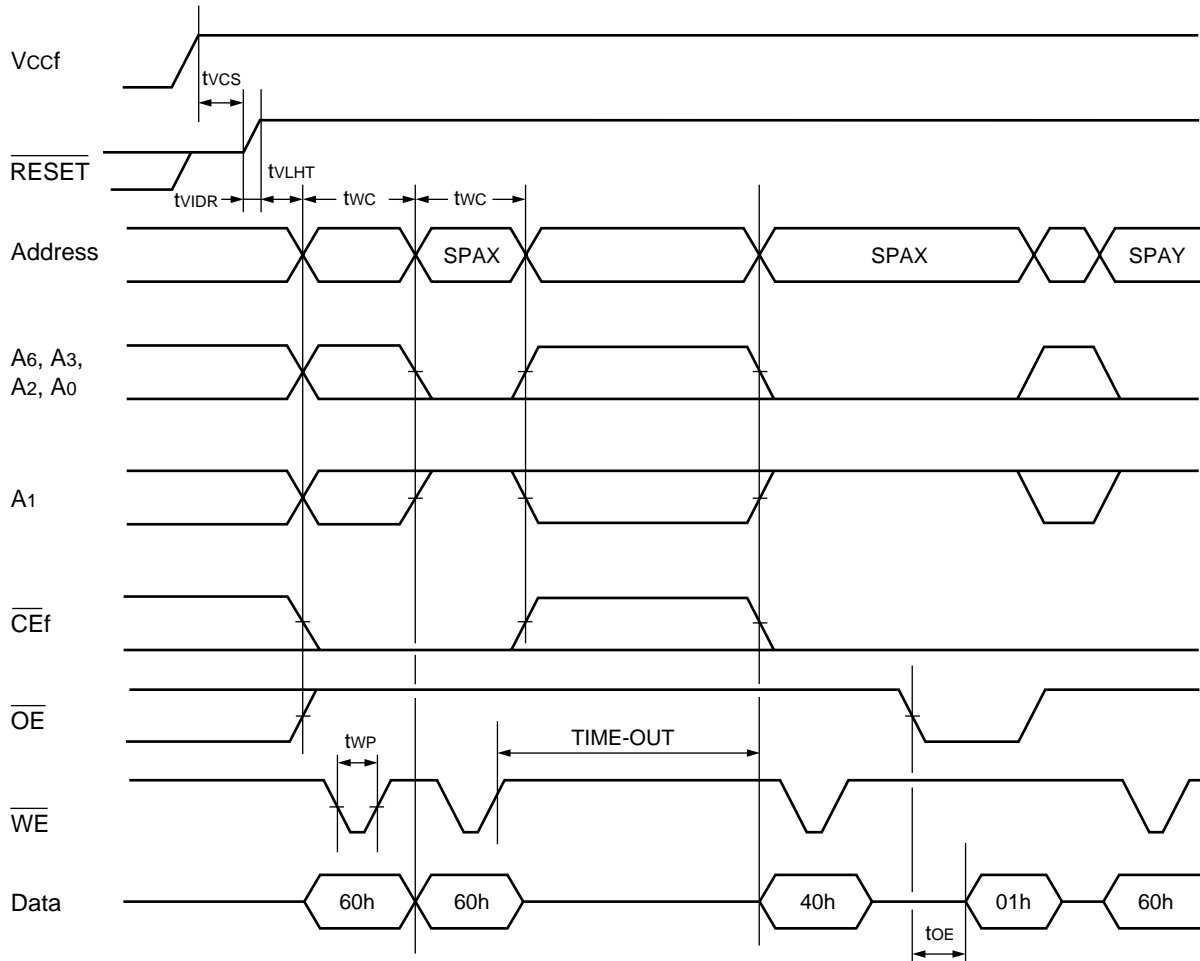
• Temporary Sector Unprotection (Flash)



• Acceleration Mode Timing Diagram (Flash)



• Extended Sector Group Protection (Flash)

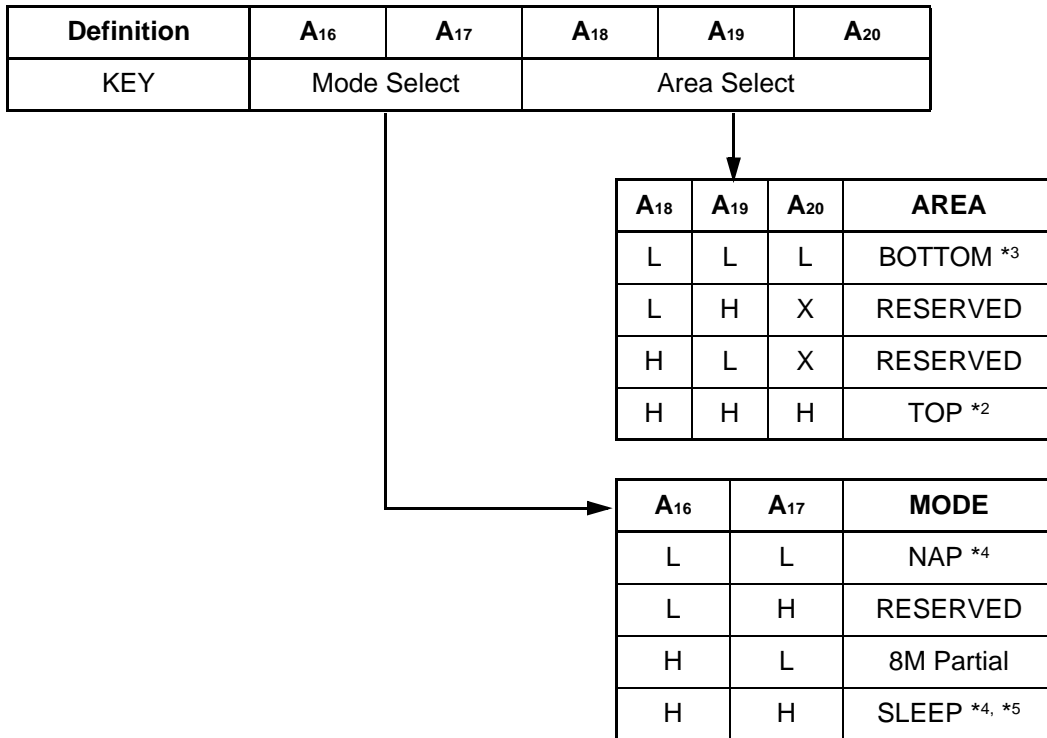


SPAX : Sector Group Address to be protected
 SPAY : Next Sector Group Address to be protected
 TIME-OUT : Time-Out window = 250 μ s (Min)

■ 32M FCRAM CHARACTERISTICS for MCP

1. FCRAM Power Down Program Key Table*1

Basic Key Table



Available Key Table

MODE	A ₁₆	A ₁₇	A ₁₈	A ₁₉	A ₂₀	Data Retention Area
	Mode Select		Area Select			
NAP	L	L	X	X	X	None
8M Partial	H	L	L	L	L	Bottom 8M only
	H	L	H	H	H	Top 8M only
SLEEP	H	H	X	X	X	None

*1 : The Power Down Program can be performed one time after compliance of Power-up timings and it should not be re-programmed after regular Read or Write.

Unspecified addresses, A₁₅ to A₀, can be either High or Low during the programming.

The RESERVED key should not be used.

*2 : TOP area is from the lowest address location. (i.e., A₂₀ to A₀ = L)

*3 : BOTTOM area is from the highest address location. (i.e., A₂₀ to A₀ = H)

*4 : NAP and SLEEP do not retain the data and Area Select is ignored.

*5 : Default state. Power Down Program to this SLEEP mode can be omitted.

2. AC Characteristics

• READ OPERATION (FCRAM)

Parameter	Symbol	Value		Unit	Notes
		Min	Max		
Read Cycle Time	t _{RC}	70	—	ns	
Chip Enable Access Time	t _{CE}	—	65	ns	*1,*3
Output Enable Access Time	t _{OE}	—	40	ns	*1
Address Access Time	t _{AA}	—	65	ns	*1,*4
Output Data Hold Time	t _{OH}	5	—	ns	*1
$\overline{\text{CE}}1\text{r}$ Low to Output Low-Z	t _{CLZ}	5	—	ns	*2
$\overline{\text{OE}}$ Low to Output Low-Z	t _{OLZ}	0	—	ns	*2
$\overline{\text{CE}}1\text{r}$ High to Output High-Z	t _{CHZ}	—	20	ns	*2
$\overline{\text{OE}}$ High to Output High-Z	t _{OHZ}	—	20	ns	*2
Address Setup Time to $\overline{\text{CE}}1\text{r}$ Low	t _{ASC}	-5	—	ns	*5
Address Setup Time to $\overline{\text{OE}}$	t _{ASO}	25	—	ns	*3,*6
	t _{ASO(ABS)}	10	—	ns	*7
$\overline{\text{LB}} / \overline{\text{UB}}$ Setup Time to $\overline{\text{CE}}1\text{r}$ Low	t _{BSC}	-5	—		*5
$\overline{\text{LB}} / \overline{\text{UB}}$ Setup Time to $\overline{\text{OE}}$ Low	t _{BSO}	10	—		
Address Invalid Time	t _{AX}	—	5	ns	*4,*8
Address Hold Time from $\overline{\text{CE}}1\text{r}$ Low	t _{CLAH}	70	—	ns	*4
Address Hold Time from $\overline{\text{OE}}$ Low	t _{OLAH}	45	—	ns	*4,*9
Address Hold Time from $\overline{\text{CE}}1\text{r}$ High	t _{CHAH}	-5	—	ns	
Address Hold Time from $\overline{\text{OE}}$ High	t _{OHAH}	-5	—	ns	
$\overline{\text{LB}} / \overline{\text{UB}}$ Hold Time from $\overline{\text{CE}}1\text{r}$ High	t _{CHBH}	-5	—		
$\overline{\text{LB}} / \overline{\text{UB}}$ Hold Time from $\overline{\text{OE}}$ High	t _{OHBH}	-5	—		
$\overline{\text{CE}}1\text{r}$ Low to $\overline{\text{OE}}$ Low Delay Time	t _{CLOL}	25	1000	ns	*3,*6,*9,*10
$\overline{\text{OE}}$ Low to $\overline{\text{CE}}1\text{r}$ High Delay Time	t _{OLCH}	45	—	ns	*9
$\overline{\text{CE}}1\text{r}$ High Pulse Width	t _{CP}	12	—	ns	
$\overline{\text{OE}}$ High Pulse Width	t _{OP}	25	1000	ns	*6,*9,*10
	t _{OP(ABS)}	12	—	ns	*7

*1 : The output load is 30 pF.

*2 : The output load is 5 pF.

*3 : The t_{CE} is applicable if $\overline{\text{OE}}$ is brought to Low before $\overline{\text{CE}}1\text{r}$ goes Low and is also applicable if actual value of both or either t_{ASO} or t_{CLOL} is shorter than specified value.

*4 : Applicable only to A₀ and A₁ when both $\overline{\text{CE}}1\text{r}$ and $\overline{\text{OE}}$ are kept at Low for the address access.

*5 : Applicable if $\overline{\text{OE}}$ is brought to Low before $\overline{\text{CE}}1\text{r}$ goes Low.

*6 : The t_{ASO}, t_{CLOL}(Min) and t_{OP}(Min) are reference values when the access time is determined by t_{OE}. If actual value of each parameter is shorter than specified minimum value, t_{OE} become longer by the amount of subtracting actual value from specified minimum value.

For example, if actual t_{ASO}, t_{ASO}(actual), is shorter than specified minimum value, t_{ASO}(Min), during $\overline{\text{OE}}$ control access (ie., $\overline{\text{CE}}1\text{r}$ stays Low), the t_{OE} become t_{OE}(Max) + t_{ASO}(Min) - t_{ASO}(actual).

*7 : The t_{ASO(ABS)} and t_{OP(ABS)} is the absolute minimum value during $\overline{\text{OE}}$ control access.

*8 : The t_{AX} is applicable when both A₀ and A₁ are switched from previous state.

*9 : If actual value of either t_{CLOL} or t_{OP} is shorter than specified minimum value, both t_{OLAH} and t_{OLCH} become t_{RC}(Min) - t_{CLOL}(actual) or t_{RC}(Min) - t_{OP}(actual).

*10 : Maximum value is applicable if $\overline{\text{CE}}1\text{r}$ is kept at Low.

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• WRITE OPERATION (FCRAM)

Parameter	Symbol	Value		Unit	Notes
		Min	Max		
Write Cycle Time	t_{WC}	70	—	ns	*1
Address Setup Time	t_{AS}	0	—	ns	*2
Address Hold Time	t_{AH}	35	—	ns	*2
$\overline{CE1r}$ Write Setup Time	t_{CS}	0	1000	ns	
$\overline{CE1r}$ Write Hold Time	t_{CH}	0	1000	ns	
\overline{WE} Setup Time	t_{WS}	0	—	ns	
\overline{WE} Hold Time	t_{WH}	0	—	ns	
\overline{LB} and \overline{UB} Setup Time	t_{BS}	-5	—	ns	
\overline{LB} and \overline{UB} Hold Time	t_{BH}	-5	—	ns	
\overline{OE} Setup Time	t_{OES}	0	1000	ns	*3
\overline{OE} Hold Time	t_{OEH}	25	1000	ns	*3, *4
	$t_{OEH(ABS)}$	12	—	ns	*5
\overline{OE} High to $\overline{CE1r}$ Low Setup Time	t_{OHCL}	-5	—	ns	*6
\overline{OE} High to Address Hold Time	t_{OHAH}	-5	—	ns	*7
$\overline{CE1r}$ Write Pulse Width	t_{CW}	45	—	ns	*1, *8
\overline{WE} Write Pulse Width	t_{WP}	45	—	ns	*1, *8
$\overline{CE1r}$ Write Recovery Time	t_{WRC}	10	—	ns	*1, *9
\overline{WE} Write Recovery Time	t_{WR}	10	1000	ns	*1, *3, *9
Data Setup Time	t_{DS}	15	—	ns	
Data Hold Time	t_{DH}	0	—	ns	
$\overline{CE1r}$ High Pulse Width	t_{CP}	12	—	ns	*9

*1 : Minimum value must be equal or greater then the sum of actual t_{CW} (or t_{WP}) and t_{WRC} (or t_{WR}).

*2 : New write address is valid from either $\overline{CE1r}$ or \overline{WE} is brought to High.

*3 : The t_{OEH} is specified from end of $t_{WC}(\text{Min})$. The $t_{OEH}(\text{Min})$ is a reference value when the access time is determined by t_{OE} .

If actual value, $t_{OEH}(\text{actual})$ is shorter than specified minimum value, t_{OE} become longer by the amount of subtracting actual value from specified minimum value.

*4 : The $t_{OEH}(\text{Max})$ is applicable if $\overline{CE1r}$ is kept at Low and both \overline{WE} and \overline{OE} are kept at High.

*5 : The $t_{OEH(ABS)}$ is the absolute minimum value if write cycle is terminated by \overline{WE} and $\overline{CE1r}$ stays Low.

*6 : $t_{OHCL}(\text{Min})$ must be satisfied if read operation is not performed prior to write operation.

In case \overline{OE} is disabled after $t_{OHCL}(\text{Min})$, \overline{WE} Low must be asserted after $t_{RC}(\text{Min})$ from $\overline{CE1r}$ Low.

In other words, read operation is initiated if $t_{OHCL}(\text{Min})$ is not satisfied.

*7 : Applicable if $\overline{CE1r}$ stays Low after read operation.

*8 : t_{CW} and t_{WP} is applicable if write operation is initiated by $\overline{CE1r}$ and \overline{WE} , respectively.

*9 : t_{WRC} and t_{WR} is applicable if write operation is terminated by $\overline{CE1r}$ and \overline{WE} , respectively.

The $t_{WR}(\text{Min})$ can be ignored if $\overline{CE1r}$ is brought to High together or after \overline{WE} is brought to High.

In such case, the $t_{CP}(\text{Min})$ must be satisfied.

• **POWER DOWN and POWER DOWN PROGRAM PARAMETERS (FCRAM)**

Parameter	Symbol	Value		Unit	Note
		Min	Max		
CE2r Low Setup Time for Power Down Entry	t _{CSP}	10	—	ns	
CE2r Low Hold Time after Power Down Entry	t _{C2LP}	70	—	ns	
$\overline{\text{CE1r}}$ High Hold Time following CE2r High after Power Down Exit (SLEEP mode only)	t _{CHH}	350	—	μs	
$\overline{\text{CE1r}}$ High Setup Time following CE2r High after Power Down Exit (Except for SLEEP mode)	t _{CHHN}	1	—	μs	
$\overline{\text{CE1r}}$ High Setup Time following CE2r High after Power Down Exit	t _{CHS}	10	—	ns	
$\overline{\text{CE1r}}$ High to $\overline{\text{PE}}$ Low Setup Time	t _{EPS}	70	—	ns	*
$\overline{\text{PE}}$ Power Down Program Pulse Width	t _{EP}	70	—	ns	*
$\overline{\text{PE}}$ High to $\overline{\text{CE1r}}$ Low Hold Time	t _{EPH}	70	—	ns	*
Address Setup Time to $\overline{\text{PE}}$ High	t _{EAS}	15	—	ns	*
Address Setup Time from $\overline{\text{PE}}$ High	t _{EAH}	0	—	ns	*

* : Applicable to Power Down Program.

• **OTHER TIMING PARAMETERS (FCRAM)**

Parameter	Symbol	Value		Unit	Note
		Min	Max		
$\overline{\text{CE1r}}$ High to $\overline{\text{OE}}$ Invalid Time for Standby Entry	t _{CHOX}	10	—	ns	
$\overline{\text{CE1r}}$ High to $\overline{\text{WE}}$ Invalid Time for Standby Entry	t _{CHWX}	10	—	ns	*1
CE2r Low Hold Time after Power-up	t _{C2LH}	50	—	ms	*2
CE2r High Hold Time after Power-up	t _{C2HL}	50	—	ms	*3
$\overline{\text{CE1r}}$ High Hold Time following CE2r High after Power-up	t _{CHH}	350	—	ms	*2
Input Transition Time	t _r	1	25	ns	*4

*1 : It may write some data into any address location if t_{CHWX} is not satisfied.

*2 : Must satisfy t_{CHH}(Min) after t_{C2LH}(Min).

*3 : Requires Power Down mode entry and exit after t_{C2HL}.

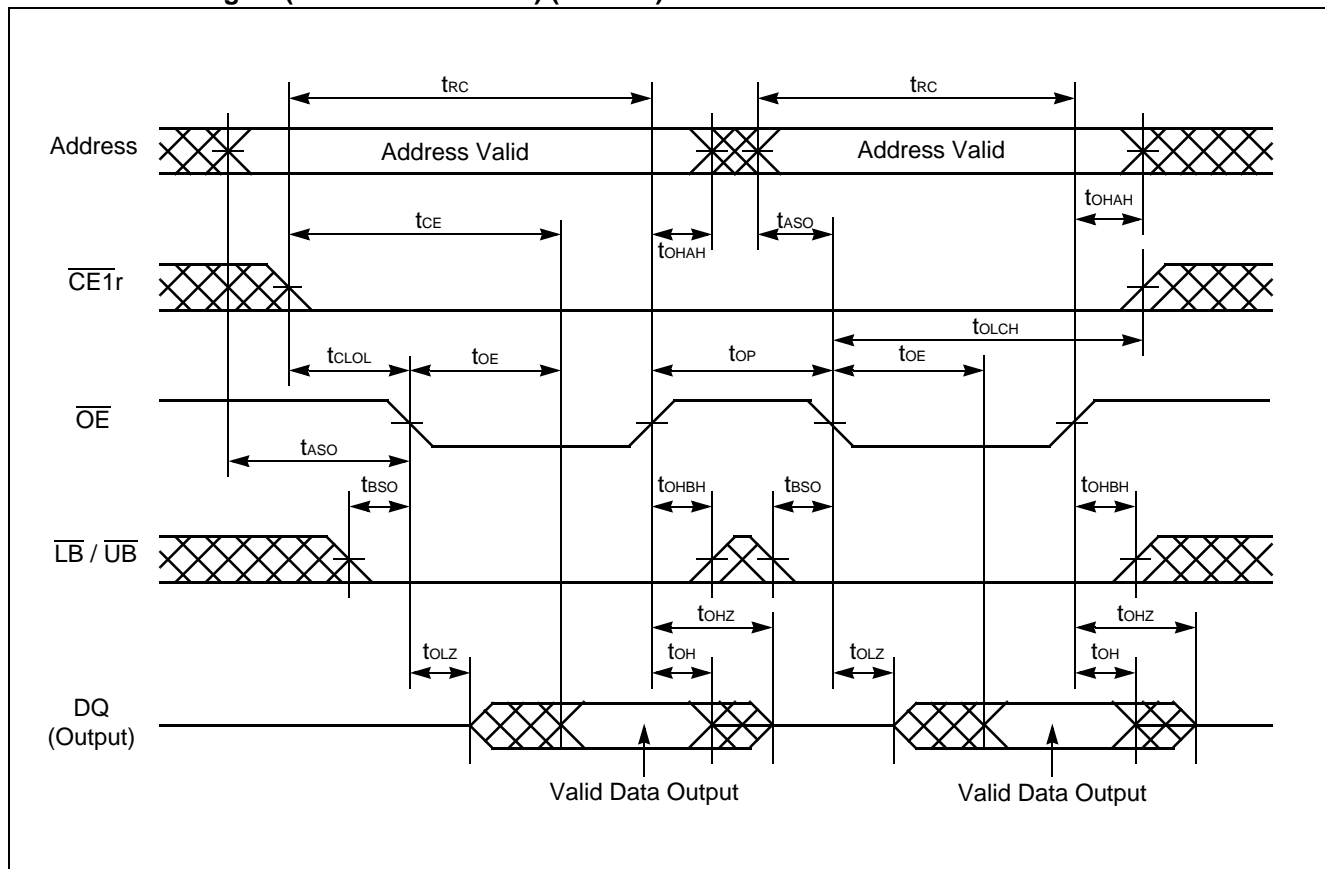
*4 : The input Transition Time(t_r) at AC testing is 5 ns as shown in below. If actual t_r is longer than 5 ns, it may violate AC specification of some timing parameters.

• **AC TEST CONDITIONS (FCRAM)**

Description	Symbol	Test Setup	Value	Unit	Note
Input High Level	V _{IH}	V _{CCF} = 2.7 V to 3.1 V	2.3	V	
Input Low Level	V _{IL}	V _{CCF} = 2.7 V to 3.1 V	0.4	V	
Input Timing Measurement Level	V _{REF}	V _{CCF} = 2.7 V to 3.1 V	1.3	V	
Input Transition Time	t _r	Between V _{IL} and V _{IH}	5	ns	

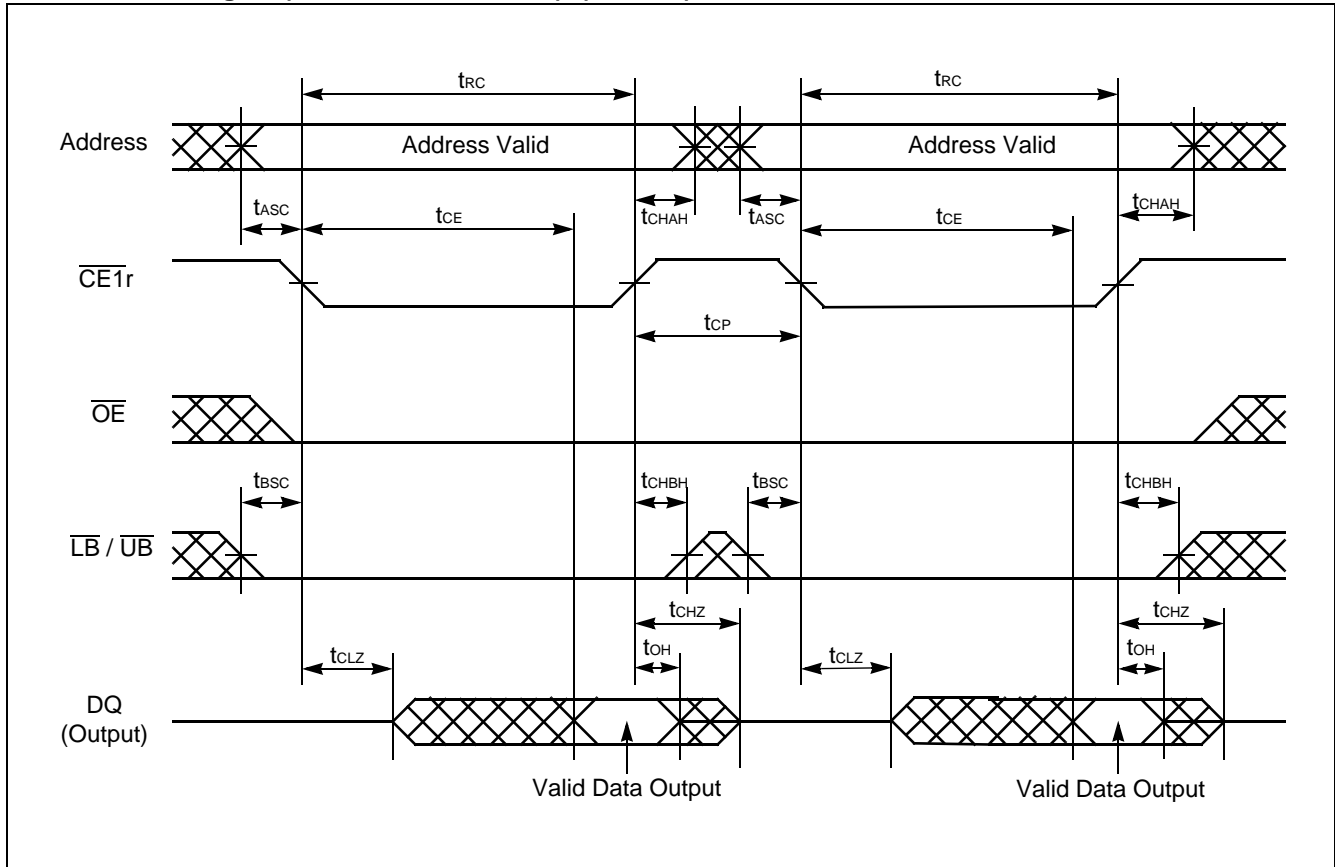
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• READ Timing #1 ($\overline{\text{OE}}$ Control Access) (FCRAM)



Note : $\overline{\text{CE2r}}$, $\overline{\text{PE}}$ and $\overline{\text{WE}}$ must be High for entire read cycle.
 Either or both $\overline{\text{LB}}$ and $\overline{\text{UB}}$ must be Low when both $\overline{\text{CE1r}}$ and $\overline{\text{OE}}$ are Low.

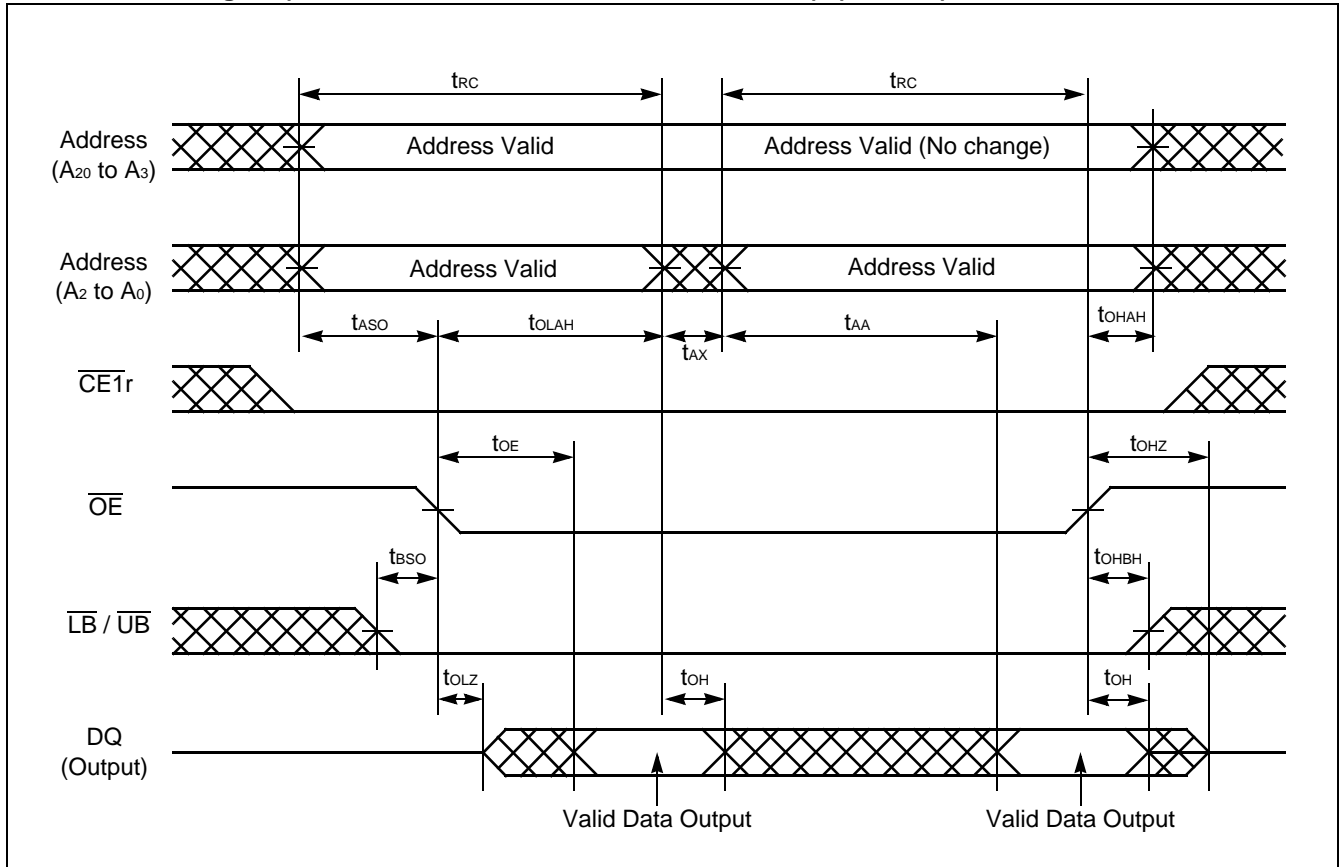
• READ Timing #2 ($\overline{CE1r}$ Control Access) (FCRAM)



Note : $\overline{CE2r}$, \overline{PE} and \overline{WE} must be High for entire read cycle.
 Either or both \overline{LB} and \overline{UB} must be Low when both $\overline{CE1r}$ and \overline{OE} are Low.

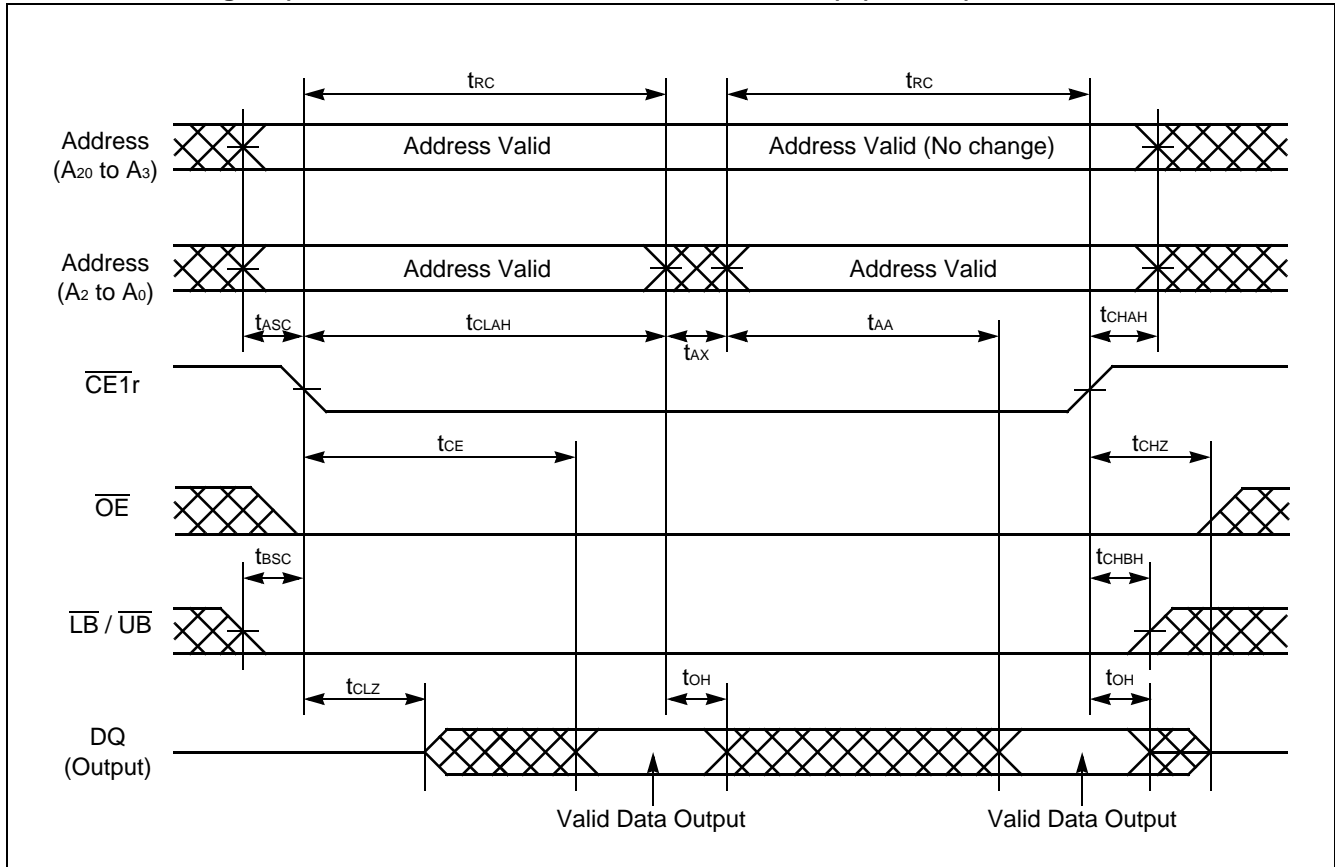
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• READ Timing #3 (Address Access after \overline{OE} Control Access) (FCRAM)



Note : $\overline{CE2r}$, \overline{PE} and \overline{WE} must be High for entire read cycle.
 Either or both \overline{LB} and \overline{UB} must be Low when both $\overline{CE1r}$ and \overline{OE} are Low.

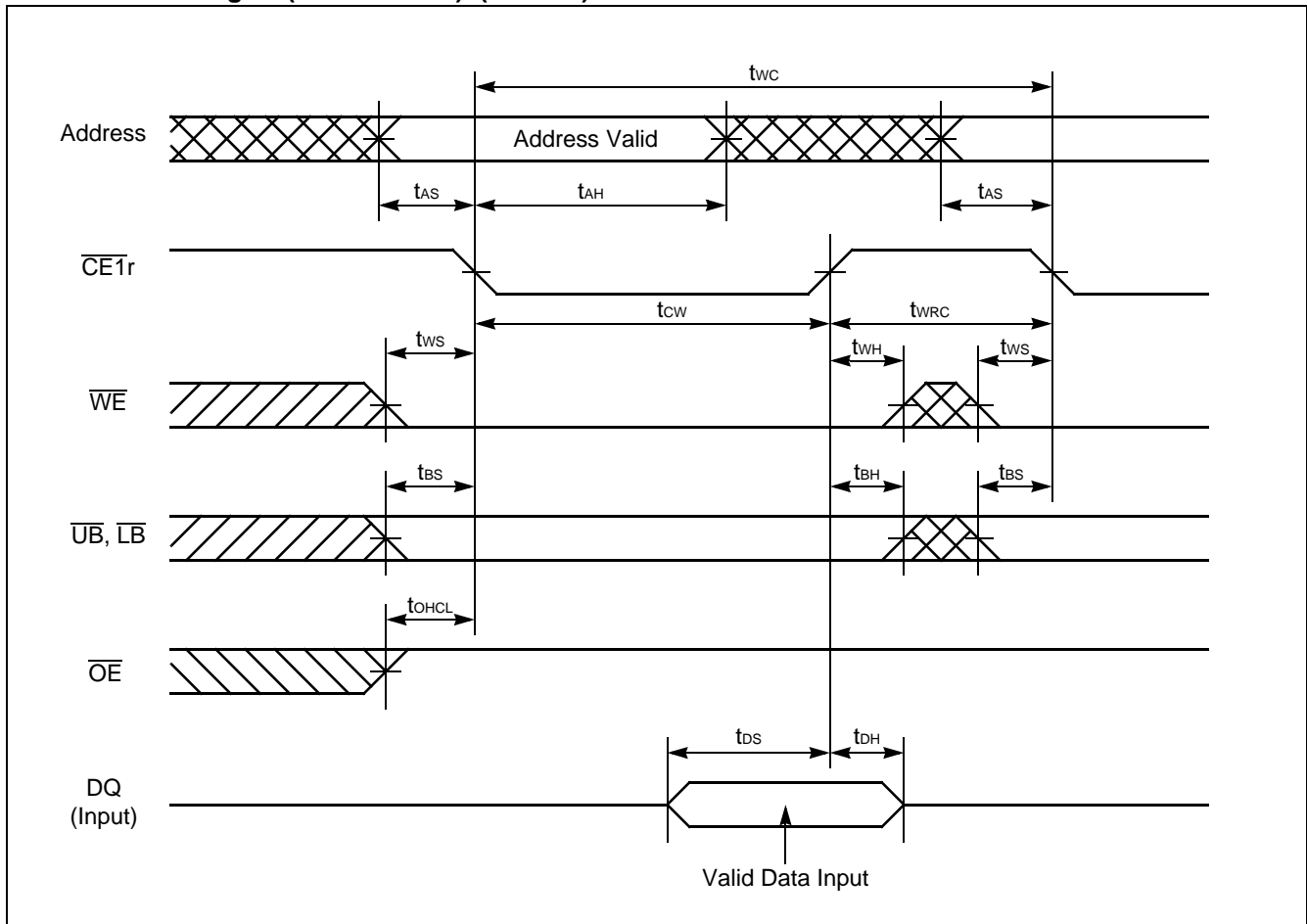
• READ Timing #4 (Address Access after $\overline{\text{CE1r}}$ Control Access) (FCRAM)



Note : $\overline{\text{CE2r}}$, $\overline{\text{PE}}$ and $\overline{\text{WE}}$ must be High for entire read cycle.
 Either or both $\overline{\text{LB}}$ and $\overline{\text{UB}}$ must be Low when both $\overline{\text{CE1r}}$ and $\overline{\text{OE}}$ are Low.

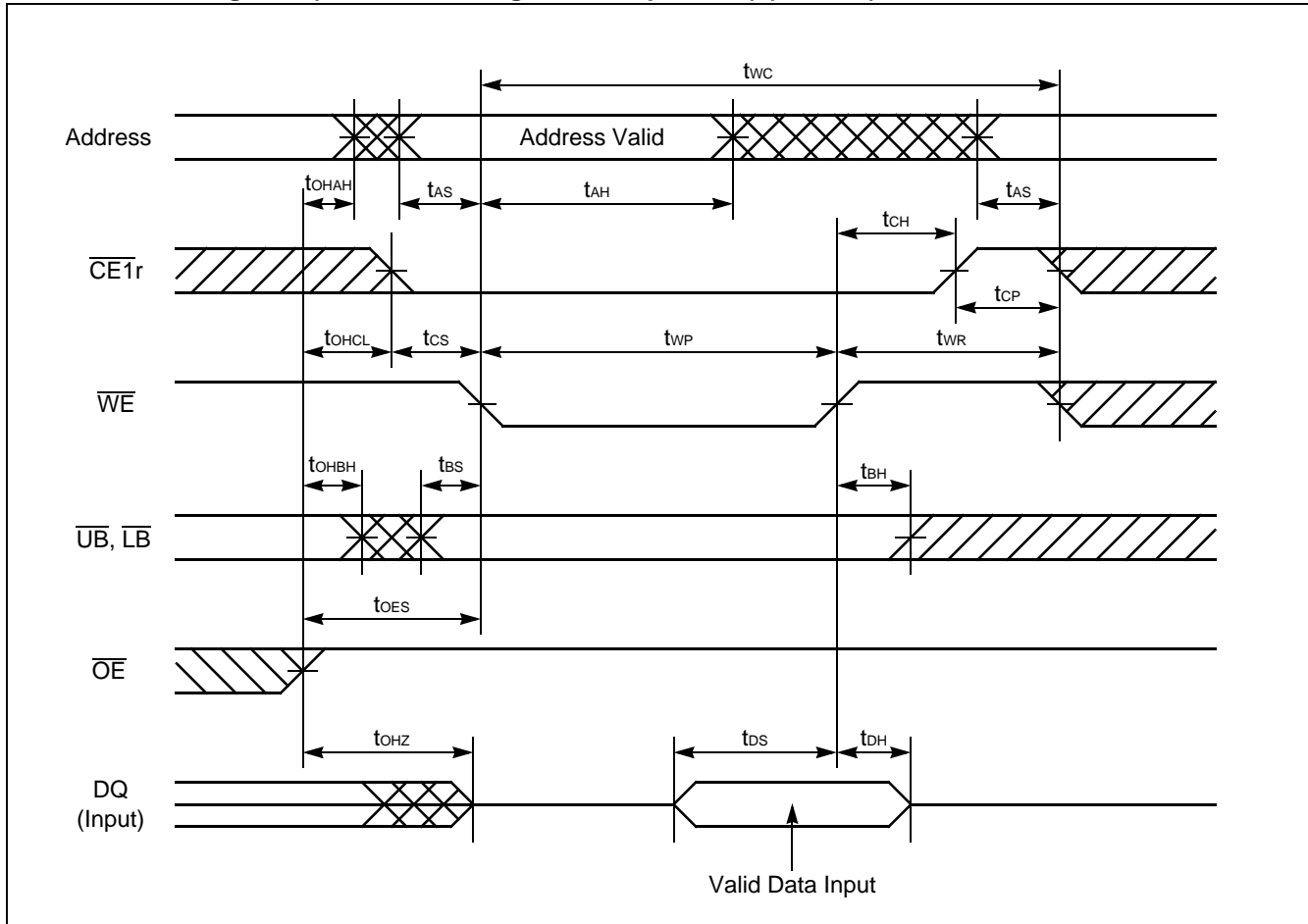
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• WRITE Timing #1 ($\overline{\text{CE1r}}$ Control) (FCRAM)



Note : $\overline{\text{CE2r}}$ and $\overline{\text{PE}}$ must be High for write cycle.

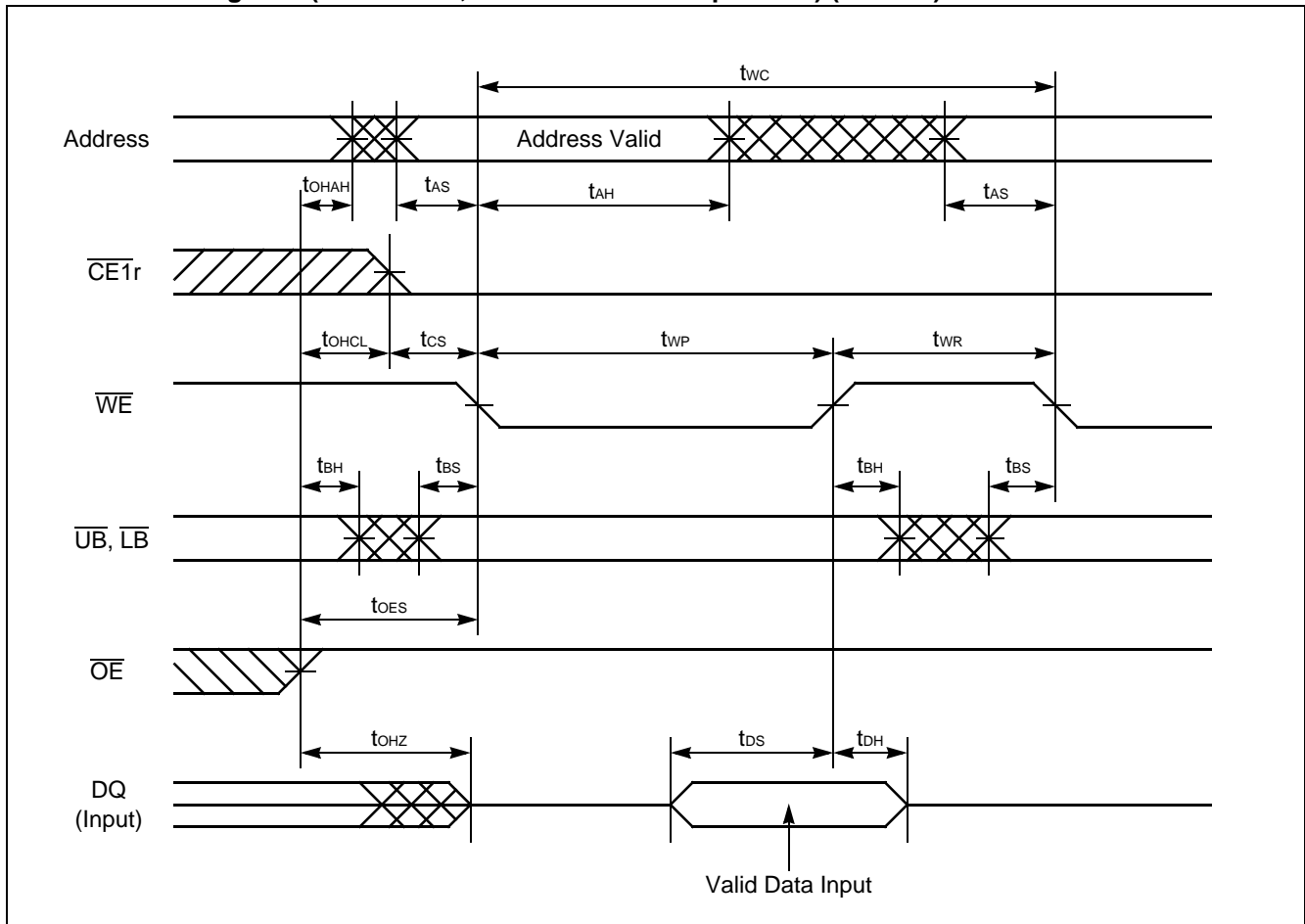
• WRITE Timing #2-1 (\overline{WE} Control, Single Write Operation) (FCRAM)



Note : $\overline{CE2r}$ and \overline{PE} must be High for write cycle.

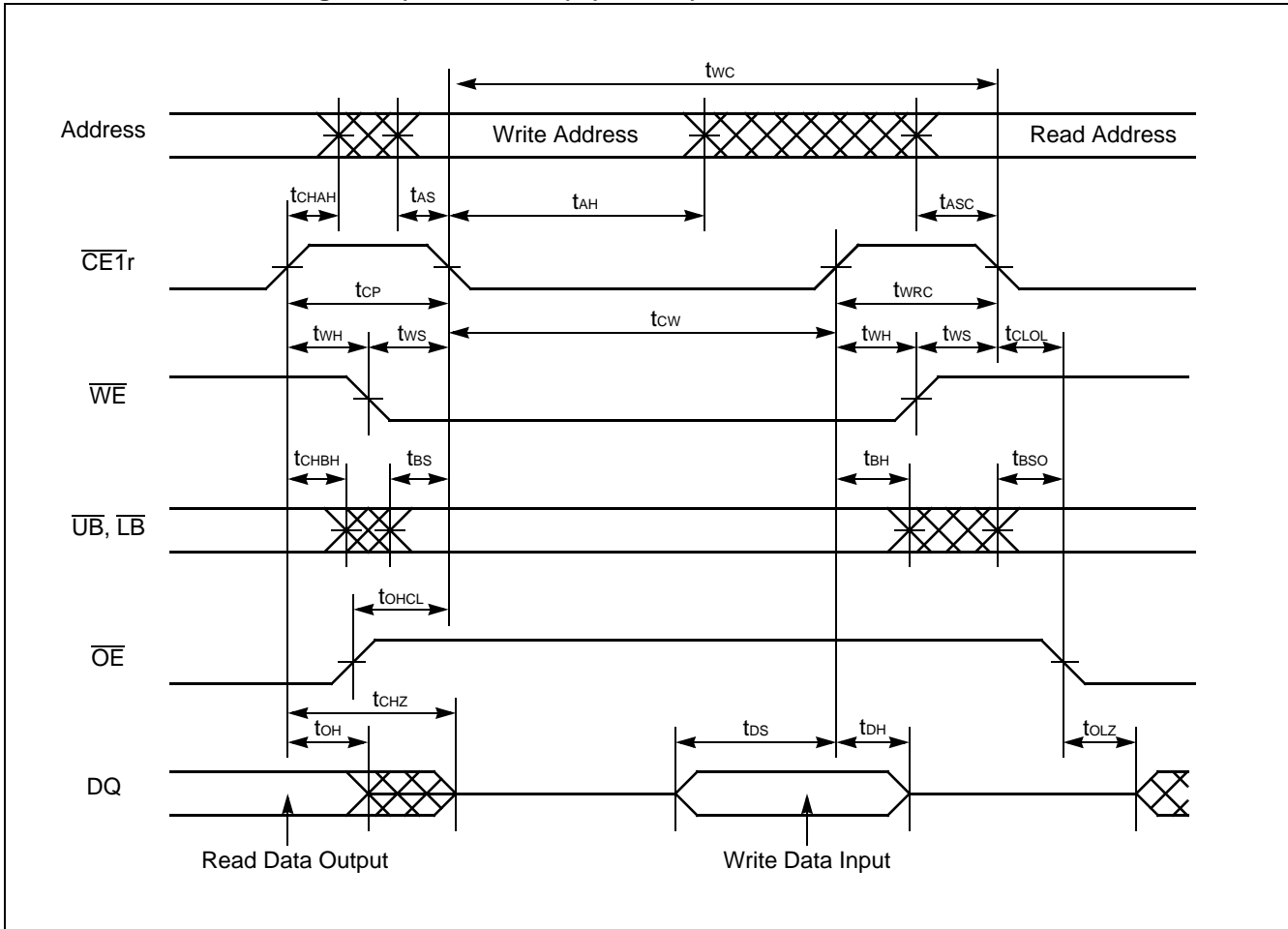
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• WRITE Timing #2-2 (\overline{WE} Control, Continuous Write Operation) (FCRAM)



Note : $\overline{CE2r}$ and \overline{PE} must be High for write cycle.

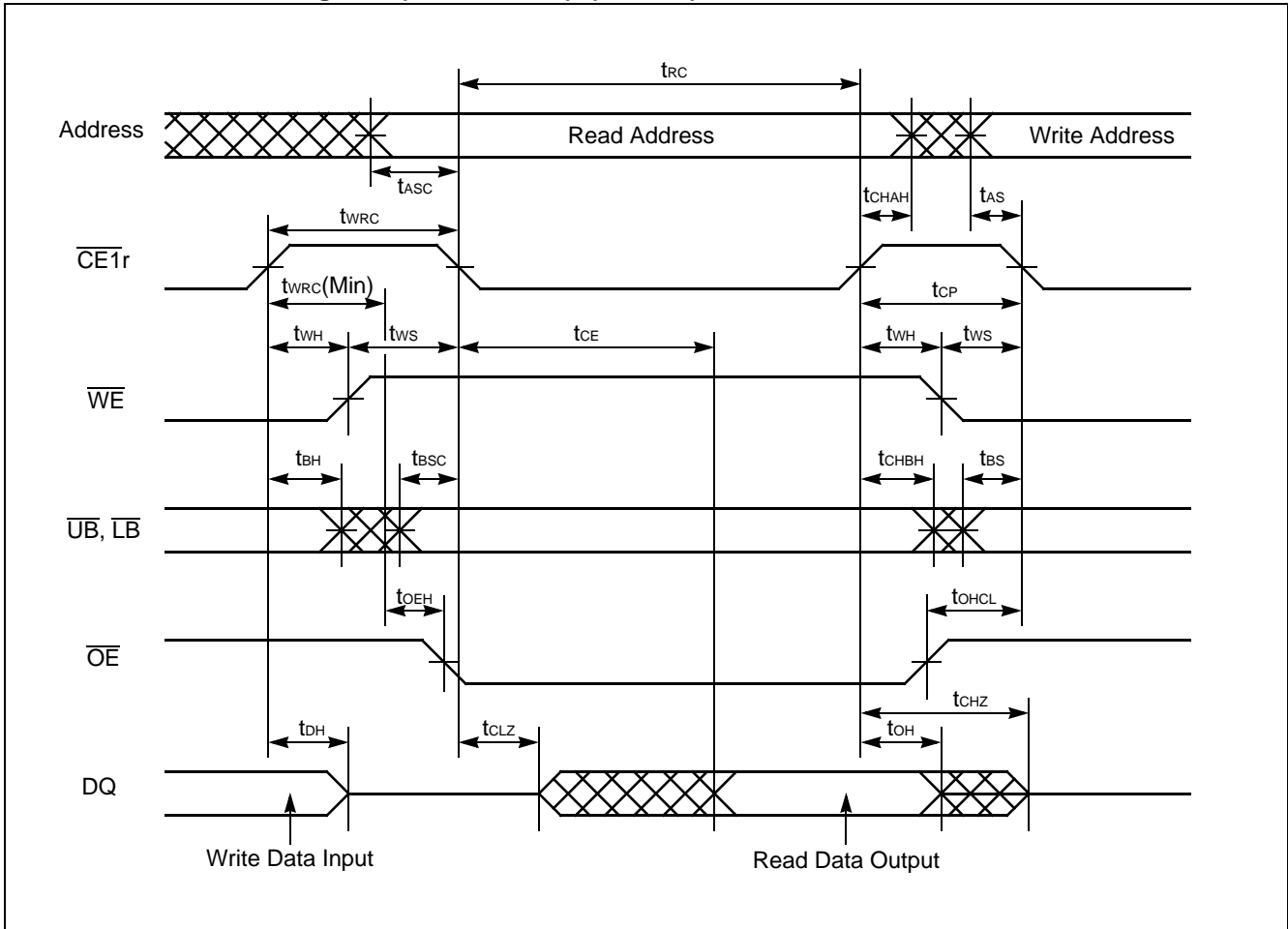
• READ / WRITE Timing #1-1 ($\overline{\text{CE1r}}$ Control) (FCRAM)



Note : Write address is valid from either $\overline{\text{CE1r}}$ or $\overline{\text{WE}}$ of last falling edge.

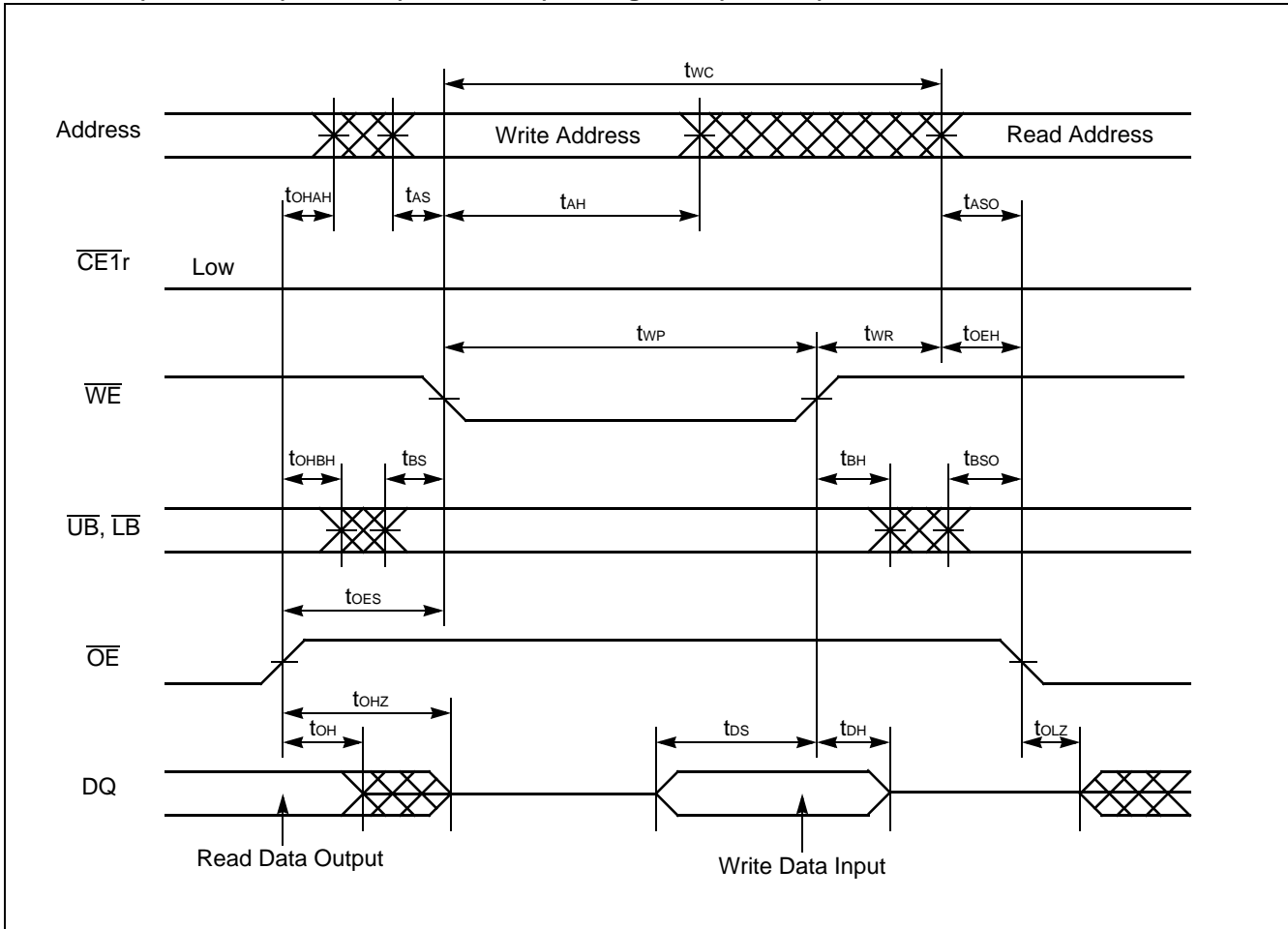
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• READ / WRITE Timing #1-2 ($\overline{CE1r}$ Control) (FCRAM)



Note : The t_{OE} is specified from the time satisfied both t_{WRC} and $t_{WR}(\text{Min})$.

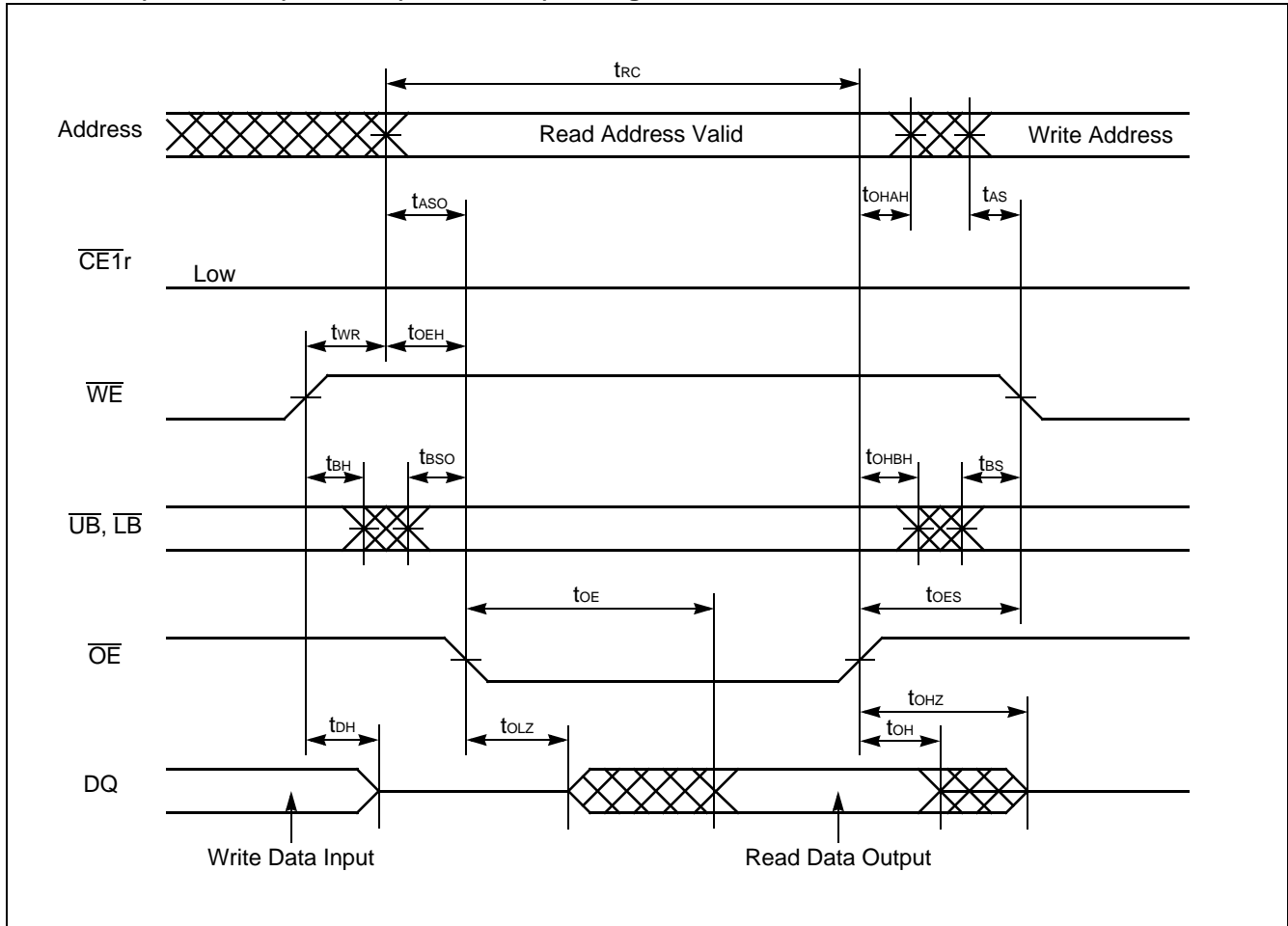
• READ(\overline{OE} Control) / WRITE(\overline{WE} Control) Timing #2-1 (FCRAM)



Note : $\overline{CE1r}$ can be tied to Low for \overline{WE} and \overline{OE} controlled operation.
 When $\overline{CE1r}$ is tied to Low, output is exclusively controlled by \overline{OE} .

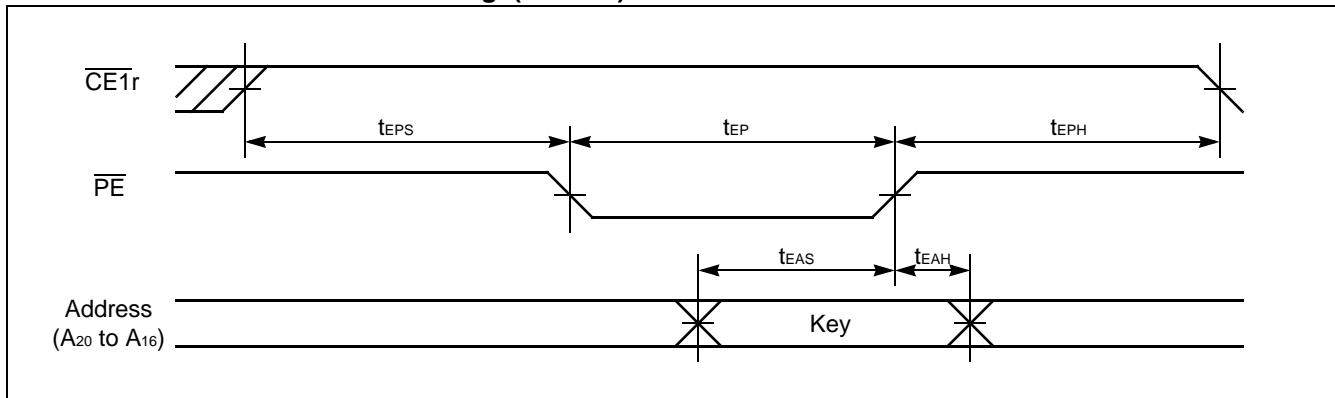
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• READ(\overline{OE} Control) / WRITE(\overline{WE} Control) Timing #2-2



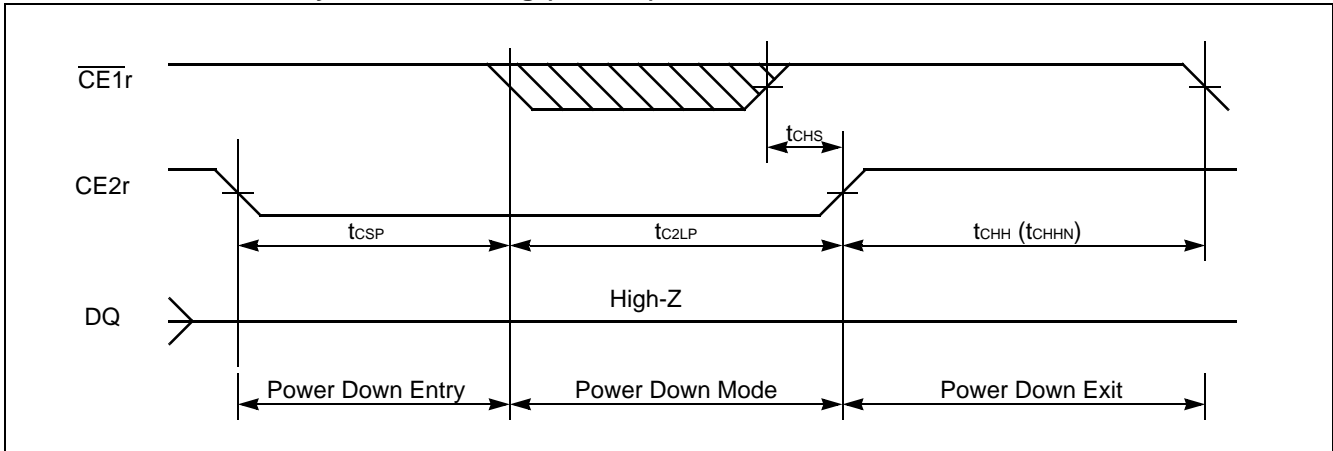
Note : $\overline{CE1r}$ can be tied to Low for \overline{WE} and \overline{OE} controlled operation.
When $\overline{CE1r}$ is tied to Low, output is exclusively controlled by \overline{OE} .

• POWER DOWN PROGRAM Timing (FCRAM)



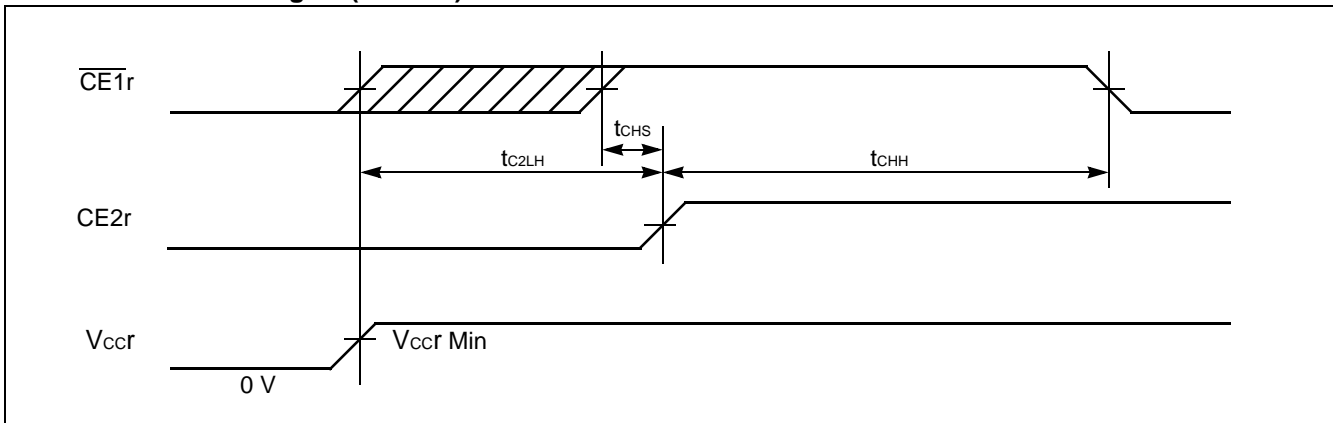
Note : $\overline{CE2r}$ must be High for Power Down Programming.
Any other inputs not specified above can be either High or Low.

• POWER DOWN Entry and Exit Timing (FCRAM)



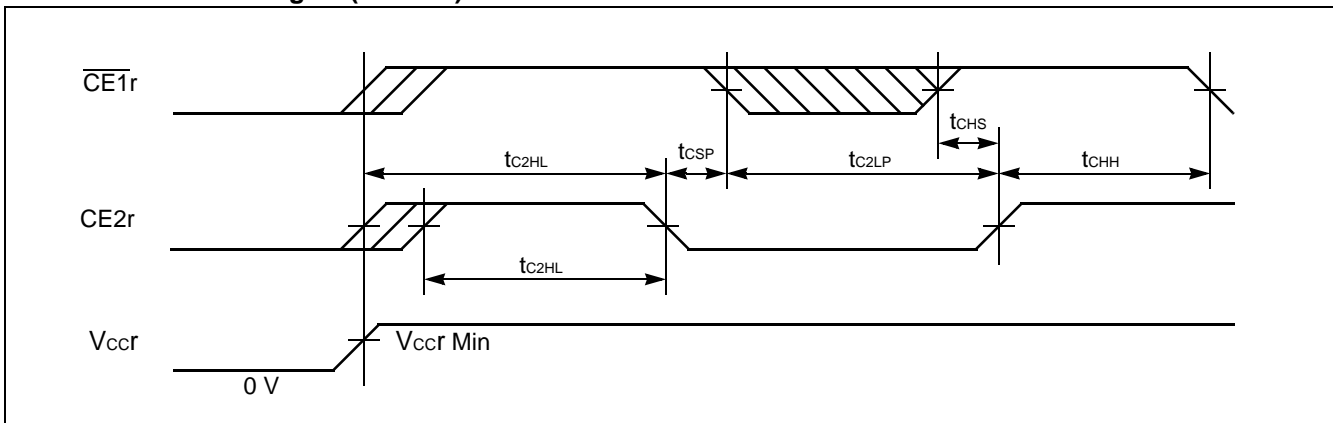
Note : This Power Down mode can be also used for Power-up #2 below except that t_{CHHN} can not be used at Power-up timing.

• POWER-UP Timing #1 (FCRAM)



Note : The t_{C2LH} specifies after V_{ccr} reaches specified minimum level.

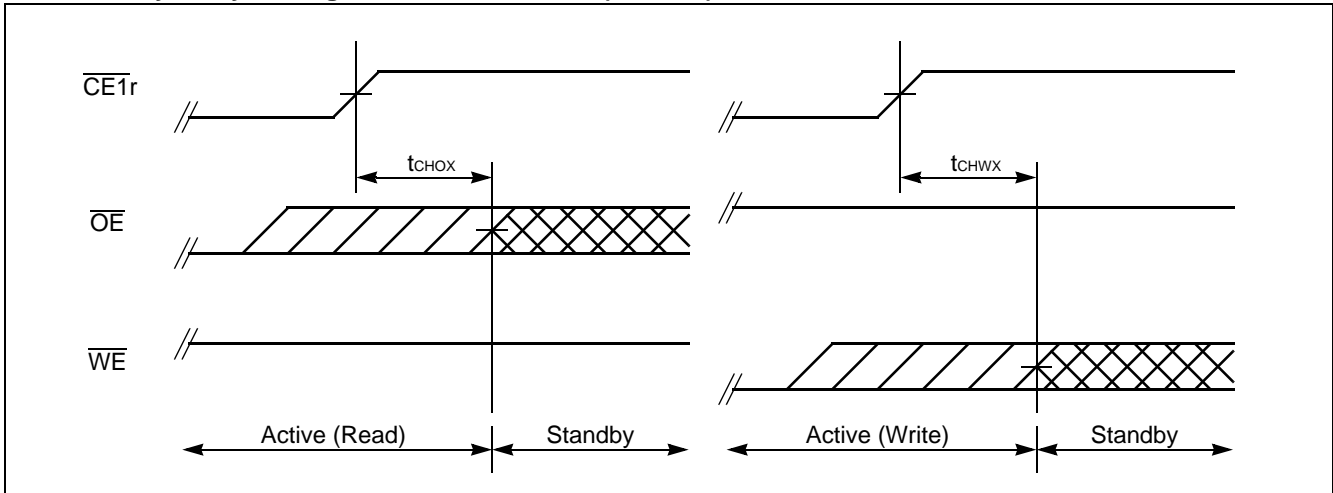
• POWER-UP Timing #2 (FCRAM)



Note : The t_{C2HL} specifies from $CE2r$ Low to High transition after V_{ccr} reaches specified minimum level. $\overline{CE1r}$ must be brought to High prior to or together with $CE2r$ Low to High transition.

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• Standby Entry Timing after Read or Write (FCRAM)



Note : Both t_{CHOX} and t_{CHWX} define the earliest entry timing for Standby mode. If either of timing is not satisfied, it takes t_{RC} (Min) period from either last address transition of A_1 and A_0 , or $\overline{CE1r}$ Low to High transition.

■ ERASE AND PROGRAMMING PERFORMANCE (Flash)

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector Erase Time	—	0.5	2	s	Excludes programming time prior to erasure
Word Programming Time	—	6	100	μ s	Excludes system-level overhead
Chip Programming Time	—	25.2	95	s	Excludes system-level overhead
Erase/Program Cycle	100,000	—	—	cycle	

Note : Typical Erase conditions $T_A = +25^\circ\text{C}$, V_{CCf_1} & $V_{CCf_2} = 2.9\text{ V}$

Typical Program conditions $T_A = +25^\circ\text{C}$, V_{CCf_1} & $V_{CCf_2} = 2.9\text{ V}$

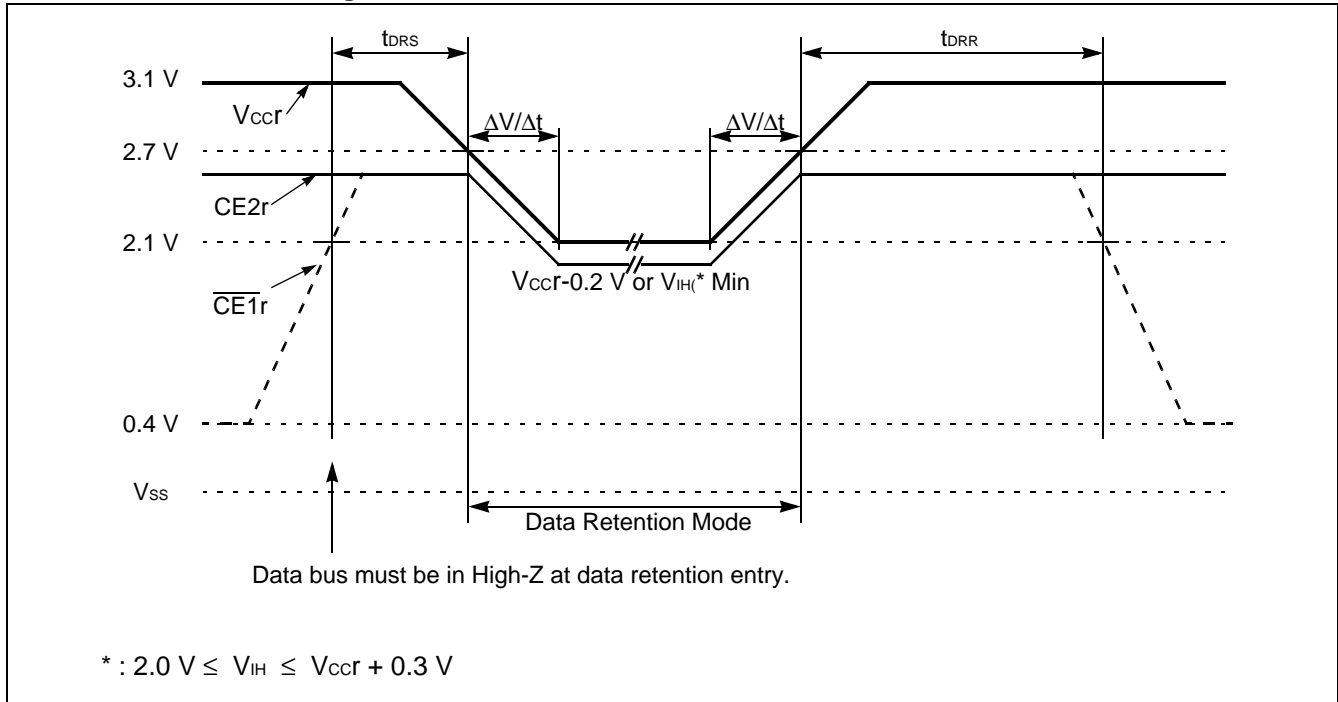
Data= Checker

3. DATA RETENTION Low V_{CCr} Characteristics (FCRAM)

Parameter	Symbol	Test Conditions	Value		Unit
			Min	Max	
V _{CCr} Data Retention Supply Voltage	V _{DR}	$\overline{CE1r} = CE2r \geq V_{CCr} - 0.2 \text{ V}$ or $\overline{CE1r} = CE2r = V_{IH}$	2.1	3.1	V
V _{CCr} Data Retention Supply Current	I _{DR}	$2.1 \text{ V} \leq V_{CCr} \leq 2.7 \text{ V}$, $V_{IN} = V_{IH}^*$ or V_{IL} , $\overline{CE1r} = CE2r = V_{IH}^*$, I _{OUT} = 0 mA	—	1.5	mA
	I _{DR1}	$2.1 \text{ V} \leq V_{CCr} \leq 2.7 \text{ V}$, $V_{IN} \leq 0.2 \text{ V}$ or $V_{IN} \geq V_{CCr} - 0.2 \text{ V}$, $\overline{CE1r} = CE2r \geq V_{CCr} - 0.2 \text{ V}$, I _{OUT} = 0 mA	—	100	μA
Data Retention Setup Time	t _{DRS}	$2.7 \text{ V} \leq V_{CCr} \leq 3.1 \text{ V}$ at data retention entry	0	—	ns
Data Retention Recovery Time	t _{DRR}	$2.7 \text{ V} \leq V_{CCr} \leq 3.1 \text{ V}$ after data retention	200	—	ns
V _{CCr} Voltage Transition Time	ΔV/Δt	—	0.2	—	V/μs

* : $2.0 \text{ V} \leq V_{IH} \leq V_{CCr} + 0.3 \text{ V}$

• Data Retention Timing



■ PIN CAPACITANCE

Parameter	Symbol	Test Setup	Value		Unit
			Typ	Max	
Input Capacitance	C_{IN}	$V_{IN} = 0$	11	14	pF
Output Capacitance	C_{OUT}	$V_{OUT} = 0$	12	16	pF
Control Pin Capacitance	C_{IN2}	$V_{IN} = 0$	14	16	pF
\overline{WP}/ACC Pin Capacitance	C_{IN3}	$V_{IN} = 0$	21.5	26	pF

Note : Test conditions $T_A = +25^\circ\text{C}$, $f = 1.0 \text{ MHz}$

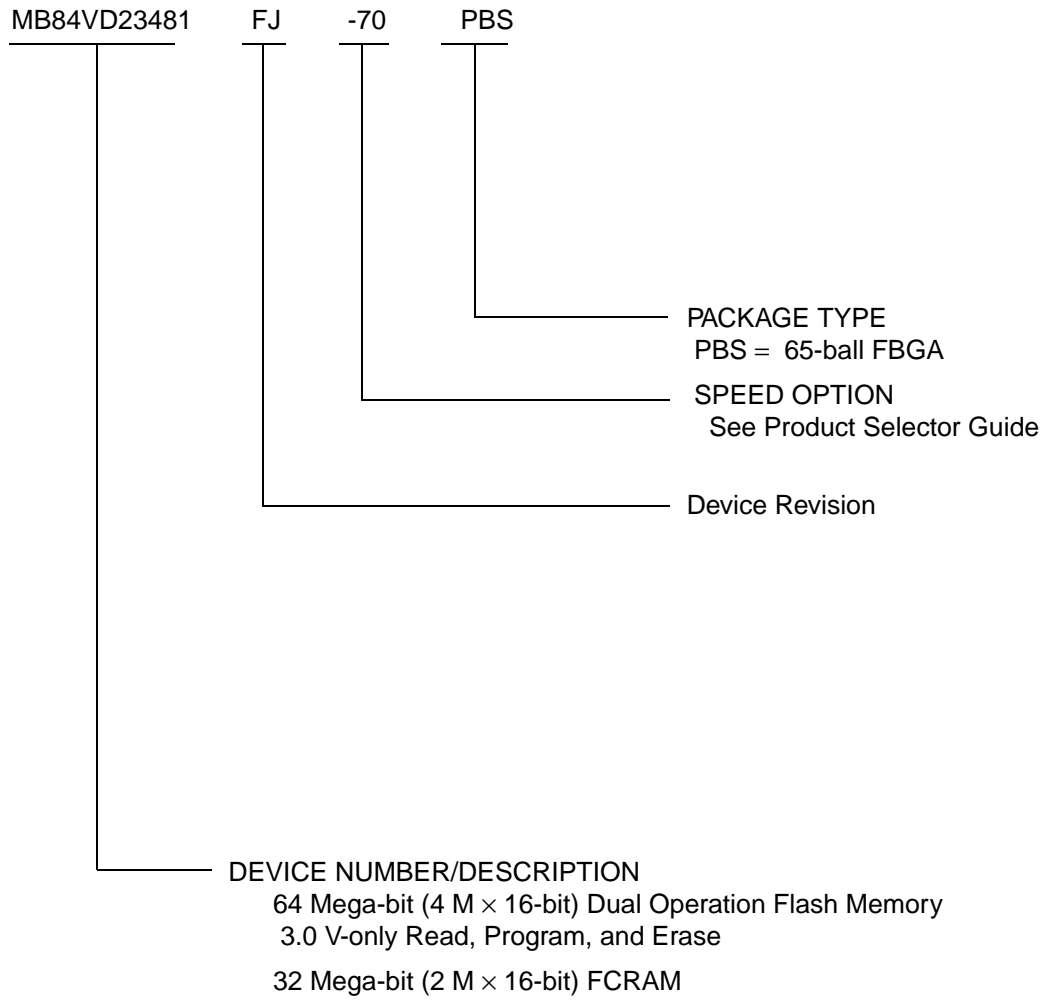
■ HANDLING OF PACKAGE

Please handle this package carefully since the sides of package create acute angles.

■ CAUTION

- The high voltage (V_{ID}) cannot apply to address pins and control pins except \overline{RESET} . Exception is when autoselect and sector group protect function are used, then the high voltage (V_{ID}) can be applied to \overline{RESET} .
- Without the high voltage (V_{ID}), sector group protection can be achieved by using "Extended Sector Group Protection" command.

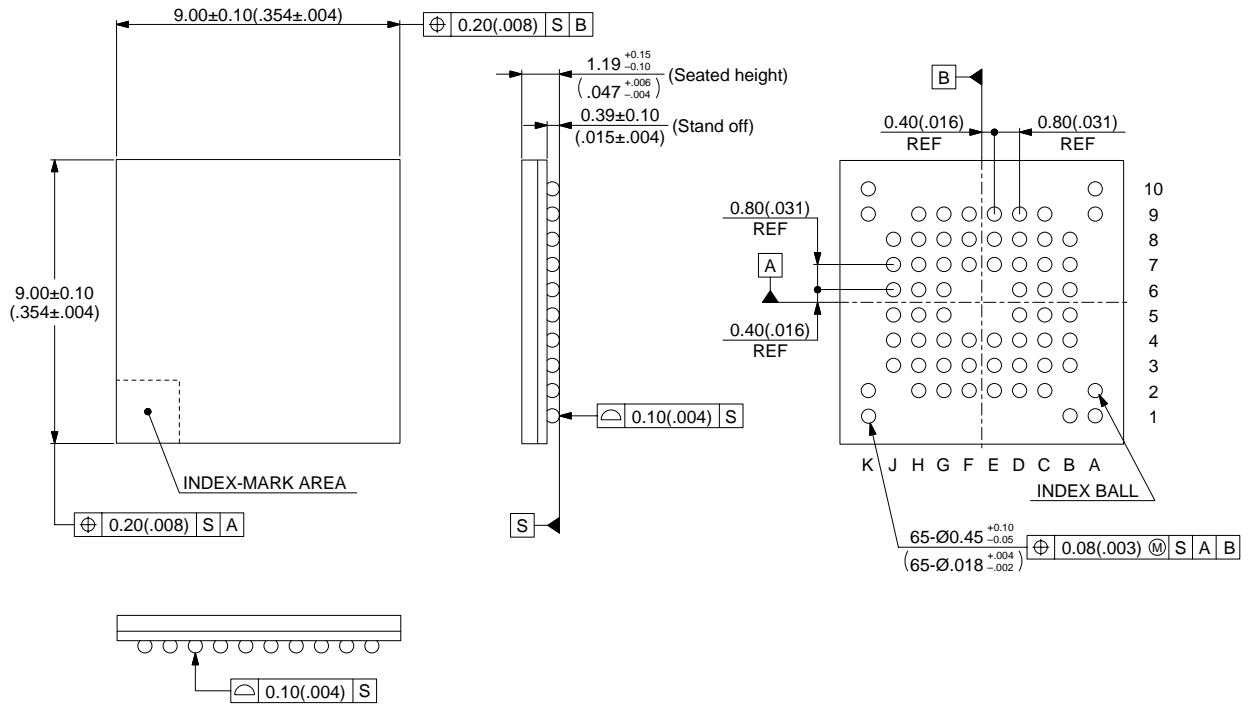
■ ORDERING INFORMATION



MB84VD23481FJ-70

■ PACKAGE DIMENSION

65-ball plastic FBGA
(BGA-65P-M01)



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Dimensions in mm (inches).

Note: The values in parentheses are reference values.

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