September 1993
Edition 1.0

FUJITSU

DATA SHEET

MB85323A-60/-70/-80

CMOS 1 M x 36 Fast Page Mode DRAM Module

CMOS 1,024,576 x 36 Bit Fast Page Mode DRAM Module

The Fujitsu MB85323A is a fully decoded, CMOS dynamic random access memory (DRAM) module consisting of eight MB814400A devices and four MB81C1000A devices. The MB85323A is optimized for those applications requiring high speed, high performance and large memory storage. The operation and electrical characteristics of the MB85323A are the same as the MB814400A which features fast page mode operation. For ease of memory expansion, the MB85323A is offered in a 72-pad Single In-line Memory Module package (SIMM).

PRELIMINARY

See page 3-60
MSS-72P-P37

See page 3-61
MSS-72P-P57

PRODUCT LINE & FEATURES

Parameter	MB85323A-60	MB85323A-70	MB85323A-80
$\overline{RAS}$ Access Time	60ns max.	70ns max.	80ns max.
Random Cycle Time	110ns min.	125ns min.	140ns min.
Address Access Time	30ns max.	35ns max.	40ns max.
$\overline{CAS}$ Access Time	15ns max.	20ns max.	20ns max.
Fast Page Mode Cycle Time	40ns min.	45ns min.	45ns min.
Power Dissipation • Operating mode	6468mW max.	5896mW max.	5324mW max.
• Standby mode	132mW max. (TTL level) / 66mW max. (CMOS level)		

- Organization :
  1,024,576 words x 36 bits
- Memory :
  MB814400A, 8 pcs
  MB81C1000A, 4 pcs
- Decoupling Capacitor :
  0.22 µF, 12 pcs
- Package and Ordering Information:
  72-pad SIMM, order as
  MB85323A-xxPJPBK
  (PJPBK = Gold Pad) or
  MB85323A-xxPJPB
  (PJPB = Solder Pad)

ABSOLUTE MAXIMUM RATINGS (See NOTE.)

Parameter	Symbol	Value	Unit
Supply Voltage	VCC	−1.0 to +7.0	V
Input Voltage	VIN	−1.0 to +7.0	V
Output Voltage	VOUT	−1.0 to +7.0	V
Short Circuit Output Current	IOUT	50	mA
Power Dissipation	PD	12.0	W
Storage Temperature	TSTG	−55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DQ0	2	1	VSS
DQ1	4	3	DQ18
DQ2	6	5	DQ19
DQ3	8	7	DQ20
VCC	10	9	DQ21
A0	12	11	NC
A2	14	13	A1
A4	16	15	A3
A6	18	17	A5
DQ4	20	19	NC
DQ5	22	21	DQ22
DQ6	24	23	DQ23
DQ7	26	25	DQ24
A7	28	27	DQ25
VCC	30	29	NC
A9	32	31	A8
$\overline{RAS2}$	34	33	NC
DQ8	36	35	DQ26
DQ35	38	37	DQ17
$\overline{CAS0}$	40	39	VSS
$\overline{CAS3}$	42	41	$\overline{CAS2}$
$\overline{RAS0}$	44	43	$\overline{CAS1}$
NC	46	45	NC
NC	48	47	$\overline{WE}$
DQ27	50	49	DQ9
DQ28	52	51	DQ10
DQ29	54	53	DQ11
DQ30	56	55	DQ12
DQ31	58	57	DQ13
DQ32	60	59	VCC
DQ33	62	61	DQ14
DQ34	64	63	DQ15
NC	66	65	DQ16
PD2	68	67	PD1
PD4	70	69	PD3
VSS	72	71	NC

Pin #	Symbol	-60	-70	-80
67	PD1	Vss	Vss	Vss
68	PD2	Vss	Vss	Vss
69	PD3	NC	Vss	NC
70	PD4	NC	NC	Vss

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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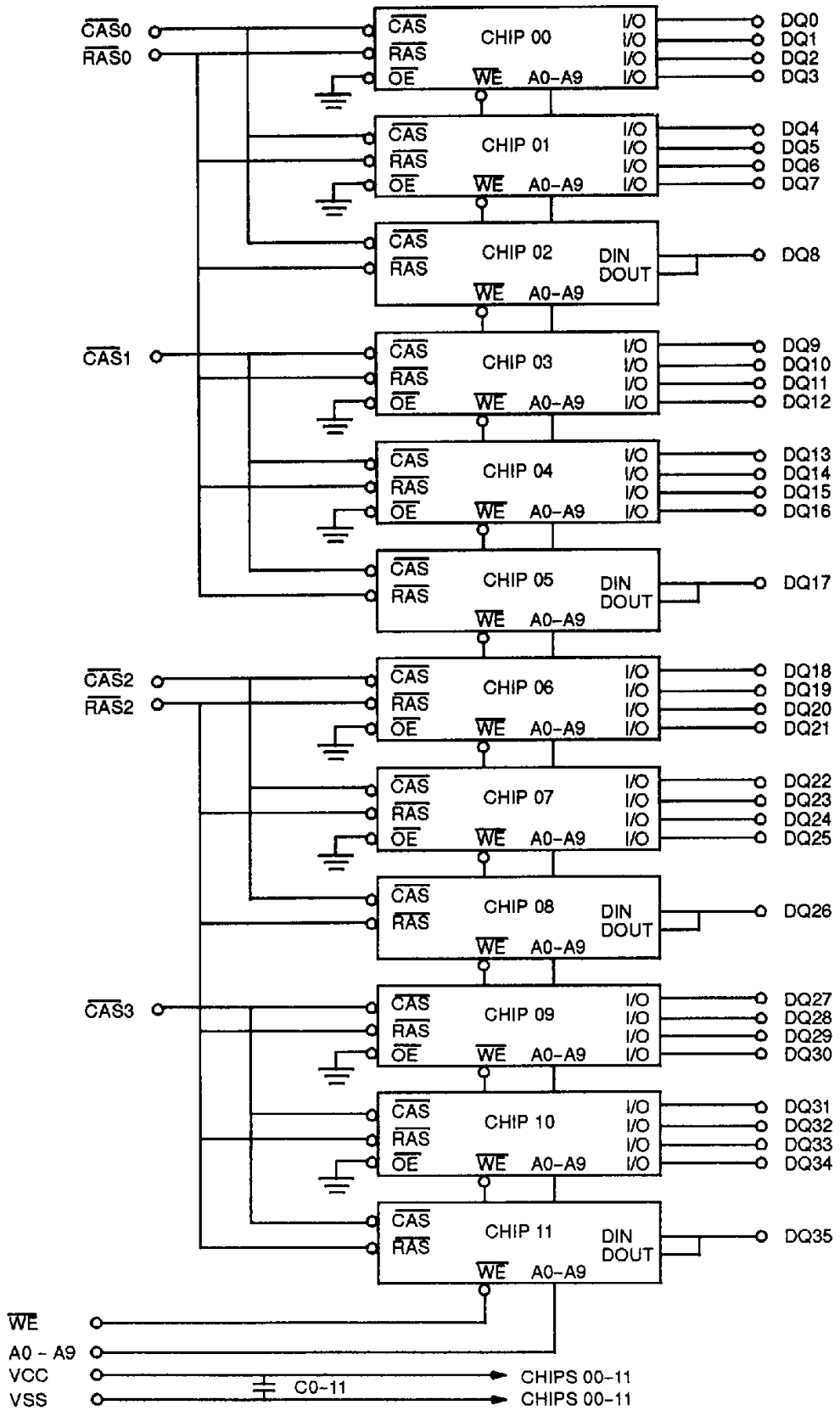
FUNCTIONAL BLOCK DIAGRAM



DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Notes	Symbol	Conditions	Values Min	Values Typ	Values Max	Unit
Output High Voltage		VOH	IOH = −5mA	2.4	—	—	V
Output Low Voltage		VOL	IOL = 4.2mA	—	—	0.4	V
Input Leakage Current	$\overline{RAS}$	II(L)	0V ≤ VIN ≤ 5.5V; 4.5V ≤ VCC ≤ 5.5V; VSS=0V; all other pins not under test = 0V	−40	—	40	µA
	$\overline{CAS}$			−30	—	30	
	ADD, $\overline{WE}$			−80	—	80	
Output Leakage Current		IO(L)	0V ≤ VOUT ≤ 5.5V; Data out disabled	−20	—	20	µA
Operating Current (Average power supply current) [1]	MB85323A-60	ICC1	$\overline{RAS}$ & $\overline{CAS}$ cycling; tRC = min.	—	—	1176	mA
	MB85323A-70					1072	
	MB85323A-80					968	
Standby Current (Power supply current)	TTL Level	ICC2	$\overline{RAS}$ = $\overline{CAS}$ = VIH	—	—	24	mA
	CMOS Level		$\overline{RAS}$ = $\overline{CAS}$ ≥ VCC-0.2V			12	
Refresh Current #1 (Average power supply current) [1]	MB85323A-60	ICC3	$\overline{CAS}$ = VIH; $\overline{RAS}$ = cycling; tRC = min.	—	—	1176	mA
	MB85323A-70					1072	
	MB85323A-80					968	
Fast Page Mode Current [1]	MB85323A-60	ICC4	$\overline{RAS}$ = VIL; $\overline{CAS}$ = cycling; tPC = min.	—	—	684	mA
	MB85323A-70					624	
	MB85323A-80					584	
Refresh Current #2 (Average power supply current) [1]	MB85323A-60	ICC5	$\overline{RAS}$ = cycling; $\overline{CAS}$-before-$\overline{RAS}$ tRC = min.	—	—	1016	mA
	MB85323A-70					912	
	MB85323A-80					808	

Note: 1. ICC depends on the output load conditions and cycle rate; The specified values are obtained with the output open.
ICC depends on the number of address change as $\overline{RAS}$ = VIL and $\overline{CAS}$ = VIH, VIL > −0.5V.
ICC1, ICC3 and ICC5 are specified at one time of address change during $\overline{RAS}$ = VIL and $\overline{CAS}$ = VIH.
ICC4 is specified at one time of address change during one Page cycle.

CAPACITANCE (T_A = 25°C, f = 1MHz)

Parameter	Symbol	Value Typ	Value Max	Unit
Input Capacitance, A0 to A9	CIN1	—	60	pF
Input Capacitance, $\overline{RAS}$0 and $\overline{RAS}$2	CIN2	—	34	pF
Input Capacitance, $\overline{CAS}$0 to $\overline{CAS}$3	CIN3	—	19	pF
Input Capacitance, $\overline{WE}$	CIN4	—	51	pF
I/O Capacitance, (DQ0-7, DQ9-16, DQ18-25, DQ27-34)	CDQ1	—	10	pF
I/O Capacitance, (DQ8, DQ17, DQ26, DQ35)	CDQ2	—	13	pF

AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes 1, 2, 3

No.	Parameter	Notes	Symbol	MB85323A-60		MB85323A-70		MB85323A-80		Unit
				Min	Max	Min	Max	Min	Max	
1	Time Between Refresh	17	tREF	—	16.4	—	16.4	—	16.4	ms
2	Random Read/Write Cycle Time		tRC	110	—	125	—	140	—	ns
3	Access Time from $\overline{RAS}$	4, 7	tRAC	—	60	—	70	—	80	ns
4	Access Time from $\overline{CAS}$	5, 7	tCAC	—	15	—	20	—	20	ns
5	Column Address Access Time	6, 7	tAA	—	30	—	35	—	40	ns
6	Output Hold Time		tOH	0	—	0	—	0	—	ns
7	Output Buffer Turn on Delay Time		tON	0	—	0	—	0	—	ns
8	Output Buffer Turn off Delay Time	8	tOFF	—	15	—	15	—	20	ns
9	Transition Time		tT	2	50	2	50	2	50	ns
10	$\overline{RAS}$ Precharge Time		tRP	40	—	45	—	50	—	ns
11	$\overline{RAS}$ Pulse Width		tRAS	60	100000	70	100000	80	100000	ns
12	$\overline{RAS}$ Hold Time		tRSH	15	—	20	—	20	—	ns
13	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		tCRP	5	—	5	—	5	—	ns
14	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	9, 10	tRCD	20	45	20	50	20	60	ns
15	$\overline{CAS}$ Pulse Width		tCAS	15	—	20	—	20	—	ns
16	$\overline{CAS}$ Hold Time		tCSH	60	—	70	—	80	—	ns
17	$\overline{CAS}$ Precharge Time (C-B-R Refresh)	15	tCPN	10	—	10	—	10	—	ns
18	Row Address Setup Time		tASR	0	—	0	—	0	—	ns
19	Row Address Hold Time		tRAH	10	—	10	—	10	—	ns
20	Column Address Setup Time		tASC	0	—	0	—	0	—	ns
21	Column Address Hold Time		tCAH	12	—	12	—	15	—	ns
22	$\overline{RAS}$ to Column Address Delay Time	11	tRAD	15	30	15	35	15	40	ns
23	Column Address to $\overline{RAS}$ Lead Time		tRAL	30	—	35	—	40	—	ns
24	Column Address to $\overline{CAS}$ Lead Time		tCAL	30	—	35	—	40	—	ns
25	Read Command Setup Time		tRCS	0	—	0	—	0	—	ns
26	Read Command Hold Time Referenced to $\overline{RAS}$	12	tRRH	0	—	0	—	0	—	ns
27	Read Command Hold Time Referenced to $\overline{CAS}$	12	tRCH	0	—	0	—	0	—	ns
28	Write Command Setup Time	13	tWCS	0	—	0	—	0	—	ns
29	Write Command Hold Time		tWCH	10	—	10	—	12	—	ns
30	$\overline{WE}$ Pulse Width		tWP	10	—	10	—	12	—	ns
31	Write Command to $\overline{RAS}$ Lead Time		tRWL	15	—	20	—	20	—	ns
32	Write Command to $\overline{CAS}$ Lead Time		tCWL	15	—	18	—	20	—	ns
33	DIN Setup Time		tDS	0	—	0	—	0	—	ns
34	DIN Hold Time		tDH	10	—	10	—	12	—	ns
35	$\overline{RAS}$ Precharge Time to $\overline{CAS}$ Active Time Low (Refresh Cycle)		tRPC	0	—	0	—	0	—	ns

AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.) Notes 1, 2, 3

No.	Parameter	Notes	Symbol	MB85323A-60		MB85323A-70		MB85323A-80		Unit
				Min	Max	Min	Max	Min	Max	
36	$\overline{CAS}$ Setup Time (C-B-R Refresh)		tCSR	0	—	0	—	0	—	ns
37	$\overline{CAS}$ Hold Time (C-B-R refresh)		tCHR	10	—	10	—	12	—	ns
38	$\overline{WE}$ Set Up Time from $\overline{RAS}$	16	tWSR	0	—	0	—	0	—	ns
39	$\overline{WE}$ Hold Time from $\overline{RAS}$	16	tWHR	10	—	10	—	10	—	ns
40	DIN to $\overline{CAS}$ Delay Time		tDZC	0	—	0	—	0	—	ns
41	Fast Page Mode $\overline{RAS}$ Pulse Width		tRASP	—	100000	—	100000	—	100000	ns
42	Fast Page Mode Read/Write Cycle Time		tPC	40	—	45	—	45	—	ns
43	Access Time from $\overline{CAS}$ Precharge	7, 14	tCPA	—	35	—	40	—	40	ns
44	Fast Page Mode $\overline{CAS}$ Precharge Time		tCP	10	—	10	—	10	—	ns
45	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge		tRHCP	35	—	40	—	40	—	ns

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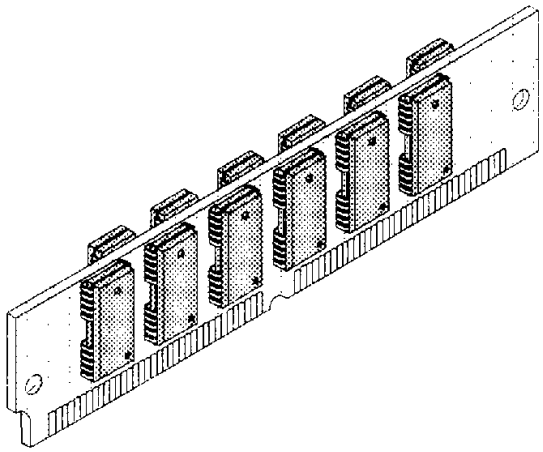
Notes:

1. An initial pause ($\overline{RAS}$=$\overline{CAS}$=VIH) of 200µs is required after power-up followed by any eight $\overline{RAS}$-only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles are required instead of eight $\overline{RAS}$ cycles.
2. AC characteristics assume tT = 5ns.
3. VIH (min) and VIL (max) are reference levels for measureing the timing of input signals. Also, transition times are measured between VIH (min) and VIL (max).
4. Assumes that tRCD ≤ tRCD (max), tRAD≤ tRAD (max). If tRCD is greater than the maximum recommended value shown in this table, tRAC will be increased by the amount that tRCD exceeds the value shown.
5. If tRCD≥ tRCD (max), tRAD≥ tRAD (max), and tASC≥ tAA- tCAC - tT, access time is tCAC.
6. If tRAD≥ tRAD (max) and tASC≤ tAA- tCAC - tT, access time is tAA.
7. Measured with a load equivalent to two TTL loads and 100 pF.
8. tOFF is specified that output buffer change to high impedance state.
9. Operation within the tRCD (max) limit ensures that tRAC (max) can be met. tRCD (max) is specified as a reference point only; if tRCD is greater than the specified tRCD (max) limit, access time is controlled exclusively by tCAC or tAA.
10. tRCD (min) = tRAH (min)+ 2tT + tASC (min).
11. Operation within the tRAD (max) limit ensures that tRAC (max) can be met. tRAD (max) is specified as a reference point only; if tRAD is greater than the specified tRAD (max) limit, access time is controlled exclusively by tCAC or tAA.
12. Either tRRH or tRCH must be satisfied for a read cycle.
13. If tWCS > tWCS (min), the data output pin will remain in the high-Z state through the entire cycle.
14. tCPA is access time from the selection of a new column address (caused by changing $\overline{CAS}$ from "L" to "H"). Therefore, if tCP becomes long, tCPA also becomes longer than tCPA (max).
15. Assumes that $\overline{CAS}$-before-$\overline{RAS}$ refresh.
16. Assumes that test mode function for non-parity bit.
17. tREF is for distributed refresh (1024 refresh cycles / 16.4 ms). For burst refresh, tREF = 8.2 ms (1024 refresh cycles / 8.2 ms).

*Source: See MB814400A Data Sheet for details on the electricals.

PACKAGE DIMENSIONS

(Suffix: PJPBK)



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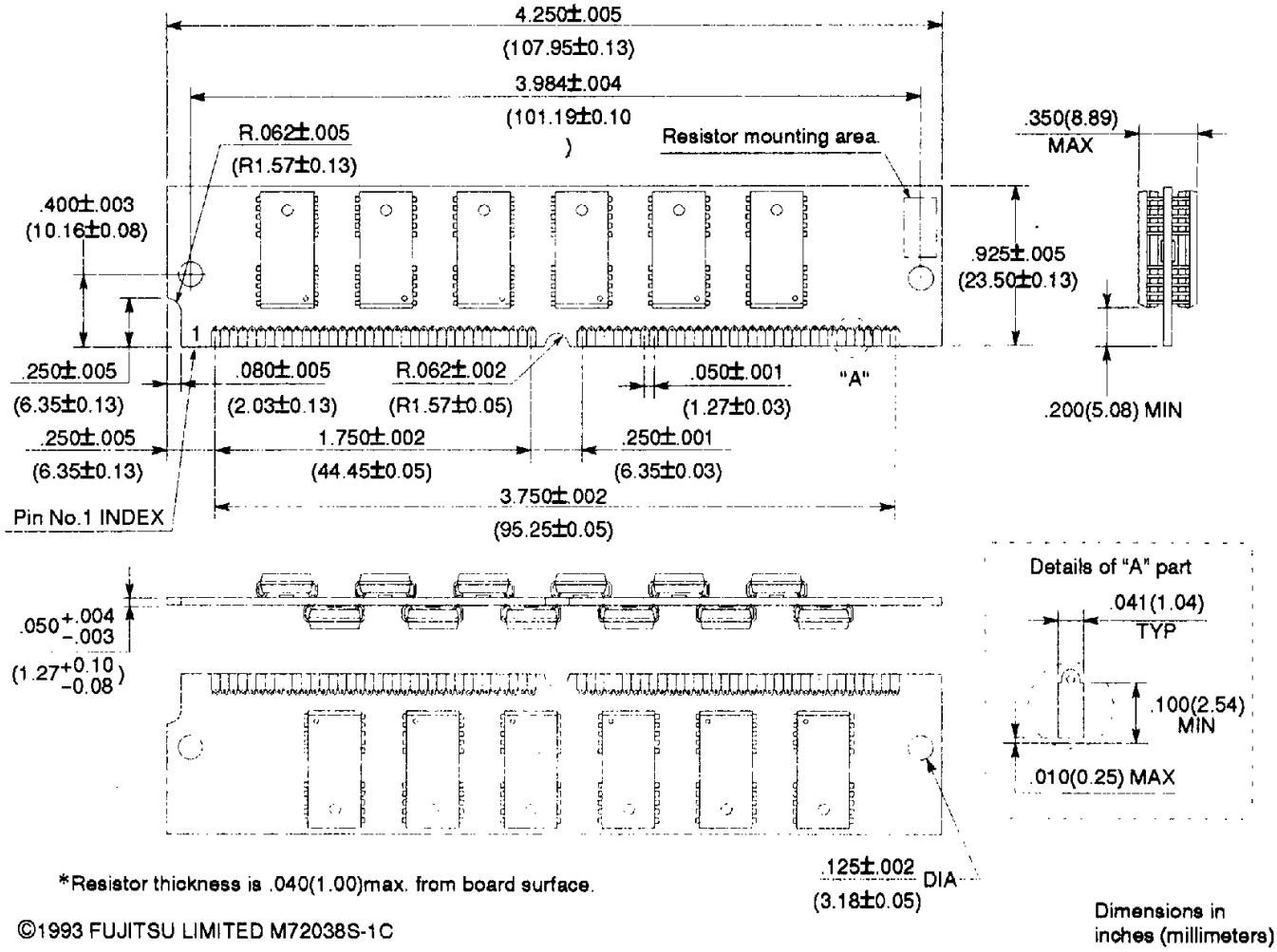
72-PAD PLASTIC SINGLE IN-LINE TYPE MODULE
(CASE No.: MSS-72P-P37)

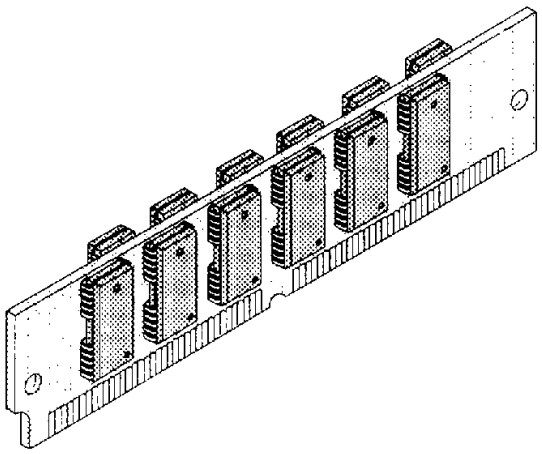


*Resistor thickness is .040(1.00)max. from board surface.

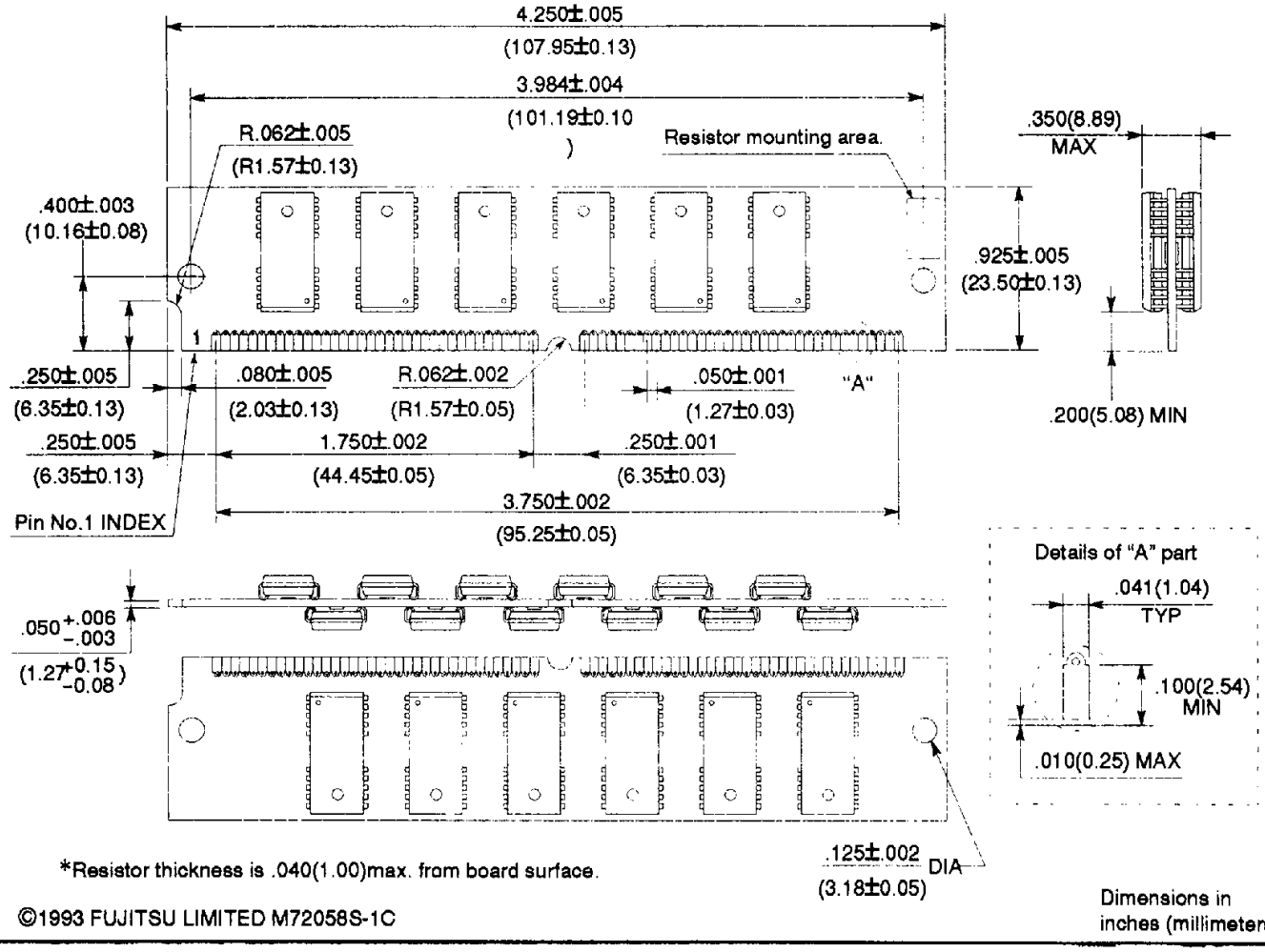
Dimensions in inches (millimeters)

PACKAGE DIMENSIONS

(Suffix: PJPB)



72-PAD PLASTIC SINGLE IN-LINE TYPE MODULE
(CASE No.: MSS-72P-P57)



*Resistor thickness is .040(1.00)max. from board surface.

Dimensions in inches (millimeters)