FUJITSU

PRODUCT PROFILE

MB85402-30/40

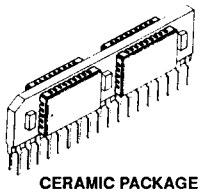
CMOS STATIC RAM MODULE

16384 Words x 16-Bit

PRELIMINARY

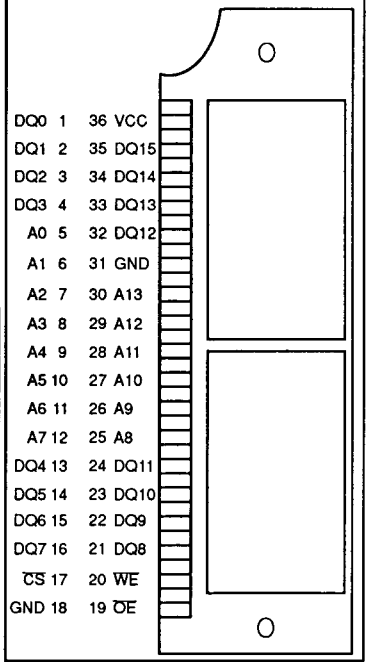
The Fujitsu MB85402 is a fully decoded, CMOS static random access memory module (SRAM) with four MB81C75 devices mounted on a 36-pin ceramic module. Organized as four 16K x 4 devices, the MB85402 is optimized for memory applications requiring high speed, large memory storage, and high density. A separate output enable function ($\overline{OE}$) provides maximum control for those systems where bus contention may be a problem.

- Organized as 16,384 x 16-Bit Words
- Access Time/Cycle Time
  - –30: 30 ns Max.
  - –40: 40 ns Max.
- Low Power Dissipation
  - Active: 1760 mW Max.
  - Standby: 220 mW CMOS Level
    440 mW TTL Level
- Static Operation
- Single +5 V ±10% Power Supply
- Common I/O
- Separate Output Enable ($\overline{OE}$)
- Disable $\overline{OE}$ function by connecting to GND
- Input/Output Pins TTL Compatible
- 36-pin ceramic Module (Dual-In-Line SIP)
- Temperature Range: 0°C to 70°C



CERAMIC PACKAGE
MTP–36C–C01

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Rating
Supply Voltage	V_{CC}	–0.5 to +7.0	V
Input Voltage	V_{IN}	–3.5 to +7.0	V
Output Voltage	V_{OUT}	–0.5 to +7.0	V
Short Circuit Output Current	I_{OUT}	±20	mA
Power Dissipation	P_D	4.0	W
Temperature under Bias	T_{BIAS}	–10 to +85	°C
Storage Temperature	T_{STG}	–65 to +150	°C

NOTE: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational section of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAPACITANCE (T_A = 25°C, f = 1MHz)

PARAMETER	SYMBOL	VALUE		UNIT
		Typ	Max	
Input Capacitance (V_{IN} = OV)	C_{IN}		50	pF
I/O Capacitance ($V_{I/O}$ = OV)	$C_{I/O}$		15	pF

DC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted)

PARAMETER		SYMBOL	VALUE			UNIT
			Min	Typ	Max	
Input Leakage Current (V_{IN} = OV to V_{CC})		I_{LI}	– 40		40	µA
Output Leakage Current ($\overline{CS}$ = V_{IH}, V_{OUT} = OV to V_{CC})		I_{LO}	– 40		40	µA
Standby Power Supply Current	CMOS level	I_{SB1}			40	mA
	TTL level	I_{SB2}			80	mA
Active Power Supply Current ($\overline{CS}$ = V_{IL}, I_{OUT} = O mA, V_{IN} = OV or V_{CC})		I_{CC1}			240	mA
Operating Power Supply Current (I_{OUT} = O mA, t_{CYCLE} = Min.)		I_{CC2}			400	mA
Input High Level		V_{IH}	2.2		6.0	V
Input Low Level[1]		V_{IL}	–0.5		0.8	V
Output High Level (I_{OH} = – 4 mA)		V_{OH}	2.4			V
Output Low Level (I_{OL} = 8 mA)		V_{OL}			0.4	V

Note: [1] –2.OV level with a maximum pulse width of 20 ns.

AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted)*

READ CYCLE

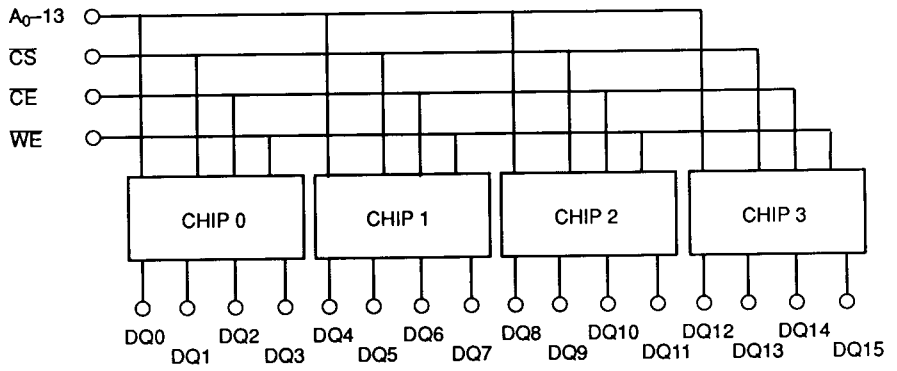
PARAMETER	SYM	MB85402–30		MB85402–40		UNIT	NOTE
		Min	Max	Min	Max		
Read Cycle Time	t_{RC}	30		40		ns	1
Address Access Time	t_{AA}		30		40	ns	2
$\overline{CS}$ Access Time	t_{ACS}		30		40	ns	3
$\overline{OE}$ Access Time	t_{OE}		13		15	ns	3
Output Hold from Address Change	t_{OH}	5		5		ns	
Output Hold from $\overline{CS}$	t_{OHC}	3		3		ns	
$\overline{CS}$ to Output Low–Z	t_{CLS}	5		5		ns	4,5
$\overline{OE}$ to Output Low–Z	t_{OLZ}	0		0		ns	4,5
$\overline{CS}$ to Output High–Z	t_{CHZ}		13		15	ns	4,5
$\overline{OE}$ to Output High–Z	t_{OHZ}		13		15	ns	4,5
Power Up from $\overline{CS}$	t_{PU}	0		0		ns	
Power Down from $\overline{CS}$	t_{PD}		25		30	ns	

WRITE CYCLE

PARAMETER	SYM	MB85402–30		MB85402–40		UNIT	NOTE
		Min	Max	Min	Max		
Write Cycle Time	t_{WC}	30		40		ns	2
Address Valid to End of Write	t_{AW}	25		35		ns	
$\overline{CS}$ to End of Write	t_{CW}	25		35		ns	
Data Valid to End of Write	t_{DW}	13		17		ns	
Data Hold Time	t_{DH}	2		2		ns	
Write Pulse Width	t_{WP}	25		35		ns	
Address Setup Time	t_{AS}	0		0		ns	
Write Recovery Time	t_{WR}	2		2		ns	
Output to High–Z	t_{WHZ}		13		15	ns	3,4
Output to Low–Z	t_{WLZ}		25		35	ns	3,4

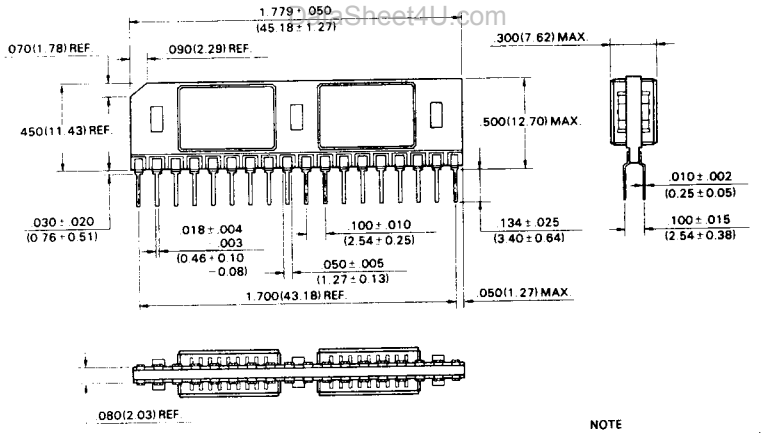
Notes: *Refer to MB81C75 data sheet electricals for an explanation of the notes.

FUNCTIONAL BLOCK DIAGRAM



PACKAGE DIMENSIONS

36-LEAD CERAMIC MODULE
(CASE NO.: MTP-36C-C01)



NOTE
1. Dimension in inches and (millimeters).