May 1990

PRODUCT PROFILE

FUJITSU

MB85415-30/40

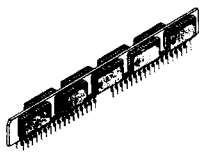
CMOS STATIC RAM MODULE

PRELIMINARY

16384 Words x 36-Bit

The Fujitsu MB85415 is a fully decoded, CMOS static random access memory module (SRAM) with nine MB81C75 devices mounted on a 70-pin Epoxy module. Additionally, these modules incorporate a presence detect feature that permits system level memory density verification for those applications with multiple modules. Organized as nine 16K x 4 common I/O devices, the MB85415 is optimized for memory applications where low power, high performance, large memory storage, and high density are required.

- Organized as 16384 x 36-Bit Words
- Access Time/Cycle Time
  –30: 30 ns Max.
  –40: 40 ns Max.
- Low Power Dissipation
  Active: 3960 mW (Max)
  Standby: 495 mW CMOS Level
  990 mW TTL Level
- Static Operation
- Single +5 V ±10% Power Supply
- Dual Control Pins (x4, x8)
- Presence Detect: PD0 = GND; PD1 = Open
- Common Data Inputs and Outputs
- Input/Output Pins TTL Compatible
- 70-pin Epoxy Module (ZIP)
- Temperature Range: 0°C to 70°C



PLASTIC PACKAGE
MZP–70P–P01

PIN ASSIGNMENT

PD0 (GND)	2	1	GND
DQ0	4	3	PD1
DQ0	6	5	DQ1
DQ0	8	7	DQ1
DQ0	10	9	DQ1
VCC	12	11	DQ1
A1	14	13	A0
A3	16	15	A2
A5	18	17	A4
DQ2	20	19	VSS
DQ2	22	21	DQ3
DQ2	24	23	DQ3
DQ2	26	25	DQ3
DQ4	28	27	DQ3
GND	30	29	DQ4
$\overline{W}1$	32	31	$\overline{W}2$
NC	34	33	NC
		35	$\overline{CS}1$
$\overline{CS}2$	36		
NC	38	37	NC
NC	40	39	$\overline{OE}$
DQ4	42	41	GND
DQ6	44	43	DQ4
DQ6	46	45	DQ5
DQ6	48	47	DQ5
DQ6	50	49	DQ5
GND	52	51	DQ5
A7	54	53	A6
A9	56	55	A8
A11	58	57	A10
A12	60	59	VCC
DQ8	62	61	A13
DQ8	64	63	DQ7
DQ8	66	65	DQ7
DQ8	68	67	DQ7
GND	70	69	DQ7

ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Rating
Supply Voltage	V_{CC}	–0.5 to +7.0	V
Input Voltage	V_{IN}	–3.5 to +7.0	V
Output Voltage	V_{OUT}	–0.5 to +7.0	V
Short Circuit Output Current	I_{OUT}	±50	mA
Power Dissipation	P_D	8.0	W
Temperature under Bias	T_{BIAS}	–10 to +85	°C
Storage Temperature	T_{STG}	–45 to +125	°C

NOTE: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational section of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages

CAPACITANCE (T_A = 25°C, f = 1MHz)

PARAMETER	SYMBOL	VALUE		UNIT
		Typ	Max	
Input Capacitance, Address and $\overline{OE}$	C_{IN1}		105	pF
Input Capacitance, $\overline{CS}_1$ and $\overline{WE}_1$	C_{IN2}		85	pF
Input Capacitance, $\overline{CS}_2$ and $\overline{WE}_2$	C_{IN3}		12	pF
Output Capacitance, DQ_{0-35}	$C_{I/O}$		12	pF

DC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted)*

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PARAMETER		SYMBOL	VALUE			UNIT
			Min	Typ	Max	
Input Leakage Current (V_{IN} = OV to V_{CC})		I_{LI}	–90		90	µA
Output Leakage Current ($\overline{CS}$ = V_{IH}, V_{OUT} = OV to V_{CC})		I_{LO}	–10		10	µA
Standby Power Supply Current	CMOS level	I_{SB1}			90	mA
	TTL level	I_{SB2}			180	mA
Active Power Supply Current ($\overline{CS}$ = V_{IL}, I_{OUT} = O mA)		I_{CC1}			540	mA
Operating Supply Current (Cycle = Min., I_{OUT} = 0 mA)		I_{CC2}			720	mA
Input High Level		V_{IH}	2.2		6.0	V
Input Low Level[1]		V_{IL}	–0.5		0.8	V
Output High Level (I_{OH} = –4 mA)		V_{OH}	2.4			V
Output Low Level (I_{OL} = 16 mA)		V_{OL}			0.4	V

Note: [1]–2.OV level with a maximum pulse width of 20 ns.

AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted)*

READ CYCLE

PARAMETER	SYM	MB85415-30		MB85415-40		UNIT	NOTE
		Min	Max	Min	Max		
Read Cycle Time	t_{RC}	30		40		ns	1
Address Access Time	t_{AA}		30		40	ns	
$\overline{CS}$ Access Time	t_{ACS}		30		40	ns	2
$\overline{OE}$ Access Time	t_{OE}		15		20	ns	2
Output Hold from Address Change	t_{OH}	5		5		ns	
Output Hold from Output Disable	t_{OHC}	3		3		ns	
$\overline{CS}$ to Output Low-Z	t_{CLZ}	5		5		ns	3,4
$\overline{OE}$ to Output Low-Z	t_{OLZ}	0		0		ns	3,4
$\overline{CS}$ to Output High-Z	t_{CHZ}		10		15	ns	3,4
$\overline{OE}$ to Output High-Z	t_{OHZ}		10		15	ns	3,4
Power Up from $\overline{CS}$	t_{PU}	0		0		ns	
Power Down from $\overline{CS}$	t_{PD}		20		30	ns	

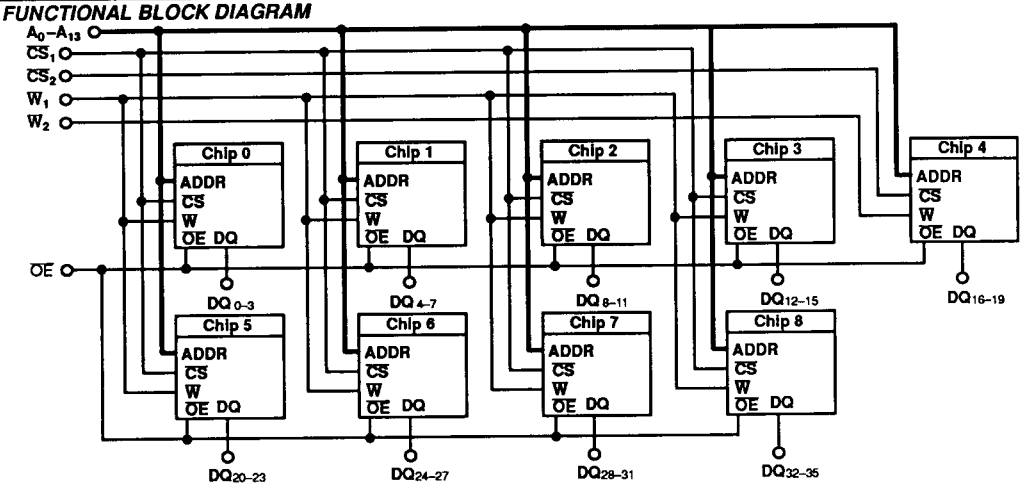
WRITE CYCLE

PARAMETER	SYM	MB85415-30		MB85415-40		UNIT	NOTE
		Min	Max	Min	Max		
Write Cycle Time	t_{WC}	30		40		ns	2
Address Valid to End of Write	t_{AW}	25		35		ns	
$\overline{CS}$ to End of Write	t_{CW}	25		35		ns	
Data Hold Time	t_{DH}	2		2		ns	
Write Pulse Width	t_{WP}	20		30		ns	
Data Valid to End of Write	t_{DW}	15		20		ns	
Address Setup Time	t_{AS}	0		0		ns	
Write Recovery Time	t_{WR}	2		2		ns	
Output High-Z from $\overline{WE}$	t_{WHZ}		10		15	ns	3,4
Output Low-Z from $\overline{WE}$	t_{LWZ}	0	20	0	20	ns	3,4

Notes: *Refer to MB81C75 data sheet electricals for an explanation of the notes.

MB85415-30/-40

FUNCTIONAL BLOCK DIAGRAM



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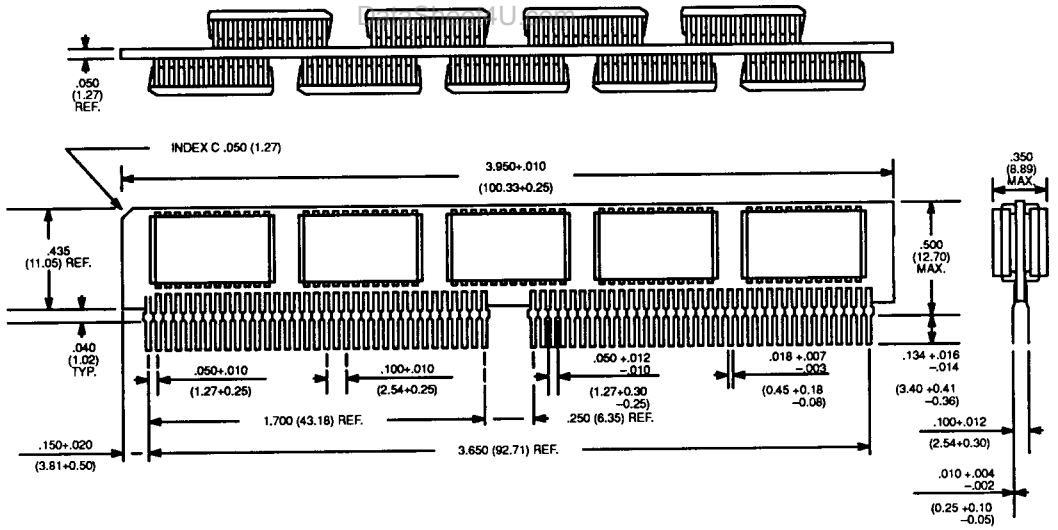
PACKAGE DIMENSIONS

70-LEAD EPOXY MODULE
(Case No.: MZP-70P-P01)



NOTE: Dimensions in inches
and (millimeters)