

May 1990

PRODUCT PROFILE

FUJITSU

MB85420-40/50**CMOS STATIC RAM MODULE****262144 Words x 8-Bit**

The Fujitsu MB85420 is a fully decoded, CMOS static random access memory module (SRAM) with eight MB81C81A devices mounted on a 60-pin Epoxy module. Two SELECT pins provide expansion to 512K four bit words. Additionally, these modules incorporate a presence detect feature that permits system level memory density verification for those applications with multiple modules. Organized as eight 256Kx1 devices, the MB85420 is optimized for memory applications where low power, high performance, large memory storage, and high density are required.

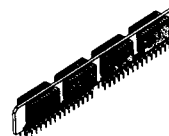
- Organized as 262,144 x 8-Bit Words
- Access Time/Cycle Time
 - 40: 40 ns Max.
 - 50: 50 ns Max.
- Low Power Dissipation
 - Active: 5280 mW Max. (–40)
 - 4400 mW Max. (–50)
 - Standby: 660 mW Max
 - CMOS Level
 - 1320 mW Max
 - TTL Level
- Static Operation
- Single +5 V \pm 10% Power Supply
- Dual SELECT Pins (x4, x8)
- Presence Detect: PD0 = Open; PD1 = GND
- Separate Data Inputs and Outputs
- Input/Output Pins TTL Compatible
- 60-pin Epoxy Module (ZIP)
- Temperature Range: 0°C to 70°C

ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Rating
Supply Voltage	V _{CC}	–0.5 to +7.0	V
Input Voltage	V _{IN}	–3.5 to +7.0	V
Output Voltage	V _{OUT}	–0.5 to +7.0	V
Short Circuit Output Current	I _{OUT}	\pm 20	mA
Power Dissipation	P _D	8.0	W
Temperature under Bias	T _{BIAS}	–10 to +85	°C
Storage Temperature	T _{STG}	–45 to +125	°C

NOTE: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational section of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

PRELIMINARY

PLASTIC PACKAGE
MZP-60P-P02

PAD ASSIGNMENT

PD0	2	1	VSS
NC	4	3	PD1
VCC	6	5	NC
D0	8	7	D1
Q0	10	9	Q1
A9	12	11	NC
A14	14	13	A10
A12	16	15	A11
A17	18	17	A13
VSS	20	19	A16
D2	22	21	D3
Q2	24	23	Q3
WE	26	25	VCC
A4	28	27	A15
CS1	30	29	NC
NC	32	31	CS2
NC	34	33	NC
VCC	36	35	NC
D4	38	37	D5
Q4	40	39	Q5
A0	42	41	VSS
A6	44	43	A1
A2	46	45	A5
A7	48	47	A3
A9	49	48	A8
NC	50	51	D7
D6	52	53	Q7
Q6	54	55	VCC
NC	56	57	NC
NC	58	59	NC
VSS	60	58	NC

DataSheet

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MB85420-40/-50**CAPACITANCE ($T_A = 25^\circ\text{C}$, $f = 1\text{MHz}$)**

PARAMETER	SYMBOL	VALUE		UNIT
		Typ	Max	
Input Capacitance, Address and WE	C_{IN1}		70	pF
Input Capacitance, \overline{CS}_1 and \overline{CS}_2	C_{IN2}		45	pF
Input Capacitance, D_{IN}	C_{IN3}		9	pF
Output Capacitance, D_{OUT}	C_{OUT}		12	pF

DC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted)

PARAMETER	SYMBOL	VALUE			UNIT
		Min	Typ	Max	
Input Leakage Current ($V_{IN} = 0\text{V to }V_{CC}$)	I_{LI}	-80		80	μA
Output Leakage Current ($\overline{CS} = V_{IH}$, $V_{OUT} = 0\text{V to }V_{CC}$)	I_{LO}	-50		50	μA
Standby Power Supply Current	CMOS level			120	mA
	TTL level			240	mA
Active Power Supply Current ($\overline{CS} = V_{IL}$, $I_{OUT} = 0\text{ mA}$)	MB85420-40			960	mA
	MB85420-50			800	mA
Peak Power on Supply Current ($\overline{CS} = \text{Lower of }V_{CC}\text{ or }V_{IH}$)	I_{PO}			240	mA
Input High Level	V_{IH}	2.2		6.0	V
Input Low Level ¹	V_{IL}	-0.5		0.8	V
Input High Level ($I_{OH} = -4\text{ mA}$)	V_{OH}	2.4			V
Input Low Level ($I_{OL} = 16\text{ mA}$)	V_{OL}			0.4	V

Note: ¹-3.0V level with a maximum pulse width of 20 ns.

MB85420-40/-50**AC CHARACTERISTICS**

(At recommended operating conditions unless otherwise noted)*

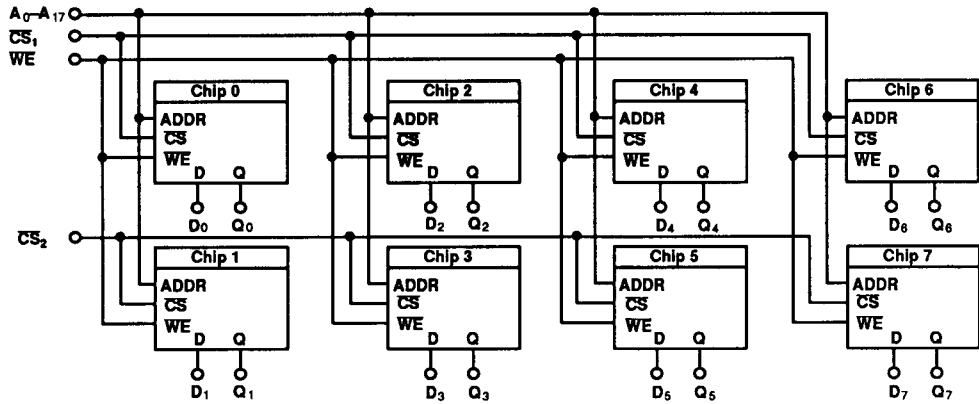
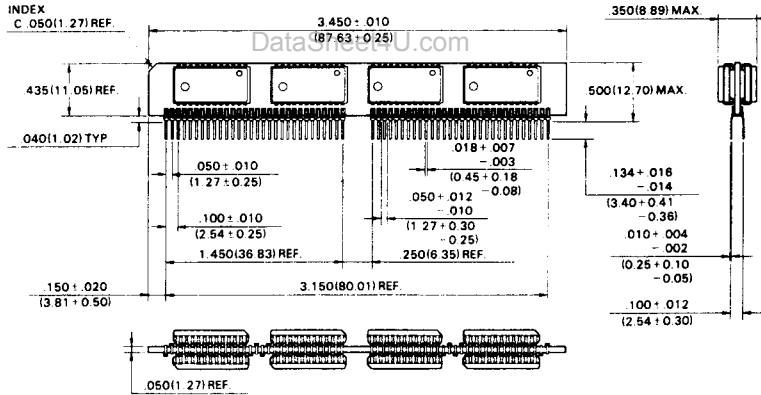
READ CYCLE

PARAMETER	SYM	MB85420-40		MB85420-50		UNIT	NOTE
		Min	Max	Min	Max		
Read Cycle Time	t_{RC}	40		50		ns	1
Address Access Time	t_{AA}		40		50	ns	
CS Access Time	t_{ACS}		40		50	ns	2
Output Hold from Address Change	t_{OH}	5		5		ns	
CS to Output Low-Z	t_{LZ}	5		5		ns	3,4
CS to Output High-Z	t_{HZ}	0	20	0	25	ns	3,4
Power Up from CS	t_{PU}	0		0		ns	
Power Down from CS	t_{PD}		40		50	ns	

WRITE CYCLE

PARAMETER	SYM	MB85420-40		MB85420-50		UNIT	NOTE
		Min	Max	Min	Max		
Write Cycle Time	t_{WC}	40		50		ns	2
Address Valid to End of Write	t_{AW}	35		45		ns	
CS to End of Write	t_{CW}	35		45		ns	
Data Valid to End of Write	t_{DW}	20		25		ns	
Data Hold Time	t_{DH}	0		0		ns	
Write Pulse Width	t_{WP}	30		35		ns	
Address Setup Time	t_{AS1}	5		5		ns	
	t_{AS2}	0		0		ns	
Write Recovery Time	t_{WR}	5		5		ns	
Output High-Z from WE	t_{WZ}	0	20	0	25	ns	3,4
Output Low-Z from WE	t_{OW}	0		0		ns	3,4

Notes: * Refer to MB81C81A data sheet electricals for an explanation of the notes.

MB85420-40/-50**FUNCTIONAL BLOCK DIAGRAM****PACKAGE DIMENSIONS****60-Lead Epoxy Module
(Case No. MZP-60P-P02)****NOTES**

- 1 Dimension in inches and (millimeters).
- 2 Pin No. 1, Back side