May 1990

PRODUCT PROFILE

FUJITSU

MB85421-40/50

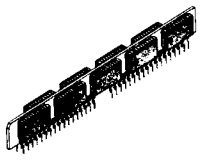
CMOS STATIC RAM MODULE

PRELIMINARY

262144 Words x 9-Bit

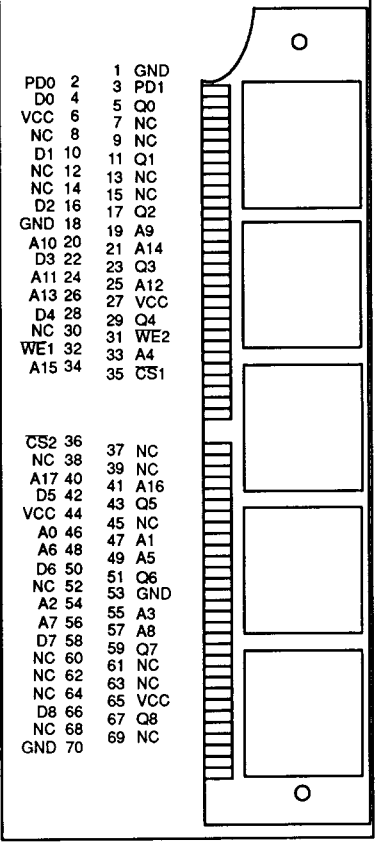
The Fujitsu MB85421 is a fully decoded, CMOS static random access memory module with nine MB81C81A devices mounted on a 70-pin Epoxy module. A separate SELECT pin provides parity capability. Additionally, these modules incorporate a presence detect feature that permits system level verification of memory density for those applications with multiple modules. Organized as nine 256K x 1 devices, the MB85421 is optimized for memory applications where low power, high performance, large memory storage, and high density are required.

- Organized as 262,144 x 9-Bit Words
- Access Time/Cycle Time
  - –40: 40 ns Max.
  - –50: 50 ns Max.
- Low Power Dissipation
  - Active: 5940 mW Max. (–40)
    4950 mW Max. (–50)
  - Standby: 742 CMOS Level
    1485 TTL Leve)
- Static Operation
- Single +5 V ±10% Power Supply
- Parity Capability
- Presence Detect: PD0 = Open; PD1 = GND
- Separate Data Inputs and Outputs
- Input/Output Pins TTL Compatible
- 70-pin Epoxy Module (ZIP)
- Temperature Range: 0°C to 70°C



PLASTIC PACKAGE
MZP-70P-P01

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Rating
Supply Voltage	V_{CC}	–0.5 to +7.0	V
Input Voltage	V_{IN}	–3.5 to +7.0	V
Output Voltage	V_{OUT}	–0.5 to +7.0	V
Short Circuit Output Current	I_{OUT}	±20	mA
Power Dissipation	P_D	8.0	W
Temperature under Bias	T_{BIAS}	–10 to +85	°C
Storage Temperature	T_{STG}	–45 to +125	°C

NOTE: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational section of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

CAPACITANCE (T_A = 25°C, f = 1MHz)

PARAMETER	SYMBOL	VALUE		UNIT
		Typ	Max	
Input Capacitance, Address, $\overline{WE}_1$, and $\overline{CS}_1$	C_{IN1}		105	pF
Input Capacitance, $\overline{CS}_2$ and $\overline{WE}_2$, D_{IN}	C_{IN2}		15	pF
Output Capacitance, D_{OUT}	C_{OUT}		15	pF

DC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted)

PARAMETER		SYMBOL	VALUE			UNIT
			Min	Typ	Max	
Input Leakage Current (V_{IN} = OV to V_{CC})		I_{LI}	–90		90	µA
Output Leakage Current ($\overline{CS}$ = V_{IH}, V_{OUT} = OV to V_{CC})		I_{LO}	–50		50	µA
Standby Power Supply Current	CMOS level	I_{SB1}			135	mA
	TTL level	I_{SB2}			270	mA
Active Power Supply Current ($\overline{CS}$ = V_{IL}, I_{OUT} = O mA)	MB85420–40	I_{CC}			1080	mA
	MB85420–50				900	mA
Peak Power on Supply Current ($\overline{CS}$ = Lower of V_{CC} or V_{IH})		I_{PO}			240	mA
Input High Level		V_{IH}	2.2		6.0	V
Input Low Level[1]		V_{IL}	–0.5		0.8	V
Input High Level (I_{OH} = –4 mA)		V_{OH}	2.4			V
Input Low Level (I_{OL} = 16 mA)		V_{OL}			0.4	V

Note: [1]–2.OV level with a maximum pulse width of 20 ns.

AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted)*

READ CYCLE

PARAMETER	SYM	MB85421–40		MB85421–50		UNIT	NOTE
		Min	Max	Min	Max		
Read Cycle Time	t_{RC}	40		50		ns	1
Address Access Time	t_{AA}		40		50	ns	
$\overline{CS}$ Access Time	t_{ACS}		40		50	ns	2
Output Hold from Address Change	t_{OH}	5		5		ns	
$\overline{CS}$ to Output Low–Z	t_{LZ}	5		5		ns	3,4
$\overline{CS}$ to Output High–Z	t_{HZ}	0	20	0	25	ns	3,4
Power Up from $\overline{CS}$	t_{PU}	0		0		ns	
Power Down from $\overline{CS}$	t_{PD}		40		50	ns	

WRITE CYCLE

PARAMETER	SYM	MB85421–40		MB85421–50		UNIT	NOTE
		Min	Max	Min	Max		
Write Cycle Time	t_{WC}	40		50		ns	2
Address Valid to End of Write	t_{AW}	35		45		ns	
$\overline{CS}$ to End of Write	t_{CW}	35		45		ns	
Data Valid to End of Write	t_{DW}	20		25		ns	
Data Hold Time	t_{DH}	0		0		ns	
Write Pulse Width	t_{WP}	30		35		ns	
Address Setup Time	t_{AS1}	5		5		ns	
	t_{AS2}	0		0		ns	
Write Recovery Time	t_{WR}	5		5		ns	
Output High–Z from $\overline{WE}$	t_{WZ}	0	20	0	25	ns	3,4
Output Low–Z from $\overline{WE}$	t_{OW}	0		0		ns	3,4

Notes: * Refer to MB81C81A data sheet electricals for an explanation of the notes.

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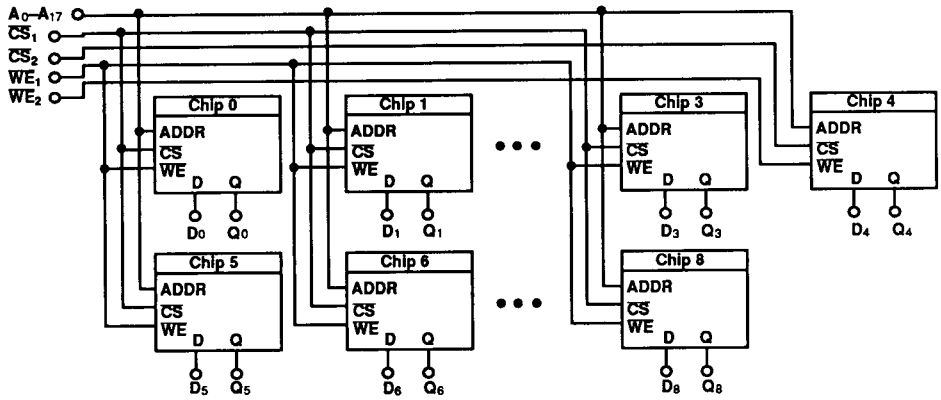
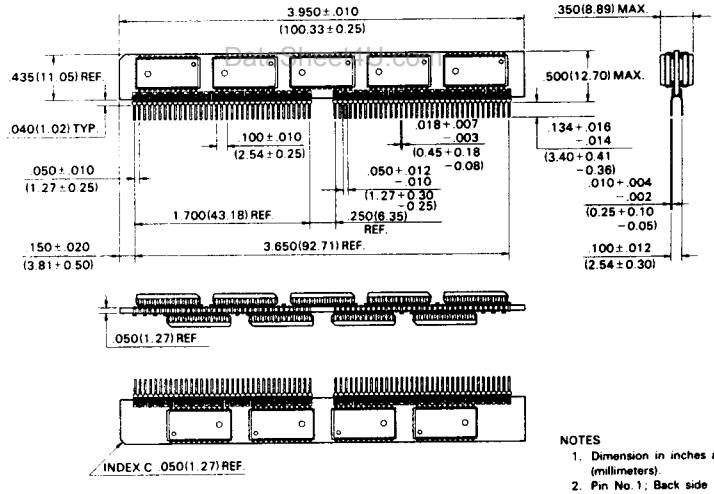
MB85421-40/-50

FUNCTIONAL BLOCK DIAGRAM



PACKAGE DIMENSIONS

70-Lead Epoxy Module
(Case No.: MZP-70P-P01)



NOTES
1. Dimension in inches and (millimeters).
2. Pin No.1; Back side