FUJITSU SEMICONDUCTOR
DATA SHEET

DS501-00006-3v1-E

Memory FRAM

4 M Bit (256 K × 16)

MB85R4002A

■ DESCRIPTIONS

The MB85R4002A is an FRAM (Ferroelectric Random Access Memory) chip consisting of 262,144 words × 16 bits of nonvolatile memory cells fabricated using ferroelectric process and silicon gate CMOS process technologies.
The MB85R4002A is able to retain data without using a back-up battery, as is needed for SRAM.
The memory cells used in the MB85R4002A can be used for 10^{10} read/write operations, which is a significant improvement over the number of read and write operations supported by Flash memory and E^2PROM.
The MB85R4002A uses a pseudo-SRAM interface that is compatible with conventional asynchronous SRAM.

■ FEATURES

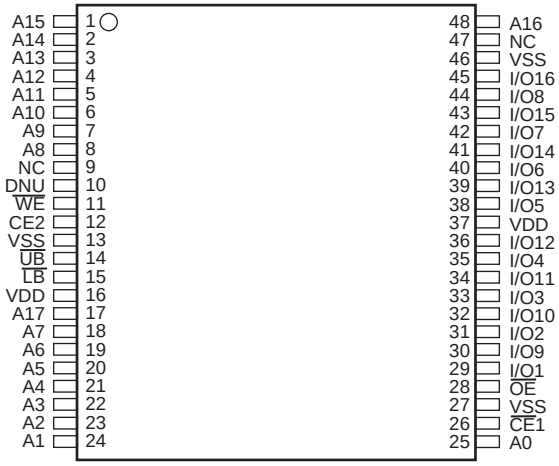
- Bit configuration : 262,144 words × 16 bits
- $\overline{LB}$ and $\overline{UB}$ data byte control
- Read/write endurance : 10^{10} times / byte
- Data retention : 10 years (+ 55 °C), 55 years (+ 35 °C)
- Operating power supply voltage : 3.0 V to 3.6 V
- Low power operation : Operating power supply current 15 mA (Typ)
  Standby current 50 μA (Typ)
- Operation ambient temperature range : − 40 °C to + 85 °C
- Package : 48-pin plastic TSOP (FPT-48P-M48)
  RoHS compliant

2013.4

FUJITSU

■ PIN ASSIGNMENTS

(TOP VIEW)

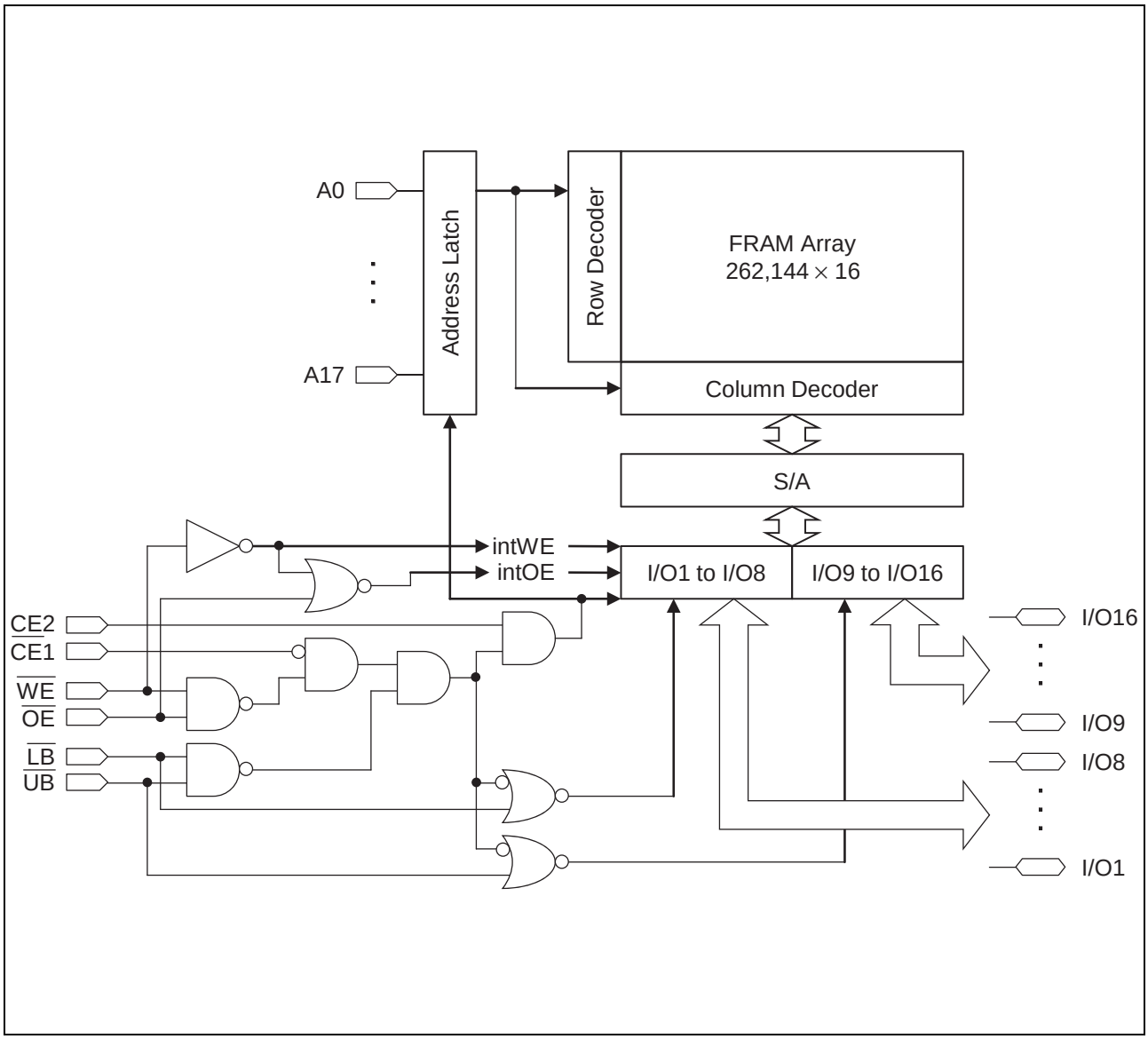


(FPT-48P-M48)

■ PIN DESCRIPTIONS

Pin Number	Pin Name	Functional Description
1 to 8, 17 to 25, 48	A0 to A17	Address Input pins
29 to 36, 38 to 45	I/O1 to I/O16	Data Input/Output pins
26	$\overline{CE}1$	Chip Enable 1 Input pin
12	CE2	Chip Enable 2 Input pin
11	$\overline{WE}$	Write Enable Input pin
28	$\overline{OE}$	Output Enable Input pin
14, 15	$\overline{LB}$, $\overline{UB}$	Data Byte Control Input pins
16, 37	VDD	Supply Voltage pins Connect all two pins to the power supply.
13, 27, 46	VSS	Ground pins Connect all three pins to ground.
9, 47	NC	No Connect pins Leave these pins open, or connect to VDD or VSS.
10	DNU	Do Not Use pin Make sure to connect this pin to VDD.

■ BLOCK DIAGRAM



■ FUNCTIONAL TRUTH TABLE

Mode	$\overline{CE1}$	CE2	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	I/O1 to I/O8	I/O9 to I/O16	Supply Current
Standby Precharge	H	X	X	X	X	X	Hi-Z	Hi-Z	Standby (I_{SB})
	X	L	X	X	X	X			
	X	X	H	H	X	X			
	X	X	X	X	H	H			
Read	↓	H	H	L	L	L	Data Output	Data Output	Operation (I_{DD})
					L	H	Data Output	Hi-Z	
					H	L	Hi-Z	Data Output	
	L	↑	H	L	L	L	Data Output	Data Output	
					L	H	Data Output	Hi-Z	
					H	L	Hi-Z	Data Output	
Read (Pseudo-SRAM, $\overline{OE}$ control*1)	L	H	H	↓	L	L	Data Output	Data Output	
					L	H	Data Output	Hi-Z	
					H	L	Hi-Z	Data Output	
Write	↓	H	L	H	L	L	Data Input	Data Input	
					L	H	Data Input	Hi-Z	
					H	L	Hi-Z	Data Input	
	L	↑	L	H	L	L	Data Input	Data Input	
					L	H	Data Input	Hi-Z	
					H	L	Hi-Z	Data Input	
Write (Pseudo-SRAM, $\overline{WE}$ control*2)	L	H	↓	H	L	L	Data Input	Data Input	
					L	H	Data Input	Hi-Z	
					H	L	Hi-Z	Data Input	

Note: L = V_{IL}, H = V_{IH}, X can be either H, L, ↓ or ↑, Hi-Z = High Impedance

↓ : Latch address and latch data at falling edge, ↑ : Latch address and latch data at rising edge

*1 : $\overline{OE}$ control of the Pseudo-SRAM means the valid address at the falling edge of $\overline{OE}$ to read.

*2 : $\overline{WE}$ control of the Pseudo-SRAM means the valid address and data at the falling edge of $\overline{WE}$ to write.

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Power Supply Voltage*	V_{DD}	–0.5	+4.0	V
Input Pin Voltage*	V_{IN}	–0.5	V_{DD} + 0.5 (≤ 4.0)	V
Output Pin Voltage*	V_{OUT}	–0.5	V_{DD} + 0.5 (≤ 4.0)	V
Operation Ambient Temperature	T_A	–40	+85	°C
Storage Temperature	T_{STG}	–55	+125	°C

* : All voltages are referenced to VSS (ground 0 V).

WARNING: Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings.
Do not exceed any of these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage*	V_{DD}	3.0	3.3	3.6	V
High Level Input Voltage*	V_{IH}	$V_{DD} \times 0.8$	—	V_{DD} + 0.5 (≤ 4.0)	V
Low Level Input Voltage*	V_{IL}	–0.5	—	+0.6	V
Operation Ambient Temperature	T_A	– 40	—	+85	°C

* : All voltages are referenced to VSS (ground 0 V).

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions.

Any use of semiconductor devices will be under their recommended operating condition.
Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure.

No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

(within recommended operating conditions)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Input Leakage Current*1	$\|I_{LI}\|$	V_{IN} = 0 V to V_{DD}	—	—	10	µA
Output Leakage Current	$\|I_{LO}\|$	V_{OUT} = 0 V to V_{DD}, $\overline{CE}1$ = V_{IH} or $\overline{OE}$ = V_{IH}	—	—	10	µA
Operating Power Supply Current*2	I_{DD}	$\overline{CE}1$ = 0.2 V, CE2 = V_{DD} – 0.2 V, I_{out} = 0 mA	—	15	20	mA
Standby Current*3	I_{SB}	$\overline{CE}1 \geq V_{DD} - 0.2$ V	—	50	150	µA
		CE2 ≤ 0.2 V				
		$\overline{OE} \geq V_{DD} - 0.2$ V, $\overline{WE} \geq V_{DD} - 0.2$ V				
		$\overline{LB} \geq V_{DD} - 0.2$ V, $\overline{UB} \geq V_{DD} - 0.2$ V				
High Level Output Voltage	V_{OH}	I_{OH} = – 1.0 mA	$V_{DD} \times 0.8$	—	—	V
Low Level Output Voltage	V_{OL}	I_{OL} = 2.0 mA	—	—	0.4	V

*1 : This also applies to DNU pins.

*2 : During the measurement of I_{DD} , the Address and Data In were taken to only change once per active cycle.
Iout : output current

*3 : All pins other than setting pins shall be input at the CMOS level voltages such as H ≥ V_{DD} – 0.2 V, L ≤ 0.2 V.

2. AC Characteristics

• **AC Test Conditions**

Power Supply Voltage	: 3.0 V to 3.6 V
Operation Ambient Temperature	: –40 °C to +85 °C
Input Voltage Amplitude	: 0.3 V to 2.7 V
Input Rising Time	: 5 ns
Input Falling Time	: 5 ns
Input Evaluation Level	: 2.0 V / 0.8 V
Output Evaluation Level	: 2.0 V / 0.8 V
Output Load Capacitance	: 50 pF

(1) Read Cycle

Parameter	Symbol	Value		Unit
		Min	Max	
Read Cycle time	t_{RC}	150	—	ns
$\overline{CE}$1 Active Time	t_{CA1}	120	—	ns
CE2 Active Time	t_{CA2}	120	—	ns
$\overline{OE}$ Active Time	t_{RP}	120	—	ns
$\overline{LB}$, $\overline{UB}$ Active Time	t_{BP}	120	—	ns
Precharge Time	t_{PC}	20	—	ns
Address Setup Time	t_{AS}	0	—	ns
Address Hold Time	t_{AH}	50	—	ns
$\overline{OE}$ Setup Time	t_{ES}	0	—	ns
$\overline{LB}$, $\overline{UB}$ Setup Time	t_{BS}	5	—	ns
Output Data Hold time	t_{OH}	0	—	ns
Output Set Time	t_{LZ}	30	—	ns
$\overline{CE}$1 Access Time	t_{CE1}	—	120	ns
CE2 Access Time	t_{CE2}	—	120	ns
$\overline{OE}$ Access Time	t_{OE}	—	120	ns
Output Floating Time	t_{OHZ}	—	20	ns

(2) Write Cycle

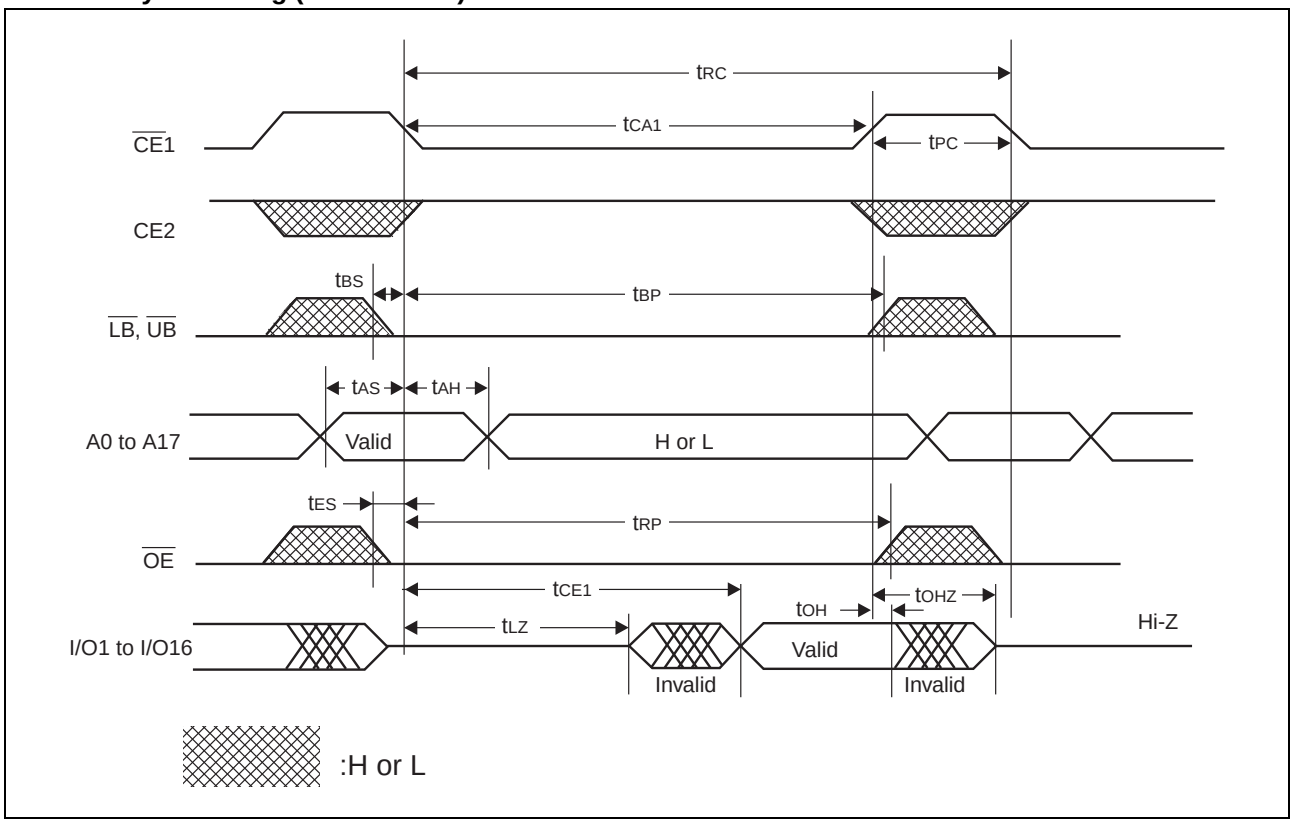
Parameter	Symbol	Value		Unit
		Min	Max	
Write Cycle Time	t_{WC}	150	—	ns
$\overline{CE}$1 Active Time	t_{CA1}	120	—	ns
CE2 Active Time	t_{CA2}	120	—	ns
$\overline{LB}$, $\overline{UB}$ Active Time	t_{BP}	120	—	ns
Precharge Time	t_{PC}	20	—	ns
Address Setup Time	t_{AS}	0	—	ns
Address Hold Time	t_{AH}	50	—	ns
$\overline{LB}$, $\overline{UB}$ Setup Time	t_{BS}	5	—	ns
Write Pulse Width	t_{WP}	120	—	ns
Data Setup Time	t_{DS}	0	—	ns
Data Hold Time	t_{DH}	50	—	ns
Write Setup Time	t_{WS}	0	—	ns

3. Pin Capacitance

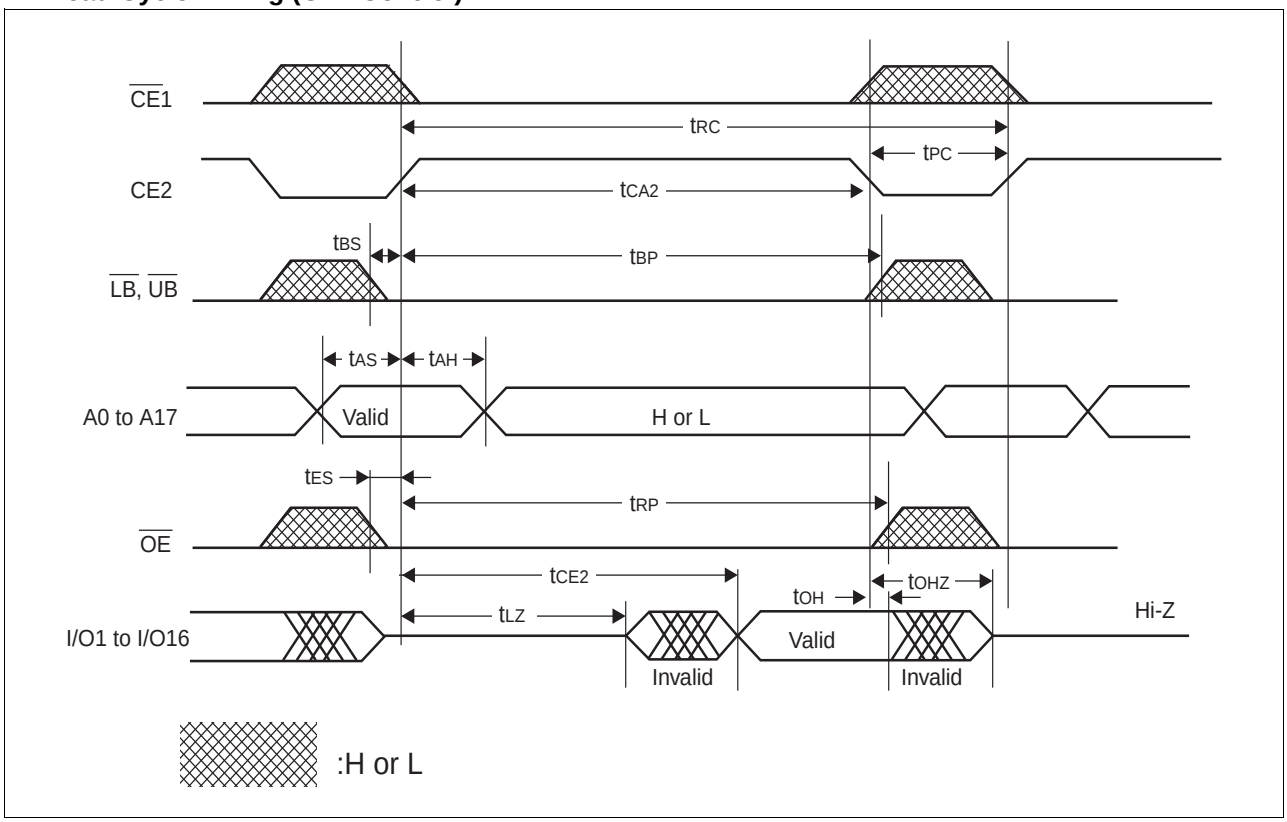
Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Input Capacitance	C_{IN}	$V_{DD} = V_{IN} = V_{OUT} = 0$ V, f = 1 MHz, $T_A = +25$ °C	—	—	10	pF
Output Capacitance	C_{OUT}		—	—	10	pF
DNU Pin Input Capacitance	C_{DNU}		—	—	10	pF

■ TIMING DIAGRAMS

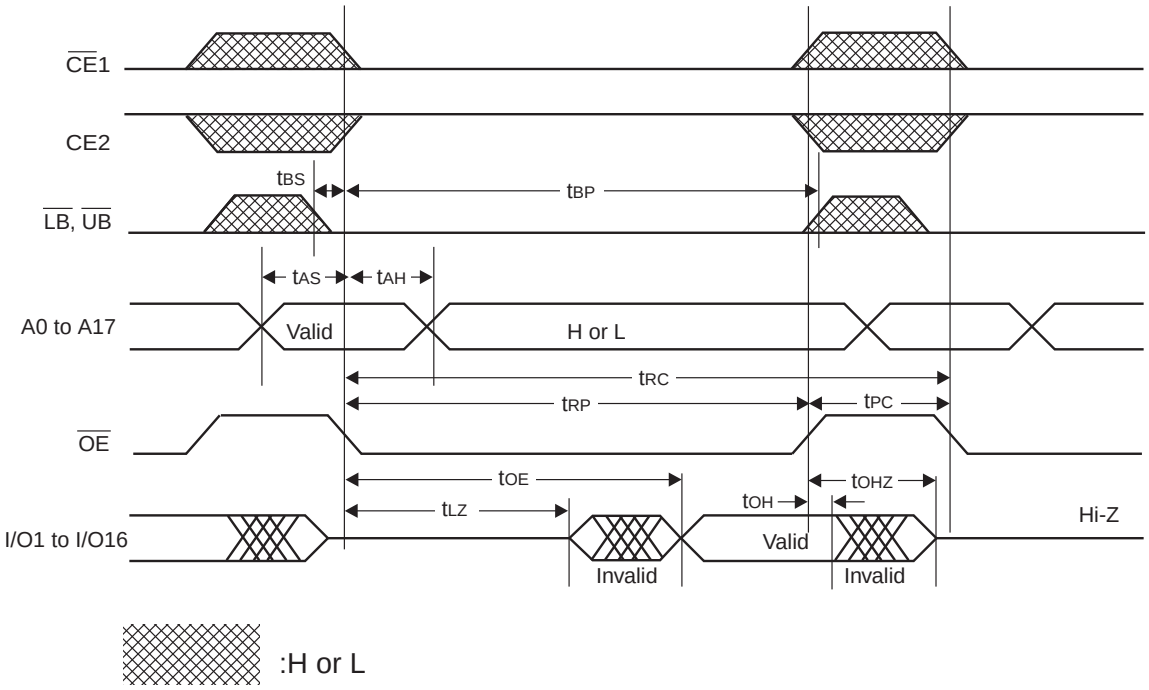
1. Read Cycle Timing ($\overline{CE}$1 Control)



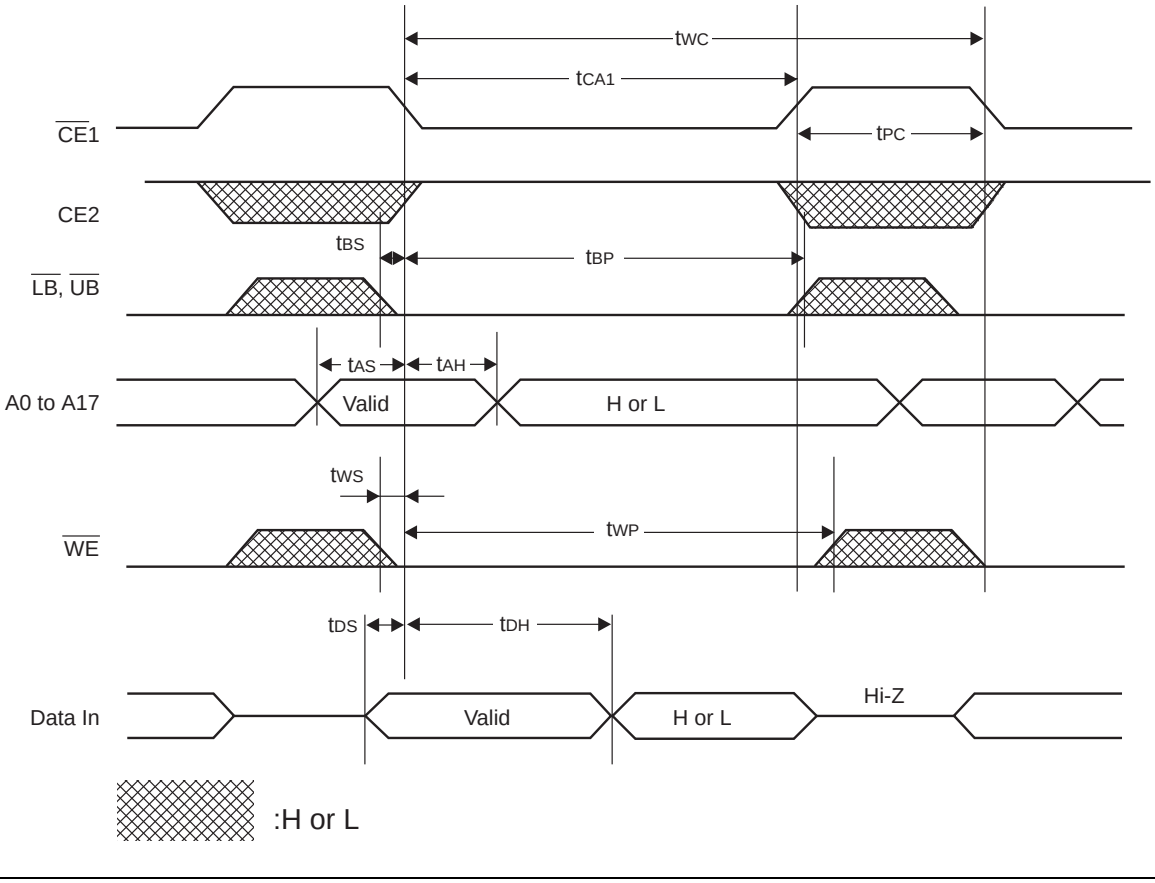
2. Read Cycle Timing (CE2 Control)



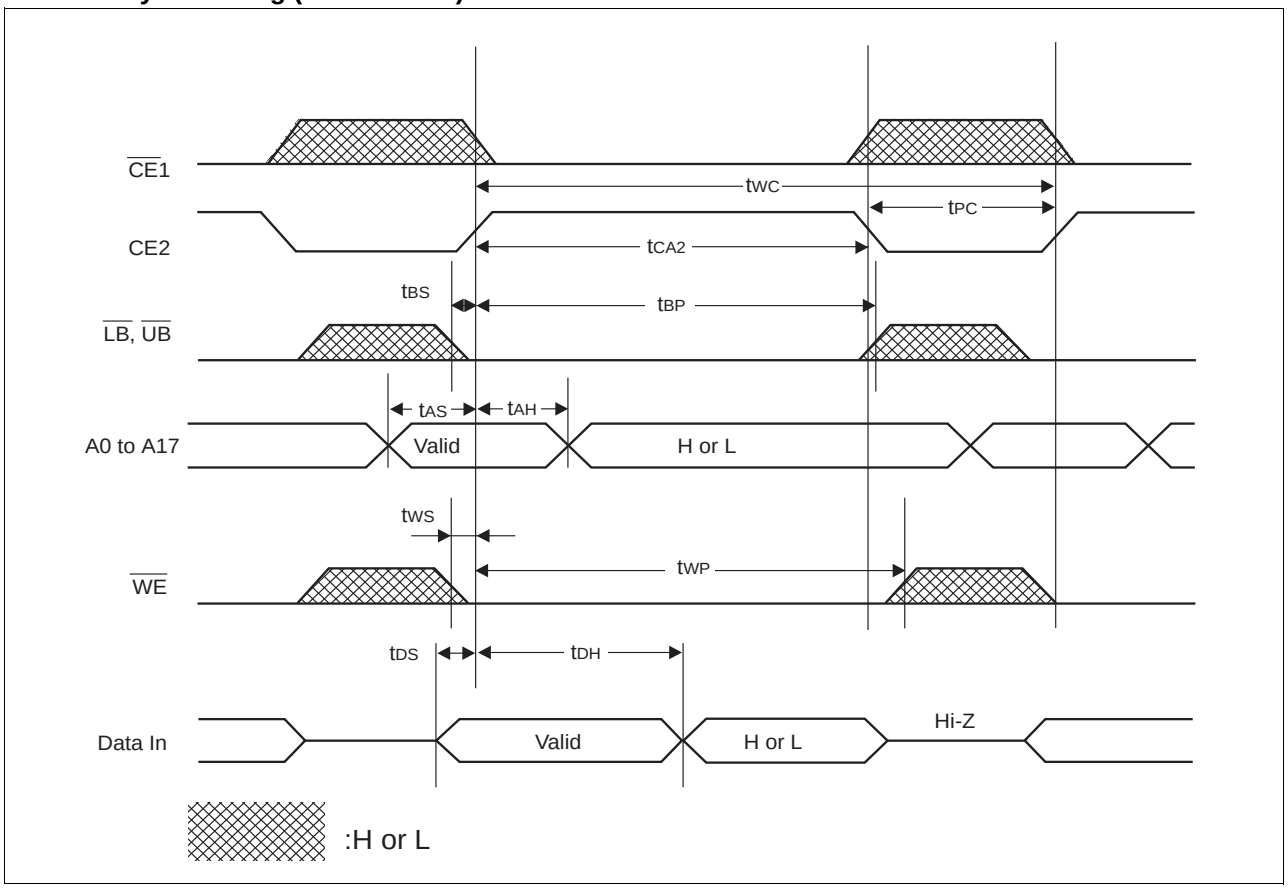
3. Read Cycle Timing ($\overline{OE}$ Control)



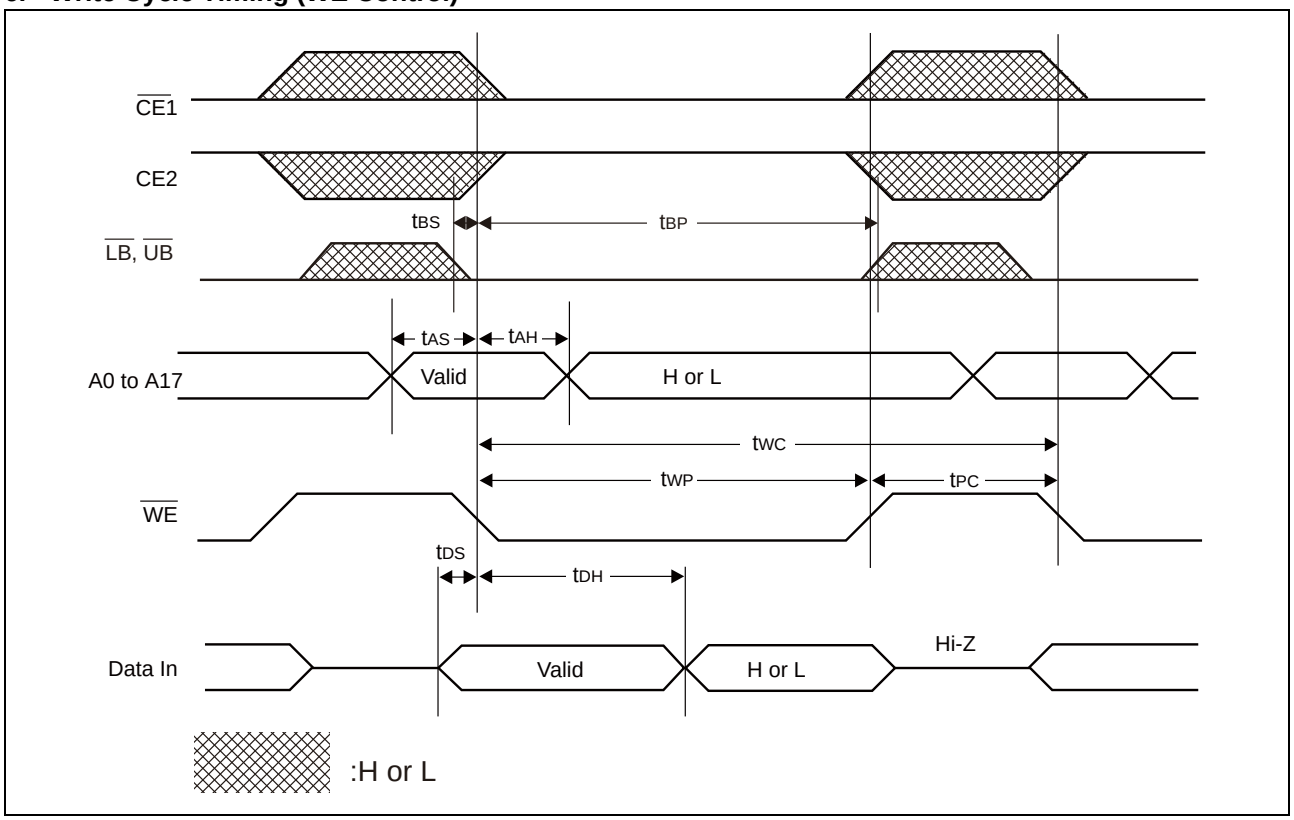
4. Write Cycle Timing ($\overline{CE1}$ Control)



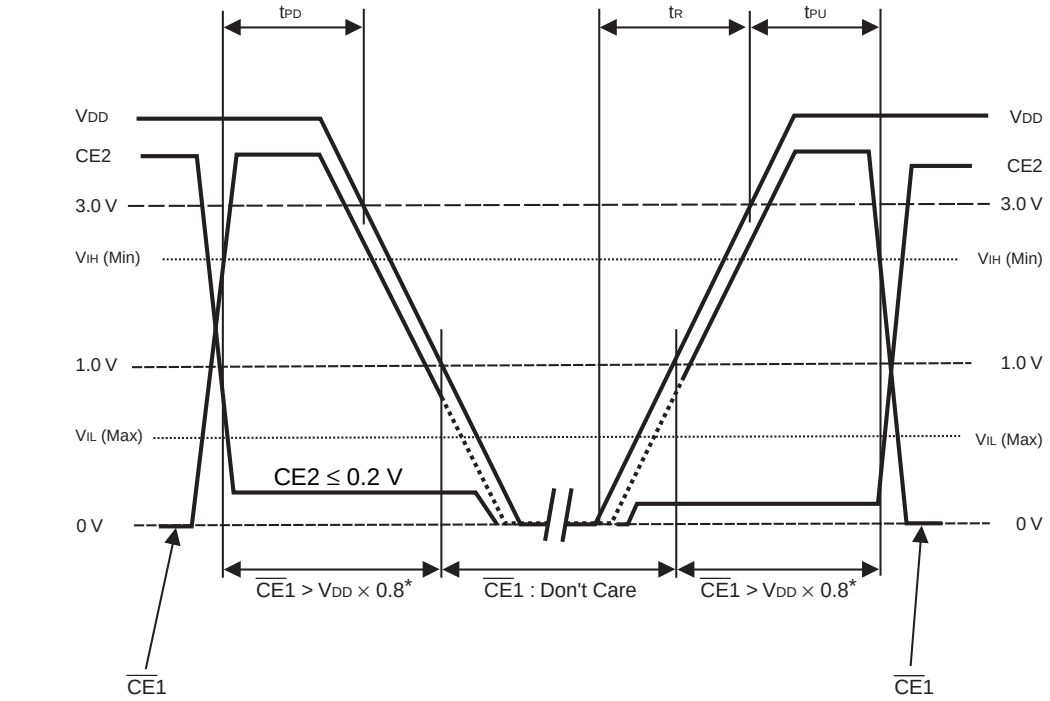
5. Write Cycle Timing (CE2 Control)



6. Write Cycle Timing ($\overline{WE}$ Control)



■ POWER ON/OFF SEQUENCE



Parameter	Symbol	Value			Unit
		Min	Typ	Max	
$\overline{CE}1$ level hold time for Power OFF	t_{PD}	85	—	—	ns
$\overline{CE}1$ level hold time for Power ON	t_{PU}	85	—	—	ns
Power supply rising time	t_R	0.05	—	200	ms

If the device does not operate within the specified conditions of read cycle, write cycle or power on/off sequence, memory data can not be guaranteed.
In case the power is turned on or off, use the power supply reset IC and fix the CE2 to low level, to prevent unexpected writing. Use either of $\overline{CE}1$ or CE2, or both to disable control of the device.

■ FRAM CHARACTERISTICS

Item	Min	Max	Unit	Parameter
Read/Write Endurance*1	10^{10}	—	Times/byte	Operation Ambient Temperature T_A = + 85 °C
Data Retention*2	10	—	Years	Operation Ambient Temperature T_A = + 55 °C
	55	—		Operation Ambient Temperature T_A = + 35 °C

*1 : Total number of reading and writing defines the minimum value of endurance, as an FRAM memory operates with destructive readout mechanism.

*2 : Minimun values define retention time of the first reading/writing data right after shipment, and these values are calculated by qualification results.

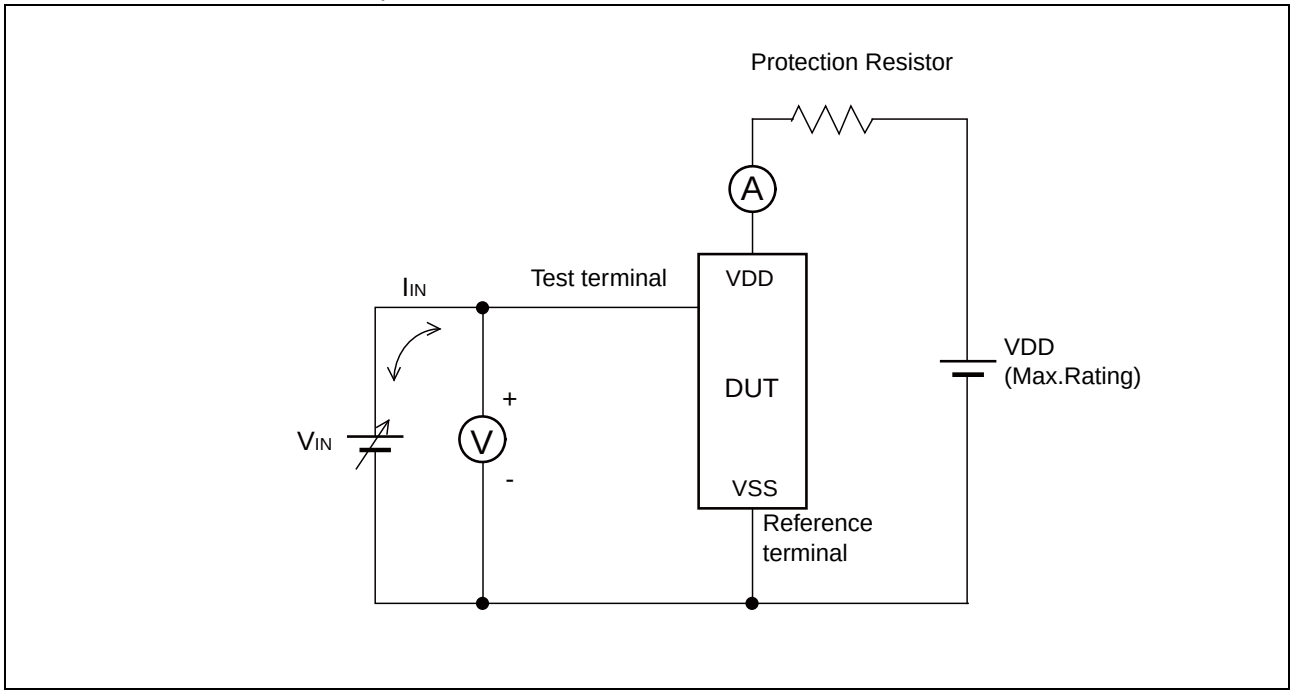
■ NOTES ON USE

Data written before performing IR reflow is not guaranteed after IR reflow.

■ ESD AND LATCH-UP

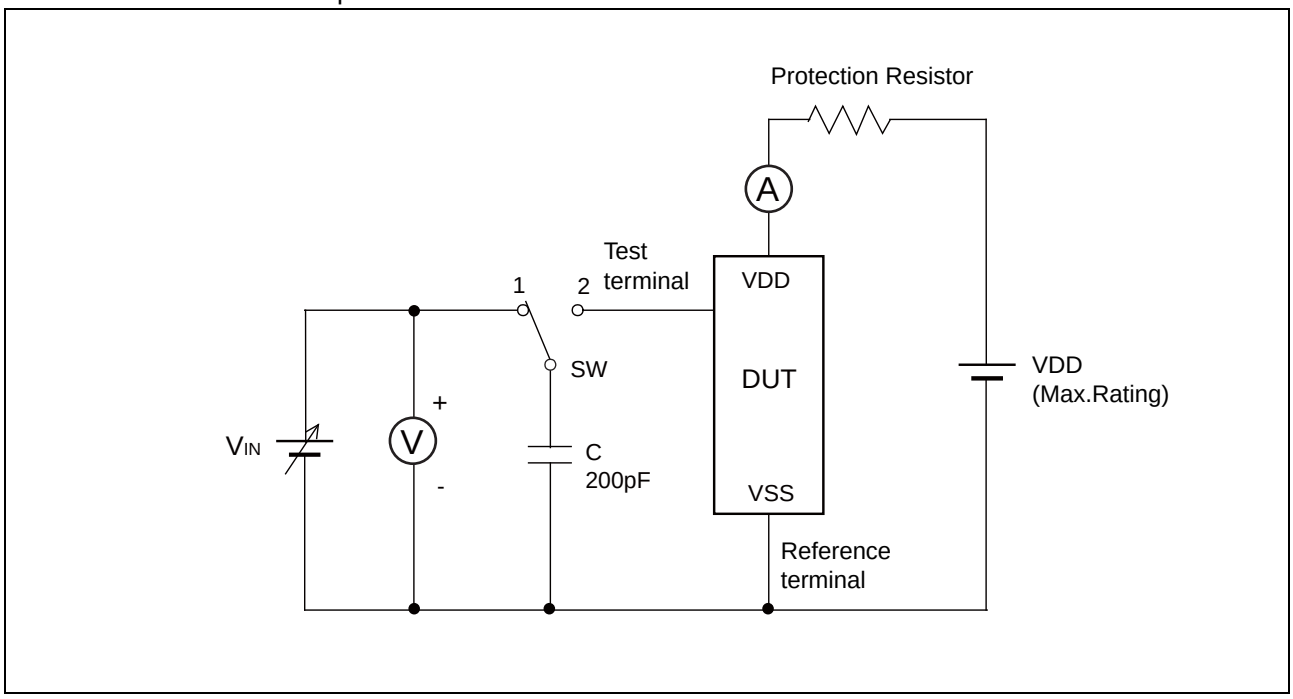
Test	DUT	Value
ESD HBM (Human Body Model) JESD22-A114 compliant	MB85R4002ANC-GE1	≥ |2000 V|
ESD MM (Machine Model) JESD22-A115 compliant		≥ |200 V|
ESD CDM (Charged Device Model) JESD22-C101 compliant		—
Latch-Up (I-test) JESD78 compliant		—
Latch-Up (V_{supply} overvoltage test) JESD78 compliant		—
Latch-Up (Current Method) Proprietary method		≥ |300 mA|
Latch-Up (C-V Method) Proprietary method		—

- Current method of Latch-Up Resistance Test



Note : The voltage V_{IN} is increased gradually and the current I_{IN} of 300 mA at maximum shall flow.
Confirm the latch up does not occur under $I_{IN} = \pm 300$ mA.
In case the specific requirement is specified for I/O and I_{IN} cannot be 300 mA, the voltage shall be increased to the level that meets the specific requirement.

• C-V method of Latch-Up Resistance Test

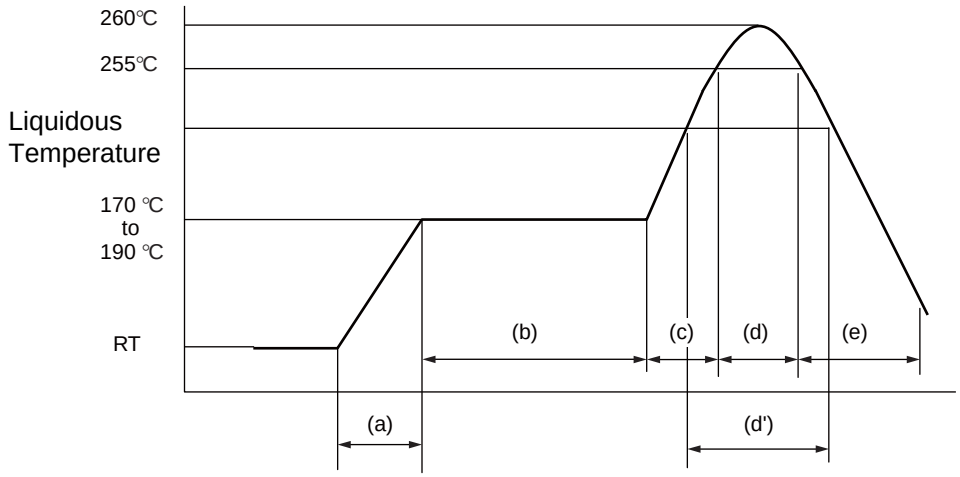


Note : Charge voltage alternately switching 1 and 2 approximately 2 sec interval. This switching process is considered as one cycle.
Repeat this process 5 times. However, if the latch-up condition occurs before completing 5 times, this test must be stopped immediately.

■ REFLOW CONDITIONS AND FLOOR LIFE

Item	Condition	
Method	IR (infrared reflow) , Convection	
Times	2	
Floor life	Before unpacking	Please use within 2 years after production.
	From unpacking to 2nd reflow	Within 8 days
	In case over period of floor life	Baking with 125 °C+/-3 °C for 24hrs+2hrs/-0hrs is required. Then please use within 8 days. (Please remember baking is up to 2 times)
Floor life condition	Between 5 °C and 30 °C and also below 70%RH required. (It is preferred lower humidity in the required temp range.)	

Reflow Profile



(a) Average ramp-up rate : 1 °C/s to 4 °C/s
(b) Preheat & Soak : 170 °C to 190 °C, 60 s to 180 s
(c) Average ramp-up rate : 1 °C/s to 4 °C/s
(d) Peak temperature : Temperature 260 °C Max; 255 °C within 10 s
(d') Liquidous temperature : Up to 230 °C within 40 s or
Up to 225 °C within 60 s or
Up to 220 °C within 80 s
(e) Cooling : Natural cooling or forced cooling

Note : Temperature on the top of the package body is measured.

■ RESTRICTED SUBSTANCES

This product complies with the regulations below (Based on current knowledge as of November 2011).

- EU RoHS Directive (2002/95/EC)
- China RoHS (Administration on the Control of Pollution Caused by Electronic Information Products (电子信息产品污染控制管理办法))
- Vietnam RoHS (30/2011/TT-BCT)

Restricted substances in each regulation are as follows.

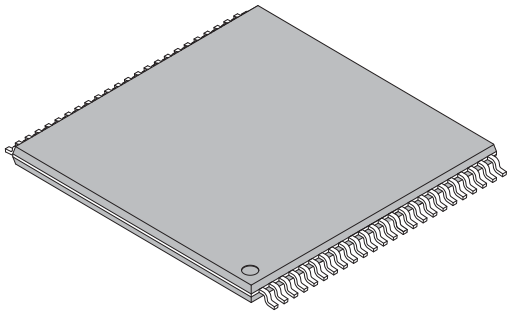
Substances	Threshold	Contain status*
Lead and its compounds	1,000 ppm	❍
Mercury and its compounds	1,000 ppm	❍
Cadmium and its compounds	100 ppm	❍
Hexavalent chromium compound	1,000 ppm	❍
Polybrominated biphenyls (PBB)	1,000 ppm	❍
Polybrominated diphenyl ethers (PBDE)	1,000 ppm	❍

* : The mark of "❍" shows below a threshold value.

■ ORDERING INFORMATION

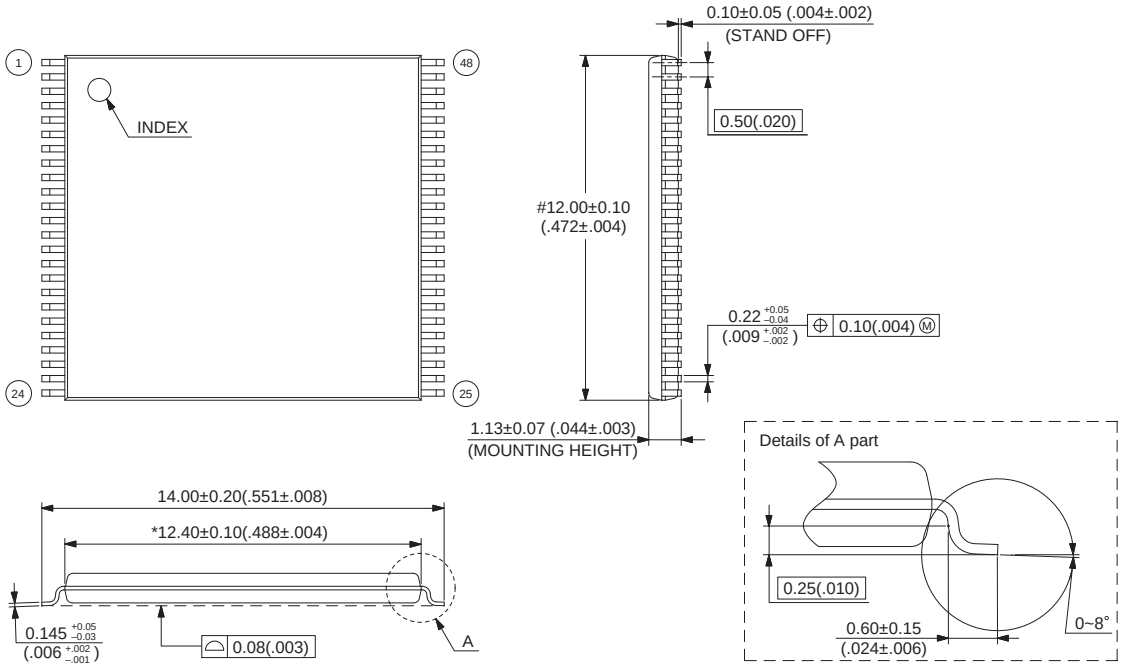
Part Number	Package	Shipping form	Minimum shipping quantity
MB85R4002ANC-GE1	48-pin plastic TSOP (FPT-48P-M48)	Tray	1

■ PACKAGE DIMENSIONS

48-pin plastic TSOP		
	Lead pitch	0.50 mm
	Package width × package length	12.00 mm × 12.40 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.20 mm MAX
	Weight	0.36 g
(FPT-48P-M48)		

48-pin plastic TSOP
(FPT-48P-M48)

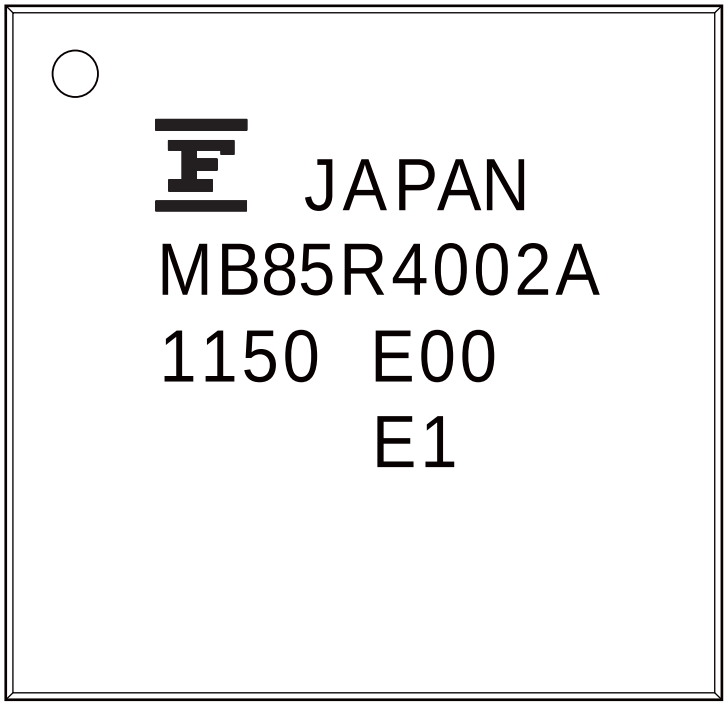
Note 1) # : Resin protrusion. (Each side : +0.15 (.006) Max).
Note 2) * : These dimensions do not include resin protrusion.
Note 3) Pins width and pins thickness include plating thickness.
Note 4) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

■ MARKING

[MB85R4002A-GE1]



[FPT-48P-M48]

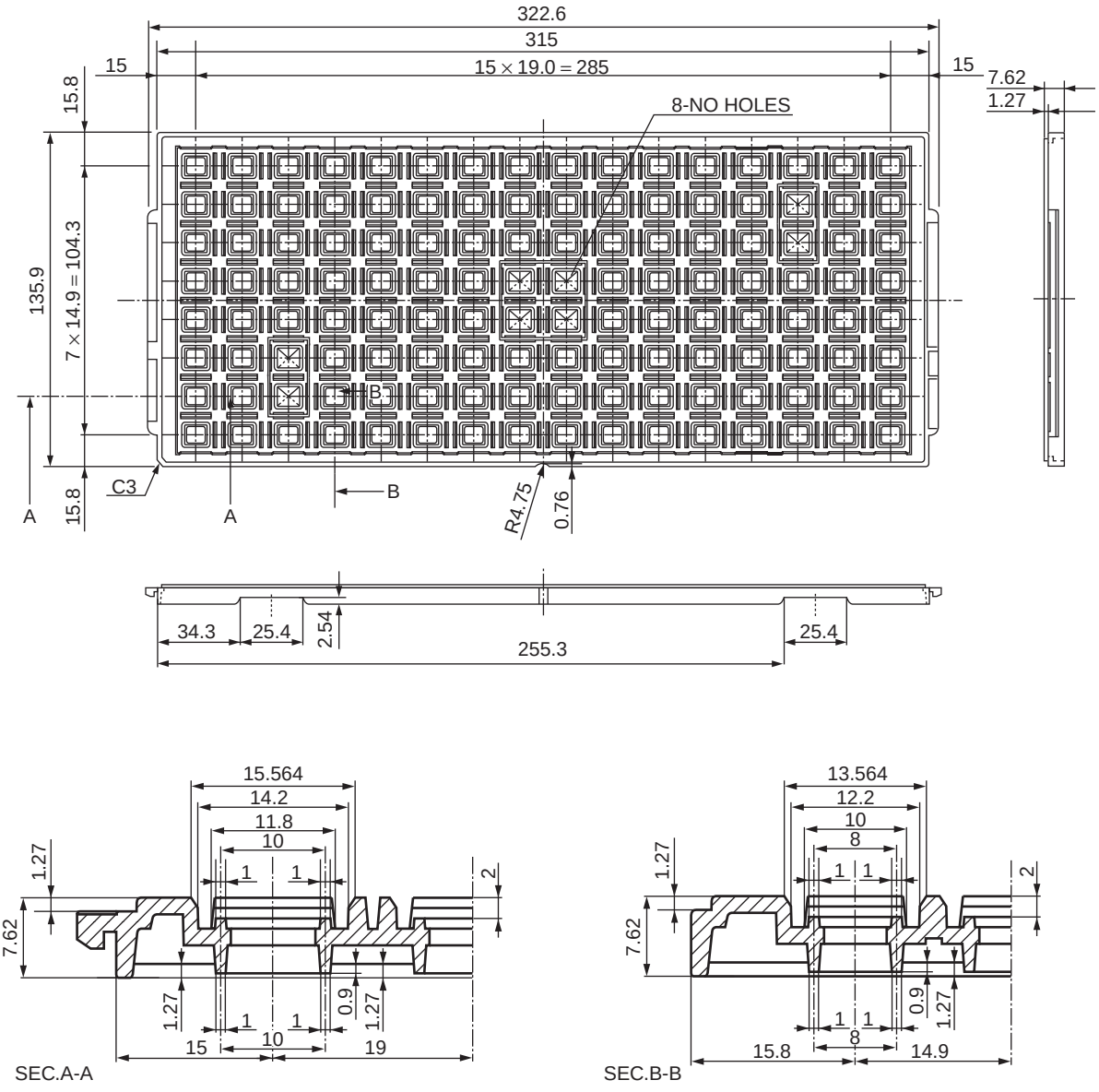
■ SHIPPING FORM

1. Tray

1.1 Tray Dimensions

TSOP48, 56 (I)

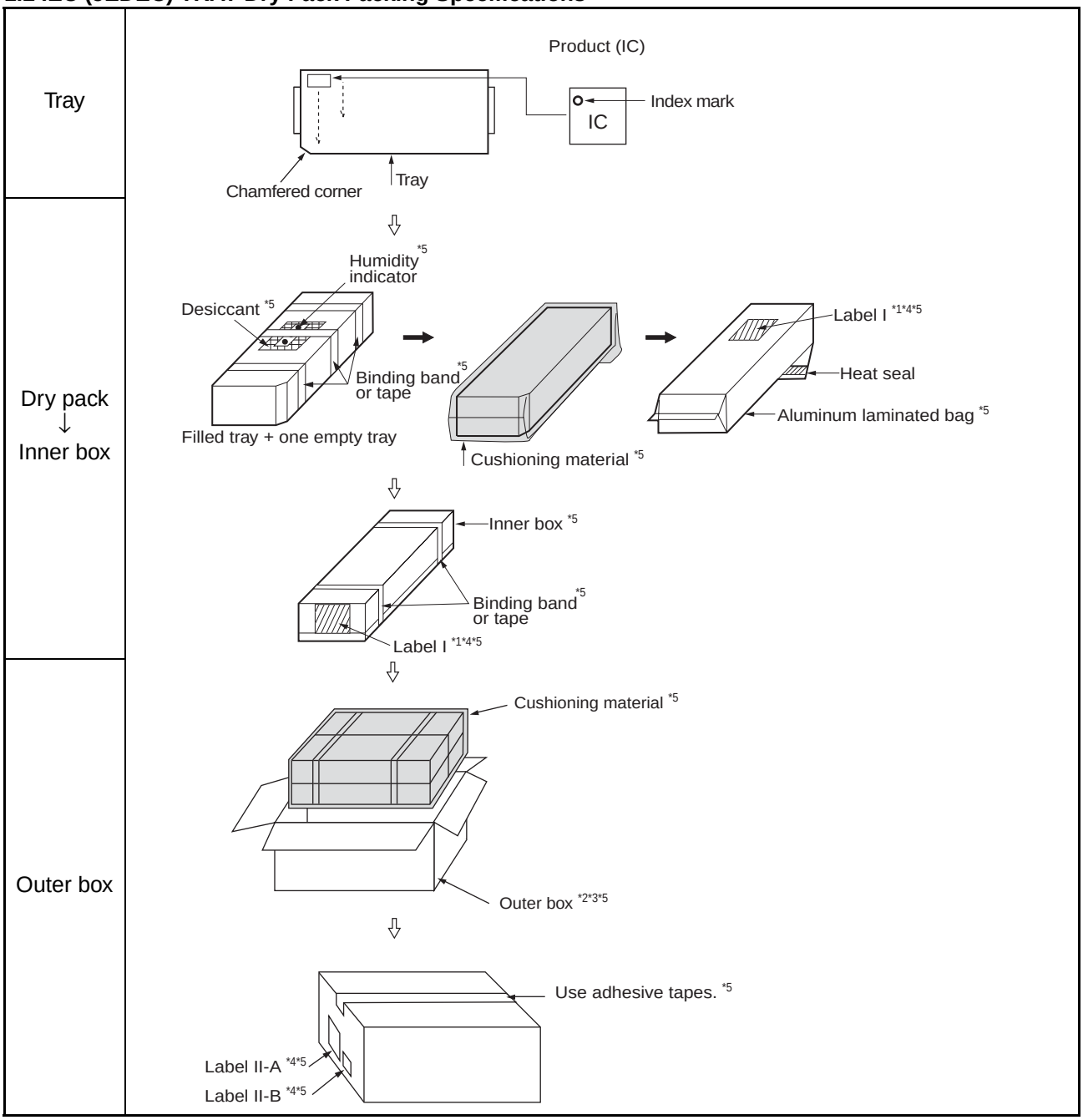
PKG code	Maximum storage capacity		
	pcs/tray	pcs/inner box	pcs/outer box
FPT-48P-M48	128	1280	5120



(Dimensions in mm)

Material : Conductive polyphenyleneether
Heat proof temperature : 125 °C MAX
Weight : 133 g

1.2 IEC (JEDEC) TRAY Dry Pack Packing Specifications



*1: For a product of witch part number is suffixed with "E1", a " G Pb " marks is display to the moisture barrier bag and the inner boxes.

*2: The size of the outer box may be changed depending on the quantity of inner boxes.

*3: The space in the outer box will be filled with empty inner boxes, or cushions, etc.

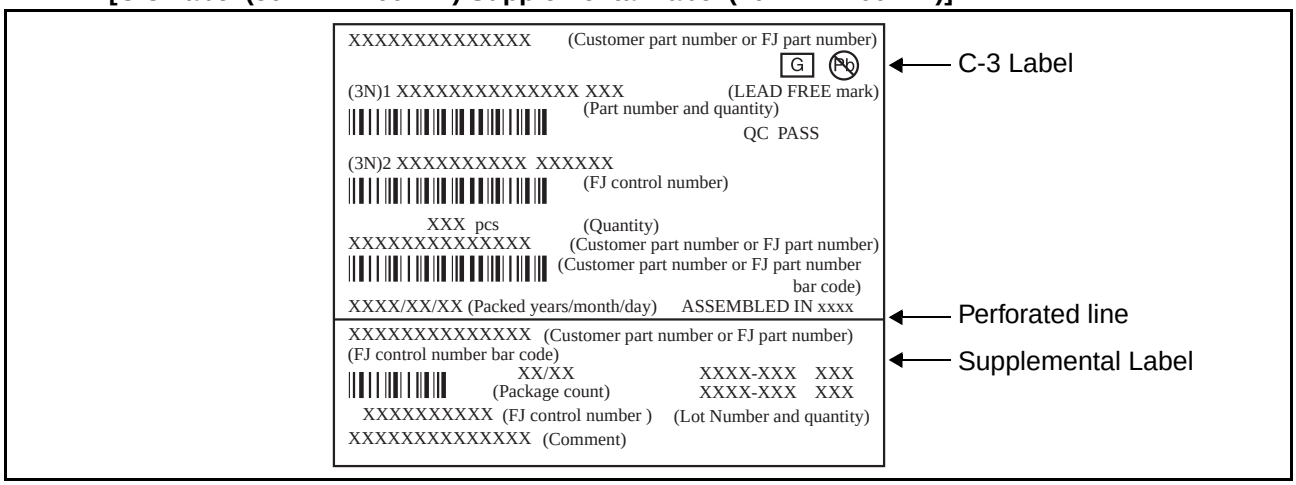
*4: Please refer to an attached sheet about the indication label.

*5: The packing materials except tray may differ slightly from the color and dimensions depend on country of manufacture.

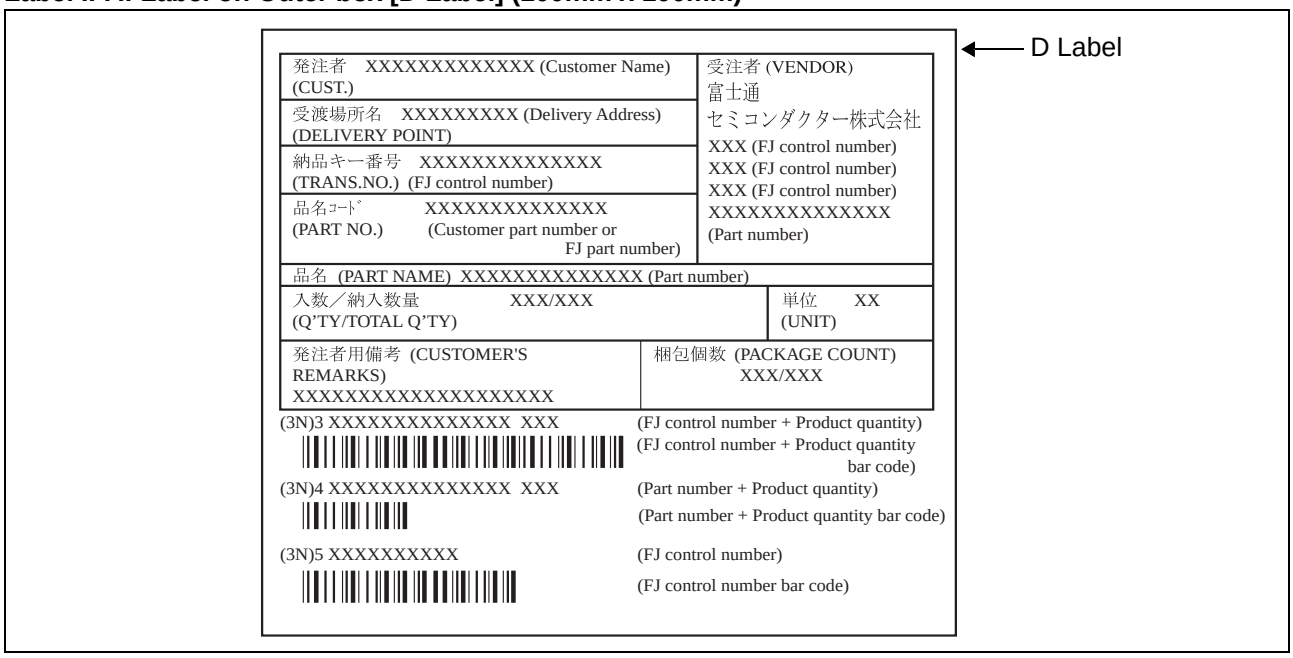
Note: The packing specifications may not be applied when the product is delivered via a distributer.

1.3 Product label indicators

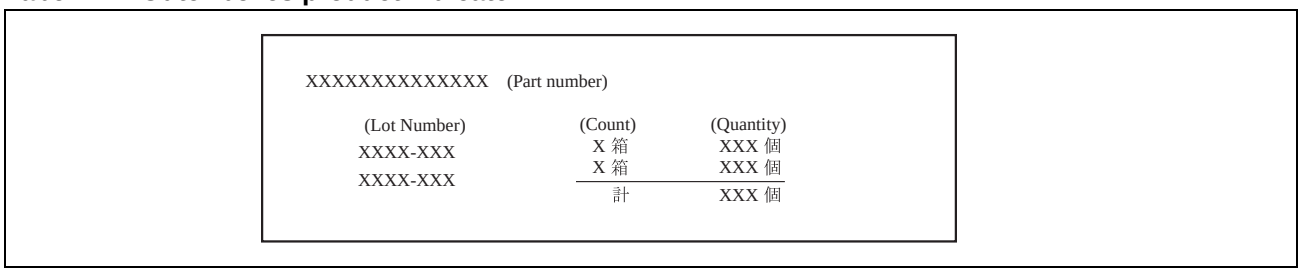
Label I: Label on Inner box/Moisture Barrier Bag/ (It sticks it on the reel for the emboss taping) [C-3 Label (50mm x 100mm) Supplemental Label (20mm x 100mm)]



Label II-A: Label on Outer box [D Label] (100mm x 100mm)



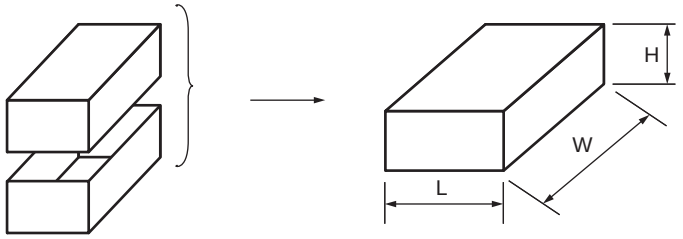
Label II-B: Outer boxes product indicate



Note: Depending on shipment state, "Label II-A" and "Label II-B" on the external boxes might not be printed.

1.4 Dimensions for Containers

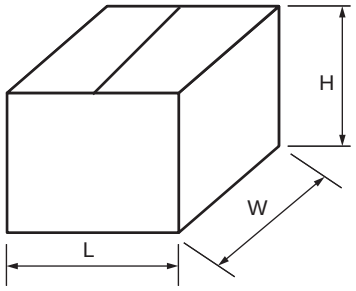
(1) Dimensions for inner box



L	W	H
165	360	75

(Dimensions in mm)

(2) Dimensions for outer box



L	W	H
355	385	195

(Dimensions in mm)

■ MAJOR CHANGES IN THIS EDITION

A change on a page is indicated by a vertical line drawn on the left side of that page.

Page	Section	Change Results
1	■ FEATURES	Revised the Data retention. 10 years (+ 55 °C) → 10 years (+ 55 °C), 55 years (+ 35 °C)
4	■ FUNCTIONAL TRUTH TABLE	Revised the table.
5	■ ABSOLUTE MAXIMUM RANGES	Revised the Storage Temperature. − 40 °C → + 55 °C
12	■ POWER ON/OFF SEQUENCE	Deleted the following description: “Because turning the power-on from an intermediate level cause malfunction, when the power is turned on, V_{DD} is required to be started from 0V (see the figure below).” Moved the following description under the table: “If the device does not operate within the specified conditions of read cycle, write cycle or power on/off sequence, memory data can not be guaranteed. In case the power is turned on or off, use the power supply reset IC and fix the CE2 to low level, to prevent unexpected writing. Use either of $\overline{CE}1$ or CE2, or both to disable control of the device.”
	■ FRAM CHARACTERISTICS	Revised the table and Note.

MEMO

MEMO

MEMO

FUJITSU SEMICONDUCTOR LIMITED

Nomura Fudosan Shin-yokohama Bldg. 10-23, Shin-yokohama 2-Chome,
Kohoku-ku Yokohama Kanagawa 222-0033, Japan
Tel: +81-45-415-5858
http://jp.fujitsu.com/fsl/en/

For further information please contact:

North and South America
FUJITSU SEMICONDUCTOR AMERICA, INC.
1250 E. Arques Avenue, M/S 333
Sunnyvale, CA 94085-5401, U.S.A.
Tel: +1-408-737-5600 Fax: +1-408-737-5999
http://us.fujitsu.com/micro/

Europe
FUJITSU SEMICONDUCTOR EUROPE GmbH
Pittlerstrasse 47, 63225 Langen, Germany
Tel: +49-6103-690-0 Fax: +49-6103-690-122
http://emea.fujitsu.com/semiconductor/

Korea
FUJITSU SEMICONDUCTOR KOREA LTD.
902 Kosmo Tower Building, 1002 Daechi-Dong,
Gangnam-Gu, Seoul 135-280, Republic of Korea
Tel: +82-2-3484-7100 Fax: +82-2-3484-7111
http://kr.fujitsu.com/fsk/

Asia Pacific
FUJITSU SEMICONDUCTOR ASIA PTE. LTD.
151 Lorong Chuan,
#05-08 New Tech Park 556741 Singapore
Tel : +65-6281-0770 Fax : +65-6281-0220
http://sg.fujitsu.com/semiconductor/

FUJITSU SEMICONDUCTOR SHANGHAI CO., LTD.
30F, Kerry Parkside, 1155 Fang Dian Road, Pudong District,
Shanghai 201204, China
Tel : +86-21-6146-3688 Fax : +86-21-6146-3660
http://cn.fujitsu.com/fss/

FUJITSU SEMICONDUCTOR PACIFIC ASIA LTD.
2/F, Green 18 Building, Hong Kong Science Park,
Shatin, N.T., Hong Kong
Tel : +852-2736-3232 Fax : +852-2314-4207
http://cn.fujitsu.com/fsp/

Edited: Sales Promotion Department