Product Flyer

Mixed Signal Division

MB86064

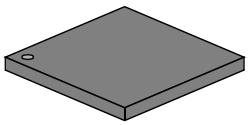
October 2004
Version 1.1

FME/MS/DAC80/FL/5085

Dual 14-bit 1GSa/s DAC

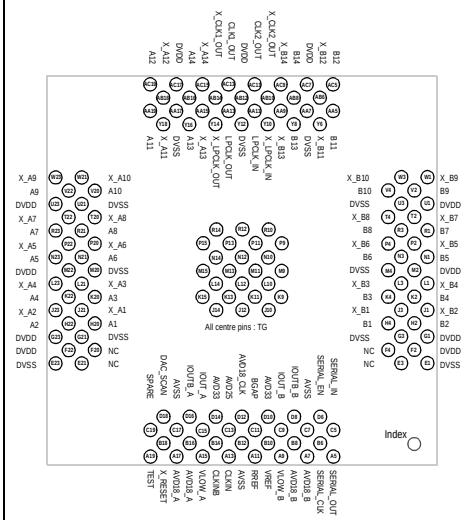
The Fujitsu MB86064 is a Dual 14-bit 1GSa/s digital to analog converter (DAC), delivering exceptional dynamic performance. Each high performance DAC core is capable of generating multi-standard, multi-carrier communication transmit signals, suitable for 2, 2.5 and 3G systems. DAC data is input via two high-speed LVDS ports. These operate in a pseudo double data rate (DDR) mode, with data latched on both rising and falling edges. Alternatively, the device can be configured as a multiplexed dual-port single DAC. To simplify system integration the DAC operates from a clock running at half the DAC conversion rate.

PLASTIC PACKAGE
EFBGA-120



Package Dimensions
12 mm x 12 mm

PIN ASSIGNMENT



Not to scale. Viewed from above.

Features

- Dual 14-bit, 1GSa/s Digital to Analog conversion
- Exceptional dynamic performance
  - 74dBc ACLR for 4 UMTS carriers @ 276MHz direct-IF
- 100MHz image-free generated bandwidth capability
  - supports UMTS plus digital pre-distortion bandwidth
- Proprietary performance enhancement features
- LVDS data interface
- Register selectable on-chip LVDS termination resistors
- Fujitsu 4-wire serial control interface
- Two 16k point programmable on-chip waveform memories
- Low power 3.3V analog and 1.8V digital operation
- 750mW per DAC power dissipation at 1GSa/s
- 0.18µm CMOS technology with Triple Well
- Performance enhanced EFBGA package
- Industrial temperature range (-40°C to +85°C)

Applications

- Multi-carrier, Multi-standard cellular infrastructure
  - CDMA, W-CDMA, GSM/EDGE, UMTS
- Wideband communications systems
- High Direct-IF architectures
- Arbitrary waveform generation
- Test equipment
- Radar, video & display systems

Functional Overview

The MB86064 is a high performance Dual 14-bit 1GSa/s DAC. In addition to two DAC cores the device features a host of features designed to help both system integration and operation. A functional block diagram is shown in Figure 1. Analog performance at high frequencies is enhanced by novel current switch and switch driver designs which provide constant data-independent switching delay, reducing jitter and distortion.

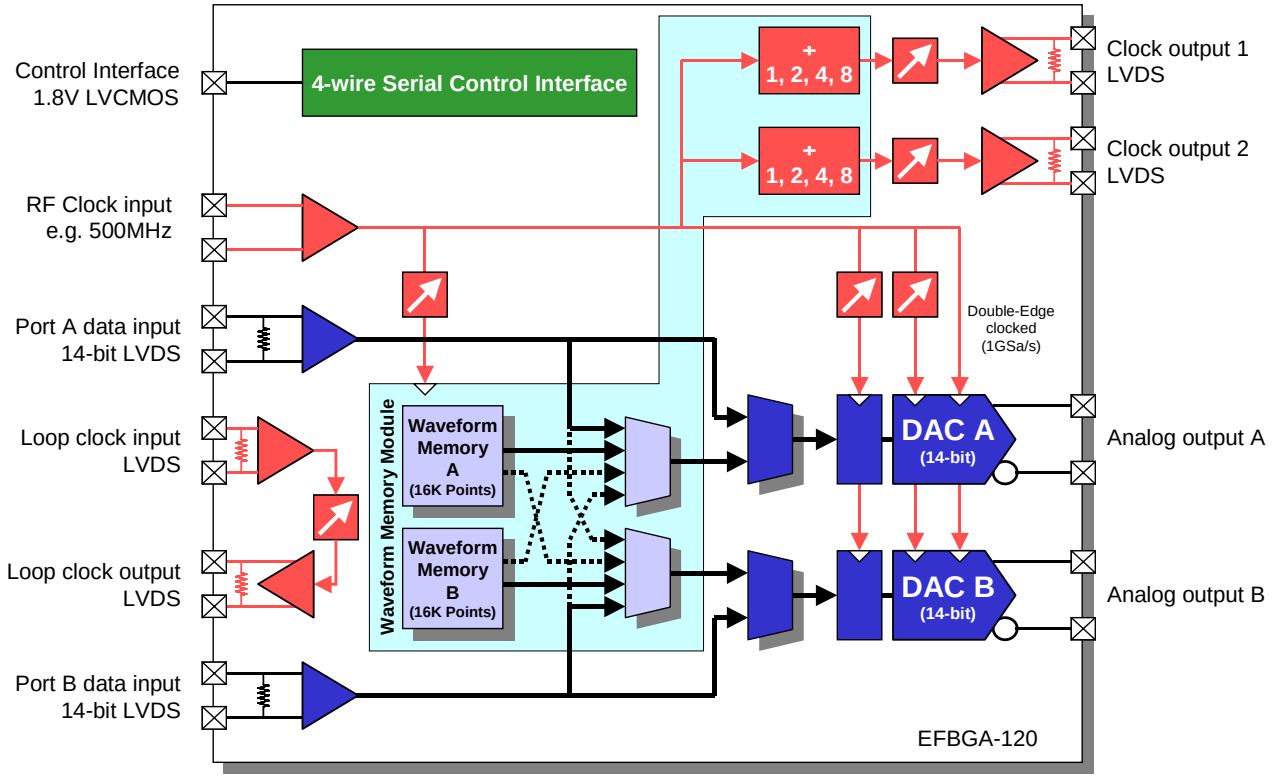


Figure 1 MB86064 Functional Block Diagram

The device requires an input clock at half the DAC conversion rate as each DAC core is clocked on both edges of the input clock. Each DAC core can be regarded as two interleaved DACs, each running at half rate. The main reason for adopting this approach is that the switch driver inherently includes a multiplex function through its two input ports. Compared to a conventional switch driver this allows twice as long to acquire and convert, though because the two paths share current sources they match exactly at low frequencies. A characteristic of this architecture is a suppressed image appearing reflected about Fs(dac)/4 of Fclk-Fsig. Duty cycle error in the input clock will exacerbate this image, but can be minimised by trimming the differential DC offset at the clock input pins.

The big advantage of this approach compared to a single DAC running at half the rate is much reduced sinx/x roll off, which gives increased output power and better in-band flatness when generating high output frequencies (e.g. 200MHz and above). This is illustrated in Figure 2 as line 1. An alternative approach using a return-to-zero output stage has the same sinx/x roll off (and switch driver speed) but 6dB lower output power and a large image at Fclk-Fout. See Line 2.

Line 3 illustrates a conventional DAC running at half rate.

Input Data

Unsigned binary data to each DAC core is input via a dedicated parallel LVDS port. As with the DAC core, data is latched on every rising and falling edge of the clock in a pseudo DDR mode. For synchronisation of data generator(s) two LVDS clock outputs and a Loop-Clock facility are provided.

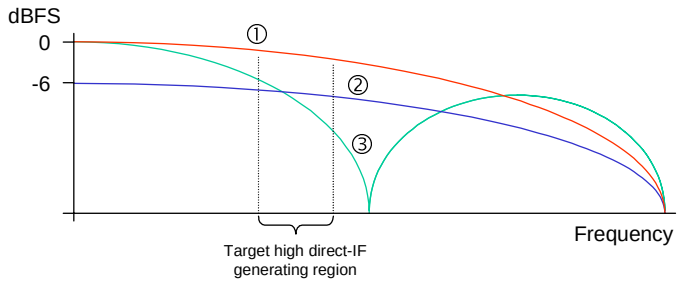


Figure 2 Benefits of DAC core architecture to Sinx/x response

Loop-Clock

Maintaining valid clock-to-data timing becomes increasingly difficult at higher clock rates, particularly taking into account device-to-device variations. The MB86064 minimises potential problems through its DDR data interface and by providing a loop-clock facility. The on-chip 'loop' consists of an LVDS input connected to an LVDS output, through a programmable delay stage. This loop-through, and the associated tracking from the data generating device, should be incorporated in the feedback loop of a Delay-Locked Loop (DLL) or Phase-Locked Loop (PLL) clock generator, within the data generating device. This enables the system to compensate for variations in input/output delays in both the data generating device and the DAC.

Performance Enhancement Features

Each DAC core integrates a number of performance enhancing features. Performance levels now reach the level sought after for next generation systems and high direct-IF architectures.

Serial Control Interface

A Fujitsu 4-wire serial interface is provided for configuration and control of the DAC. Programmed data is stored in a number of read/writable registers.

Waveform Memory Module

The MB86064 incorporates a Waveform Memory Module featuring two 16k point on-chip waveform memories. These allow the DAC cores to be driven with user programmed waveforms without the need for external high speed, pattern generators.

Development Kit

A comprehensive Development Kit (DK), DK86064, is available which comprises a number of modules. A base motherboard provides an interface to the DAC, Clock and Data modules. Also included is a PC USB Interface Lead & Control Software.

For further details, please refer to the associated documentation.

Worldwide Headquarters

Japan

Tel: +81 44 754 3753
Fax: +81 44 754 3329

Fujitsu Limited
Kamikodanaka 4-1-1
Nakahara-ku
Kawasaki-shi
Kanagawa-ken 211-8588
Japan

http://www.fujitsu.com

Asia

Tel: +65 281 0770
Fax: +65 281 0220

Fujitsu Microelectronics Asia Pte Ltd
151 Lorong Chauan
New Tech Park
#05-08
Singapore 556741

http://www.fmal.fujitsu.com

USA

Tel: +1 408 737 5600
Fax: +1 408 737 5999

Fujitsu Microelectronics America, Inc.
1250 E. Arques Avenue, M/S 333
Sunnyvale, CA 94088-3470
USA

Tel: +1 800 866 8608
Fax: +1 408 737 5984

Customer Response Center
Mon-Fri: 7am-5pm (PST)

http://www.fma.fujitsu.com/

Europe

Tel: +49 6103 6900
Fax: +49 6103 690122

Fujitsu Microelectronics Europe GmbH
Am Siebenstein 6-10
D-63303 Dreieich-Buchschlag
Germany

http://www.fme.fujitsu.com/