FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-22001-1E

ASSP Communication Control

IEEE 1394 Bus Controller (for MPEG, DVC)

MB86612

■ DESCRIPTION

The MB86612 is 1394 serial bus controller exclusively for MPEG and DVC data transfer, compatible with the IEEE 1394 “FireWire” standard (IEEE Standard 1394-1995). Two built-in ports plus a differential transceiver and comparator are provided to enable formation of networks in a 1394 cable environment. The MB86612 supports s100 data transfer speeds.

By integrating the physical layer and link layer on one chip, The MB86612 is designed to reduce mounting area as well as power consumption.

The MB86612 has an exclusive data port for isochronous transfer, provides automatic packetizing and separation of header and data units, and is optimized for continuity of transfer processing.

The MB86612 supports MPEG and DVC AV/C protocols, and includes the necessary built-in automatic operations and CSR’s for providing the necessary operations for MPEG and DVC data transfer.

■ FEATURES

- Compatible with IEEE 1394 high-performance serial bus standards
- Physical layer and link layer integrated on one chip
- 2 cable ports
- Supports s100 transfer speed (98.304 Mbit/sec)
- 3.3V single power supply operation
- Built-in PLL (for crystal oscillator) for internal clock signal generation
- Power saving modes
  1) Forced sleep mode at instruction from MPU
  2) Automatic sleep mode for non-connected ports
- Header and data units automatically separated at receiving and automatic packetizing for sending
- Supports cycle master functions

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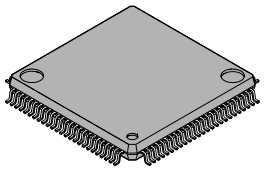
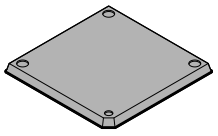
■ PACKAGES

100-pin plastic LQFP



(FPT-100P-M05)

120-pin plastic FBGA



(BGA-120P-M01)

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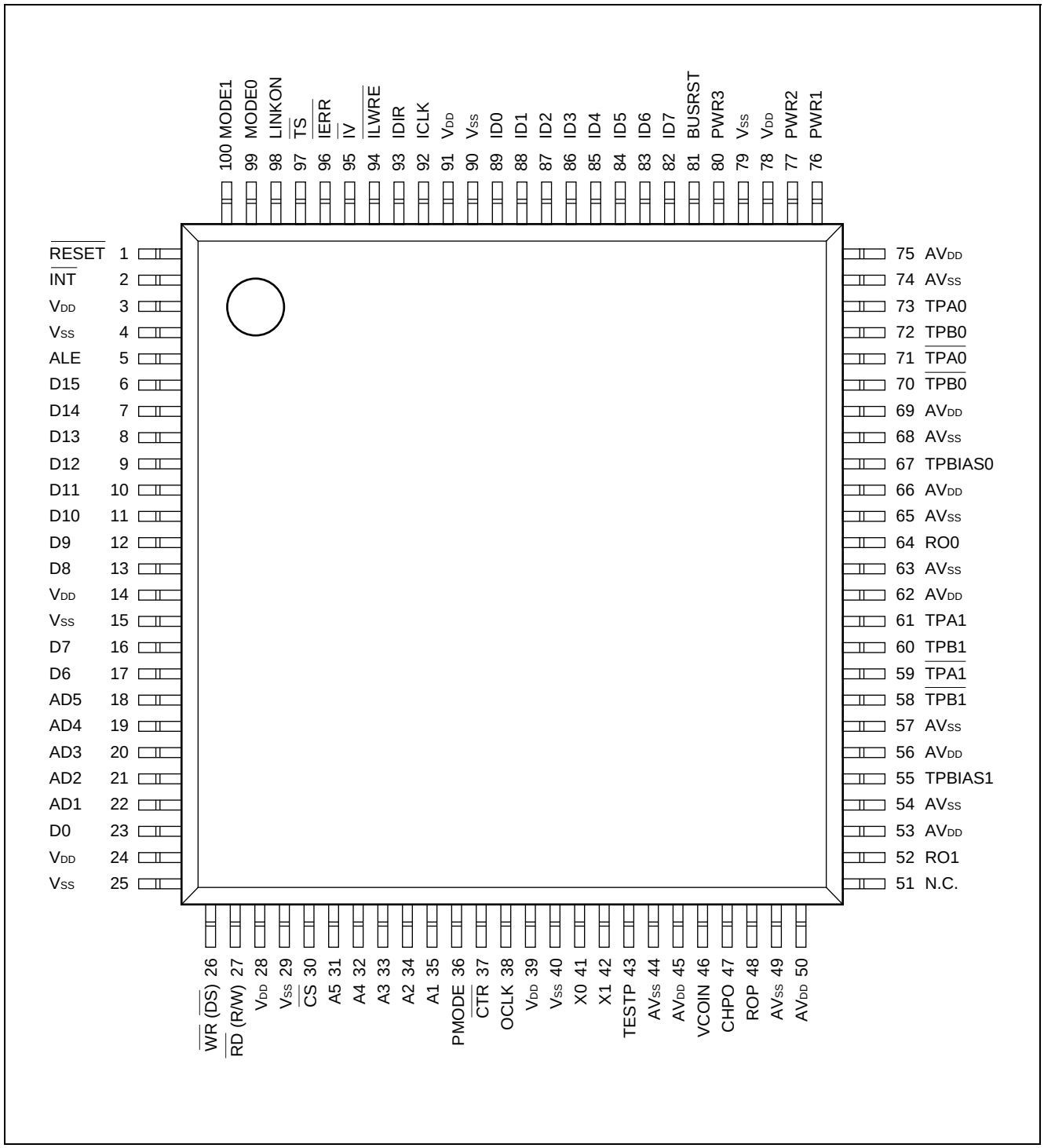
- Built-in CSR's to provide isochronous resource manager functions
- 32-bit CRC generation and check functions
- General purpose port for asynchronous transfer and control (16-bit MPU bus)
- Exclusive built-in ports for isochronous transfer (8-bit bus)
- Built-in CRS's and automatic processes to support AV/C protocol (MPEG, DVC)
  1) Automatic separation of CIP headers at receiving, and automatic packetizing at sending.
  2) Automatic generation of source packet headers (time stamp).
  3) Source packet header (time stamp) match detection
  4) DBC area automatic increment function
  5) Empty packet sending and receiving
  6) On-chip PCR (input/output 1 channel each)
  7) Each CSR with automatic C&S lock processing and read processing
  8) Automatic processing of late packet generation
- Compatible with 4-core or 6-core cables
- Packages: LQFP-100, FBGA-120

■ PIN ASSIGNMENTS

1. LQFP-100



2. FBGA-120

13	12	11	10	9	8	7	6	5	4	3	2	1	
N.C.	AV_{DD}	AV_{SS}	VCOIN	TESTP	XO	OCLK	PMODE	A3	A5	V_{DD}	N.C.	$\overline{WR}$ ($\overline{DS}$)	N
N.C.	RO1	N.C.	CHPO	AV_{SS}	X1	V_{DD}	$\overline{CTR}$	A2	A4	V_{SS}	$\overline{RD}$ (R/W)	V_{SS}	M
AV_{DD}	AV_{SS}	TP-BIAS1	ROP	AV_{DD}	N.C.	V_{SS}	N.C.	A1	N.C.	$\overline{CS}$	N.C.	V_{DD}	L
AV_{SS}	AV_{SS}	$\overline{TPB1}$								D0	AD1	AD2	K
$\overline{TPA1}$	TPB1	N.C.								AD3	AD4	AD5	J
TPA1	AV_{DD}	AV_{SS}								D6	N.C.	D7	I
N.C.	RO0	AV_{SS}			TOP VIEW					V_{SS}	V_{DD}	D8	H
AV_{DD}	TP-BIAS0	N.C.								N.C.	D9	D10	G
AV_{SS}	AV_{DD}	$\overline{TPB0}$								D11	D12	N.C.	E
$\overline{TPA0}$	TPB0	N.C.								D13	D14	D15	D
TPA0	AV_{SS}	PWR3	ID7	ID4	ID1	V_{SS}	IDIR	$\overline{IV}$	LINKON	ALE	V_{SS}	V_{DD}	C
AV_{DD}	PWR2	V_{SS}	N.C.	ID5	ID2	ID0	ICLK	N.C.	$\overline{TS}$	N.C.	$\overline{INT}$	N.C.	B
PWR1	N.C.	V_{DD}	BUSRST	ID6	ID3	N.C.	V_{DD}	$\overline{ILWRE}$	$\overline{IERR}$	MODE0	MODE1	$\overline{RESET}$	A

△
1 pin

■ PIN LIST

1. LQFP-100

NO.	I/O	Pin Name	NO.	I/O	Pin Name
1	ID	$\overline{\text{RESET}}$	36	IU	PMODE
2	O	$\overline{\text{INT}}$	37	O	$\overline{\text{CTR}}$
3	—	V_{DD}	38	O	OCLK
4	—	V_{SS}	39	—	V_{DD}
5	ID	ALE	40	—	V_{SS}
6	ID/O	D15	41	I/O	X0
7	ID/O	D14	42	I	X1
8	ID/O	D13	43	—	TESTP
9	ID/O	D12	44	—	AV_{SS}
10	ID/O	D11	45	—	AV_{DD}
11	ID/O	D10	46	I	VCOIN
12	ID/O	D9	47	O	CHPO
13	ID/O	D8	48	O	ROP
14	—	V_{DD}	49	—	AV_{SS}
15	—	V_{SS}	50	—	AV_{DD}
16	ID/O	D7	51	—	N.C.
17	ID/O	D6	52	O	RO1
18	ID/O	AD5	53	—	AV_{DD}
19	ID/O	AD4	54	—	AV_{SS}
20	ID/O	AD3	55	O	TPBIAS1
21	ID/O	AD2	56	—	AV_{DD}
22	ID/O	AD1	57	—	AV_{SS}
23	ID/O	D0	58	I/O	$\overline{\text{TPB1}}$
24	—	V_{DD}	59	I/O	$\overline{\text{TPA1}}$
25	—	V_{SS}	60	I/O	TPB1
26	ID	$\overline{\text{WR}}$ ($\overline{\text{DS}}$)	61	I/O	TPA1
27	ID	$\overline{\text{RD}}$ (R/W)	62	—	AV_{DD}
28	—	V_{DD}	63	—	AV_{SS}
29	—	V_{SS}	64	O	RO0
30	ID	$\overline{\text{CS}}$	65	—	AV_{SS}
31	ID	A5	66	—	AV_{DD}
32	ID	A4	67	O	TPBIAS0
33	ID	A3	68	—	AV_{SS}
34	ID	A2	69	—	AV_{DD}
35	ID	A1	70	I/O	$\overline{\text{TPB0}}$

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NO.	I/O	Pin Name	NO.	I/O	Pin Name
71	I/O	$\overline{\text{TPA0}}$	86	ID/O	ID3
72	I/O	TPB0	87	ID/O	ID2
73	I/O	TPA0	88	ID/O	ID1
74	—	AV_{SS}	89	ID/O	ID0
75	—	AV_{DD}	90	—	V_{SS}
76	I	PWR1	91	—	V_{DD}
77	I	PWR2	92	ID	ICLK
78	—	V_{DD}	93	ID	IDIR
79	—	V_{SS}	94	O	$\overline{\text{ILWRE}}$
80	I	PWR3	95	ID	$\overline{\text{IV}}$
81	I	BUSRST	96	O	$\overline{\text{IERR}}$
82	ID/O	ID7	97	ID/O	$\overline{\text{TS}}$
83	ID/O	ID6	98	O	LINKON
84	ID/O	ID5	99	ID	MODE0
85	ID/O	ID4	100	ID	MODE1

2. FBGA-120

Pin No.	Ball No.	I/O	Pin Name	Pin No.	Ball No.	I/O	Pin Name	Pin No.	Ball No.	I/O	Pin Name
1	A1	ID	$\overline{\text{RESET}}$	37	N4	ID	A5	73	H13	I/O	TPA1
2	B1	—	N.C.	38	M4	ID	A4	74	H12	—	AV_{DD}
3	B2	O	$\overline{\text{INT}}$	39	L4	—	N.C.	75	H11	—	AV_{SS}
4	C1	—	V_{DD}	40	N5	ID	A3	76	G13	—	N.C.
5	C2	—	V_{SS}	41	M5	ID	A2	77	G12	—	RO0
6	C3	ID	ALE	42	L5	ID	A1	78	G11	—	AV_{SS}
7	D1	ID/O	D15	43	N6	IU	PMODE	79	F13	—	AV_{DD}
8	D2	ID/O	D14	44	M6	O	$\overline{\text{CTR}}$	80	F12	—	TPBIAS0
9	D3	ID/O	D13	45	L6	—	N.C.	81	F11	—	N.C.
10	E1	—	N.C.	46	N7	O	OCLK	82	E13	—	AV_{SS}
11	E2	ID/O	D12	47	M7	—	V_{DD}	83	E12	—	AV_{DD}
12	E3	ID/O	D11	48	L7	—	V_{SS}	84	E11	I/O	$\overline{\text{TPB0}}$
13	F1	ID/O	D10	49	N8	I/O	X0	85	D13	I/O	$\overline{\text{TPA0}}$
14	F2	ID/O	D9	50	M8	I	X1	86	D12	I/O	TPB0
15	F3	—	N.C.	51	L8	—	N.C.	87	D11	—	N.C.
16	G1	ID/O	D8	52	N9	O	TESTP	88	C13	I/O	TPA0
17	G2	—	V_{DD}	53	M9	—	AV_{SS}	89	C12	—	AV_{SS}
18	G3	—	V_{SS}	54	L9	—	AV_{DD}	90	B13	—	AV_{DD}
19	H1	ID/O	D7	55	N10	I	VCOIN	91	A13	I	PWR1
20	H2	—	N.C.	56	M10	O	CHPO	92	A12	—	N.C.
21	H3	ID/O	D6	57	L10	O	ROP	93	B12	I	PWR2
22	J1	ID/O	AD5	58	N11	—	AV_{SS}	94	A11	—	V_{DD}
23	J2	ID/O	AD4	59	M11	—	N.C.	95	B11	—	V_{SS}
24	J3	ID/O	AD3	60	N12	—	AV_{DD}	96	C11	I	PWR3
25	K1	ID/O	AD2	61	N13	—	N.C.	97	A10	I	BUSRST
26	K2	ID/O	AD1	62	M13	—	N.C.	98	B10	—	N.C.
27	K3	ID/O	D0	63	M12	O	RO1	99	C10	ID/O	ID7
28	L1	—	V_{DD}	64	L13	—	AV_{DD}	100	A9	ID/O	ID6
29	L2	—	N.C.	65	L12	—	AV_{SS}	101	B9	ID/O	ID5
30	M1	—	V_{SS}	66	L11	O	TPBIAS1	102	C9	ID/O	ID4
31	N1	ID	$\overline{\text{WR}}$ ($\overline{\text{DS}}$)	67	K13	—	AV_{DD}	103	A8	ID/O	ID3
32	N2	—	N.C.	68	K12	—	AV_{SS}	104	B8	ID/O	ID2
33	M2	ID	$\overline{\text{RD}}$ (R/W)	69	K11	I/O	$\overline{\text{TPB1}}$	105	C8	ID/O	ID1
34	N3	—	V_{DD}	70	J13	I/O	$\overline{\text{TPA1}}$	106	A7	—	N.C.
35	M3	—	V_{SS}	71	J12	I/O	TPB1	107	B7	ID/O	ID0
36	L3	ID	$\overline{\text{CS}}$	72	J11	—	N.C.	108	C7	—	V_{SS}

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Pin No.	Ball No.	I/O	Pin Name	Pin No.	Ball No.	I/O	Pin Name	Pin No.	Ball No.	I/O	Pin Name
109	A6	—	V_{DD}	113	B5	—	N.C.	117	C4	O	LINKON
110	B6	ID	ICLK	114	C5	ID	$\overline{IV}$	118	A3	ID	MODE0
111	C6	ID	IDIR	115	A4	O	$\overline{IERR}$	119	B3	—	N.C.
112	A5	O	$\overline{ILWRE}$	116	B4	ID/O	$\overline{TS}$	120	A2	ID	MODE1

■ PIN DESCRIPTION

1. 1394 Interface

Pin name	I/O	Function
TPA0	I/O	Cable port 0 TPA positive signal I/O pin
$\overline{\text{TPA0}}$	I/O	Cable port 0 TPA negative signal I/O pin
TPB0	I/O	Cable port 0 TPB positive signal I/O pin
$\overline{\text{TPB0}}$	I/O	Cable port 0 TPB negative signal I/O pin
TPA1	I/O	Cable port 1 TPA positive signal I/O pin
$\overline{\text{TPA1}}$	I/O	Cable port 1 TPA negative signal I/O pin
TPB1	I/O	Cable port 1 TPB positive signal I/O pin
$\overline{\text{TPB1}}$	I/O	Cable port 1 TPB negative signal I/O pin
TPBIAS0	O	Cable port 0 common voltage reference voltage output pin
TPBIAS1	O	Cable port 1 common voltage reference voltage output pin
RO0	O	Connect to GND through 4.7 kΩ resistance
RO1	O	Connect to GND through 4.7 kΩ resistance

2. Isochronous-data Interface

Pin name	I/O	Function
ICLK	I	Isochronous data interface CLK signal input pin (DC to 16 MHz). Note: When this clock is stopped, transfer is stopped. Also the “Data FIFO init (63h)” instruction (operand: 21) is invalid.
IDIR	I	Isochronous transfer sending/receiving switching signal input pin. 0 input: Clear ISO FIFO, go to sending mode. Sending starts after receiving 1 packet of data. 1 input: Clear ISO FIFO, go to receiving mode. If a ‘1’ signal is entered during packet sending, receiving mode begins after sending of the current packet. The $\overline{\text{ILWRE}}$ signal is asserted after receiving 1 packet. Note: This signal should normally be left at ‘1’, and switched to ‘0’ only when sending.
$\overline{\text{ILWRE}}$	O	Isochronous FIFE access enable signal output pin. Sending: Asserted when 1 or more empty source packets are present in ISO FIFO. When negated, the data output up to the leading edge for the next ICLX. Receiving: Asserted when receiving of 1 source packet of data is completed. Negate conditions for this signal are determined by the ilwre-mode bit (bit 11) in the mode-control register.
ID7 to ID0	I/O	Isochronous transfer data input/output bits. (MSB is ID7, LSB is ID0)
$\overline{\text{IV}}$	I	ID7 to ID0 enable signal input pin. Sending: While this signal is active, data from the ID7 to ID0 pins is loaded into ISO FIFO memory at the rising edge of the ICLK signal. Receiving: While this signal is active, data from ISO FIFO memory is sent to the ID7 to ID0 pins. Data is switched at the falling edge of the ICLK signal.

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Pin name	I/O	Function
$\overline{TS}$	I/O	Sending: DVC mode time stamp trigger signal input pin. (Input) The cycle timer value when this signal is asserted is added to the sending offset value and becomes the sending time stamp. Receiving: Time stamp match detect signal. (output) In MPEG mode, this signal is negative after reading 1 source packet of data. In DVC mode, this signal is asserted for the duration of 32 ticlk (32 periods of the ICLK signal). If an error is detected in a receiving isochronous packet this signal is not output.
IERR	O	This signal is output when an error is detected in a receiving isochronous packet. When an error is detected the $\overline{TS}$ signal is not output, so that this signal should be used to trigger reading of the receiving packet. If an error such as causing discarding of received packets within a device, this signal is not output.
$\overline{CTR}$	O	This signal is output when the cycle timer value is changed. This signal may be output or not output, according to the CTR bit (bit 0) in the mode-control register.
OCLK	O	Cycle timer clock output (24.576 MHz). This signal may be output or not output, according to the CTR bit (bit 0) in the mode-control register.

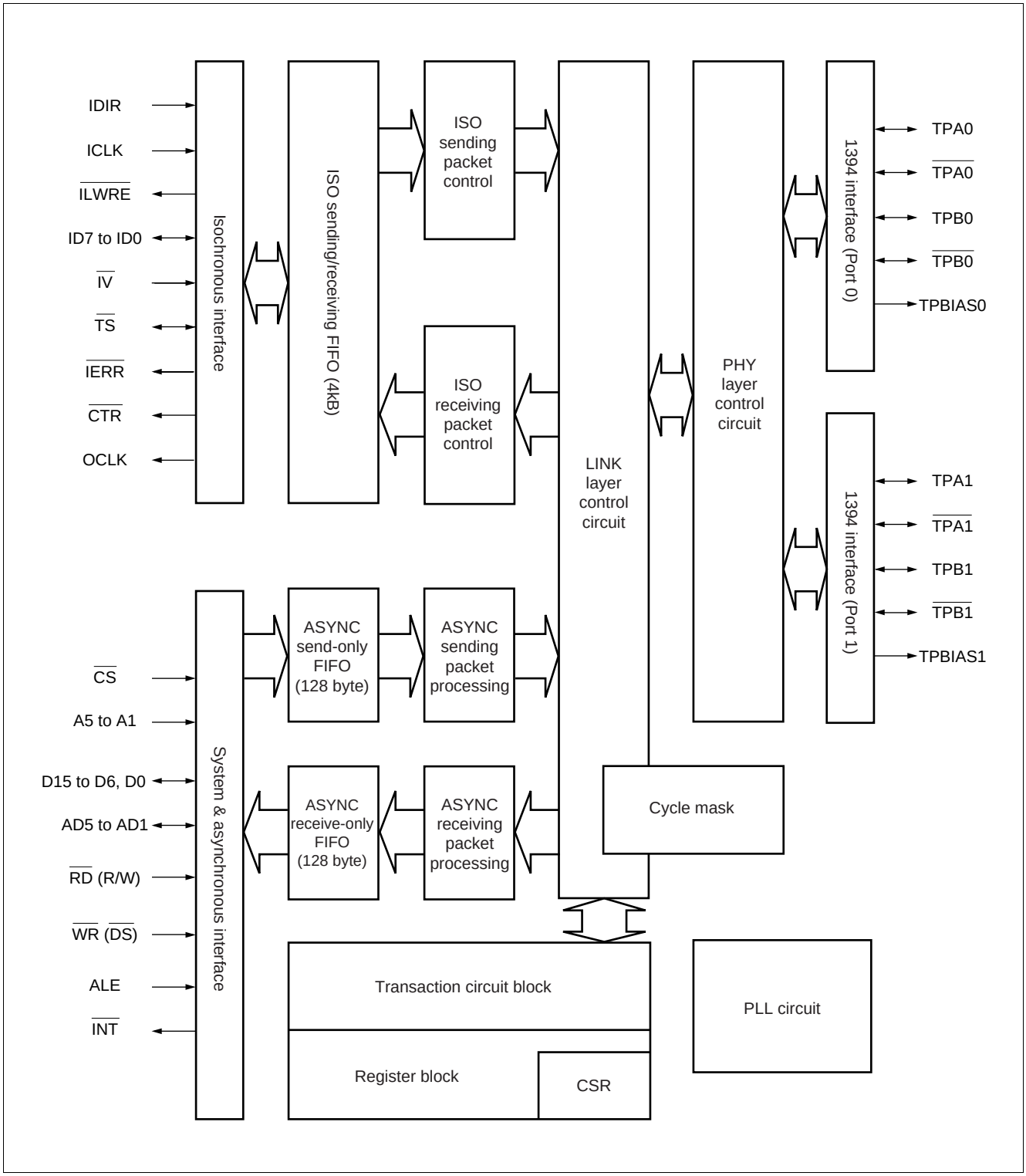
3. System Interface

Pin name	I/O	Function
$\overline{CS}$	I	Input pin for signals used by the MPU to select the MB86612 as an I/O device.
A5 to A1	I	Address input pins for internal register selection. Valid only in non-multiplexed mode. If multiplexed mode is selected these pins should be fixed at ‘0’.
D15 to D6, D0	I/O	16-bit data bus input/output pins (MSB is D15, LSB is D0).
AD5 to AD1	I/O	16-bit data bus input/output pins (MSB is AD5, LSB is AD1). Used for address input signals when multiplexed mode is selected.
$\overline{RD}$ (R/W)	I	80-series mode: Read strobe signal input pin, used to output data from the MB86612 to the data bus. 68-series mode: Control signal input pin, used for data input/output operations to the MB86612.
$\overline{WR}$ ($\overline{DS}$)	I	80-series mode: Write strobe signal input pin, used to input data from the data bus to the MB86612. 68-series mode: $\overline{DS}$ signal input pin, output when data bus is enabled.
ALE	I	ALE signal input pin, for signal output when addresses are enabled in multiplexed mode. In non-multiplexed mode, this signal should be fixed at ‘0’.
$\overline{INT}$	O	Interrupt output pin.

4. Other

Pin name	I/O	Function
X0	I/O	External crystal connection pins for oscillator circuits.
X1	I	
VCOIN	I	VCO input pin for internal PLL.
CHPO	O	Charge pump output pin for internal PLL.
ROP	O	Connect to GND through 4.7 kΩ resistance.
$\overline{\text{RESET}}$	I	Reset signal input pin. This signal should be set to '0' when the system power supply is off.
MODE0	I	Input '0' for 80-series mode. Input '1' for 68-series mode.
MODE1	I	Input '0' for non-multiplexed mode. Input '1' for multiplexed mode.
PMODE	I	For cable power supply, set to '0' for power startup. Set to '1' when cable power supply is off or until system power is on.
PWR1 to PWR3	I	When operating from cable power supply, these pins determine the value of the 'POWER_CLASS' area of Self-ID packets. When operating from system power supply, these pins correspond to the power bit in the Self-ID-PKT-param setting register.
BUSRST	I	When the MB86612 is started from the power supply this bit determines whether a bus reset is applied automatically. Input '0' for no bus reset. Input '1' for bus reset. When this bit is set to '1', a bus reset is executed 200 μs after the int-reset bit (bit 9) in the flag & status register (address 02h) is set to '1'.
LINKON	O	Link-on packet receiving detection pin. Outputs an 'H' signal for 1 to 2 tclk (1 to 2 cycles of the crystal oscillator input signal) when a link-0n packet is received. When this signal is not used, leave it open.
AV_{DD}	—	Analog power supply
AV_{SS}	—	Analog ground
V_{DD}	—	Digital power supply
V_{SS}	—	Digital ground
TESTP	—	Test pin. Do not connect.

■ BLOCK DIAGRAM



■ BLOCK DESCRIPTIONS

- PHY Layer Control Circuit
  This block contains the IEEE 1394 physical layer control circuits.
  Both asynchronous transfer and isochronous transfer in a cable environment are supported.
  The transfer speed is 98.304 Mbit/sec.
  Two analog transceiver/receiver ports are built-in.
  This block provides bus status monitoring initialization operation after a bus reset is applied, as well as arbitration and encoding/decoding functions for data sending and receiving.

- LINK Layer Control Circuit
  This block controls the generation and transfer of IEEE 1394 standard packets.
  32-bit CRC generation and checking is performed for packet headers and data.
  A 32-bit cycle timer register is built-in to provide cycle master functions.

- Sending/Receiving FIFO
  Contains built-in 4-byte FIFO areas, used for isochronous smoothing and rate conversion for both sending and receiving.
  Contains independent sending and receiving 128-byte FIFO areas for asynchronous transfer.

- Packet Processing
  Sending: Performs packetizing of headers, data and CRC. Automatically generates and attaches CRC.
  Receiving: Separates 1394 packet headers and data, strips CRC.

- Special Transaction Circuits
  These circuits operate with the packet processing block in handling data from the isochronous interface, packetizing for MPEG and DVC transfer as well as rebuilding receiving data for the isochronous interface.

- Register Block
  This block contains various device control registers, as well as registers for setting parameters required for 1394 transfer, AVC protocol registers and CSR.
  The built-in CSR provides isochronous resource manager functions.

- PLL Circuit
  This block uses the reference clock signal generated by the crystal oscillator circuit to create internal operating clock and transfer clock signals.
  Reference oscillator frequency: 8.192 MHz.

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min.	Max.	
Power supply voltage*1	V_{DD}	V_{SS} – 0.5	4.0	V
Input voltage*1	V_I	V_{SS} – 0.5	V_{DD} + 0.5	V
Output voltage*1	V_O	V_{SS} – 0.5	V_{DD} + 0.5	V
Strage temperature	Tst	–55	+125	°C
Operating temperature*2	Top	–40	+85	°C
Output current*3	I_O	–14	+14	mA
Overshoot*4	—	—	V_{DD} + 1.0	V
Undershoot*4	—	—	V_{SS} – 1.0	V

*1: Voltage values are based on Vss = 0 V.
*2: Not warranted for continuous operation.
*3: Normal output current flow (Minimum at Vo = 0 V, maximum at Vo = V_{DD}).
*4: 50 ns or less.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter		Symbol	Value		Unit
			Min.	Max.	
Power supply voltage*		V_{DD}	3.0	3.6	V
“H” level input voltage	CMOS input	V_{IH}	$V_{DD} \times 0.65$	V_{DD}	V
“L” level input voltage	CMOS input	V_{IL}	V_{SS}	$V_{DD} \times 0.25$	V
Differential input voltage (for data transfer)	Cable input	V_{ID}	142	260	mV
Differential input voltage (for arbitration)	Cable input	V_{IDA}	173	260	mV
Common mode input voltage	Cable input	V_{CM}	1.165	2.515	V
Receiving input jitter	Cable input	—	—	1.08	ns
Receiving input skew	Cable input	—	—	0.8	ns
Output current	CMOS output	I_{OH}/I_{OL}	–4	4	mA
	TPBIAS	Iot	–2	10	mA
Operating temperature		Ta	0	+70	°C

* : Voltage values are based on Vss = 0 V.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

1.1 System Interface, etc

(V_{DD} = 3 to 3.6 V , V_{SS} = 0 V, Ta = 0 to +70°C)

Parameter		Symbol	Conditions	Value			Unit
				Min.	Typ.	Max.	
"H" level input voltage		V_{IH}	CMOS	$V_{DD} \times 0.65$	—	V_{DD}	V
"L" level input voltage		V_{IL}	CMOS	V_{SS}	—	$V_{DD} \times 0.25$	V
"H" level output voltage		V_{OH}	I_{OH} = –4 mA	V_{DD} – 0.5	—	V_{DD}	V
"L" level output voltage		V_{OL}	I_{OL} = –4 mA	V_{SS}	—	0.4	V
Input leak current	Input pins	I_{LI}	V_I = 0V to V_{DD}	–5	—	5	µA
	3-state pin input	I_{LZ}		–5	—	5	µA
Input pull-up/pull down resistance		Rp	$V_{IH} = V_{DD}$	25	50	200	kΩ
Power supply current		I_{DDS0}	No port connected*1	—	—	220	mA
		I_{DDS1}	1 port connected*1	—	—	270	mA
		I_{DDS2}	2 ports connected*1	—	—	300	mA
		I_{DDSS}	Forced sleep*1	—	—	50	mA
		I_{DDCN}	Non repeating*2	—	—	220	mA
		I_{DDCR}	Repeating*2	—	—	240	mA

*1: Operating from system power supply
*2: Operating from cable power supply

1.2 1394 Interface Driver

(V_{DD} = 3 to 3.6 V , V_{SS} = 0 V, Ta = 0 to +70°C)

Parameter	Symbol	Conditions	Value		Unit
			Min.	Max.	
Differential output voltage	V_{OD}	R_1 = 56 Ω	172	265	mV
Common phase current	I_{CM}	Driver enabled	–0.81	0.44	mA
Off state voltage	V_{OFF}	Driver disabled	—	20	mV
TPBIAS output voltage	V_O	—	1.665	2.015	V

1.3 1394 Interface - Comparator

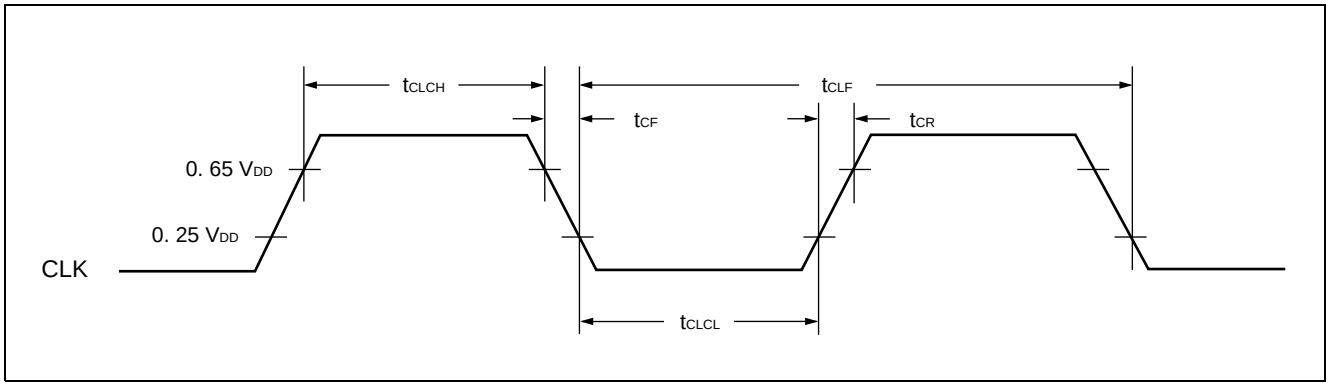
(V_{DD} = 3 to 3.6 V , V_{SS} = 0 V, Ta = 0 to +70°C)

Parameter	Symbol	Conditions	Value		Unit
			Min.	Max.	
Common phase input current	I_{IC}	Driver disabled	–20	20	µA
Arbitration comparator “H” level threshold voltage	V_{SCH}	Driver disabled	168	—	mV
Arbitration comparator “Z” level threshold voltage	V_{SEZ}	Driver disabled	–30	30	mV
Arbitration comparator “L” level threshold voltage	V_{SCL}	Driver disabled	—	–168	mV
Port status comparator disconnection detect voltage	V_{SD}	Driver disabled	0.6	—	V
Port status comparator connection detect voltage	V_{SC}	Driver disabled	—	1.0	V

2. AC Characteristics

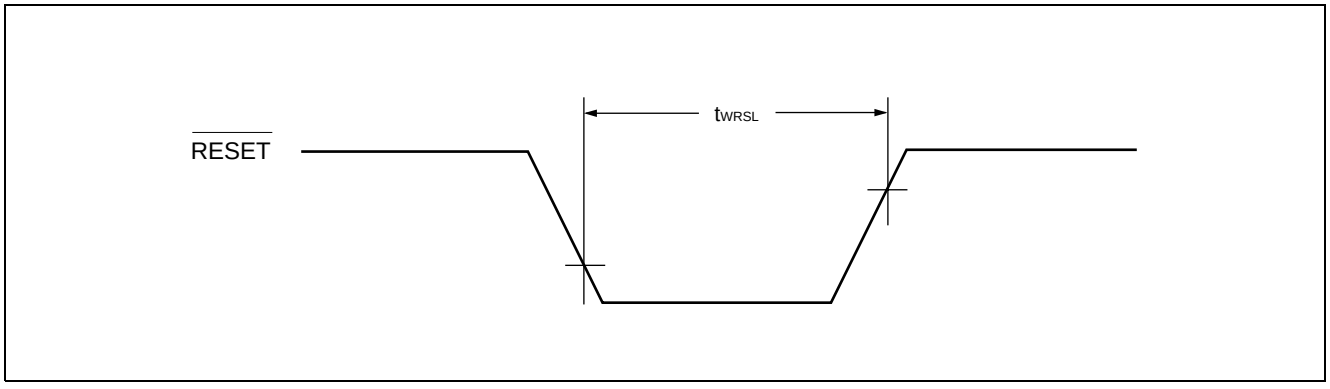
2.1 System Clock

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Clock frequency	f_C	—	8.192	—	MHz
Clock cycle time	t_{CLF}	—	1/fc	—	ns
Clock pulse width	t_{CLCH} t_{CLCL}	50	—	—	ns
Clock rise/fall time	t_{CR} t_{CF}	—	—	5	ns



2.2 System Reset

Parameter	Symbol	Value		Unit
		Min.	Max.	
Reset (RESET) “L” level pulse width	t_{WRSL}	4 tclf	—	ns



2.3 Driver

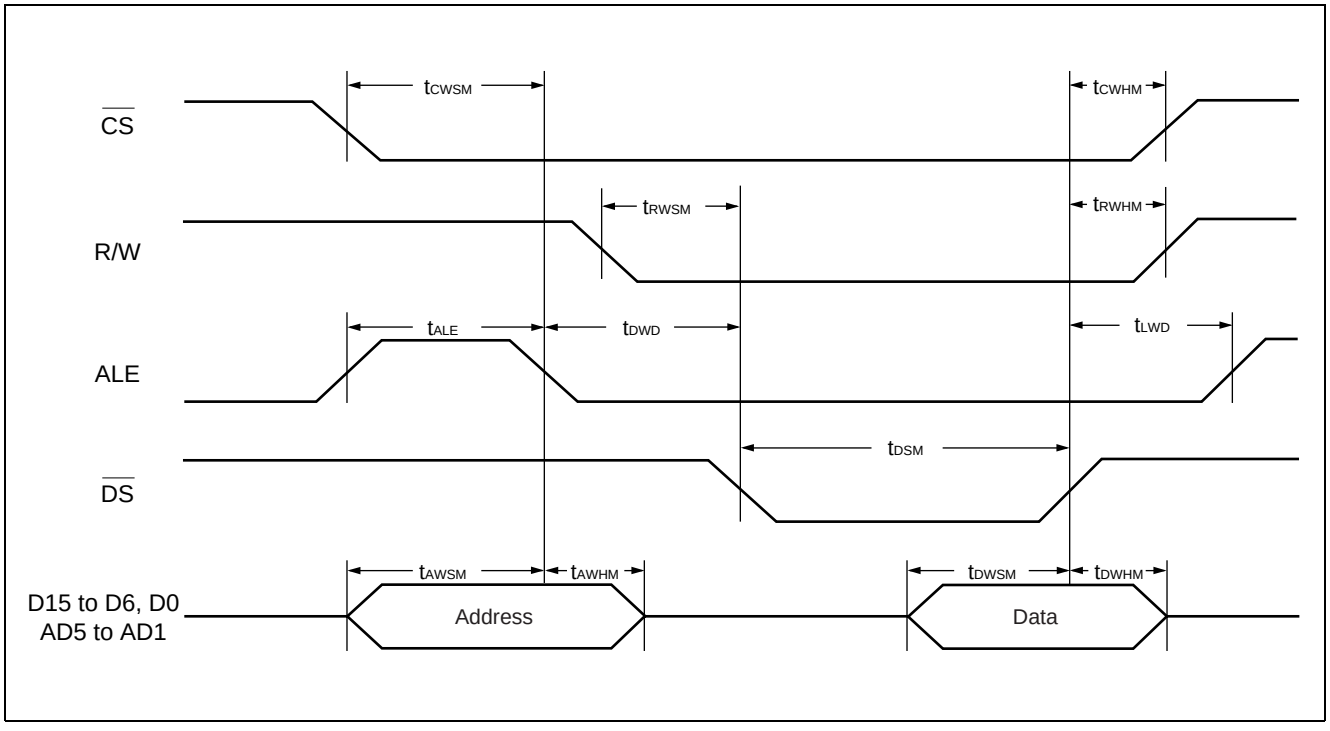
Parameter	Symbol	Value		Unit
		Min.	Max.	
Sending jitter	t_{JT}	—	±0.8	ns
Sending skew	t_{SK}	—	±0.8	ns
Sending rise time*	t_{DR}	—	3.2	ns
Sending fall time*	t_{DF}	—	3.2	ns

* : 10 to 90% value.

2.4 System Interface

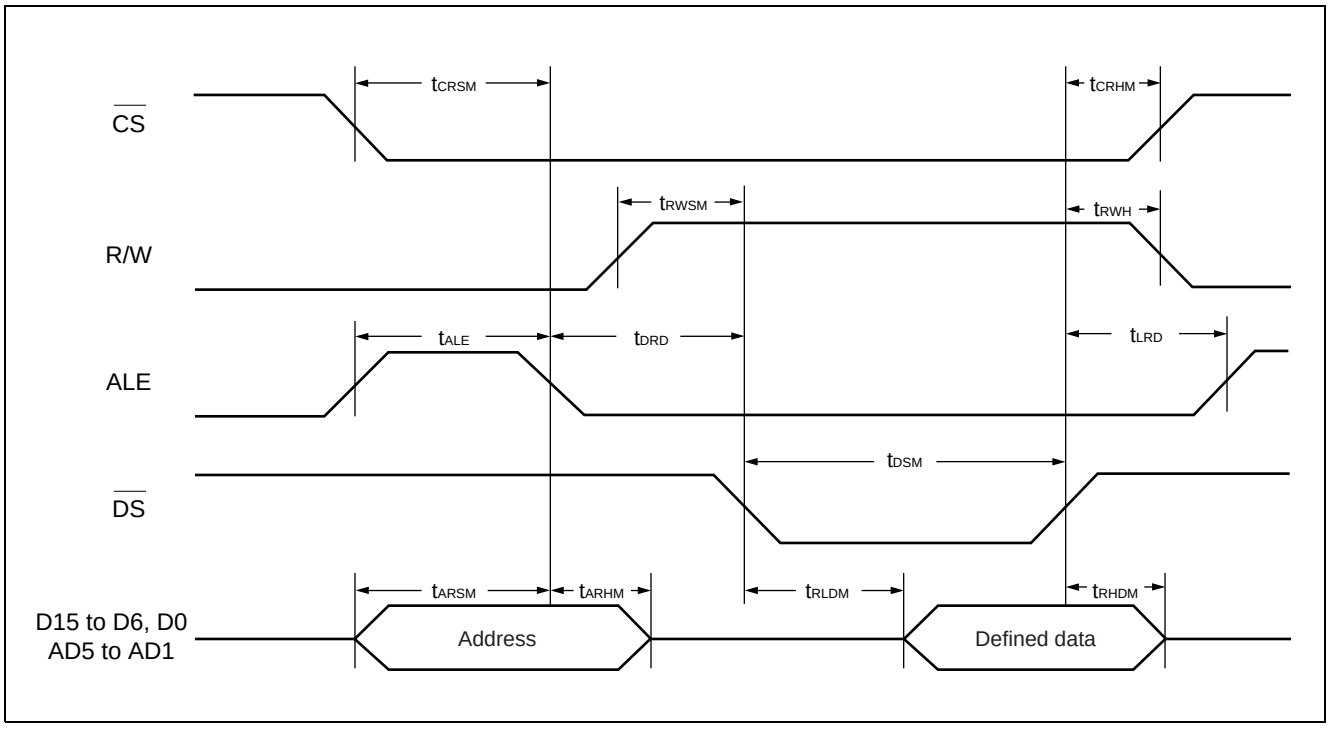
(1) 68-Series Register Write Operation (multiplexed)

Parameter	Symbol	Value		Unit
		Min.	Max.	
Address setup time	t_{AWSM}	10	—	ns
Address hold time	t_{AWHM}	5	—	ns
$\overline{CS}$ setup time	t_{CWSM}	10	—	ns
$\overline{CS}$ hold time	t_{CWHM}	5	—	ns
Data setup time	t_{DWSM}	10	—	ns
Data hold time	t_{DWHM}	0	—	ns
R/W setup time	t_{RWSM}	5	—	ns
R/W hold time	t_{RWHM}	5	—	ns
ALE fall to $\overline{DS}$ fall time	t_{DWD}	10	—	ns
$\overline{DS}$ rise to ALE rise time	t_{LWD}	5	—	ns
ALE “H” level pulse width	t_{ALE}	10	—	ns
$\overline{DS}$ “L” level pulse width	t_{DSM}	20	—	ns



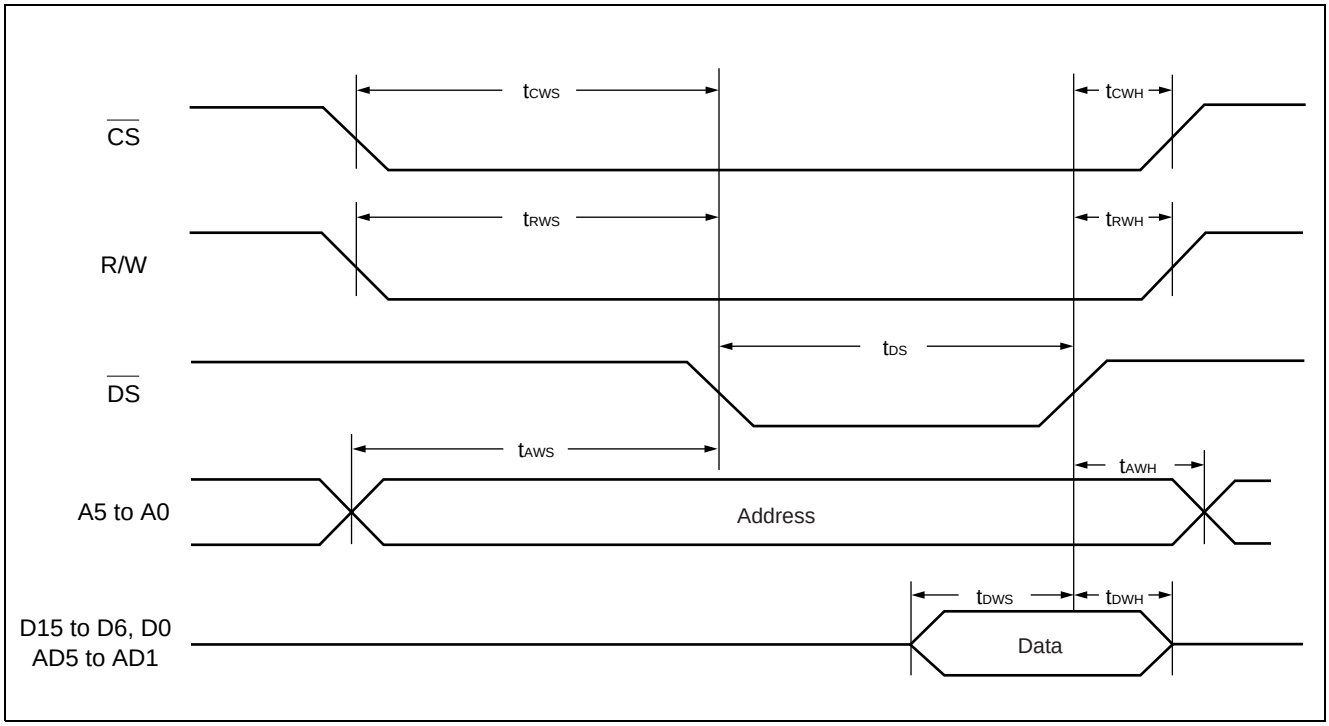
(2) 68-System Register Read Operation (multiplexed)

Parameter	Symbol	Value		Unit
		Min.	Max.	
Address setup time	t_{ARSM}	10	—	ns
Address hold time	t_{ARHM}	5	—	ns
$\overline{CS}$ setup time	t_{CRSM}	10	—	ns
$\overline{CS}$ hold time	t_{CRHM}	5	—	ns
Data output definition time	t_{RLDM}	—	15	ns
Data output disabled time	t_{RHDM}	0	—	ns
R/W setup time	t_{RWSM}	5	—	ns
R/W hold time	t_{RWH}	5	—	ns
ALE fall to $\overline{DS}$ fall time	t_{DRD}	10	—	ns
$\overline{DS}$ rise to ALE rise time	t_{LRD}	5	—	ns
ALE “H” level pulse width	t_{ALE}	10	—	ns
$\overline{DS}$ “L” level pulse width	t_{DSM}	20	—	ns



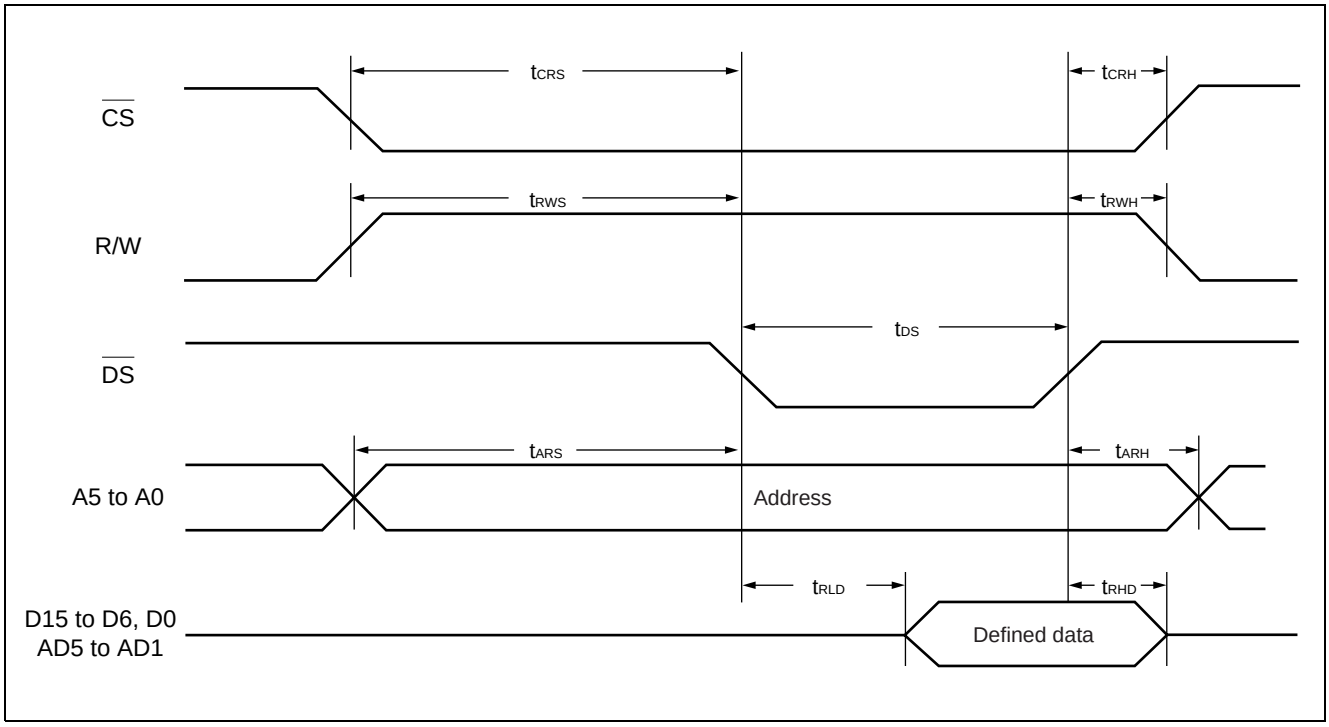
(3) 68-Series Register Write Operation (non-multiplexed)

Parameter	Symbol	Value		Unit
		Min.	Max.	
Address setup time	t_{AWS}	5	—	ns
$\overline{CS}$ setup time	t_{CWS}	5	—	ns
$\overline{CS}$ hold time	t_{CWH}	5	—	ns
Data setup time	t_{DWS}	10	—	ns
Data hold time	t_{DWH}	0	—	ns
$\overline{DS}$ "L" level pulse width	t_{DS}	20	—	ns
R/W setup time	t_{RWS}	5	—	ns
R/W hold time	t_{RWH}	5	—	ns
$\overline{DS}$ rise to address hold time	t_{AWH}	5	—	ns



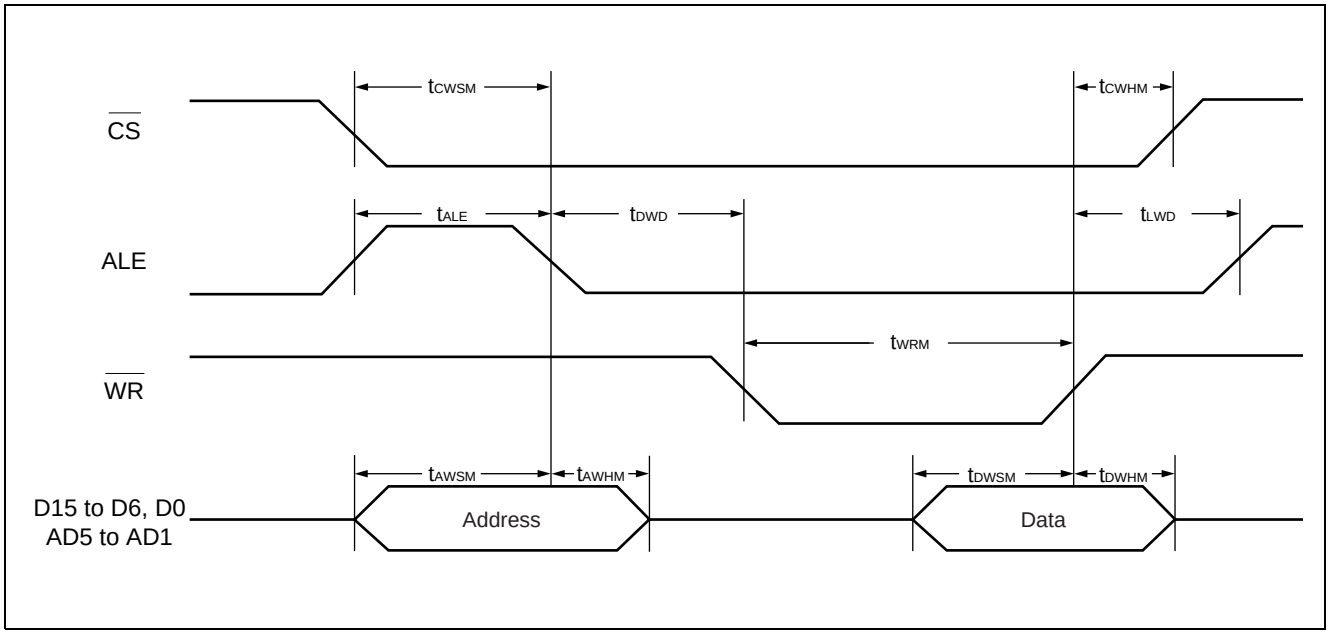
(4) 68-Series Register Read Operation (non-multiplexed)

Parameter	Symbol	Value		Unit
		Min.	Max.	
Address setup time	t_{ARS}	5	—	ns
$\overline{CS}$ setup time	t_{CRS}	5	—	ns
$\overline{CS}$ hold time	t_{CRH}	5	—	ns
Data output definition time	t_{RLD}	—	15	ns
Data output disabled time	t_{RHD}	0	—	ns
$\overline{DS}$ "L" level pulse width	t_{DS}	20	—	ns
R/W setup time	t_{RWS}	5	—	ns
R/W hold time	t_{RWH}	5	—	ns
Address hold time	t_{ARH}	5	—	ns



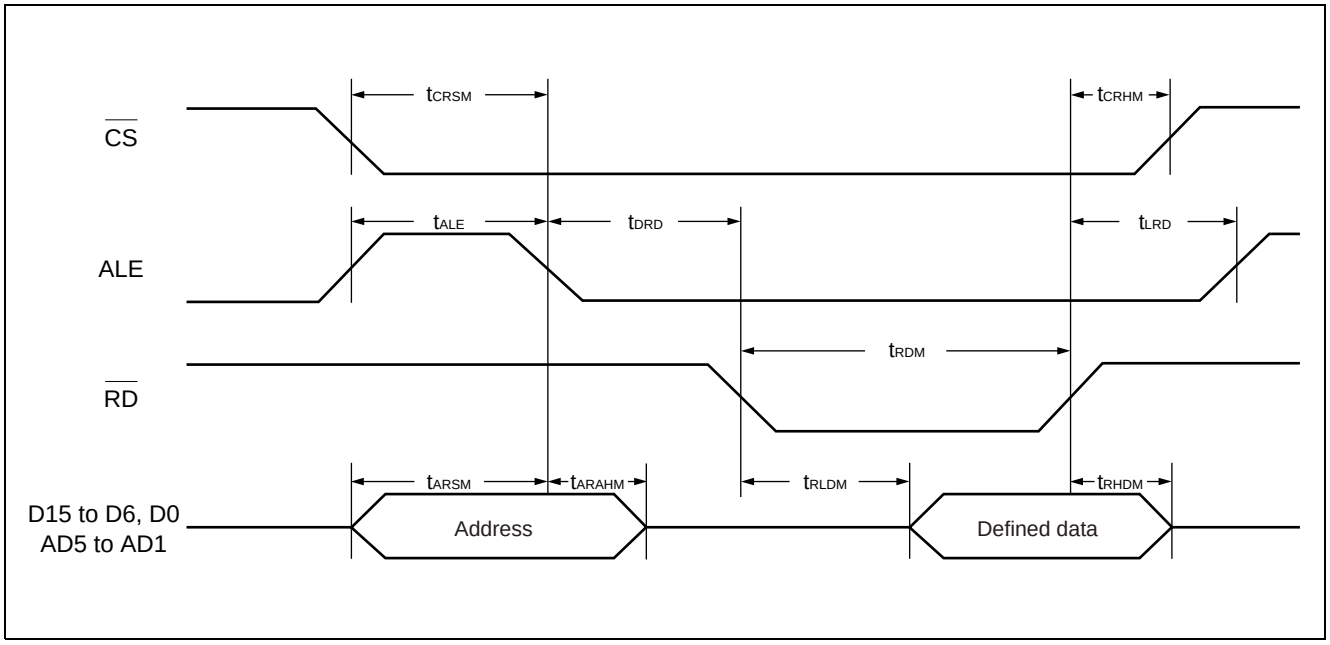
(5) 80-Series Register Write Operation (multiplexed)

Parameter	Symbol	Value		Unit
		Min.	Max.	
Address setup time	t_{AWSM}	10	—	ns
Address hold time	t_{AWHM}	5	—	ns
$\overline{CS}$ setup time	t_{CWSM}	10	—	ns
$\overline{CS}$ hold time	t_{CWHM}	5	—	ns
Data setup time	t_{DWSM}	10	—	ns
Data hold time	t_{DWHM}	0	—	ns
ALE fall to $\overline{WR}$ fall time	t_{DWD}	10	—	ns
$\overline{WR}$ rise to ALE rise time	t_{LWD}	5	—	ns
ALE “H” level pulse width	t_{ALE}	10	—	ns
$\overline{WR}$ “L” level pulse width	t_{WRM}	20	—	ns



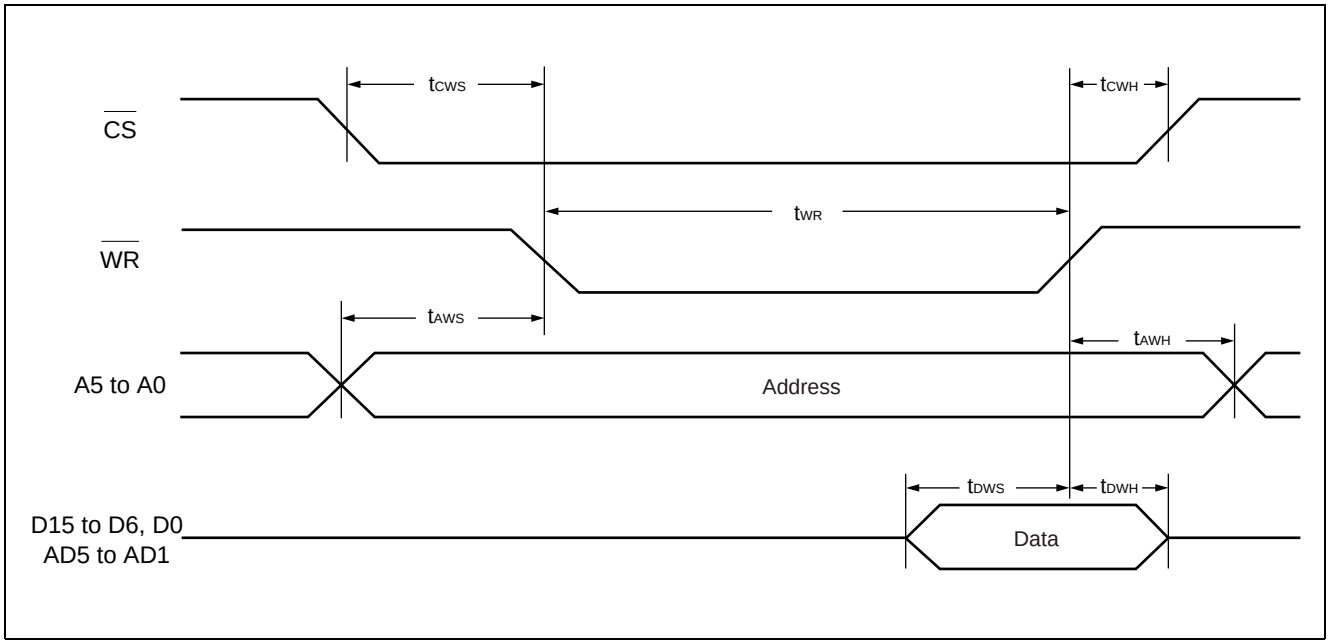
(6) 80-Series Register Read Operation (multiplexed)

Parameter	Symbol	Value		Unit
		Min.	Max.	
Address setup time	t_{ARSM}	10	—	ns
Address hold time	t_{ARAHM}	5	—	ns
$\overline{CS}$ setup time	t_{CRSM}	10	—	ns
$\overline{CS}$ hold time	t_{CRHM}	5	—	ns
Data output definition time	t_{RLDM}	—	15	ns
Data output disabled time	t_{RHDM}	0	—	ns
ALE fall to $\overline{RD}$ fall time	t_{DRD}	10	—	ns
$\overline{RD}$ rise to ALE rise time	t_{LRD}	5	—	ns
ALE “H” level pulse width	t_{ALE}	10	—	ns
$\overline{RD}$ “L” level pulse width	t_{RDM}	20	—	ns



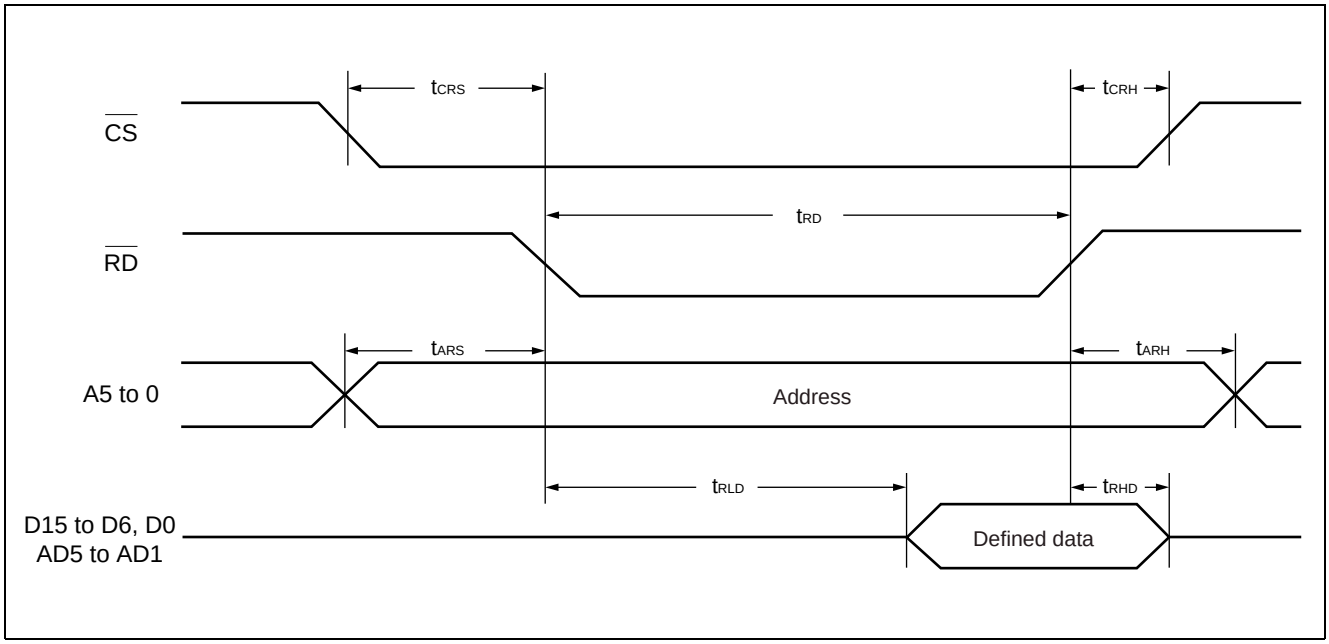
(7) 80-Series Register Write Operation (non-multiplexed)

Parameter	Symbol	Value		Unit
		Min.	Max.	
Address setup time	t_{AWS}	5	—	ns
$\overline{CS}$ setup time	t_{CWS}	5	—	ns
$\overline{CS}$ hold time	t_{CWH}	5	—	ns
Data setup time	t_{DWS}	10	—	ns
Data hold time	t_{DWH}	0	—	ns
$\overline{WR}$ "L" level pulse width	t_{WR}	20	—	ns
Address hold time	t_{AWH}	5	—	ns



(8) 80-Series Register Read Operation (non-multiplexed)

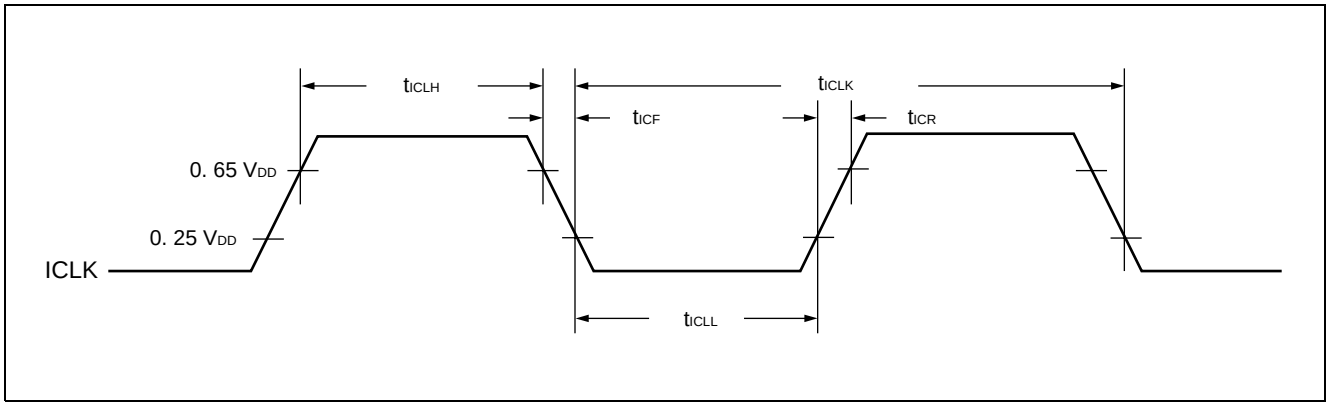
Parameter	Symbol	Value		Unit
		Min.	Max.	
Address setup time	t_{ARS}	5	—	ns
$\overline{CS}$ setup time	t_{CRS}	5	—	ns
$\overline{CS}$ hold time	t_{CRH}	5	—	ns
Data output definition time	t_{RLD}	—	15	ns
Data output disabled time	t_{RHD}	0	—	ns
$\overline{RD}$ "L" level pulse width	t_{RD}	20	—	ns
Address hold time	t_{ARH}	5	—	ns



2.5 Isochronous Interface

2.5.1 ICLK

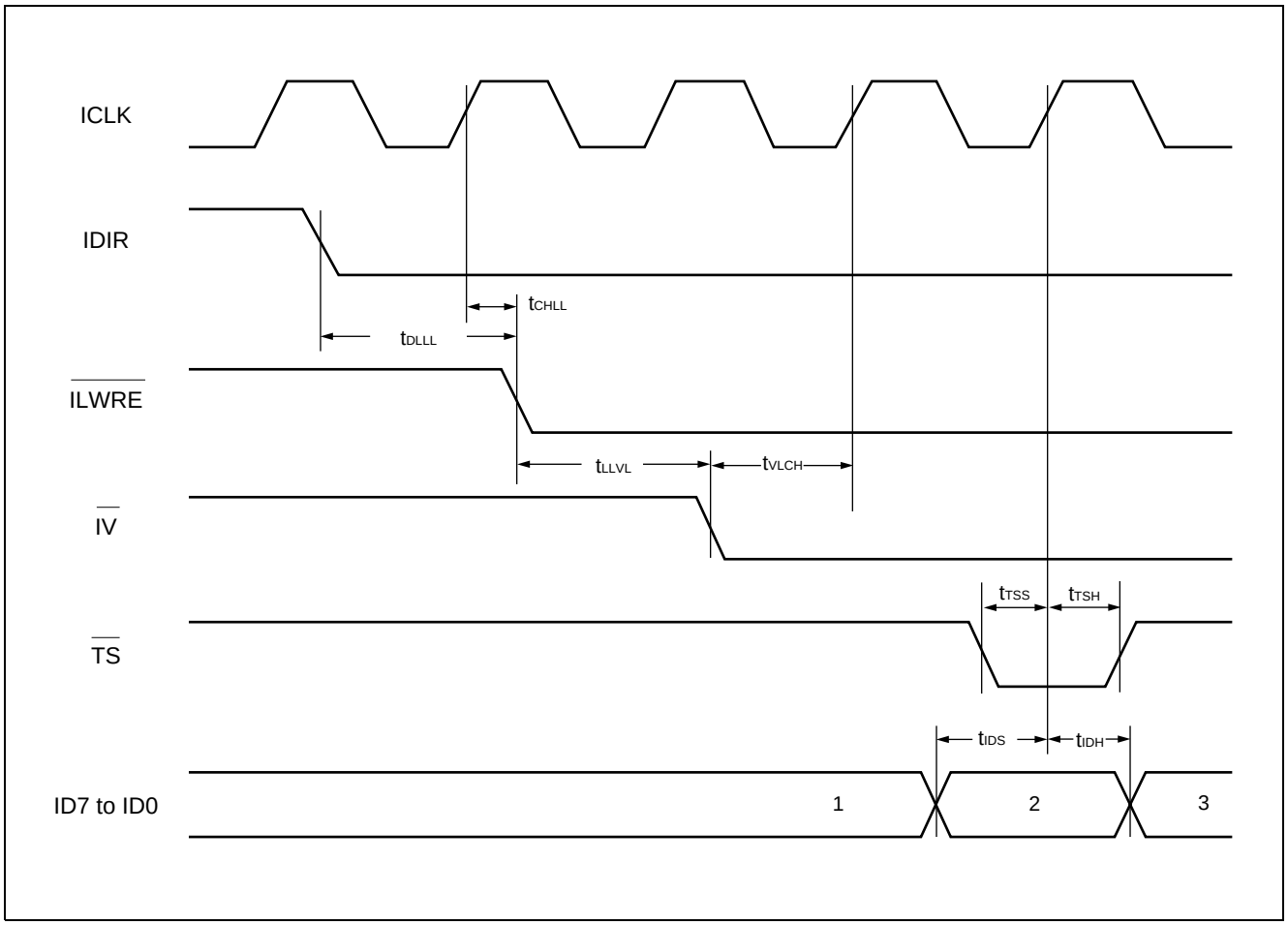
Parameter	Symbol	Value		Unit
		Min.	Max.	
Clock frequency	—	DC	16	MHz
Clock cycle time	t_{ICLK}	62.5	∞	ns
Clock pulse width	t_{ICLH} t_{ICLL}	10	—	ns
Clock rise/fall time	t_{ICR} t_{ICF}	—	10	ns



2.5.2 Sending Operation

(1) Start Sending Operation

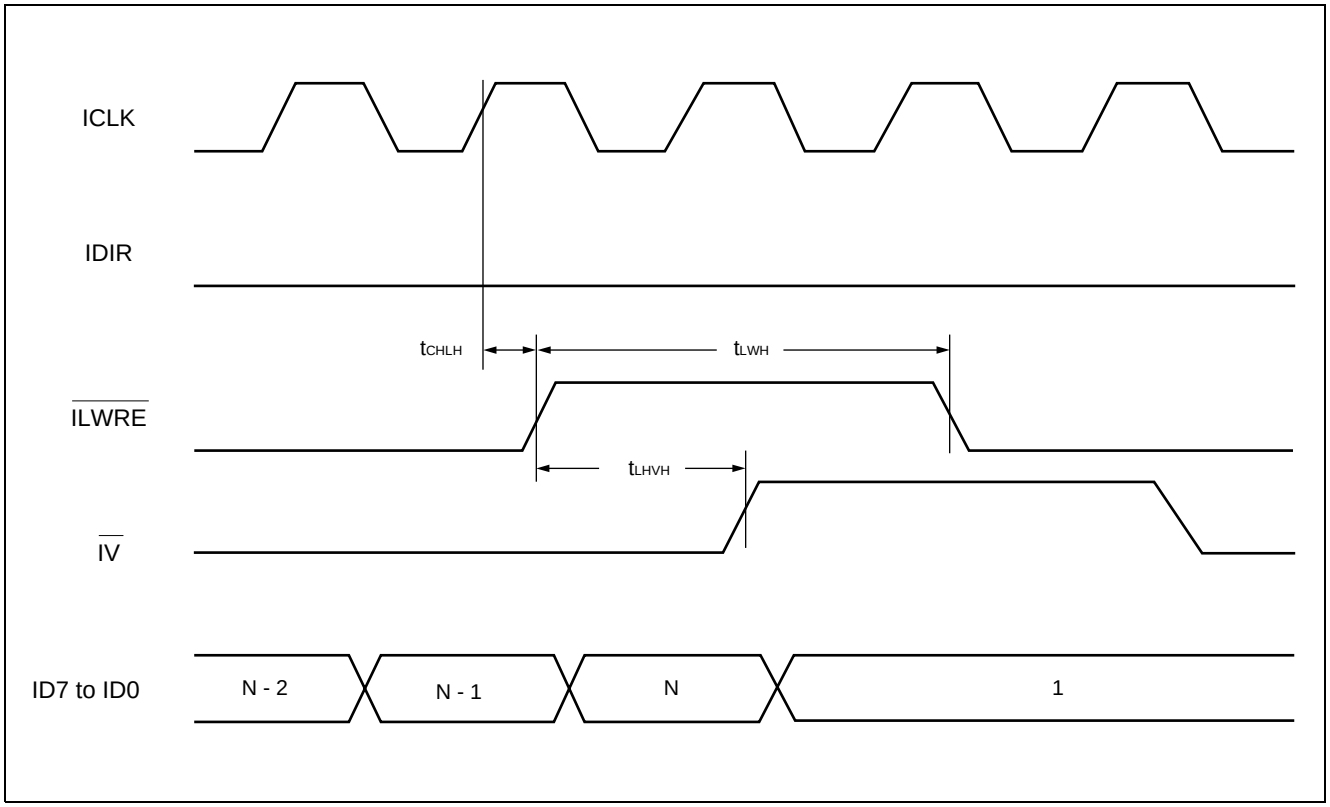
Parameter	Symbol	Value		Unit
		Min.	Max.	
IDIR fall to $\overline{\text{ILWRE}}$ fall	t_{DLLL}	—	4 ticlk + 10	ns
ICLK rise to $\overline{\text{ILWRE}}$ fall	t_{CHLL}	—	40	ns
$\overline{\text{ILWRE}}$ fall to $\overline{\text{IV}}$ fall	t_{LLVL}	1 ticlk + 10	—	ns
$\overline{\text{IV}}$ fall to ICLK rise	t_{VLCH}	20	—	ns
Data setup time	t_{IDS}	20	—	ns
Data hold time	t_{IDH}	0	—	ns
$\overline{\text{TS}}$ input setup time*	t_{TSS}	20	1 ticlk – 10	ns
$\overline{\text{TS}}$ input hold time*	t_{TSH}	20	1 ticlk – 10	ns



* : Specifications t_{IDH} and t_{TSS} are valid in DVC mode only. $\overline{\text{TS}}$ input is not used in MPEG mode.

(2) End Sending Operation

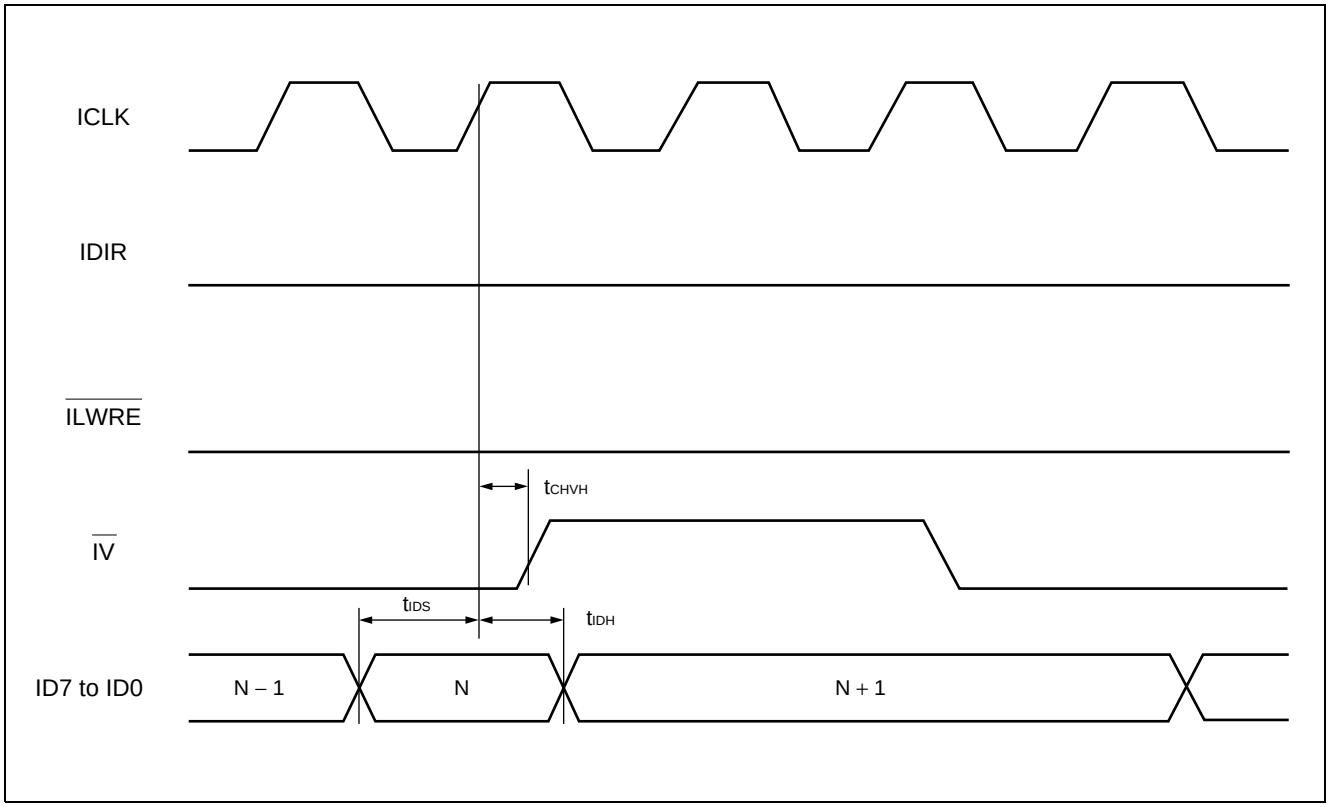
Parameter	Symbol	Value		Unit
		Min.	Max.	
ICLK rise to $\overline{\text{ILWRE}}$ rise	t_{CHLH}	—	40	ns
$\overline{\text{ILWRE}}$ rise to $\overline{\text{IV}}$ rise	t_{LHVH}	1 ticlk + 10	—	ns
$\overline{\text{ILWR}}$ negate time*	t_{LWH}	2 ticlk – 10	—	ns



* : The MB86612 operates in 'negate mode', in which the $\overline{\text{ILWRE}}$ signal is negated for each source packet received, as well as 'assert mode', in which the $\overline{\text{ILWRE}}$ signal is continuously asserted as long as ISO sending and receiving FIFO writing are enabled. The above timing chart shows operation in negate mode. If there one or more packets of empty space are present in the sending or receiving FIFO area, the $\overline{\text{ILWRE}}$ signal is again asserted.Note that even in assert mode, if writing to the ISO sending or receiving FIFO areas is disabled, the $\overline{\text{ILWRE}}$ signal is negated according to the timing shown above, and re-asserted when writing is again enabled.

(3) $\overline{IV}$ Temporary Negation in Sending Operation

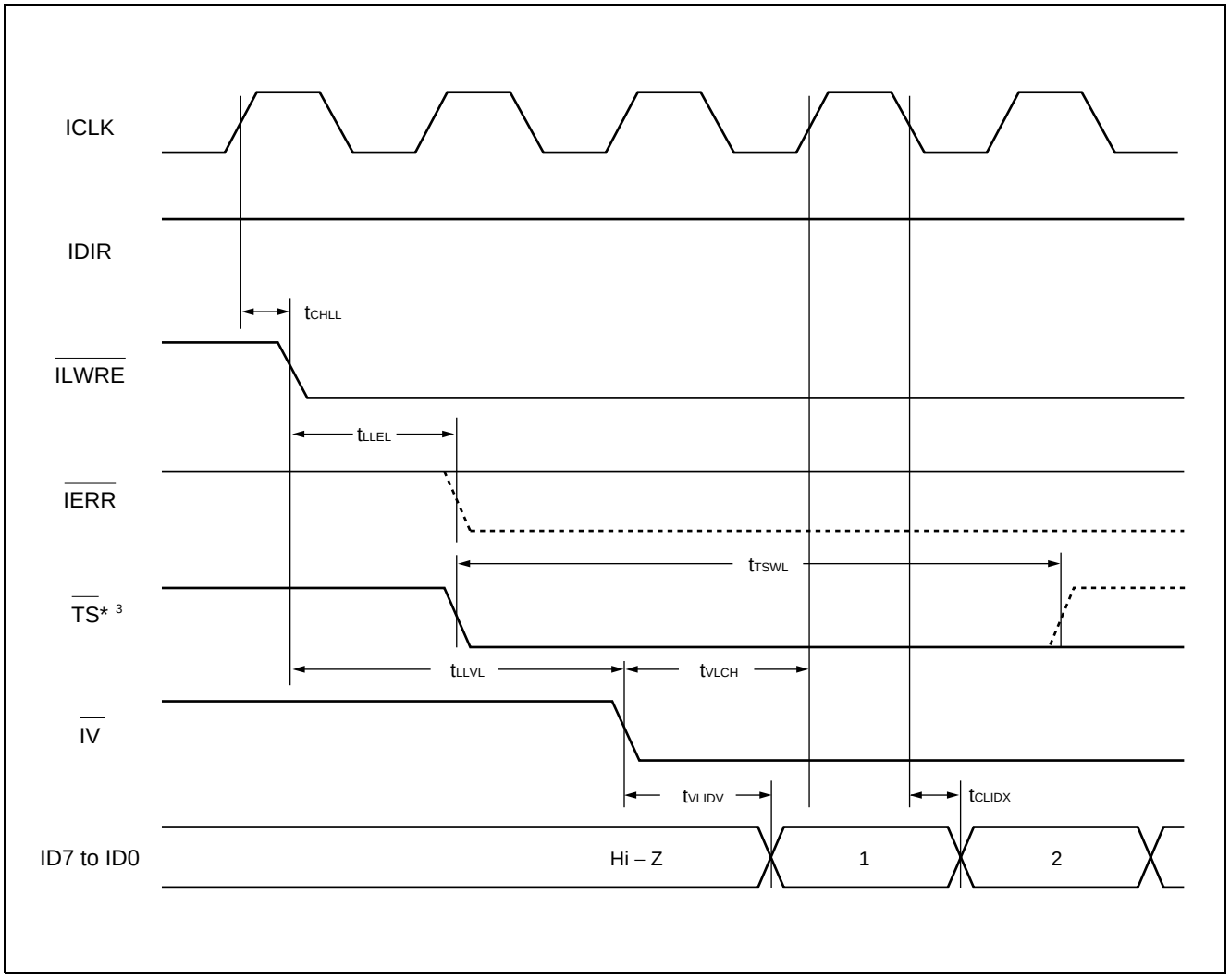
Parameter	Symbol	Value		Unit
		Min.	Max.	
ICLK rise to $\overline{IV}$ rise	t_{CHVH}	0	1 ticlk – 20	ns
Date setup time	t_{IDS}	20	—	ns
Data hold time	t_{IDH}	0	—	ns



2.5.3 Receiving Operation

(1) Start Receiving Operation

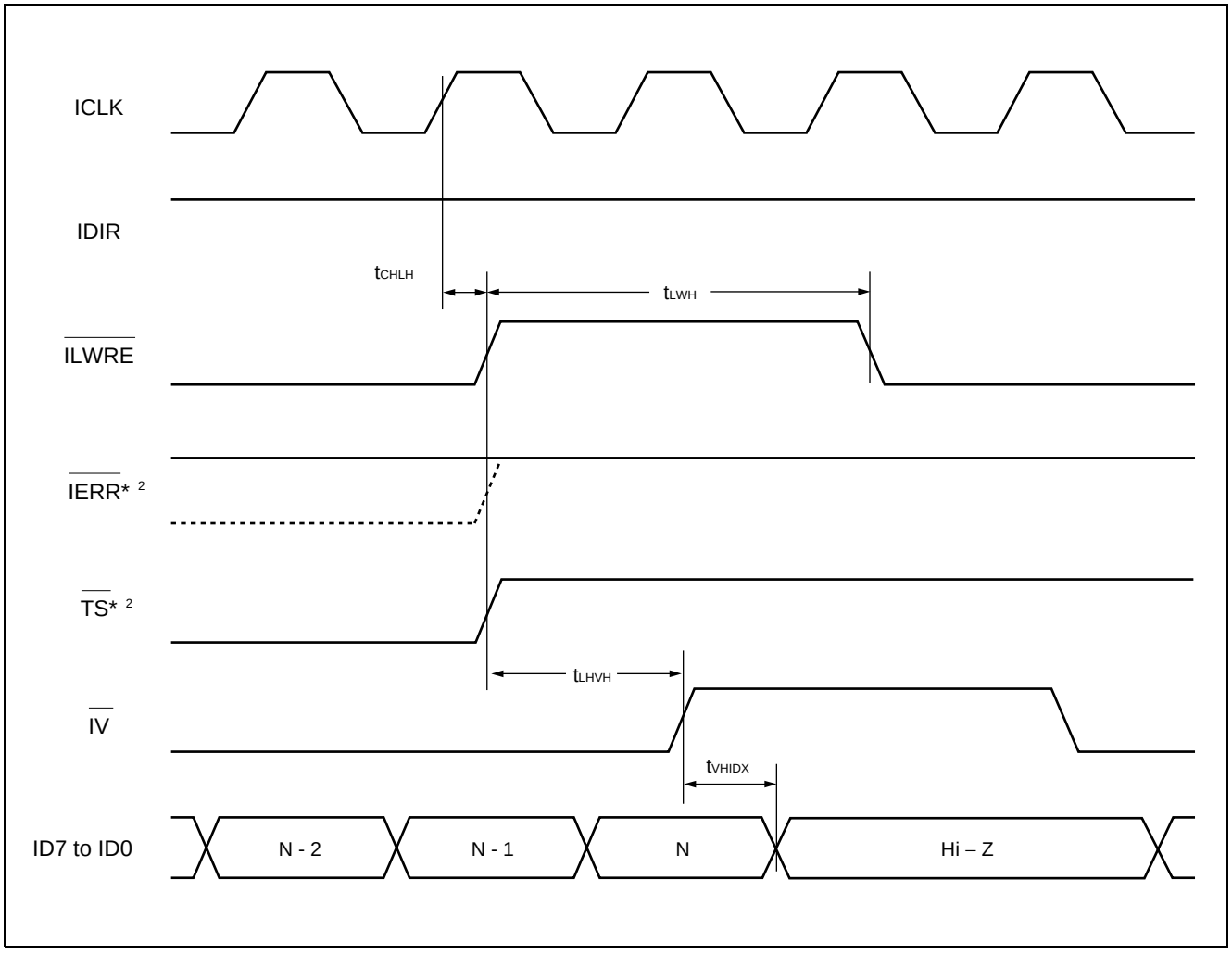
Parameter	Symbol	Value		Unit
		Min.	Max.	
ICLK rise to $\overline{\text{ILWRE}}$ fall	t_{CHLL}	—	40	ns
$\overline{\text{ILWRE}}$ fall to $\overline{\text{IERR}}$ fall*1	t_{LLEL}	—	1 ticlk + 10	ns
$\overline{\text{ILWRE}}$ fall to $\overline{\text{IV}}$ fall	t_{LLVL}	1 ticlk + 10	—	ns
$\overline{\text{IV}}$ fall to ICLK rise	t_{VLCH}	20	—	ns
Data output definition time	t_{VLIDV}	—	20	ns
Data output disable time	t_{CLIDX}	0	10	ns
$\overline{\text{TS}}$ output assert time*2	t_{TSWL}	32 ticlk – 10	—	ns



*1: The $\overline{\text{IERR}}$ signal is output when an error is detected in receiving data.
*2: Specification t_D is valid only in DVC mode. It does not apply to MPEG mode.
*3: The $\overline{\text{TS}}$ signal is output in synchronization with the rise of the ICLK pulse at the time the receiving packet time stamp match is detected.

(2) End Receiving Operation

Parameter	Symbol	Value		Unit
		Min.	Max.	
ICLK rise to $\overline{\text{ILWRE}}$ rise	t_{CHLH}	—	40	ns
$\overline{\text{ILWRE}}$ rise to $\overline{\text{IV}}$ rise	t_{LHVH}	1 ticlk + 10	—	ns
Final data output disable time	t_{VHIDX}	—	20	ns
$\overline{\text{ILWRE}}$ negate time*1	t_{LWH}	2 ticlk – 10	—	ns

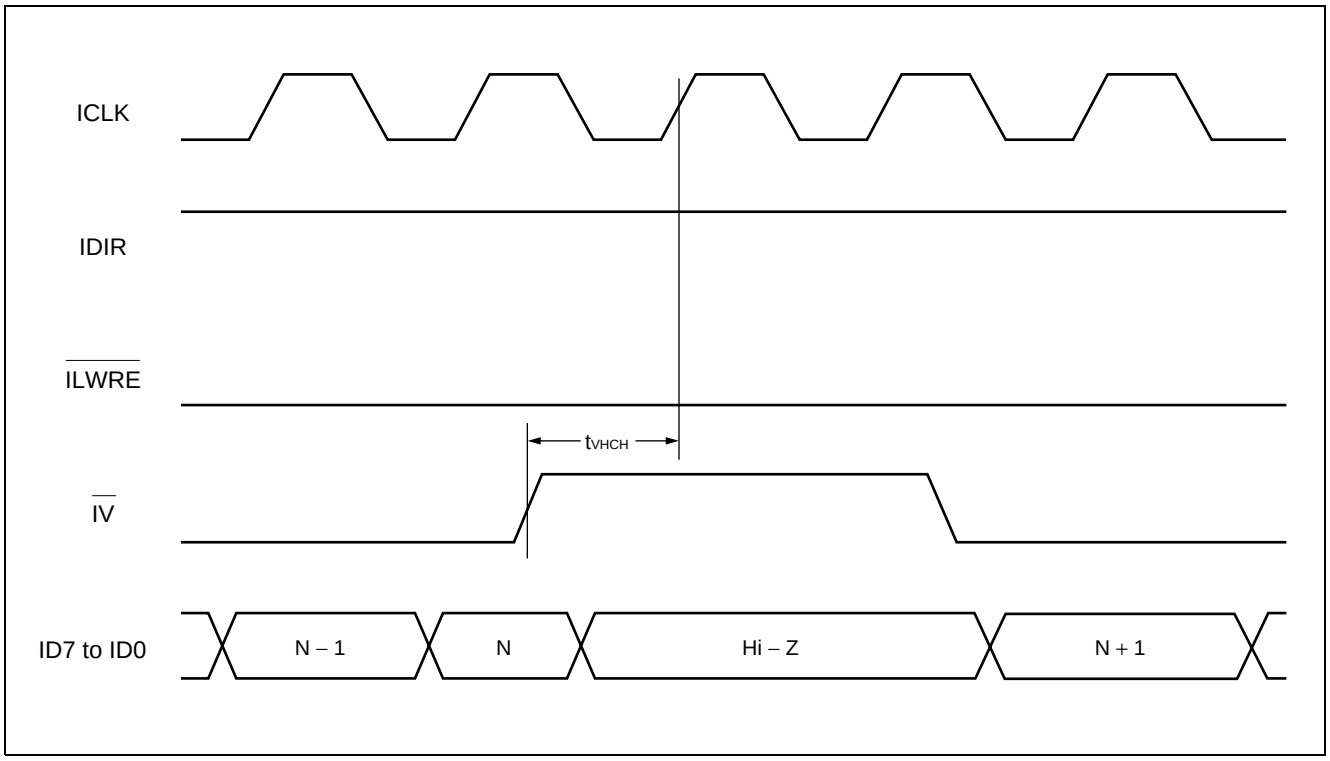


*1: The MB86612 operates in 'negate mode', in which the $\overline{\text{ILWRE}}$ signal is negated for each source packet received, as well as 'assert mode', in which the $\overline{\text{ILWRE}}$ signal is continuously asserted as long as ISO sending and receiving FIFO writing are enabled. The above timing chart shows operation in negate mode. If there one or more packets of empty space are present in the sending or receiving FIFO area, the $\overline{\text{ILWRE}}$ signal is again asserted.Note that even in assert mode, if writing to the ISO sending or receiving FIFO areas is disabled, the $\overline{\text{ILWRE}}$ signal is negated according to the timing shown above, and re-asserted when writing is again enabled.

*2: The $\overline{\text{TS}}$ (in MPEG mode) and $\overline{\text{IERR}}$ signals are negated in synchronization with the $\overline{\text{ILWRE}}$ signal.

(3) $\overline{IV}$ Temporary Negation in Receiving Operation

Parameter	Symbol	Value		Unit
		Min.	Max.	
$\overline{IV}$ rise to ICLK rise	t_{VHCH}	40	—	ns



■ INTERNAL REGISTERS

The MB86612 internal registers have 3-bank construction, with 16-bit access to all registers.
Bank 0 contains registers necessary for IEEE 1394 settings and transfer, bank 1 contains registers necessary for AV/C (MPEG, DVC) operation, and bank 2 contains CSR's.
In addition each bank has registers used in common for MB86612 device control.

1. Bank Common Registers

The following registers can be accessed in any bank from bank 0 to bank 2.

Address						Write operation	Read operation
HEX	A5	A4	A3	A2	A1		
00	0	0	0	0	0	mode-control register	←
02	0	0	0	0	1	(reserved)	flag & status register
04	0	0	0	1	0	instruction fetch register	←
06	0	0	0	1	1	interrupt mask register	interrupt code register
08	0	0	1	0	0	(reserved)	Receiving acknowledge display register
0A	0	0	1	0	1	ASYNC data port (sending)	ASYNC data port (receiving)
0C	0	0	1	1	0	(reserved)	←
0E	0	0	1	1	1	(reserved)	←
3E	1	1	1	1	1	bank select register	←

2. Bank 0 Registers

Bank 0 contains the registers required for 1394 settings and transfers.

Access to this bank is enabled by writing ‘0000h’ to the bank select register (3Eh).

Address						Write operation	Read operation
HEX	A5	A4	A3	A2	A1		
10	0	1	0	0	0	Sending ISO PKT header setting register (high)	Receiving ISO PKT header display register (high)
12	0	1	0	0	1	Sending ISO PKT header setting register (low)	Receiving ISO PKT header display register (low)
14	0	1	0	1	0	Sending ASYNC des ID setting register	(reserved)
16	0	1	0	1	1	Sending ASYNC PKT param setting register	Receiving ASYNC PKT param display register
18	0	1	1	0	0	Sending ASYNC data length setting register	Receiving ASYNC data length display register
1A	0	1	1	0	1	Sending ASYNC ex tcode setting register	Receiving ASYNC ex tcode display register
1C	0	1	1	1	0	Sending ASYNC source ID setting register	Receiving ASYNC source ID display register
1E	0	1	1	1	1	Sending ASYNC resp param setting register	Receiving ASYNC resp param display register
20	1	0	0	0	0	Sending ASYNC des offset setting register (high)	Receiving ASYNC des offset display register (high)
22	1	0	0	0	1	Sending ASYNC des offset setting register (middle)	Receiving ASYNC des offset display register (middle)
24	1	0	0	1	0	Sending ASYNC des offset setting register (low)	Receiving ASYNC des offset display register (low)
26	1	0	0	1	1	(reserved)	←
28	1	0	1	0	0	(reserved)	PHY ID display register
2A	1	0	1	0	1	(reserved)	NODE config display register
2C	1	0	1	1	0	(reserved)	PORT config display register (port0)
2E	1	0	1	1	1	(reserved)	PORT config display register (port1)
30	1	1	0	0	0	state clear setting register	root ID display register
32	1	1	0	0	1	Self ID PKT param setting register	ISO resource manager ID display register
34	1	1	0	1	0	(reserved)	←
36	1	1	0	1	1	(reserved)	←
38	1	1	1	0	0	(reserved)	cycle timer monitor display register (high)
3A	1	1	1	0	1	(reserved)	cycle timer monitor display register (low)
3C	1	1	1	1	0	(reserved)	←

3. Bank 1 Registers

Bank 1 contains the registers required for AV/C (MPEG, DVC) protocols.

Access to this bank is enabled by writing ‘0001h’ to the bank select register (3Eh).

Address						Write operation	Read operation
HEX	A5	A4	A3	A2	A1		
10	0	1	0	0	0	Sending time stamp offset setting register	Receiving time stamp display register (high)
12	0	1	0	0	1	Sending time stamp offset setting register	Receiving time stamp display register (low)
14	0	1	0	1	0	Sending CIP header setting register (highest)	Receiving CIP header display register (highest)
16	0	1	0	1	1	Sending CIP header setting register (high)	Receiving CIP header display register (high)
18	0	1	1	0	0	Sending CIP header setting register (low)	Receiving CIP header display register (low)
1A	0	1	1	0	1	Sending CIP header setting register (lowest)	Receiving CIP header display register (lowest)
1C	0	1	1	1	0	OMPR (high)	←
1E	0	1	1	1	1	OMPR (low)	←
20	1	0	0	0	0	OPCR0 (high)	←
22	1	0	0	0	1	OPCR0 (low)	←
24	1	0	0	1	0	(reserved)	←
26	1	0	0	1	1	(reserved)	←
28	1	0	1	0	0	(reserved)	←
2A	1	0	1	0	1	(reserved)	←
2C	1	0	1	1	0	IMPR (high)	←
2E	1	0	1	1	1	IMPR (low)	←
30	1	1	0	0	0	IPCR0 (high)	←
32	1	1	0	0	1	IPCR0 (low)	←
34	1	1	0	1	0	(reserved)	←
36	1	1	0	1	1	(reserved)	←
38	1	1	1	0	0	(reserved)	←
3A	1	1	1	0	1	(reserved)	←
3C	1	1	1	1	0	AV mode setting register	AV status register

4. Bank 2 Registers

Bank 2 contains CSR's.

Access to this bank is enabled by writing '0002h' to the bank select register (3Eh).

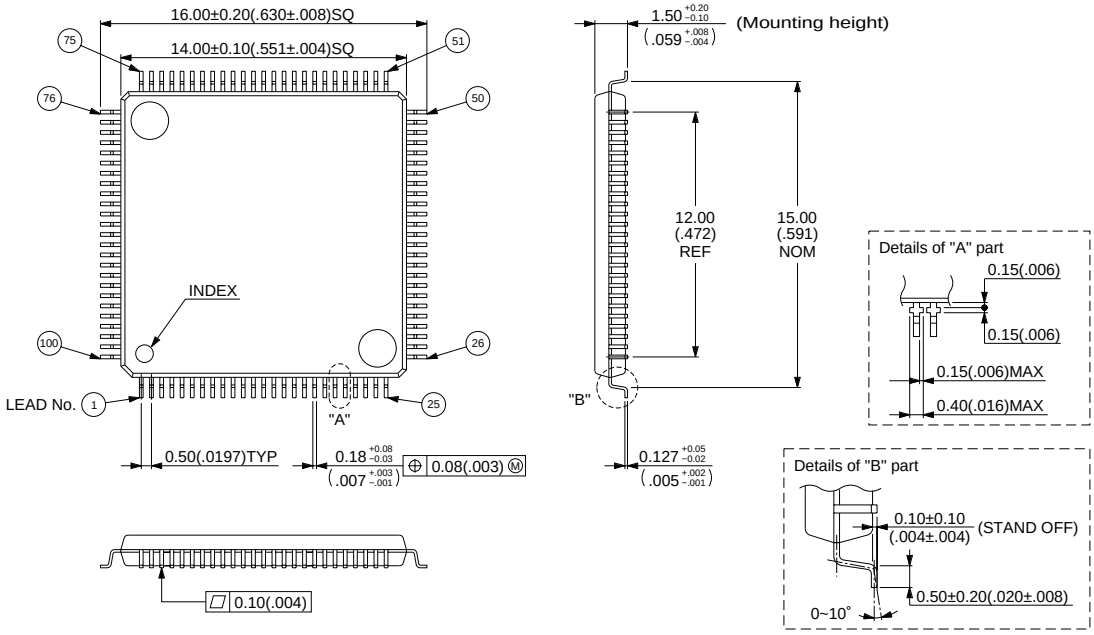
Address						Write operation	Read operation
HEX	A5	A4	A3	A2	A1		
10	0	1	0	0	0	bus manager ID register (high)	←
12	0	1	0	0	1	bus manager ID register (low)	←
14	0	1	0	1	0	bandwidth available register (high)	←
16	0	1	0	1	1	bandwidth available register (low)	←
18	0	1	1	0	0	channels available high register (high)	←
1A	0	1	1	0	1	channels available high register (low)	←
1C	0	1	1	1	0	channels available low register (high)	←
1E	0	1	1	1	1	channels available low register (low)	←
20	1	0	0	0	0	(reserved)	←
22	1	0	0	0	1	(reserved)	←
24	1	0	0	1	0	(reserved)	←
26	1	0	0	1	1	(reserved)	←
28	1	0	1	0	0	(reserved)	←
2A	1	0	1	0	1	(reserved)	←
2C	1	0	1	1	0	(reserved)	←
2E	1	0	1	1	1	(reserved)	←
30	1	1	0	0	0	(reserved)	←
32	1	1	0	0	1	(reserved)	←
34	1	1	0	1	0	(reserved)	←
36	1	1	0	1	1	(reserved)	←
38	1	1	1	0	0	(reserved)	←
3A	1	1	1	0	1	(reserved)	←
3C	1	1	1	1	0	(reserved)	←

■ ORDERING INFORMATION

Partnumber	Package	Remarks
MB86612PFV	100-pin plastic LQFP (FPT-100P-M05)	
MB86612PBT	120-pin plastic FBGA (BGA-120P-M01)	

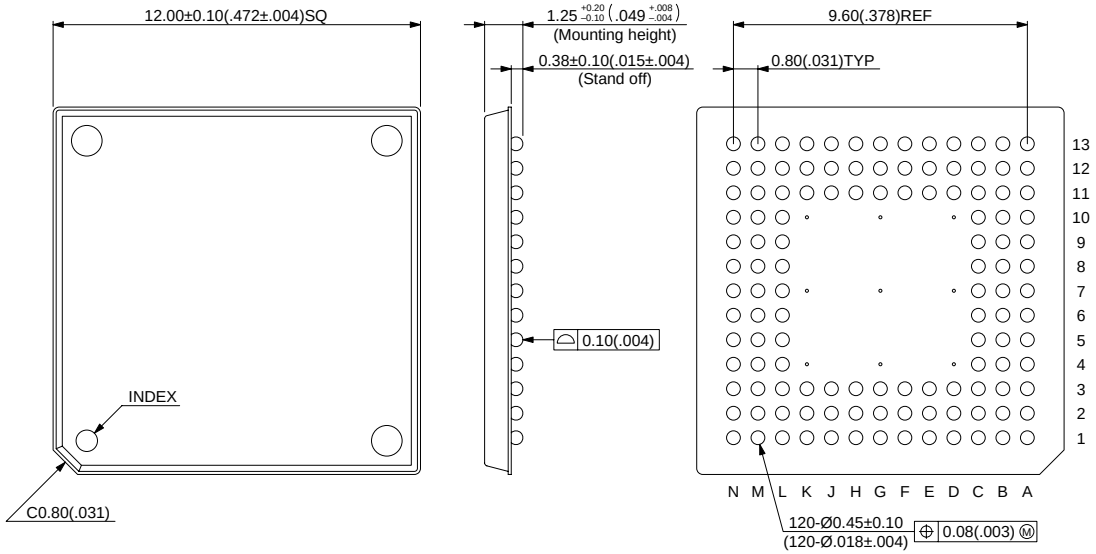
■ PACKAGE DIMENSIONS

100-pin plastic LQFP
(FPT-100P-M05)



Dimensions in mm (inches)

120-pin plastic FBGA
(BGA-120P-M01)



Dimensions in mm (inches)

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