FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-05309-3E

Microprocessor SPARClite

CMOS

32-bit Embedded Controller

MB86830 Series

MB86831/832/833/834/835/836

■ DESCRIPTION

The MB86830 series is a SPARClite *1 series of RISC architecture processors, providing high performance for a variety of embedded applications. Conforming to the SPARC *2 architecture, the MB86830 series is upward code-compatible with the conventional products in the SPARClite family. When running at 100 MHz, the MB86830 series provides performance of 121 VAX-MIPS.

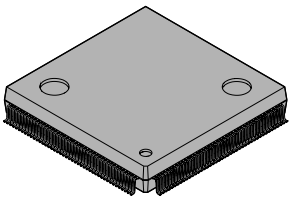
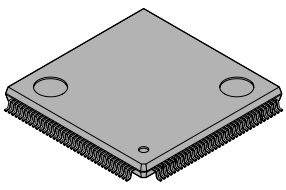
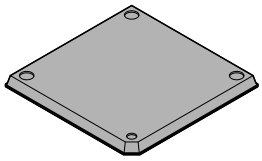
The MB86830 series has on-chip data and instruction caches, allowing the processor to operate independently of the wait time for external memory. The independent instruction bus and internal data bus serve as high-bandwidth interfaces between the IU (integer unit) and caches. The MB86830 series also contains an internal multiplier circuit that facilitates interfacing with external devices, thereby providing high performance with continuous cache hits. The DRAM controller supports both of EDO and fast-page mode DRAMs. The interrupt controller (IRC) supports eight channels of interrupts, allowing a trigger mode and mask to be set for each of the channels. To get the most out of the system with a minimum number of external circuits, the MB86830 series supports chip select output, programmable wait state generator, and page mode DRAM interfaces.

The combination of these features of the MB86830 series achieves high levels of speed, flexibility, and efficiency, making it a line of ideal controllers for a variety of low-cost, high-performance embedded systems.

*1 : SPARClite is a trademark of SPARC International, Inc. in the United States.
Fujitsu Microelectronics, Inc. has been granted permission to use the trademark.

*2 : SPARC is a registered trademark of SPARC International, Inc. in the United States.
SPARC is based on technology developed by Sun Microsystems, Inc.

■ PACKAGE

176-pin plastic QFP MB86831/832/834	144-pin plastic LQFP MB86833/835/836	144-pin plastic FBGA MB86836
		
(FPT-176P-M01)	(FPT-144P-M08)	(BGA-144P-M02)

■ FEATURES

- IU (integer unit)
  Maximum operating frequency : 120 MHz
  SPARC architecture V8E conforming
  With 32-bits general register :136 / register window : 8
- Instruction cash
  The entry lock function is supported
- Data cache
  No cash controlling function supported
  The entry lock function is supported
- BIU (bus interface unit)
  Purifetchi baffa :1
  Write buffer :4
  The burst mode is supported
  Programmable chip selection function :6
  Programmable weight state control :6
  For 8/16/32-bits bus
  Automatic insertion function of idling cycle after ROM region is accessed
  For burst mode ROM
- With internal clock multiplication circuit
- Sleep mode (low power consumption mode) supported
- With DRAM controller (except on the MB86836)
- With interrupt request controller (IRC)
- On-chip general-purpose 16-bit timer (MB86836 only):1 channel (equivalent to the MB86942)
- Support for the JTAG test port (MB86836 only)

■ PRODUCT LINEUP

Item \ Part number	MB86831	MB86832	MB86833	MB86834	MB86835	MB86836
CPU maximum frequency (MHz)	66/80	66/80/100	66	108/120	84	90/108*1
BUS maximum frequency (MHz)	40		33	40		
Ancillary Version Register	$(0000)_{16}$	$(0001)_{16}$	$(0002)_{16}$	$(0003)_{16}$	$(0004)_{16}$	$(0001)_{16}$
Instruction cache	4 KB/2 way	8 KB/2 way	1 KB/Direct	16 KB/2 way	4 KB/2 way	8 KB/2 way
Data cache	2 KB/2 way	8 KB/2 way	1 KB/Direct	16 KB/2 way	2 KB/2 way	8 KB/2 way
Cache size change function	No	8/4/2/1 KB selectable	No			
ADR pin	ADR<27:2>		ADR<23:2>	ADR<27:2>	ADR<23:2>	
ADR enhancement (ASISEL)	No	ADR<31:2>	ADR<27:2>	ADR<31:2>	ADR<27:2>	
Clock gear function	No	Yes				
DSU	No	Yes	No	Yes	No	
DRAM controller	4bank		1bank	4bank	1bank	No
JTAG test port	No					Yes
General porpose 16-bit timer*2	No					1ch
Internal pull-up/down resister pin	P63	P63, P162 to P164	No			P41 to P44, P79
Internal power supply (V_{DD3})	3.3 V			2.5 V	3.3 V	2.5 V
I/O power supply (V_{DD5})	3.3 V to 5.0 V			3.3 V		
Package	SQFP176 FPT-176P-M01 24 × 24 mm		LQFP144 FPT-144P-M08 20 × 20 mm	SQFP176 FPT-176P-M01 24 × 24 mm	LQFP144 FPT-144P-M08 20 × 20 mm	LQFP144 FPT-144P-M08 20 × 20 mm FBGA144 BGA-144P-M02 12 × 12 mm

*1:MB86836 108 MHz version is under developement.

*2: The general-purpose timer on the MB86836 is a subset of the prescaler-integrated 16-bit timer on the MB86942. For the type supporting only the internal clock mode, refer to the document for the MB86941/942.

■ FOR PACKAGE AND PART NUMBER

Package	MB86831	MB86832	MB86833	MB86834	MB86835	MB86836
FPT-176P-M01	Yes	Yes	No	Yes	No	No
FPT-144P-M08	No	No	Yes	No	Yes	Yes
BGA-144P-M02	No	No	No	No	No	Yes

Note:Refer to“PACKAGE DIMENSIONS” for details in each package.

■ DIFFERENCES

1.Package

- MB86831/832/834 : QFP176
- MB86833/835/836 : LQFP144
- MB86836 : FBGA144

2.Pin array

- MB86831/832/834 : The pin is interchangeable.However, the terminal of MB86834 is the pull-up resistor none.
- MB86833/835 : The pin is interchangeable.
- MB86836 : MB86833/835, from which DRAMC related pins are deleted and to which one channel of general-purpose 16-bit timer and the JTAG pin are added.

3.Maximum operation frequency

- MB86831 : 66MHz/80MHz
- MB86832 : 66MHz/80MHz/100MHz
- MB86833 : 66MHz
- MB86834 : 108MHz/120MHz
- MB86835 : 84MHz
- MB86836 : 90MHz/108MHz

4.Power-supply voltage

Power-supply voltage	MB86831	MB86832	MB86833	MB86834	MB86835	MB86836
Internal power-supply voltage	3.3 V			2.5 V	3.3 V	2.5 V
I/O power-supply voltage	3.3 V or 5.0 V			3.3 V	3.3 V	3.3 V

* : The power-supply voltage is different (Refer to “ELECTRIC CHARACTERISTICS”) depending on the condition of the operation frequency.

5.Cache memory

Cache memory	MB86831	MB86832	MB86833	MB86834	MB86835	MB86836
Instruction cash	4 KB/2 way	8 KB/2 way	1 KB/Direct	16 KB/2 way	4 KB/2 way	8 KB/2 way
Data cash	2 KB/2 way	8 KB/2 way	1 KB/Direct	16 KB/2 way	2 KB/2 way	8 KB/2 way

6.Register

Register name	MB86831/832/833/835/836	MB86834
Instruction Cache Invalidate Register (ICINVLD)	Map of ASI = 0x0c, ADR = 0x00001000(Bank1) ASI = 0x0c, ADR = 0x80001000(Bank2)	Map of ASI = 0x0c, ADR = 0x00008000(Bank1) ASI = 0x0c, ADR = 0x80008000(Bank2)
Data Cache Invalidate Register (DCINVLD)	Map of ASI = 0x0e, ADR = 0x00001000(Bank1) ASI = 0x0e, ADR = 0x80001000(Bank2)	Map of ASI = 0x0e, ADR = 0x00008000(Bank1) ASI = 0x0e, ADR = 0x80008000(Bank2)

Register name	MB86831	MB86832	MB86833	MB86834	MB86835	MB86836
Ancillary Version Register (VER2)	$(00)_{16}$	$(01)_{16}$	$(02)_{16}$	$(03)_{16}$	$(04)_{16}$	$(01)_{16}$

7.Clock gear

- MB86832/833/834/835/836 : Supported
- MB86831 : No supported

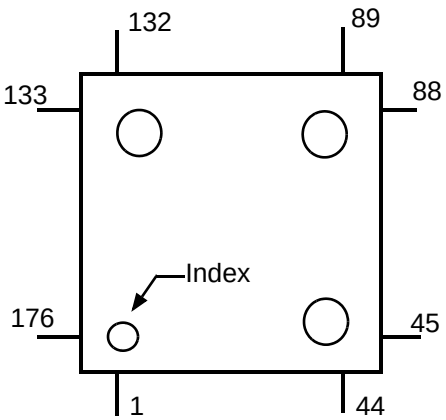
8.External signal

Item	MB86831	MB86832	MB86833	MB86834	MB86835	MB86836
ASISEL pin function	No	Multiplex of ADR<31:28> and ASI<3:0>	Multiplex of ADR<27:24> and ASI<3:0>	Multiplex of ADR<31:28> and ASI<3:0>	Multiplex of ADR<27:24> and ASI<3:0>	
DSU (debugging support unit)	No	Yes	No	Yes	No	
DRAM controller	4Bank supported	4Bank supported	1Bank supported*	4Bank supported	1Bank supported*	No
General-purpose 16-bit timer	No					Wih 1ch. prescaler (Equivalent to MB86942)
JTAG	No					Support
Pull-up resistor or pull-down resistor	Inclusion	Inclusion	No			Inclusion

*:RAS1# to RAS3# and DWE1# to DWE3# deletion.

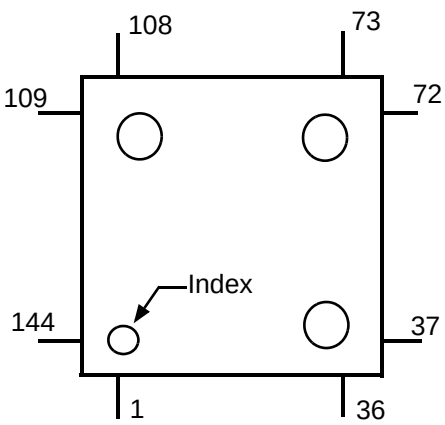
■ PIN ASSIGNMENT

(TOP VIEW)



(FPT-176P- M01)

(TOP VIEW)



(FPT-144P-M08)

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	144	143	141	138	134	130	126	123	119	115	111	109	108
B	1	2	142	139	135	131	127	122	118	114	112	110	107
C	3	4	5	140	136	132	128	124	120	116	113	106	105
D	7	6	8	9	137	133	129	125	121	117	104	103	102
E	11	10	12	13						101	100	99	98
F	15	14	16	17						97	96	95	94
G	18	19	20	21						93	92	91	90
H	22	23	24	25						89	88	86	87
J	26	27	28	29						85	84	82	83
K	30	31	32	45	49	53	57	61	65	81	80	78	79
L	33	34	41	44	48	52	56	60	64	68	77	76	75
M	35	38	40	42	46	50	55	59	63	67	70	74	73
N	36	37	39	43	47	51	54	58	62	66	69	71	72

GND : 12

V_{DD5} (V_{DD1}) ; I/O power supply : 8

V_{DD3} (V_{DD2}) ; Internal power supply : 8

(BGA-144P- M02)

- MB86831/832/834

Pin no.	Pin symbol	Pin no.	Pin symbol	Pin no.	Pin symbol	Pin no.	Pin symbol	Pin no.	Pin symbol
1	V_{DD3}	37	D<4>	73	BMREQ#	109	ADR<11>	145	FLOAT#
2	D<31>	38	BMODE8#	74	OVF#	110	READY#	146	PDOWN#
3	D<30>	39	V_{SS}	75	SAMEPAGE#	111	V_{DD3}	147	WKUP#
4	D<29>	40	D<3>	76	AS#	112	ADR<12>	148	RESET#
5	D<28>	41	D<2>	77	V_{DD3}	113	ADR<13>	149	V_{SS}
6	V_{SS}	42	D<1>	78	RDWR#	114	ADR<14>	150	IDLEEN
7	BMODE16#	43	D<0>	79	RDYOUT#	115	ADR<15>	151	CLKSEL1
8	D<27>	44	V_{DD3}	80	CS5#	116	V_{SS}	152	CLKSEL0
9	D<26>	45	V_{SS}	81	CS4#	117	ADR<16>	153	CLKEXT
10	D<25>	46	DWE3#	82	V_{DD5}	118	ADR<17>	154	CLKIN
11	D<24>	47	DWE2#	83	V_{SS}	119	ADR<18>	155	V_{DD5}
12	V_{DD5}	48	DWE1#	84	CS3#	120	ADR<19>	156	IRQ11
13	D<23>	49	DWE0#	85	CS2#	121	V_{DD5}	157	IRQ10
14	D<22>	50	V_{SS}	86	CS1#	122	ADR<20>	158	IRQ9
15	D<21>	51	V_{DD5}	87	CS0#	123	ADR<21>	159	IRQ8
16	D<20>	52	RAS0#	88	V_{SS}	124	ADR<22>	160	V_{SS}
17	V_{SS}	53	RAS1#	89	V_{DD3}	125	ADR<23>	161	Reserved
18	D<19>	54	RAS2#	90	BE3#	126	MEXC#	162	[ASISEL *]
19	D<18>	55	RAS3#	91	BE2#	127	V_{SS}	163	[EMUBRK# *]
20	D<17>	56	V_{DD3}	92	BE1#	128	ADR<24>	164	[EMUENB# *]
21	D<16>	57	CAS0#	93	BE0#	129	ADR<25>	165	V_{DD3}
22	BTEST#	58	CAS1#	94	V_{SS}	130	ADR<26>	166	[EMUSD3]
23	V_{DD3}	59	CAS2#	95	NONCACHE#	131	ADR<27>	167	[EMUSD2]
24	D<15>	60	CAS3#	96	Reserved	132	V_{DD3}	16	[EMUSD1]
25	D<14>	61	V_{SS}	97	Reserved	133	V_{SS}	169	[EMUSD0]
26	D<13>	62	DOE#	98	ADR<2>	134	ASI<3>[/ADR<28>]	170	V_{DD5}
27	D<12>	63	CLKSEL2 *	99	ADR<3>	135	ASI<2>[/ADR<29>]	171	V_{SS}
28	V_{SS}	64	ERROR#	100	V_{DD5}	136	ASI<1>[/ADR<30>]	172	[EMUD3]
29	D<11>	65	LOCK#	101	ADR<4>	137	ASI<0>[/ADR<31>]	173	[EMUD2]
30	D<10>	66	CTEST#	102	ADR<5>	138	V_{SS}	174	[EMUD1]
31	D<9>	67	V_{DD5}	103	ADR<6>	139	V_{DD5}	175	[EMUD0]
32	D<8>	68	BREQ#	104	ADR<7>	140	IRL<3>/IRQ15	176	V_{SS}
33	V_{DD5}	69	PBREQ#	105	V_{SS}	141	IRL<2>/IRQ14		
34	D<7>	70	BGRNT#	106	ADR<8>	142	IRL<1>/IRQ13		
35	D<6>	71	BMACK#	107	ADR<9>	143	IRL<0>/IRQ12		
36	D<5>	72	V_{SS}	108	ADR<10>	144	V_{DD3}		

V_{DD3} :For internal power supply.
V_{DD5} :For I/O power supply.
Reserved:This pin must be open.
*:The pull-up resistor is built into. However, there is no pull-up resistor in MB86834.
[ ]:Pin is added with MB86832/834. Please use this terminal by the opening in case of MB86831-66 and 80.

- MB86833/835

Pin no.	Pin symbol	Pin no.	Pin symbol	Pin no.	Pin symbol	Pin no.	Pin symbol
1	V_{DD3}	37	V_{DD3}	73	V_{DD3}	109	V_{DD3}
2	BMODE16#	38	D<2>	74	BE3#	110	MEXC#
3	D<28>	39	D<1>	75	BE2#	111	ADR<23>
4	D<27>	40	D<0>	76	BE1#	112	ASI<3>/ADR<24>
5	D<26>	41	DWE0#	77	BE0#	113	ASI<2>/ADR<25>
6	D<25>	42	RAS0#	78	Reserved	114	ASI<1>/ADR<26>
7	D<24>	43	CAS0#	79	Reserved	115	ASI<0>/ADR<27>
8	D<23>	44	CAS1#	80	NONCACHE#	116	IRL<3>/IRQ15
9	V_{SS}	45	V_{SS}	81	V_{SS}	117	V_{SS}
10	D<22>	46	CAS2#	82	ADR<2>	118	IRL<2>/IRQ14
11	D<21>	47	CAS3#	83	ADR<3>	119	IRL<1>/IRQ13
12	D<20>	48	DOE#	84	ADR<4>	120	IRL<0>/IRQ12
13	D<19>	49	ERROR#	85	ADR<5>	121	FLOAT#
14	D<18>	50	LOCK#	86	ADR<6>	122	PDOWN#
15	D<17>	51	CTEST#	87	ADR<7>	123	WKUP#
16	D<16>	52	BREQ#	88	ADR<8>	124	RESET#
17	BTEST#	53	PBREQ#	89	ADR<9>	125	IDLEEN
18	V_{DD5}	54	V_{DD5}	90	V_{DD5}	126	V_{DD5}
19	V_{SS}	55	V_{SS}	91	V_{SS}	127	V_{SS}
20	D<15>	56	BGRNT#	92	ADR<10>	128	CLKSEL2
21	D<14>	57	BMACK#	93	ADR<11>	129	CLKSEL1
22	D<13>	58	BMREQ#	94	ADR<12>	130	CLKSEL0
23	D<12>	59	OVF#	95	ADR<13>	131	CLKEXT
24	D<11>	60	SAMEPAGE#	96	ADR<14>	132	CLKIN
25	D<10>	61	AS#	97	ADR<15>	133	IRQ11
26	D<9>	62	RDWR#	98	ADR<16>	134	IRQ10
27	D<8>	63	RDYOUT#	99	ADR<17>	135	IRQ9
28	BMODE8#	64	CS5#	100	READY#	136	IRQ8
29	V_{DD3}	65	V_{DD3}	101	V_{DD3}	137	V_{DD3}
30	V_{SS}	66	V_{SS}	102	V_{SS}	138	V_{SS}
31	D<7>	67	CS4#	103	ADR<18>	139	Reserved
32	D<6>	68	CS3#	104	ADR<19>	140	ASISEL
33	D<5>	69	CS2#	105	ADR<20>	141	D<31>
34	D<4>	70	CS1#	106	ADR<21>	142	D<30>
35	D<3>	71	CS0#	107	ADR<22>	143	D<29>
36	V_{DD5}	72	V_{DD5}	108	V_{DD5}	144	V_{DD5}

V_{DD3} :For internal power supply.
V_{DD5} :For I/O power supply.
Reserved:This pin must be open.

• MB86836

Pin no.	Pin symbol	Pin no.	Pin symbol	Pin no.	Pin symbol	Pin no.	Pin symbol
1	V_{DD3}	37	V_{DD3}	73	V_{DD3}	109	V_{DD3}
2	BMODE16#	38	D<2>	74	BE3#	110	MEXC#
3	D<28>	39	D<1>	75	BE2#	111	ADR<23>
4	D<27>	40	D<0>	76	BE1#	112	ASI<3>/ADR<24>
5	D<26>	41	TRST#	77	BE0#	113	ASI<2>/ADR<25>
6	D<25>	42	TCK*	78	VPD	114	ASI<1>/ADR<26>
7	D<24>	43	TMS*	79	IN0	115	ASI<0>/ADR<27>
8	D<23>	44	TDI*	80	NONCACHE#	116	IRL<3>/IRQ15
9	V_{SS}	45	V_{SS}	81	V_{SS}	117	V_{SS}
10	D<22>	46	TDO	82	ADR<2>	118	IRL<2>/IRQ14
11	D<21>	47	OUT0	83	ADR<3>	119	IRL<1>/IRQ13
12	D<20>	48	PRSCK0	84	ADR<4>	120	IRL<0>/IRQ12
13	D<19>	49	ERROR#	85	ADR<5>	121	FLOAT#
14	D<18>	50	LOCK#	86	ADR<6>	122	PDOWN#
15	D<17>	51	CTEST#	87	ADR<7>	123	WKUP#
16	D<16>	52	BREQ#	88	ADR<8>	124	RESET#
17	BTEST#	53	PBREQ#	89	ADR<9>	125	IDLEEN
18	V_{DD5}	54	V_{DD5}	90	V_{DD5}	126	V_{DD5}
19	V_{SS}	55	V_{SS}	91	V_{SS}	127	V_{SS}
20	D<15>	56	BGRNT#	92	ADR<10>	128	CLKSEL2
21	D<14>	57	BMACK#	93	ADR<11>	129	CLKSEL1
22	D<13>	58	BMREQ#	94	ADR<12>	130	CLKSEL0
23	D<12>	59	OVF#	95	ADR<13>	131	CLKEXT
24	D<11>	60	SAMEPAGE#	96	ADR<14>	132	CLKIN
25	D<10>	61	AS#	97	ADR<15>	133	IRQ11
26	D<9>	62	RDWR#	98	ADR<16>	134	IRQ10
27	D<8>	63	RDYOUT#	99	ADR<17>	135	IRQ9
28	BMODE8#	64	CS5#	100	READY#	136	IRQ8
29	V_{DD3}	65	V_{DD3}	101	V_{DD3}	137	V_{DD3}
30	V_{SS}	66	V_{SS}	102	V_{SS}	138	V_{SS}
31	D<7>	67	CS4#	103	ADR<18>	139	Reserved
32	D<6>	68	CS3#	104	ADR<19>	140	ASISEL
33	D<5>	69	CS2#	105	ADR<20>	141	D<31>
34	D<4>	70	CS1#	106	ADR<21>	142	D<30>
35	D<3>	71	CS0#	107	ADR<22>	143	D<29>
36	V_{DD5}	72	V_{DD5}	108	V_{DD5}	144	V_{DD5}

V_{DD3} : 2.5-V power pin (for supplying internal power)
V_{DD5} : 3.3-V power pin (for supplying I/O power)
Reserved : Leave the pin open.

VPD: Test pin. Usually fixed to the L level.
* : With an internal pull-down resistor

■ PIN DESCRIPTION

1. CPU Core Related Pins

<table>
<tr><th>Symbol</th><th>Pin name</th><th>I/O</th><th>Function</th></tr>
<tr><td>CLKIN</td><td>CLOCK</td><td>I</td><td>Clock input pin.
The clock regulates external bus operation.The bus AC characteristics are determined based on the clock.</td></tr>
<tr><td>CLKEXT</td><td>EXTERNAL CLOCK BYPASS</td><td>I</td><td>External clock select pin.
The “L” level at this pin selects the clock signal generated by the internal PLL circuit; theC“H” level selects the external clock signal (input through the CLKIN pin) as it is.Fix this pin usually at the “L” level.</td></tr>
<tr><td>RESET#</td><td>SYSTEM RESET</td><td>I</td><td>Reset input.
The “L” input to this pin initializes the CPU.</td></tr>
<tr><td>CLKSEL0
CLKSEL1
CLKSEL2</td><td>INTERNAL CLOCK SELECT</td><td>I</td><td>Internal clock setting pins.
These pins are used to set the IU (integer unit) and cache operating clock frequencies to x1, x2, x3, x4, or x5 of the external clock frequency.
<table>
<tr><th>CLKSEL2</th><th>CLKSEL1</th><th>CLKSEL0</th><th>Internal clock</th></tr>
<tr><td>H</td><td>L</td><td>L</td><td>×1</td></tr>
<tr><td>H</td><td>L</td><td>H</td><td>×2</td></tr>
<tr><td>H</td><td>H</td><td>L</td><td>×3</td></tr>
<tr><td>H</td><td>H</td><td>H</td><td>×4</td></tr>
<tr><td>L</td><td>H</td><td>H</td><td>×5</td></tr>
</table>
Any other setting is prohibited.</td></tr>
<tr><td>ASISEL</td><td>ADDRESS SPACE IDENTI-FIERS SELECT</td><td>I</td><td>ASI select signal
This pin selects the ASI or ADR pin.
Setting this pin to “L” prohibits the “L” input to the AS# pin in the bus grant state.
On the MB86832, this pin is pulled up with a resistor of about 50 kΩ.
<table>
<tr><th>ASISEL</th><th>MB86832/834
ASI<3:0>/ADR<28:31></th><th>MB86833/835/836
ASI<3:0>/ADR<24:27></th></tr>
<tr><td>L</td><td>ADR<28:31></td><td>ADR<24:27></td></tr>
<tr><td>H</td><td>ASI<3:0></td><td>ASI<3:0></td></tr>
</table></td></tr>
<tr><td>CTEST#
BTEST#</td><td>CTEST
BTEST</td><td>I</td><td>Test pins.
Fix these pins usually to the “H” level.</td></tr>
<tr><td>ADR<27:2>
or
ADR<23:2>
(MB86833/
835/836)</td><td>ADDRESS BUS</td><td>I/O</td><td>Address pin.
The ADR<27:2>pin (ADR<23:2>pin on the MB86833/835/836)handles the signal for identifying an instruction address or data address.For using the 8/16-bit bus width, ADR<1> and ADR<0> are output multiplexed with BE2# and BE3#, respectively.This pin remains enabled during the bus cycle; the value output during the idle cycle is not guaranteed.
In the bus grant state, the pin serves as an input used, e.g., by the CS generator circuit (while the “L” input to the AS# pin is prohibited with the ASISEL pin at the “L” level) and ADR<31:28> (ADR<31:24> on the MB86833/835/836) is handled internally as 0.</td></tr>
</table>

(Continued)

(Continued)

<table>
<tr><th>Symbol</th><th>Pin name</th><th>I/O</th><th>Function</th></tr>
<tr><td>D<31:0></td><td>DATA BUS</td><td>I/O</td><td>Data bus signal.
This pin provides a bidirectional data bus used for instruction fetch, data load, and data store operations. Instructions and word data must be aligned at addresses which are multiples of the number 4.
Half words and double words must be aligned at addresses which are multiples of the numbers 2 and 8, respectively. D<7:0> and D<15:0> are used in the 8-bit and 16-bit bus modes, respectively. For use in the 16-bit bus mode, a pull-up resistor must be connected to the data bus which is not used (D<31:8> for the 8-bit bus and D<31:16> for the 16-bit bus).</td></tr>
<tr><td>AS#</td><td>ADDRESS STROBE</td><td>I/O</td><td>Address strobe signal.
This pin outputs the “L” level signal for the first bus cycle. Basically, the bus cycle starts with the AS# signal asserted and ends up with the READY# or RDYOUT# signal asserted.
In the bus grant state, the pin serves as an input used for the signals to actuate the CS generator and wait state generator circuits.</td></tr>
<tr><td>RDWR#</td><td>READ/WRITE BUS TRANSACTION</td><td>I/O</td><td>Read/write signal.
This pin outputs the “L” level signal when the current bus cycle is the write cycle or the “H” level signal when it is the read or idle cycle. The output level remains at “H” or“L” during the entire bus cycle from the beginning to end.
In the bus grant state, the pin serves as an input used for generating the DWE0#-DWE3# and DOE# signals to enable the DRAM controller. The signal at this pin is not used when the DRAM controller is disabled.</td></tr>
<tr><td>BE0#
BE1#
BE2#
BE3#</td><td>BYTE ENABLE</td><td>O
O
I/O
O</td><td>Bye enable signals.
These pins are used to indicate the bytes valid for in write mode when the 32-bit bus width is used.
In read mode, all of the BE0# to BE3# signals are asserted regardless of the data type. For the 8-bit or 16-bit bus width, the BE2# and BE3# pins output ADR<1> and ADR<0>, respectively.
The BE0# to BE3# pins remain enabled during the bus cycle; the output level during the idle cycle is not guaranteed.
In the bus grant state, the pins enter the High-Z state and, only when the DRAM controller is on with the 16-bit bus width used, the BE2# pin serves as the ADR<1> input pin.
<table>
<tr><th>Width of bus</th><th colspan="2">Access type</th><th>BE0#</th><th>BE1#</th><th>BE2#</th><th>BE3#</th></tr>
<tr><td rowspan="8">Width of 32-bits bus</td><td rowspan="7">Write</td><td>Byte-0 (D<31:24>) *</td><td>0</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>Byte-1 (D<23:16>)</td><td>1</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>Byte-2 (D<15:8>)</td><td>1</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>Byte-3 (D<7:0>)</td><td>1</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>Half word-0(D<31:16>)</td><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>Half word-1(D<15:0>)</td><td>1</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>Word</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>Read</td><td>All data types</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
</table>
(Continued)</td></tr>
</table>

(Continued)

(Continued)

<table>
<tr><th>Symbol</th><th>Pin name</th><th>I/O</th><th>Function</th></tr>
<tr><td>BE0#
BE1#
BE2#
BE3#</td><td>BYTE ENABLE</td><td>O
O
I/O
O</td><td>(Continued)
<table>
<tr><th>Width of bus</th><th colspan="2">Access type</th><th>BE0#</th><th>BE1#</th><th>BE2#</th><th>BE3#</th></tr>
<tr><td rowspan="10">Width of 16-bits bus</td><td rowspan="8">Write</td><td>Byte-0 (D<15:8>)</td><td>1</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>Byte-1 (D<7:0>)</td><td>0</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>Byte-2 (D<15:8>)</td><td>1</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>Byte-3 (D<7:0>)</td><td>0</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>Half word-0 (D<15:0>)</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>Half word-1 (D<15:0>)</td><td>0</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>Word (D<15:0>) access-0</td><td>0</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>Word (D<15:0>)access-1</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td rowspan="2">Read</td><td>Access-0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>Access-1</td><td>0</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td rowspan="18">Width of 8-bits bus</td><td rowspan="13">Write</td><td>Byte-0</td><td>X</td><td>X</td><td>0</td><td>0</td></tr>
<tr><td>Byte-1</td><td>X</td><td>X</td><td>0</td><td>1</td></tr>
<tr><td>Byte-2</td><td>X</td><td>X</td><td>1</td><td>0</td></tr>
<tr><td>Byte-3</td><td>X</td><td>X</td><td>1</td><td>1</td></tr>
<tr><td>Half word-0 access-1</td><td>X</td><td>X</td><td>0</td><td>1</td></tr>
<tr><td>Half word-0 access-0</td><td>X</td><td>X</td><td>0</td><td>0</td></tr>
<tr><td>Half word-1 access-0</td><td>X</td><td>X</td><td>1</td><td>1</td></tr>
<tr><td>Half word-1 access-1</td><td>X</td><td>X</td><td>1</td><td>0</td></tr>
<tr><td>word access-0</td><td>X</td><td>X</td><td>1</td><td>1</td></tr>
<tr><td>word access-1</td><td>X</td><td>X</td><td>1</td><td>0</td></tr>
<tr><td>word access-2</td><td>X</td><td>X</td><td>0</td><td>1</td></tr>
<tr><td>word access-3</td><td>X</td><td>X</td><td>0</td><td>0</td></tr>
<tr><td rowspan="5">Read</td><td>Access-0</td><td>X</td><td>X</td><td>0</td><td>0</td></tr>
<tr><td>Access-1</td><td>X</td><td>X</td><td>0</td><td>1</td></tr>
<tr><td>Access-2</td><td>X</td><td>X</td><td>1</td><td>0</td></tr>
<tr><td>Access-3</td><td>X</td><td>X</td><td>1</td><td>1</td></tr>
</table>
* : The mark such as (D<31:24>) shows the bit of the data bus used.</td></tr>
<tr><td>CS0#
CS1#
CS2#
CS3#
CS4#
CS5#</td><td>CHIP SELECT</td><td>O</td><td>Chip select signals.
These chip select signals are asserted when the Address Range Specifier Register (ARSR) and Address Mask Register (AMR) is accessed with the CS Enable bit (bit 4) in the System Support Control Register (SSCR) set to “1.” (Note, however, that only the CS0# pin is independent of the CS Enable bit.)</td></tr>
</table>

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Symbol	Pin name	I/O	Function
BREQ#	BUS REQUEST	I	Bus request signal. When the BREQ# signal is asserted by external bus mastering, the CPU releases the bus as shown below upon termination of the current bus cycle: (1)When executing the Atomic Load Store instruction, the CPU releases the bus after completing both of loading and storing. (2)When loading or storing a double word: If the BREQ# signal is asserted at the first word, the CPU releases the bus after transfer of the first word. If the BREQ# signal is asserted in the bus cycle for the second word, the CPU releases the bus after transfer of the second word. (3)When storing data at the 8/16-bit bus width: The CPU releases the bus after transfer of that size of data which is handled by the instruction (for example, after writing 8-bit data four times when storing word data using an 8-bit bus). (4)When loading data at the 8/16-bit bus width: The CPU releases the bus after transfer of one word. When the ASISEL pin is at the “L” level, the “L” input to the AS# pin is prohibited in the bus grant state.
BGRNT#	BUS GRANT	O	Bus grant signal. Upon reception of a bus request (BREQ#), the BGRNT# signal is asserted to notify the external device of the bus released status.
IRL3 IRL2 IRL1 IRL0	INTERRUPT REQUEST LEVEL	I	Interrupt input pins. These pins are used to input an encoded interrupt level. They handle a group of asynchronous input signals, notifying the IU (integer unit) of an interrupt level only when the same level is detected twice at the fall of an external clock pulse. IRL = 0000_{2} and IRL = $1111_{(2)}$ indicate no interrupt and a nonmaskable interrupt as defined in the SPARC architecture. IRL must be determined for priority by an external circuit and must be held until confirmed by the CPU.
READY#	EXTERNAL READY	I	Ready signal input pin. Input the “L” level signal to upon completion of a bus cycle. Upon reception of READY#=“L”, the CPU starts the next bus cycle. Note, however, that the“L” input to this pin is not necessary when the internal wait state generator circuit is used. For burst transfer, instruction fetch or data load using an 8-bit bus, instruction fetch or data load using an 16-bit bus, the pin must input the ready signal for the prescribed number of times whenever the address strobe signal is asserted.
MEXC#	MEMORY EXCEPTION	I	Memory access exception pin. If this pin inputs the “L” level signal in the same cycle as the ready signal input, the CPU handles it as an instruction access or data access exception to generate a trap. The operation of the device is unpredictable if the MEXC# signal is asserted at a timing other than the same cycle as the ready signal input. (An exception occurring with the PSR ET bit set to “0” results in an error state.)

(Continued)

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Symbol	Pin name	I/O	Function
ERROR#	ERROR SIGNAL	O	Error signal. This pin outputs an error signal indicating that the CPU has stopped in the error state resulting from a trap occurring with traps disabled. The CPU can exit the error state only by a reset.
ASI<3:0>	ADDRESS SPACE IDENTIFIERS	I/O	ASI pin (address space identification signal) or ADR pin. Setting the ASISEL pin to "H" selects the ASI pin; setting it to "L" selects the ADR<28:31> pin on the MB86832/834 or ADR<24:27> pin on the MB86833/835/836. When the ASISEL pin is set to "L", the "L" input to the AS# pin is prohibited. A choice of these pins is supported by the MB8682/833/834/835/836 but not by the MB86831-66/80 (only ASI<3:0> is available). Like the ADR<27:2> pin (ADR<23:2> pin on the MB86833/835/836), this pin remains enabled for output during the bus cycle. The ASI pin serves as an input in the bus grant state, used for CS generation and internal resource address decoding. When ASI<3:0> is input from an external device, ASI<7:4> is handled as "0" in the CPU.
LOCK#	BUS LOCK	O	Bus lock signal. During execution of the Atomic Load Store instruction, the CPU asserts the LOCK# signal to indicate that the current bus transaction requires multiple transfers which cannot be divided. At a bus request (BREQ#) during execution of an atomic instruction, the CPU releases the bus (by asserting the BGRNT# signal) upon completion of the instruction execution. For normal use (where bus access permission is controlled by BREQ#/BGRNT#), the LOCK# signal need not be used.
RDYOUT#	READY OUTPUT	O	Ready signal output. This pin outputs the composite signal consisting of the ready signal generated by the internal wait state generator circuit and the external ready signal (READY#). While the delay of the internally generated ready signal is regulated based on the clock input, the input from the pin is output delayed as it is at the timing of generation of the external ready signal.
IDLEEN	IDLE ENABLE	I	Idle insertion enable pin. If the cycle that follows access to the CS0# area is load or store operation when this pin is at the "H" level, the CPU starts the next bus cycle after inserting two idle clock cycles. This is efficient when EPROM which takes long data bus output off time is connected directly to the CPU.When this pin is at the "L" level, the CPU inserts only one idle cycle before a write cycle immediately after a read cycle (this control is compatible with conventional SPARClite processors). Fix this pin at the "H" or "L" level.
BMODE8# BMODE16#	BOOT MODE 8 BOOT MODE 16	I	CS0# area bus width setting signals. These pins input signals at a reset to determine the bus width of the CS0# area. Setting the BMODE8# pin to "L" selects the 8-bit bus mode; setting the BMODE16# pin to "L" selects the 16-bit bus mode. (The bus width for the CS1#-CS5# area is specified by the Bus Width/Cacheable Control Register (BWCR).) Fix these pins to "L" or "H". However, it is not allowed to set both of them to "L".

(Continued)

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Symbol	Pin name	I/O	Function
NONCACHE#	NON-CACHE-ABLE	I	Non-cacheable signal. This pin inputs the signal for exclusion from data caching. The NON-CACHE# signal is enabled by setting the Cacheability Enable bit (bit 7) in the Cache/BIU Control Register (CBIR). The “L” input to this pin when data is read prevents the data and its address from being written to the data cache (the NONCACHE# signal is disabled at an instruction fetch). Usually, the NONCACHE# signal must be asserted in the cycle in which the address strobe signal is asserted. Even if the NON-CACHE# signal is asserted after a delay of one or more cycles, how-ever, the signal can be used by setting the Non-cacheable bit (bit 9, bit 8) in the Cache/BIU Control Register (CBIR).
PDOWN#	POWER DOWN	O	Sleep mode (low power consumption mode) output pin. “L” level input to this pin releases the CPU from the sleep mode (low power consumption mode) to start operation. Although the pin is an asynchronous input, it requires an “L” width of at least two clock cycles. Input “L” to this pin only when the PDOWN# pin is at the “L” level.
WKUP#	WAKE-UP	I	Sleep mode (low power consumption mode) cancel pin. “L” input to this pin cancels the CPU sleep mode (low power consump-tion mode), causing the CPU to start operation. Although the pin is an asynchronous input, it requires an “L” width of at least two clock cycles. Input the“L” signal to this pin only when PDOWN# is “L”. When PDOWN# goes “H”, set this pin to "H".
BMREQ#	BURST MODE REQUEST	O	Burst transfer request pin. If a cache miss occurs when the Instruction Burst Enable bit or Data Burst Enable bit in the Bus Control Register (BCR) has been set, the CPU sets the BMREQ# signal to “L” and requests external memory for burst transfer. The BMREQ# signal is also asserted when the DRAM Burst Enable bit in the System Support Control Register (SSCR) has been set. In this case, however, the external device need not return the BMACK# signal because the internal DRAM controller responds to the request.
BMACK#	BURST MODE ACKNOWL-EDGE	I	Burst mode acknowledge input. When a burst transfer request is issued, the burst transfer mode is es-tablished if the “L” level asserted until the same cycle as the READY# signal is input to this pin. (It is also established either when the “L” level is input in the same cycle as the READY# signal or when the “L” level input in an earlier cycle continues until the same cycle as the READY# signal.) When the DRAM Burst Enable bit in the System Support Con-trol Register (SSCR) has been set, the burst transfer mode is estab-lished even though this pin receives the BMACK# signal.
PBREQ#	PROCESSOR BUS REQUEST	O	Processor bus request signal. When the CPU requires accessing an external bus The PBREQ# signal is asserted to issue a processor bus request to the external bus master when the CPU requires accessing an external bus (when it requires external access after a cache miss) while the CPU has relinquished bus access permission.

(Continued)

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Symbol	Pin name	I/O	Function
OVF#	TIMER OVER-FLOW	O	Timer overflow signal. This pin outputs the “L” pulse when the timer reaches 0 after starting counting according to the settings in the DRAM Refresh Timer Register and DRAM Refresh Timer Pre-load Register with the TIMER ON/OFF bit in the System Support Control Register (SSCR) set to “1” The pulse width is the 1-clock width of the external bus clock when bit 31 in the DRAM Refresh Timer Pre-load Register is “0”. When the bit is “1”, the pulse width is the 3-clock width. The timer performs counting based on the external bus clock. Although this pin is used usually for the DRAM refresh request signal, it can be connected to the interrupt input (IRQx) of the interrupt controller (IRC) when the pulse width has been specified as the 3-clock width.
SAMEPAGE#	SAME PAGE DETECT	O	Same-page detection output pin. When the Same-Page Enable bit in the System Support Control Register (SSCR) has been “1”, this pin outputs the“L” level if the CS4# pin is at the “L” level and if the address masked by the Same-Page Mask Register (SPGMR) matches the previously accessed address when compared. The SAMEPAGE# signal remains output during the bus cycle.
FLOAT#	FLOATING	I	Pin float input. Fixing this pin at the “L” level puts all of the output pins and bidirectional pins to the High-Z state.

- State of pins

Pin symbol	At reset	At bus grant
ADR<27:2>	O (X)	I (D)
AS#	O (H)	I (Z)
BE0#	O (X)	O (Z)
BE2#	O (X)	I (Z)
CS0# to CS5#	O (H)	O (V)
ERROR#	O (H)	O (V)
LOCK#	O (H)	O (Z)
PDOWN#	O (H)	O (H)
PBREQ#	O (H)	O (V)
SAMEPAGE#	O (H)	O (V)

Pin symbol	At reset	At bus grant
D<31:0>	I (Z)	I (Z)
RDWR#	O (H)	I (Z)
BE1#	O (X)	O (Z)
BE3#	O (X)	O (Z)
BGRNT#	O (H)	O (L)
ASI<3:0>	O (X)	I (Z)
RDYOUT#	O (V)	O (V)
BMREQ#	O (H)	O (H)
OVF#	O (H)	O (V)

O (V) :The circuit is active with the output at a valid level.
O (X) :The circuit is inactive with the output indeterminate.
O (Z) :Output pins and High-Z.
O (H) :The “H”level is output.
O (L) :The “L” level is output.
I (Z) :Input pins and High-Z
I (D) :When the DRAM controller has been enabled, the pin is switched to serve as an output, from the clock cycle that follows the clock cycle in which the AS# pin becomes “L”, and remains as the output until the ready signal input pin becomes “L”. When the DRAM controller has been disabled, the pin enters the High-Z state.

2. DRAM Controller Related Pins (MB86831/832/833/834/835)

Symbol	Pin name	I/O	Function
RAS0# RAS1# RAS2# RAS3#	DRAM ROW ADDRESS STROBE	O	DRAM controller RAS outputs. The RAS0# to RAS3# signals are control signals corresponding to DRAM banks 0 to 3, respectively. The MB86833/835 does not support banks 1 to 3 because the RAS1# to RAS3# pins do not exist on the chip.
CAS0# CAS1# CAS2# CAS3#	DRAM COLUMN ADDRESS STROBE	O	DRAM CAS control outputs. For using the 32-bit bus width along with 2-CAS DRAM, the CAS0# to CAS3# pins are controlled in association with byte 0 (b31 to b24), byte 1 (b23 to b16), byte 2 (b15 to b8), and byte 3 (b7 to b0), respectively. For using the 16-bit bus width along with 2-CAS DRAM, the CAS2# and CAS3# pins correspond to byte 0 (byte data at an even-numbered address) and byte 1 (byte data at an odd-numbered address), respectively. When the 16-bit bus width is used, the outputs from the CAS0# and CAS1# pins are unpredictable. When 2-WE DRAM is used, the CAS0# to CAS3# pins provide the same output.
DWE0# DWE1# DWE2# DWE3#	DRAM WRITE ENABLE	O	DRAM write enable control outputs. For using 2-WE DRAM, the DWE0# to DWE3# signals are controlled in association with byte 0 (b31 to b24), byte 1 (b23 to b16), byte 2 (b15 to b8), and byte 3 (b7 to b0), respectively. When 2-CAS DRAM is used, the DWE0# to DWE3# pins provide the same output. The DWE1# to DWE3# pins do not exist on the MB86833/835.
DOE#	DRAM OUTPUT	O	DRAM OE control output. When fast-page DRAM is used, the DRAM can be controlled without using the DOE# signal because the DWEx# and CASx# pins are controlled at the early write timing. When EDO (hyper page mode) DRAM is used, the DOE# signal is required for high-impedance control of the DRAM output.
ADR<13:2>	ADDRESS BUS	I/O	DRAM address signal. The DRAM controller outputs the multiplexed row and column addresses to a CPU address pin of ADR<13:2>.

- State of pins

Pin symbol	At reset	At bus grant
RAS3# to RAS0#	O (H)	O (V)
DOE#	O (H)	O (V)

Pin symbol	At reset	At bus grant
CAS3# to CAS0#	O (H)	O (V)
ADR<13:2>	O (X)	I (D)

O (V) : The circuit is active with the output at a valid level.
O (X) : The circuit is inactive with the output indeterminate.
O (H) : The “H” level is output.
I (D) : When the DRAM controller has been enabled, the pin is switched to serve as an output, from the clock cycle that follows the clock cycle in which the AS# pin becomes “L”, and remains as the output until the ready signal input pin becomes “L”. When the DRAM controller has been disabled, the pin enters the High-Z state.

3. Interrupt controller (IRC) Related Pins

Symbol	Pin name	I/O	Function
IRQ15/IRL3 IRQ14/IRL2 IRQ13/IRL1 IRQ12/IRL0 IRQ11 IRQ10 IRQ9 IRQ8	INTERRUPT REQUEST	I	Interrupt input pins. When the active level set for the interrupt controller (IRC) trigger mode is input to these pins, the request sense register of the interrupt controller (IRC) holds the interrupt request. (The interrupt controller (IRC) evaluates priority levels and performs coding for the IRL<3:0> pin, and notifies the CPU core of the interrupt level.) The IRQ15 to IRQ12 signals are assigned to the IRL<3:0> pin. They function as IRQ15 to IRQ12 when the interrupt controller (IRC) becomes enabled.

4. Signals for the general-purpose 16-bit timer (MB86836)

Symbol	Pin name	I/O	Function
PRSCK0	Prescaler Clock Output0	O	Prescaler output pin. The external clock mode is not supported, which is included in the functions of the prescaler on the MB86942. The pin is reset to “L”.
OUT0	Timer Output0	O	Timer output pin. The external clock mode is not supported, which is included in the functions of the timer on the MB86942. The pin is reset to “L”.
IN0	Timer Input0	I	Timer count operation control pin. This pin inputs the GATE signal in MODE0 to MODE3 and the external trigger signal in MODE4.This pin has an internal pull-down resistor.

- Pin status

Symbol	Reset	Bus granted
PRSCK0	O (L)	O (V)
OUT0	O (L)	O (V)

Note : O (L) : Output “L” level
O (V) : Circuit activated ; effective level is output

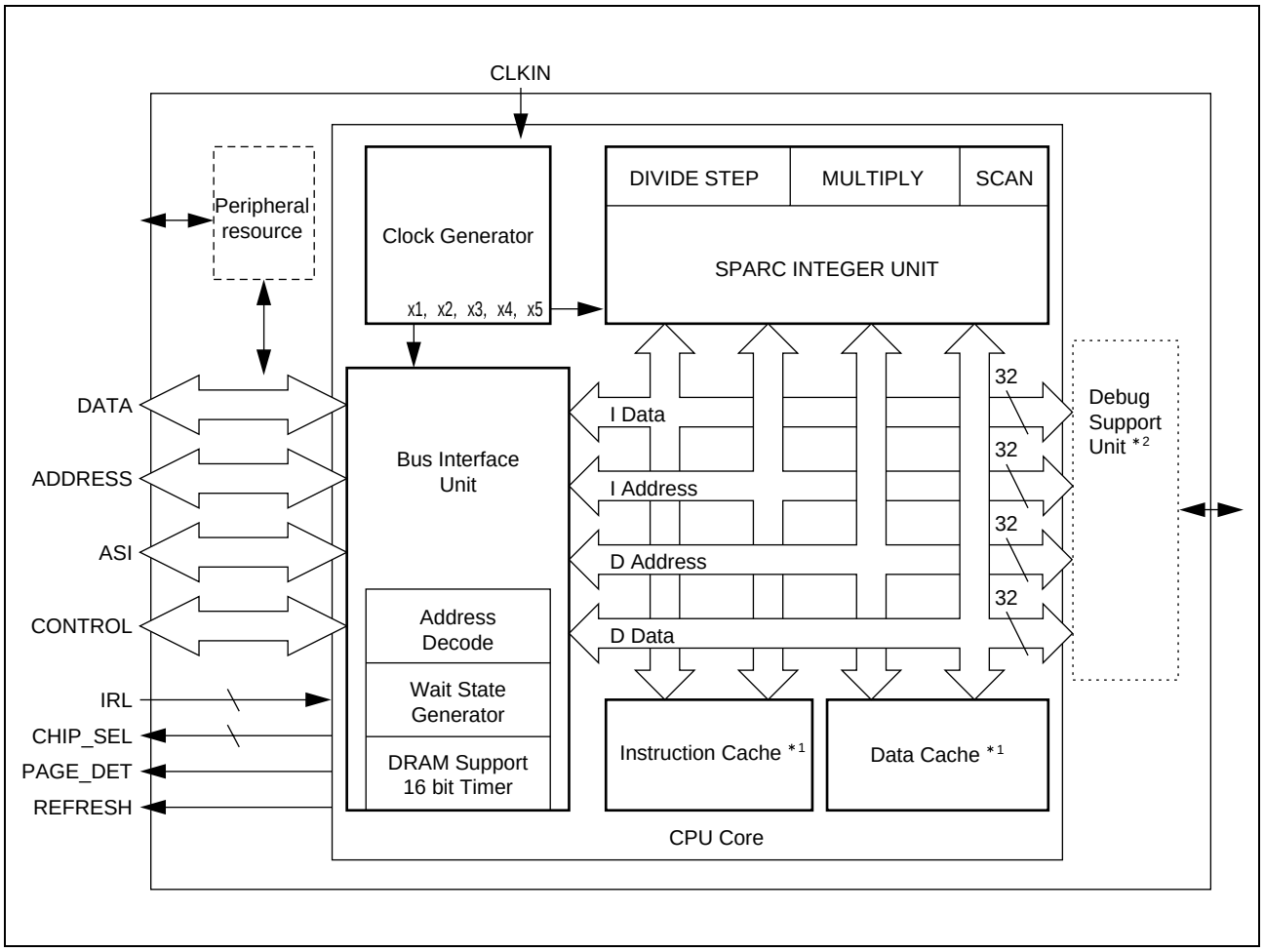
5. DDSU (Debug Support Unit) Related Pins (MB86832/834)

Symbol	Pin name	I/O	Function
EMUBRK#	Emulator Break	I	Emulator Break pin. When a reset is canceled, the EMUBRK# signal level is input to set a mode in combination with the EMUENG# signal level. The MB86832 contains a pull-up resistor (about 50 kΩ). Leave this pin open when the DSU (debug support unit) is not used. The MB86834 has no pull-up resistor.
EMUENB#	Emulator Enable	I/O	Emulator Enable pin. When a reset is canceled, the EMUENB# signal level is input to set a mode in combination with the EMUBRK# signal level. When a reset is canceled, this pin becomes an output pin after four clock cycles if either (DSUBRK# = DSUENB# = “L”) or (DSUBRK# = “H”, DSUENB# = “L”) is set. The MB86832 contains a pull-up resistor (about 50 kΩ). Leave this pin open when the DSU (debug support unit) is not used. The MB86834 has no pull-up resistor.
EMUD<3:0>	Emulator Data Bus	I/O	Emulator Data pin. This pin outputs traced instruction addresses divided into eight components in the monitor mode. It also inputs instruction codes and outputs instruction or data addresses in the DSU mode. Since this pin serves as an output with the DSU disabled, leave the pin open if the DSU (debug support unit) is not to be used.
EMUSD<3:0>	Emulator Status/ Data Bus	I/O	Emulator Status/Data pin. This pin outputs the CPU status in the monitor mode and. It also inputs instruction codes and outputs instruction or data addresses in the DSU mode. Since this pin serves as an output with the DSU disabled, leave the pin open if the DSU (debug support unit) is not to be used.

6. Signals for the JTAG Test Port (MB86836)

Symbol	Pin name	I/O	Function
TCK	Test Clock	I	JTAG test clock input pin. This pin has an internal pull-down resistor.
TMS	Test Mode	I	JTAG test mode selection pin. This pin has an internal pull-down resistor.
TDI	Test Data In	I	JTAG test data input pin. This pin has an internal pull-down resistor.
TDO	Test Data Out	O	JTAG test data output pin.
TRST#	Test Reset	I	JTAG test reset pin. This pin is reset to “L”. It has an internal pull-down resistor.

■ BLOCK DIAGRAM



*1:The cache capacity is as follows.

Item \ Parts number	MB86831	MB86832	MB86833	MB86834	MB86835	MB86836
Instruction cash	4 KB/2 way	8 KB/2 way	1 KB/Direct	16 KB/2 way	4 KB/2 way	8 KB/2 way
Data cash	2 KB/2 way	8 KB/2 way	1 KB/Direct	16 KB/2 way	2 KB/2 way	8 KB/2 way

*2:DSU (debug support unit) is added with MB86832/834.

■ ELECTRIC CHARACTERISTICS

1. ABSOLUTE MAXIMUM RATINGS

(1)MB86831-66/MB86832-66/MB86833

(V_{SS} = 0.0 V)

Parameter	Symbol	Rating		Unit
		Min.	Max.	
Power supply voltage(I/O)	V_{DD5}	– 0.5	6	V
Power supply voltage(Internal)	V_{DD3}	– 0.5	4	V
Input voltage	V_I	– 0.5	V_{DD5} + 0.5	V
Storage temperature	T_{STG}	– 55	+ 125	°C
Temperature at bias	T_{BIAS}	0	+ 70	°C
Overshoot	—	Within V_{DD5} + 1.0 V (Within 50 ns)		—
Undershoot	—	Within V_{SS} – 1.0 V (Within 50 ns)		—

(2)MB86834-108,-120/MB86836-90,-108

(V_{SS} = 0.0 V)

Parameter	Symbol	Rating		Unit
		Min.	Max.	
Power supply voltage(I/O)	V_{DD5}(V_{DDE})	– 0.5	4.0	V
Power supply voltage(Internal)	V_{DD3}(V_{DDI})	– 0.5	3.0	V
Input voltage	V_I	– 0.5	V_{DDE} + 0.5	V
Storage temperature	T_{STG}	– 55	+ 125	°C
Temperature at bias	T_{BIAS}	0	+ 70	°C

(3)MB86835

(V_{SS} = 0.0 V)

Parameter	Symbol	Rating		Unit
		Min.	Max.	
Power supply voltage(I/O)	V_{DD5}	– 0.5	4	V
Power supply voltage(Internal)	V_{DD3}	– 0.5	4	V
Input voltage	V_I	– 0.5	V_{DD5} + 0.5	V
Storage temperature	T_{STG}	– 55	+ 125	°C
Temperature at bias	T_{BIAS}	0	+ 70	°C
Overshoot	—	Within V_{DD5} + 1.0 V (Within 50 ns)		—
Undershoot	—	Within V_{SS} – 1.0 V (Within 50 ns)		—

(Notes on Board Wiring)

- For connecting the power supply and ground (GND), use multiple V_{DD} and V_{SS} pins. The system board based on the MB86830 series must be a multilayer board containing power supply (V_{DD}) and GND (V_{SS}) layers for stable power supply. Leave any pin designated as “N.C.” unconnected.
- Insert sufficient decoupling capacitors near the MB86830 series. Changes to the output levels of many of the output pins on the MB86830 series (in particular, those with large load capacitance) may cause variation in power supply.
- For those systems which run at a high frequency, low-inductance capacitors and mutual wiring are recommended. Inductance can be lowered by shortening the distance between the processor and decoupling capacitor.
- For system reliability, the pin entering the tristate when the MB86830 series enters the bus grant state should be driven by a bus master. In particular, the LOCK#, ADR<27:2>, ASI<3:0> (ASI<3:0>/ADR<28:31>, ASI<3:0> /ADR<24:27>), BE0# to BE3#, D<31:0>, AS#, and RDWR# pins must be driven by other bus masters. Usually, these pins require no external pull-up resistor because they are driven by the processor when the processor is active or idle.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current,temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. RECOMMENDED OPERATING CONDITIONS

(1)MB86831-66/MB86832-66/MB86833

(V_{SS} = 0.0 V)

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Power supply voltage (I/O = 5.0 V)	V_{DD5}	4.75	5.0	5.25	V
Power supply voltage (I/O = 3.3 V)	V_{DD5}	3.0	3.3	3.6	V
Power supply voltage (internal)	V_{DD3}	3.0	3.3	3.6	V
“L” level input voltage	V_{IL}	0	—	$V_{DD3} \times 0.25$	V
“H” level input voltage	V_{IH}	$V_{DD3} \times 0.65$	—	V_{DD5}	V
Operating temperature	Topr	0	+ 25	+ 70	°C

(2)MB86831-80/MB86832- 80, -100

(V_{SS} = 0.0 V)

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Power supply voltage (I/O = 5.0 V)	V_{DD5}	4.75	5.0	5.25	V
Power supply voltage (I/O = 3.3 V)	V_{DD5}	3.15	3.3	3.45	V
Power supply voltage (internal)	V_{DD3}	3.15	3.3	3.45	V
“L” level input voltage	V_{IL}	0	—	$V_{DD3} \times 0.25$	V
“H” level input voltage	V_{IH}	$V_{DD3} \times 0.65$	—	V_{DD5}	V
Operating temperature	Topr	0	+ 25	+ 70	°C

(3)MB86834-108,-120/MB86836-90,-108

(V_{SS} = 0.0 V)

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Power supply voltage (I/O)	$V_{DD5}(V_{DDE})$	3.15	3.3	3.45	V
Power supply voltage (internal)	$V_{DD3}(V_{DDE})$	2.4	2.5	2.6	V
“L” level input voltage	V_{IL}	– 0.3	—	0.8	V
“H” level input voltage	V_{IH}	2.0	—	V_{DDE} + 0.3	V
Operating temperature	Topr	0	+ 25	+ 70	°C

(4)MB86835

(V_{SS} = 0.0 V)

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Power supply voltage (I/O = 3.3 V)	V_{DD5}	3.15	3.3	3.45	V
Power supply voltage (internal)	V_{DD3}	3.15	3.3	3.45	V
"L" level input voltage	V_{IL}	0	—	$V_{DD3} \times 0.25$	V
"H" level input voltage	V_{IH}	$V_{DD3} \times 0.65$	—	V_{DD5}	V
Operating temperature	Topr	0	+ 25	+ 70	°C

- The MB86831/832/833 can be used with a 5.0-V or 3.3-V interface.
  5.0-V interface: V_{DD5} = 5.0 V, V_{DD3} = 3.3 V (two power supplies)
  3.3-V interface: V_{DD5} = V_{DD3} = 3.3 V (single power supply)
- When the 3.3-V interface is used, all signals input to the MB86830 series must be 3.3 V because the MB86830 series cannot input 5.0-V signals with that interface.
- When the 5.0-V interface is used, the output fully swings at 5.0 V. Although the input is always defined by a 3.3-V power supply, it can also accept 3.3 V or more.
- When the 5.0-V interface is used, the MB86830 series requires two power supplies. Follow the procedures below to turn on and off these power supplies:
  Power-on procedure: $V_{DD3} \rightarrow V_{DD5} \rightarrow$ signal
  Shutdown procedure: Signal $\rightarrow V_{DD5} \rightarrow V_{DD3}$
- The MB86834/836 requires two power supplies of V_{DDE} (3.3-V system) and V_{DDI} (2.5-V system). Follow the procedures below to turn on and off these power supplies:
  Power-on procedure: $V_{DDI} \rightarrow V_{DDE} \rightarrow$ signal
  Shutdown procedure: Signal $\rightarrow V_{DDE} \rightarrow V_{DDI}$
- The MB86835 has two V_{DD}, V_{DD3} and V_{DD5}. Connect each of them to a 3.3-V power supply.
- The MB86834/835/836 uses only a 3.3-V interface; they cannot accept 5-V signals.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

3. DC Characteristics

(1)MB86831-66 (Maximum internal operation frequency:66 MHz)

- 5.0 V interface

(V_{DD5} = 5.0 V ± 5%, V_{DD3} = 3.3 V ± 0.3 V, V_{SS} = 0.0 V, T_A = 0 °C to + 70 °C)

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
"L" level input voltage	V_{IL}	—	0	—	$V_{DD3} \times 0.25$	V
"H" level input voltage	V_{IH}	—	$V_{DD3} \times 0.65$	—	V_{DD5}	V
"L" level output voltage	V_{OL}	I_{OL} = 4 mA	0	—	0.4	V
"H" level output voltage	V_{OH}	I_{OH} = − 4 mA	V_{DD5} − 0.5	—	V_{DD5}	V
Input leakage current	I_{LI}	V_{IN} = 0 or V_{DD5}	− 10	—	10	µA
Trial state output leakage current	I_{LZ}	V_{OUT} = 0 or V_{DD5}	− 10	—	10	µA
Power supply current (V_{DD5})	I_{DD}	33 MHz No-load	—	40	—	mA
Power supply current (V_{DD3})	I_{DD}	66 MHz	—	150	—	mA
At sleep power supply current(V_{DD3})	I_{SLEEP}	66 MHz	—	15	—	mA
Capacity of pins	C_{PIN}	V_{DD5} = V_I = 0 f = 1 MHz	—	—	16	pF

- 3.3 V interface

(V_{DD5} = V_{DD3} = 3.3 V ± 0.3%, V_{SS} = 0.0 V, T_A = 0 °C to + 70 °C)

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
"L" level input voltage	V_{IL}	—	0	—	$V_{DD3} \times 0.25$	V
"H" level input voltage	V_{IH}	—	$V_{DD3} \times 0.65$	—	V_{DD5}	V
"L" level output voltage	V_{OL}	I_{OL} = 2 mA	0	—	0.4	V
"H" level output voltage	V_{OH}	I_{OH} = − 2 mA	V_{DD5} − 0.5	—	V_{DD5}	V
Input leakage current	I_{LI}	V_{IN} = 0 or V_{DD5}	− 10	—	10	µA
Trial state output leakage current	I_{LZ}	V_{OUT} = 0 or V_{DD5}	− 10	—	10	µA
Power supply current (V_{DD5})	I_{DD}	33 MHz No-load	—	30	—	mA
Power supply current (V_{DD3})	I_{DD}	66 MHz	—	150	—	mA
At sleep power supply current(V_{DD3})	I_{SLEEP}	66 MHz	—	15	—	mA
Capacity of pins	C_{PIN}	V_{DD5} = V_I = 0 f = 1 MHz	—	—	16	pF

(2)MB86831-80 (Maximum internal operation frequency:80 MHz)

- 5.0 V interface

(V_{DD5} = 5.0 V ± 5%, V_{DD3} = 3.3 V ± 0.15 V, V_{SS} = 0.0 V, T_A = 0 °C to + 70 °C)

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
"L" level input voltage	V_{IL}	—	0	—	$V_{DD3} \times 0.25$	V
"H" level input voltage	V_{IH}	—	$V_{DD3} \times 0.65$	—	V_{DD5}	V
"L" level output voltage	V_{OL}	I_{OL} = 4 mA	0	—	0.4	V
"H" level output voltage	V_{OH}	I_{OH} = − 4 mA	V_{DD5} − 0.5	—	V_{DD5}	V
Input leakage current	I_{LI}	V_{IN} = 0 or V_{DD5}	− 10	—	10	µA
Trial state output leakage current	I_{LZ}	V_{OUT} = 0 or V_{DD5}	− 10	—	10	µA
Power supply current (V_{DD5})	I_{DD}	40MHz No-load	—	50	—	mA
Power supply current (V_{DD3})	I_{DD}	80MHz	—	200	—	mA
At sleep power supply current(V_{DD3})	I_{SLEEP}	80MHz	—	20	—	mA
Capacity of pins	C_{PIN}	$V_{DD5} = V_I = 0$ f = 1 MHz	—	—	16	pF

- 3.3 V interface

(V_{DD5} = 5.0 V ± 5%, V_{DD3} = 3.3 V ± 0.15 V, V_{SS} = 0.0 V, T_A = 0 °C to + 70 °C)

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
"L" level input voltage	V_{IL}	—	0	—	$V_{DD3} \times 0.25$	V
"H" level input voltage	V_{IH}	—	$V_{DD3} \times 0.65$	—	V_{DD5}	V
"L" level output voltage	V_{OL}	I_{OL} = 2 mA	0	—	0.4	V
"H" level output voltage	V_{OH}	I_{OH} = − 2 mA	V_{DD5} − 0.5	—	V_{DD5}	V
Input leakage current	I_{LI}	V_{IN} = 0 or V_{DD5}	− 10	—	10	µA
Trial state output leakage current	I_{LZ}	V_{OUT} = 0 or V_{DD5}	− 10	—	10	µA
Power supply current (V_{DD5})	I_{DD}	40MHz No-load	—	36	—	mA
Power supply current (V_{DD3})	I_{DD}	80MHz	—	200	—	mA
At sleep power supply current(V_{DD3})	I_{SLEEP}	80MHz	—	20	—	mA
Capacity of pins	C_{PIN}	$V_{DD5} = V_I = 0$ f = 1 MHz	—	—	16	pF

(3)MB86832-66 (Maximum internal operation frequency:66 MHz)

- 5.0 V interface

(V_{DD5} = 5.0 V ± 5%, V_{DD3} = 3.3 V ± 0.3 V, V_{SS} = 0.0 V, T_A = 0 °C to + 70 °C)

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
"L" level input voltage	V_{IL}	—	0	—	$V_{DD3} \times 0.25$	V
"H" level input voltage	V_{IH}	—	$V_{DD3} \times 0.65$	—	V_{DD5}	V
"L" level output voltage	V_{OL}	I_{OL} = 4 mA	0	—	0.4	V
"H" level output voltage	V_{OH}	I_{OH} = − 4 mA	V_{DD5} − 0.5	—	V_{DD5}	V
Input leakage current	I_{LI}	V_{IN} = 0 or V_{DD5}	− 10	—	10	µA
Trial state output leakage current	I_{LZ}	V_{OUT} = 0 or V_{DD5}	− 10	—	10	µA
Power supply current (V_{DD5})	I_{DD}	33 MHz No-load	—	40	—	mA
Power supply current (V_{DD3})	I_{DD}	66 MHz	—	200	—	mA
At sleep power supply current(V_{DD3})	I_{SLEEP}	66 MHz	—	15	—	mA
Capacity of pins	C_{PIN}	V_{DD5} = V_I = 0 f = 1 MHz	—	—	16	pF

- 3.3 V interface

(V_{DD5} = V_{DD3} = 3.3 V ± 0.3 V, V_{SS} = 0.0 V, T_A = 0 °C to + 70 °C)

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
"L" level input voltage	V_{IL}	—	0	—	$V_{DD3} \times 0.25$	V
"H" level input voltage	V_{IH}	—	$V_{DD3} \times 0.65$	—	V_{DD5}	V
"L" level output voltage	V_{OL}	I_{OL} = 2 mA	0	—	0.4	V
"H" level output voltage	V_{OH}	I_{OH} = − 2 mA	V_{DD5} − 0.5	—	V_{DD5}	V
Input leakage current	I_{LI}	V_{IN} = 0 or V_{DD5}	− 10	—	10	µA
Trial state output leakage current	I_{LZ}	V_{OUT} = 0 or V_{DD5}	− 10	—	10	µA
Power supply current (V_{DD5})	I_{DD}	33 MHz No-load	—	30	—	mA
Power supply current (V_{DD3})	I_{DD}	66 MHz	—	200	—	mA
At sleep power supply current(V_{DD3})	I_{SLEEP}	66 MHz	—	15	—	mA
Capacity of pins	C_{PIN}	V_{DD5} = V_I = 0 f = 1 MHz	—	—	16	pF

(4)MB86832-80 (Maximum internal operation frequency:80 MHz)

- 5.0 V interface

(V_{DD5} = 5.0 V ± 5%, V_{DD3} = 3.3 V ± 0.15 V, V_{SS} = 0.0 V, T_A = 0 °C to + 70 °C)

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
"L" level input voltage	V_{IL}	—	0	—	$V_{DD3} \times 0.25$	V
"H" level input voltage	V_{IH}	—	$V_{DD3} \times 0.65$	—	V_{DD5}	V
"L" level output voltage	V_{OL}	I_{OL} = 4 mA	0	—	0.4	V
"H" level output voltage	V_{OH}	I_{OH} = – 4 mA	V_{DD5} – 0.5	—	V_{DD5}	V
Input leakage current	I_{LI}	V_{IN} = 0 or V_{DD5}	– 10	—	10	µA
Trial state output leakage current	I_{LZ}	V_{OUT} = 0 or V_{DD5}	– 10	—	10	µA
Power supply current (V_{DD5})	I_{DD}	40MHz No-load	—	50	—	mA
Power supply current (V_{DD3})	I_{DD}	80MHz	—	250	—	mA
At sleep power supply current(V_{DD3})	I_{SLEEP}	80MHz	—	20	—	mA
Capacity of pins	C_{PIN}	V_{DD5} = V_I = 0 f = 1 MHz	—	—	16	pF

- 3.3 V interface

(V_{DD5} = V_{DD3} = 3.3 V ± 0.15 V, V_{SS} = 0.0 V, T_A = 0 °C to + 70 °C)

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
"L" level input voltage	V_{IL}	—	0	—	$V_{DD3} \times 0.25$	V
"H" level input voltage	V_{IH}	—	$V_{DD3} \times 0.65$	—	V_{DD5}	V
"L" level output voltage	V_{OL}	I_{OL} = 2 mA	0	—	0.4	V
"H" level output voltage	V_{OH}	I_{OH} = – 2 mA	V_{DD5} – 0.5	—	V_{DD5}	V
Input leakage current	I_{LI}	V_{IN} = 0 or V_{DD5}	– 10	—	10	µA
Trial state output leakage current	I_{LZ}	V_{OUT} = 0 or V_{DD5}	– 10	—	10	µA
Power supply current (V_{DD5})	I_{DD}	40MHz No-load	—	36	—	mA
Power supply current (V_{DD3})	I_{DD}	80MHz	—	250	—	mA
At sleep power supply current(V_{DD3})	I_{SLEEP}	80MHz	—	20	—	mA
Capacity of pins	C_{PIN}	V_{DD5}= V_I = 0 f = 1 MHz	—	—	16	pF

(5)MB86832-100 (Maximum internal operation frequency:100 MHz)

- 5.0 V interface

(V_{DD5} = 5.0 V ± 5%, V_{DD3} = 3.3 V ± 0.15 V, V_{SS} = 0.0 V, T_A = 0 °C to + 70 °C)

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
"L" level input voltage	V_{IL}	—	0	—	$V_{DD3} \times 0.25$	V
"H" level input voltage	V_{IH}	—	$V_{DD3} \times 0.65$	—	V_{DD5}	V
"L" level output voltage	V_{OL}	I_{OL} = 4 mA	0	—	0.4	V
"H" level output voltage	V_{OH}	I_{OH} = – 4 mA	V_{DD5} – 0.5	—	V_{DD5}	V
Input leakage current	I_{LI}	V_{IN} = 0 or V_{DD5}	– 10	—	10	µA
Trial state output leakage current	I_{LZ}	V_{OUT} = 0 or V_{DD5}	– 10	—	10	µA
Power supply current (V_{DD5})	I_{DD}	33MHz No-load	—	40	—	mA
Power supply current (V_{DD3})	I_{DD}	100MHz	—	300	—	mA
At sleep power supply current(V_{DD3})	I_{SLEEP}	100MHz	—	25	—	mA
Capacity of pins	C_{PIN}	V_{DD5}= V_I = 0 f = 1 MHz	—	—	16	pF

- 3.3 V interface

(V_{DD5} = V_{DD3} = 3.3 V ± 0.15 V, V_{SS} = 0.0 V, T_A = 0 °C to + 70 °C)

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
"L" level input voltage	V_{IL}	—	0	—	$V_{DD3} \times 0.25$	V
"H" level input voltage	V_{IH}	—	$V_{DD3} \times 0.65$	—	V_{DD5}	V
"L" level output voltage	V_{OL}	I_{OL} = 2 mA	0	—	0.4	V
"H" level output voltage	V_{OH}	I_{OH} = – 2 mA	V_{DD5} – 0.5	—	V_{DD5}	V
Input leakage current	I_{LI}	V_{IN} = 0 or V_{DD5}	– 10	—	10	µA
Trial state output leakage current	I_{LZ}	V_{OUT} = 0 or V_{DD5}	– 10	—	10	µA
Power supply current (V_{DD5})	I_{DD}	33MHz No-load	—	30	—	mA
Power supply current (V_{DD3})	I_{DD}	100MHz	—	300	—	mA
At sleep power supply current(V_{DD3})	I_{SLEEP}	100MHz	—	25	—	mA
Capacity of pins	C_{PIN}	V_{DD5} = V_I = 0 f = 1 MHz	—	—	16	pF

(6)MB86833 (Maximum internal operation frequency:66 MHz)

- 5.0 V interface

(V_{DD5} = 5.0 V ± 5%, V_{DD3} = 3.3 V ± 0.3 V, V_{SS} = 0.0 V, T_A = 0 °C to + 70 °C)

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
"L" level input voltage	V_{IL}	—	0	—	$V_{DD3} \times 0.25$	V
"H" level input voltage	V_{IH}	—	$V_{DD3} \times 0.65$	—	V_{DD5}	V
"L" level output voltage	V_{OL}	I_{OL} = 4 mA	0	—	0.4	V
"H" level output voltage	V_{OH}	I_{OH} = – 4 mA	V_{DD5} – 0.5	—	V_{DD5}	V
Input leakage current	I_{LI}	V_{IN} = 0 or V_{DD5}	– 10	—	10	µA
Trial state output leakage current	I_{LZ}	V_{OUT} = 0 or V_{DD5}	– 10	—	10	µA
Power supply current (V_{DD5})	I_{DD}	33 MHz No-load	—	40	—	mA
Power supply current (V_{DD3})	I_{DD}	66 MHz	—	120	—	mA
At sleep power supply current(V_{DD3})	I_{SLEEP}	66 MHz	—	15	—	mA
Capacity of pins	C_{PIN}	$V_{DD5} = V_I = 0$ f = 1 MHz	—	—	16	pF

- 3.3 V interface

(V_{DD5} = V_{DD3} = 3.3 V ± 0.3 V, V_{SS} = 0.0 V, T_A = 0 °C to + 70 °C)

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
"L" level input voltage	V_{IL}	—	0	—	$V_{DD3} \times 0.25$	V
"H" level input voltage	V_{IH}	—	$V_{DD3} \times 0.65$	—	V_{DD5}	V
"L" level output voltage	V_{OL}	I_{OL} = 2 mA	0	—	0.4	V
"H" level output voltage	V_{OH}	I_{OH} = – 2 mA	V_{DD5} – 0.5	—	V_{DD5}	V
Input leakage current	I_{LI}	V_{IN} = 0 or V_{DD5}	– 10	—	10	µA
Trial state output leakage current	I_{LZ}	V_{OUT} = 0 or V_{DD5}	– 10	—	10	µA
Power supply current (V_{DD5})	I_{DD}	33 MHz No-load	—	30	—	mA
Power supply current (V_{DD3})	I_{DD}	66 MHz	—	120	—	mA
At sleep power supply current(V_{DD3})	I_{SLEEP}	66 MHz	—	15	—	mA
Capacity of pins	C_{PIN}	$V_{DD5} = V_I = 0$ f = 1 MHz	—	—	16	pF

(7)MB86834-108 (Maximum internal operation frequency:108 MHz)

(V_{DD5} = 3.3 V ± 0.15 V, V_{DD3} = 2.5 V ± 0.1 V, V_{SS} = 0.0 V, T_A = 0 °C to + 70 °C)

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
"L" level input voltage	V_{IL}	—	0	—	0.8	V
"H" level input voltage	V_{IH}	—	2.0	—	V_{DDE}	V
"L" level output voltage	V_{OL}	I_{OL} = 2.0mA	0	—	0.4	V
"H" level output voltage	V_{OH}	I_{OH} = − 2.0mA	V_{DDE} − 0.4	—	V_{DDE}	V
Input leakage current	I_{LI}	V_{IN} = 0 or V_{DDE}	− 5	—	5	µA
Trial state output leakage current	I_{LZ}	V_{OUT} = 0 or V_{DDE}	− 5	—	5	µA
Power supply current (V_{DD5})	I_{DD}	33 MHz No-load	—	30	—	mA
Power supply current (V_{DD3})	I_{DD}	108 MHz	—	250	—	mA
At sleep power supply current(V_{DD3})	I_{SLEEP}	108 MHz	—	20	—	mA
Capacity of pins	C_{PIN}	V_{DDE} = V_I = 0 f = 1 MHz	—	—	16	pF

(8)MB86834-120 (Maximum internal operation frequency:120 MHz)

(V_{DD5} = 3.3 V ± 0.15 V, V_{DD3} = 2.5 V ± 0.1 V, V_{SS} = 0.0 V, T_A = 0 °C to + 70 °C)

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
"L" level input voltage	V_{IL}	—	0	—	0.8	V
"H" level input voltage	V_{IH}	—	2.0	—	V_{DDE}	V
"L" level output voltage	V_{OL}	I_{OL} = 2.0mA	0	—	0.4	V
"H" level output voltage	V_{OH}	I_{OH} = − 2.0mA	V_{DDE} − 0.4	—	V_{DDE}	V
Input leakage current	I_{LI}	V_{IN} = 0 or V_{DDE}	− 5	—	5	µA
Trial state output leakage current	I_{LZ}	V_{OUT} = 0 or V_{DDE}	− 5	—	5	µA
Power supply current (V_{DD5})	I_{DD}	40 MHz No-load	—	36	—	mA
Power supply current (V_{DD3})	I_{DD}	120 MHz	—	280	—	mA
At sleep power supply current(V_{DD3})	I_{SLEEP}	120 MHz	—	23	—	mA
Capacity of pins	C_{PIN}	V_{DDE} = V_I = 0 f = 1 MHz	—	—	16	pF

(9)MB86835 (Maximum internal operation frequency:84 MHz)

(V_{DD5} = V_{DD3} = 3.3 V ± 0.15 V, V_{SS} = 0.0 V, T_A = 0 °C to + 70 °C)

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
"L" level input voltage	V_{IL}	—	0	—	$V_{DD3} \times 0.25$	V
"H" level input voltage	V_{IH}	—	$V_{DD3} \times 0.65$	—	V_{DD5}	V
"L" level output voltage	V_{OL}	I_{OL} = 2 mA	0	—	0.4	V
"H" level output voltage	V_{OH}	I_{OH} = – 2 mA	V_{DD5} – 0.5	—	V_{DD5}	V
Input leakage current	I_{LI}	V_{IN} = 0 or V_{DD5}	– 10	—	10	µA
Trial state output leakage current	I_{LZ}	V_{OUT} = 0 or V_{DD5}	– 10	—	10	µA
Power supply current (V_{DD5} + V_{DD3})	I_{DD}	84 MHz No-load	—	200	—	mA
At sleep power supply current (V_{DD3})	I_{SLEEP}	84 MHz	—	20	—	mA
Capacity of pins	C_{PIN}	V_{DD5} = V_I = 0 f = 1 MHz	—	—	16	pF

(10)MB86836-90 (Maximum internal operation frequency:90 MHz)

(V_{DD5} = 3.3 V ± 0.15 V, V_{DD3} = 2.5 V ± 0.1 V, V_{SS} = 0.0 V, T_A = 0 °C to + 70 °C)

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
"L" level input voltage	V_{IL}	—	0	—	0.8	V
"H" level input voltage	V_{IH}	—	2.0	—	V_{DD5}	V
"L" level output voltage	V_{OL}	I_{OL} = 2 mA	0	—	0.4	V
"H" level output voltage	V_{OH}	I_{OH} = – 2 mA	V_{DD5} – 0.4	—	V_{DD5}	V
Input leakage current	I_{LI}	V_{IN} = 0 or V_{DD5}	– 5	—	5	µA
Trial state output leakage current	I_{LZ}	V_{OUT} = 0 or V_{DD5}	– 5	—	5	µA
Power supply current (V_{DD5} = 3.3 V)	I_{DD}	40 MHz No-load	—	36	—	mA
Power supply current (V_{DD3} = 2.5 V)	I_{DD}	90 MHz	—	180	—	mA
At sleep power supply current	I_{SLEEP}	90 MHz	—	17	—	mA
Capacity of pins	C_{PIN}	V_{DD5} = V_I = 0 f = 1 MHz	—	—	16	pF

(11)MB86836-108 (Maximum internal operation frequency:108 MHz)

(V_{DD5} = 3.3 V ± 0.15 V, V_{DD3} = 2.5 V ± 0.1 V, V_{SS} = 0.0 V, T_A = 0 °C to + 70 °C)

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
"L" level input voltage	V_{IL}	—	0	—	0.8	V
"H" level input voltage	V_{IH}	—	2.0	—	V_{DD5}	V
"L" level output voltage	V_{OL}	I_{OL} = 2 mA	0	—	0.4	V
"H" level output voltage	V_{OH}	I_{OH} = – 2 mA	V_{DD5} – 0.4	—	V_{DD5}	V
Input leakage current	I_{LI}	V_{IN} = 0 or V_{DD5}	– 5	—	5	µA
Trial state output leakage current	I_{LZ}	V_{OUT} = 0 or V_{DD5}	– 5	—	5	µA
Power supply current (V_{DD5} = 3.3 V)	I_{DD}	40 MHz No-load	—	36	—	mA
Power supply current (V_{DD3} = 2.5 V)	I_{DD}	108 MHz	—	200	—	mA
At sleep power supply current	I_{SLEEP}	108 MHz	—	20	—	mA
Capacity of pins	C_{PIN}	V_{DD5} = V_I = 0 f = 1 MHz	—	—	16	pF

4. AC Characteristics

All are provided by CLKIN (BUS clock), and the AC characteristic does not depend on the frequency of the operation in CPU.

(1)MB86831-66/MB86832-66/MB86833 (Maximum internal operation frequency:66 MHz)

(V_{DD3} = 3.3 V ± 0.3 V, V_{SS} = 0.0 V, T_A = 0 °C to + 70 °C)

Classification	Parameter	Symbol	Value				Unit
			V_{DD5} = 5.0 V ± 5%		V_{DD5} = 3.3 V ± 0.3 V		
			Min.	Max.	Min.	Max.	
CLK	CLKIN cycle time	—	30	100	30	100	ns
	CLKIN high time	—	10	—	10	—	ns
	CLKIN low time	—	10	—	10	—	ns
	CLKIN rising time	—	—	3	—	3	ns
	CLKIN falling time	—	—	3	—	3	ns
Output	Delay time	D<31:0>	—	20	—	20	ns
	Hold time		2	—	2	—	ns
	Delay time	ADR<27:2>	—	20	—	21	ns
	Hold time		2	—	2	—	ns
	Delay time	BE0# to BE3#	—	20	—	21	ns
	Hold time		2	—	2	—	ns
	Delay time	ASI<3:0>	—	20	—	21	ns
	Hold time		2	—	2	—	ns
	Delay time	CS0# to CS5#	—	20	—	21	ns
	Hold time		2	—	2	—	ns
	Delay time	SAMEPAGE#	—	20	—	21	ns
	Hold time		2	—	2	—	ns
	Delay time	RDWR#	—	18	—	19	ns
	Hold time		2	—	2	—	ns
	Delay time	LOCK#	—	18	—	19	ns
	Hold time		2	—	2	—	ns
	Delay time	AS#	—	18	—	19	ns
	Hold time		2	—	2	—	ns
	Delay time	OVF#	—	20	—	21	ns
	Hold time		2	—	2	—	ns
	Delay time	BGRNT#	—	18	—	19	ns
	Hold time		2	—	2	—	ns
	Delay time	PBREQ#	—	18	—	19	ns
	Hold time		2	—	2	—	ns
	Delay time	BMREQ#	—	18	—	19	ns
	Hold time		2	—	2	—	ns

(Continued)

(Continued)

(V_{DD3} = 3.3 V ± 0.3 V, V_{SS} = 0.0 V, T_A = 0 °C to + 70 °C)

Classification	Parameter	Symbol	Value				Unit
			V_{DD5} = 5.0 V ± 5%		V_{DD5} = 3.3 V ± 0.3 V		
			Min.	Max.	Min.	Max.	
Output	Delay time	RDYOUT# (Internal ready mode)	—	20	—	21	ns
	Hold time		2	—	2	—	ns
	Delay time	RDYOUT# * (External ready mode)	—	15	—	15	ns
	Hold time		2	—	2	—	ns
	Delay time	ERROR#	—	20	—	21	ns
	Hold time		2	—	2	—	ns
	Delay time	PDOWN#	—	20	—	21	ns
	Hold time		2	—	2	—	ns
Input	Setup time	READY#	14	—	14	—	ns
	Hold time		2	—	2	—	ns
	Setup time	MEXC#	14	—	14	—	ns
	Hold time		2	—	2	—	ns
	Setup time	D<31:0>	14	—	14	—	ns
	Hold time		2	—	2	—	ns
	Setup time	BREQ#	12	—	12	—	ns
	Hold time		2	—	2	—	ns
	Setup time	BMACK#	12	—	12	—	ns
	Hold time		2	—	2	—	ns
	Setup time	IRL<3:0>	Asynchronous		Asynchronous		ns
	Hold time		Asynchronous		Asynchronous		ns
	Setup time	WKUP#	Asynchronous		Asynchronous		ns
	Hold time		Asynchronous		Asynchronous		ns
External bus master input	Setup time	RDWR#	12	—	12	—	ns
	Hold time		2	—	2	—	ns
	Setup time	AS#	12	—	12	—	ns
	Hold time		2	—	2	—	ns
	Input setup time	ASI<3:0>	12	—	12	—	ns
	Hold time		2	—	2	—	ns
	Setup time	ADR<27:2>	12	—	12	—	ns
	Hold time		2	—	2	—	ns
	Setup time	BE2#	12	—	12	—	ns
	Hold time		2	—	2	—	ns

(Continued)

(Continued)

(V_{DD3} = 3.3 V ± 0.3 V, V_{SS} = 0.0 V, T_A = 0 °C to + 70 °C)

Classification	Parameter	Symbol	Value				Unit
			V_{DD5} = 5.0 V ± 5%		V_{DD5} = 3.3 V ± 0.3 V		
			Min.	Max.	Min.	Max.	
DRAMC output	Delay time	RAS0# to RAS3#	—	15	—	15	ns
	Hold time		2	—	2	—	ns
	Delay time	CAS0# to CAS3#	—	15	—	15	ns
	Hold time		2	—	2	—	ns
	Delay time	DWE0# to DWE3#	—	15	—	15	ns
	Hold time		2	—	2	—	ns
	Delay time	DOE#	—	15	—	15	ns
	Hold time		2	—	2	—	ns
IRC input	Setup time	IRQ15 to IRQ8	Asynchronous		Asynchronous		ns
	Hold time		Asynchronous		Asynchronous		ns
	"H" level period		2 × P + 10	—	2 × P + 10	—	ns
	"L" level period		2 × P + 10	—	2 × P + 10	—	ns

P:Period (Cycle time)

* : RDYOUT# at the external ready mode is provided for from READY# input.

Notes

- Each parameter is valid within the specified ranges of temperatures and supply voltages unless otherwise noted.
- Each voltage value is based on the GND (V_{SS} = 0.0 V) level. The timing measurement reference point is 1.5 V, the input level is 0.4 to 2.4 V, and the input rise time and fall time are 2 ns or less.
- Do not leave more than one output pins short-circuited for 1 second or more.
- The external output load capacitance is 30 pF.
- The specifications of pins other than those pins designated as asynchronous inputs and than the RDYOUT# pin in external ready mode are determined by the rising edge of the external clock (CLKIN).
- These specifications are subject to change for improvement.
- The reset period requires at least 4 CLKIN cycles. The PLL oscillation stabilization delay time requires at least 4000 clock (CLKIN) pulses. For 40-MHz (25 ns) clock input, for example, the reset signal must therefore be negated 100 µs later.

(2)MB86831-80/MB86832-80 (Maximum internal operation frequency:80 MHz)

(V_{DD3} = 3.3 V ± 0.15 V, V_{SS} = 0.0 V, T_A = 0 °C to + 70 °C)

Classification	Parameter	Symbol	Value				Unit
			V_{DD5} = 5.0 V ± 5%		V_{DD5} = 3.3 V ± 0.15 V		
			Min.	Max.	Min.	Max.	
CLK	CLKIN cycle time	—	25	100	25	100	ns
	CLKIN high time	—	8	—	8	—	ns
	CLKIN low time	—	8	—	8	—	ns
	CLKIN rising time	—	—	3	—	3	ns
	CLKIN falling time	—	—	3	—	3	ns
Output	Delay time	D<31:0>	—	16	—	20	ns
	Hold time		2	—	2	—	ns
	Delay time	ADR<27:2>	—	18	—	21	ns
	Hold time		2	—	2	—	ns
	Delay time	BE0# to BE3#	—	16	—	21	ns
	Hold time		2	—	2	—	ns
	Delay time	ASI<3:0>	—	16	—	21	ns
	Hold time		2	—	2	—	ns
	Delay time	CS0# to CS5#	—	16	—	21	ns
	Hold time		2	—	2	—	ns
	Delay time	SAMEPAGE#	—	16	—	21	ns
	Hold time		2	—	2	—	ns
	Delay time	RDWR#	—	14	—	19	ns
	Hold time		2	—	2	—	ns
	Delay time	LOCK#	—	14	—	19	ns
	Hold time		2	—	2	—	ns
	Delay time	AS#	—	14	—	19	ns
	Hold time		2	—	2	—	ns
	Delay time	OVF#	—	16	—	21	ns
	Hold time		2	—	2	—	ns
	Delay time	BGRNT#	—	14	—	19	ns
	Hold time		2	—	2	—	ns
	Delay time	PBREQ#	—	14	—	19	ns
	Hold time		2	—	2	—	ns
	Delay time	BMREQ#	—	16	—	19	ns
	Hold time		2	—	2	—	ns
	Delay time	RDYOUT# (Internal ready mode)	—	16	—	21	ns
	Hold time		2	—	2	—	ns

(Continued)

(Continued)

(V_{DD3} = 3.3 V ± 0.15 V, V_{SS} = 0.0 V, T_A = 0 °C to + 70 °C)

Classification	Parameter	Symbol	Value				Unit
			V_{DD5} = 5.0 V ± 5%		V_{DD5} = 3.3 V ± 0.15 V		
			Min.	Max.	Min.	Max.	
Output	Delay time	RDYOUT# * (External ready mode)	—	14	—	15	ns
	Hold time		2	—	2	—	ns
	Delay time	ERROR#	—	14	—	21	ns
	Hold time		2	—	2	—	ns
	Delay time	PDOWN#	—	14	—	21	ns
	Hold time		2	—	2	—	ns
Input	Setup time	READY#	10	—	10	—	ns
	Hold time		2	—	2	—	ns
	Setup time	MEXC#	10	—	10	—	ns
	Hold time		2	—	2	—	ns
	Setup time	D<31:0>	12	—	12	—	ns
	Hold time		2	—	2	—	ns
	Setup time	BREQ#	10	—	10	—	ns
	Hold time		2	—	2	—	ns
	Setup time	BMACK#	10	—	10	—	ns
	Hold time		2	—	2	—	ns
	Setup time	IRL<3:0>	Asynchronous		Asynchronous		ns
	Hold time		Asynchronous		Asynchronous		ns
	Setup time	WKUP#	Asynchronous		Asynchronous		ns
	Hold time		Asynchronous		Asynchronous		ns
External bus master input	Setup time	RDWR#	12	—	12	—	ns
	Hold time		2	—	2	—	ns
	Setup time	AS#	12	—	12	—	ns
	Hold time		2	—	2	—	ns
	Input setup time	ASI<3:0>	12	—	12	—	ns
	Hold time		2	—	2	—	ns
	Setup time	ADR<27:2>	12	—	12	—	ns
	Hold time		2	—	2	—	ns
	Setup time	BE2#	12	—	12	—	ns
	Hold time		2	—	2	—	ns

(Continued)

(Continued)

(V_{DD3} = 3.3 V ± 0.15 V, V_{SS} = 0.0 V, T_A = 0 °C to + 70 °C)

Classification	Parameter	Symbol	Value				Unit
			V_{DD5} = 5.0 V ± 5%		V_{DD5} = 3.3 V ± 0.15 V		
			Min.	Max.	Min.	Max.	
DRAMC output	Delay time	RAS0# to RAS3#	—	12	—	15	ns
	Hold time		2	—	2	—	ns
	Delay time	CAS0# to CAS3#	—	12	—	15	ns
	Hold time		2	—	2	—	ns
	Delay time	DWE0# to DWE3#	—	12	—	15	ns
	Hold time		2	—	2	—	ns
	Delay time	DOE#	—	12	—	15	ns
	Hold time		2	—	2	—	ns
IRC input	Setup time	IRQ15 to IRQ8	Asynchronous		Asynchronous		ns
	Hold time		Asynchronous		Asynchronous		ns
	“H” level period		2 × P + 10	—	2 × P + 10	—	ns
	“L” level period		2 × P + 10	—	2 × P + 10	—	ns

P:Period (Cycle time)

* : RDYOUT# at the external ready mode is provided for from READY# input.

Notes

- Each parameter is valid within the specified ranges of temperatures and supply voltages unless otherwise noted.
- Each voltage value is based on the GND (V_{SS} = 0.0 V) level. The timing measurement reference point is 1.5 V, the input level is 0.4 to 2.4 V, and the input rise time and fall time are 2 ns or less.
- Do not leave more than one output pins short-circuited for 1 second or more.
- The external output load capacitance is 30 pF.
- The specifications of pins other than those pins designated as asynchronous inputs and than the RDYOUT# pin in external ready mode are determined by the rising edge of the external clock (CLKIN).
- These specifications are subject to change for improvement.
- The reset period requires at least 4 CLKIN cycles. The PLL oscillation stabilization delay time requires at least 4000 clock (CLKIN) pulses. For 40-MHz (25 ns) clock input, for example, the reset signal must therefore be negated 100 µs later.

(3)MB86832-100 (Maximum internal operation frequency:100 MHz)

(V_{DD3} = 3.3 V ± 0.15 V, V_{SS} = 0.0 V, T_A = 0 °C to + 70 °C)

Classification	Parameter	Symbol	Value				Unit
			V_{DD5} = 5.0 V ± 5%		V_{DD5} = 3.3 V ± 0.15 V		
			Min.	Max.	Min.	Max.	
CLK	CLKIN cycle time	—	25	100	25	100	ns
	CLKIN high time	—	10	—	10	—	ns
	CLKIN low time	—	10	—	10	—	ns
	CLKIN rising time	—	—	3	—	3	ns
	CLKIN falling time	—	—	3	—	3	ns
Output	Delay time	D<31:0>	—	16	—	20	ns
	Hold time		2	—	2	—	ns
	Delay time	ADR<27:2>	—	18	—	21	ns
	Hold time		2	—	2	—	ns
	Delay time	BE0# to BE3#	—	16	—	21	ns
	Hold time		2	—	2	—	ns
	Delay time	ASI<3:0>	—	16	—	21	ns
	Hold time		2	—	2	—	ns
	Delay time	CS0# to CS5#	—	16	—	21	ns
	Hold time		2	—	2	—	ns
	Delay time	SAMEPAGE#	—	16	—	21	ns
	Hold time		2	—	2	—	ns
	Delay time	RDWR#	—	14	—	19	ns
	Hold time		2	—	2	—	ns
	Delay time	LOCK#	—	14	—	19	ns
	Hold time		2	—	2	—	ns
	Delay time	AS#	—	14	—	19	ns
	Hold time		2	—	2	—	ns
	Delay time	OVF#	—	16	—	21	ns
	Hold time		2	—	2	—	ns
	Delay time	BGRNT#	—	14	—	19	ns
	Hold time		2	—	2	—	ns
	Delay time	PBREQ#	—	14	—	19	ns
	Hold time		2	—	2	—	ns
	Delay time	BMREQ#	—	16	—	19	ns
	Hold time		2	—	2	—	ns
	Delay time	RDYOUT# (Internal ready mode)	—	16	—	21	ns
	Hold time		2	—	2	—	ns

(Continued)

(Continued)

(V_{DD3} = 3.3 V ± 0.15 V, V_{SS} = 0.0 V, T_A = 0 °C to + 70 °C)

Classification	Parameter	Symbol	Value				Unit
			V_{DD5} = 5.0 V ± 5%		V_{DD5} = 3.3 V ± 0.15 V		
			Min.	Max.	Min.	Max.	
Output	Delay time	RDYOUT# * (External ready mode)	—	14	—	15	ns
	Hold time		2	—	2	—	ns
	Delay time	ERROR#	—	14	—	21	ns
	Hold time		2	—	2	—	ns
	Delay time	PDOWN#	—	14	—	21	ns
	Hold time		2	—	2	—	ns
Input	Setup time	READY#	10	—	10	—	ns
	Hold time		2	—	2	—	ns
	Setup time	MEXC#	10	—	10	—	ns
	Hold time		2	—	2	—	ns
	Setup time	D<31:0>	12	—	12	—	ns
	Hold time		2	—	2	—	ns
	Setup time	BREQ#	10	—	10	—	ns
	Hold time		2	—	2	—	ns
	Setup time	BMACK#	10	—	10	—	ns
	Hold time		2	—	2	—	ns
	Setup time	IRL<3:0>	Asynchronous		Asynchronous		ns
	Hold time		Asynchronous		Asynchronous		ns
	Setup time	WKUP#	Asynchronous		Asynchronous		ns
	Hold time		Asynchronous		Asynchronous		ns
External bus master input	Setup time	RDWR#	12	—	12	—	ns
	Hold time		2	—	2	—	ns
	Setup time	AS#	12	—	12	—	ns
	Hold time		2	—	2	—	ns
	Input Setup time	ASI<3:0>	12	—	12	—	ns
	Hold time		2	—	2	—	ns
	Setup time	ADR<27:2>	12	—	12	—	ns
	Hold time		2	—	2	—	ns
	Setup time	BE2#	12	—	12	—	ns
	Hold time		2	—	2	—	ns

(Continued)

(Continued)

(V_{DD3} = 3.3 V ± 0.15 V, V_{SS} = 0.0 V, T_A = 0 °C to + 70 °C)

Classification	Parameter	Symbol	Value				Unit
			V_{DD5} = 5.0 V ± 5%		V_{DD5} = 3.3 V ± 0.15 V		
			Min.	Max.	Min.	Max.	
DRAMC output	Delay time	RAS0# to RAS3#	—	12	—	15	ns
	Hold time		2	—	2	—	ns
	Delay time	CAS0# to CAS3#	—	12	—	15	ns
	Hold time		2	—	2	—	ns
	Delay time	DWE0# to DWE3#	—	12	—	15	ns
	Hold time		2	—	2	—	ns
	Delay time	DOE#	—	12	—	15	ns
	Hold time		2	—	2	—	ns
IRC input	Setup time	IRQ15 to IRQ8	Asynchronous		Asynchronous		ns
	Hold time		Asynchronous		Asynchronous		ns
	"H" level period		2 × P + 10	—	2 × P + 10	—	ns
	"L" level period		2 × P + 10	—	2 × P + 10	—	ns

P:Period (Cycle time)

* : RDYOUT# at the external ready mode is provided for from READY# input.

Notes

- Each parameter is valid within the specified ranges of temperatures and supply voltages unless otherwise noted.
- Each voltage value is based on the GND (V_{SS} = 0.0 V) level. The timing measurement reference point is 1.5 V, the input level is 0.4 to 2.4 V, and the input rise time and fall time are 2 ns or less.
- Do not leave more than one output pins short-circuited for 1 second or more.
- The external output load capacitance is 30 pF.
- The specifications of pins other than those pins designated as asynchronous inputs and than the RDYOUT# pin in external ready mode are determined by the rising edge of the external clock (CLKIN).
- These specifications are subject to change for improvement.
- The reset period requires at least 4 CLKIN cycles. The PLL oscillation stabilization delay time requires at least 4000 clock (CLKIN) pulses. For 40-MHz (25 ns) clock input, for example, the reset signal must therefore be negated 100 µs later.

(4)MB86834-108,-120

(V_{DD5} = 3.3 V ± 0.15 V, V_{DD3} = 2.5 V ± 0.1 V, V_{SS} = 0.0 V, T_A = 0 °C to + 70 °C)

Classification	Parameter	Symbol	Value		Unit
			Min.	Max.	
CLK	CLKIN cycle time	—	25	40	ns
	CLKIN high time	—	8	—	ns
	CLKIN low time	—	8	—	ns
	CLKIN rising time	—	—	3	ns
	CLKIN falling time	—	—	3	ns
Output	Delay time	D<31:0>	—	20	ns
	Hold time		2	—	ns
	Delay time	ADR<27:2>	—	21	ns
	Hold time		2	—	ns
	Delay time	BE0# to BE3#	—	21	ns
	Hold time		2	—	ns
	Delay time	ASI<3:0>	—	21	ns
	Hold time		2	—	ns
	Delay time	CS0# to CS5#	—	21	ns
	Hold time		2	—	ns
	Delay time	SAMEPAGE#	—	21	ns
	Hold time		2	—	ns
	Delay time	RDWR#	—	19	ns
	Hold time		2	—	ns
	Delay time	LOCK#	—	19	ns
	Hold time		2	—	ns
	Delay time	AS#	—	19	ns
	Hold time		2	—	ns
	Delay time	OVF#	—	21	ns
	Hold time		2	—	ns
	Delay time	BGRNT#	—	19	ns
	Hold time		2	—	ns
	Delay time	PBREQ#	—	19	ns
	Hold time		2	—	ns
	Delay time	BMREQ#	—	19	ns
	Hold time		2	—	ns

(Continued)

(Continued)

(V_{DD5} = 3.3 V ± 0.15 V, V_{DD3} = 2.5 V ± 0.1 V, V_{SS} = 0.0 V, T_A = 0 °C to + 70 °C)

Classification	Parameter	Symbol	Value		Unit
			Min.	Max.	
Output	Delay time	RDYOUT# (Internal ready mode)	—	21	ns
	Hold time		2	—	ns
	Delay time	RDYOUT# * (External ready mode)	—	15	ns
	Hold time		2	—	ns
	Delay time	ERROR#	—	21	ns
	Hold time		2	—	ns
	Delay time	PDOWN#	—	21	ns
	Hold time		2	—	ns
Input	Setup time	READY#	10	—	ns
	Hold time		2	—	ns
	Setup time	MEXC#	10	—	ns
	Hold time		2	—	ns
	Setup time	D<31:0>	12	—	ns
	Hold time		2	—	ns
	Setup time	BREQ#	10	—	ns
	Hold time		2	—	ns
	Setup time	BMACK#	10	—	ns
	Hold time		2	—	ns
	Setup time	IRL<3:0>	Asynchronous		ns
	Hold time		Asynchronous		ns
	Setup time	WKUP#	Asynchronous		ns
	Hold time		Asynchronous		ns
External bus master input	Setup time	RDWR#	12	—	ns
	Hold time		2	—	ns
	Setup time	AS#	12	—	ns
	Hold time		2	—	ns
	Input setup time	ASI<3:0>	12	—	ns
	Hold time		2	—	ns
	Setup time	ADR<27:2>	12	—	ns
	Hold time		2	—	ns
	Setup time	BE2#	12	—	ns
	Hold time		2	—	ns

(Continued)

(Continued)

(V_{DD5} = 3.3 V ± 0.15 V, V_{DD3} = 2.5 V ± 0.1 V, V_{SS} = 0.0 V, T_A = 0 °C to + 70 °C)

Classification	Parameter	Symbol	Value		Unit
			Min.	Max.	
DRAM-Coutput	Delay time	RAS0# to RAS3#	—	15	ns
	Hold time		2	—	ns
	Delay time	CAS0# to CAS3#	—	15	ns
	Hold time		2	—	ns
	Delay time	DWE0# to DWE3#	—	15	ns
	Hold time		2	—	ns
	Delay time	DOE#	—	15	ns
	Hold time		2	—	ns
IRC input	Setup time	IRQ15 to IRQ8	Asynchronous		ns
	Hold time		Asynchronous		ns
	“H” level period		2 × P + 10	—	ns
	“L” level period		2 × P + 10	—	ns

P:Period (Cycle time)

* : RDYOUT# at the external ready mode is provided for from READY# input.

Notes

- Each parameter is valid within the specified ranges of temperatures and supply voltages unless otherwise noted.
- Each voltage value is based on the GND (V_{SS} = 0.0 V) level. The timing measurement reference point is 1.5 V, the input level is 0.4 to 2.4 V, and the input rise time and fall time are 2 ns or less.
- Do not leave more than one output pins short-circuited for 1 second or more.
- The external output load capacitance is 30 pF.
- The specifications of pins other than those pins designated as asynchronous inputs and than the RDYOUT# pin in external ready mode are determined by the rising edge of the external clock (CLKIN).
- These specifications are subject to change for improvement.
- The reset period requires at least 4 CLKIN cycles. The PLL oscillation stabilization delay time requires at least 4000 clock (CLKIN) pulses. For 40 MHz (25 ns) clock input, for example, the reset signal must therefore be negated 100 µs later.

(5)MB86835

(V_{DD5} = V_{DD3} = 3.3 V ± 0.15 V, V_{SS} = 0.0 V, T_A = 0 °C to + 70 °C)

Classification	Parameter	Symbol	Value		Unit
			MB86835		
			Min.	Max.	
CLK	CLKIN cycle time	—	25	100	ns
	CLKIN high time	—	8	—	ns
	CLKIN low time	—	8	—	ns
	CLKIN rising time	—	—	3	ns
	CLKIN falling time	—	—	3	ns
Output	Delay time	D<31:0>	—	20	ns
	Hold time		2	—	ns
	Delay time	ADR<27:2>	—	21	ns
	Hold time		2	—	ns
	Delay time	BE0# to BE3#	—	21	ns
	Hold time		2	—	ns
	Delay time	ASI<3:0>	—	21	ns
	Hold time		2	—	ns
	Delay time	CS0# to CS5#	—	21	ns
	Hold time		2	—	ns
	Delay time	SAMEPAGE#	—	21	ns
	Hold time		2	—	ns
	Delay time	RDWR#	—	19	ns
	Hold time		2	—	ns
	Delay time	LOCK#	—	19	ns
	Hold time		2	—	ns
	Delay time	AS#	—	19	ns
	Hold time		2	—	ns
	Delay time	OVF#	—	21	ns
	Hold time		2	—	ns
	Delay time	BGRNT#	—	19	ns
	Hold time		2	—	ns
	Delay time	PBREQ#	—	19	ns
	Hold time		2	—	ns
	Delay time	BMREQ#	—	19	ns
	Hold time		2	—	ns

(Continued)

(Continued)

(V_{DD3} = 3.3 V ± 0.15 V, V_{SS} = 0.0 V, T_A = 0 °C to + 70 °C)

Classification	Parameter	Symbol	Value		Unit
			MB86835		
			Min.	Max.	
Output	Delay time	RDYOUT# (Internal ready mode)	—	21	ns
	Hold time		2	—	ns
	Delay time	RDYOUT# * (External ready mode)	—	15	ns
	Hold time		2	—	ns
	Delay time	ERROR#	—	21	ns
	Hold time		2	—	ns
	Delay time	PDOWN#	—	21	ns
	Hold time		2	—	ns
Input	Setup time	READY#	10	—	ns
	Hold time		2	—	ns
	Setup time	MEXC#	10	—	ns
	Hold time		2	—	ns
	Setup time	D<31:0>	12	—	ns
	Hold time		2	—	ns
	Setup time	BREQ#	10	—	ns
	Hold time		2	—	ns
	Setup time	BMACK#	10	—	ns
	Hold time		2	—	ns
	Setup time	IRL<3:0>	Asynchronous		ns
	Hold time		Asynchronous		ns
	Setup time	WKUP#	Asynchronous		ns
	Hold time		Asynchronous		ns
External bus master input	Setup time	RDWR#	12	—	ns
	Hold time		2	—	ns
	Setup time	AS#	12	—	ns
	Hold time		2	—	ns
	Input setup time	ASI<3:0>	12	—	ns
	Hold time		2	—	ns
	Setup time	ADR<27:2>	12	—	ns
	Hold time		2	—	ns
	Setup time	BE2#	12	—	ns
	Hold time		2	—	ns

(Continued)

(Continued)

(V_{DD3} = 3.3 V ± 0.15 V, V_{SS} = 0.0 V, T_A = 0 °C to + 70 °C)

Classification	Parameter	Symbol	Value		Unit
			MB86835		
			Min.	Max.	
DRAMC output	Delay time	RAS0# to RAS3#	—	15	ns
	Hold time		2	—	ns
	Delay time	CAS0# to CAS3#	—	15	ns
	Hold time		2	—	ns
	Delay time	DWE0# to DWE3#	—	15	ns
	Hold time		2	—	ns
	Delay time	DOE#	—	15	ns
	Hold time		2	—	ns
IRC nput	Setup time	IRQ15 to IRQ8	Asynchronous		ns
	Hold time		Asynchronous		ns
	"H" level period		2 × P + 10	—	ns
	"L" level period		2 × P + 10	—	ns

P:Period (Cycle time)

* : RDYOUT# at the external ready mode is provided for from READY# input.

Notes

- Each parameter is valid within the specified ranges of temperatures and supply voltages unless otherwise noted.
- Each voltage value is based on the GND (V_{SS} = 0.0 V) level. The timing measurement reference point is 1.5 V, the input level is 0.4 to 2.4 V, and the input rise time and fall time are 2 ns or less.
- Do not leave more than one output pins short-circuited for 1 second or more.
- The external output load capacitance is 30 pF.
- The specifications of pins other than those pins designated as asynchronous inputs and than the RDYOUT# pin in external ready mode are determined by the rising edge of the external clock (CLKIN).
- These specifications are subject to change for improvement.
- The reset period requires at least 4 CLKIN cycles. The PLL oscillation stabilization delay time requires at least 4000 clock (CLKIN) pulses. For 40 MHz (25 ns) clock input, for example, the reset signal must therefore be negated 100 µs later.
- An AC characteristic of pins and internal maximum operation frequency is separately defined.
- The maximum operation frequency of an external bus is 40MHz though the maximum internal operation frequency are 80 MHz or 100 MHz (CLKIN Min.=25ns).Therefore,when an external bus is used with 40MHz, an internal frequency are 84 MHz and 100 MHz.
- Relation between external bus clock and internal clock

CLKIN	MB86835(84MHz)				
	× 1	× 2	× 3	× 4	× 5
20 MHz	20 MHz	40 MHz	60 MHz	80 MHz	N/A
33.3 MHz	33.3 MHz	66.6 MHz	N/A	N/A	N/A
40 MHz	40 MHz	80 MHz	N/A	N/A	N/A

(6)MB86836-90,-108(Preliminary)

(V_{DD5} = 3.3 V ± 0.15 V, V_{DD3} = 2.5 V ± 0.1 V, V_{SS} = 0.0 V, T_A = 0 °C to + 70 °C)

Classification	Parameter	Symbol	Value		Unit
			Min.	Max.	
CLK	CLKIN cycle time	—	25	40	ns
	CLKIN high time	—	8	—	ns
	CLKIN low time	—	8	—	ns
	CLKIN rising time	—	—	3	ns
	CLKIN falling time	—	—	3	ns
Output	Delay time	D<31:0>	—	20	ns
	Hold time		2	—	ns
	Delay time	ADR<27:2>	—	21	ns
	Hold time		2	—	ns
	Delay time	BE0# to BE3#	—	21	ns
	Hold time		2	—	ns
	Delay time	ASI<3:0>	—	21	ns
	Hold time		2	—	ns
	Delay time	CS0# to CS5#	—	21	ns
	Hold time		2	—	ns
	Delay time	SAMEPAGE#	—	21	ns
	Hold time		2	—	ns
	Delay time	RDWR#	—	19	ns
	Hold time		2	—	ns
	Delay time	LOCK#	—	19	ns
	Hold time		2	—	ns
	Delay time	AS#	—	19	ns
	Hold time		2	—	ns
	Delay time	OVF#	—	21	ns
	Hold time		2	—	ns
	Delay time	BGRNT#	—	19	ns
	Hold time		2	—	ns
	Delay time	PBREQ#	—	19	ns
	Hold time		2	—	ns
	Delay time	BMREQ#	—	19	ns
	Hold time		2	—	ns

(Continued)

(Continued)

(V_{DD5} = 3.3 V ± 0.15 V, V_{DD3} = 2.5 V ± 0.1 V, V_{SS} = 0.0 V, T_A = 0 °C to + 70 °C)

Classification	Parameter	Symbol	Value		Unit
			Min.	Max.	
Output	Delay time	RDYOUT# (Internal ready mode)	—	21	ns
	Hold time		2	—	ns
	Delay time	RDYOUT# * (External ready mode)	—	15	ns
	Hold time		2	—	ns
	Delay time	ERROR#	—	21	ns
	Hold time		2	—	ns
	Delay time	PDOWN#	—	21	ns
	Hold time		2	—	ns
Input	Setup time	READY#	10	—	ns
	Hold time		2	—	ns
	Setup time	MEXC#	10	—	ns
	Hold time		2	—	ns
	Setup time	D<31:0>	12	—	ns
	Hold time		2	—	ns
	Setup time	BREQ#	10	—	ns
	Hold time		2	—	ns
	Setup time	BMACK#	10	—	ns
	Hold time		2	—	ns
	Setup time	IRL<3:0>	Asynchronous		ns
	Hold time		Asynchronous		ns
	Setup time	WKUP#	Asynchronous		ns
	Hold time		Asynchronous		ns
External bus master input	Setup time	RDWR#	12	—	ns
	Hold time		2	—	ns
	Setup time	AS#	12	—	ns
	Hold time		2	—	ns
	Input setup time	ASI<3:0>	12	—	ns
	Hold time		2	—	ns
	Setup time	ADR<27:2>	12	—	ns
	Hold time		2	—	ns
	Setup time	BE2#	12	—	ns
	Hold time		2	—	ns

(Continued)

(Continued)

(V_{DD5} = 3.3 V ± 0.15 V, V_{DD3} = 2.5 V ± 0.1 V, V_{SS} = 0.0 V, T_A = 0 °C to + 70 °C)

Classification	Parameter	Symbol	Value		Unit
			Min.	Max.	
DRAM-Coutput	Delay time	RAS0# to RAS3#	—	15	ns
	Hold time		2	—	ns
	Delay time	CAS0# to CAS3#	—	15	ns
	Hold time		2	—	ns
	Delay time	DWE0# to DWE3#	—	15	ns
	Hold time		2	—	ns
	Delay time	DOE#	—	15	ns
	Hold time		2	—	ns
IRC input	Setup time	IRQ15 to IRQ8	Asynchronous		ns
	Hold time		Asynchronous		ns
	"H" level period		2 × P + 10	—	ns
	"L" level period		2 × P + 10	—	ns

P:Period (Cycle time)

* : RDYOUT# at the external ready mode is provided for from READY# input.

Notes

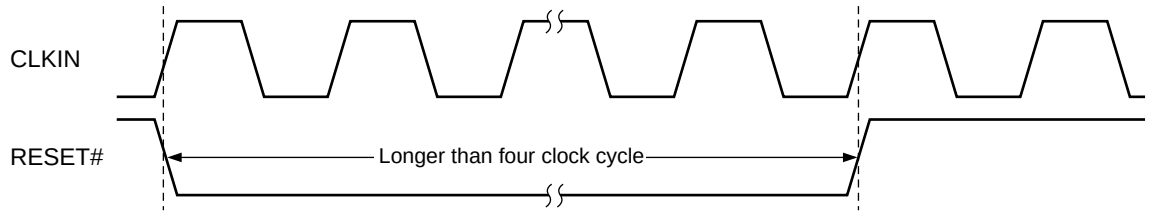
- Each parameter is valid within the specified ranges of temperatures and supply voltages unless otherwise noted.
- Each voltage value is based on the GND (V_{SS} = 0.0 V) level. The timing measurement reference point is 1.5 V, the input level is 0.4 to 2.4 V, and the input rise time and fall time are 2 ns or less.
- Do not leave more than one output pins short-circuited for 1 second or more.
- The external output load capacitance is 30 pF.
- The specifications of pins other than those pins designated as asynchronous inputs and than the RDYOUT# pin in external ready mode are determined by the rising edge of the external clock (CLKIN).
- These specifications are subject to change for improvement.
- The reset period requires at least 4 CLKIN cycles. The PLL oscillation stabilization delay time requires at least 4000 clock (CLKIN) pulses. For 40 MHz (25 ns) clock input, for example, the reset signal must therefore be negated 100 µs later.
- An AC characteristic of pins and internal maximum operation frequency is separately defined.
- The maximum operation frequency of an external bus is 40MHz though the maximum internal operation frequency are 90 MHz or 100 MHz (CLKIN Min.=25ns).Therefore,when an external bus is used with 40MHz, an internal frequency is 80 MHz
- Relation between external bus clock and internal clock

CLKIN	MB86836(90MHz)					MB86836(108MHz)*				
	× 1	× 2	× 3	× 4	× 5	× 1	× 2	× 3	× 4	× 5
27 MHz	27 MHz	54 MHz	81 MHz	N/A	N/A	27 MHz	54 MHz	81 MHz	108 MHz	N/A
33.3 MHz	33.3 MHz	66.6 MHz	N/A	N/A	N/A	33.3 MHz	66.6 MHz	100MHz	N/A	N/A
36 MHz	36MHz	72 MHz	N/A	N/A	N/A	36MHz	72 MHz	108MHz	N/A	N/A
40 MHz	40 MHz	80 MHz	N/A	N/A	N/A	40 MHz	80 MHz	N/A	N/A	N/A

*: MB86836 108MHz version is under developement.

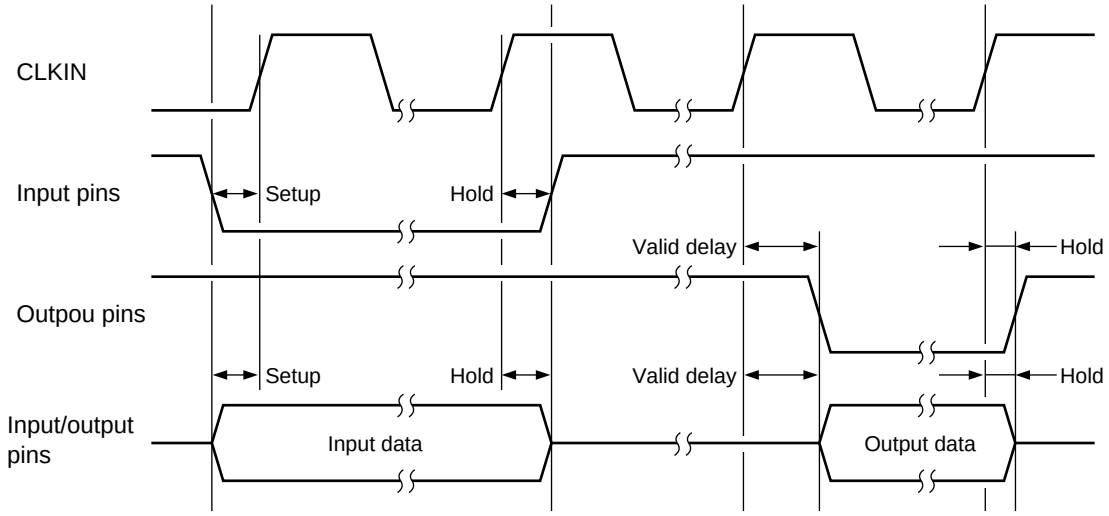
■ TIMING DIAGRAM

- Reset timing



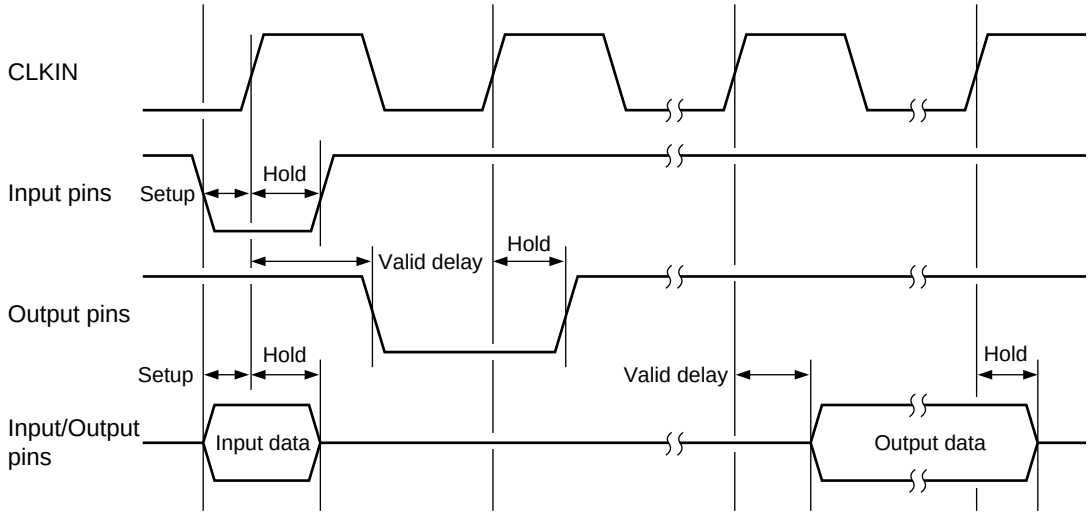
Note : CLKIN is steady, and raise reset input "H", please after at least 100msec.

- Input/output timing 1



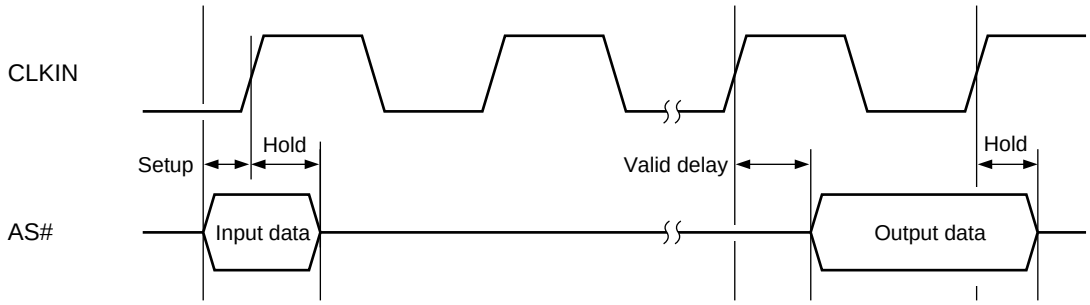
Input pins : BREQ#, BMACK#
Outpou pins : BE0# to BE1#, BE3#, CS0# to CS5#, SAMEPAGE#, LOCK#, OVF#, BGRNT#, PBREQ#, BMREQ#, ERROR#, PDOWN#, RAS0# to RAS3#, CAS0# to CAS3#, DWE0# to DWE3#, DOE#
Input/output pins : D<31: 0>, ASI<3: 0>, RDWR#, BE2#

- Input/output timing 2

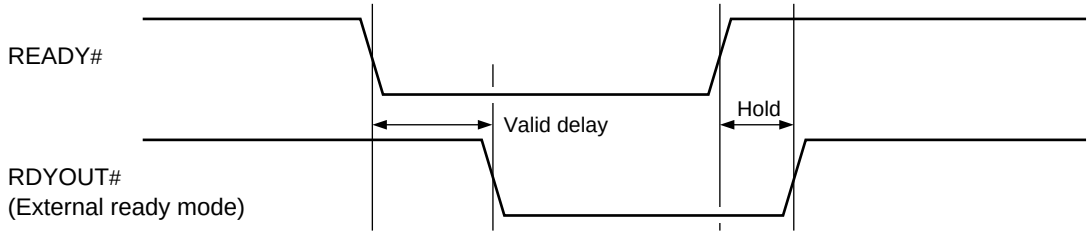


Imput pins : READY#, MEXC#
Output pins : RDYOUT# (internal ready mode)
Input/output pins : ADR<27: 2>

- Input/output timing 3



- Input/output timing 4



■ ARCHITECTURE

The MB86830 series is a line of 32-bit RISC processors running at an operating frequency of 100 MHz, providing high performance of 121 VAX-MIPS. As products belong to the Fujitsu SPARClite family, the MB86830 series is based on the SPARC architecture and are thus upward code-compatible with the conventional products in the SPARClite family. The MB86830 series was developed in particular for embedded applications, providing high performance and high level of integration when used as embedded controllers.
The MB86830 series has an efficient set of instructions and is hardwired so that most of them can be executed in one cycle. The IU (integer unit) features five pipelined execution stages designed for processing data interlocks, providing a branch handler optimized for for efficient transition of control and a bus interface for processing one-cycle bus access for on-chip memory.
The internal register file consisting of a stack of eight windows, made up of 136 registers in total, speeds up interrupt response and context switching. The register file minimizes memory access during procedure linkage and facilitates parameter passing and variable assignment.
The MB86830 series contains instruction and data caches to isolate processor operation from external memory. These caches are designed for highest flexibility so that it can lock each entry to improve the performance of the entire system.
The independent instruction and internal data buses serve as high-bandwidth interfaces between the IU (integer unit) and the on-chip caches. These buses support single-cycle instruction execution and single-cycle data transfer between the IU and caches in parallel.
The MB86830 series incorporates an integer multiplier and auxiliary hardware for division. The MB86830 series can therefore execute 32-bit integer multiplication in five cycles, 16-bit integer multiplication in three cycles, 8-bit integer multiplication in two cycles, and integer multiplication by 0 in one cycle.

1. Main Features

(1)High-speed execution of instructions
Most of the instructions in most programs are simple, designing the programs so as to execute such simple instructions as fast as possible dramatically improves the program execution time.

(2)High-capacity register set
The register set reduces the number of required accesses to data memory. Registers are organized into a stack of groups called register windows, allowing themselves to be used efficiently for high-priority tasks such as interrupt services and operating system working registers. A stack of (overlapping) register windows also contributes to simplifying parameter passing during procedure linkage, thereby reducing the code size of most programs.

(3)On-chip caches
The MB86830 series incorporates data and instruction caches so that the processor can work independently of the slower memory subsystem. These caches are implemented in two-way set-associative configuration on the MB86831/832; they are directly mapped on the MB86833.

(4)Locking entries in caches
The MB86830 series can lock both of data and instruction entries in their respective caches, ensuring high performance in processing important or frequently called routines. Each cache offers maximum flexibility so that entries can be locked in all or selective part of the cache.

(5)Bus interface
The MB86830 series supports programmable chip selection, a wait state generator, and fast page mode DRAM, minimizing the necessity of connecting external circuits.

(6)On-chip DRAM controller
The on-chip DRAM controller supports fast page mode and EDO DRAMs. It also controls self-refreshing of DRAM in sleep mode (low power consumption mode).

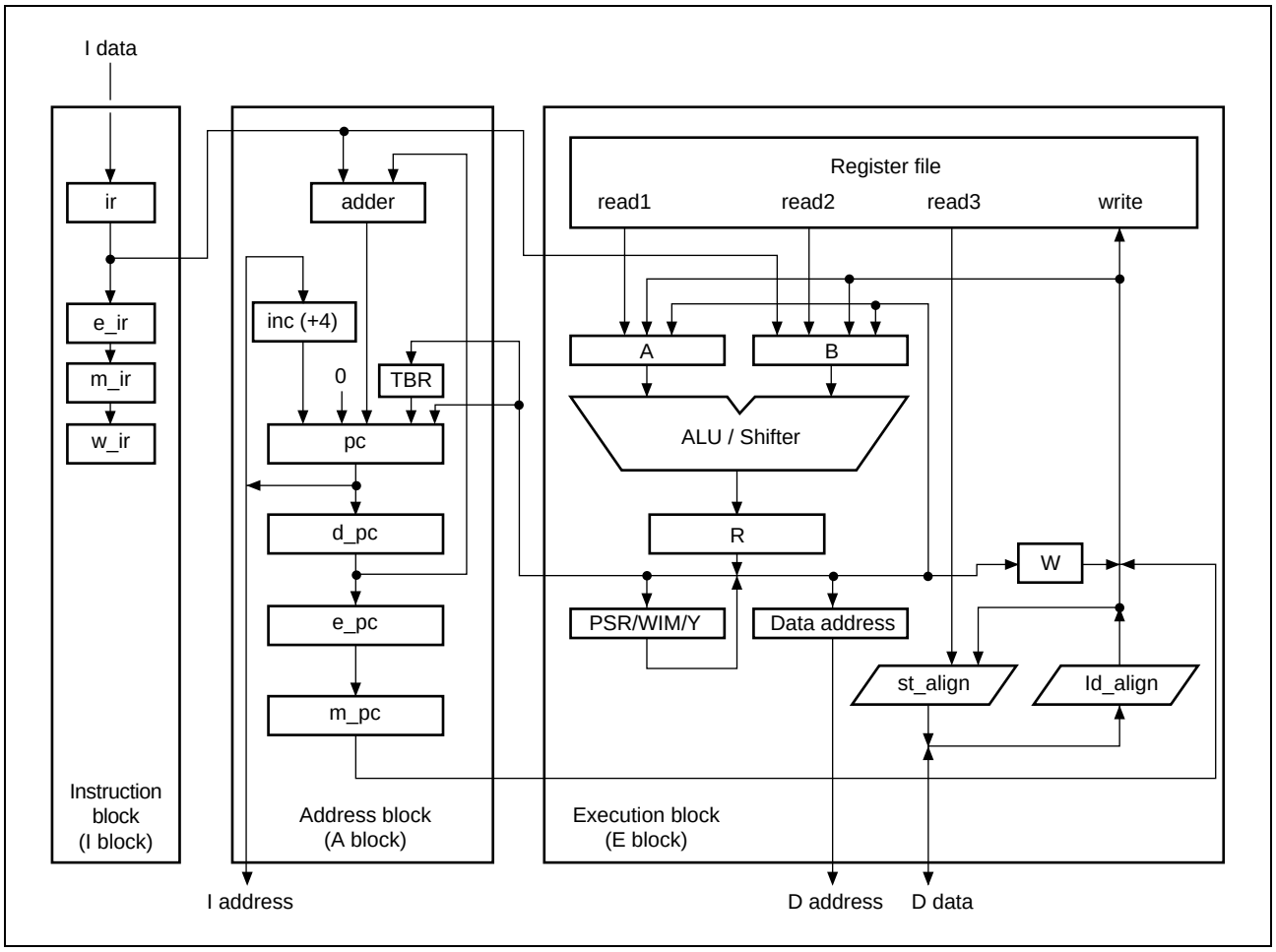
(7)On-chip interrupt controller
The on-chip interrupt controller accepts interrupt inputs through eight channels, allowing a trigger mode to be set independently for each of the channels. The interrupt request accepted according to the trigger mode is encoded and output to the processor.

(8)Multiplier circuit
The MB86830 series incorporates a multiplier circuit which can be selectively set to an operating clock frequency of x1, x2, x3, x4,or x5 of the external clock frequency, allowing the processor to run at high speed.

(9) Instruction set
The MB86830 series supports high-speed integer multiply instructions which are executed in five, three, and two cycles respectively for 32-, 16-, and 8-bit multiplications. The integer divide step instruction is near 10 times faster in divide time than the previous SPARC implementation. The scan instruction supports the function for detecting 1 or 0 at the MSB in a word in a single cycle.

2. CPU
The CPU core of the MB86830 series is a high-performance version implemented by full custom design of the SPARC architecture. The CPU core contains a compact circuitry for integrating peripheral circuits, designed to be customizable to a variety of applications. The CPU core consists of three function units: instruction, address, and execution blocks (see “Integer operation unit internal block diagram”).
The role of five execution stages for instruction pipelining is to decode all instructions and generate control signals for other blocks. The five pipelined stages are the fetch (F), decode (D), execute (E), memory (M), and write back (W) stages. The instruction memory returns an instruction addressed at stage (F), the register file returns an operand addressed at stage (D), the ALU perform calculation to obtain the result at stage(E), the external memory is addressed at stage(M), and the register file is written back at stage (W).

- Integer operation unit internal block diagram



3. Address Space

The MB86830 series has a wide addressable range in which user and supervisor spaces can be defined independently. Of 30 lines of addresses, eight lines of address space identifiers (ASI) are used to distinguish between protected and unprotected spaces. Tow of 256 different ASI values are used to define the user data and user instruction spaces; the rest are used to define the supervisor space.

When a reset, synchronous trap, or asynchronous trap occurs, the processor enters the supervisor mode. In the supervisor mode, the processor executes instructions in the supervisor space and transfers data. The processor can access other ASI values even when staying in the supervisor mode. The processor can use the remaining ASI values, excluding the reserved values, to allocate other spaces as application definable spaces.

By distinguishing between the user and supervisor spaces, hardware can prevent inadvertent or unauthorized access to system resources. When a real-time operating system (RTOS) is developed, for example, individual spaces provide the mechanism for separating the RTOS space efficiently from the user space.

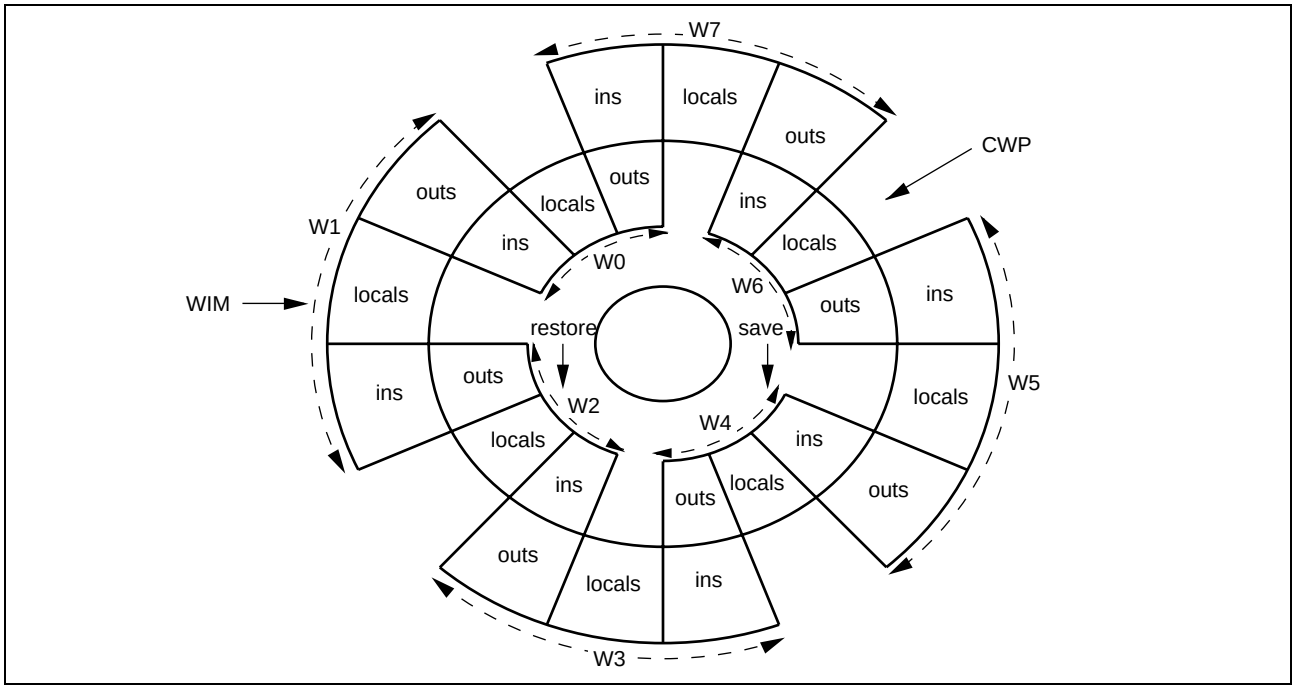
4. Registers

The register set of the MB86830 series is made up of the registers to be used for general-purpose functions and those to be used for control and status report purpose. The MB86830 series has 136 general-purpose registers divided into eight global registers and a stack of eight register blocks (register windows). Each register window incorporates 24 registers, of which eight registers are local to that window, eight “out” registers are overlapping the next register window, and eight “in” registers are overlapping the previous register window. (See “General register composition”.)

This register configuration allows a parameter to be passed to a subroutine. The next register window is made

available b writing the parameter to be passed to the “out” register and using a procedure call to decrement the window pointer by one. The passed parameter remains in the “in“ registers in the current register window and can be used by that subroutine.
Register windows improve the performance of embedded applications. This is because these windows serve as the local variable caches for storing interrupt, subroutine, context, or operating system variables without increasing overhead. In addition, the code size of programs can be reduced by using an efficient method of executing procedure linkage without optimizing the code using an inlining compiler.
The register file consists of 4-port registers: 3-port read and 1-port write registers. Even the store instruction can therefore be executed in one cycle, which requires three operands to be read from the register file.
The control and status registers are divided into those defined in the SPARC architecture and those mapped into the alternate address space for controlling the functions of peripheral devices.

- General register composition



5. Instruction Set

The MB86830 series is upward code-compatible with other SPARC processors. The MB86830 series now supports additional instructions to improve performance, which were previously not directly supported. In addition to a set of already supported SPARC instructions, the MB86830 series has been provided with the integer multiply and integer divide step instructions as well as the scan instruction for detecting “1” or “0” at the MSB.
For the list of supported instructions, see the instruction set below.

- Instruction set

LOGICAL	ARITHMETIC/SHIFT	DATA MOVEMENT
CONDITION CODES UNCHANGED AND OR XOR AND NOT OR NOT XNOR CONDITION CODES SET AND OR XOR AND NOT OR NOT XNOR	CONDITION CODES UNCHANGED ADD SUBTRACT MULTIPLY (SIGNED/UNSIGNED) SCAN SETHI SHIFT LEFT LOGICAL SHIFT RIGHT LOGICAL SHIFT RIGHT ARITHMETIC CONDITION CODES SET ADD SUBTRACT MULTIPLY (SIGNED/UNSIGNED) MULTIPLY STEP DIVIDE STEP	TO USER/SUPERVISOR SPACE SIGNED LOAD BYTE LOAD HALF-WORD LOAD WORD LOAD DOUBLE WORD STORE BYTE STORE HALF-WORD STORE WORD STORE DOUBLE WORD TO USER SPACE UNSIGNED LOAD BYTE LOAD HALF-WORD TO ALTERNATE SPACE SIGNED LOAD BYTE LOAD HALF-WORD LOAD WORD LOAD DOUBLE WORD STORE BYTE STORE HALF-WORD STORE WORD STORE DOUBLE WORD TO ALTERNATE SPACE UNSIGNED LOAD BYTE LOAD HALF-WORD ATOMIC OPERATION IN USER SPACE SWAP WORD LOAD/STORE UNSIGNED BYTE ATOMIC OPERATION IN ALTERNATE SPACE SWAP WORD LOAD/STORE UNSIGEND BYTE
CONTROL TRANSFER	EXTENDED AND CONDITION CODES UNCHANGED ADD SUBTRACT EXTENDED AND CONDITION CODES SET ADD SUBTRACT TAGGED AND CONDITION CODES SET (WITH AND WITHOUT TRAP ON OVERFLOW) ADD SUBTRACT	
CONDITIONAL BRANCH CONDITIONAL TRAP CALL RETURN SAVE RESTORE JUMP AND LINK		
READ/WRITE CONTROL REGISTER		
READ PSR WRITE PSR READ TBR WRITE TBR	READ WIM WRITE WIM READ Y WRITE Y	RDASR WRASR

6. Interrupts

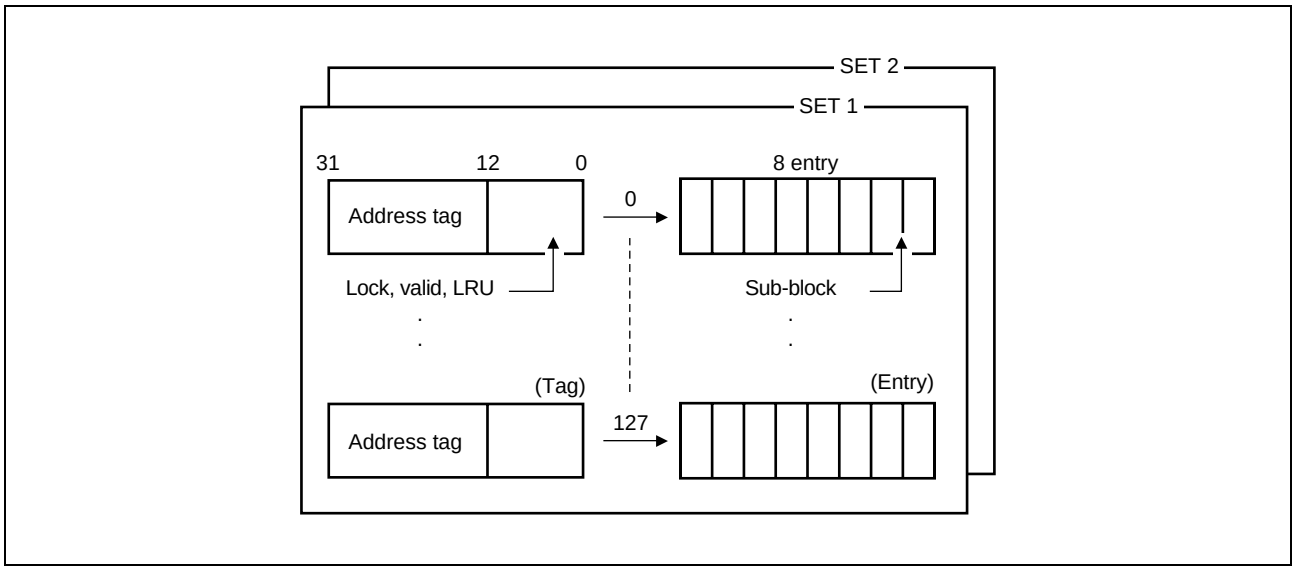
One of the key criteria to determine whether a processor is suitable for embedded applications is whether the processor can completely service interrupts within the minimum interrupt processing time. The processors implemented as the MB86830 series guarantee not only short average wait time but also short maximum wait time.
The interrupt response time is the sum of the time for the processor to complete the current task after recognizing an interrupt and the time for the processor to start executing the interrupt service routine. The MB86830 series offers a variety of functions to minimize the both factors.
To minimize the time to complete the current task, the MB86830 series is designed so that the task can be interrupted easily or it can be completed in a minimum of cycles. For this purpose, the MB86830 series implements the cache system that updates only one word at a time using a prefetch buffer when a cache miss occurs, interruptible integer division using a divide step instruction, high-speed multiplication using a multiplier, and a 4-word write buffer for processing a pending bus transaction.
To minimize the time required for starting executing the interrupt service routine, the processor switches the register window to a new one upon detection of an interrupt. This function allows the service routine to be executed

without saving the current register in advance. The user can also lock the service routine in the cache, allowing faster processing with the routine. At this time, the on-chip data cache can be used as a high-speed local stack to minimize the delay in accessing the routine variable in the service routine.
The MB86830 series has a maximum of 15 interrupt levels to directly support 15 interrupt sources. The highest interrupt level is nonmaskable.

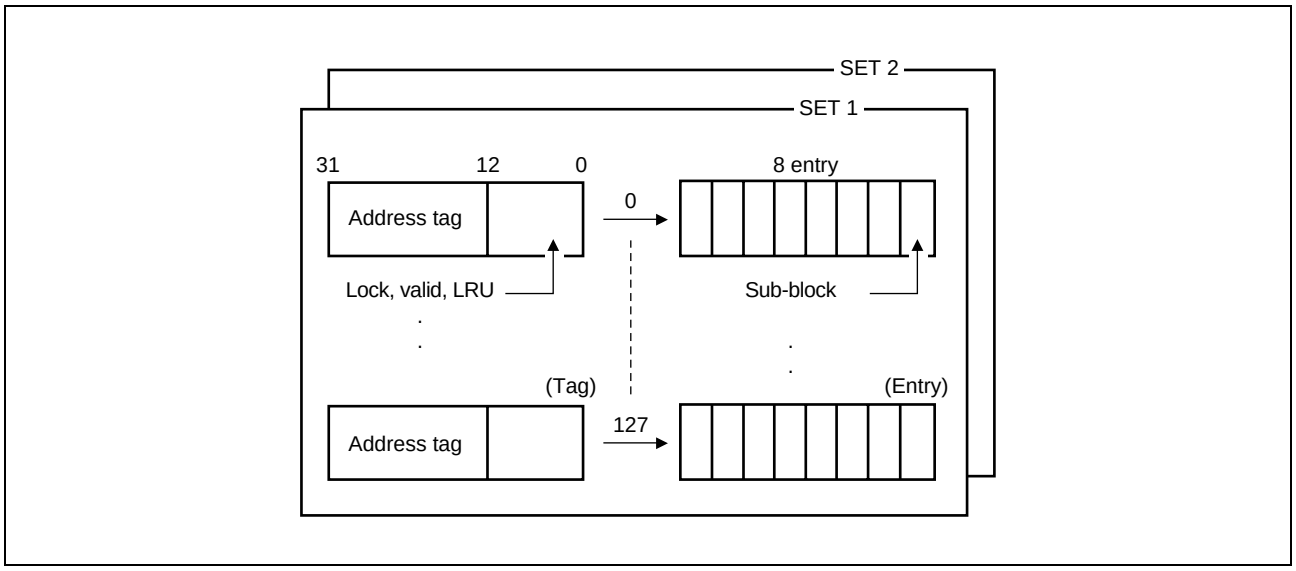
7. Caches

The MB86830 series incorporates independent data and instruction caches, allowing a high-performance system to be constructed without the need for high-speed external memory or relevant control logics. The caches are mapped onto physical addresses.
The instruction cache consists of: 64 units/2 banks on the MB86831/835, 128 units/2 banks on the MB86832/836, 256 units/2 banks on a 32-byte line on the MB86834, and 64 units/1 bank on a 16-byte line on the MB86833. The data cache consists of: 64 units/2 banks on the MB86831/835, 64 units/1 bank on a 16-byte line on the MB86833, 128 units/2 banks on the MB86832/836, and 256 units/2 banks on a 32-byte line on the MB86834. (See “The composition of the data cache” and “The composition of the instruction cash.”) Each line is divided into 4-byte sub-blocks. When a cache miss occurs, the cache is updated in one word (4 bytes) or four words (16 bytes), selectively. Updating the cache in one word eliminates the wait time for an interrupt generated for replacing a long cache line; updating the cache in four words can result improvement in cache hit rate.
Updating the cache in four words uses the burst mode. The instruction prefetch buffer fetches the next instruction in advance, assuming that it corresponds to the next instruction cache miss.
The caches can be used in the normal mode or in either of two lock modes. In the normal mode, the cache in two-way set-associative configuration replaces one of two corresponding entries using the LRU (Least Recently Used) algorithm. As an alternate method, the entire cache or only the selected entry can be locked depending on the lock mode in use. The lock mode can lock a time-critical routine in the cache. The global cache lock mode locks the entries in the entire instruction or data cache.
The two control bits in the cache control register enable or disable the lock in the instruction and data caches. Once an entire cache is locked, any valid entry in the cache cannot be replaced. To ensure optimum performance, however, an invalid entry is updated when it is accessed. This update is performed automatically without generating time penalty.The instruction or data entry selected by local cache locking can be locked automatically in the corresponding cache. This mechanism can ensure the fastest response from a certain important interrupt routine by locking the code of the routine in the cache.
Also, of those routines which can be removed from the cache, frequently used ones should be given priority in performance in some cases. In such cases, the entries can be locked.
The local cache lock mode can lock individual entries or lock entries automatically by hardware. To lock each entry, the lock bit in the corresponding cache tag line is set by software. For automatic cache locking, the lock function is enabled or disabled depending on the bit in the corresponding cache control register. The enable/disable bit is set at the beginning of the routine for which the entry is to be locked. The location of cache access generated with the bit enabling the lock function is locked in the cache. Automatic cache locking does not involve overhead other than the initial setting cycle.
When a cache entry is unlocked, the data cache assign the cache entry only at load time based on the write-through update policy. The write operation is buffered and the processor can continue execution while data is being written back to memory. In contrast, the data written to the locked data cache location is not written to main memory.
The above method reduces external bus access and allows part of the data cache to be used as on-chip RAM which is not mapped into external memory.
The data and instruction caches are designed to be accessed through the independent data and instruction buses to load/write data from/to the cache at a maximum speed of 1 CPI (Clock/Instruction).

- The composition of the data cache (For MB86832).



- The composition of the instruction cash (For MB86832).



8. Bus Interface

The bus interface unit (BIU) is designed to simplify the interface between the MB86830 series and other parts of the system. The non-multiplexed address bus and data bus allow a high-speed system to be constructed easily. Also, the internal circuitry allows such a system to be constructed with a minimum of external hardware.
The bus interface supports programmable wait state generation, chip select output by address decoding, same-page detection for supporting page mode DRAM, booting from 8/16/32-bit memory, and a automatic reload timer for refreshing DRAM. In addition, the burst mode can be used to perform cache line fill operation at high speed.

9. DRAM Controller

With the DRAM controller controlling DRAM, the MB86830 series can write/read data to/from DRAM. The DRAM controller can control up to four banks on the MB86831/832/834 or only one bank on the MB86833/835. The fast page mode, DRAM mode, or EDO DRAM mode can be selected depending on the register setting. The DRAM

controller also controls the RAS and CAS to place DRAM in the self-refresh mode when the processor enters the sleep mode (low power consumption mode).
The MB86836 has no DRAM controller.

10. Interrupt Controller (IRC)

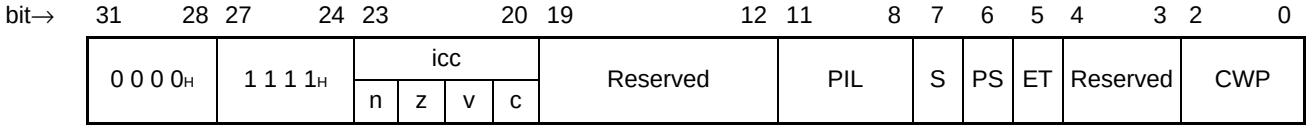
The interrupt controller (IRC) accepts interrupts inputs through eight channels, depending on the trigger mode and mask bit set for each of the channels. When accepting an interrupt, the interrupt controller encodes it according to the interrupt priority level and outputs the interrupt level to the processor. The interrupt level remains held unless it is cleared by the processor. The processor is not therefore informed of the next interrupt.

11. Multiplier Circuit

The CLKSEL0, CLKSEL1, and CLKSEL2 pins can be used to select the multiplier circuit to be used. The ×1, ×2, ×3, ×4, or ×5 multiplier circuits are supported, which allow the processor to run faster.

12. IU (Integer Unit) Dedicated Registers (Not Memory Mapped)

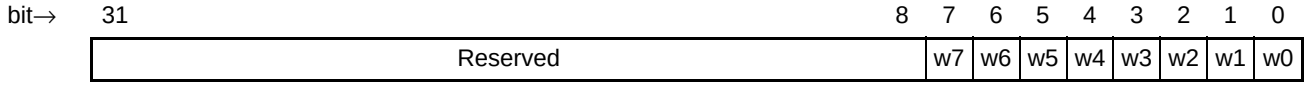
(1)Processor Status Register (PSR)



bit 23 to bit 20 :Integer condition code [icc] (n:Negative = 1, z:Zero = 1, v:Overflow = 1, c:Carry = 1)
bit 19 to bit 12 :Reserved[“0”Write, Don’t care for read]
bit 11 to bit 8 :Processor Interrupt Level [PIL] (Value = 1 to 15, RST = X)
bit 7 :Supervisor Mode [S] (Supervisor = 1, User = 0, RST = 1)
bit 6 :Prior S Mode [PS]
bit 5 :Enable Trap [ET] (Enable = 1, Disable = 0, RST = 0)
bit 4 to bit 3 :Reserved [“0”Write, Don’t care for read]
bit 2 to bit 0 :Current Window Point [CWP] (Value = 0 to 7, RST = X)

X:Don’t care

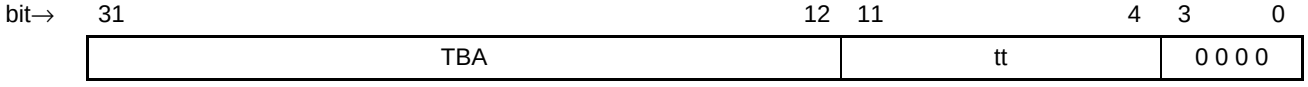
(2)Window Invalid Mask Register (WIM)



bit 31 to bit 8 :Reserved [“0”Write, Don’t care for read]
bit 7 to bit 0 :Window mask [w7 to w0] (Invalid = 1, Valid = 0, RST = X)

X:Don’t care

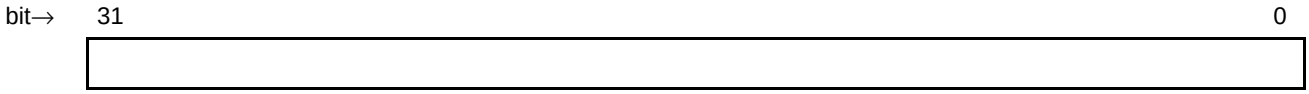
(3)Trap Base Register (TBR)



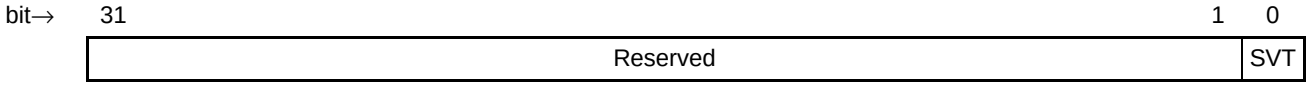
bit 31 to bit 12 :Trap base address [TBA] (RST = X)
bit 11 to bit 4 :Trap type [tt] (RST = X)

X:Don’t care

(4)Y Register (Y)



(5)Ancillary State Register 17 (ASR17)

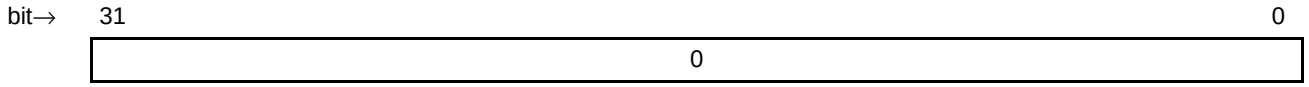


bit 31 to bit 1 :Reserved [“0”Write, Don’t care for read]
bit 0 :Single Vector Trapping [SVT] (Enable = 1, Disable = 0, RST = 0)

13. IU (Integer Unit) General-Purpose Registers (Not Memory Mapped)

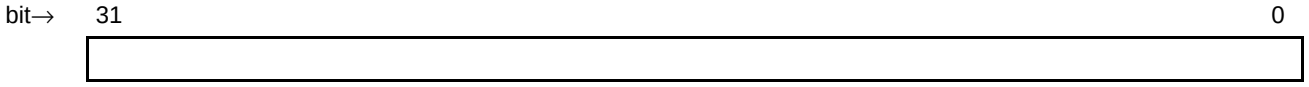
The IU (integer unit) contains 136 32-bit general-purpose registers for holding arguments for operations and their results. Of these registers, only 32 registers can be accessed through blocks called register windows.
The integer unit has eight register windows. The register window to be used is determined by the CWP bits (bits 2 to 0) in the Processor Status Register (PSR). Each register window consists of eight global registers available commonly to all register windows and 24 registers (in-register × 8, local register × 8, out-register × 8). The in-registers and out-registers are used commonly between adjacent register windows.

(1)Zero Register (r0)



bit 31 to bit 0 :0

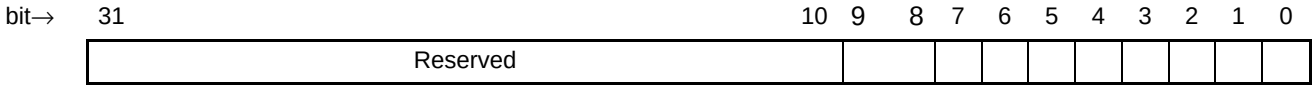
(2)General register (r1 to r31)



Don’t care at reset.

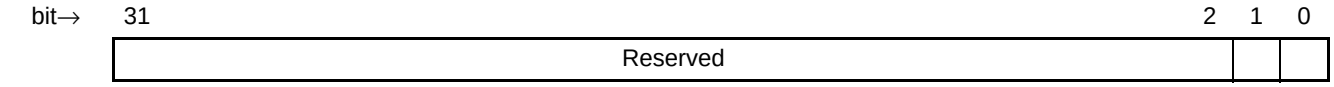
14. Bit map of register with built-in CPU core

(1)Cache/BIU Control Register (CBIR) **ASI= 0x01, Address= 0x00000000H**



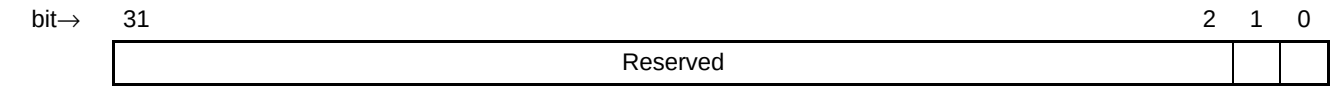
bit 31 to bit 10 :Reserved [“0”Write, Don’t care for read]
bit 9 to bit 8 :Non-cacheable Wait-state [Don’t care for read]
bit 7 :Cacheability Enable [Don’t care for read] (Enable = 1, Disable = 0, RST = 0)
bit 6 :Reserved [“0”Write, Don’t care for read]
bit 5 :Write Buffer Enable (Enable = 1, Disable = 0, RST = 0)
bit 4 :Prefetch Buffer Enable (Enable = 1, Disable = 0, RST = 0)
bit 3 :Data Cache Lock (Lock = 1, Unlock = 0, RST = 0)
bit 2 :Data Cache Enable (Enable = 1, Disable = 0, RST = 0)
bit 1 :Instruction Cache Lock (Lock = 1, Unlock = 0, RST = 0)
bit 0 :Instruction Cache Enable (Enable = 1, Disable = 0, RST = 0)

(2)Lock Control Register (LCR) **ASI= 0x01, Address= 0x00000004H**



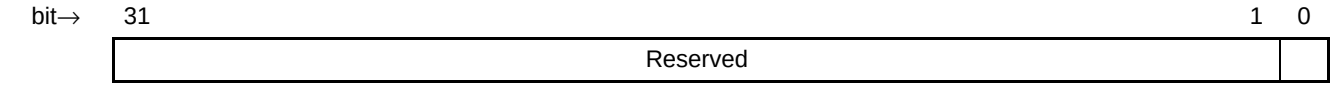
bit 31 to bit 2 :Reserved [“0”Write, Don’t care for read]
bit 1 :Data Cache Entry Auto Lock (Enable = 1, Disable = 0, RST = 0)
bit 0 :Instruction Cache Entry Auto Lock (Enable = 1, Disable = 0, RST = 0)

(3)Lock Control Save Register (LCSR) **ASI = 0x01, Address = 0x00000008H**



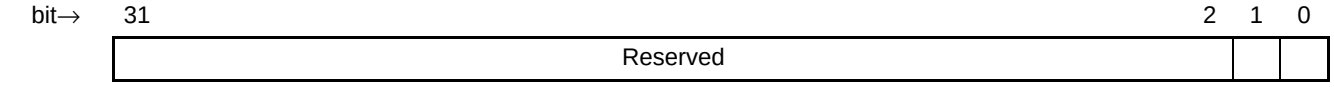
bit 31 to bit 2 :Reserved [“0”Write, Don’t care for read]
bit 1 :Previous Data Cache Auto Lock (Off = 0, On = 1, RST = 0)
bit 0 :Previous Instruction Cache Auto Lock (Off = 0, On = 1, RST = 0)

(4)Restore Lock Control Register (RLCR) **ASI = 0x01, Address = 0x00000010H**



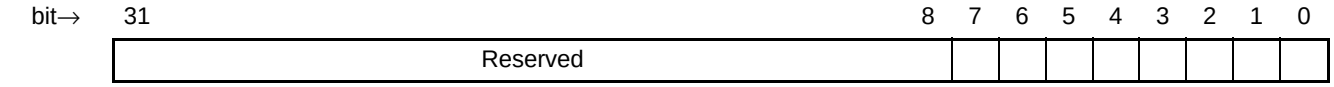
bit 31 to bit 1 :Reserved [“0”Write, Don’t care for read]
bit 0 :Restore Lock Control Register (Restore = 1, Ignore = 0, RST = 0)

(5)Bus Control Register (BCR) **ASI = 0x01, Address = 0x00000020H**



bit 31 to bit 2 :Reserved [“0”Write, Don’t care for read]
bit 1 :Data Burst Enable (Enable = 1, Disable = 0, RST = 0)
bit 0 :Instruction Burst Enable (Enable = 1, Disable = 0, RST = 0)

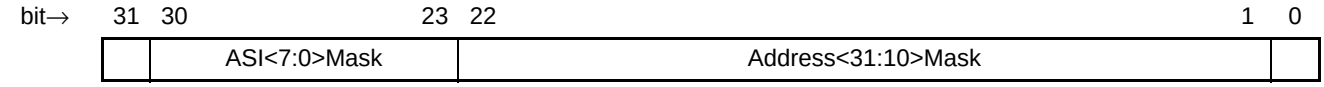
(6)System Support Control Register (SSCR) **ASI = 0x01, Address = 0x00000080H**



bit 31 to bit 8 :Reserved [“0”Write, Don’t care for read]
bit 7 :DRAM Burst Enable (Enable = 1, Disable = 0, RST = 0)
bit 6 :DRAM Controller Enable (Enable = 1, Disable = 0, RST = 0)
bit 5 :Same Page Enable (Enable = 1, Disable = 0, RST = 0)
bit 4 :CS Enable (Enable = 1, Disable = 0, RST = 0) *
bit 3 :Programmable Wait-state (Enable = 1, Disable = 0, RST = 1)
bit 2 :Timer On/Off (Enable = 1, Disable = 0, RST = 0)
bit 1 to bit 0 :Reserved “0”Write, Don’t care for read]

*:CS0 is always enable.

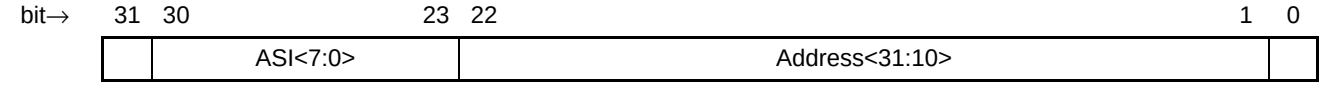
(7)Same Page Mask Register (SPGMR) **ASI = 0x01, Address = 0x00000120H**



bit 31 :Reserved [“0”Write, Don’t care for read]
bit 30 to bit 23 :ASI<7:0>Mask (Care = 0, Don’t Care = 1, RST = X)
bit 22 to bit 1 :Address<31:10>Mask (Care = 0, Don’t Care = 1, RST = X)
bit 0 :Reserved [“0”Write,Don’t care for read]

X:Don’t care

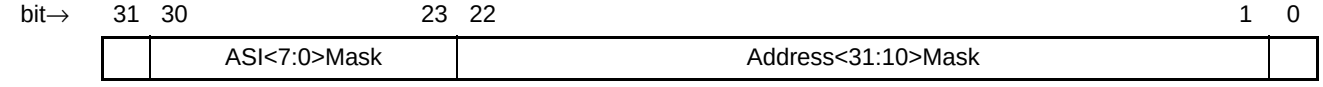
(8)Address Range Specifier Register (ARSR) **ASI = 0x01, Address = 0x00000124H to 0x00000134H**



bit 31 :Reserved [“0”Write, Don’t care for read]
bit 30 to bit 23 :ASI<7:0>(RST = X) *
bit 22 to bit 1 :Address<31:10>(RST = X) *
bit 0 :Reserved [“0”Write, Don’t care for read]

*CS0 is fixed to Address<31: 15>=0,Address<14: 10>=0,ASI<7:0>=0x09.
X:Don’t care

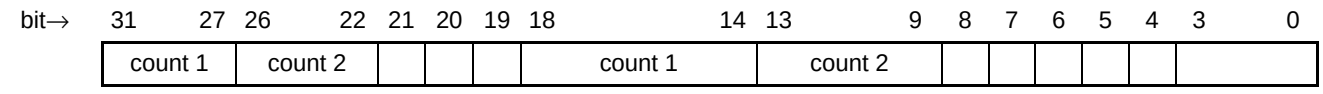
(9)Address Mask Register (AMR) **ASI = 0x01, Address = 0x00000140H to 0x00000154H**



bit 31 :Reserved [“0”Write, Don’t care for read]
bit 30 to bit 23 :ASI<7:0>Mask (CS0:RST = 0, CS1 to CS5:RST = X)
bit 22 to bit 1 :Address<31:10>Mask (CS0:RST = <31:15> = 0, <14:10> = 0x1f, CS1 to CS5:RST = X)
bit 0 :Reserved [“0”Write, Don’t care for read]

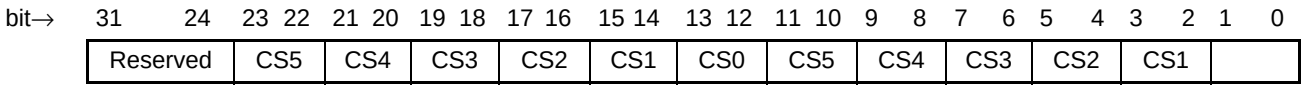
X:Don’t care

(10)Wait State Specifier Register (WSSR) **ASI = 0x01, Address = 0x00000160H to 0x00000168H**



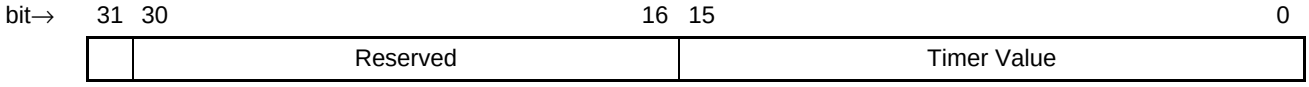
bit 31 to bit 27,bit 18 to bit 14 :count 1 (CS0:RST = 0x1f, CS1 to CS5:RST = 0)
bit 26 to bit 22,bit 13 to bit 9 :count 2 (CS0:RST = 0x1f, CS1 to CS5:RST = 0)
bit 21,bit 8 :Wait Enable (On = 1, Off = 0,CS0:RST = 1, CS1 to CS5:RST = 0)
bit 20,bit 7 :Single Cycle Non Burst Mode (On = 1, Off = 0,RST = 0)
bit 19,bit 6 :Override (On = 1, Off = 0, CS0 = 1, CS1 to CS5 = 0)
bit 5,bit 4 :Single Cycle Burst Mode (On = 1, Off = 0, RST = 0)
bit 3 to bit 0 :Reserved [“0”Write, Don’t care for read]

(11)Bus Width/Cacheable Register (BWCR) **ASI = 0x01, Address = 0x0000016CH**



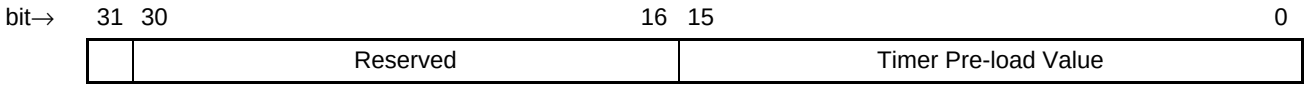
bit 31 to bit 24 :Reserved [“0”Write, Don’t care for read]
bit 23,bit 21,bit 19,bit 17,bit 15,bit 13 :Internal/External Cacheable (0 = External, 1 = Internal)
bit 22,bit 20,bit 18,bit 16,bit 14,bit 12 :Cacheable (0 = cacheable, 1 = noncacheable)
bit 11 to bit 10,bit 9 to bit 8,bit 7 to bit 6,bit 5 to bit 4,
bit 3 to bit 2 :Bus Width Control bit
bit 1 to bit 0 :Reserved [“0”Write, Don’t care for read]

(12)DRAM Refresh Timer Register (REFTMR) **ASI = 0x01, Address = 0x00000174H**



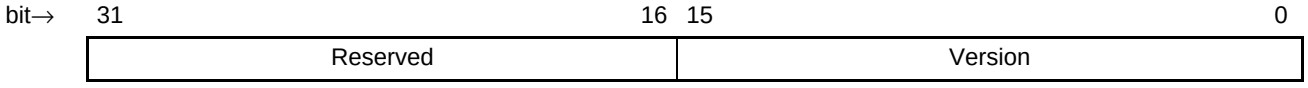
bit 31 :Test Mode [“0“Write, Don’t care for read]
bit 30 to bit 16 :Reserved [“0”Write, Don’t care for read]
bit 15 to bit 0 :Timer Value (RST = 0xffff)

(13)DRAM Refresh Timer Pre-load (DRLD) **ASI = 0x01, Address = 0x00000178H**



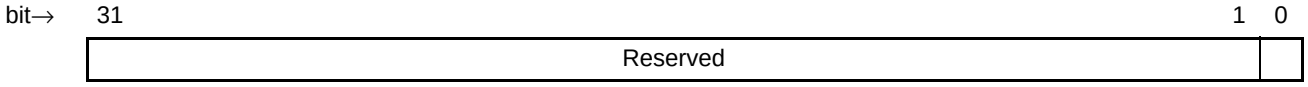
bit 31 :3 Cycle Mode (On = 1, Off = 0, RST = 0)
bit 30 to bit 16 :Reserved [“0”Write, Don’t care for read]
bit 15 to bit 0 :Timer Pre-load Value (RST = 0xffff)

(14)Ancillary Version Register (VER2)[Read only] **ASI = 0x01, Address = 0x00020000H**



bit 31 to bit 16 :Reserved [Don’t care for read]
bit 15 to bit 0 :Version
(MB86831:Value = 0, MB86832:Value = 1, MB86833:Value = 2, MB86834:Value = 3,
MB86835:Value = 4, MB86836:Value = 1)

(15)Sleep Mode Register (SLPMD)[Write only] **ASI = 0x01, Address = 0x00020004H**



bit 31 to bit 1 :Reserved
bit 0 :Sleep Mode (On = 1, Off = 0, RST = 0)

15. Bit map of register for cash access

(1)Instruction Tag Lock Bit (ICLOCK) [Wite only] **ASI = 0x02**

Capacity 16 KB
- Bank 1:Address = $0x00000000_H$ to $0x00001fe0_H$ (+32)
- Bank 2:Address = $0x80000000_H$ to $0x80001fe0_H$ (+32)

Capacity 8 KB
- Bank 1:Address = $0x00000000_H$ to $0x00000fe0_H$ (+32)
- Bank 2:Address = $0x80000000_H$ to $0x80000fe0_H$ (+32)

Capacity 4 KB
- Bank 1:Address = $0x00000000_H$ to $0x000007e0_H$ (+32)
- Bank 2:Address = $0x80000000_H$ to $0x800007e0_H$ (+32)

Capacity 2 KB
- Bank 1:Address = $0x00000000_H$ to $0x000003f0_H$ (+16)
- Bank 2:Address = $0x80000000_H$ to $0x800003f0_H$ (+16)

Capacity 1 KB
- Bank 2:Address = $0x80000000_H$ to $0x800003f0_H$ (+16)

bit→	31	1	0
	Reserved		

bit 31 to bit 1 :Reserved [“0”Write, Don’t care for read]
bit 0 :Entry Lock (Lock = 1, Unlock = 0, RST = 0)

(2)Data Tag Lock Bit (DCLOCK)[Wite only] **ASI = 0x03**

Capacity 16 KB
- Bank 1:Address = $0x00000000_H$ to $0x00001fe0_H$ (+32)
- Bank 2:Address = $0x80000000_H$ to $0x80001fe0_H$ (+32)

Capacity 8 KB
- Bank 1:Address = $0x00000000_H$ to $0x00000fe0_H$ (+32)
- Bank 2:Address = $0x80000000_H$ to $0x80000fe0_H$ (+32)

Capacity 4 KB
- Bank 1:Address = $0x00000000_H$ to $0x000007e0_H$ (+32)
- Bank 2:Address = $0x80000000_H$ to $0x800007e0_H$ (+32)

Capacity 2 KB
- Bank 1:Address = $0x00000000_H$ to $0x000003f0_H$ (+16)
- Bank 2:Address = $0x80000000_H$ to $0x800003f0_H$ (+16)

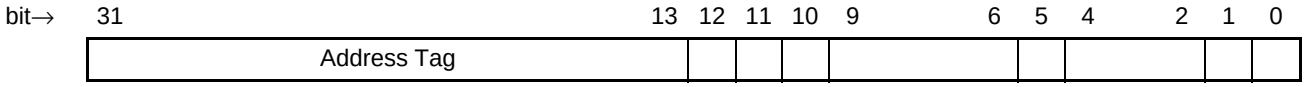
Capacity 1 KB
- Bank 2:Address = $0x80000000_H$ to $0x800003f0_H$ (+16)

bit→	31	1	0
	Reserved		

bit 31 to bit 1 :Reserved [“0”Write, Don’t care for read]
bit 0 :Entry Lock (Lock = 1, Unlock = 0, RST = 0)

(3)Instruction Cache Tag (ICTAG)

ASI = **0x0c**
Capacity 16 KB
Bank 1:Address = 0x00000000H to 0x00001fe0H (+32)
Bank 2:Address = 0x80000000H to 0x80001fe0H (+32)
Capacity 8 KB
Bank 1:Address = 0x00000000H to 0x00000fe0H (+32)
Bank 2:Address = 0x80000000H to 0x80000fe0H (+32)
Capacity 4 KB
Bank 1:Address = 0x00000000H to 0x000007e0H (+32)
Bank 2:Address = 0x80000000H to 0x800007e0H (+32)
Capacity 2 KB
Bank 1:Address = 0x00000000H to 0x000003f0H (+16)
Bank 2:Address = 0x80000000H to 0x800003f0H (+16)
Capacity 1 KB
Bank 2:Address = 0x80000000H to 0x800003f0H (+16)

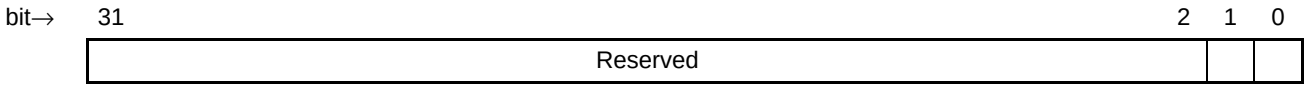


bit 31 to bit 13 :Address Tag (RST = X)
bit 12 :Capacity 16 KB = <Reserved>, Other = <Address Tag>
bit 11 :Capacity 16 KB, 8 KB = <Reserved>, Other = <Address Tag>
bit 10 :Capacity 16 KB, 8 KB, 4 KB = <Sub Block Valid>(Valid = 1, Invalid = 0, RST = 0)
Capacity 2 KB, 1 KB = <Address Tag>
bit 9 to bit 6 :Sub Block Valid (Valid = 1, Invalid = 0,RST = 0)
bit 4 to bit 2 :Capacity 16 KB, 8 KB, 4 KB = <Sub Block Valid>(Valid = 1, Invalid = 0, RST = 0)
Capacity2 KB, 1 KB = <Reserved> [Don't care for read]
bit 5 :User/Supervisor (User = 0, Supervisor = 1, RST = X)
bit 1 :Capacity1 KB = <Reserved>, Other= LRU (RST = 0) *
bit 0 :Entry Lock (Lock = 1, Unlock = 0, RST = 0)

*:BANK only, BANK 2 is Reserved
X:Don't care

(4)Instruction Cache Invalidate Register (ICINVLD)[Wite only]

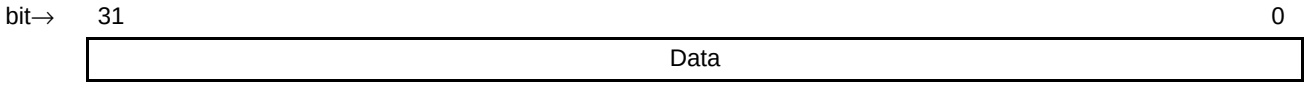
ASI = **0x0c**
Capacity 16 KB
Bank 1:Address = 0x00008000H
Bank 2:Address = 0x80008000H
Other
Bank 1:Address = 0x00001000H
Bank 2:Address = 0x80001000H



bit 31 to bit 2 :Reserved ["0"Write]
bit 1 :Cache LRU, Lock Bit Clear (Clear = 1, Not Clear = 0)
bit 0 :Valid Bit Clear (Clear = 1, Not Clear = 0)

(5)Instruction Cache Data RAM (ICDATA)

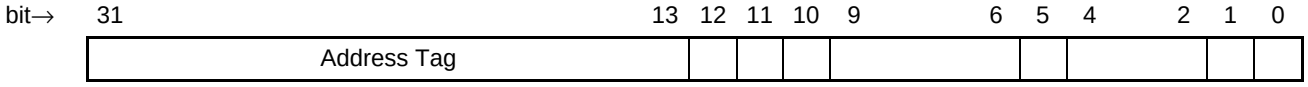
ASI = **0x0d**
Capacity 16 KB
Bank 1:Address = 0x00000000H to 0x00001ffcH (+4)
Bank 2:Address = 0x80000000H to 0x80001ffcH (+4)
Capacity 8 KB
Bank 1:Address = 0x00000000H to 0x00000ffcH (+4)
Bank 2:Address = 0x80000000H to 0x80000ffcH (+4)
Capacity 4 KB
Bank 1:Address = 0x00000000H to 0x000007fcH (+4)
Bank 2:Address = 0x80000000H to 0x800007fcH (+4)
Capacity 2 KB
Bank 1:Address = 0x00000000H to 0x000003fcH (+4)
Bank 2:Address = 0x80000000H to 0x800003fcH (+4)
Capacity 1 KB
Bank 2:Address = 0x80000000H to 0x800003fcH



bit 31 to bit 0:Data (RST = X)
X:Don't care

(6)Data Cache Tag (DCTAG)

ASI = **0x0e**
Capacity 16 KB
Bank 1:Address = 0x00000000H to 0x00001fe0H (+32)
Bank 2:Address = 0x80000000H to 0x80001fe0H (+32)
Capacity 8 KB
Bank 1:Address = 0x00000000H to 0x00000fe0H (+32)
Bank 2:Address = 0x80000000H to 0x80000fe0H (+32)
Capacity 4 KB
Bank 1:Address = 0x00000000H to 0x000007e0H (+32)
Bank 2:Address = 0x80000000H to 0x800007e0H (+32)
Capacity 2 KB
Bank 1:Address = 0x00000000H to 0x000003f0H(+16)
Bank 2:Address = 0x80000000H to 0x800003f0H (+16)
Capacity 1 KB
Bank 2:Address = 0x80000000H to 0x800003f0H (+16)

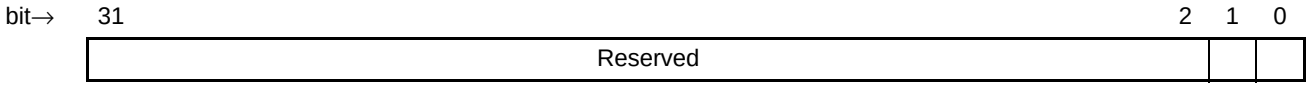


bit 31 to bit 13 :Address Tag (RST = X)
bit 12 :Capacity 16 KB = <Reserved>, Other = <Address Tag>
bit 11 :Capacity 16 KB, 8 KB = <Reserved>, Other = <Address Tag>
bit 10 :Capacity 16 KB, 8 KB, 4 KB = <Sub Block Valid>(Valid = 1, Invalid = 0, RST = 0)
Capacity 2 KB, 1 KB = <Address Tag>
bit 9 to bit 6 :Sub Block Valid (Valid = 1, Invalid = 0,RST = 0)
bit 4 to bit 2 :Capacity 16 KB, 8 KB, 4 KB = <Sub Block Valid>(Valid = 1, Invalid = 0, RST = 0)
Capacity 2 KB, 1 KB = <Reserved>[Don't care for read]
bit 5 :User/Supervisor (User = 1, Supervisor = 0, RST = X)
bit 1 :Capacity 1 KB = <Reserved>, Other = LRU (RST = 0) *
bit 0 :Entry Lock (Lock = 1, Unlock = 0, RST = 0)

*:BANK 1 only, BANK 2 is Reserved
X:Don't care

(7)Data Cache Invalidate Register (DCINVLD)[Wite only]

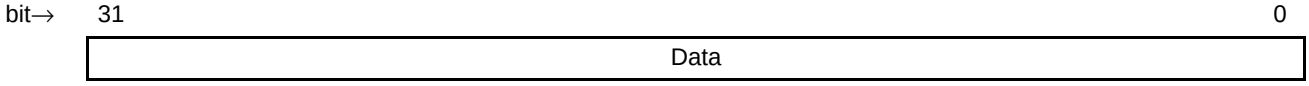
ASI = **0x0e**
Capacity 16 KB
Bank 1:Address = 0x00008000H
Bank 2:Address = 0x80008000H
Other
Bank 1:Address = 0x00001000H
Bank 2:Address = 0x80001000H



bit 31 to bit 2 :Reserved [“0”Write]
bit 1 :Cache LRU, Lock Bit Clear (Clear = 1, Not Clear = 0)
bit 0 :Valid Bit Clear (Clear = 1, Not Clear = 0)

(8)Data Cache Data RAM(DCDATA)

ASI = **0x0f**
Capacity 16 KB
Bank 1:Address = 0x00000000H to 0x00001ffcH (+4)
Bank 2:Address = 0x80000000H to 0x80001ffcH (+4)
Capacity 8 KB
Bank 1:Address = 0x00000000H to 0x00000ffcH (+4)
Bank 2:Address = 0x80000000H to 0x80000ffcH (+4)
Capacity 4 KB
Bank 1:Address = 0x00000000H to 0x000007fcH (+4)
Bank 2:Address = 0x80000000H to 0x800007fcH (+4)
Capacity 2 KB
Bank 1:Address = 0x00000000H to 0x000003fcH (+4)
Bank 2:Address = 0x80000000H to 0x800003fcH (+4)
Capacity 1 KB
Bank 2:Address = 0x80000000H to 0x800003fcH (+4)



bit 31 to bit 0 :Data (RST = X)

X:Don’t care

16. Interrupt controller (IRC)

(1)Trigger Mode 0 Register (TRGM0)

CS3# = L, Address<9:2> = 0x00

bit→	31 … 16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved	ch 15		ch 14		ch 13		ch 12		ch 11		ch 10		ch 9		ch 8	

bit 31 to bit 16 :Reserved [“0”Write, Don’t care for read]
bit 15 to bit 0 :Trigger Mode (High Level = 00, Low Level = 01, High Edge = 10, Low Edge = 11, RST = 00)

(2)Trigger Mode 1 Register (TRGM1)

CS3# = L, Address<9:2> = 0x01

bit→	31 … 16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved	ch 7		ch 6		ch 5		ch 4		ch 3		ch 2		ch 1		0	0

bit 31 to bit 16 :Reserved [“0”Write, Don’t care for read]
bit 15 to bit 2 :Trigger Mode (High Level = 00, Low Level = 01, High Edge = 10, Low Edge = 11, RST = 00)
bit 1 to bit 0 :Reserved [“0”Write, Read“0”]

(3)Request Sense Register (REQSNS)[Read only]

CS3# = L, Address<9:2> = 0x02

bit→	31 … 16	15 … 1	0
	Reserved	Request Sense 15 to Request Sense 1	0

bit 31 to bit 16 :Reserved [Don’t care for read]
bit 15 to bit 1 :Request Sense 15 to Request Sense 1 (RST = 0)
bit 0 :Reserved [Read“0”]

(4)Request Clear Register (REQCLR)[Wite only]

CS3# = L, Address<9:2> = 0x03

bit→	31 … 16	15 … 1	0
	Reserved	Request Clear 15 to Request Clear 1	0

bit 31 to bit 16 :Reserved [“0”Write]
bit 15 to bit 1 :Request Clear 15 to Request Clear 1 (Clear = 1, Not Clear = 0)
bit 0 :Reserved [“0”Write]

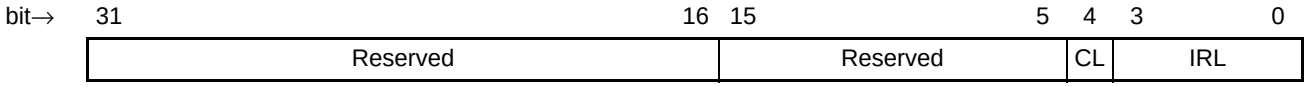
(5)Interrupt Mask Register (IMASK)

CS3# = L, Address<9:2> = 0x04

bit→	31 … 16	15 … 1	0
	Reserved	Mask 15 to Mask 1	IM

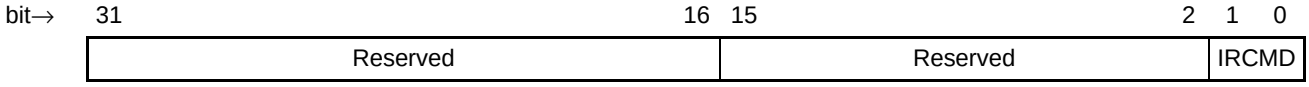
bit 31 to bit 16 :Reserved [“0”Write, Don’t care for read]
bit 15 to bit 1 :Mask 15 to Mask 1 (Mask = 1, Not Mask = 0, RST = 1)
bit 0 :IRL Mask (Mask = 1, Not Mask = 0, RST = 0)

(6)IRL Latch/Clear Register (IRLAT) **CS3# = L, Address<9:2> = 0x05**



bit 31 to bit 16 :Reserved [“0”Write, Don’t care for read]
bit 15 to bit 5 :Reserved [“0”Write, Read"0"]
bit 4 :IRL Clear [Wite only] (Clear = 1, Not Clear = 0)
bit 3 to bit 0 :IRL Latch [Read only] (RST = 0000)

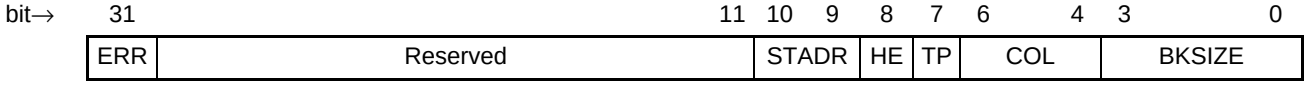
(7)IRC Mode Register (IMODE) **CS3# = L, Address<9:2> = 0x06**



bit 31 to bit 16 :Reserved [“0”Write, Don’t care for read]
bit 15 to bit 2 :Reserved [“0”Write, Read“0”]
bit 1 to bit 0 :IRC Mode [IRCMD] (Disable = 00, Enable = 01, RST = 00)

17. DRAM controller

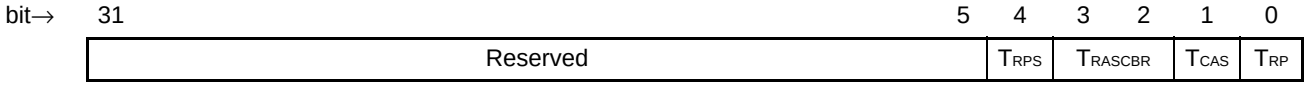
(1)DRAM Bank Configuration Register (DBANKR) **CS3# = L, Address<9:2> = 0x08**



bit 31 :Access Error [ERR] (Error = 1, No Error = 0, RST = X, “0”Write Clear)
bit 30 to bit 11 :Reserved [“0”Write, Don’t care for read]
bit 10 to bit 9 :DRAM Start Address [STADR] (RST = 01)
bit 8 :Hyper Page Enable [HE] (Page Mode DRAM = 0, EDO DRAM = 1, RST = 0)
bit 7 :DRAM Type[TP] (4CAS-1WE= 0, 4WE -1CAS = 1, RST = 0)
bit 6 to bit 4 :Column Address [COL] (RST = 011)
bit 3 to bit 0 :Bank Size [BKSIZE] (RST = 0011)

X:Don’t care

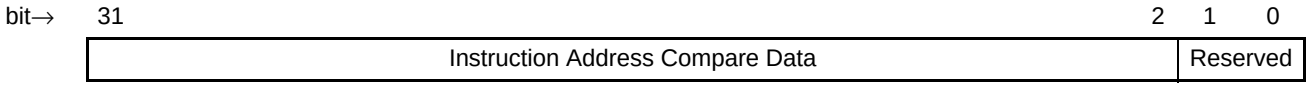
(2)DRAM Timing Register (DTIMR) **CS3# = L, Address<9:2> = 0x09**



bit 31 to bit 5 :Reserved [“0”Write, Don’t care for read]
bit 4 :RAS#Precharge time specification bits [T_{RPS}] at Self-Refresh (2 Cycle = 0, 4 Cycle = 1, RST = 1)
bit 3 to bit 2 :RAS#Pulse width specification bit [T_{RASCBR}] at CBR Refresh
(1 Cycle = 00, 2 Cycle = 01, 3 Cycle = 10, RST = 01)
bit 1 :CAS#Pulse width specification bit [T_{CAS}] (1 Cycle = 0, 2 Cycle = 1, RST = 1)
bit 0 :RAS#Precharge width specification bit [T_{RP}] (1 Cycle = 0, 2 Cycle = 1, RST = 0)

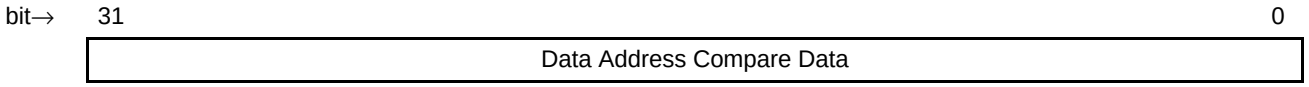
18. DSU (Debugging support unit)(MB86832/834)

(1)Instruction Address Descriptor Register (INSTADR) ASI = 0x01, Address = 0x0000ff00H to 0x0000ff04H



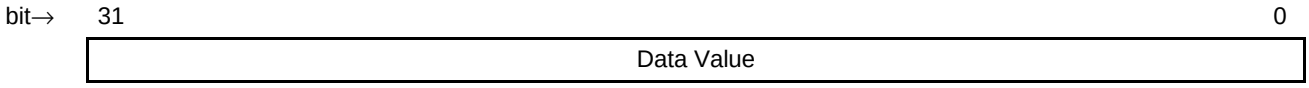
bit 31 to bit 2 :Instruction Address Compare Data (RST = 0x00000000H)
bit 1 to bit 0 :Reserved [“0”Write, Don’t care for read]

(2)Data Address Descriptor Register (DATAADR) ASI = 0x01, Address = 0x0000ff08H to 0x0000ff0cH



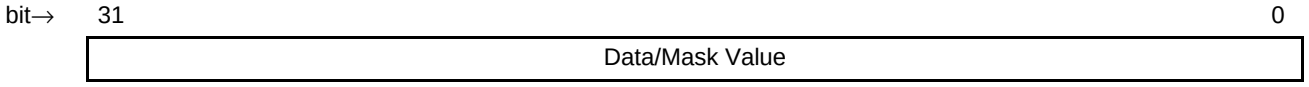
bit 31 to bit 0 :Data Address Compare Data (RST = 0x00000000H)

(3)Data Value Descriptor Register (DVDR) ASI = 0x01, Address = 0x0000ff10H



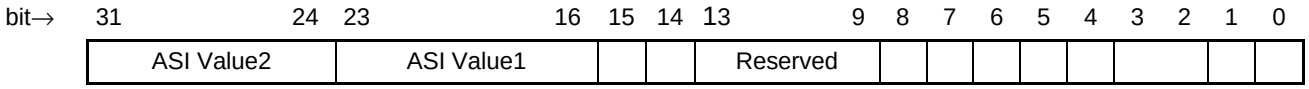
bit 31 to bit 0 :Data Value (RST = 0x00000000H)

(4)Data Value Descriptor Register/Mask Register (DVDMSK) ASI = 0x01, Address = 0x0000ff14H



bit 31 to bit 0 :Data/Mask Value (RST = 0x00000000H)

(5)Debug Control Register (DSUCR) ASI = 0x01, Address = 0x0000ff18H

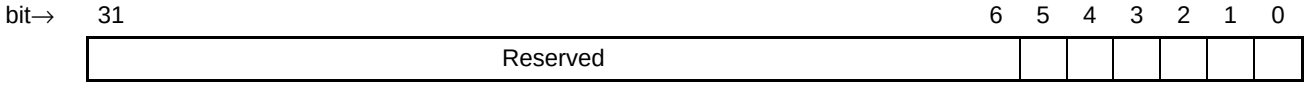


bit 31 to bit 24 :ASI Value2 (RST = 0x00)
bit 23 to bit 16 :ASI Value1 (RST = 0x00)
bit 15 :Instruction User/Supervrisor2 (Supervrisor = 1, User = 0, RST = 0)
bit 14 :Instruction User/Supervrisor1 (Supervrisor = 1, User = 0, RST = 0)
bit 13 to bit 9 :Reserved
bit 8 :Enable Data Address2 Break (Enable = 1, Disable = 0, RST = 0)
bit 7 :Enable Data Address1 Break (Enable = 1, Disable = 0, RST = 0)
bit 6 :Enable Instruction Address2 Break (Enable = 1, Disable = 0, RST = 0)
bit 5 :Enable Instruction Address1 Break (Enable = 1, Disable = 0, RST = 0)
bit 4 :Single Step (On = 1, Off = 0, RST = 0)
bit 3 to bit 2 :Data Value Transaction Type (RST = 0x0)

bit 3	bit 2	Type
0	0	Break only on Loads
0	1	Break only on Stores
1	0	Break on Load or Store
1	1	Break Always

bit 1 :Data Value Condition (Outside = 1, Inside = 0, RST = 0)
bit 0 :Data Value Mask (Mask = 1, Range = 0, RST = 0)

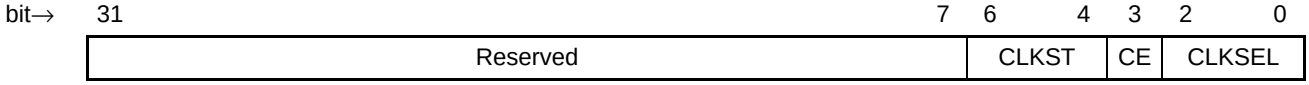
(6)Debug Status Register (DSR) **ASI = 0x01, Address = 0x0000ff1C$_H$**



bit 31 to bit 6 :Reserved [“0”Write, Don’t care for read]
bit 5 :Data Address 2 Match (Match = 1, Not Match = 0, RST = 0)
bit 4 :Data Address 1 Match (Match = 1, Not Match = 0, RST = 0)
bit 3 :Instruction Address 2 Match (Match = 1, Not Match = 0, RST = 0)
bit 2 :Instruction Address 1 Match (Match = 1, Not Match = 0, RST = 0)
bit 1 :EMUENBL [Read only]
bit 0 :EMUBRK [Read only]

19. Clock gear (Not supported in MB86831-66,80)

Internal Clock Control/Status Register (ICCS) **CS3# = L, Address<9:2> = 0x0b**



bit 31 to bit 7 :Reserved [“0”Write, Don’t care for read]
bit 6 to bit 4 :Internal Clock Status [CLKST]
bit 3 :Internal Clock Change Enable [CE] (Enable = 1, Disable = 0, RST = 0)
bit 2 to bit 0 :Internal Clock Select [CLKSEL]

CLKST	Internal Clock
100	× 1
101	× 2
110	× 3
111	× 4
011	× 5
010	Reserved
001	
000	

- **Register explanation**

Internal Clock Control/Status Register (ICCS)

bit→	31 … 7	6 … 4	3	2 … 0
	Reserved	CLKST	CE	CLKSEL

bit 31 to bit 7 :Reserved [“0”Write, Don’t care for read]
bit 6 to bit 4 :CLKST (Internal Clock Status)(An initial value is a set point of external terminal CLKSEL2, CLKSEL1, and CLKSEL0.)
Can know the multiplication rate that CPU works by the bit which shows Internal Clock.

CLKST	Internal Clock
100	× 1
101	× 2
110	× 3
111	× 4
011	× 5
010	Reserved
001	
000	

bit 3 :CE (Internal Clock Change Enable)(Initial value “0”)
Internal Clock change inable bit.Internal Clock is changed according to the CLKSEL bit according to this value at sleep mode (low power consumption mode).
1: Internal Clock is changed by the CLKSEL bit.
0: No change Internal Clock.
It is necessary to set “1” in this bit to change Internal Clock before sleep mode (low power consumption mode) is set.
bit 2 to bit 0 :CLKSEL (Internal Clock Select)
Internal Clock specification bit.

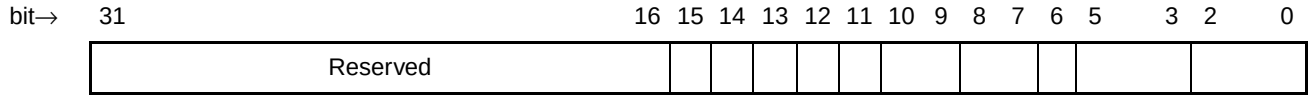
20. General-purpose 16-bit Timer (MB86836)

(1) Prescaler0 (PRS0) **CS3# = L, Address<9:2> = 0x0c**

bit→	31 … 16	15	14	13 … 11	10 … 8	7 … 0
	Reserved	EX	Test	Reserved	Select	Prescale Value

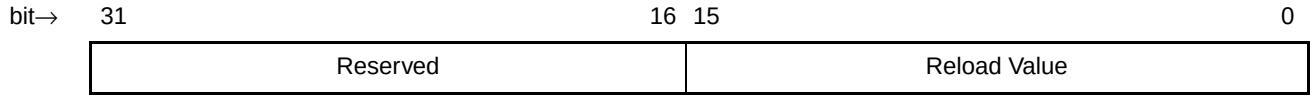
bit 31 to bit 16 :Reserved [“0”Write, Don’t care for read]
bit 15 :External Clock [“0”Write]
Support to only internal clock mode
bit 14 :Test [“0”Write]
bit 13 to bit 11 :Reserved [“0”Write, Don’t care for read]
bit 10 to bit 8 :Select (RST = 000)
bit 7 to bit 0 :Prescale Value (RST = 01)

(2) Timer Control Register (TCR) **CS3# = L, Address<9:2> = 0x0d**



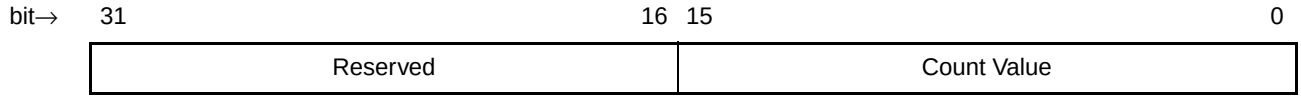
bit 31 to bit 16 :Reserved [“0”Write, Don’t care for read]
bit 15 :Value Of OUT Signal
bit 14 :Value Of IN Signal
bit 13 :Reserved [“0”Write, Don’t care for read]
bit 12 :Test [“0”Write]
bit 11 :Count Enable (Enable = 1, Disable = 0, RST = 0)
bit 10 to bit 9 :Clock Select (Internal Clock = 0, Prescaler Clock = 2, Don’t Use = 1 or 3, RST = 0)
bit 8 to bit 7 :OUT Signal Control (Keep = 0, Set = 1, Reset = 2, Don’t Use = 3)
bit 6 :Invert (true = 0, Invert = 1, RST = 0)
bit 5 to bit 3 :Mode Select
bit 2 to bit 0 :Event Select

(3) Reload Value Register (RVR) **CS3# = L, Address<9:2> = 0x0e**



bit 31 to bit 16 :Reserved [“0”Write, Don’t care for read]
bit 15 to bit 0 :Reload Value

(4) Count Value Register (CVR) [Read Only] **CS3# = L, Address<9:2> = 0x0f**



bit 31 to bit 16 :Reserved [“0”Write, Don’t care for read]
bit 15 to bit 0 :Count Value

For details on each register, refer to the manual for the MB86942.

21. Notes on Register Setting

(1)Cache/BIU Control Register

- To set Cache Enable or Cache Disable, be sure to insert at least three NOP instructions after the Enable or Disable instruction.
- The Non-Cacheable bit (bit 9, bit 8) and Cacheability Enable bit (bit 7) cannot be read.

(2)Bus Control Register

- Enable burst transfer after setting Cache Enable. To set Cache Disable, disable burst transfer in advance.

(3)System Support Control Register

- Set Cache Enable before setting DRAM Burst Enable. To set Cache Disable, disable the DRAM Burst Enable bit.
- Before setting DRAM Burst Enable, be sure to set Burst Enable using the Bus Control Register.
- The SAMEPAGE# pin may become “L” at the first CS4 access after setting Same Page Enable.
- The Same Page circuit holds previous data even after the bus master is changed.
- Set the Same Page Mask Register before setting Same Page Enable to “1”.
- Before changing the Same Page Enable (bit 5) setting, set Cache Disable.
- Set all of the Address Range Specifier Registers and Address Mask Registers before setting CS Enable to “1”. (Set all of the Address Range Specifier Registers and Address Mask Registers even if any CS is not to be used.)
- Before changing the CS Enable (bit 4) setting, set Cache Disable.
- When setting the Programmable Wait-state, be sure to set the Wait State Specifier Register.

(4)Wait State Specifier Register

- Do not set the Wait Enable bit and the Single Cycle Non Burst Mode bit to “1” at the same time.
- If the Single Cycle Non Burst Mode bit is set to “1” in the burst mode, the ready signal is generated in one cycle regardless of the setting of the Single Cycle Burst Mode bit.
- When setting the CS3 Wait State Specifier Register, be sure to set the Override bit to“1”. (The Wait State bit can also be set to “1”.)
  When the half-word load instruction is executed with CS3 in 16-bit Bus Mode, the CPU accesses twice but the ready signal from the peripheral resource is generated only once. Therefore the CPU hangs at the second access. To generate the second ready signal, set the Wait Enable bit to “1” (the CPU discards the data received at the second access).

(5)Bus Width/Cacheable Register

- In the DRAM Controller Enable state with CS4# = “L”, CS5 is handled as a Non-Cacheable signal.
- In the DRAM Controller Enable state, the CS5 bus width follows the CS4 bus width setting. When the CS4 Bus Width Control bit has been set to $(10)_2$, for example, the CS5 bus width is forced to be set to $(10)_2$.
- The CS3 Bus Width can be set only to the 16-bit or 32-bit bus width. When the 16-bit bus width is set, use Half-Word Load (address “0”) or Half-Word Store (address “0”) to access the interrupt controller (IRC) and DRAM controller registers.

(6)DRAM Refresh Timer Register

- Be sure to set the Test Mode bit to “0”. Otherwise, TOVF# may not become “L”.
- Since the timer performs counting based on the external clock, it is not affected by the multiplier circuit.

(7)Sleep Mode Register

- To set the sleep mode (low power consumption mode), disable the caches.
- The instruction to set the sleep mode (low power consumption mode) must be followed by at least three NOP instructions.

(8)Trigger Mode Register

- Set the Interrupt Mask Register to $(ffff)_{16}$ before changing the Trigger mode.

- The Request Sense Register may contain “1” when the Trigger Mode is changed. Therefore, issue “Request Clear” before canceling interrupt masks.
  The interrupt controller (IRC) and DRAM controller registers cannot be accessed until CS3# becomes“L”.

(9)Cache Invalidate Register
When the caches are off, write to the Cache Invalidate Register.

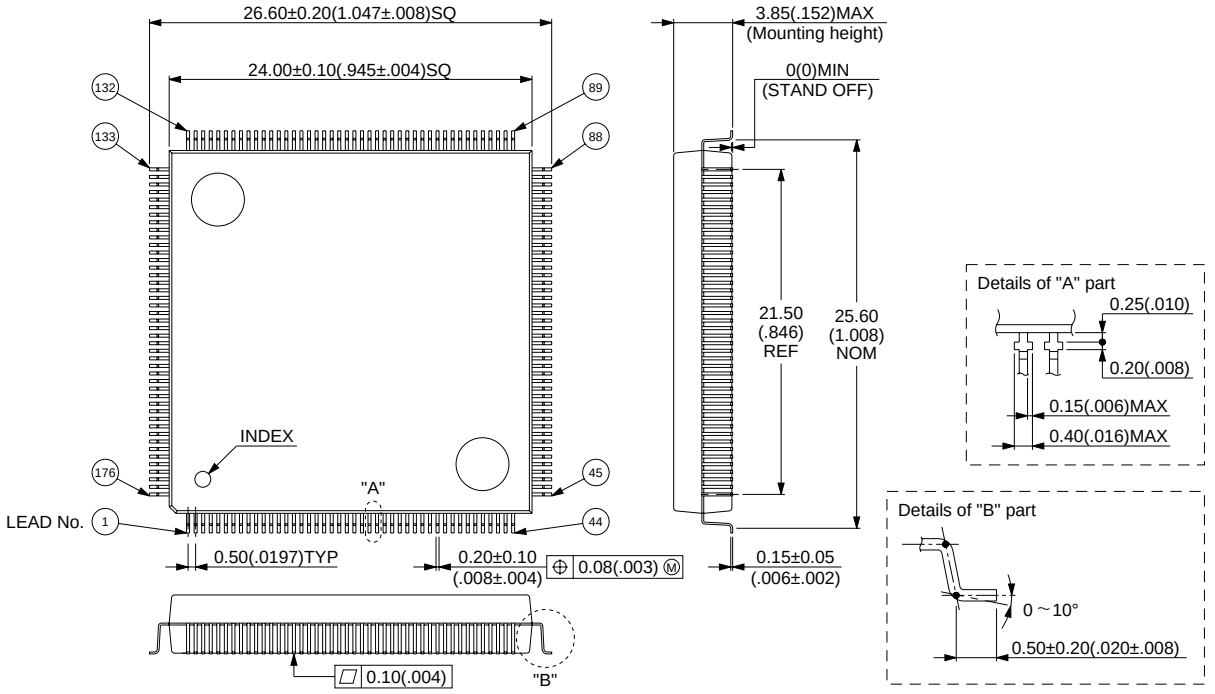
(10)Internal Clock Control/Status Register
To change clock multiplication by setting the CE bit in the internal clock control/status register to “1”, input the “L” pulse to the WKUP# pin at least 4000 CLKIN after entering the sleep mode.

■ ORDERINGINFORMATION

Part number	Package	Remarks
MB86831PFV	Plastic QFP 176-pin (FPT-176P-M01)	
MB86831-80PFV	Plastic QFP 176-pin (FPT-176P-M01)	
MB86832-66PFV	Plastic QFP 176-pin (FPT-176P-M01)	
MB86832- 80PFV	Plastic QFP 176-pin (FPT-176P-M01)	
MB86832-100PFV	Plastic QFP 176-pin (FPT-176P-M01)	
MB86833PMT2	Plastic LQFP 144-pin (FPT-144P-M08)	
MB86834PFV	Plastic QFP 176-pin (FPT-176P-M01)	
MB86834-120PFV	Plastic QFP 176-pin (FPT-176P-M01)	
MB86835PMT2	Plastic LQFP 144-pin (FPT-144P-M08)	
MB86836PMT2	Plastic LQFP 144-pin (FPT-144P-M08)	
MB86836-108PMT2	Plastic LQFP 144-pin (FPT-144P-M08)	Under development
MB86836PBT	Plastic FBGA 144-pin (BGA-144P-M02)	
MB86836-108PBT	Plastic FBGA 144-pin (BGA-144P-M02)	Under development

■ PACKAGE DIMENSIONS

176-pin plastic QFP
(FPT-176P-M01)



Dimensions inmm (inches)

(Continued)

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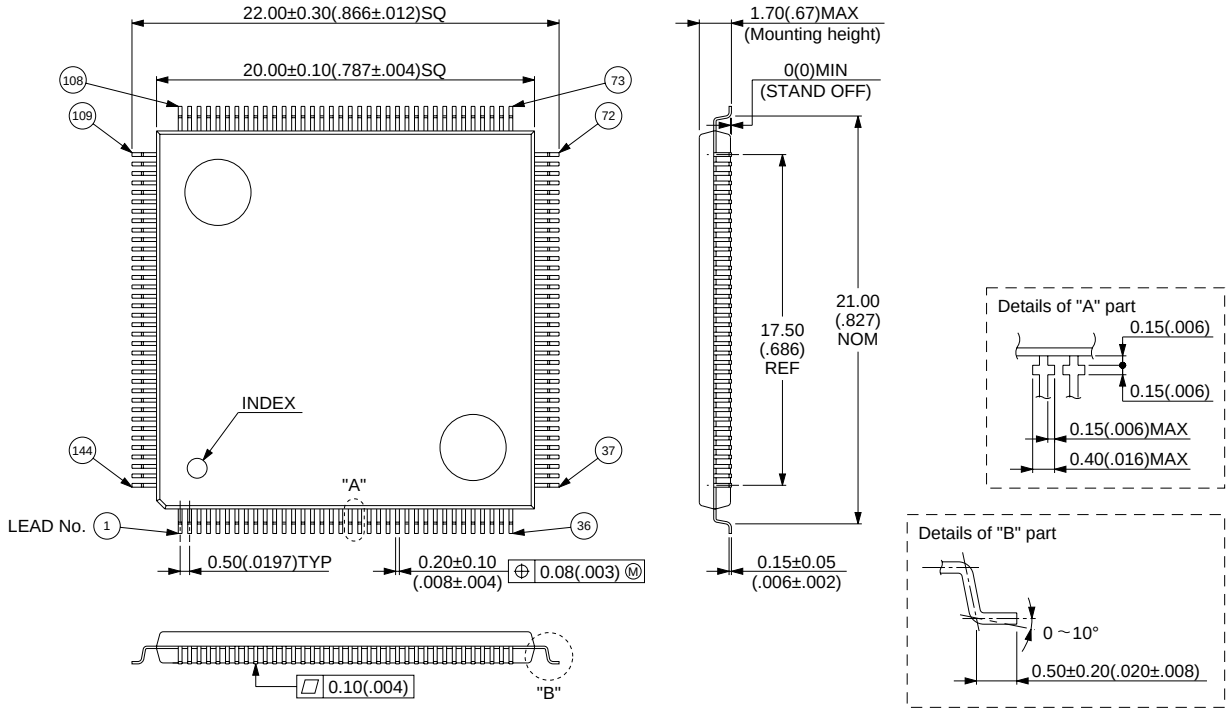
144-pin plastic LQFP
(FPT-144P-M08)



Dimensions inmm (inches)

(Continued)

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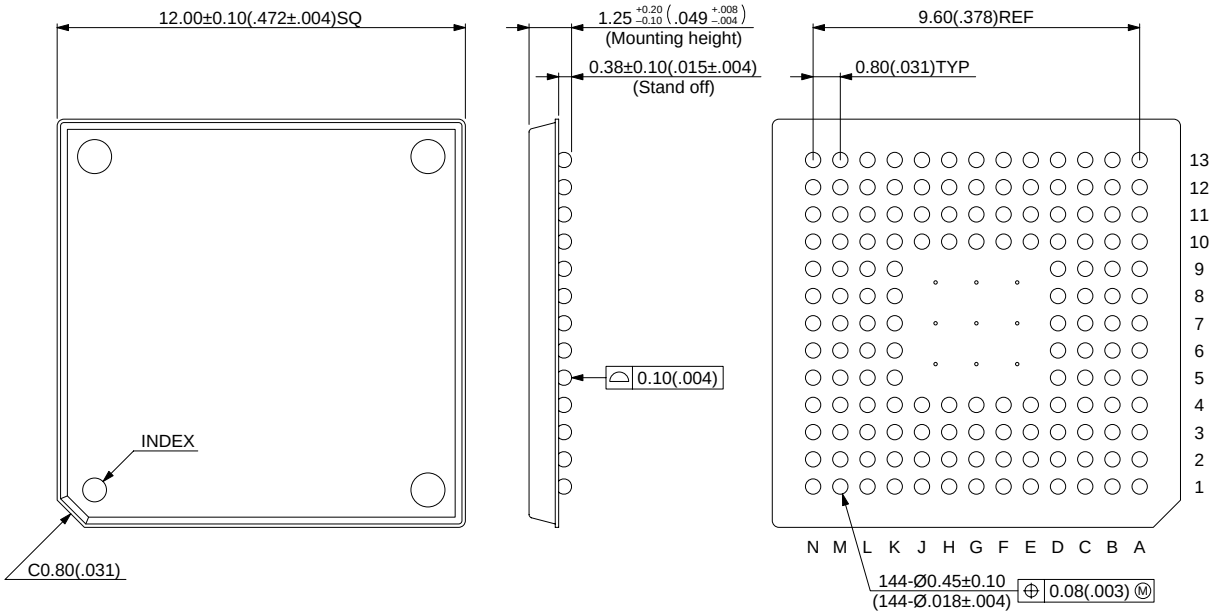
144-pin plastic FBGA
(BGA-144P-M02)



Dimensions inmm (inches)

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