MB86930

930 Series 32-BIT RISC EMBEDDED PROCESSOR

FUJITSU

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FEATURES

- 40 MHz (25ns/cycle) operating frequency
- SPARC high-performance RISC architecture
- 2 Kbytes 2-way set associative instruction cache
- 2 Kbytes 2-way set associative data cache
- Flexible locking mechanism for data and instruction cache entries
- Harvard-style separate instruction and data buses on-chip
- 8 window, 136 word register file
- Fast interrupt response time
- 247 address spaces, 4 Gbyte each
- User and supervisor modes
- Buffered writes and instruction pre-fetching
- Fast page-mode DRAM support
- Programmable address decoder and wait-state generator
- 16-bit auto reload timer
- On-chip clock generator circuit
- JTAG test interface
- Emulator support hardware
- Single vector trapping
- 0.8 micron gate, 3 level metal CMOS technology

GENERAL DESCRIPTION

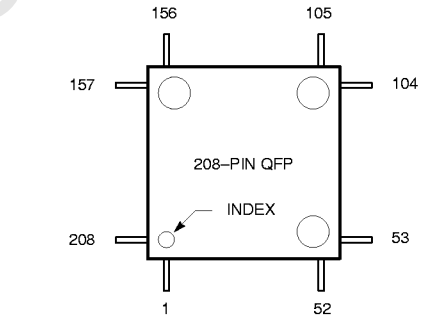
The MB86930 is a member of the 930 series of RISC processors which offers high performance and high integration for a wide range of embedded applications. The processor is based on the SPARC architecture and is upward code compatible with previous implementations. At 40 MHz, the processor executes with 40 MIPs peak and 37 MIPs sustained performance.

On-chip data and instruction caches are included to help decouple the processor from external memory latency. Separate on-chip instruction and data paths provide a high bandwidth interface between the IU and caches. Included to maximize the performance of the system with minimum glue logic, are chip select outputs, programmable wait-state generation and built-in support for a high performance connection to page-mode DRAM. See MB86930 block diagram on page 5.

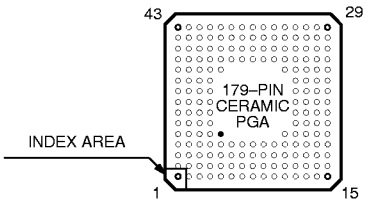
Support for debug and diagnostic tools has been included on-chip and allows for direct connection to hardware emulators and improves debug capability when using ROM based monitors.

These features combine to give the MB86930 superior speed, flexibility and efficiency to make it the ideal choice for a wide variety of low-cost, high-performance embedded systems.

PIN CONFIGURATION



TOP VIEW



(For pin assignment, see pin assignment table)

PIN ASSIGNMENT — 179-PIN PGA

PIN NO.	PIN NAME	TYPE	PIN NO.	PIN NAME	TYPE	PIN NO.	PIN NAME	TYPE	PIN NO.	PIN NAME	TYPE
1	VDD	—	46	ADR < 19 >	O	91	IRL < 2 >	I	136	VSS	—
2	ASI < 0 >	O	47	ADR < 18 >	O	92	ADR < 31 >	O	137	ADR < 24 >	O
3	–BE < 2 >	O	48	ADR < 16 >	O	93	ADR < 29 >	O	138	VDD	—
4	–SAME_PAGE	O	49	ADR < 15 >	O	94	VDD	—	139	VSS	—
5	–CS < 5 >	O	50	ADR < 13 >	O	95	ADR < 23 >	O	140	VDD	—
6	–CS < 2 >	O	51	ADR < 12 >	O	96	ADR < 21 >	O	141	ADR < 10 >	O
7	–CS < 1 >	O	52	VSS	—	97	ADR < 20 >	O	142	ADR < 8 >	O
8	–AS	O	53	ADR < 7 >	O	98	ADR < 17 >	O	143	VDD	—
9	RD/–WR	O	54	ADR < 5 >	O	99	ADR < 14 >	O	144	ASI < 7 >	O
10	–BGRNT	O	55	ADR < 3 >	O	100	ADR < 11 >	O	145	VDD	—
11	–READY	I	56	ASI < 5 >	O	101	ADR < 9 >	O	146	VSS	—
12	–RESET	I	57	ASI < 4 >	O	102	ADR < 6 >	O	147	VSS	—
13	D < 0 >	I/O	58	ASI < 1 >	O	103	ADR < 4 >	O	148	VDD	—
14	VDD	—	59	–BE < 1 >	O	104	ASI < 6 >	O	149	VSS	—
15	VSS	—	60	VDD	—	105	ASI < 3 >	O	150	VDD	—
16	VDD	—	61	VSS	—	106	ASI < 2 >	O	151	VSS	—
17	D < 10 >	I/O	62	–CS < 3 >	O	107	–BE < 0 >	O	152	D < 1 >	I/O
18	D < 14 >	I/O	63	–CS < 0 >	O	108	–BE < 3 >	O	153	D < 4 >	I/O
19	D < 15 >	I/O	64	–LOCK	O	109	–CS < 4 >	O	154	VSS	—
20	D < 16 >	I/O	65	VDD	—	110	VSS	—	155	VSS	—
21	D < 17 >	I/O	66	–MEXC	I	111	–ERROR	O	156	VDD	—
22	D < 20 >	I/O	67	VDD	—	112	VSS	—	157	VSS	—
23	D < 21 >	I/O	68	D < 3 >	I/O	113	–BREQ	I	158	VDD	—
24	VDD	—	69	VSS	—	114	D < 2 >	I/O	159	VSS	—
25	D < 25 >	I/O	70	VDD	—	115	D < 6 >	I/O	160	D < 30 >	I/O
26	D < 28 >	I/O	71	D < 9 >	I/O	116	D < 7 >	I/O	161	EMU_D < 0 >	I/O
27	D < 29 >	I/O	72	D < 12 >	I/O	117	D < 8 >	I/O	162	VSS	—
28	VSS	—	73	D < 13 >	I/O	118	D < 11 >	I/O	163	VSS	—
29	VDD	—	74	VDD	—	119	VSS	—	164	VDD	—
30	EMU_SD < 1 >	I/O	75	D < 18 >	I/O	120	D < 19 >	I/O	165	VSS	—
31	VDD	—	76	D < 22 >	I/O	121	D < 23 >	I/O	166	VDD	—
32	VSS	—	77	VSS	—	122	D < 24 >	I/O	167	VSS	—
33	CLKOUT2	O	78	D < 26 >	I/O	123	D < 27 >	I/O	168	VDD	—
34	XTAL1	I	79	VDD	—	124	D < 31 >	I/O	169	ADR < 28 >	O
35	XTAL2	O	80	VDD	—	125	EMU_D < 2 >	I/O	170	VSS	—
36	–TIMER_OVF	O	81	–EMU_ENB	I	126	EMU_D < 3 >	I/O	171	VSS	—
37	TDO	O	82	EMU_SD < 0 >	I/O	127	EMU_SD < 2 >	I/O	172	VDD	—
38	–TMS	I	83	EMU_SD < 3 >	I/O	■ 128	–EMU_BRK	I	173	VSS	—
39	TDI	I	84	VSS	—	129	CLKOUT1	O	174	VDD	—
40	IRL < 1 >	I	85	VDD	—	130	VDD	—	175	VSS	—
41	IRL < 3 >	I	86	VSS	—	131	VSS	—	176	ADR < 2 >	O
42	ADR < 30 >	O	87	VDD	—	■ 132	–TRST	I	177	D < 5 >	I/O
43	VDD	—	88	VDD	—	133	IRL < 0 >	I	178	EMU_D < 1 >	I/O
44	ADR < 25 >	O	89	TCK	I	134	VSS	—	179	ADR < 27 >	O
45	ADR < 22 >	O	90	CLK_ECB	I	135	ADR < 26 >	O			

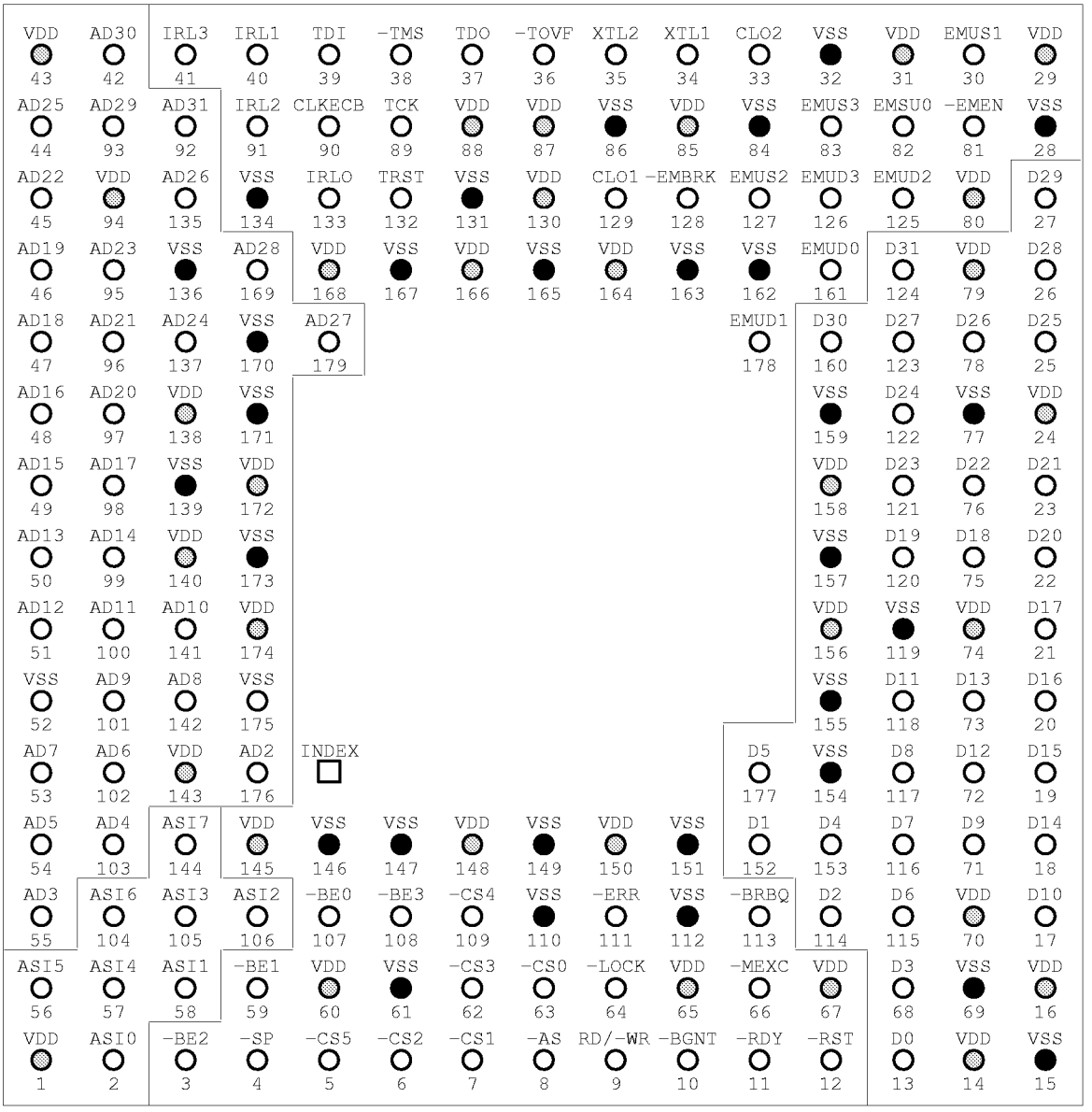
ORDERING CODE

Clock Frequency (MHz)	Ordering Code	Package Type	Marking on Part	P/N on Box
20	MB86930-20PFV-G	Plastic QFP 208	MB86930-20	MB86930-20PFV-G-BND
30	MB86930-30ZF-G	Ceramic QFP 208	MB86930-30	MB86930-30ZF-G-BND
40	MB86930-40ZF-G	Ceramic QFP 208 w/FIN	MB86930-40	MB86930-40ZF-G-BND-FIN
40	MB86930-40CR-G	Ceramic PGA 179	MB86930-40	MB86930-40CR-G-BND

Note: The ordering code is for production level product. Early shipments of this device may be marked with "ES" to indicate that the part is not yet at full production status. Contact your local Fujitsu representative for additional information on "ES" level products.

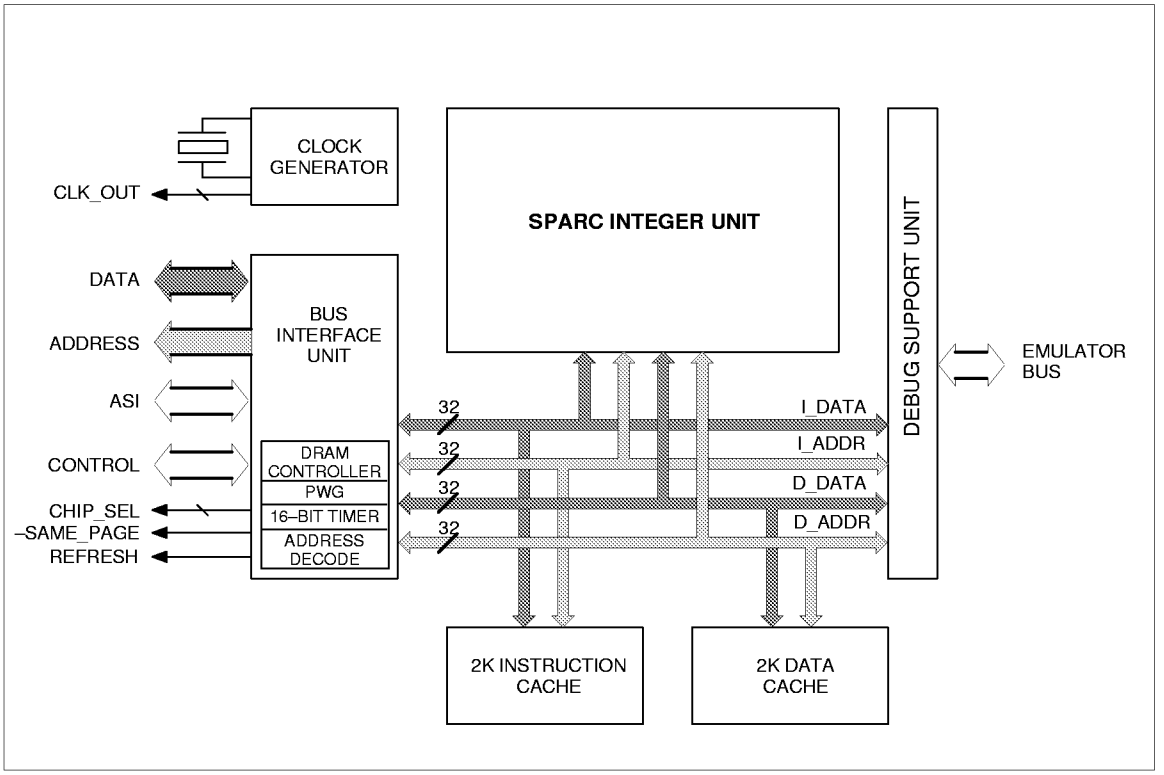
PIN ASSIGNMENT — 208-PIN QFP

PIN NO.	PIN NAME	TYPE	PIN NO.	PIN NAME	TYPE	PIN NO.	PIN NAME	TYPE	PIN NO.	PIN NAME	TYPE
1	ADR < 28 >	O	53	EMU_D < 0 >	I/O	105	D < 4 >	I/O	157	VDD	—
2	ADR < 29 >	O	54	VSS	—	106	VSS	—	158	N.C.	—
3	ADR < 30 >	O	55	–EMU_ENB	I	107	VDD	—	159	ASI < 4 >	O
4	ADR < 31 >	O	56	VSS	—	108	D < 3 >	I/O	160	ASI < 5 >	O
5	VDD	—	57	VDD	–	109	D < 2 >	I/O	161	ASI < 6 >	O
6	VSS	—	58	D < 31 >	I/O	110	D < 1 >	I/O	162	ASI < 7 >	O
7	VDD	—	59	D < 30 >	I/O	111	D < 0 >	I/O	163	ADR < 2 >	O
8	IRL < 3 >	I	60	D < 29 >	I/O	112	VDD	—	164	ADR < 3 >	O
9	IRL < 2 >	I	61	VDD	—	113	–RESET	I	165	ADR < 4 >	O
10	IRL < 1 >	I	62	D < 28 >	I/O	114	–BREQ	I	166	ADR < 5 >	O
11	IRL < 0 >	I	63	D < 27 >	I/O	115	VSS	—	167	VDD	—
12	VSS	—	64	VSS	—	116	–MEXC	I	168	VSS	—
13	CLK_ECB	I	65	D < 26 >	I/O	117	–READY	O	169	ADR < 6 >	O
14	TDI	I	66	D < 25 >	I/O	118	VSS	—	170	ADR < 7 >	O
15	–TRST	I	67	D < 24 >	I/O	119	VDD	—	171	N.C.	—
16	TCK	I	68	VSS	—	120	–BGRNT	O	172	ADR < 8 >	O
17	TMS	I	69	VDD	—	121	VDD	—	173	ADR < 9 >	O
18	VDD	—	70	VDD	—	122	–ERROR	O	174	VSS	—
19	VSS	—	71	VDD	—	123	–LOCK	O	175	VDD	—
20	VSS	—	72	D < 23 >	I/O	124	N.C.	—	176	ADR < 10 >	O
21	VDD	—	73	D < 22 >	I/O	125	RD/–WR	O	177	N.C.	—
22	VDD	—	74	VSS	—	126	–AS	O	178	ADR < 11 >	O
23	VSS	—	75	D < 21 >	I/O	127	N.C.	—	179	ADR < 12 >	O
24	TDO	O	76	D < 20 >	I/O	128	VSS	—	180	VDD	—
25	–TIMER_OVF	O	77	VDD	—	129	VSS	—	181	ADR < 13 >	O
26	VDD	—	78	D < 19 >	I/O	130	VSS	—	182	VDD	—
27	VSS	—	79	VSS	—	131	–CS < 0 >	O	183	VSS	—
28	VDD	—	80	D < 18 >	I/O	132	N.C.	—	184	ADR < 14 >	O
29	XTAL2	O	81	N.C.	—	133	–CS < 1 >	O	185	VSS	—
30	XTAL1	I	82	D < 17 >	I/O	134	VSS	—	186	ADR < 15 >	O
31	VSS	—	83	D < 16 >	I/O	135	–CS < 2 >	O	187	ADR < 16 >	O
32	N.C.	—	84	VDD	—	136	–CS < 3 >	O	188	N.C.	—
33	CLKOUT1	O	85	VSS	—	137	–CS < 4 >	O	189	ADR < 17 >	O
34	VDD	—	86	VDD	—	138	N.C.	—	190	VSS	—
35	CLKOUT2	O	87	D < 15 >	I/O	139	VDD	—	191	VDD	—
36	VSS	—	88	N.C.	—	140	–CS < 5 >	O	192	ADR < 18 >	O
37	N.C.	—	89	D < 14 >	I/O	141	–SAME_PAGE	O	193	ADR < 19 >	O
38	VDD	—	90	D < 13 >	I/O	142	VDD	—	194	ADR < 20 >	O
39	VSS	—	91	D < 12 >	I/O	143	VSS	—	195	N.C.	—
40	N.C.	—	92	D < 11 >	I/O	144	VDD	—	196	ADR < 21 >	O
41	–EMU_BRK	I	93	VSS	—	145	N.C.	—	197	VDD	—
42	VSS	—	94	D < 10 >	I/O	146	–BE < 3 >	O	198	VSS	—
43	VDD	—	95	D < 9 >	I/O	147	VSS	—	199	ADR < 22 >	O
44	EMU_SD < 3 >	I/O	96	D < 8 >	I/O	148	–BE < 2 >	O	200	ADR < 23 >	O
45	EMU_SD < 2 >	I/O	97	VDD	—	149	–BE < 1 >	O	201	ADR < 24 >	O
46	EMU_SD < 1 >	I/O	98	VSS	—	150	–BE < 0 >	O	202	ADR < 25 >	O
47	VSS	—	99	VSS	—	151	ASI < 0 >	O	203	VSS	—
48	VDD	—	100	VDD	—	152	VSS	—	204	VDD	—
49	EMU_SD < 0 >	I/O	101	D < 7 >	I/O	153	VDD	—	205	VDD	—
50	EMU_D < 3 >	I/O	102	D < 6 >	I/O	154	ASI < 1 >	O	206	VSS	—
51	EMU_D < 2 >	I/O	103	N.C.	—	155	ASI < 2 >	O	207	ADR < 26 >	O
52	EMU_D < 1 >	I/O	104	D < 5 >	I/O	156	ASI < 3 >	O	208	ADR < 27 >	O



MB86930 179 PGA Pin Assignment (Top View)

BLOCK DIAGRAM



SIGNAL DESCRIPTIONS

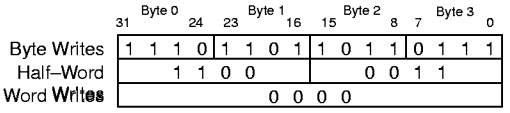
SYMBOL	TYPE	DESCRIPTION
–RESET	I A (L)	**SYSTEM RESET:** Asserting reset for at least 4 processor cycles after the clock has stabilized, causes the MB86930 to be initialized.
XTAL1, (CLK_IN) XTAL2	I/O O G (Q) I (Q)	**EXTERNAL OSCILLATOR:** The crystal inputs determine execution rate and timing of the MB86930 processor. Connecting a crystal to these pins forms a complete crystal oscillator circuit. The crystal oscillator frequency is the same as the processor operating frequency. When driving the processor with an external clock, XTAL2 pin should be left floating.
CLKOUT1	O G (Q) I (Q)	**CLOCK OUTPUT 1:** This is an output signal against which MB86930 bus transactions can be referenced. The CLKOUT1 frequency is the same as the frequency applied to XTAL1 and is the same as the processor operating frequency. CLKOUT1 is in phase with CLK_IN.
CLKOUT2	O G (Q) I (Q)	**CLOCK OUTPUT 2:** This is an output signal against which MB86930 bus transactions can be referenced. The CLKOUT2 frequency is the same as the frequency applied to XTAL1 and is the same as the processor operating frequency. CLKOUT2 is out of phase with CLK_IN.
–LOCK	O S (L) G (Z) I (1)	**BUS LOCK:** This is a control signal asserted by the processor to indicate to the system that the current bus transaction requires more than one transfer on the bus. The Atomic Load Store instruction for example requires contiguous bus transactions which cause the assertion of the bus lock signal. The bus may not be granted to another bus owner as long as –LOCK is active. –LOCK is asserted with the assertion of –AS and remains active until –READY is asserted at the end of the locked transaction.
–BREQ	I S (L)	**BUS REQUEST:** Asserted by another device on the bus to indicate that it wants ownership of the bus. The request must be answered with a bus grant (–BGRNT) from the MB86930 before the device can proceed by driving the bus. Once the bus has been granted, the device has ownership of the bus until it de–asserts –BREQ. The user should ensure that devices on the bus cannot monopolize the bus to the exclusion of the CPU. Inputs to –BREQ while –RESET is active are valid and cause Bus Grant to be asserted.
–BGRNT	O S (L) G (0) I (Q)	**BUS GRANT:** Asserted by the CPU in response to a request from a device wanting ownership of the bus. The CPU grants the bus to other devices only after all transfers for the current transaction are completed. See the "Note" section at the end of this table and the "Type" column for other signals to determine the effect due to the assertion of –BGRNT.
–ERROR	O A (L) G (Q) I (Q)	**ERROR SIGNAL:** Asserted by the CPU to indicate that it has halted in an error state as a result of encountering a synchronous trap while traps are disabled. In this situation the CPU saves the PC and nPC registers, sets the tt value in the TBR, enters into an error state and asserts the –ERROR signal. The system can monitor the –ERROR pin and initiate a reset under the error condition. This pin is high on reset.
–MEXC	I S (L)	**MEMORY EXCEPTION:** Asserted by the memory system to indicate a memory error on either a data or instruction access. Assertion of this signal initiates either a data or instruction access exception trap in the IU. The current bus access is invalidated by asserting the –MEXC in the same cycle as the –READY signal. Assertion in any other bus cycle gives indeterminate results. The IU ignores the contents of the data bus in cycles where –MEXC is asserted.
IRL <3:0>	I S (L)	**INTERRUPT REQUEST BUS:** The value on these pins defines the external interrupt level. IRL <3:0>=1111 forces a non–maskable interrupt. IRL value of 0000 indicates no pending interrupts. All other values indicate maskable interrupts as enabled in the PIL field of the processor status register (PSR). Interrupts should be latched and prioritized by external logic and should be held pending until acknowledged by the processor. An interrupt controller is available on the MB86940.

1. In the following descriptions, signal names preceded by a minus sign (–) indicate an active low state. Dual function pins have two names separated by a slash (/).

SIGNAL DESCRIPTIONS (Continued)

SYMBOL	TYPE	DESCRIPTION
–TIMER_OVF	O S (L) G (Q) I (Q)	**TIMER UNDERFLOW:** Asserted by the processor to indicate that the internal 16–bit timer has underflowed. This signal can be used to initiate a DRAM refresh cycle or a one cycle periodic waveform. On reset, the timer is turned off and –TIMER_OVF is high.
–SAME_PAGE	O S (L) G (1) I (1)	**SAME–PAGE DETECT:** The –SAME_PAGE is used to take advantage of fast consecutive accesses within Fast Page Mode DRAM page boundaries. This signal is an output asserted by the processor when the current address is within the same page as the previous memory access. The –SAME_PAGE signal is asserted with –AS and remains active for one processor cycle. –SAME_PAGE is never asserted in the first transaction following a transaction by another device on the bus. The page size is specified by writing the SAME–PAGE MASK register.
–CS0, –CS1, –CS2, –CS3, –CS4, –CS5	O S (L) G (1) I (1)	**CHIP SELECTS:** These outputs are asserted when the value on the address bus matches the address range in one of the corresponding ADDRESS RANGE registers. The signals are used to decode the current address into one of six address ranges. Address ranges should not overlap. Each address range has a corresponding wait specifier which is used to automatically assert the –READY signal after a user defined number of processor clock cycles. This allows a variety of memory and I/O devices with different access times to be connected to the MB86930 without the need for additional logic.
ADR < 31:2>	O S (L) G (Z) I (1)	**ADDRESS BUS:** The 30–bit ADDRESS BUS (A31–A2) is an output which identifies the data or instruction address of a 32–bit word. Reads are always one word in size while byte, half–word, or word transaction sizes for writes is identified by separate byte–enable signals (–BE0–3). The address bus is valid for the duration of the bus transaction.
ASI < 7:0>	O S (L) G (Z) I (1)	**ADDRESS SPACE IDENTIFIERS:** The ADDRESS SPACE IDENTIFIERS are outputs which indicate to which of 256 available spaces the current ADDRESS BUS value corresponds. The ASI values are defined as follows: **ASI < 7:0> — ADDRESS SPACE** 0x1 — Control Registers 0x2 — Instruction Cache Lock 0x3 — Data Cache Lock 0x4 – 0x7 — Application Definable 0x8 — User Instruction Space 0x9 — Supervisor Instruction Space 0xA — User Data Space 0xB — Supervisor Data Space 0xC — Instruction Cache Tag RAM 0xD — Instruction Cache Data RAM 0xE — Data Cache Tag RAM 0xF — Data Cache Data RAM 0x10 – 0xFD — Application Definable 0xFE – 0xFF — Reserved for Debug Hardware The ASI values specified as “application definable” can be used by supervisor mode instructions such as **Load Alternate** and **Store Alternate**. The ASI value is available in the same cycle in which the corresponding address value is asserted on the address bus. The ASI pins are valid for the duration of the bus transaction. ASI values 0x8, 0x9, 0xA, and 0xB are cacheable.

SIGNAL DESCRIPTIONS (Continued)

SYMBOL	TYPE	DESCRIPTION
–BE3–0	O S (L) G (Z) I (O)	**BYTE ENABLES:** These pins indicate whether the current store transaction is a byte, half-word or word transaction. –BE3–0 signals are available in the same cycle in which the corresponding address value is asserted on the address bus and is valid for the duration of the bus transaction. This bus should be used only to qualify store transactions. For load transactions all sub–word requests are read (and replaced in the cache) as words and then the appropriate byte or half–word is extracted by the integer unit. Possible values for –BE3–0 are as follows: 
D <31:0>	I/O S (L) G (Z) I (Z)	**DATA BUS:** The bus interface has 32 bidirectional data pins (D31–D0) to transfer data in thirty–two bit quantities. D(31) corresponds to the most significant bit of the least significant byte of the 32–bit word. A double word is aligned on an 8–byte boundary, a word is aligned on a 4–byte boundary, and a half–word is aligned on a 2–byte boundary. If a load or store of any of these quantities is not properly aligned, a Not Aligned Trap will occur in the processor. In write bus cycles, the point at which data is driven onto the bus depends on the type of the preceding cycle. If the preceding cycle was a write, data is driven in the cycle immediately following the cycle in which –READY was asserted. If the preceding cycle was a read, data is driven one cycle after the cycle in which –READY was asserted to minimize bus contention between the processor and the system. All bits of the data bus are driven regardless of word size. The values on the pins not corresponding to the byte or half–word being written are undefined.
–AS	O S (L) G (Z) I (1)	**ADDRESS STROBE:** A control signal asserted by the MB86930 or other bus master to indicate the start of a new bus transaction. A bus transaction begins with the assertion of –AS and ends with the assertion of –READY. –AS remains asserted for 1 clock cycle. During cycles in which neither the processor nor another bus master is driving the bus the bus is idle, and –AS remains de–asserted.
RD/–WR	O S (L) G (Z) I (1)	**READ/BUS TRANSACTION:** This signal specifies whether the current bus transaction is a read or a write operation. When –AS is asserted and RD/–WR is low, then the current transaction is a write. With –AS asserted and RD/–WR high, the current transaction is a read. RD/–WR remains active for the duration of the bus transaction and is de–asserted with the assertion of –READY.
–READY	I S (L)	**READY:** This is a control signal asserted by the external memory system to indicate that the current bus transaction is being completed and that it is ready to start with the next bus transaction in the following cycle. In case of a fetch from memory, the processor will strobe the value on the data bus at the rising edge of CLK_IN following the assertion of –READY. For the case of a write, the memory system will assert –READY when the appropriate access time has been met. In most cases, no additional logic is required to generate the –READY signal. On–chip circuitry can be programmed to assert –READY based on the address of the current transaction. The external system can override the internal ready generator to terminate the current bus cycle early. Up to 6 address ranges each with different transaction times can be programmed.
CLK_ECB	I	**EXTERNAL CLOCK BYPASS:** Tying this signal high causes the CLK_IN signal to bypass the Phases Lock Loop (PLL). This signal is used for testing of the chip.
EMU_SD <3:0>	I/O	**EMULATOR STATUS/DATA BITS:** Bi–directional pins used by a hardware emulator to control and monitor MB86930 execution. These pins should be left unconnected.

SIGNAL DESCRIPTIONS (Continued)

SYMBOL	TYPE	DESCRIPTION
EMU_D < 3:0>	I/O	**EMULATOR DATA BITS:** Bi–directional pins used by a hardware emulator to control and monitor MB86930 execution. These pins should be left unconnected.
–EMU_BRK	I	**EMULATOR BREAK REQUEST LINE:** Input used by a hardware emulator to request a trap when emulation is enabled. This pin should be left unconnected.
–EMU_ENB	I	**EMULATOR ENABLE:** Tied low while the MB86930 is being reset to enable hardware emulator mode on the chip. This pin should be left unconnected.
TCK	I	**TEST CLOCK:** JTAG compatible test clock input.
TMS	I	**TEST MODE:** JTAG compatible test mode select pin.
TDI	I	**TEST DATA IN:** JTAG compatible test data input.
TDO	O	**TEST DATA OUT:** JTAG compatible test data output.
–TRST	I	**TEST RESET:** Asynchronous reset for JTAG logic. If not using JTAG, this signal must be pulled low.

NOTE:
I = Input Only Pin
O = Output Only Pin
I/O = Either Input or Output Pin
– = Pins "must be" connected as described
A(L)= Asynchronous: Inputs may be asynchronous to CLKOUT.
S(L)= Synchronous: Inputs must meet setup and hold times relative to CLK_IN Outputs are Synchronous to CLK_IN

G(...) = While the bus is granted to another bus master (–BGRNT=asserted), the pir is
G (1) is driven to V_{CC}
G (0) is driven to V_{SS}
G (Z) floats
G(Q) is a valid output

I (...) = While the bus is between bus cycles (or being reset) and is not granted to another bus master, the pin is
I (1) is driven to V_{CC}
I (0) is driven to V_{SS}
I (Z) floats
I (Q) is a valid output

OVERVIEW

The Fujitsu MB86930 is a high–performance, 32–bit RISC processor which executes at 40 MIPs peak and 37 MIPs sustained performance with 40 MHz clock frequency. It is a fourth generation version of Fujitsu's popular MB86900, MB86901 and MB86902 processors. Like its predecessors, the MB86930 is based on the SPARC architecture and is upward code compatible with previous implementations. Most importantly, the MB86930 has been developed specifically with the needs of embedded applications in mind and offers high performance and high integration for these applications.

The MB86930 instruction set is streamlined and hardwired for fast execution with most instructions executing in a single cycle. The Integer Unit (IU) features a 5–stage pipeline which has been designed to handle data interlocks, has an optimized branch handler for efficient control transfers, and a bus interface to handle single cycle bus accesses to on–chip memory.

An internal register file consisting of 136 registers organized into eight overlapping windows speeds interrupt response time and context switches. The register file minimizes accesses to memory during procedure linkages and facilitates passing of parameters and assignment of variables.

On–chip 2 Kbyte data and instruction caches have been added to decouple the processor from external memory. These caches have been designed with maximum flexibility in mind and allow entries to be locked to improve overall system performance.

Separate 32–bit on–chip instruction and data paths provide a high bandwidth interface between the IU and on–chip cache. These buses support single cycle instruction execution as well as single cycle data transfers with the cache. Future expansion of the MB86930 design is supported by this bus definition as well.

The MB86930 also includes hardware for integer multiply and divide. The hardware support significantly improves the performance of these operations with 32–bit integer multiplies executing in 5 clock cycles, 16–bit integer multiplies in 3 cycles, 8–bit integer multiplies in 2 cycles, and a multiply by zero can complete in a single cycle.

KEY FEATURES

Fast Instruction Execution: Simple functions make up the bulk of instructions in most programs so that execution speed can be greatly improved by designing these instructions to execute in as short a time as possible. The majority of instructions execute in one cycle with only a few of the more complex, such as integer multiply, taking additional cycles.

Large Register Set: The large register set reduces the number of required accesses to data memory. The registers are organized in overlapping groups called register windows which allows registers to be reserved for high priority tasks, such as interrupts, or for recurring requirements such as operating system working registers. The overlapping windows also simplify parameter passing during procedure linkage and reduce code in most programs.

On–Chip Caches: To decouple the speed of the processor from the memory sub–system, data and instructions caches have been added. The caches are organized as two–way set–associative for improved hit rates. In addition, the set–associative caches allow entries to be locked, individually or as a bank, without significantly degrading the cache performance.

Cache Locking: Both data and instruction entries can be locked into their respective caches to ensure deterministic response and highest performance for critical or frequently recurring routines. Maximum flexibility has been designed into the cache to allow all or selected portions to be locked.

Bus Interface: The requirement for glue logic between the MB86930 and the system is minimized by providing programmable chip selects, programmable wait–state circuitry, and support for connection to fast page–mode DRAM. Multiple bus masters are supported through a simple handshake protocol.

Clock Generator: To simplify the clock design a crystal can be connected directly to the on–chip oscillator or an external clock source can be used. A built in phase–locked loop minimizes the skew between on and off–chip clocks.

Enhanced Instruction Set: The MB86930 incorporates a fast integer multiply instruction which executes in a fast 5, 3 or 2 cycles for 32–bit, 16–bit or 8–bit multiplicands. An integer divide–step instruction cuts divide times by a factor of 10 over previous SPARC implementations. A scan instruction supports a single cycle search for the most significant 1 or 0 in a word.

Fully Static Circuit Design: Embedded applications that need a means to reduce power consumption can take advantage of the MB86930's fully static design. The processor clock can be slowed or stopped for arbitrary periods of time to reduce operating current with no loss of internal state. Noise immunity is improved as well. (Note: stopping the clock will result in the Phase–Lock Loop losing lock. Lock must be re–established before normal operation can be resumed.)

Test and Debug Interface: The MB86930 supports production test through industry standard JTAG boundary scan. Hardware emulation is supported with on–chip breakpoint and single step logic. A dedicated emulator bus provides a means to trace transactions between the integer unit and on–chip cache.

CPU

The MB86930 core is a high performance full custom implementation of the SPARC architecture. The core is compact to leave room for peripheral integration and yet is designed in a way to allow the major blocks to be customized for varying application requirements. The core is made up of three functional units: the Instruction block, the Address block and the Execute block (see Figure 1).

A five stage instruction pipeline is responsible for decoding all instructions and generating the control signals to the other blocks. The 5–stage pipeline consists of Fetch (F), Decode (D), Execute (E), Memory (M) and Writeback (W). Instruction memory is addressed and returns instructions in the (F) stage, the register file is addressed and returns operands in the (D) stage, the ALU computes results in the (E) stage, external memory is addressed in the (M) stage, and the register file is written back in the (W) stage.

TABLE 1. MB86930 Instruction Set

LOGICAL	ARITHMETIC/SHIFT	DATA MOVEMENT
CONDITION CODES UNCHANGED AND OR XOR AND NOT OR NOT XNOR **CONDITION CODES SET** AND OR XOR AND NOT OR NOT XNOR	**CONDITION CODES UNCHANGED** ADD SUBTRACT MULTIPLY(SIGNED/UNSIGNED) SCAN SETHI SHIFT LEFT LOGICAL SHIFT RIGHT LOGICAL SHIFT RIGHT ARITHMETIC **CONDITION CODES SET** ADD SUBTRACT MULTIPLY(SIGNED/UNSIGNED) MULTIPLY STEP DIVIDE STEP **EXTENDED AND CONDITION CODES UNCHANGED** ADD SUBTRACT **EXTENDED AND CONDITION CODES SET** ADD SUBTRACT **TAGGED AND CONDITION CODES SET (WITH AND WITHOUT TRAP ON OVERFLOW)** ADD SUBTRACT	**TO USER/SUPERVISOR SPACE SIGNED** LOAD BYTE LOAD HALF–WORD LOAD WORD LOAD DOUBLE WORD STORE BYTE STORE HALF–WORD STORE WORD STORE DOUBLE WORD **TO USER SPACE UNSIGNED** LOAD BYTE LOAD HALF–WORD **TO ALTERNATE SPACE SIGNED** LOAD BYTE LOAD HALF–WORD LOAD WORD LOAD DOUBLE WORD STORE BYTE STORE HALF–WORD STORE WORD STORE DOUBLEWORD **TO ALTERNATE SPACE UNSIGNED** LOAD BYTE LOAD HALF–WORD **ATOMIC OPERATION IN USER SPACE** SWAP WORD LOAD/STORE UNSIGNED BYTE **ATOMIC OPERATION IN ALTERNATE SPACE** SWAP WORD LOAD/STORE UNSIGNED BYTE
CONTROL TRANSFER		
CONDITIONAL BRANCH CONDITIONAL TRAP CALL RETURN SAVE RESTORE JUMP AND LINK		
READ/WRITE CONTROL REGISTER		
READ PSR WRITE PSR READ TBR WRITE TBR	READ WIM WRITE WIM READ Y WRITE Y	RDASR WRASR

ADDRESS SPACE

The MB86930 offers a large addressing range and allows separate user and supervisor spaces to be defined. In addition to 32 address lines, 4 alternate address space identifiers (ASIs) distinguish between protected and unprotected space. Of the 256 possible ASI values, two define accesses to user data and user instruction space while the remaining ASI values define supervisor space.

Anytime a reset, synchronous trap or asynchronous trap occurs, the processor is placed into the supervisor mode. In this mode, the processor executes instructions and moves data out of supervisor space. While in supervisor mode, the processor also has access to the remaining ASI values. Except for those mentioned and those reserved for control register space, the remaining ASI values can be used to access other alternate data spaces defined by the application.

The distinction of user versus supervisor space allows the hardware to protect against accidental or un–authorized access to system resources. For real time operating system (RTOS) development for example, the separate spaces provide a mechanism for effectively partitioning RTOS space from user space.

REGISTERS

The MB86930 register set is divided into those used for general purpose functions and those used for control and status.

The 136 general purpose registers are divided into 8 global registers and 8 overlapping blocks or "windows". Each window contains 24 registers. Of these, 8 are local to the window, 8 "out" registers overlap with the next window and 8 "in" registers overlap with the previous window (see Figure 2).

This organization makes it easy to pass parameters to subroutines. Parameters that are to be passed along are written to the "out" registers and the subsequent procedure call decrements the window pointer to make a new set of registers available. The passed parameters are now available to the subroutine in the current window's "in" registers.

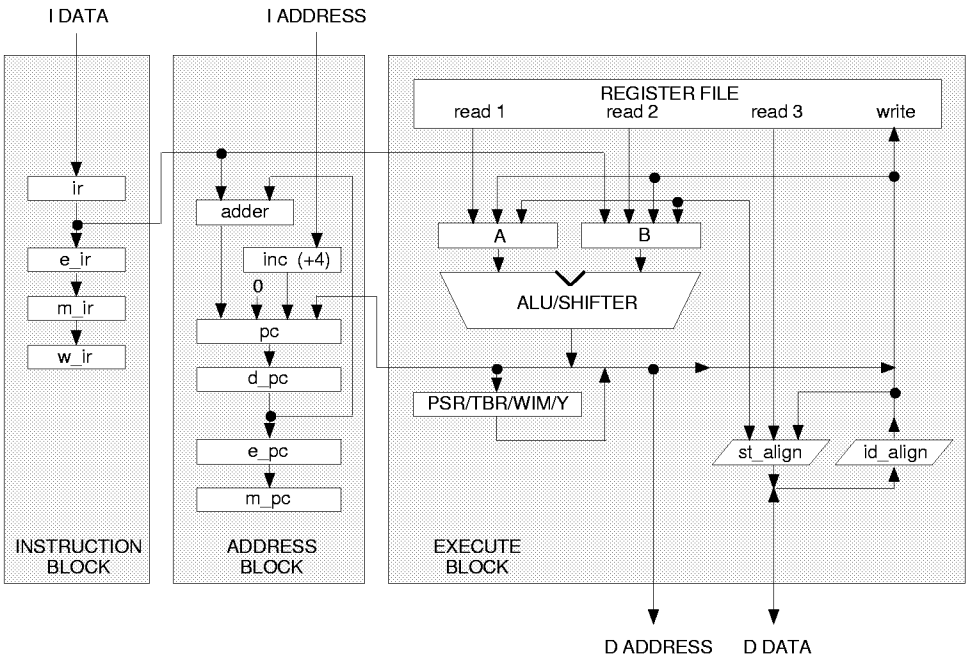


Figure 1. MB86930 Integer Unit Data Path

Register windows improve performance in embedded applications because they function as local variable caches which retain either interrupt, subroutine, context or operating system variables with no additional overhead. In addition, code can be reduced by exploiting the efficient execution of procedure linkage by preventing in–lining compiler optimizations.

The registers that make up the register file each have three read–only and one write–only port. The use of a four port register file allows even store instructions, which may require that three operands be read out of the register file, to proceed at one instruction per cycle.

The control and status registers include those defined by the SPARC architecture (see Table 1) and those mapped into alternate address space to control peripheral functions (see Table 2).

INSTRUCTION SET

The MB86930 is upward code compatible with other SPARC processors. Additional instructions, previously not directly supported, have been added to improve performance in embedded applications. Integer multiply, integer divide step, and scan for first changed bit have been added to the already powerful SPARC instruction set. See Table 1 for a list of supported instructions.

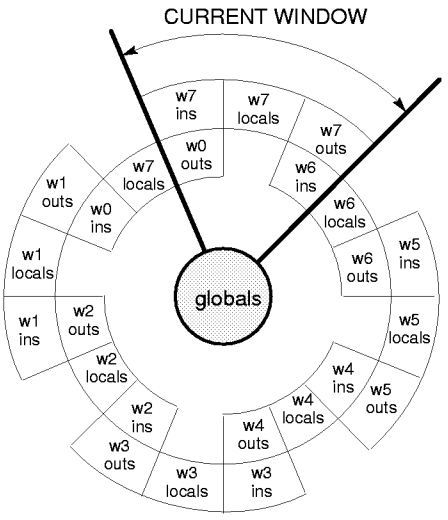


Figure 2. General Purpose Register Organization

INTERRUPTS

A key measure of a processor's suitability for use in embedded application is in its ability to handle interrupts with a minimum of delay and in a deterministic fashion. The MB86930 implementation has been tailored to insure not only low average latency but low maximum latency as well.

Interrupt response time is made up of the sum of the times it takes the processor to finish its current task after recognizing an interrupt, and the time it takes to begin executing interrupt service routine instructions. The MB86930 implements numerous features to minimize both factors.

To minimize the time it takes to finish the current task, the MB86930 is designed so that tasks can either be interrupted or completed in a minimum of cycles. Implementation details that accomplish this aim include cache line misses that are filled one word at a time through a pre–fetch buffer, integer divide that is interruptible through the use of a divide step instruction, fast multiply and a 1 word write buffer to limit pending bus transactions.

To minimize the time required to start executing the interrupt service routine the processor switches to a new register window when an interrupt is detected. This feature allows the service routine to be executed without first requiring that the current registers be saved. The user can also elect to lock the service routine into the cache. This makes the routine available for immediate access. The on–chip data cache can also serve the service routine as a fast local stack for minimum delay in accessing routine variables.

The MB86930 provides for up to 15 different interrupt levels and direct support for 15 separate interrupt sources. The highest interrupt level is non–maskable.

CACHE

The MB86930 has separate on–chip data and instruction caches. This allows the user to build a high performance system without incurring the cost of requiring fast external memory and the associated control logic.

The data and instruction caches are each organized as two banks of sixty–four 16–byte lines (see Figure 4). The lines are organized as two–way set–associative for good performance even when cache locking is in effect. Lines are divided into four sub–blocks each four bytes wide. On a cache miss, the cache is updated in sub–block increments for efficient re–fill of typical code segments and to avoid interrupt latency incurred by long cache line replacements. An instruction pre–fetch buffer fetches the next sequential instruction anticipating that it will be needed to fill the next instruction cache miss.

The caches can be used in either normal or one of two lock modes. In normal mode, the caches use an LRU (least recently used) algorithm to replace one of the two appropriate entries. Alternately, the two locking modes allow the entire cache or just selected entries to be locked. The lock modes allow time critical routines to be locked in cache.

Global locking allows the entire content of either the instruction or data cache to be frozen. Two control bits in the cache control register enable or disable locking for either cache. With the entire cache locked, no valid entry can be replaced. To insure best possible performance however, invalid entries will be updated if they are accessed. This is done automatically and incurs no time penalty.

Local cache locking makes it possible to dynamically lock selected instructions or data entries into the appropriate cache. This feature gives the flexibility, for example, to assure deterministic response for certain critical interrupt routines by locking the routine's code into the cache. Entries can also be locked where it is desirable to give performance priority to certain often used routines which might otherwise be removed from cache. The 2–way set–associativity allows the cache to perform effectively even with some locked entries.

In local lock mode, each entry can either be locked individually by software or automatically with hardware assist. For individual locking, software writes the lock bit in the appropriate cache tag line. For automatic locking, a bit in each cache control register enables or disables the feature. The enable bit is set at the beginning of a routine for which the entries are to be locked. This causes the location of any cache access occurring while the bit is enabled to be locked into the cache. In addition to requiring just one initial cycle to enable, automatic entry locking incurs no overhead while in effect.

In unlocked operation, the data cache uses a write–through update policy and allocates a cache entry only on a load. Writes are buffered so that the processor can continue executing while data is written back to memory. In contrast, writes to locked data cache locations are not written through to main memory. Besides reducing external bus activity, this design supports configuring a portion of data cache as on–chip RAM which does not map to external memory.

The data and instruction caches are designed to be accessed independently over separate data and instruction buses to allow data to be loaded from and stored to cache at peak rates of 1 CPI.

BUS INTERFACE

The Bus Interface Unit (BIU) is designed to simplify the interface between the MB86930 and the rest of the system. Separate address and data buses make it easy to build fast systems. At the same time, on–chip circuitry allows these systems to be built with a minimum of external hardware.

The bus interface supports fully programmable wait–state generation, address decoding with chip select outputs, same page detection to support page–mode DRAM, and an auto–reload timer to support a refresh counter.

CLOCK GENERATOR

The on–chip clock generator provides a means to directly connect the MB86930 to either a crystal oscillator or an external clock source. For either case, the external frequency is the same as the chip operating frequency.

A clock output signal provides the system with a reference by which external timing can be synchronized when not using an external clock source. The skew between the internal clock and an external input clock source is minimized by the inclusion of an on–chip phase lock loop circuit.

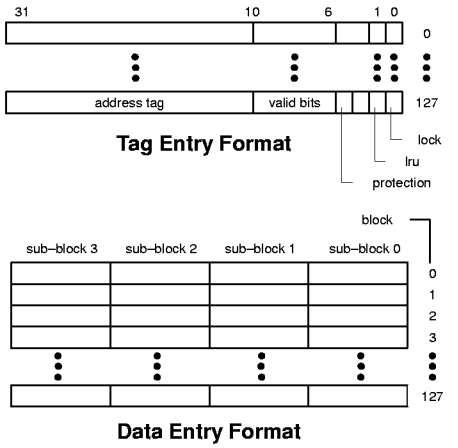
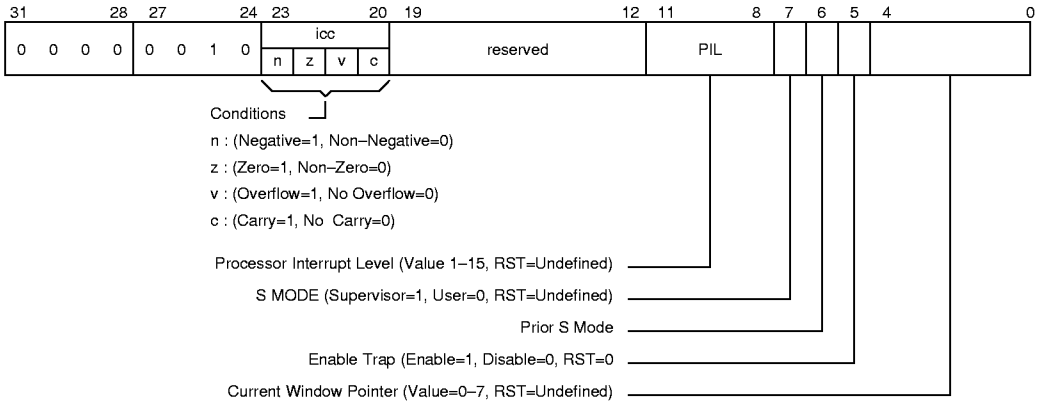


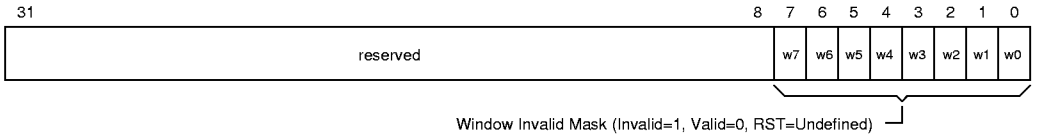
Figure 3. Instruction and Data Cache Organization

TABLE 1. MB86930 Control and Status registers (All registers are read/write)

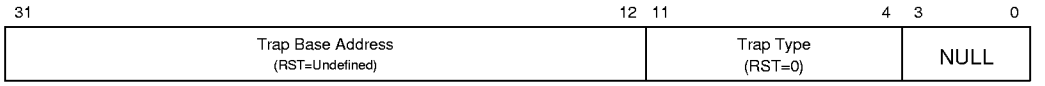
Processor State Register | **PSR**



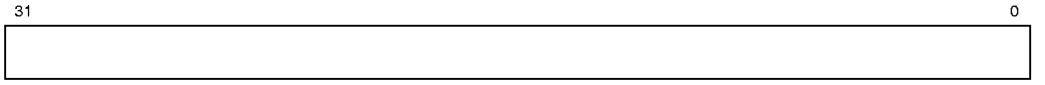
Window Invalid Mask | **WIM**



Trap Base Register | **TBR**



Y Register | **Y**



Ancillary State Register 17 | **ASR 17**

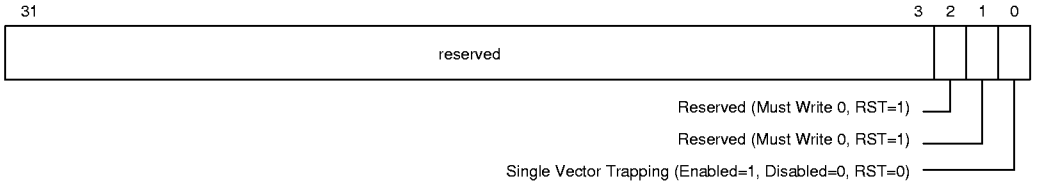
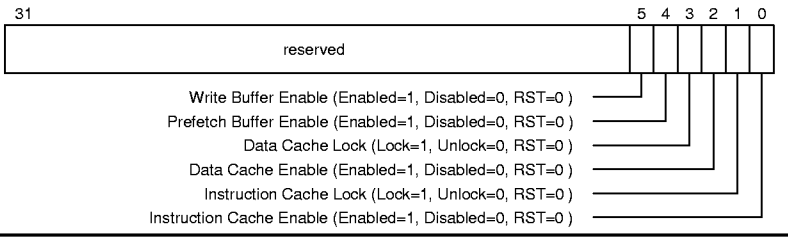
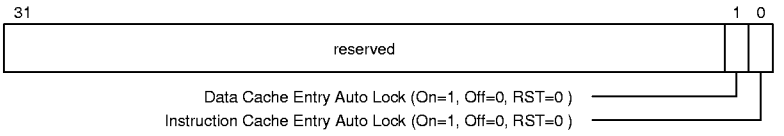


TABLE 2. MB86930 Memory Mapped Control Registers (All registers are read/write)

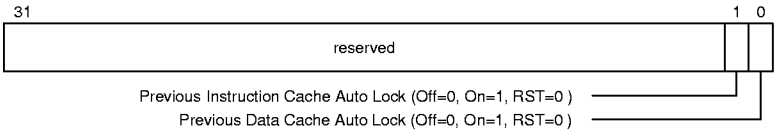
Cache/BIU Control	
ASI	ADDRESS
0x 1	0x 0000 0000



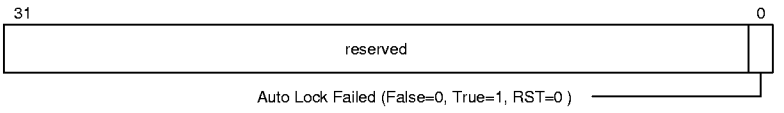
Lock Control	
ASI	ADDRESS
0x 1	0x 0000 0004



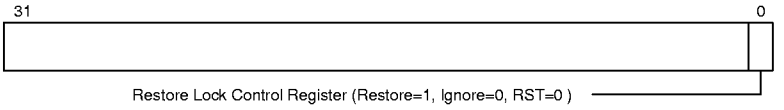
Lock Control Save	
ASI	ADDRESS
0x 1	0x 0000 0008



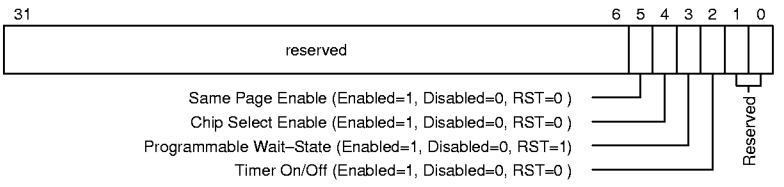
Cache Status	
ASI	ADDRESS
0x 1	0x 0000 000C



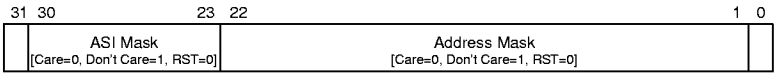
Restore Lock Control	
ASI	ADDRESS
0x 1	0x 0000 0010



System Support Control	
ASI	ADDRESS
0x 1	0x 0000 0080

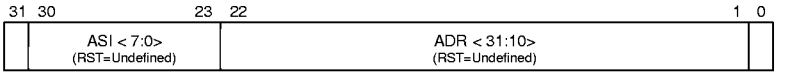


Same Page Mask	
ASI	ADDRESS
0x 1	0x 0000 0120



Address Range[1]

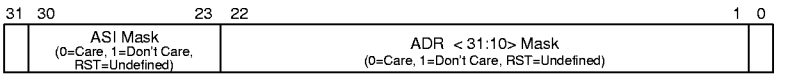
ASI	ADDRESS
0x 1	CS1 0x 0000 0124 CS2 0x 0000 0128 CS3 0x 0000 012C CS4 0x 0000 0130 CS5 0x 0000 0134



NOTE: CS0 is hardwired to ASI=0x9 ADR < 31:10> = < 0..0>

Address Mask

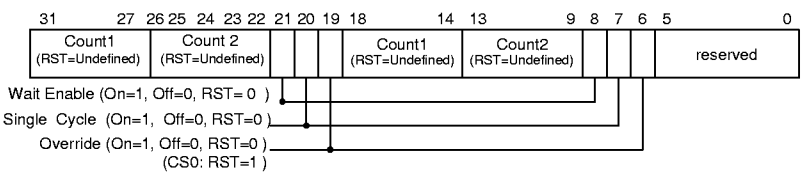
ASI	ADDRESS
0x 1	CS0 0x 0000 0140 CS1 0x 0000 0144 CS2 0x 0000 0148 CS3 0x 0000 014C CS4 0x 0000 0150 CS5 0x 0000 0154



NOTE: CS0 is hardwired to ASI=0x9; At Reset, ADR < 31:15> = 0, ADR < 14:10> = 1

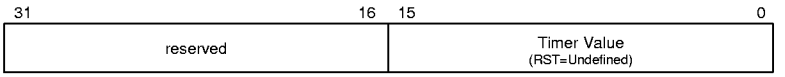
Wait State Specifier

ASI	ADDRESS
0x 1	CS1,CS0 0x 0000 0160 CS3,CS2 0x 0000 0164 CS5,CS4 0x 0000 0168



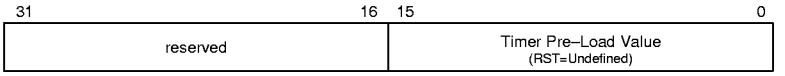
Timer

ASI	ADDRESS
0x 1	0x 0000 0174



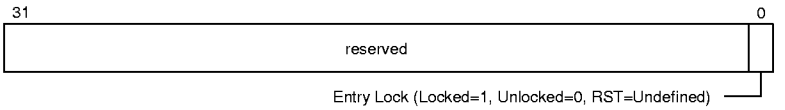
Timer Pre–Load

ASI	ADDRESS
0x 1	0x 0000 0178



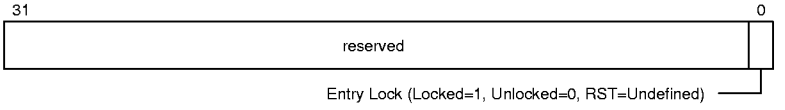
Instruction Tag Lock Bits

ASI	ADDRESS
0x 2	Bank 1 0x 0000 0000 ↓ by 4 0x 0000 0400 Bank 2 0x 8000 0000 ↓ by 4 0x 8000 0400



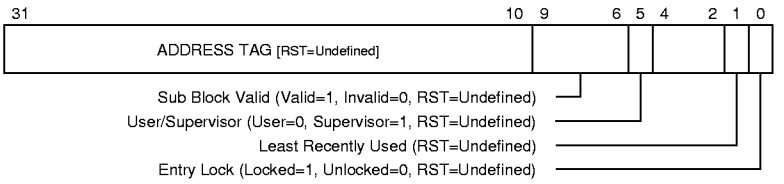
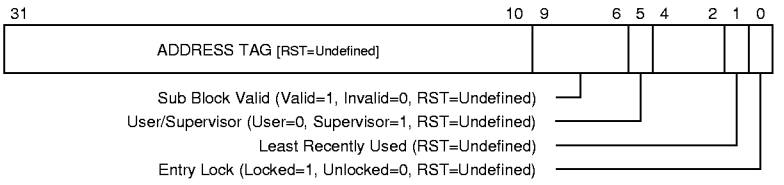
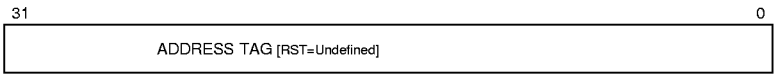
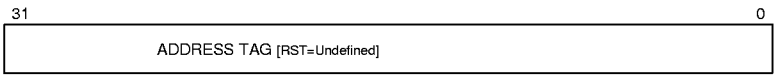
Data Tag Lock Bits

ASI	ADDRESS
0x 3	Bank 1 0x 0000 0000 ↓ by 4 0x 0000 0400 Bank 2 0x 8000 0000 ↓ by 4 0x 8000 0400



1. This register is Write Only

TABLE 2. MB86930 Memory Mapped Control Registers (Continued)

Instruction Cache Tag		
ASI	**ADDRESS**	
0x C	Bank 1 0x 0000 0000 ↓ by 4 0x 0000 0400 Bank 2 0x 8000 0000 ↓ by 4 0x 8000 0400	
Data Cache Tag		
ASI	**ADDRESS**	
0x E	Bank 1 0x 0000 0000 ↓ by 4 0x 0000 0400 Bank 2 0x 8000 0000 ↓ by 4 0x 8000 0400	
Instruction Cache Data		
ASI	**ADDRESS**	
0x D	Bank 1 0x 0000 0000 ↓ by 1 word 0x 0000 0400 Bank 2 0x 8000 0000 ↓ by 1 word 0x 8000 0400	
Data Cache Data		
ASI	**ADDRESS**	
0x F	Bank 1 0x 0000 0000 ↓ by 1 word 0x 0000 0400 Bank 2 0x 8000 0000 ↓ by 1 word 0x 8000 0400	

BUS OPERATION

The Bus Interface Unit (BIU) has the logic which allows the MB86930 to interface with the system. The system interface is made up of the address and data buses, the interrupt request bus and various control signals. The BIU is either handling requests for external memory operations, arbitrating for bus access, or idle.

Operation of the BIU

The BIU receives requests for external memory operations from the Cache Control Logic (CCL). In the case of reads from external memory, it performs the read operation and returns the data to the Cache and IU. A parallel path is used to make the data available to the IU in the same cycle that it is written to the cache.

In the case of a write to external memory, the BIU makes use of a write buffer which can hold a one word write transaction. When the BIU receives a request for a write transaction it stores the write data and address in the write buffer allowing the IU to continue operating out of on–chip cache and/or its register file. The BIU then proceeds to complete the write to external memory. In most cases the write buffer will hide external memory latency from the IU. The exceptions are in cases where the write buffer is still filled from a previous transaction or if the subsequent IU cycle results in an instruction cache miss. In these cases, IU execution is held until the write buffer is emptied.

The BIU includes a one stage prefetch buffer for instruction fetches. This buffer is used to fetch the next sequential instruction after an instruction cache miss. The instruction is prefetched only if the BIU does not have a request for a bus transaction from the IU nor is any external device requesting use of the bus. The prefetch buffer operation is suspended if the buffer is full. This occurs if the prefetched instruction is a hit in the instruction cache. The buffer restarts after another instruction cache miss. If an exception occurs during an instruction prefetch, the exception is not sent to the IU unless the instruction is actually requested by the IU. The prefetch buffer operates only when the instruction cache is on.

In any cycle the BIU can receive a request for accesses to either or both instruction and/or data memory. If it receives a request for both in the same cycle, it completes the data memory transaction first.

Exception Handling

The external memory system can indicate an exception during a memory operation. The BIU signals the appropriate data or instruction exception to the IU which will trap accordingly.

As mentioned above, the IU can continue operation after putting the data and address for a store in the write buffer. If an exception is detected while completing this buffered write, then the BIU indicates a data access exception to the IU.

Any system which needs to recover from this error should store the address and data of such write transactions in hardware. If the system can generate both read and write exceptions, then the system must also provide a status bit which indicates whether the exception was generated on a read or on a write transaction. With access to this information the data access exception service routine can determine the cause of the exception and recover accordingly.

Bus Cycles

Timings 1 through 9 illustrate representative combinations of bus cycles.

Load

Whenever an instruction fetch or a load from data memory has a miss in the cache, the BIU performs a read from external memory.

A read transaction begins with the BIU asserting –AS, to indicate a new bus transaction. The –AS signal is de–asserted after one cycle. At the same time the ADR < 31:2> and ASI < 7:0> bits are driven with the location to be read. The BIU drives the RD/–WR signal high to indicate a read transaction.

The external memory system responds with the read data on pins D < 31:0 >. It also asserts the –READY signal when the data is ready. For slow memory, the –READY signal can be delayed until data is valid.

A load double operation is treated as back–to–back reads.

Load with Exception

If the external memory system sees a memory exception it can terminate the current memory transaction by asserting the –MEXC and –READY signals. The data on the data bus is ignored by the MB86930.

Store

A write transaction begins with the BIU asserting –AS, to indicate a new bus transaction. The –AS signal is de–asserted after one phase. At the same time the ADR < 31:2> and ASI < 7:0> pins are driven with the location to be written while the D < 31:0> pins has corresponding write data. The –BE0–3 pins indicate byte, half–word or word transaction width. The BIU drives the RD/–WR signal low to indicate a write transaction.

The external memory system responds by asserting the –READY signal when it has stored the data.

A store double operation is treated as back–to–back writes.

Store with Exception

If an access exception occurs on a write, the external memory system can terminate the current memory transaction by asserting the –MEXC and –READY signals. The external memory system is expected to ignore the data on the data bus in this situation.

Atomic Load Store

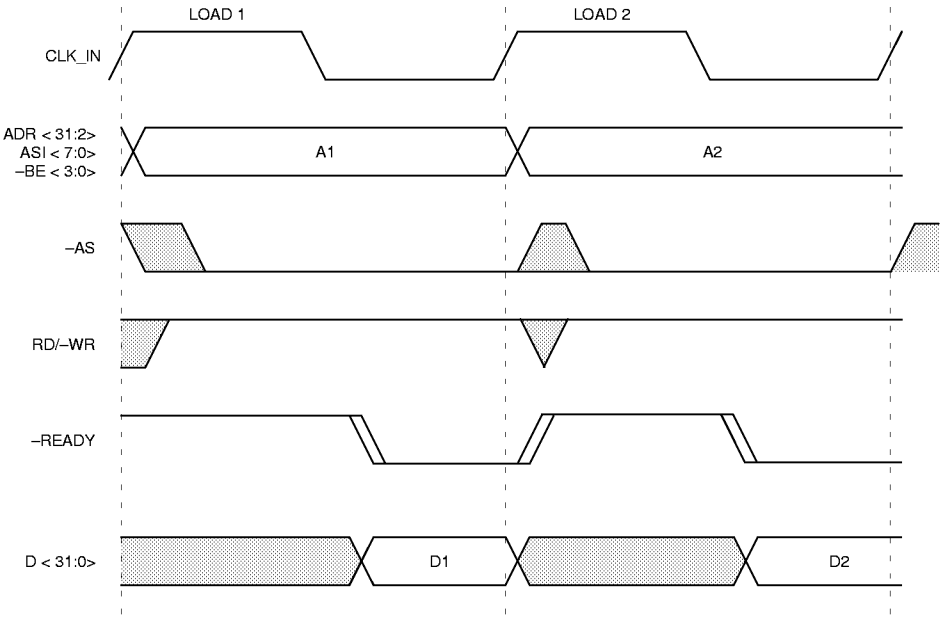
An atomic load store executes as a load followed by a store with no operation allowed in between. The –LOCK signal is asserted to indicate that the bus is being used for more than one external memory operation.

There is one cycle between the termination of the read and the beginning of the write to provide time for the switching of the data bus drivers.

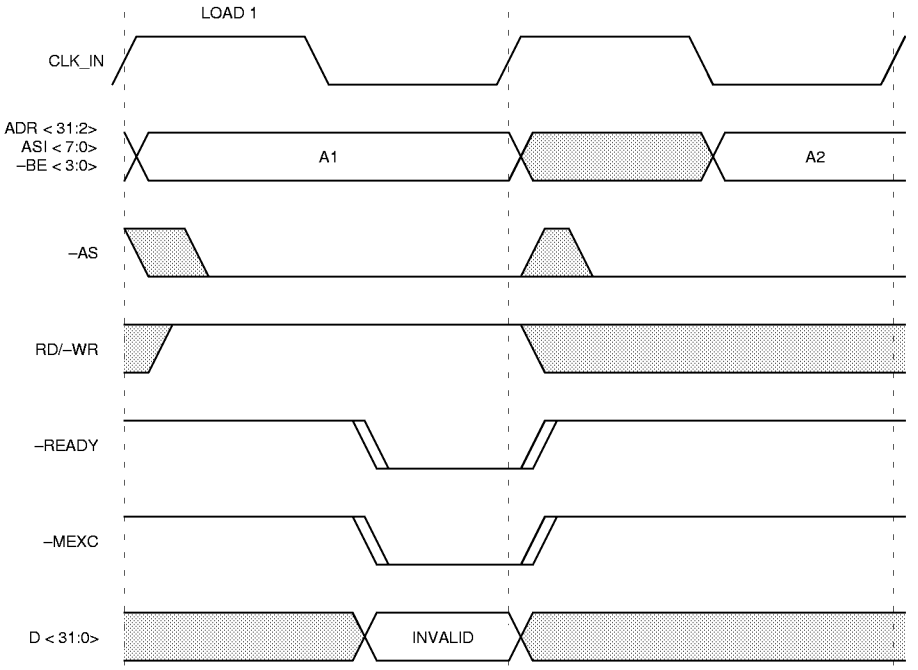
External Bus Request and Grant

Any external device can request ownership of the bus by asserting the –BREQ signal. The BIU asserts the –BGRNT signal to indicate that it is relinquishing control of the bus and also three–states all of its bus drivers. In the following cycle, the external device can complete its transaction. On completion of its transaction the external device de–asserts the –BREQ signal. The BIU responds by de–asserting the –BGRNT signal in the following cycle.

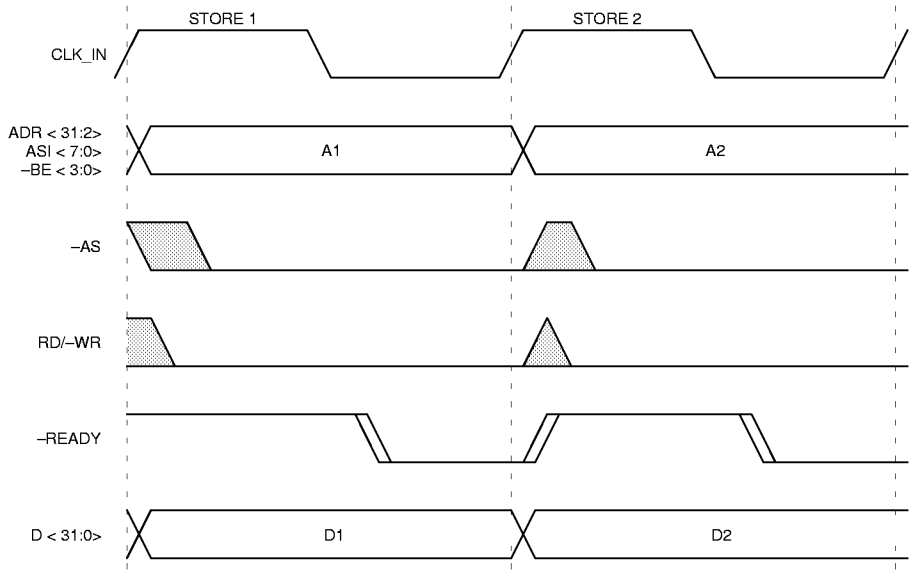
The MB86930 is the default owner of the bus.



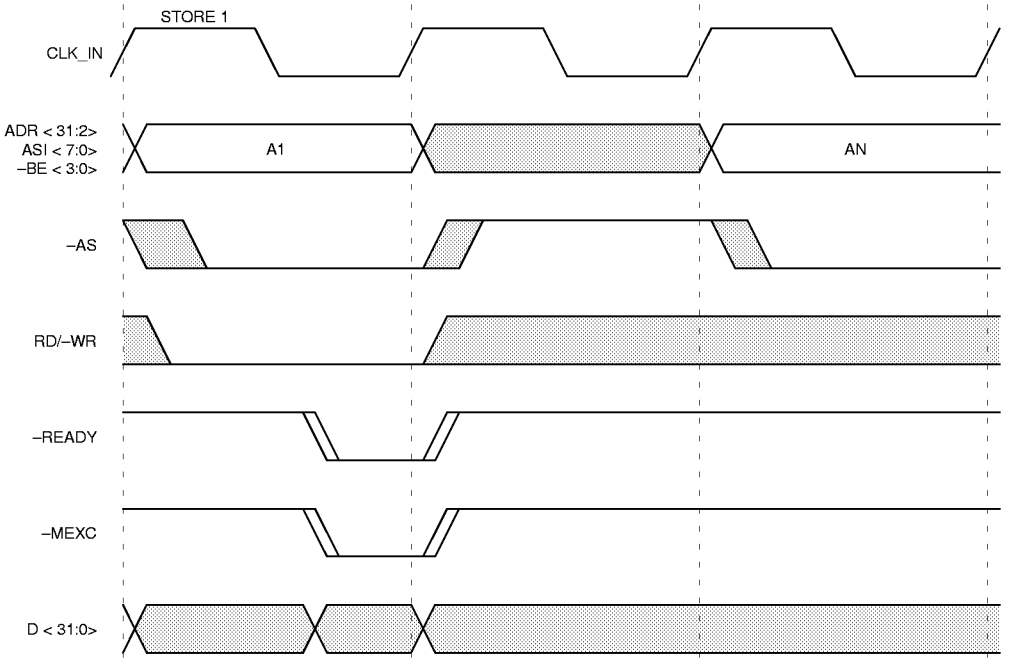
Timing 1. Typical Back-to-Back Loads (Same as Load Double)



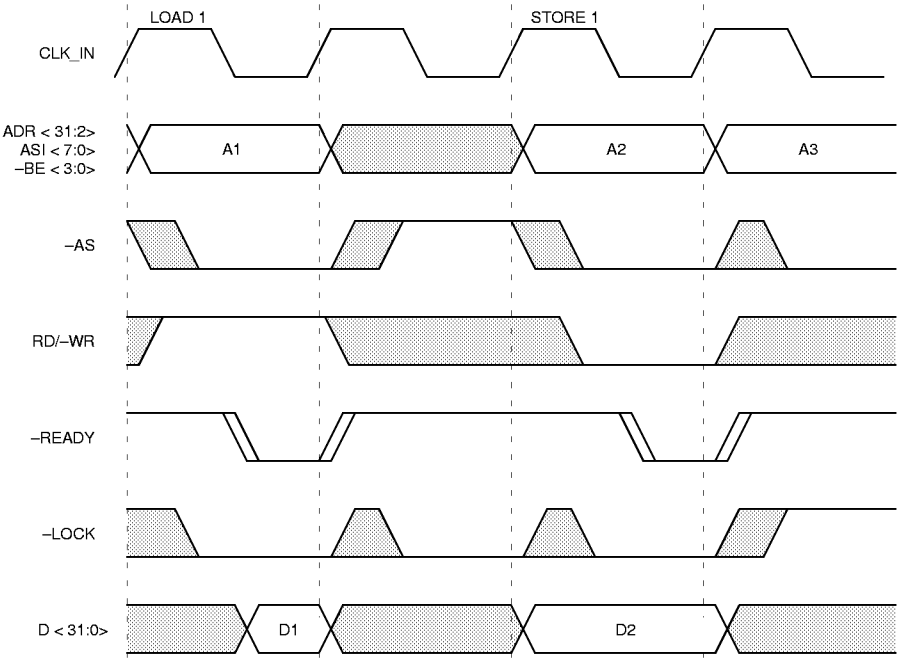
Timing 2. Load with Exception



Timing 3. Typical Back–to–Back Stores (Same as Store Double)

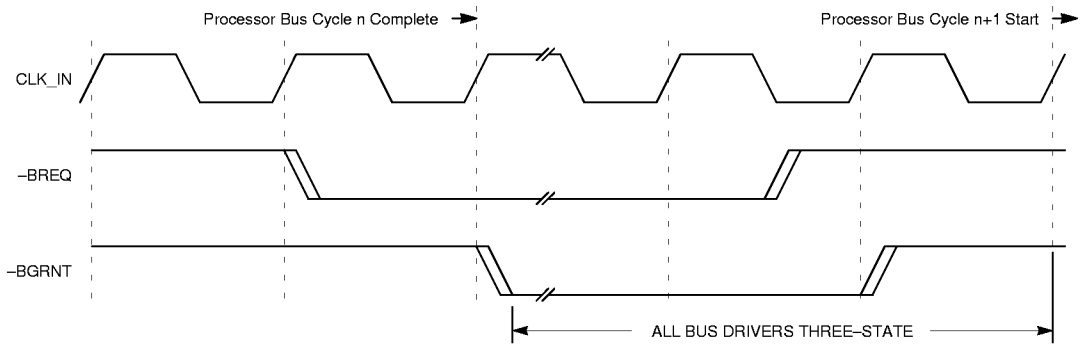


Timing 4. Store with Exception



Note: A load followed by a store requires an intervening clock cycle on the bus while a store followed by a load can occur in consecutive clock cycles.

Timing 5. Atomic Operation



Timing 6. Bus Request and Grant Cycle

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Conditions	Min.	Max.	Units
V_{CC}	Supply voltage		–0.3	6	V
V_I	Input voltage		–0.3	V_{CC} + 0.3	V
T_J	Operating junction temperature			125	°C

Notes: 1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operation section of this specification is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods may affect device reliability.

Recommended Connections:

1. Power and ground connections must be made to multiple V_{CC} and V_{SS} pins. Every MB86930 based circuit board should include power (V_{CC}) and ground (V_{SS}) planes for power distribution. Every V_{CC} pin must be connected to the power plane, and every V_{SS} pin must be connected to the ground plane. Pins identified as "N.C." must not be connected in the system.
2. Liberal decoupling capacitance should be placed near the MB86930. The processor can cause transient power surges when its numerous output buffers transition, particularly when connected to large capacitive loads.
3. Low inductance capacitors and interconnections are recommended for best high frequency electrical performance. Inductance can be reduced by shortening the board traces between the processor and decoupling capacitors as much as possible. Capacitors specifically designed for PGA and QFP packages will offer the lowest possible inductance.
4. For reliable operation, alternate bus masters must drive any pins that are three–stated by the MB86930 when it has granted the bus, in particular –LOCK, ADR < 31:2 >, ASI < 7:0 >, –BE0–3, D < 31:0 >, –AS, and RD/–WR must be driven by alternate bus masters. These pins are normally driven by the processor during active and idle bus states and don't require external pullups. N.C. pins must always remain unconnected.

PACKAGE THERMAL CHARACTERISTICS

Symbol	Parameter	Package	Value			Units
$\varnothing_{JC}$	Thermal resistance junction to case	208 Plastic QFP 208 Ceramic QFP 208 Ceramic QFP w/ Heat Sink 179 Ceramic PGA	5.0 1.8 1.6 8.0			°C/W
			0 m/s	**1 m/s**	**3 m/s**	
$\varnothing_{JA}$	Thermal resistance junction to ambient	208 Plastic QFP 208 Ceramic QFP 208 Ceramic QFP w/ Heat Sink 179 Ceramic PGA	25 19 16 25	22 15 12 19	19 13 8 13	°C/W

Note: All numbers for package thermal characteristics assume multilayer PCB, except for the numbers for PGA package, which assume a single layer PCB.

DC SPECIFICATIONS [3] V_{CC} = 5V ± 5%

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IL}	Input low voltage		0	–	0.8	V
V_{IH}	Input high voltage (All pins except XTAL1)		2.0	–	V_{CC}	V
	Input high voltage (Pin XTAL1)		2.8	–	V_{CC}	V
V_{OL}	Output low voltage	I_{OL} = 3.2mA	0	–	0.45	V
V_{OH}	Output high voltage	I_{OH} = –0.4mA	2.4	–	V_{CC}	V
I_{LI}	Input leakage current	V_{IN} = 0 or V_{CC}	–10	–	10	µA
I_{LZ}	3–state output leakage current	V_{OUT} = 0 or V_{CC}	–10	–	10	µA
I_{CC}	Operating power supply current. Use Icc (typ) to calculate maximum case and ambient temperature allowed. Ambient temperature of die is 125°C. For example, allowed ambient temperature = 125°C.– (I_{CC}) • (5.25V) • $\varnothing_{JA}$	20 MHz	–	330	440	mA
		30 MHz	–	410	470	mA
		40 MHz	–	460	570	mA
C_{PIN}	Pin capacitance (All pins except XTAL2)	V_{CC} = V_I = 0 f = 1 MHz	–	–	13	pF
	Pin capacitance (Pin XTAL2)		–	–	16	pF

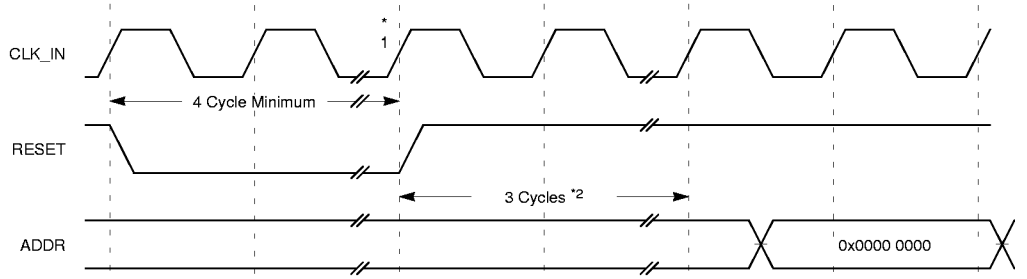
AC CHARACTERISTICS[1,2,4] V_{CC} = 5V ± 5%, T_A 0–70°C

Symbol	Parameter Description		20 MHz		30 MHz		40 MHz		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t1	CLKIN period		50	100	33	100	25	100	ns
t2	CLKIN high Time		10		8		6		ns
t3	CLKIN low time		14		12		10		ns
t4	CLKIN rise time			4		3		2	ns
t5	CLKIN fall time			4		3		2	ns
t6	CLKIN to CLKOUT delay [7]		0	8	0	8	0	7	ns
t7	CLKIN to CLKOUT2 delay [7]		25	33	17	25	13	20	ns
t8	CLKOUT1, CLKOUT2 high time [7]		0.35xPeriod		0.3xPeriod		0.25xPeriod		ns
t9	CLKOUT1, CLKOUT2 low time[7]		0.4xPeriod		0.4xPeriod		0.4xPeriod		ns
t10	CLKOUT1, CLKOUT2 fall time[7]			3		3		3	ns
t11	CLKOUT1, CLKOUT2 rise time[7]			4		4		3	ns
t12	D < 31:0>	Output valid delay		21		19		16	ns
		Output hold	2		2		2		
	ADR < 31:2>	Output valid delay		24		23		20	ns
		Output hold	2		2		2		
	–BE0–3	Output valid delay		19		18		16	ns
		Output hold	2		2		2		
	ASI < 7:0>	Output valid delay		22		20		17	ns
		Output hold	2		2		2		
t13	–CS	Output valid delay		24		23		20	ns
		Output hold	2		2		2		
t14	–SAME_PAGE	Output valid delay		23		22		20	ns
		Output hold	2		2		2		

AC CHARACTERISTICS[1,2,4] V_{CC} = 5V ± 5%, T_A 0–70°C (Continued)

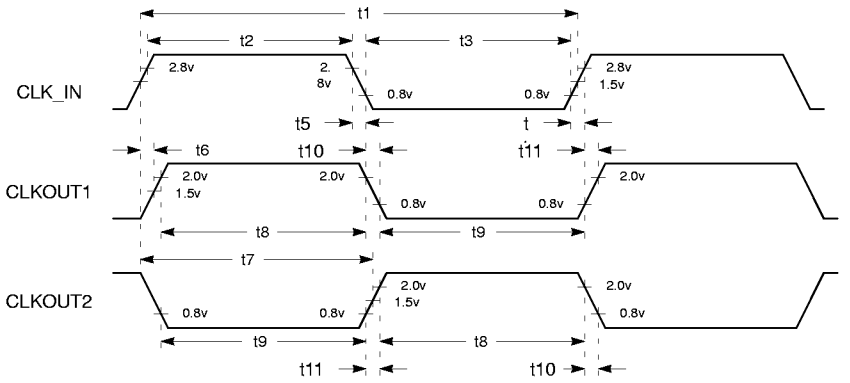
Symbol	Parameter Description		20 MHz		30 MHz		40 MHz		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t15	RD/–WR	Output valid delay		18		17		15	ns
		Output hold	2		2		2		
t16	–LOCK	Output valid delay		19		18		16	ns
		Output hold	2		2		2		
t17	–AS	Output valid delay		21		20		18	ns
		Output hold	2		2		2		
t18	–TIMER_OVF	Output valid delay		20		19		18	ns
		Output hold	2		2		2		
t19	–BGRNT	Output valid delay		20		18		15	ns
		Output hold	2		2		2		
t20	–MEXC input setup time		14		12		12		ns
t21	–READY input setup time		15		14		12		ns
t22	D < 31:0> input setup time		11		10		9		ns
t23	–BREQ input setup time		8		7		6		ns
t24	IRL < 3:0> input setup time [6]		6		6		6		ns
t25	–MEXC input hold time		2		2		1		ns
t26	–READY input hold time		2		2		1		ns
t27	D < 31:0> input hold time		3		3		2		ns
t28	–BREQ input hold time		3		3		2		ns
t29	IRL < 3:0> input hold time [6]		5		5		5		ns

1. Parameters are valid over specified temperature range and supply voltage range unless otherwise noted.
2. All voltage measurements are referenced to ground. All time measurements are referenced at input and output levels of 1.5V. For testing, all inputs swing between 0.4V and 2.4V (Except XTAL1 which swings from 0.4V to 3.0V). Input rise and fall times are 2ns or less.
3. Not more than one output may be shorted at a time for a maximum duration of one second.
4. Timing specifications apply to frequency of operation listed at top of column.
5. All output timings are based on a 50pF load.
6. The IRL input setup and hold times are measured with respect to the midpoint of the input clock cycle.
7. These specs will be improved in the future.
8. Data bus output driver control is same as for RD/–WR so timing is similar.



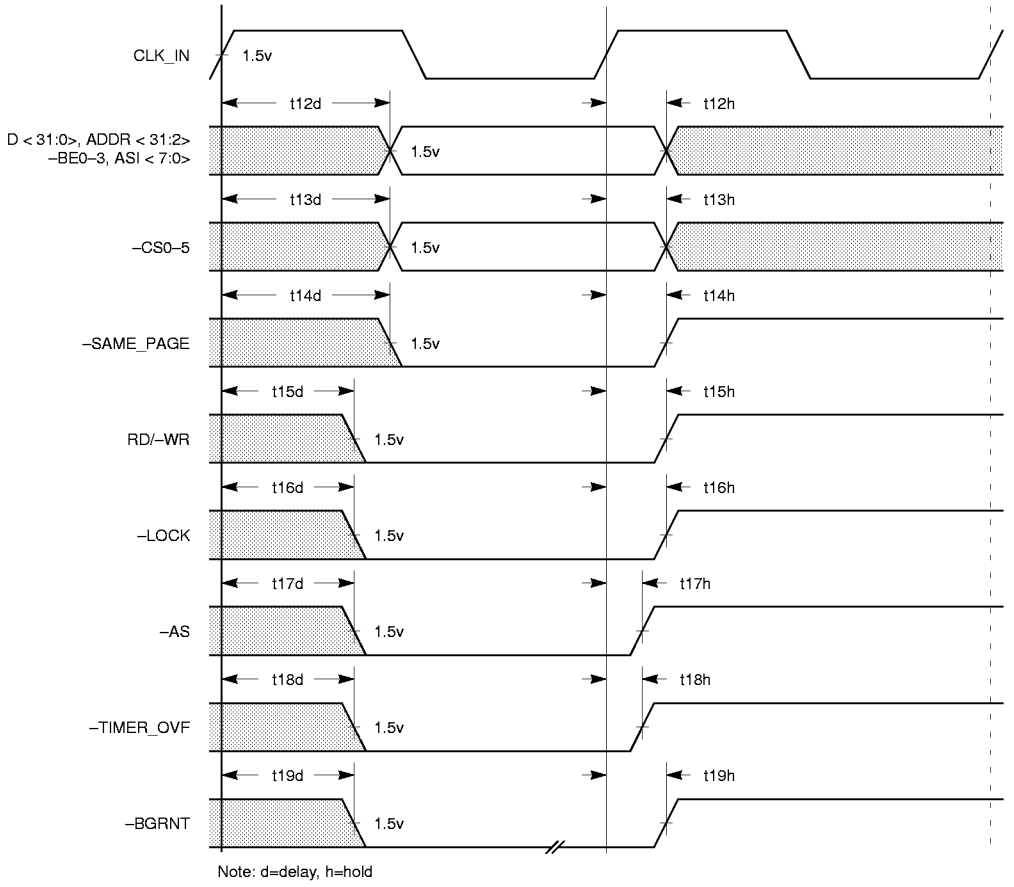
*1. CLK_IN must be stable for at least 100µs before RESET is de–asserted.
*2. When RESET hold time (3ns) is met.

Timing 7. Reset Timing

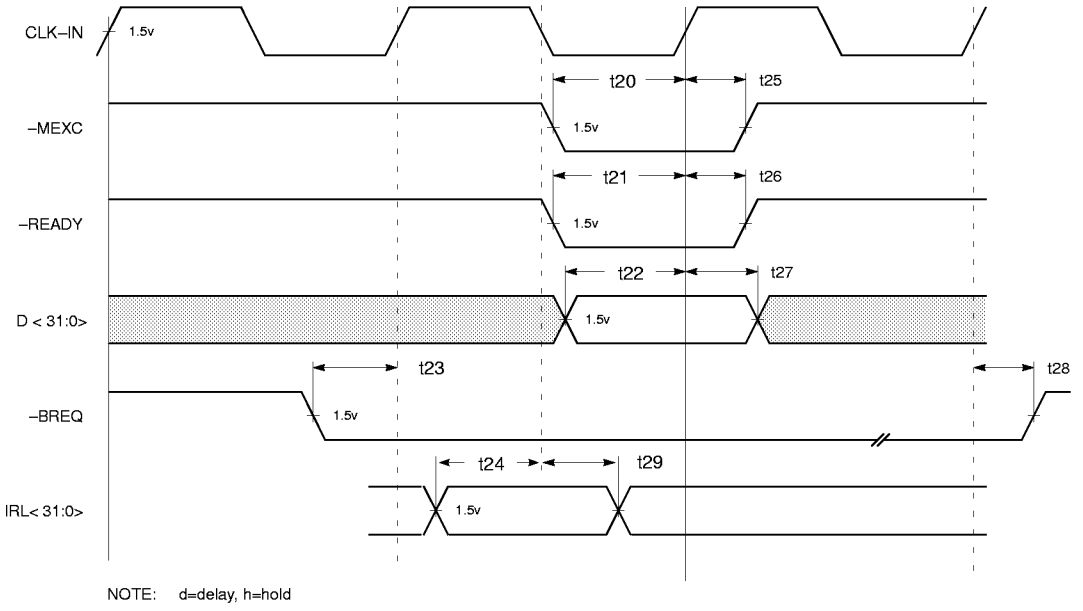


Note: CLKOUT1 and CLKOUT2 are derived from non–overlapping internal clocks, however, the relative timing of these signals is not tested.

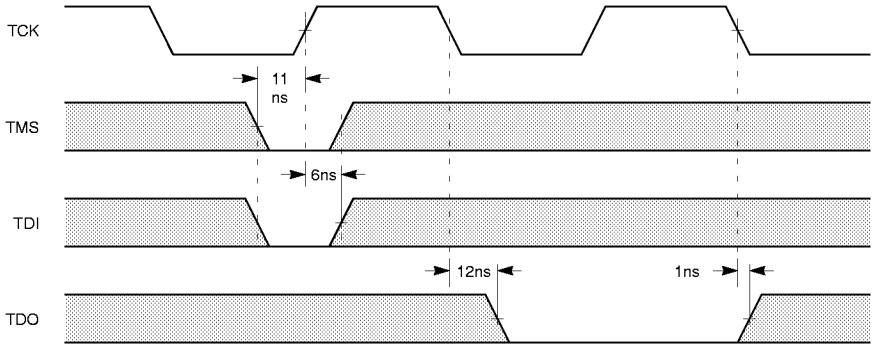
Timing 8. Clock Timing



Timing 9. I/O Output Timing

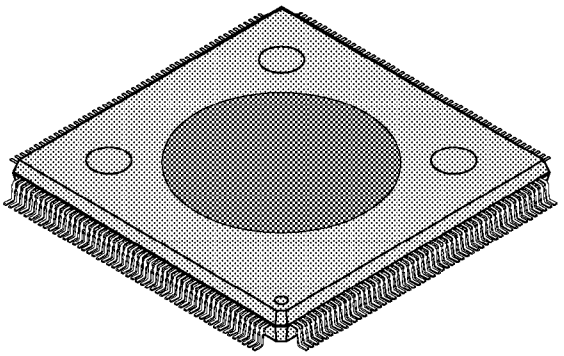


Timing 10. I/O Output Timing



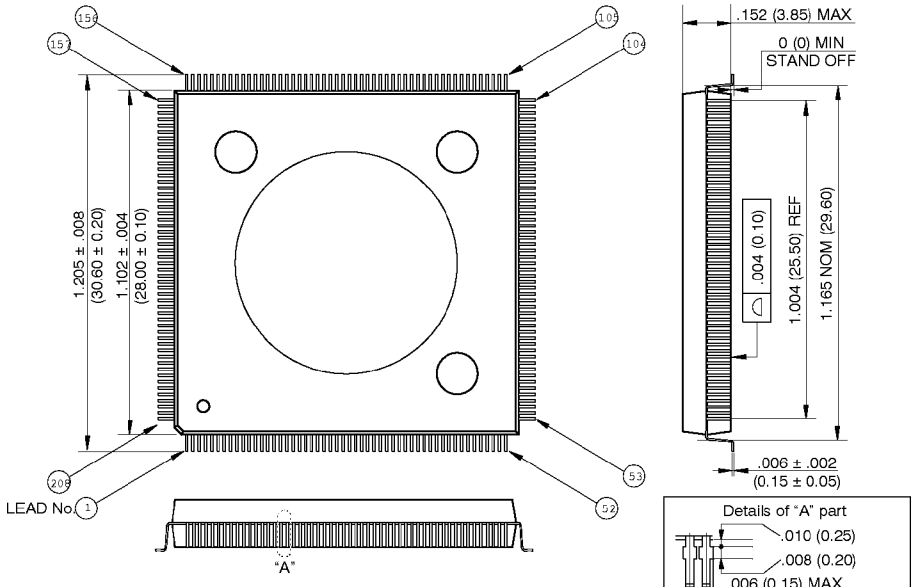
Timing 11. JTAG Timing

208-LEAD FLAT PACKAGE (SQFP)

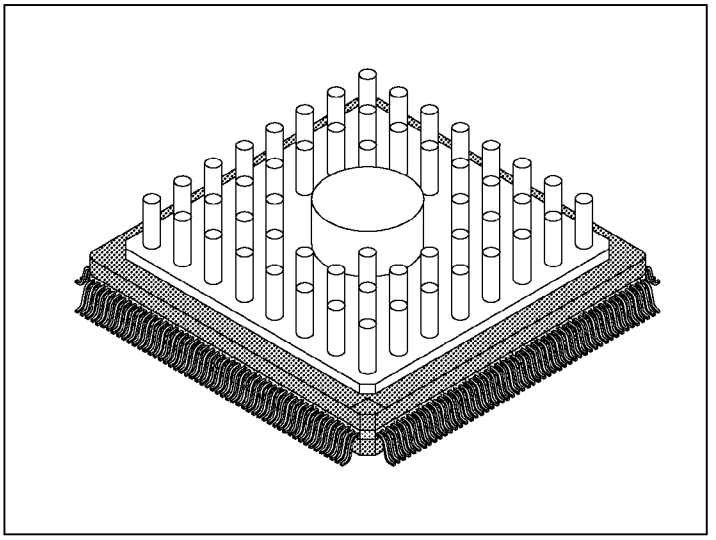


Ordering Information: MB86930-20PF-G

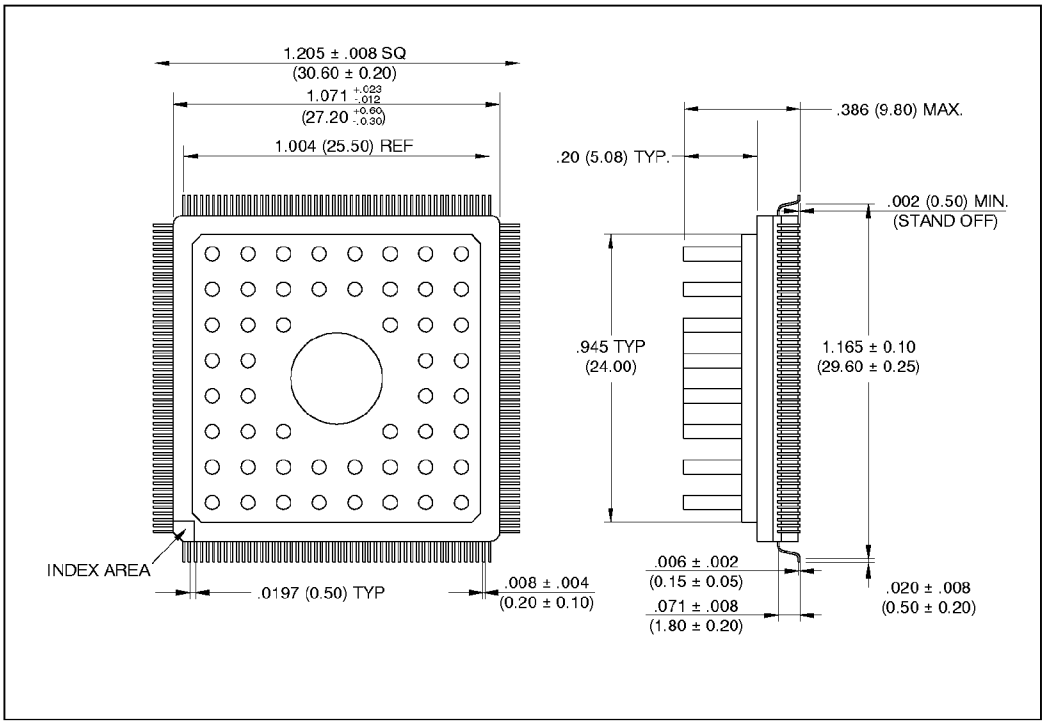
208-LEAD FLAT PACKAGE (SQFP)



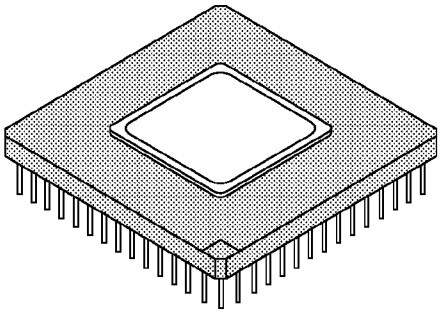
Dimensions in inches (millimeters)



Ordering Info : MB86930-30ZF-G (w/o heatsink)
: MB86930-40ZF-G (w/ heatsink)

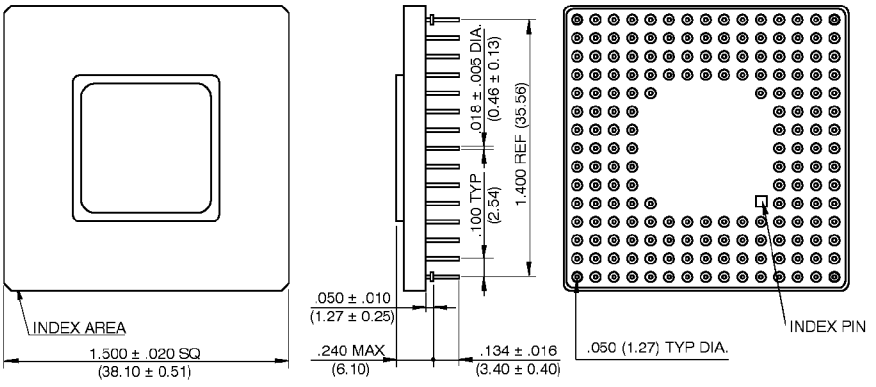


179-LEAD CERAMIC (METAL SEAL) PIN GRID ARRAY PACKAGE



Ordering Information: MB86930-40CR-G

179-LEAD CERAMIC (METAL SEAL) PIN GRID ARRAY PACKAGE
(Case No.: PGA-179C-A03)



Dimensions in inches (millimeters)