MB86936

930 SERIES 32–BIT RISC EMBEDDED PROCESSOR

FUJITSU

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FEATURES

- 50 MHz version with clock doubling
- SPARC* high performance RISC architecture
- High Performance SPARC FPU, ANSI/IEEE 754 compatible
- 8 window, 136 word register file
- 16 address spaces, 256Mbyte each
- Harvard-style separate instruction and data buses on-chip
- 4 Kbytes 2-way set associative instruction cache
- 2 Kbytes 2-way set associative data cache
- Flexible locking mechanism for data and instruction cache entries
- Option to force non-cached operation based on chip selects on Non–Cache Pin
- Four deep buffered writes and one deep instruction pre-fetching
- Core can run at double the frequency of the Bus Interface Unit.
- Bus interface support for 8, 16 or 32-bit memories read/write
- Support for burst mode cache fills
- DRAM Controller with fast page-mode DRAM support
- 3 channel DMA controller, with one channel reserved for Video Interface if enabled
- Video interface to printer engine/rasterizer, scanner
- Interrupt Controller with fast interrupt response time, with programmable priority
- Two 24-bit timers with 16-bit counter and 8-bit prescaler, with 3 modes of operation each
- Glueless interface to ROM, EEPROM
- Parity generation and checking
- Programmable address decoder and wait-state generator
- On-chip clock generator circuit
- JTAG test interface
- Emulator support hardware
- Single vector trapping
- Power down modes, with global or selective power down
- 0.5 micron gate, 3 level metal CMOS technology, 3.3V internal and 5V I/O

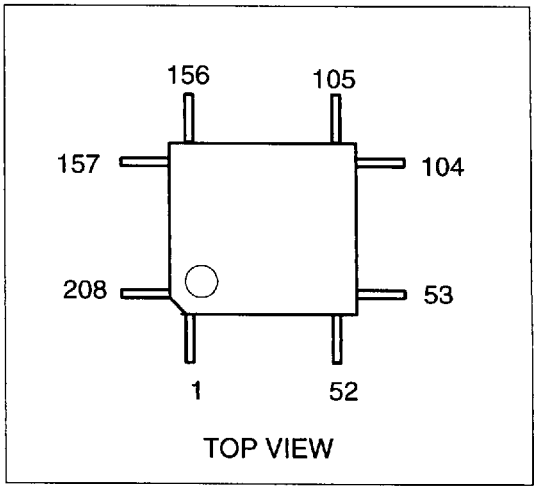
GENERAL DISCUSSION

The MB86936 is the next of the MB8693X series of RISC processors which offers high performance and high integration for a wide range of embedded applications. The processor is based on the SPARC architecture and is upward code compatible with previous implementations. At 50 MHz, the processor executes with 50 MIPS peak.

The FPU implemented on the MB86936 is compatible with ANSI/IEEE-754-1985. It is also fully compatible with Ver. 8 SPARC FPU.

The MB86936 is a superset of MB86935. Also the MB86936 is pin compatible with MB86935.

PIN CONFIGURATION



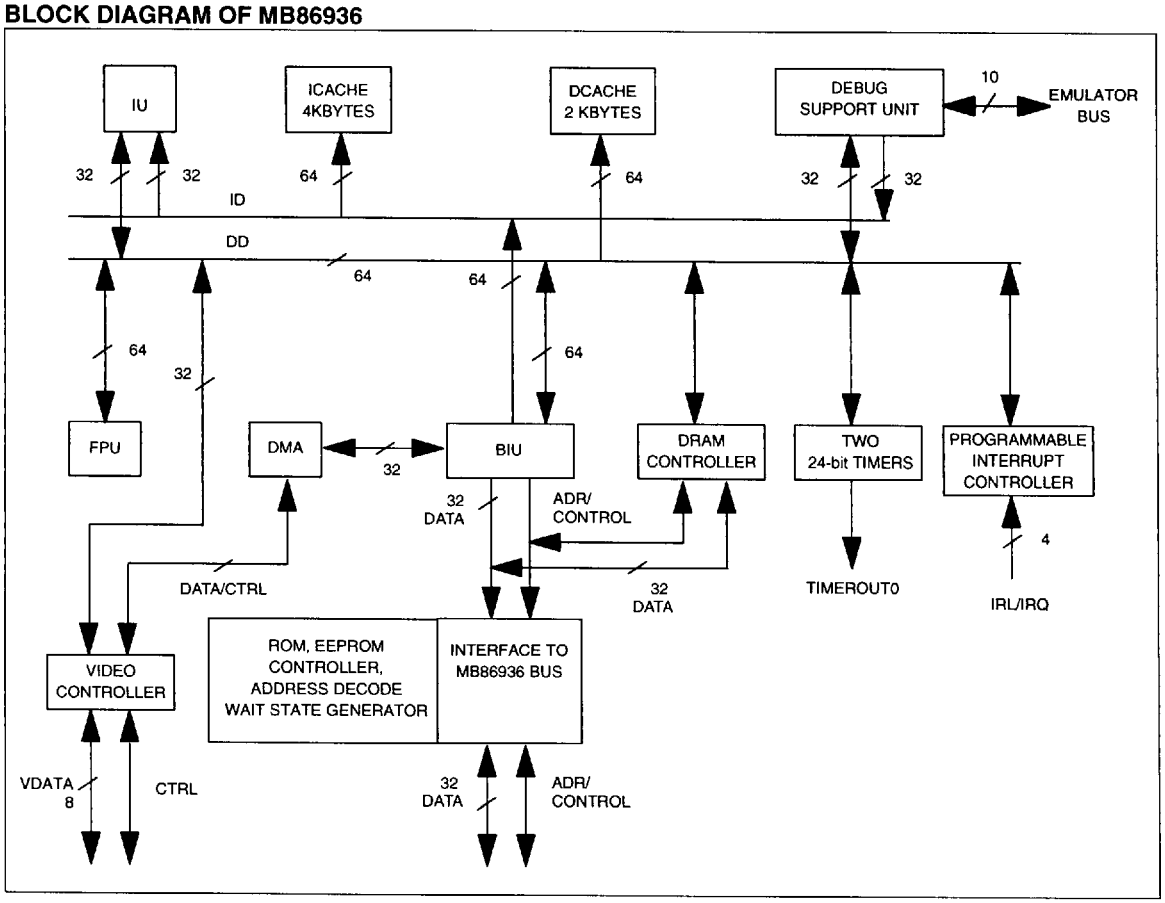
PRELIMINARY

On-chip data and instruction caches are included to help decouple the processor from external memory latency. Separate on-chip instruction and data paths provide a high bandwidth interface between the IU and caches. An on-chip 3-channel DMA controller makes use of the processor bus even while the integer unit or floating point unit are executing out of cache. Included to maximize the performance of the system with minimum glue logic are: chip select outputs, programmable wait state generation, built-in support for connection to page-mode DRAM, page-mode EEPROM, and support for 8 and 16-bit memory. See MB86936 block diagram.

Support for debug and diagnostic tools has been included on-chip and allows for direct connection to hardware emulators and improves debug capability when using ROM based monitors.

These features combine to give the MB86936 superior speed, flexibility and efficiency to make it the ideal choice for a wide variety of low cost, high performance embedded systems.

BLOCK DIAGRAM OF MB86936



Pin Assignment - 208-pin SQFP

Pin No.	I/O	Name	Pin No.	I/O	Name	Pin No.	I/O	Name
1	I/O	VDAT<3>	48		EMU_VDD	95	I/O	D<9>
2	I/O	VDAT<2>	49	I/O	EMU_SD<0>	96	I/O	D<8>
3	I/O	VDAT<1>	50	I/O	EMU_D<3>	97		VDD
4	I/O	VDAT<0>	51	I/O	EMU_D<2>	98	O	–DWE
5		IO_VDD	52	I/O	EMU_D<1>	99		IO_VSS
6		IO_VSS	53	I/O	EMU_D<0>	100		IO_VDD
7		VDD	54		VSS	101	I/O	D<7>
8	I	IRL<3> / IRQ15	55	I/O	–EMU_ENB	102	I/O	D<6>
9	I	IRL<2> / IRQ14	56		VSS	103	O	–BMREQ
10	I	IRL<1> / IRQ13	57		VDD	104	I/O	D<5>
11	I	IRL<0> / IRQ12	58	I/O	D<31>	105	I/O	D<4>
12		VSS	59	I/O	D<30>	106		VSS
13	I	CLK_ECB	60	I/O	D<29>	107		VDD
14	I	TDI	61		IO_VDD	108	I/O	D<3>
15	I	–TRST	62	I/O	D<28>	109	I/O	D<2>
16	I	TCK	63	I/O	D<27>	110	I/O	D<1>
17	I	TMS	64		IO_VSS	111	I/O	D<0>
18		IO_VDD	65	I/O	D<26>	112		VDD
19		IO_VSS	66	I/O	D<25>	113	I	–RESET
20		VSS	67	I/O	D<24>	114	I	–BREQ
21		VDD	68		VSS	115		VSS
22	I	–DREQ2	69		VDD	116	I	–MEXC
23	O	–DACK2	70		VDD	117	I	–READY
24	O	TDO	71		VDD	118		IO_VSS
25	O	–RAS2/-TIMER_OVF	72	I/O	D<23>	119	O	–CAS0
26		IO_VDD	73	I/O	D<22>	120	O	–BGRNT
27		IO_VSS	74		VSS	121		IO_VDD
28		VDD	75	I/O	D<21>	122	O	–ERROR
29	O	XTAL2	76	I/O	D<20>	123	O	–LOCK
30	I	XTAL1	77		IO_VDD	124	I	–BMACK
31	O	–RAS 0	78	I/O	D<19>	125	I/O	RD/–WR
32	I	–NONCACHE	79		IO_VSS	126	I/O	–AS
33	O	CLKOUT1	80	I/O	D<18>	127	O	–PBREQ
34	I/O	–EOP2	81	I	–BMODE16	128		IO_VSS
35	O	CLKOUT2	82	I/O	D<17>	129	O	–CAS1
36		VSS	83	I/O	D<16>	130	O	–CAS2
37	I/O	PARITY2	84		VDD	131	O	–CS0
38		VDD	85		VSS	132	I	–DREQ0
39	I	PID*	86		IO_VDD	133	O	–CS1
40	I/O	PARITY3	87	I/O	D<15>	134		VSS
41	I	–EMU_BRK	88	I	–BMODE8	135	O	–CS2
42		AVSS	89	I/O	D<14>	136	O	–CS3
43		AVDD	90	I/O	D<13>	137	O	–CS4
44	I/O	EMU_SD<3>	91	I/O	D<12>	138	I	–DREQ1
45	I/O	EMU_SD<2>	92	I/O	D<11>	139		IO_VDD
46	I/O	EMU_SD<1>	93		IO_VSS	140	O	–RAS1/–CS5
47		EMU_VSS	94	I/O	D<10>	141	O	–RAS3/–SAME_PAGE

* Test Pin: Pin 39 must be tied low in normal operation.

Pin Assignment - 208-pin SQFP

Pin No.	I/O	Name	Pin No.	I/O	Name	Pin No.	I/O	Name
142		VDD	165	I/O	ADR<4>	188	I/O	PARITY0
143		VSS	166	I/O	ADR<5>	189	I/O	ADR<17>
144		IO_VDD	167		VDD	190	O	TIMEROUT0
145	O	-DACK0	168		VSS	191	I	LSYNC
146	O	-BE3	169	I/O	ADR<6>	192	I/O	ADR<18>
147		IO_VSS	170	I/O	ADR<7>	193	I/O	ADR<19>
148	O	-BE2	171	I/O	-EOP0	194	I/O	ADR<20>
149	O	-BE1	172	I/O	ADR<8>	195	I/O	PARITY1
150	O	-BE0	173	I/O	ADR<9>	196	I/O	ADR<21>
151	I/O	ASI<0>/VDAT<4>	174		IO_VSS	197	N/A	N.C.
152		IO_VSS	175		IO_VDD	198	I	-CLKDBL
153	O	-CAS3	176	I/O	ADR<10>	199	I/O	ADR<22>
154	I/O	ASI<1>/VDAT<5>	177	I/O	-EOP1	200	I/O	ADR<23>
155	I/O	ASI<2>/VDAT<6>	178	I/O	ADR<11>	201	I/O	ADR<24>
156	I/O	ASI<3>/VDAT<7>	179	I/O	ADR<12>	202	I/O	ADR<25>
157		IO_VDD	180		IO_VDD	203		IO_VSS
158	O	-DACK1	181	I/O	ADR<13>	204		IO_VDD
159	O	-RDYOUT	182		VDD	205	I/O	PSYNC
160	I	-PDRESET	183		VSS	206	I/O	VCLK
161	O	-NVWE	184	I/O	ADR<14>	207	I/O	ADR<26>
162	O	-OE	185		IO_VSS	208	I/O	ADR<27>
163	I/O	ADR<2>	186	I/O	ADR<15>			
164	I/O	ADR<3>	187	I/O	ADR<16>			

ORDERING CODE

Clock Frequency (MHz)	Ordering Code	Package Type
25/50	MB86936-25/50-PFV-G	Plastic SQFP 208

SIGNAL DESCRIPTIONS[1]

Symbol	Type	Description
–RESET	I	**SYSTEM RESET:** Asserting reset for at least 4 processor cycles after the clock has stabilized causes the MB86936 to be initialized.
XTAL1, (CLK_IN) XTAL2	I/O O G(Q) I (Q)	**EXTERNAL OSCILLATOR:** The frequency of the XTAL1 input determines the frequency of operation of the bus. The internal frequency of operation of the part is a function of the frequency of the XTAL1 signal and the –CLKDBL signal. The XTAL2 pin should be left floating.
CLKOUT1	O G(Q) I (Q)	**CLOCK OUTPUT 1:** This is an output signal against which MB86936 bus transactions can be referenced. The CLKOUT1 frequency is the same as the frequency applied to XTAL1. CLKOUT1 is in phase with CLK_IN.
CLKOUT2	O G(Q) I (Q)	**CLOCK OUTPUT 2:** This is an output signal against which MB86936 bus transactions can be referenced. The CLKOUT2 frequency is the same as the frequency applied to XTAL1. CLKOUT2 is out of phase with CLK_IN.
–LOCK	O S(L) G(Z) I (1)	**BUS LOCK:** This is a control signal asserted by the processor to indicate to the system that the current bus transaction requires more than one transfer on the bus. The Atomic Load Store instruction, for example, requires contiguous bus transactions which cause the assertion of the bus lock signal. The bus may not be granted to another bus owner as long as –LOCK is active. –LOCK is asserted with the assertion of –AS and remains active until –READY is asserted at the end of the locked transaction.
–BREQ	I S(L)	**BUS REQUEST:** Asserted by another device on the bus to indicate that it wants ownership of the bus. The request must be answered with a bus grant (–BGRNT) from the MB86936 before the device can proceed by driving the bus. Once the bus has been granted, the device has ownership of the bus until it de-asserts –BREQ. The user should ensure that devices on the bus cannot monopolize the bus to the exclusion of the CPU. Inputs to –BREQ while –RESET is active are valid and cause Bus Grant to be asserted.
–BGRNT	O S(L) G(0) I (Q)	**BUS GRANT:** Asserted by the CPU in response to a request from a device wanting ownership of the bus. The CPU grants the bus to other devices only after all transfers for the current transaction are completed. All bus drivers are three-stated with the assertion of the bus grant signal.
–ERROR	O S(L) G(Q) I (Q)	**ERROR SIGNAL:** Asserted by the CPU to indicate that it has halted in an error state as a result of encountering a synchronous trap while traps are disabled. In this situation the CPU saves the PC and nPC registers, sets the tt value in the TBR, enters into an error state and asserts the –ERROR signal. The system can monitor the –ERROR pin and initiate a reset under the error condition. This pin is high on reset.
–MEXC	I S(L)	**MEMORY EXCEPTION:** Asserted by the memory system to indicate a memory error on either a data or instruction access. Assertion of this signal initiates either a data or instruction access exception trap in the IU. The current bus access is invalidated by asserting the –MEXC in the same cycle as the –READY signal. The IU ignores the contents of the data bus in cycles where –MEXC is asserted.
–NONCACHE	I	**NON-CACHEABLE:** Asserted by the memory system to indicate the data on the memory bus in the non-cacheable memory region. Logic 0 indicates non-cacheable and logic 1 indicates cacheable. This pin is ignored when the internal cacheability is used.

SIGNAL DESCRIPTIONS[1] (Continued)

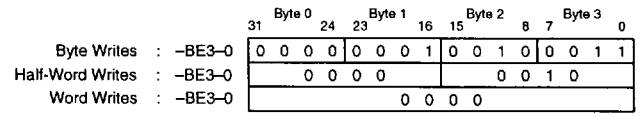
Symbol	Type	Description
IRL <3>/IRQ15 IRL <2>/IRQ14 IRL <1>/IRQ13 IRL <0>/IRQ12	I	**INTERRUPT REQUEST:** These are prioritized system requests. IRQ15 has the highest priority and IRQ1 has the lowest priority. IRQ11-1 are generated by the on-chip peripherals. IRL<3:0> are encoded interrupt inputs and IRQ15-12 are decoded interrupt inputs. The trigger for each IRQ interrupt can be programmed for a high level or a low level. The external interrupt requests are sampled during two successive external bus clock periods to minimize false interrupts.
LSYNC	I	Video line sync.
PSYNC	I/O	Video page sync.
VDAT <3:0>	I/O	Video data input/output.
VCLK	I/O	Video clock.
–CS0, –CS1, –CS2, –CS3, –CS4,	O S(L) G(1) I (1)	**CHIP SELECTS:** These outputs are asserted when the value on the address bus matches the address range in one of the corresponding ADDRESS RANGE registers. The signals are used to decode the current address into one of five address ranges. Address ranges should not overlap. Each address range has a corresponding wait specifier which is used to automatically assert the –READY signal after a user defined number of processor clock cycles. This allows a variety of memory and I/O devices with different access times to be connected to the MB86936 without the need for additional logic.
ADR <27:2>	I/O S(L) G(Z) I (1)	**ADDRESS BUS:** The 26-bit ADDRESS BUS (ADR<27:2>) is an I/O which identifies the data or instruction address of a 32-bit word. Reads are always one word in size while byte, half-word, or word transaction sizes for writes is identified by separate byte-enable signals (–BE0-3). The address bus is valid for the duration of the bus transaction. If the DRAM Controller is enabled, then MA<11:0> is output on ADR<13:2> during DRAM accesses.

SIGNAL DESCRIPTIONS[1] (Continued)

<table>
<tr><th>Symbol</th><th>Type</th><th>Description</th></tr>
<tr><td>ASI <3:0>/
VDAT<7:4></td><td>I/O
S(L)
G(Z)
I (1)
/
I/O</td><td>ADDRESS SPACE IDENTIFIERS: The ADDRESS SPACE IDENTIFIERS are I/Os which indicate to which of 16 available spaces the current ADDRESS BUS value corresponds. The ASI values are defined as follows:

<table><tr><th>ASI</th><th>ADDRESS SPACE</th></tr><tr><td>0x1</td><td>Control Register</td></tr><tr><td>0x2</td><td>Instruction Cache Lock</td></tr><tr><td>0x3</td><td>Data Cache Lock</td></tr><tr><td>0x4 - 0x7</td><td>Application Definable</td></tr><tr><td>0x8</td><td>User Instruction Space</td></tr><tr><td>0x9</td><td>Supervisor Instruction Space</td></tr><tr><td>0xA</td><td>User Data Space</td></tr><tr><td>0xB</td><td>Supervisor Data Space</td></tr><tr><td>0xC</td><td>Instruction Cache Tag RAM</td></tr><tr><td>0xD</td><td>Instruction Cache Data RAM</td></tr><tr><td>0xE</td><td>Data Cache Tag RAM</td></tr><tr><td>0xF</td><td>Data Cache Data RAM</td></tr></table>
The ASI values specified as "application definable" can be used by supervisor mode instructions such as Load Alternate and Store Alternate. The ASI value is available in the same cycle in which the corresponding address value is asserted on the address bus. The ASI pins are valid for the duration of the bus transaction. ASI 0x8, 0x9, 0xA, 0xB are cacheable. When 8-bit video is enabled, the ASI<3:0> pins are used for VDAT<7:4> I/O. However, the ASI is used internally.</td></tr>
<tr><td>–BMODE8</td><td>I
S(L)</td><td>8-BIT BOOT MODE: This signal is sampled during reset and causes read accesses, memory mapped to –CS0, to assume 8-bit ROM memory. The MB86936 generates four sequential fetches to assemble a complete instruction or data word before continuing. Bytes are fetched in sequence (0,1,2,3) as encoded by –BE[2] and –BE[3] (00, 01, 10, 11). Writes to –CS0 are unaffected by boot mode selection and, if left unconnected, a weak pull-up on this pin (and –BMODE16 pin) causes the processor to default to 32-bit mode.
Note: BMODE8 and BMODE16 should not be asserted at the same time.</td></tr>
<tr><td>–BMODE16</td><td>I
S(L)</td><td>16-BIT BOOT MODE: This signal is sampled during reset and causes read accesses, memory mapped to –CS0, to assume 16-bit ROM memory. The MB86936 generates two sequential fetches to assemble a complete instruction or data word before continuing. Half words are fetched in sequence (0,1) as encoded by –BE[2]. Writes to –CS0 are unaffected by boot mode selection. If left unconnected, a weak pull-up on this pin (and –BMODE8 pin) causes the processor to default to 32-bit mode.
Note: BMODE8 and BMODE16 should not be asserted at the same time.</td></tr>
</table>

SIGNAL DESCRIPTIONS[1] (Continued)

Symbol	Type	Description
–BE0-3	O S(L) G(Z) I (O)	**BYTE ENABLES (O):** These pins indicate whether the current store transaction is a byte, half-word or word transaction. –BE0-3 signals are available in the same cycle in which the corresponding address value is asserted on the address bus and is valid for the duration of the bus transaction. This bus should be used only to qualify store transactions. For load transactions all sub-word requests are read (and replaced in the cache) as words and then the appropriate byte or half-word is extracted by the integer unit. Possible values for –BE3-0 are as follows:  BE<2:3> are also used in 8 and 16-bit accesses as follows: Bus Mode / Byte / BE<2:3> 8-bit: 0 / 00; 1 / 01; 2 / 10; 3 / 11 16-bit: 0 & 1 / 00; 2 & 3 / 10 In 16–bit Bus mode, –BE<1:0> are byte enable. –BE<1> enables the upper byte (D<15:8>) and –BE<0> enables the lower byte (D<7:0>).
–AS	I/O S(L) G(Z) I (1)	**ADDRESS STROBE:** A control signal asserted by the MB86936 or other bus master to indicate the start of a new bus transaction. A bus transaction begins with the assertion of –AS and ends with the assertion of –READY. –AS remains asserted for 1 clock cycle. During cycles in which neither the processor nor another bus master is driving the bus the bus is idle, and –AS remains de-asserted.
D <31:0>	I/O S(L) G(Z) I (Z)	**DATA BUS:** The bus interface has 32 bidirectional data pins (D<31:0>) to transfer data in thirty-two bit quantities. D(31) corresponds to the most significant bit of the least significant byte of the 32-bit word. A double word is aligned on an 8-byte boundary, a word is aligned on a 4-byte boundary, and a half-word is aligned on a 2-byte boundary. If a load or store of any of these quantities is not properly aligned, a Not Aligned Trap will occur in the processor. In write bus cycles, the point at which data is driven onto the bus depends on the type of the preceding cycle. If the preceding cycle was a write, data is driven in the cycle immediately following the cycle in which –READY was asserted. If the preceding cycle was a read, data is driven one cycle after the cycle in which –READY was asserted to minimize bus contention between the processor and the system. Pins D<7:0> are used when the 8-bit mode is enabled and D<15:0> are used when 16-bit mode is enabled.
RD/–WR	I/O S(L) G(Z) I (1)	**READ/BUS TRANSACTION:** This signal specifies whether the current bus transaction is a read or a write operation. When –AS is asserted and RD/–WR is low, then the current transaction is a write. With –AS asserted and RD/–WR high, the current transaction is a read. RD/–WR remains active for the duration of the bus transaction and is de-asserted with the assertion of –READY.

SIGNAL DESCRIPTIONS[1] (Continued)

Symbol	Type	Description
–READY	I S(L)	**READY:** This is a control signal asserted by the external memory system to indicate that the current bus transaction is being completed and that it is ready to start with the next bus transaction in the following cycle. In case of a fetch from memory, the processor will strobe the value on the data bus at the rising edge of CLK_IN following the assertion of –READY. For the case of a write, the memory system will assert –READY when the appropriate access time has been met. In most cases, no additional logic is required to generate the –READY signal. On-chip circuitry can be programmed to assert –READY based on the address of the current transaction. The external system can override the internal ready generator to terminate the current bus cycle early. Up to 5 address ranges each with different transaction times can be programmed.
–DREQ0-2	I A(L)	**DMA REQUEST:** Indicates that an external device is requesting a DMA transfer. This signal is edge sensitive for single transfers and level sensitive for demand transfers. –DREQ0 corresponds to DMA channel 0, –DREQ1 corresponds to DMA channel 1 and –DREQ2 corresponds to DMA channel 2. If DMA Channel 0 is being used by the Video Interface, –DREQ0 is ignored.
–DACK0-2	O	**DMA ACKNOWLEDGE:** This signal is asserted when an external device asserts –DREQ and the processor accesses the external device. –DACK1 corresponds to DMA channel 0, –DACK1 corresponds to DMA channel 1 and –DACK2 corresponds to DMA channel 2.
–EOP0-2	I/O	**END OF PROCESS:** This signal is asserted by the external device when it wants to terminate a DMA transfer. Alternately, the processor drives this signal when the byte count reaches zero. –EOP0 corresponds to DMA channel 0, –EOP1 corresponds to DMA channel 1 and –EOP2 corresponds to channel 2. A pull-up holds –EOP0-2 high when it is not being driven.
–PBREQ	O	**PROCESSOR BUS REQUEST:** This signal is asserted by the processor to indicate to an external bus arbiter that it needs to regain control of the bus. This provides a handshake between the arbiter and the processor to allow the bus to be allocated based on demand.
–BMREQ	O	**BURST MODE REQUEST:** This signal is asserted by the processor to indicate to the external system that the processor's burst mode is enabled and the current transaction can be a burst. If the external system supports burst mode, it asserts –BMACK concurrently with –RDY to begin the burst mode transfer.
–BMACK	I	**BURST MODE ACKNOWLEDGE:** This signal is asserted by the system to indicate that it can support burst mode for the address currently on the bus. The system asserts –BMACK in response to the processor asserting –BMREQ.
CLK_ECB	I	**EXTERNAL CLOCK BYPASS:** Tying this signal high causes the CLK_IN signal to bypass the Phase Lock Loop (PLL). This signal is used for testing of the chip.
–CLKDBL	I	**CLOCK DOUBLER:** Tying this signal low causes the internal logic to run at twice the frequency of the clock input.

SIGNAL DESCRIPTIONS[1] (Continued)

Symbol	Type	Description
–RAS3/ –SAME_PAGE	O O S(L) G(1) I (1)	**–RAS3 DRAM Row Address Strobe:** Can be connected directly to the corresponding –RAS pin of a DRAM. Typically, –RAS is used to select a DRAM bank. When the 936 DRAM controller is disabled, this pin will output **–SAME_PAGE.** **SAME-PAGE DETECT:** The –SAME_PAGE is used to take advantage of fast consecutive accesses within Fast Page Mode DRAM page boundaries. This signal is an output asserted by the processor when the current address is within the same page as the previous memory access. –SAME_PAGE is never asserted in the first transaction following a transaction by another device on the bus. The page size is specified by writing the SAME-PAGE MASK register.
–RAS2 –TIMER_OVF	O O S(L) G(Q) I (Q)	When the 936 DRAM controller is disabled, this pin will output **–TIMER_OVF** **TIMER UNDERFLOW:** Asserted by the processor to indicate that the internal 16-bit timer has underflowed. This signal can be used to initiate a DRAM refresh cycle or a one cycle periodic waveform. On reset, the timer is turned off and –TIMER_OVF is high.
–RAS1/ –CS5, –RAS0	O	When the 936 DRAM controller is enabled –CS4, –CS5, represent the same DRAM space. This is to control which part of the DRAM is non-cacheable, When the 936 DRAM controller is disabled, –RAS1 pin will output –CS5. Please see the pin description of CHIP SELECTs –CS0-4.
–CAS0-3	O	**DRAM Column Address Strobe:** Can be connected directly to the corresponding –CAS pin of a DRAM. –CAS is used to select bytes within a 32-bit DRAM word.
–DWE	O	**DRAM Write Enable:** Can be connected directly to the corresponding –WE pin of a DRAM.
–NVWE	O	**WRITE ENABLE FOR NON-VOLATILE MEMORY:** This signal is asserted one cycle after –AS and stays asserted till one cycle before the end of the transaction for a write operation. The signal is generated only when internal wait state generation in enabled for current access.
–OE	O	**OUTPUT ENABLE:** The signal is asserted one cycle after –AS and stays asserted till the last cycle of a read operation. This signal is generated when internal wait state generation is enabled for the current access.
–READYOUT	O	Ready Out for External Bus Masters using Internal Ready Generation.
TIMEROUT0	O	Timer output pin. According to the mode, the output wave functions as (1) periodic interrupt signal output; (2) square wave output: (3) one-shot pulse output; This pin is low during reset.
PARITY 3-0	O	Parity3 corresponds to D<31:24>, Byte 0 Parity2 corresponds to D<23:16>, Byte 1 Parity1 corresponds to D<15:8>, Byte 2 Parity0 corresponds to D<7:0>, Byte 3
–PDRESET	I	Power Down Reset is asserted by the external system to get the part out of power down mode.

SIGNAL DESCRIPTIONS[1] (Continued)

Symbol	Type	Description
EMU_SD <3:0>	I/O	**EMULATOR STATUS/DATA BITS:** Bi-directional pins used by a hardware emulator to control and monitor MB86936 execution. These pins should be left unconnected.
EMU_D<3:0>	I/O	**EMULATOR DATA BITS:** Bi-directional pins used by a hardware emulator to control and monitor MB86936 execution. These pins should be left unconnected.
–EMU_BRK	I	**EMULATOR BREAK REQUEST LINE:** Input used by a hardware emulator to request a trap when emulation is enabled. This pin should be left unconnected.
–EMU_ENB	I/O	**EMULATOR ENABLE:** Tied low while the MB86936 is being reset to enable hardware emulator mode on the chip. This pin should be left unconnected.
TCK	I	**TEST CLOCK:** JTAG compatible test clock input.
TMS	I	**TEST MODE:** JTAG compatible test mode select pin.
TDI	I	**TEST DATA IN:** JTAG compatible test data input.
TDO	O	**TEST DATA OUT:** JTAG compatible test data output.
–TRST	I	**TEST RESET:** Asynchronous reset for JTAG logic. If not using JTAG, this signal must be pulled low.

1. In the following descriptions, signal names preceded by a minus sign (–) indicate an active low state. Dual function pins have two names separated by a slash (/).

NOTES:
- I = Input Only Pin
- O = Output Only Pin
- I/O = Either Input or Output Pin
- \- = Pins "must be" connected as described
- A(L) = Asynchronous: Inputs may be asynchronous to CLKOUT.
- S(L) = Synchronous: Inputs must meet setup and hold times relative to CLK_IN. Outputs are Synchronous to CLK_IN

G(...) = While the bus is granted to another bus master (–BGRNT=asserted), the pin is
- G(1) is driven to V_{CC}
- G(0) is driven to V_{SS}
- G(Z) floats
- G(Q) is a valid output

I (...) = While the bus is between bus cycles (or being reset) and is not granted to another bus master, the pin is
- I (1) is driven to V_{CC}
- I (0) is driven to V_{SS}
- I (Z) floats
- I (Q) is a valid output

OVERVIEW

The Fujitsu MB86936 is a high performance, 32-bit RISC processor which executes at 50 MIPS peak performance with 50 MHz clock frequency. It has a floating point Unit that performs single precision multiply and single precision adds at the rate of 1 per cycle. Like its predecessors, the MB86936 is based on the SPARC architecture and is upward code compatible with previous implementations. The MB86936 has been developed specifically with the needs of embedded applications in mind and offers high performance and high integration for these applications.

The MB86936 instruction set is streamlined and hardwired for fast execution with most instructions executing in a single cycle. The Integer Unit (IU) features a 5-stage pipeline which has been designed to handle data interlocks, has an optimized branch handler for efficient control transfers, and a bus interface to handle single cycle bus accesses to on-chip memory.

An internal register file consisting of 136 registers organized into eight overlapping windows speeds interrupt response time and context switches. The register file minimizes accesses to memory during procedure linkages and facilitates passing of parameters and assignment of variables.

On-chip 4 Kbyte instruction and 2 Kbyte data caches have been added to decouple the processor from external memory. These caches have been designed with maximum flexibility in mind and allow entries to be locked to improve overall system performance.

The FPU gets data from a 32 word register file for all standard FPU instructions. The 64-bit wide Dcache datapath speeds load double floating point on a hit. The 64-bit wide write buffer improves performance on store double floating point.

Separate 32-bit on-chip instruction and data paths provide a high bandwidth interface between the IU and on-chip cache. These buses support single cycle instruction execution as well as single cycle data transfers with the cache.

The MB86936 also includes hardware for integer multiply and divide step. The hardware support significantly improves the performance of these operations with 32-bit integer multiplies executing in 5 clock cycles, 16-bit integer multiplies in 3 cycles, 8-bit integer multiplies in 2 cycles, and a multiply by zero can complete in a single cycle.

KEY FEATURES

Fast Integer Unit Instruction Execution: Simple functions make up the bulk of instructions in most programs so that execution speed can be greatly improved by designing these instructions to execute in as short a time as possible. The majority of instructions execute in one cycle with only a few of the more complex, such as integer multiply, taking additional cycles.

Fast Floating Point Unit

The high performance FPU implemented on the MB86936 executes all Single/Double precision operations. The FPU has a three stage pipeline. All single precision operations, except the Divide and Square Root are executed at the rate of one per cycle. Double Precision Add and Subtract are also executed at the rate of one per cycle.

Large Register Set: The large register set for the IU reduces the number of required accesses to data memory. The registers are organized in overlapping groups called register windows which allows registers to be reserved for high priority tasks, such as interrupts, or for recurring requirements such as operating system working registers. The overlapping windows also simplify parameter passing during procedure linkage and reduce code in most programs.

On-Chip Caches: To decouple the speed of the processor from the memory sub-system, separate data and instruction caches have been added. The caches are organized as two-way set-associative for improved hit rates. In addition, the set-associative caches organization allows entries to be locked, while the rest of the cache performs normally.

Cache Locking: Both data and instruction entries can be locked into their respective caches to ensure deterministic response and highest performance for critical or frequently recurring routines. Maximum flexibility has been designed into the cache to allow all or selected portions to be locked.

Bus Interface: The requirement for glue logic between the MB86936 and the system is minimized by providing programmable chip selects, programmable wait state circuitry, programmable cacheable memory address, and support for connection to fast page-mode DRAM. Multiple bus masters are supported through a simple handshake protocol. The MB86936 can boot from either 8, 16 or 32-bit wide memory. In addition, the programmable data bus allows reading/writing of different memory widths. For high frequency operation, the bus is capable of running at half the speed of the core.

On-Chip DMA: Three DMA channels support contiguous block and chained block transfers. Byte, halfword, word, and quad-word data types are supported. Either fly-by or flow-through addressing modes can be selected. DMA channel 0 can be used for Video-DMA operations.

Clock Generator: To simplify the clock design a crystal can be connected directly to the on-chip oscillator or an external clock source can be used. A built in phase-locked loop minimizes the skew between on and off-chip clocks.

Enhanced Instruction Set: The MB86936 includes a fast integer multiply instruction which executes in a fast 5, 3 or 2 cycles for 32-bit, 16-bit or 8-bit multiplicands. An integer divide-step instruction cuts divide times by a factor of 10 over previous SPARC implementations. A scan instruction supports a single cycle search for the most significant 1 or 0 in a word or bit differing from sign bit.

Power Down Modes

The MB86936 supports multiple power down modes. The power down control register provides a mechanism to turn off the clock to various functional units. These can be turned off by the application program if it is not using the particular functional unit. Some of the units can be woken up by writing to the power down control register. -PDRESET is asserted to wake up the entire chip from power down.

TABLE 1. MB86936 Instruction Set

LOGICAL	ARITHMETIC/SHIFT	DATA MOVEMENT	FPU INSTRUCTIONS
CONDITION CODES UNCHANGED AND OR XOR AND NOT OR NOT XNOR **CONDITION CODES SET** AND OR XOR AND NOT OR NOT XNOR	**CONDITION CODES UNCHANGED** ADD SUBTRACT MULTIPLY(SIGNED/UNSIGNED) SCAN SETHI SHIFT LEFT LOGICAL SHIFT RIGHT LOGICAL SHIFT RIGHT ARITHMETIC **CONDITION CODES SET** ADD SUBTRACT MULTIPLY(SIGNED/UNSIGNED) MULTIPLY STEP DIVIDE STEP **EXTENDED AND CONDITION CODES UNCHANGED** ADD SUBTRACT **EXTENDED AND CONDITION CODES SET** ADD SUBTRACT **TAGGED AND CONDITION CODES SET (WITH AND WITHOUT TRAP ON OVERFLOW)** ADD SUBTRACT	**TO USER/SUPERVISOR SPACE SIGNED** LOAD BYTE LOAD HALF-WORD LOAD WORD LOAD DOUBLE WORD STORE BYTE STORE HALF-WORD STORE WORD STORE DOUBLE WORD **TO USER SPACE UNSIGNED** LOAD BYTE LOAD HALF-WORD **TO ALTERNATE SPACE SIGNED** LOAD BYTE LOAD HALF-WORD LOAD WORD LOAD DOUBLE WORD STORE BYTE STORE HALF-WORD STORE WORD STORE DOUBLEWORD **TO ALTERNATE SPACE UNSIGNED** LOAD BYTE LOAD HALF-WORD **ATOMIC OPERATION IN USER SPACE** SWAP WORD LOAD/STORE UNSIGNED BYTE **ATOMIC OPERATION IN ALTERNATE SPACE** SWAP WORD LOAD/STORE UNSIGNED BYTE	**CONVERSION** CONVERT INTEGER TO SINGLE CONVERT INTEGER TO DOUBLE CONVERT SINGLE TO INTEGER CONVERT DOUBLE TO INTEGER CONVERT SINGLE TO DOUBLE CONVERT DOUBLE TO SINGLE **MOVE** MOVE NEGATE ABSOLUTE VALUE **SQUARE ROOT** SQUARE ROOT SINGLE SQUARE ROOT DOUBLE **ADD/SUBTRACT** ADD SINGLE ADD DOUBLE SUBTRACT SINGLE SUBTRACT DOUBLE **MULTIPLY/DIVIDE** MULTIPLY SINGLE MULTIPLY DOUBLE MULTIPLY SINGLE TO DOUBLE DIVIDE SINGLE DIVIDE DOUBLE **FLOATING-POINT COMPARE INSTRUCTIONS** COMPARE SINGLE COMPARE DOUBLE COMPARE SINGLE AND EXCEPTION IF UNORDERED COMPARE DOUBLE AND EXCEPTION IF UNORDERED
CONTROL TRANSFER CONDITIONAL BRANCH CONDITIONAL TRAP CALL RETURN SAVE RESTORE JUMP AND LINK			**BRANCH ON FLOATING-POINT CONDITION CODES** BRANCH ALWAYS BRANCH NEVER BRANCH ON UNORDERED BRANCH ON GREATER BRANCH ON UNORDERED OR GREATER BRANCH ON LESS BRANCH ON UNORDERED OR LESS BRANCH ON LESS OR GREATER BRANCH ON NOT EQUAL BRANCH ON EQUAL BRANCH ON UNORDERED OR EQUAL BRANCH ON GREATER OR EQUAL BRANCH ON UNORDERED OR GREATER OR EQUAL BRANCH ON UNORDERED OR LESS OR EQUAL BRANCH ON LESS OR EQUAL BRANCH ON ORDERED
READ/WRITE CONTROL REGISTER READ PSR, WRITE PSR, READ TBR, WRITE TBR READ WIM, WRITE WIM, READ Y, WRITE Y READ ASR, WRITE ASR			
LOAD/STORE FLOATING-POINT LOAD FLOATING-POINT REGISTER LOAD DOUBLE FLOATING-POINT REGISTER LOAD FLOATING-POINT STATE REGISTER STORE FLOATING-POINT STORE DOUBLE FLOATING-POINT STORE FLOATING-POINT STATE REGISTER STORE DOUBLE FLOATING-POINT DEFERRED TRAP QUEUE			

Test and Debug Interface: The MB86936 supports production test through industry standard JTAG boundary scan. Hardware emulation is supported with on-chip breakpoint and single step logic. A dedicated emulator bus provides a means to trace transactions between the integer unit and on-chip cache.

CPU

The MB86936 core is a high performance fully custom implementation of the SPARC architecture. The core is compact to leave room for peripheral integration and yet is designed in a way to allow the major blocks to be customized for varying application requirements. The core is made up of three functional units: the Instruction block, the Address block and the Execute block. (see Figure 1)

A five stage instruction pipeline is responsible for decoding all instructions and generating the control signals to the other blocks. The 5-stage pipeline consists of Fetch (F), Decode(D), Execute(E), Memory(M) and Writeback(W). Instruction memory is addressed and returns instructions in the (F) stage, the register file is addressed and returned operands in the (D) stage, the ALU computes results in the (E) stage, external memory is addressed in the (M) stage, and the register file is written back in the (W) stage.

FPU

The high performance FPU implemented on the MB86936 is compatible with the ANSI/IEEE-754-1985 standard. It is fully compatible with SPARC ver. 8 FPU.

The FPU is implemented as a 3 stage pipeline. The FPU executed all Single/Double precision floating point operations. Quad precision floating point operations are not executed by the FPU. All floating point load and stores and Branch on Floating point condition code instructions are executed by the integer unit.

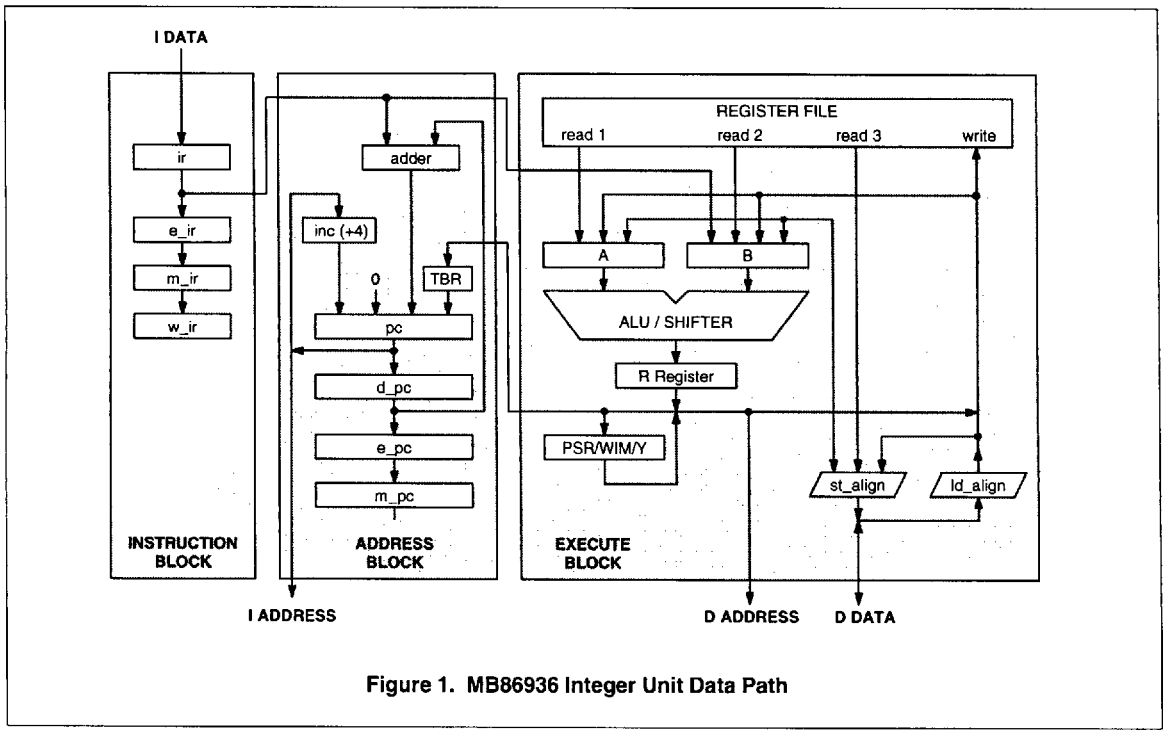


Figure 1. MB86936 Integer Unit Data Path

The performance of the FPU is summarized below:

Floating Point Operation	Throughput (in cycles)	Latency (in cycles)
All comparison and conversions	1	3
Single Precision ADD/ SUB/MUL	1	3
Single Precision DIV/ SQRT	13	14
Double Precision ADD/SUB	1	3
Double Precision MUL	4	6
Double Precision DIV/ SQRT	28	29

Even though the Floating point queue is 3 deep, whenever a divide or square root enters the queue it is marked as full to prevent any other floating point instructions from entering the queue. This is done to prevent the interrupt latency from being long.

ADDRESS SPACE

The MB86936 offers a large addressing range and allows separate user and supervisor spaces to be defined. In addition to 26 address lines, 8 alternate address space identifier bits (ASIs) distinguish between protected and unprotected space. Of the 256 possible ASI values, two define accesses to user data and user instruction space while the remaining ASI values define supervisor space.

Anytime a reset, synchronous trap or asynchronous trap occurs, the processor is placed into the supervisor mode. In this mode, the processor executes instructions and moves data out of supervisor space. While in supervisor mode, the processor also has access to the remaining ASI values. Except for those mentioned and those reserved for control register space, the remaining ASI values can be used to access other alternate data spaces defined by the application.

The distinction of user versus supervisor space allows the hardware to protect against accidental or un-authorized access to system resources. For real time operating system (RTOS) development for example, the separate spaces provide a mechanism for effectively partitioning RTOS space from user space.

REGISTERS

The MB86936 integer unit register set is divided into those used for general purpose functions and those used for control and status.

The 136 general purpose registers are divided into 8 global registers and 8 overlapping blocks or "windows". Each window contains 24 registers. Of these, 8 are local to the window, 8 "out" registers overlap with the next window and 8 "in" registers overlap with the previous window (see Figure 2).

This organization makes it easy to pass parameters to subroutines. Parameters that are to be passed along are written to the "out" registers and the subsequent procedure call decrements the window pointer to make a new set of registers available. The passed parameters are now available to the subroutine in the current window's "in" registers.

Register windows improve performance in embedded applications because they function as local variable caches which retain either interrupt, subroutine, context or operating system variables with no additional overhead. In addition, code can be reduced by exploiting the efficient execution of procedure linkage by preventing in-lining compiler optimizations.

The registers that make up the register file each have three read-only and one write-only port. The use of a four port register file allows even store instructions, which may require that three operands be read out of the register file, to proceed at one instruction per cycle.

The control and status registers include those defined by the SPARC architecture (See Table 2) and those mapped into alternate address space to control peripheral functions (See Table 3).

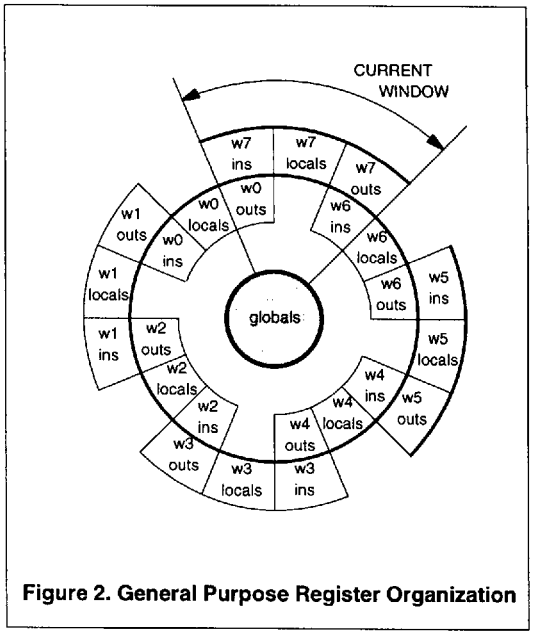


Figure 2. General Purpose Register Organization

INSTRUCTION SET

The MB86936 is upward code compatible with other SPARC processors. Additional instructions, previously not directly supported, have been added to improve performance in embedded applications. Enhanced Floating-point instructions, integer multiply, integer divide step, and scan for first changed bit have been added to the already powerful SPARC instruction set. See Table 1 for a list of supported instructions.

INTERRUPTS

A key measure of a processor's suitability for use in embedded application is in its ability to handle interrupts with a minimum of delay and in a deterministic fashion. The MB86936 implementation has been tailored to insure not only low average latency but low maximum latency as well.

Interrupt response time is made up of the sum of the times it takes the processor to finish its current task after recognizing an interrupt, and the time it takes to begin executing interrupt service routine instructions. The MB86936 implements numerous features to minimize both factors.

To minimize the time it takes to finish the current task, the MB86936 is designed so that tasks can either be interrupted or completed in a minimum number of cycles. Implementation details that accomplish this aim include cache line misses that can be filled one word at a time through a pre-fetch buffer, integer divide that is interruptible through the use of a divide step instruction, fast multiply and a 4 deep write buffer to limit pending bus transactions.

To minimize the time required to start executing the interrupt service routine the processor switches to a new register window when an interrupt is detected. This feature allows the service routine to be executed without first requiring that the current registers be saved. The user can also elect to lock the service routine into the cache. This makes the routine available for immediate access. The on-chip data cache can also serve the service routine as a fast local stack for minimum delay in accessing routine variables.

The MB86936 provides for up to 15 different interrupt levels. The highest interrupt level is non-maskable.

CACHE

The MB86936 has separate on-chip data and instruction caches. This allows the user to build a high performance system without incurring the cost of requiring fast external memory and the associated control logic. The caches are physically mapped.

The instruction cache is organized as two banks of sixty-four 32-byte lines (See Figure 5). The data cache is organized as two banks of sixty-four 16-byte lines (See Figure 4).

The lines are organized as two-way set-associative for good performance even when cache locking is in effect. Lines are divided into sub-blocks each four bytes wide. On a cache miss, the caches are updated either 1 word (4 bytes) at a time, or 4 words at a time using the processor's burst mode feature. Single word updates minimize interrupt latency associated with long cache line replacements, while 4 word burst refills maximize the use of available bus bandwidth. An instruction pre-fetch buffer fetches the next sequential instruction anticipating that it will be needed to fill the next instruction cache miss.

The caches can be used in either normal or one of two lock modes. In normal mode, the caches use an LRU (least recently used) algorithm to replace one of the two appropriate entries. Alternately, the two locking modes allow the entire cache or just selected entries to be locked. The lock modes allow time critical routines to be locked in cache.

Global locking allows the entire content of either the instruction or data cache to be frozen. Two control bits in the cache control register enable or disable locking for either cache. With the entire cache locked, no valid entry can be replaced. To insure best possible performance however, invalid entries will be updated if they are accessed. This is done automatically and incurs no time penalty.

Local cache locking makes it possible to dynamically lock selected instructions or data entries into the appropriate cache. This feature gives the flexibility, for example, to assure deterministic response for certain critical interrupt routines by locking the routine's code into the cache. Entries can also be locked where it is desirable to give performance priority to certain often used routines which might otherwise be removed from cache. The 2-way set-associativity allows the cache to perform effectively even with some locked entries.

In local lock mode, each entry can either be locked individually by software or automatically with hardware assist. For individual locking, software writes the lock bit in the appropriate cache tag line. For automatic locking, a bit in each cache control register enables or disables the feature. The enable bit is set at the beginning of a routine for which the entries are to be locked. This causes the location of any cache access occurring while the bit is enabled to be locked into the cache. In addition to requiring just one initial cycle to enable, automatic entry locking incurs no overhead while in effect. Locked locations can be cleared with a single write to a control register.

In unlocked operation, the data cache uses a write-through update policy and allocates a cache entry only on a load. Writes are buffered so that the processor can continue executing while data is written back to memory. In contrast, writes to locked data cache locations are not written through to main memory. Besides reducing external bus activity, this design supports configuring a portion of data cache as on-chip RAM which does not map to external memory.

The data and instruction caches are designed to be accessed independently over separate data and instruction buses to allow data to be loaded from and stored to cache at peak rates of 1 CPI.

The user of MB86936 has the flexibility of setting different data memory space to be cacheable or non-cacheable through either software programming or hardware control.

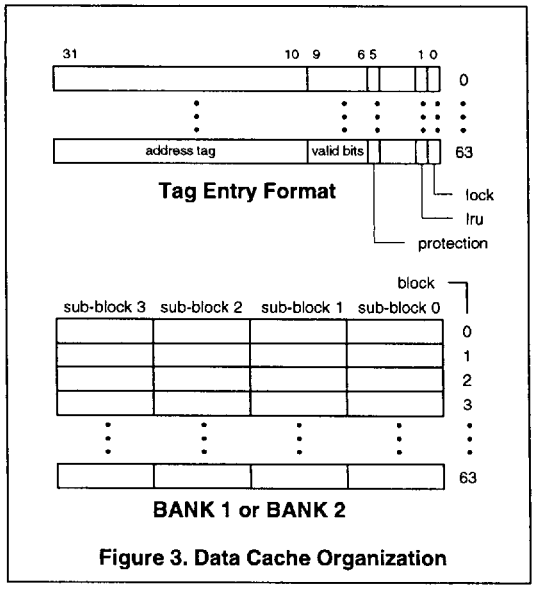


Figure 3. Data Cache Organization

Upon reset, bit 7 of Cache/Bus Interface Unit Control Register (ASI=0x01 ADR=0x0000 0000) indicate that cacheability is controlled by a hardware pin, –NON-CACHE. When the –NON-CACHE pin is low, the data associated with the address is non-cacheable, and vice versa. The hardware control of cacheability is independent of chip select.

The user can program a logic 1 into bit 7 of Cache/Bus Interface Unit Control Register to allow software to control cacheability. By programming a few bits in the BIU control register space (ASI = 0x01, Address = 0x0000 016C), MB86936 allows the option to force external memory access (non-cacheable) based on chip select.

–CS4 and –CS5 cacheability are the special case. When the internal DRAM controller is turned off, the cacheability of –CS4 and –CS5 behaves as all other chip selects. When the internal DRAM controller is enabled, data memory space referred by –CS4 will always be cacheable, and data memory space referred by –CS5 will always be non-cacheable. When the entire DRAM space referred by –CS4 is to be cacheable, memory space referred by –CS5 has to fall outside –CS4 memory space.

BUS INTERFACE

The Bus Interface Unit (BIU) is designed to simplify the interface between the MB86936 and the rest of the system. Separate address and data buses make it easy to build fast systems. At the same time, on-chip circuitry allows these systems to be built with a minimum of external hardware.

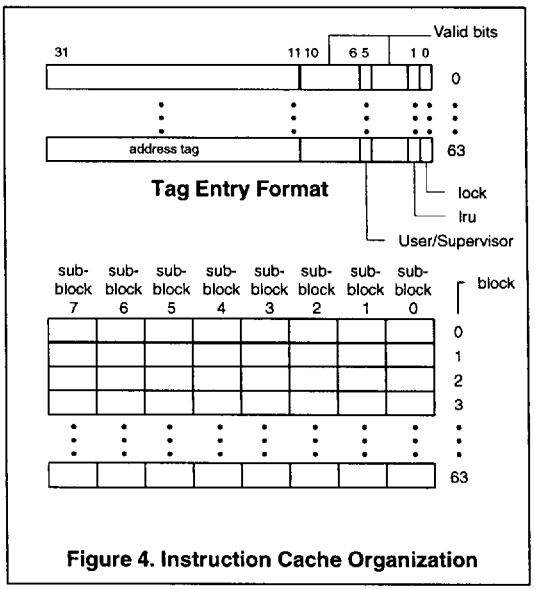


Figure 4. Instruction Cache Organization

Three DMA channels provide high speed memory-to-memory and memory-to-peripheral data transfers. The DMA channels execute independently of the processor and make it possible for the processor to continue to execute from cache while the DMA transfers are taking place. Flexible priority allows the processor to suspend transfers if it needs to use the bus (on a cache miss for example).

The MB86936 DMA controller supports byte, halfword, word and quad-word transfers. Either fly-by or flow-through transfers are possible under single, block and demand transfer modes. Transfers can be chained to support scatter/gather operations. The DMA transfers are initiated either by software or by external hardware handshake.

The BIU can also operate in a mode where the CPU core operates at twice the frequency of the bus interface. This is provided to ease the system design for system where the CPU is running at a high frequency.

The bus interface supports fully programmable wait state generation, address decoding with chip select outputs, booting from 8 and 16-bit wide memory, and an auto-reload timer. A burst mode bus supports fast cache line fills. Address pins A3 and A2 will reflect the internal address change during burst mode. Parity is generated by the BIU during writes and checked during reads. Each chip select can be also programmed to support 8, 16 or 32-bit wide memory read/write. One caution here is that when –CS4 and –CS5 is used with internal DRAM controller, only 16 and 32-bit data is supported. Please see the section on DRAM Controller for detailed description of DRAM access.

INTERRUPT CONTROLLER

MB86936 IRC functions are a superset of the IRC functions of MB86930 and MB86940. It has 3 modes:

Mode 0: Supports external encoded interrupts IRL<3:0>. (as in MB86930) (This mode will only accept external encoded interrupts.) As a result, Mode 0 supports 15 external interrupt sources and none of the internal (on-chip) interrupt sources.

Mode 1: Supports 4 external decoded interrupts IRQ15-12 and 11 internal decoded interrupts IRQ11-1 simultaneously (similar to MB86940). In addition, three groups of internal interrupt channels have programmable priority. Each group consists of two interrupt channels. The priority of channels within the group is fixed. Group 3 consists of channel 9 and 8, group 2 consists of channel 6 and 5, and group 1 consists of channel 3 and 2.

Mode 2: Supports 4 external decoded interrupts IRQ15-12 and 11 internal decoded interrupts IRQ11-1. The external interrupt channels are dispersed in priorities with internal interrupts, and there are 5 groups of internal interrupt channels that are programmable. Each group of internal interrupts that is programmable consists of 2 channels; the priority of the channels within a group cannot be changed.

Group 5 consists of channel 11 and 10, group 4 consists of channel 7 and 4, group 3 consists of channel 9 and 8, group 2 consists of channel 6 and 5, and group 1 consists of channel 3 and 2.

The interrupt channel assignments for each of the modes is described in the next page.

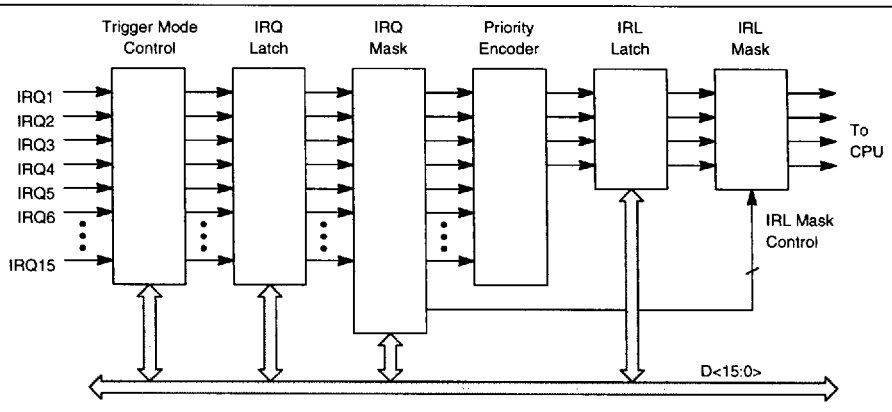


Figure 5. IRC Block Diagram in mode 1

The IRC has the following programmable interrupt trigger modes for each channel IRQ15–1 (internal or external): high-level and low-level. The external interrupt requests must be asserted for at least 2 external bus clock cycles to be recognized as in MB86940.

Details of Mode 1 operation:

The Interrupt Request Controller (IRC) is a 15-channel, programmable-trigger interrupt controller that arbitrates pending unmasked interrupt requests, encodes the highest-priority interrupt, and interrupts the processor. The system processor responds by servicing the interrupt and clearing the latched interrupt request in the IRC. IRQ11-1 are used for on-chip peripherals (Timer, Video Interface, DMA).

Figure 6 shows a block diagram of the IRC operation in mode 1.

The Trigger Mode Control logic selects one of two trigger modes for each channel: high level and low level. The processor controls the triggers by writing to the Trigger Mode registers.

The IRQ Latch captures each interrupt request. The system processor reads the latch via the Request Sense register, and clears the latch by writing to the Request Clear register.

Table of Internal Interrupt source in Mode 1:

Interrupt Channel	Interrupt Source
9	Video Controller
8	DMA Channel 1; EOP1
6	DMA Channel 0; EOP0
5	Timer0
3	Timer1
2	DMA Channel 2; EOP2

NOTE: When EOP2, EOP1, EOP0 are not used for interrupt, the IRC must be programmed to mask out the corresponding channels.

CLOCK GENERATOR

The on-chip clock generator provides a means to directly connect the MB86936 to either a crystal oscillator or an external clock source. For either case, the external frequency is the same as the chip operating frequency.

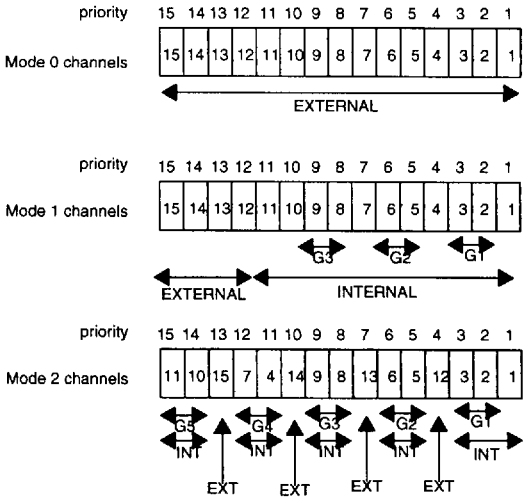


Figure 6. Interrupt channel assignment for each interrupt mode

A clock output signal provides the system with a reference by which external timing can be synchronized when not using an external clock source. The skew between the internal clock and an external input clock source is minimized by the inclusion of an on-chip phase lock loop circuit.

MB86936 allows the internal core to run at twice the frequency of external clock by enabling -CLKDBL pin.

-CLKDBL	Case
1	Normal
0	CPU runs at 2x frequency of BIU

TIMER

The MB86936 features two independent general-purpose 24-bit timer (a 16-bit counter with an 8-bit prescaler) that can be independently programmed to operate in one of the following three modes. Timer1 output is connected to bit 3 of internal interrupt request bus, therefore, will generate interrupt request when active (programmable in interrupt controller). Timer0 output is connected to bit 5 of interrupt request bus.

- Mode 0 - Periodic Interrupt Mode
- Mode 1 - Time-out Interrupt Mode
- Mode 2 - Square Wave Generator Mode

The timer has a clock prescaler that can be clocked by the internal clock. The counter itself can be independently clocked by the prescaler clock (PRSCK), or by the internal clock.

Figure 8 shows a block diagram of the timer and prescaler, and its clock options.

The pin TIMEROUT0 will be the only output of TIMER0. TIMER1 is identical to TIMER0 but it does not have Timerout output. Timer 1 can only generate interrupt.

VIDEO INTERFACE

The video Interface provides direct connection to a number of laser-beam marking engines. It may also be used to receive data from a raster input device such as a scanner or to serialize/deserialize a data stream.

General functions:

- Internal or external VCLK with programmable polarity and programmable 4-bit clock division.
- Suspend the operation when VCLK is inactive (for external VCLK only).
- Internal or external PSYNC with programmable polarity.
- External LSYNC with programmable polarity.
- Either DMA (channel 0) or interrupt request on transmit FIFO threshold or receive buffer full.
- Programmable Line-Width, Image-Address, Block-Height, Top-Margin and Left-Margin.
- Programmable interrupt sources.
- During DMA transfers, video transfer progress may be monitored by reading the DMA channel's registers.

Transmit functions:

- 8-word deep 32-bit wide FIFO with programmable threshold.
- Programmable blank level and width (1, 4 or 8) for VDAT<7:0>. When 8-bit video is enabled, ASI<3:0> pins will be used for VDAT<7:4>.
- Reverse mode transmission.
- Programmable word or quad word DMA to load the FIFO.

Receive functions:

- 1-word 32-bit wide holding buffer.
- Status to indicate receive buffer full (data available).

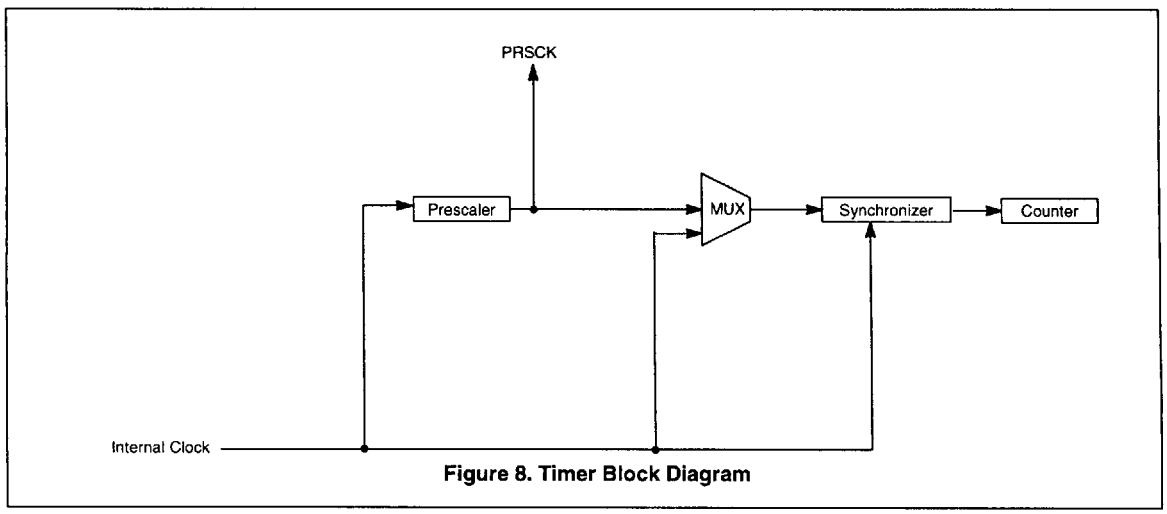


Figure 8. Timer Block Diagram

Video Interface Overview

The serial data transfer timing is controlled through the PSYNC, LSYNC and VCLK pins. Data transfers to/from main memory and the video interface can be handled either through DMA or interrupt driven means. The active level of PSYNC and LSYNC is programmable, as is the active edge of VCLK (rising or falling). The VDAT levels are also programmable: inverted or non-inverted data, and 0 or 1 for the Blank-Data level.

Both PSYNC and VCLK can be either internally or externally generated signals. The default condition is externally generated for both signals. If VCLK is internally generated, it will be a free-running divided-down version of the internal clock. If VCLK is externally generated, VCLK will be divided down internally by a factor of 1 to 16. External VCLK may be stopped at any time to suspend the video interface's operation.

Video Transmit

The page cycle begins when PSYNC is active either as an input or an output. At the beginning of a page cycle, four count-down registers are loaded from the top margin, left margin, block height and line width registers. When the top margin is zero the first line will be transmitted. Blanks will be transmitted until the left margin is zero. The actual data is transmitted until the line width is zero.

After the video-interface has been initialized, it waits for PSYNC to become active to indicate the beginning of a page. If PSYNC is a level signal, PSYNC is normally held active until the end of the page.

LSYNC being asserted indicates the beginning of a line. TopMargin number of lines (LSYNCs) are skipped before sending any data. During this time, Blank-level data is present on the VDAT pins. After LSYNC is asserted, LeftMargin bits (VCLKs) are skipped before sending the serial data. During that time, Blank-Level data is present on the VDAT lines. After the left margin is passed, data is shifted out until the end of the printed line (LineWidth VCLK's). Blank-level data is sent out on the VDAT lines until LSYNC is de-asserted and re-asserted again (next line).

The data to be transmitted does not need to be word-aligned in memory, but must be at least byte-aligned. The StartBit register is used to start the shifting at one of 4 bit positions in the first word of each line.

The video interface also has a blank-page feature which forces the VDAT output to the blank level for the entire page. To print a blank page, set the blank-page bit in the video control register to 1, and set up a normal video transmit (DMA may also be initialized, but the video interface will ignore the data). This feature is normally used in interrupt-driven transfer mode. No data needs to be written to the video transmit register (FIFO).

Aborting and Restarting Video Transmit

If a page which is being printed needs be aborted and restarted (as in the case of a paper-jam), the re-print operation can be started by writing just a few registers.

All of the video registers retain their values until they are changed by the user (or by reset), therefore, to restart a page, only the video control register will need to be written (to re-enable the video interface). However, if DMA is used, then the DMA registers will need to be re-programmed (DMA registers do not hold their value). If a chained DMA operation was used for example, this would simply require programming the DMA descriptor-pointer and the DMA control register. It is the responsibility of the software to retain the values for reprogramming the DMA registers and the video control register.

Video Receive

Only pins LSYNC, VCLK and VDAT are needed in receive mode. When LSYNC is active, the line count determines the number of bits to receive on VDAT. For high performance, the received data is buffered in a 32-bit receiving buffer. Either an interrupt or DMA is requested when the holding register is full.

The video receive operation is similar to the transmit operation, except TopMargin is not used. Serial data is collected in to a de-serializing buffer as long as PSYNC is asserted. Each line begins with LSYNC and continues for LineWidth VCLK's. When the serial data buffer becomes full (32 bits of data have been collected), the data is copied to the Receive Buffer and the receive-buffer-full flag is set in the video status register.

If PSYNC is configured to be an output, then PSYNC is used to indicate that the Video Interface is ready to accept data. PSYNC will be asserted 4 VCLK's after the video interface is enabled, and remain active until BlockHeight lines have been read in. Duplex mode and the Start-bit register have no effect in receive mode. The direction is always assumed to be forward.

Video Interrupts

The video interface is capable of generating interrupts for a number of different conditions. The user can select which conditions can cause an interrupt through use of the enable-mask bits in the video control register. The potential interrupt sources are:

- PSYNC de-asserted (only available for level PSYNC)
- End of Page
- Transmit FIFO empty/half–empty.
- Receive buffer full.

In order to receive interrupts after each chain block completes, the DMA channel 0 should be set into chaining test mode. (DMA Control Register bit 10).

Video Registers

LineWidth 16 bits, in dots (VCLKs)

The width of the printed image in VCLK's. When Line-Width is decremented down to zero, VDAT outputs blank-level from then to the end of the line. If any data remains in the shift-register when LineWidth reaches zero, that data is ignored. The LineWidth must be at least 1.

BlockHeight 16 bits, in LSYNC's

The number of lines in the printed image. This register is decremented for each LSYNC (after the top margin is skipped). When BlockHeight reaches zero, VDAT outputs blank-level data from that point to the end of the page. The BlockHeight must be at least 1.

TopMargin 16 bits, in LSYNC's

The number of lines to skip from the top of the page to the first line of the printed image. This value is decremented for every LSYNC received.

LeftMargin 16 bits, in VCLK's (dots)

The number of dots/VCLK's to skip from the edge of the page to the beginning of the printed image. The LeftMargin must be at least 1 for receiving and 2 for transmitting. There must be at least 2 VCLK's after the video data for the line is transmitted (at least a 2 VCLK right margin)

StartBit 5 bits, in dots (VCLK's)

This register defines which bit to start with when printing a line. The shift register is 32 bits wide, and this register specifies which bit will be the first bit shifted out. This start-bit applies to the beginning of each line. The valid settings are: not in duplex mode: 31, 23, 15, 7. in duplex mode: 0, 8, 16, 24.

Example (not duplex mode, 1 bit VDAT):

value = 31 means shift out all of the data in the shift register starting from bit 31 and continuing through bit 0.

value = 23 means start shifting from bit 23, through bit 0.

In duplex (reverse) mode:

value = 0 means shift out all of the data in the shift register starting from bit 0 and continuing through bit 31.

value = 8 means start shifting from bit 8, through bit 31.

Transmit FIFO register 32 bits

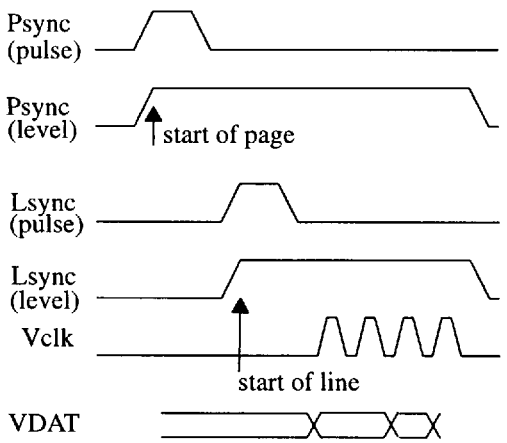
Read data from or write data to the transmit FIFO directly (without DMA). This register can be used to access the 8 word deep video transmit FIFO. Normally, the CPU would write 32-bit words to this buffer if DMA was not being used to send data to the print-engine.

Note: Reading from this register is only allowed while the video interface is disabled. Otherwise, the video interface and CPU would be competing for the data from the FIFO and the results would be unpredictable. Reading from the FIFO is primarily used for debugging purposes.

ReceiveBuffer register 32 bits

Read data from or write data to the receive buffer directly (without DMA). The receive buffer is 1 word deep (32 bits). When the shift register receives 32 bits of data, the data is transferred into this register to be read by the CPU. The status flag 'Receive Buffer Full' indicates that there is data to be read from this register.

Video Sync Signals



Note: Active high signals shown. Active polarity of the sync signals is programmable.

Video Control 1 and Video Control 2 32 bits

Bits:

- Video enable
- Video data direction (transmit/receive)
- DMA request enable
- IRQ enabled on PSYNC negated.
- IRQ enabled on End of Page.
- IRQ enabled on Transmit FIFO empty/half-empty
- IRQ enabled on Receive buffer full
- Transmit Fifo Threshold (half empty/empty)
- VCLK source: 0 = external, 1 = internal
- VCLK Drive out
- VCLK invert: 0 = normal, 1 = invert VCLK
- VCLK divide (1-16) (4 bits)
- PSYNC pulse/level (0 = level)
- LSYNC pulse/level (0 = level)
- PSYNC direction: 0 = input, 1 = output.
- PSYNC level: 0 = active low, 1 = active high

— LSYNC level: 0 = active low, 1 = active high
— VDAT blank level (data to output during blank areas)
— VDAT invert: 0 = normal, 1 = invert VCLK
— Duplex mode (reverse mode). 0 = forward, 1 = reverse (duplex)
— VDAT width: 00 = 1 bit, 01 = 4 bits. (2 bits) (in the future, 10 = 8 bits).
— Blank-page mode enable.

The control register is reset to 0.

VideoStatus 32 bits

Bits:

— Page Active
— Transmit FIFO full/not-full
— Receive Buffer full/empty
— DMA request active
— Video IRQ active
— LSYNC status
— PSYNC status
— End of Page

Note: To clear 'End of Page', '0' should be written to this register. Writing '0' will not affect the other bits in this register.

Video Signal Timing:

PSYNC and LSYNC are asynchronous inputs. PSYNC and LSYNC can be programmed to be treated as pulse-mode signals or level-mode signals. They can also be programmed to be active-high or active-low. Note: since these signals are asynchronous, they must be low noise signals.

In pulse mode, the positive edge of the signal is used as the active edge (unless the sync invert bit is set, in which case the negative signal edge is used). In level mode, LSYNC must be held active for the entire line, and PSYNC must be held active for the entire page (except in the case of video transmit abort and restart mode). PSYNC as an output is only available as a level signal.

External VCLK may be stopped (held low) at any time effectively suspending the video interface. VCLK must run at a lower frequency than the IU frequency. If VCLK is generated by the internal clock, the VCLK divisor must be set to at least 2.

LSYNC and PSYNC (as an input) must provide substantial setup and hold time with respect to the active edge of VCLK. See AC Timing for details.

DRAM CONTROLLER

The MB86936 provides all the necessary logic to directly connect up to 16MB of fast paged-mode DRAM to the MB86936 without external buffering. Address multiplexing is performed internally and the DRAM address (MA<11:0>) is output on ADR<13:2>. Four –RAS lines can access up to four banks of memory, each bank is configurable in size and width. Optional sixteen bit wide data is supported for implementing low initial cost systems. But for maximum performance, a 32-bit memory width is recommended.

An internal refresh interval timer is used to generate a –CAS before –RAS refresh cycle automatically at programmable intervals. The bank size and address muxing is programmable to accomodate a wide choice of DRAM types and memory size. Up to a total of 64MB of memory per bank can be supported if external buffers are used.

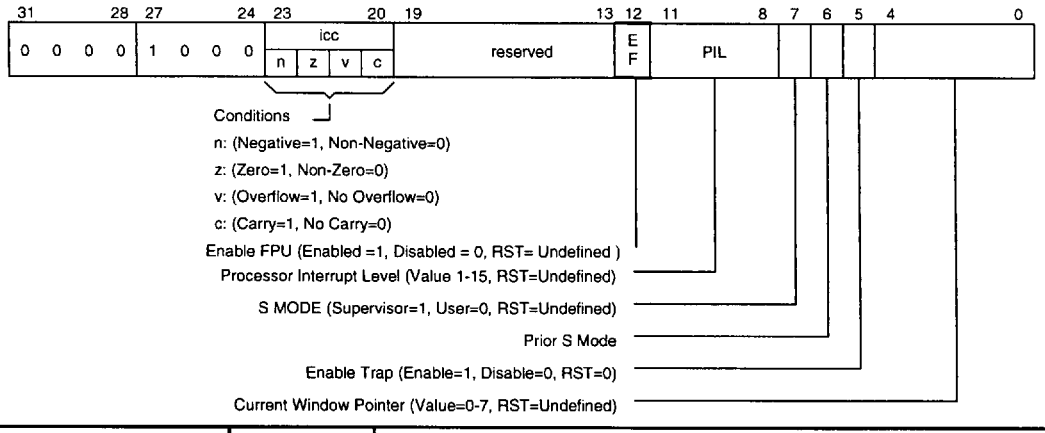
The DRAM Controller uses the internal clock to obtain finer resolution in the DRAM control signals in high frequency operations, when the bus clock frequency is half the internal clock frequency. To support a wide range of operating frequencies and DRAM latencies and to optimize the memory access time, the timing relationships of the DRAM address, –RAS, –CAS, and –DWE signals are programmable by writing the DRAM Timing Registers.

The following parameters are programmable.

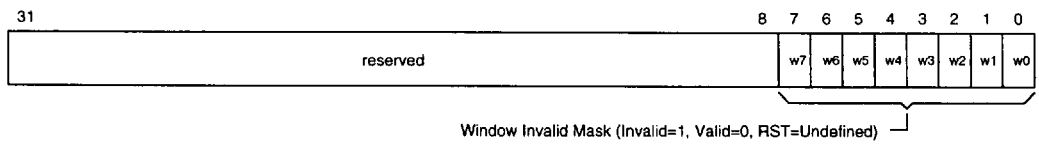
- t_{ASR} — the leading edge of –RAS may be programmed to fall one to four internal clock cycles after the row address change to provide the address to –RAS setup time.
- t_{RAH} — row address hold time. The row address to column address switching may be set to change one to four internal clock cycles after –RAS falls to satisfy the row address hold time requirement.
- t_{ASC} — column address setup time. –CAS falls one to four internal clock cycles after the row/column address change to provide the address to –CAS setup time.
- t_{CAS} — –CAS pulse width. –CAS is held active for one to four internal clock cycles after leading edge of –CAS.
- t_{CP} — –CAS pre-charge time. The –CAS pre–charge time is programmable from one to four internal clock cycles after –CAS goes high.
- t_{WCS}, t_{RCS} — Write/Read command setup time.
- t_{RP} — –RAS pre-charge time. The –RAS pre–charge time is programmable from one to four internal clock cycles.
- t_{CSR} — –CAS to –RAS setup time for –CAS before –RAS refresh (CBR) refresh. one to four internal clock cycles.
- t_{CHR} — –CAS to –RAS hold time for CBR refresh., one to four internal clock cycles.
- t_{RAS} — (CBR Refresh) –RAS pulse width.

TABLE 2. MB86936 Control and Status Registers (All registers are read/write)

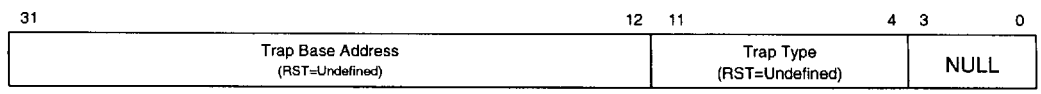
Processor State Register | **PSR**



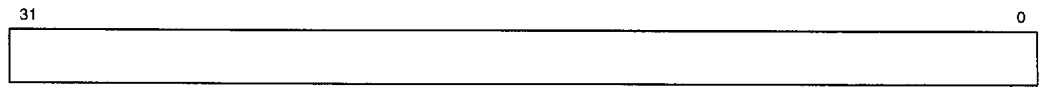
Window Invalid Mask | **WIM**



Trap Base Register | **TBR**



Y Register | **Y**



Ancillary State Register 17 | **ASR 17**

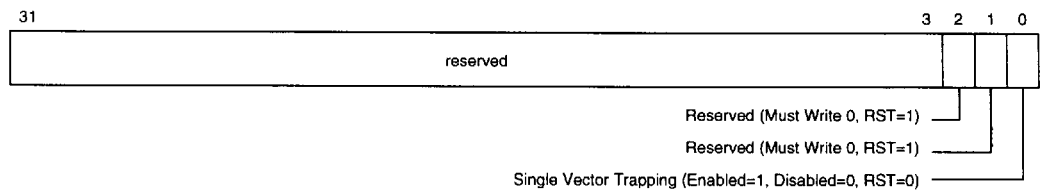
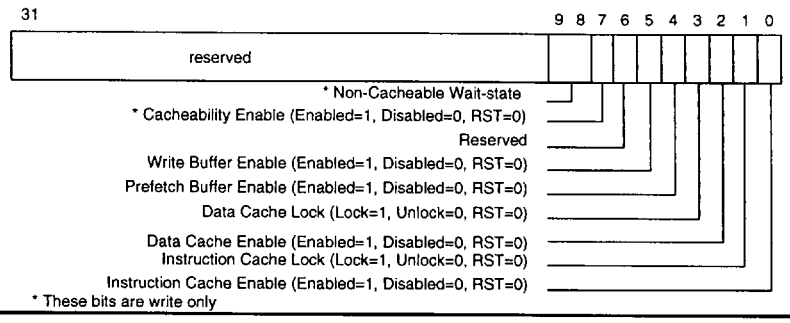
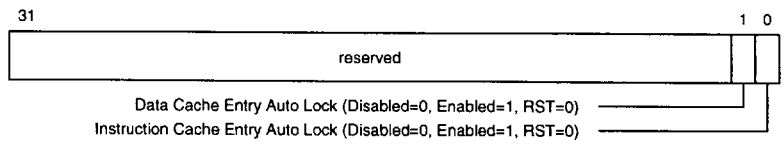


TABLE 3. MB86936 Memory Mapped Control Registers (All registers are read/write)

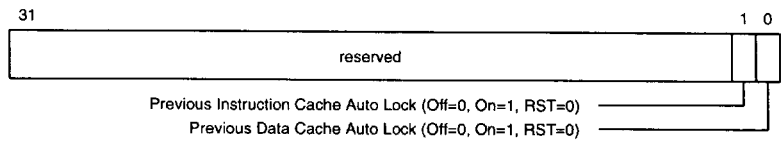
Cache/BIU Control	
ASI	**ADDRESS**
0x 1	0x 0000 0000



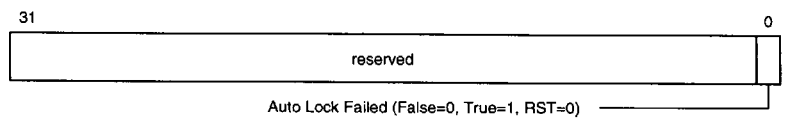
Lock Control	
ASI	**ADDRESS**
0x 1	0x 0000 0004



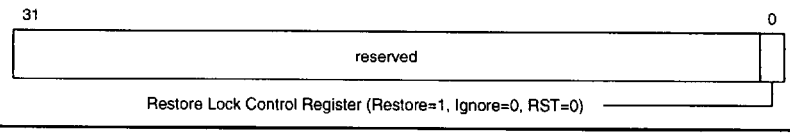
Lock Control Save	
ASI	**ADDRESS**
0x 1	0x 0000 0008



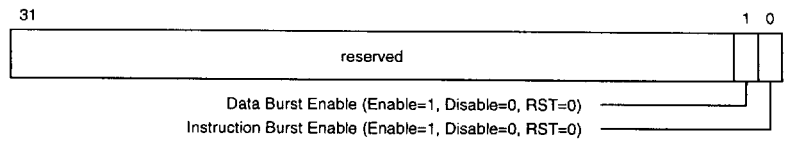
Cache Status	
ASI	**ADDRESS**
0x 1	0x 0000 000C



Restore Lock Control	
ASI	**ADDRESS**
0x 1	0x 0000 0010



Bus Control	
ASI	**ADDRESS**
0x 1	0x 0000 0020



System Support Control	
ASI	**ADDRESS**
0x 1	0x 0000 0080

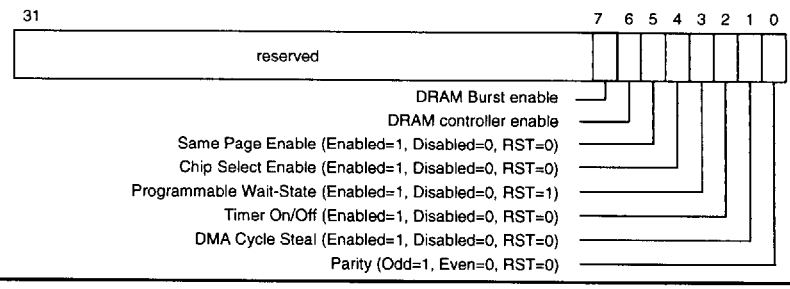
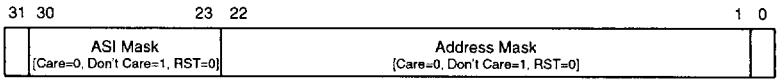


TABLE 3. MB86936 Memory Mapped Control Registers (continued)

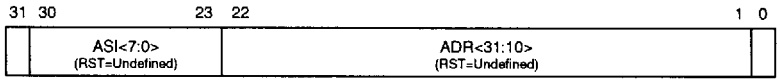
Same Page Mask

ASI	ADDRESS
0x 1	0x 0000 0120



Address Range[1]

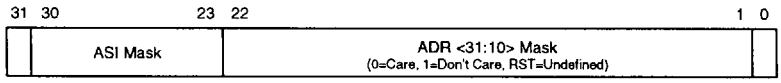
ASI	ADDRESS	
0x 1	CS1	0x 0000 0124
	CS2	0x 0000 0128
	CS3	0x 0000 012C
	CS4	0x 0000 0130
	CS5	0x 0000 0134



NOTE: CS0 is hardwired to ASI=0x9 ADR<31:10> = <0..0>

Address Mask

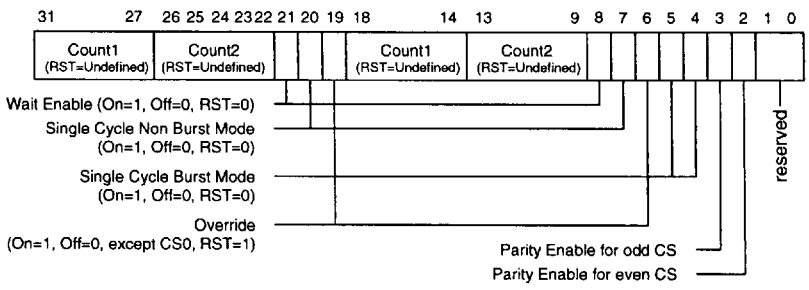
ASI	ADDRESS	
0x 1	CS0	0x 0000 0140
	CS1	0x 0000 0144
	CS2	0x 0000 0148
	CS3	0x 0000 014C
	CS4	0x 0000 0150
	CS5	0x 0000 0154



NOTE: CS0 ADR<14:10> = 1, ADR<31:15> = 0, ASI = 0x9 at reset.

Wait State Specifier

ASI	ADDRESS	
0x 1	CS1,CS0	0x 0000 0160
	CS3,CS2	0x 0000 0164
	CS5,CS4	0x 0000 0168

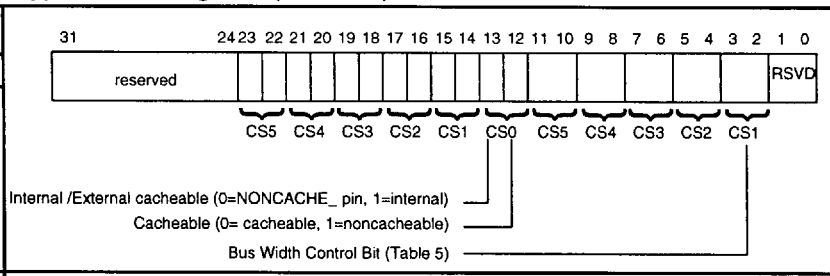


1. This register is Write Only

TABLE 3. MB86936 Memory Mapped Control Registers (continued)

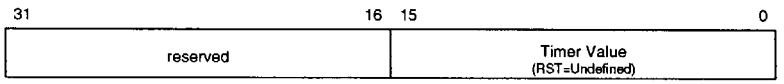
Bus Width and Cacheable

ASI	ADDRESS
0x 1	0x 0000 016C



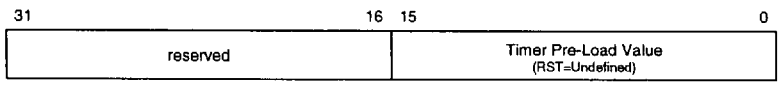
DRAM Refresh Timer

ASI	ADDRESS
0x 1	0x 0000 0174



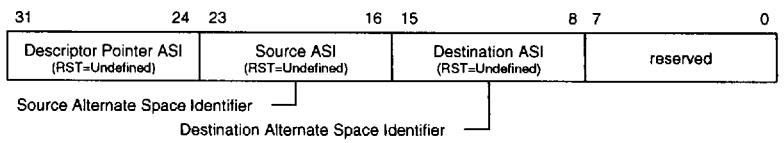
DRAM Refresh Timer Pre-Load

ASI	ADDRESS
0x 1	0x 0000 0178



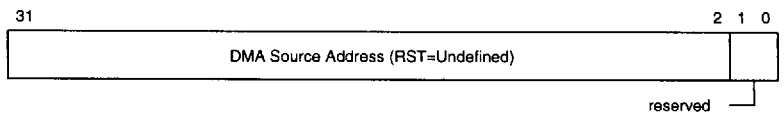
Source/Destination ASI

ASI	ADDRESS	
0x 1	0x 0000 0180	DMA0
	0x 0000 01A0	DMA1
	0x 0000 01C0	DMA2



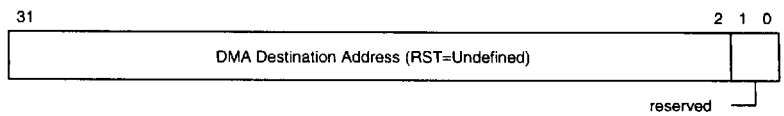
Source Address

ASI	ADDRESS	
0x 1	0x 0000 0184	DMA0
	0x 0000 01A4	DMA1
	0x 0000 01C4	DMA2



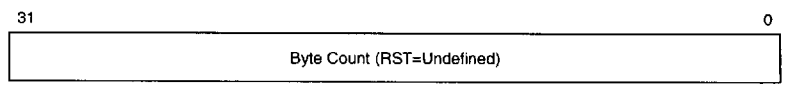
Destination Address

ASI	ADDRESS	
0x 1	0x 0000 0188	DMA0
	0x 0000 01A8	DMA1
	0x 0000 01C8	DMA2



Byte Count

ASI	ADDRESS	
0x 1	0x 0000 018C	DMA0
	0x 0000 01AC	DMA1
	0x 0000 01CC	DMA2



Descriptor Pointer

ASI	ADDRESS	
0x 1	0x 0000 0190	DMA0
	0x 0000 01B0	DMA1
	0x 0000 01D0	DMA2

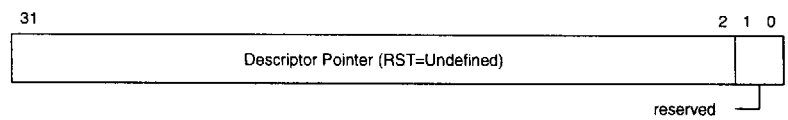
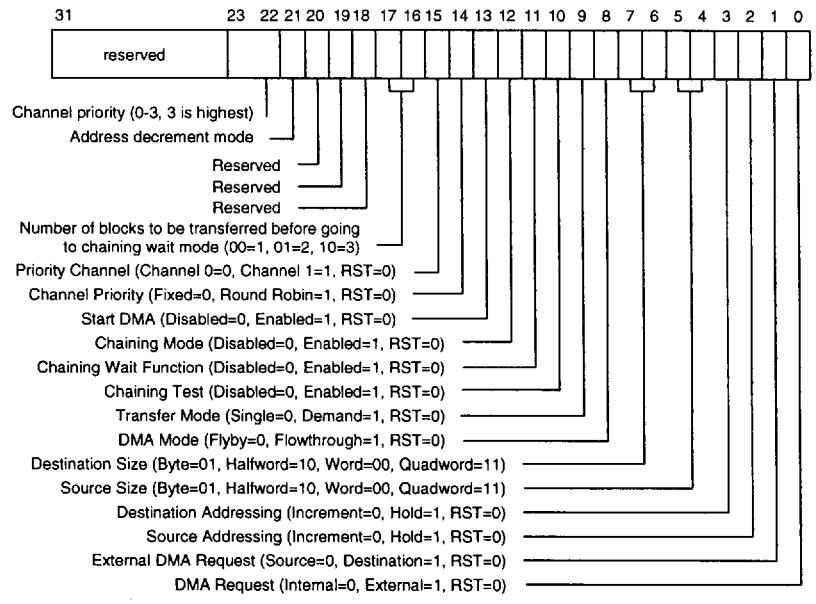


TABLE 3. MB86936 Memory Mapped Control Registers (continued)

Channel Control

ASI	ADDRESS
0x 1	0x 0000 0194 DMA0 0x 0000 01B4 DMA1 0x 0000 01D4 DMA2



Channel Status

ASI	ADDRESS
0x 1	0x 0000 0198 DMA0 0x 0000 01B8 DMA1 0x 0000 01D8 DMA2 ASR 0x18 DMA0 ASR 0x19 DMA1

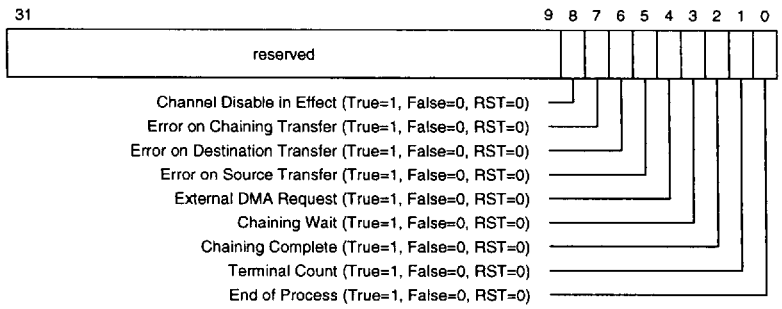
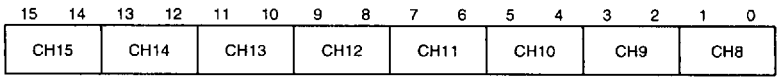
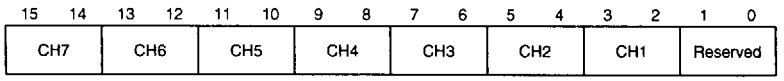


TABLE 3. MB86936 Memory Mapped Control Registers (continued)

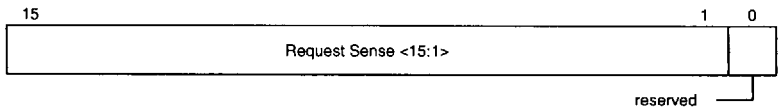
Trigger Mode 0	ASI: 0x 1	ADDRESS: 0x 0000 0200



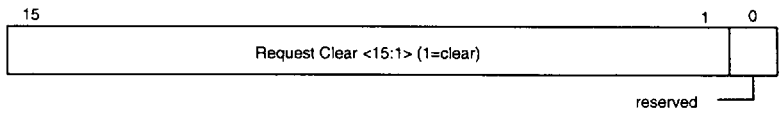
Trigger Mode 1	ASI: 0x 1	ADDRESS: 0x 0000 0204



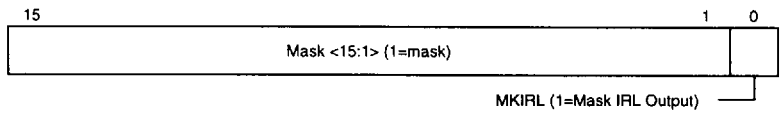
Request Sense[2]	ASI: 0x 1	ADDRESS: 0x 0000 0208



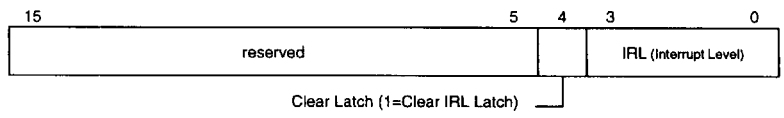
Request Clear[1]	ASI: 0x 1	ADDRESS: 0x 0000 020C



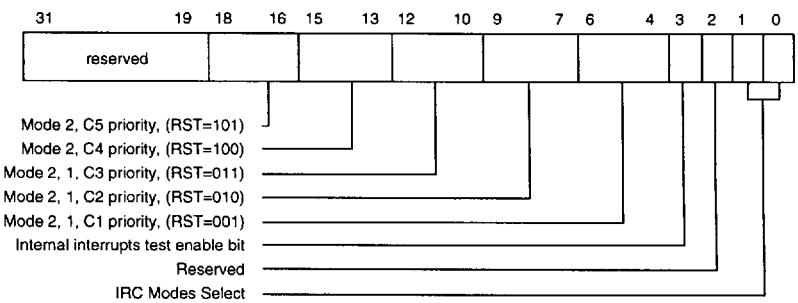
Mask	ASI: 0x 1	ADDRESS: 0x 0000 0210



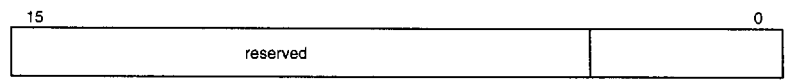
Latch Clear	ASI: 0x 1	ADDRESS: 0x 0000 0214



IRC Mode Select	ASI: 0x 1	ADDRESS: 0x 0000 0218

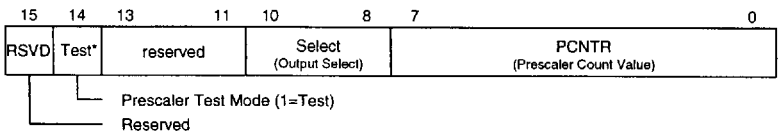
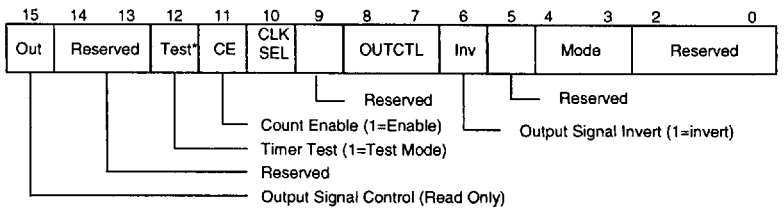
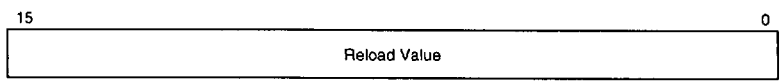
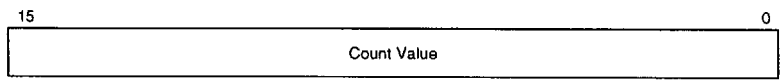
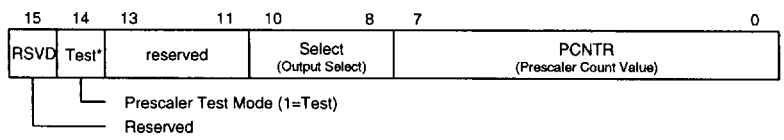
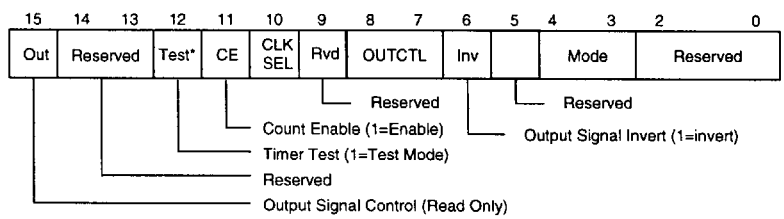
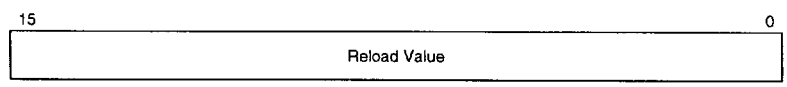
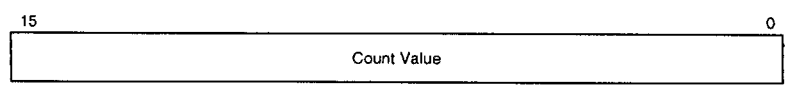


IRC	ASI: 0x 1	ADDRESS: 0x 0000 021C



1. This register is Write Only.
2. This register is Read Only.

TABLE 3. MB86936 Memory Mapped Control Registers (continued)

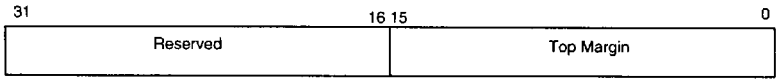
Prescaler 0 ASI: 0x 1 ADDRESS: 0x 0000 0240	
Timer Control 0 ASI: 0x 1 ADDRESS: 0x 0000 0244	
Reload 0 ASI: 0x 1 ADDRESS: 0x 0000 0248	
Count 0 [1] ASI: 0x 1 ADDRESS: 0x 0000 024C	
Prescaler 1 ASI: 0x 1 ADDRESS: 0x 0000 0250	
Timer Control 1 ASI: 0x 1 ADDRESS: 0x 0000 0254	
Reload 1 ASI: 0x 1 ADDRESS: 0x 0000 0258	
Count 1 [1] ASI: 0x 1 ADDRESS: 0x 0000 025C	

*test mode is active when global test bit is enabled. Global test bit is enabled by performing store alternate at address 0x 10000 (asi=0x1) and data 0x1.

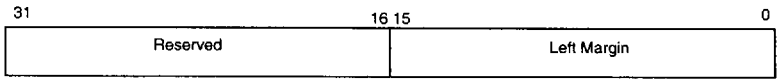
1. This register is Read Only.

TABLE 3. MB86936 Memory Mapped Control Registers (continued)

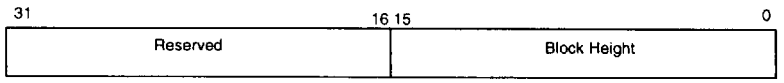
Top Margin	
ASI	**ADDRESS**
0x 1	0x 0000 0280



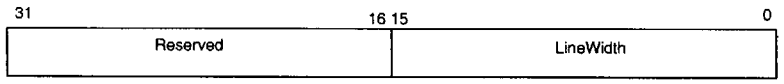
Left Margin	
ASI	**ADDRESS**
0x 1	0x 0000 0284



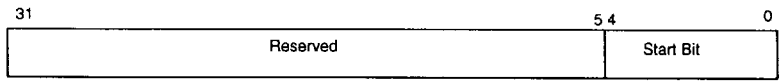
Block Height	
ASI	**ADDRESS**
0x 1	0x 0000 0288



Line Width	
ASI	**ADDRESS**
0x 1	0x 0000 028C



Start Bit	
ASI	**ADDRESS**
0x 1	0x 0000 0290



Video Control 1	
ASI	**ADDRESS**
0x 1	0x0000 0294

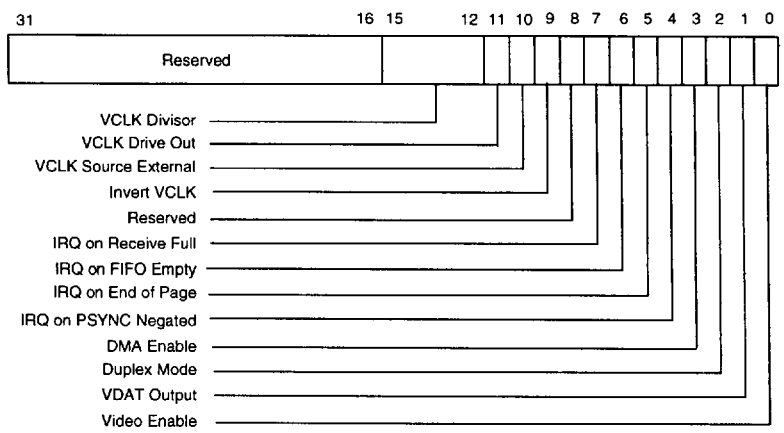
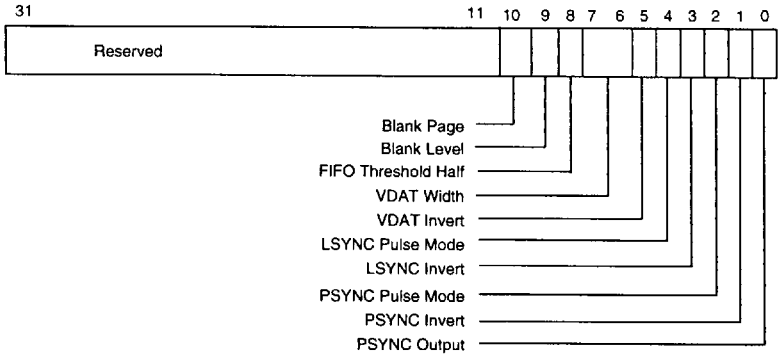
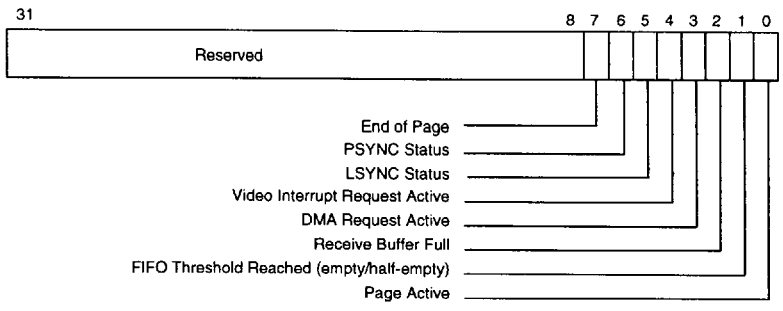


TABLE 3. MB86936 Memory Mapped Control Registers (continued)

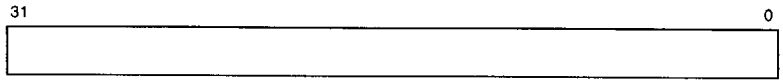
Video Control 2	
ASI	**ADDRESS**
0x 1	0x0000 0298



Video Status	
ASI	**ADDRESS**
0x 1	0x0000 029C



Transmit FIFO	
ASI	**ADDRESS**
0x 1	0x0000 02A0



Receive Buffer	
ASI	**ADDRESS**
0x 1	0x0000 02A4

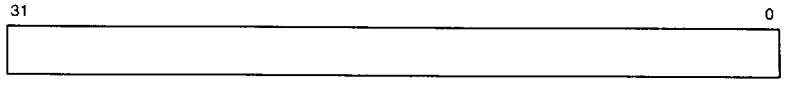
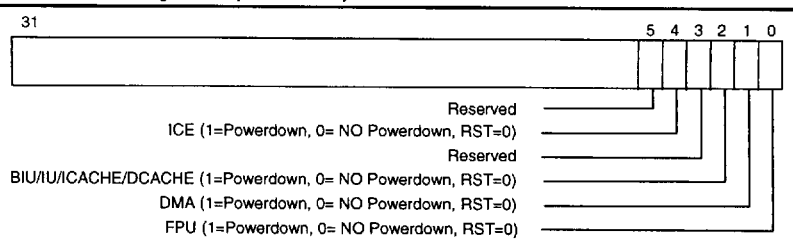
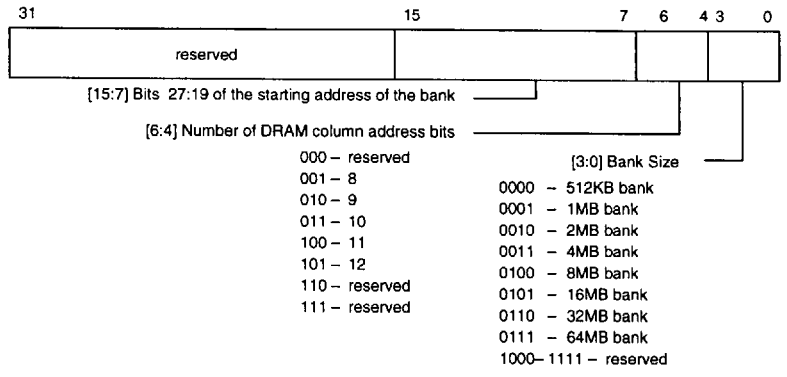


TABLE 3. MB86936 Memory Mapped Control Registers (continued)

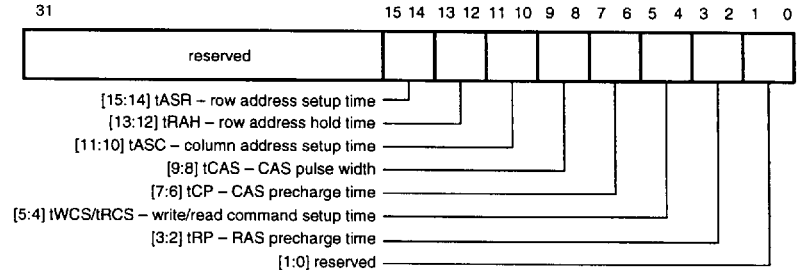
Power Down Control	
ASI	**ADDRESS**
0x 1	0x0000 0060



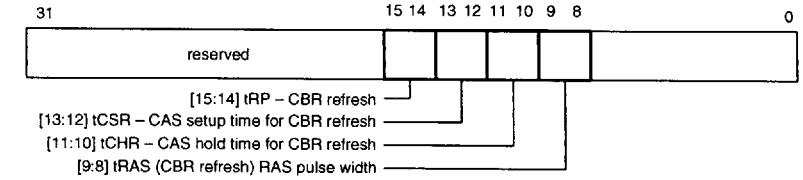
DRAM Bank Configuration	
ASI	**ADDRESS**
0x 1	bank 0: 0x 0000 07D0 bank 1: 0x 0000 07D4 bank 2: 0x 0000 07D8 bank 3: 0x 0000 07DC



DRAM Timing Register I	
ASI	**ADDRESS**
0x 1	0x 0000 07E0



DRAM Timing Register II	
ASI	**ADDRESS**
0x 1	0x 0000 07E4



Reserved	
ASI	**ADDRESS**
0x 1	0x0000 07E8- 0x 0000 07FC

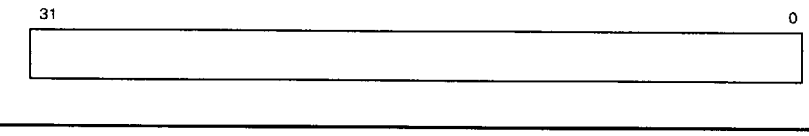
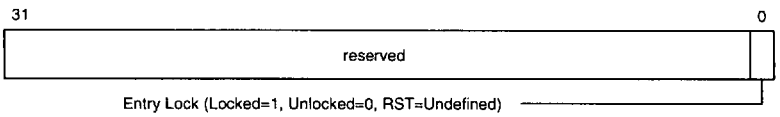


TABLE 3. MB86936 Memory Mapped Control Registers (continued)

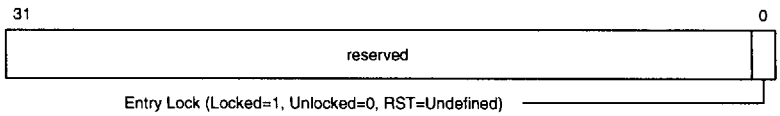
InstructionTag Lock Bits

ASI	ADDRESS
0x 2	Bank 1 0x 0000 0000 ↓ by 8 0x 0000 07F8 Bank 2 0x 8000 0000 ↓ by 8 0x 8000 07F8



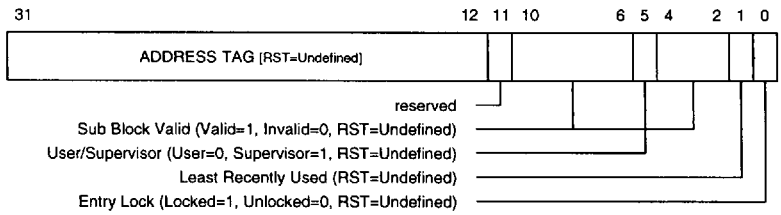
Data Tag Lock Bits

ASI	ADDRESS
0x 3	Bank 1 0x 0000 0000 ↓ by 4 0x 0000 03FC Bank 2 0x 8000 0000 ↓ by 4 0x 8000 03FC



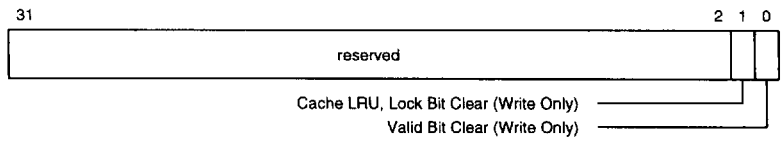
Instruction Cache Tag

ASI	ADDRESS
0x C	Bank 1 0x 0000 0000 ↓ by 8 0x 0000 07F8 Bank 2 0x 8000 0000 ↓ by 8 0x 8000 07F8



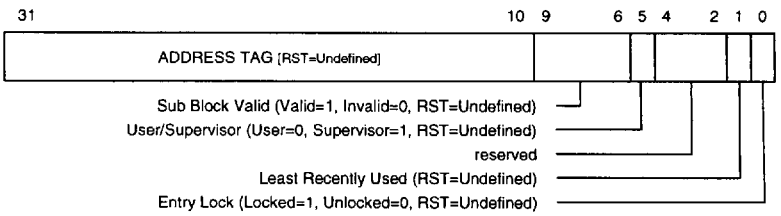
Instruction Cache Invalidate

ASI	ADDRESS
0x C	Bank 1 0x 0000 1000 Bank 2 0x 8000 1000



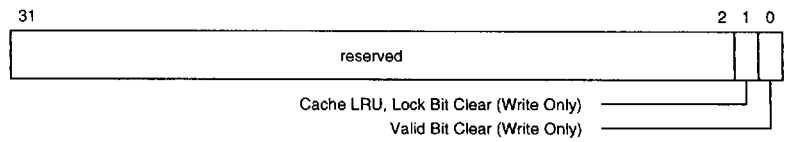
Data Cache Tag

ASI	ADDRESS
0x E	Bank 1 0x 0000 0000 ↓ by 4 0x 0000 03FC Bank 2 0x 8000 0000 ↓ by 4 0x 8000 03FC



Data Cache Invalidate

ASI	ADDRESS
0x E	Bank 1 0x 0000 1000 Bank 2 0x 8000 1000



BUS OPERATION

The Bus Interface Unit (BIU) has the logic which allows the MB86936 to interface with the system. The system interface is made up of the address and data buses, the interrupt request bus and various control signals. The BIU is either handling requests for external memory operations, arbitrating for bus access, or idle.

Operation of the BIU

In the case of a write to external memory, the BIU makes use of a write buffer which can hold a four word write transaction. When the BIU receives a request for a write transaction it stores the write data and address in the write buffer allowing the IU to continue operating out of on-chip cache and/or its register file. The BIU then proceeds to complete the write to external memory. In most cases the write buffer will hide external memory latency from the IU. The exceptions are in cases where the write buffer is still filled from a previous transaction or if the subsequent IU cycle results in an instruction cache or data cache read miss. In these cases, IU execution is held until the write buffer is emptied.

The write buffer operates only when both the instruction and data caches are on. When the bus is granted to an external bus master, a store to the write buffer does not cause the assertion of –PBREQ. This allows the external bus master to continue operating while MB86936 is executing out of the internal caches.

The BIU includes a one stage prefetch buffer for instruction fetches. This buffer is used to fetch the next sequential instruction after an instruction cache miss. The instruction is prefetched only if the BIU does not have a request for a bus transaction from the IU nor is any external device requesting use of the bus. The prefetch buffer operation is suspended if the buffer is full. This occurs if the prefetched instruction is a hit in the instruction cache. The buffer restarts after another instruction cache miss. If an exception occurs during an instruction prefetch, the exception is not sent to the IU unless the instruction is actually requested by the IU. The prefetch buffer operates only when the instruction cache is on.

In any cycle the BIU can receive a request for accesses to either or both instruction and/or data memory. If it receives a request for both in the same cycle, it completes the data memory transaction first.

Exception Handling

The external memory system can indicate an exception during a memory operation. Parity errors cause an exception as well. The BIU signals the appropriate data or instruction exception to the IU which will trap accordingly.

As mentioned above, the IU can continue operation after putting the data and address for a store in the write buffer. If an exception is detected while completing this buffered write, then the BIU indicates a data access exception to the IU.

Any system which needs to recover from this error should store the address and data of such write transactions in hardware. If the system can generate both read and write exceptions, then the system must also provide a status bit which indicates whether the exception was generated on a read or on a write transaction. With access to this information the data access exception service routine can determine the cause of the exception and recover accordingly.

If the MB86936 write buffer is turned on, an exception can potentially cause other exceptions due to the flush of 4 deep write buffer. The system which needs to recover from any one of this exception needs to store four seperate sets of address and data.

Bus Cycles

Timings 1 through 10 illustrate representative combinations of bus cycles.

Load

Regardless of the external bus size (8, 16, or 32 bits), all instruction fetches and loads (including load byte and load half word) retrieve a 32–bit quantity. This is done for compatibility with MB8693x processors with data cache where the smallest granularity in the cache is one word. Bus sizes can be programmed based on chip select regions to be 8, 16, or 32 bit wide.

Load (32–bit wide bus)

Whenever a load from data memory is requested or an instruction cache miss occurs, the BIU performs a read from external memory (see Timing 1).

With a 32–bit external data bus, a read transaction begins with the BIU asserting –AS, to indicate a new bus transaction. The –AS signal is de–asserted after one cycle. At the same time the ADR< 27:2 > and ASI< 3:0 > bits are driven with the location to be read. The BIU drives the RD/–WR signal high to indicate a read transaction. Since all loads retrieve 32 bits, –BE<0:3> are not used when the bus is 32–bit wide and are all driven low.

The external memory system responds with the read data on pins D< 31:0 >. It also asserts the –READY signal when the data is ready. For slow memory, the –READY signal can be delayed until data is valid.

A load double operation is treated as back–to–back reads.

Load (16–bit wide bus)

When the bus is programmed to be 16 bits wide (defined by the chip select region) every load will retrieve 32–bits.

Timing diagram 11. shows a load (Byte, half word, word) operating with an 16–bit bus. For the ldb and ldh the IU masks off the bits which are not required. For a 16–bit bus the –BE<2> pin is defined to be the ADR<1> address bit. –BE<2> as well as BE<0:1> are unused and are driven low.

Load (8–bit wide bus)

When the bus is programmed to be 8 bits wide (defined by the chip select region) every load will retrieve 32–bits. Timing diagram 7. shows a load (Byte, half word, word) operating with an 8–bit bus. For the ldb and ldh the IU masks off the bits which are not required. For a 8–bit bus –BE<2:3> are the ADR<1:0> address bits. –BE<0:1> are unused and are driven low.

Load with Exception

If the external memory system sees a memory exception it can terminate the current memory transaction by asserting the –MEXC and –READY signals. The data on the data bus is ignored by the MB86936.

Store

Unlike loads, MB86936 requires only the minimum number of bus cycles to complete the store. For example, only two bus cycles are required to do a half–word store on a 8–bit bus.

Store (32–bit wide bus)

A write transaction begins with the BIU asserting –AS, to indicate a new bus transaction. The –AS signal is de–asserted after one phase. At the same time the ADR <27:2> and ASI <3:0> pins are driven with the location to be written while the D <31:0> pins has corresponding write data. The –BE<0:3> are the high to low order byte enables, respectively and indicate which bytes to write for a given type of store operation (byte, half–word or word). The BIU drives the RD/–WR signal low to indicate a write transaction.

The external memory system responds by asserting the –READY signal when it has stored the data. Or, if the internal wait state generator is enabled, –READY is generated internally to the MB86936.

A store double operation is treated as back–to–back writes.

Store (16–bit wide bus)

Stores to 16–bit memory are sized to the bus. That is, for a 16–bit bus, a store word requires two cycles while a store halfword or store byte requires a single cycle. Timing diagram 8. to timing diagram 10. show the timing for different types of stores. For a 16–bit bus, the –BE<2> is defined to be ADR<1>. –BE<3> is unused and is driven low. –BE<1:0> are defined to be the high and low order byte enables, respectively.

Store (8–bit wide bus)

Stores to 8–bit memory are sized to the bus. That is, for a 8–bit bus, a store word requires four cycles, a store halfword requires two cycles, and store byte requires a single cycle. Timing diagram 12. and timing diagram 13. show the timing for different types of stores. For a 8–bit bus, the –BE<2:3> are defined to be ADR<1:0>. –BE<1:0> are unused and are driven low.

Clock Doubler Load and Store

When MB86936 is executing in clock doubler mode, the ADR<27:2> can be available half a cycle before –AS, –ASI, D<31:0>, and –BE<0:3>. This is to make ADR<27:2> available before –RAS and –CAS are asserted.

Store with Exception

If an access exception occurs on a write, the external memory system can terminate the current memory transaction by asserting the –MEXC and –READY signals. The external memory system is expected to ignore the data on the data bus in this situation.

Atomic Load Store

An atomic load store executes as a load followed by a store with no operation allowed in between. The –LOCK signal is asserted to indicate that the bus is being used for more than one external memory operation.

There is one cycle between the termination of the read and the beginning of the write to provide time for the switching of the data bus drivers.

External Bus Request and Grant

Any external device can request ownership of the bus by asserting the –BREQ signal. The BIU asserts the –BGRNT signal to indicate that it is relinquishing control of the bus and also three-states all of its bus drivers. In the following cycle, the external device can begin its transaction. On completion of its transaction the external device de-asserts the –BREQ signal. The BIU responds by de-asserting the –BGRNT signal in the following cycle.

A separate signal, –PBREQ, is asserted by the processor to indicate to a bus arbiter that it needs the bus back. This allows the bus to be allocated based on demand. The signal, –PBREQ, is asserted when the write buffer is full or MB86936 is doing an instruction or data fetch.

The MB86936 is the default owner of the bus.

8-Bit and 16-Bit Bus Modes

The MB86936 supports any chip select (–CS0 to –CS5) to be mapped into memory that can be either 8, 16, or 32-bits wide. Memory width for –CS0 is selected at

system reset. Table 4 shows the selection mode of bus width for –CS0. Memory width for –CS1 to –CS5 is selected by programming two bits for each chip select in a control register (ASI=0x01, Address=0x0000 016C). Table 5 shows the programming bits and the corresponding bus width of each chip select (–CS1 to –CS5).

Table 4. Bus Width Control of –CS0

–BMODE16	–BMODE8	Bus Width
0	0	Illegal
0	1	16 bit Memory Bus
1	0	8 bit Memory Bus
1	1	32 bit Memory Bus

Table 5. Bus Width Control Bits of –CS1 to –CS5

BW1	BW0	Bus Width
0	0	32 bit Memory Bus
0	1	8 bit Memory Bus
1	0	16 bit Memory Bus
1	1	Illegal

Transactions of 8 and 16-bit widths are similar to 32-bit transactions except that –AS is asserted only once at the beginning of the bus cycle for a load operation and –READY is asserted after each byte or halfword is available. –BE<0:3> indicates the byte or halfword being read or written (see Timing diagrams 7 and 8 for load from 8/16-bit memory).

For 32-bit write to 8 or 16-bit memory and 16-bit write to 8-bit memory, the BIU drives –BE<2:3> as ADR<1:0>, and initiates multiple transactions.

When the internal DRAM controller is turned on, MB86936 supports 8, 16, 32–bit memory bus on –CS0 to –CS3, and only 16 and 32–bit memory bus on –CS4, depending on the DRAM bus width.

Burst Mode Transactions

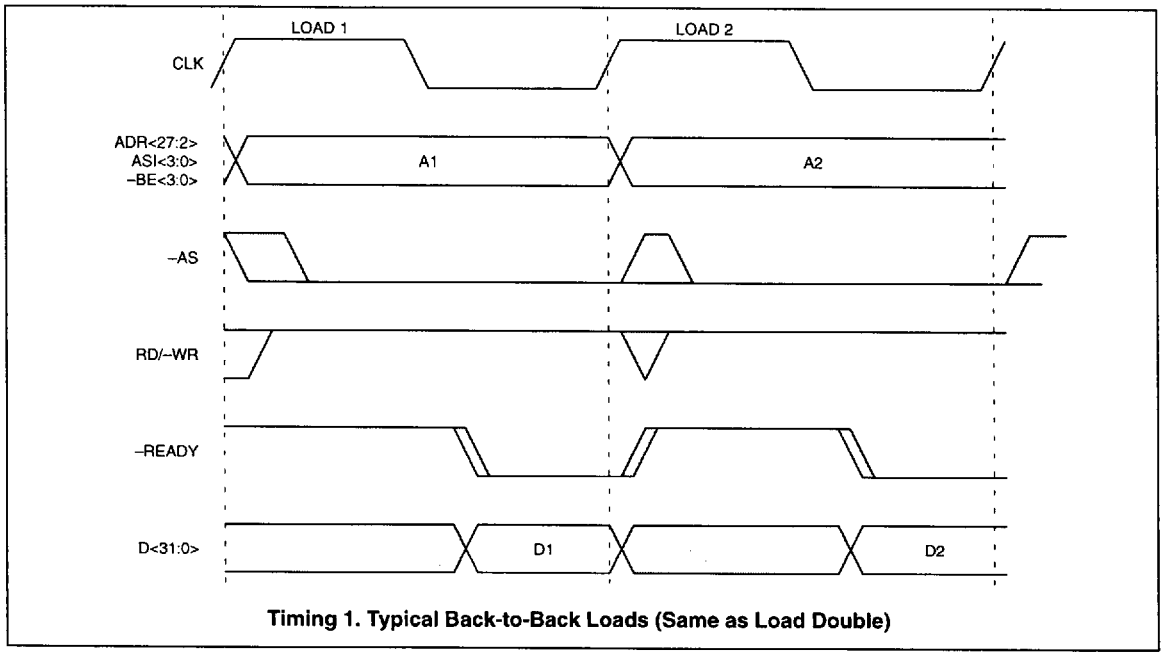
For systems that can support burst mode transactions, the MB86936 can be programmed to support 4 word bursts. When burst mode is enabled, –BMREQ is asserted at the beginning of each bus cycle for which a burst access can be done (see timing diagram 14). If the memory system can support a burst for the current bus address, it asserts –BMACK to begin the burst transaction. –BMACK is asserted on the first word of the burst transaction only. –READY is asserted with each word of the burst. Systems that do not support burst mode for the current address should not assert –BMACK (see timing diagram 15). If –BMREQ is not asserted for a transaction the memory should return only one word.

Table 6. ADR[3:2] sequence on burst mode

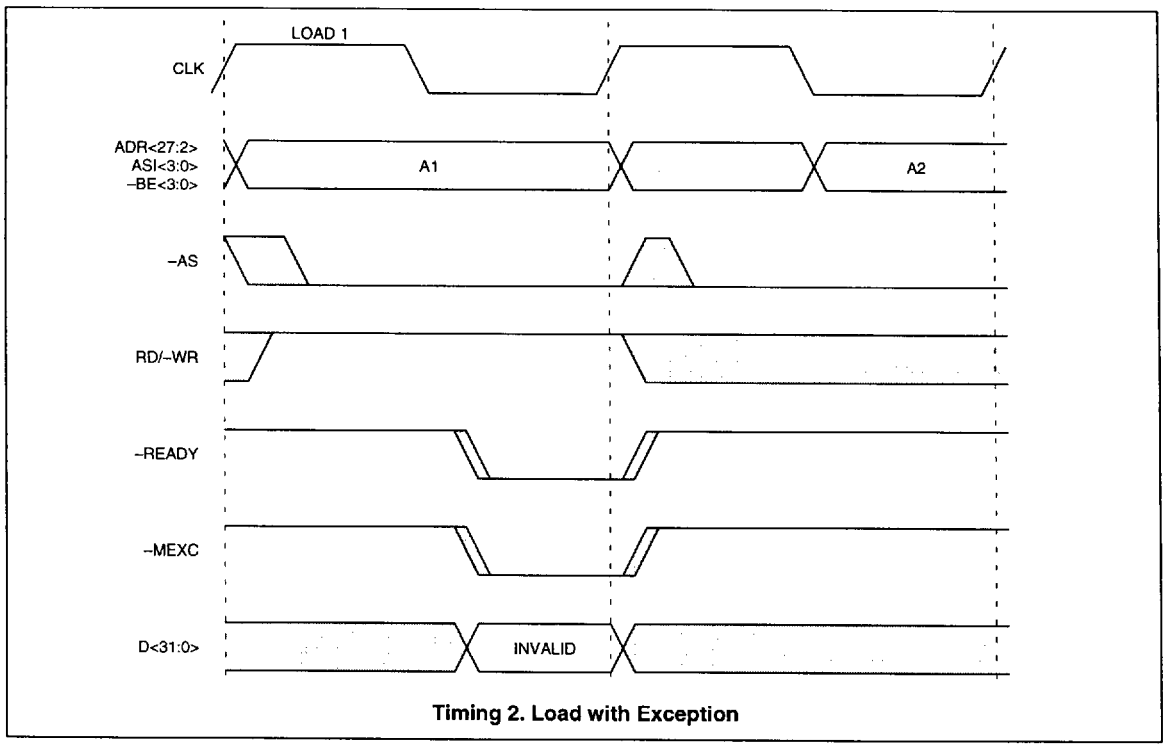
bus cycle 1	bus cycle 2	bus cycle 3	bus cycle 4
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

Direct Memory Access

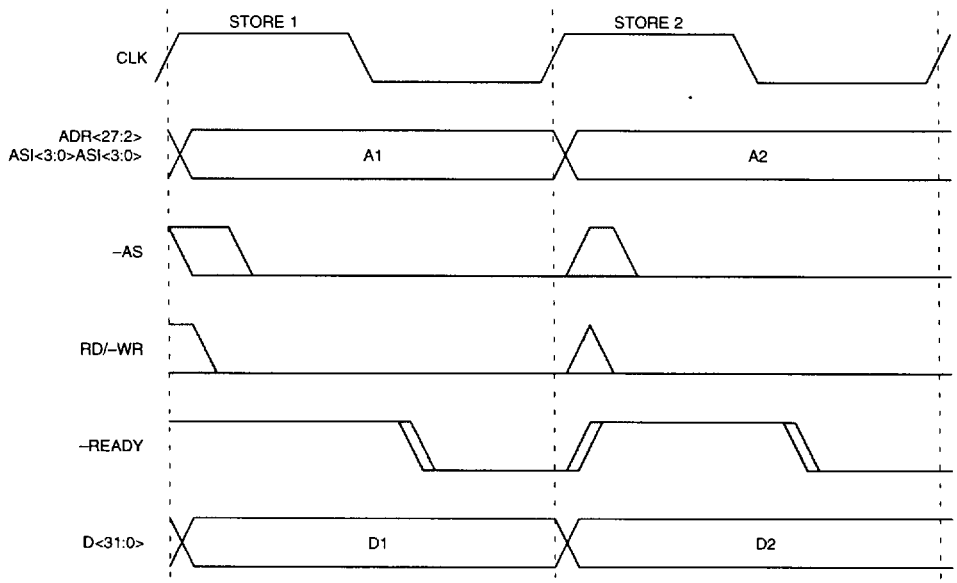
For systems that can support burst mode transactions, the MB86936 can support a number of different DMA modes. (See timing diagrams 16 through 22 for details.)



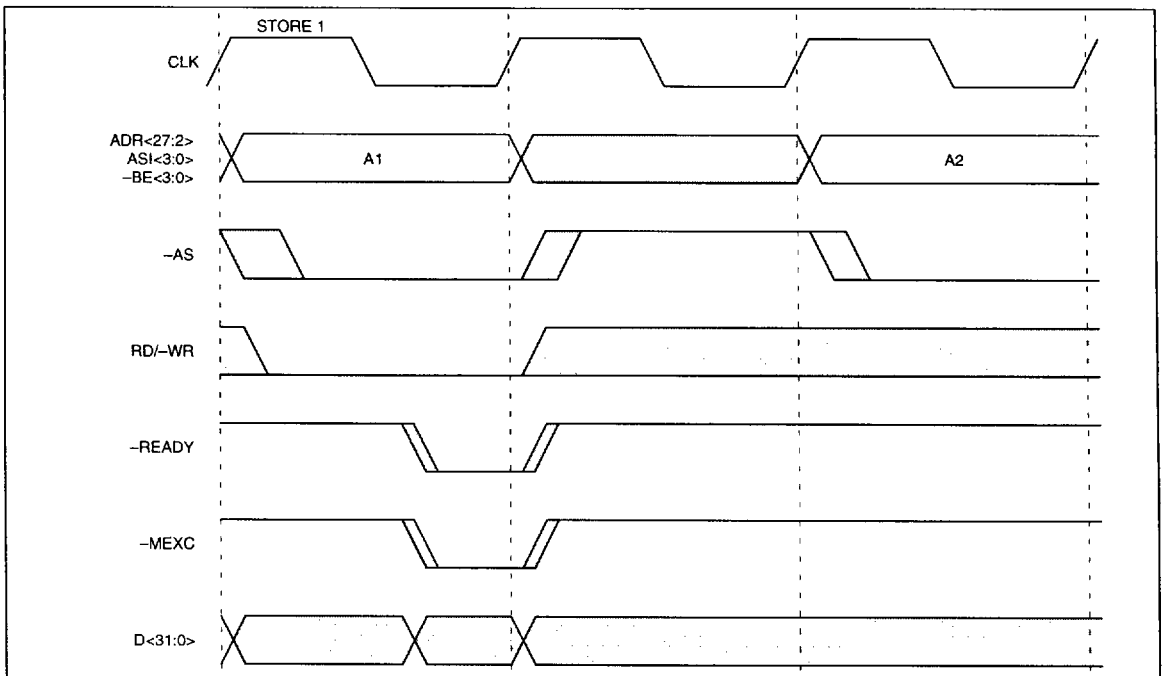
Timing 1. Typical Back-to-Back Loads (Same as Load Double)



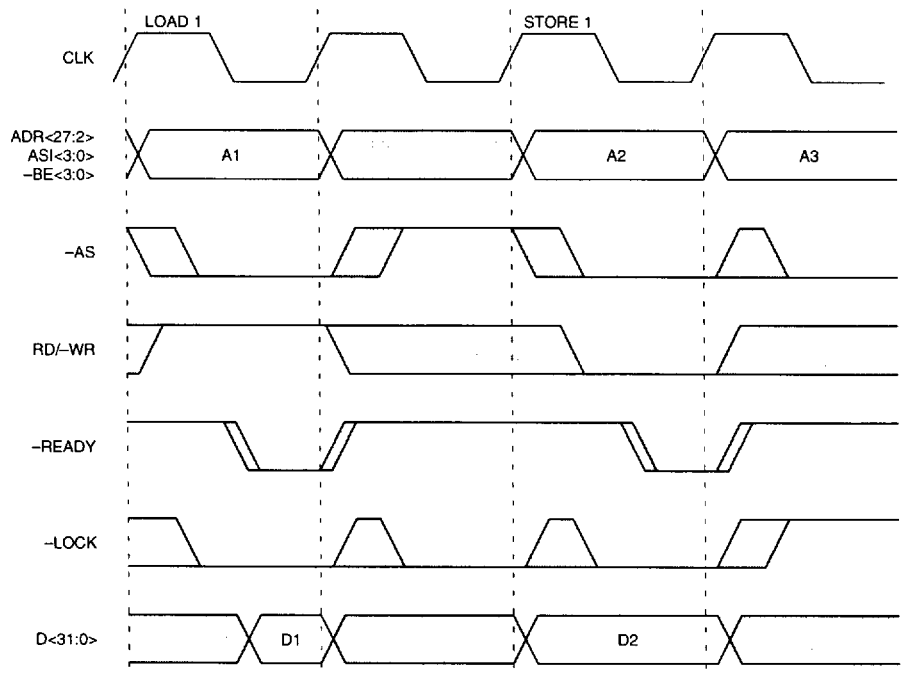
Timing 2. Load with Exception



Timing 3. Typical Back-to-Back Stores (Same as Store Double)

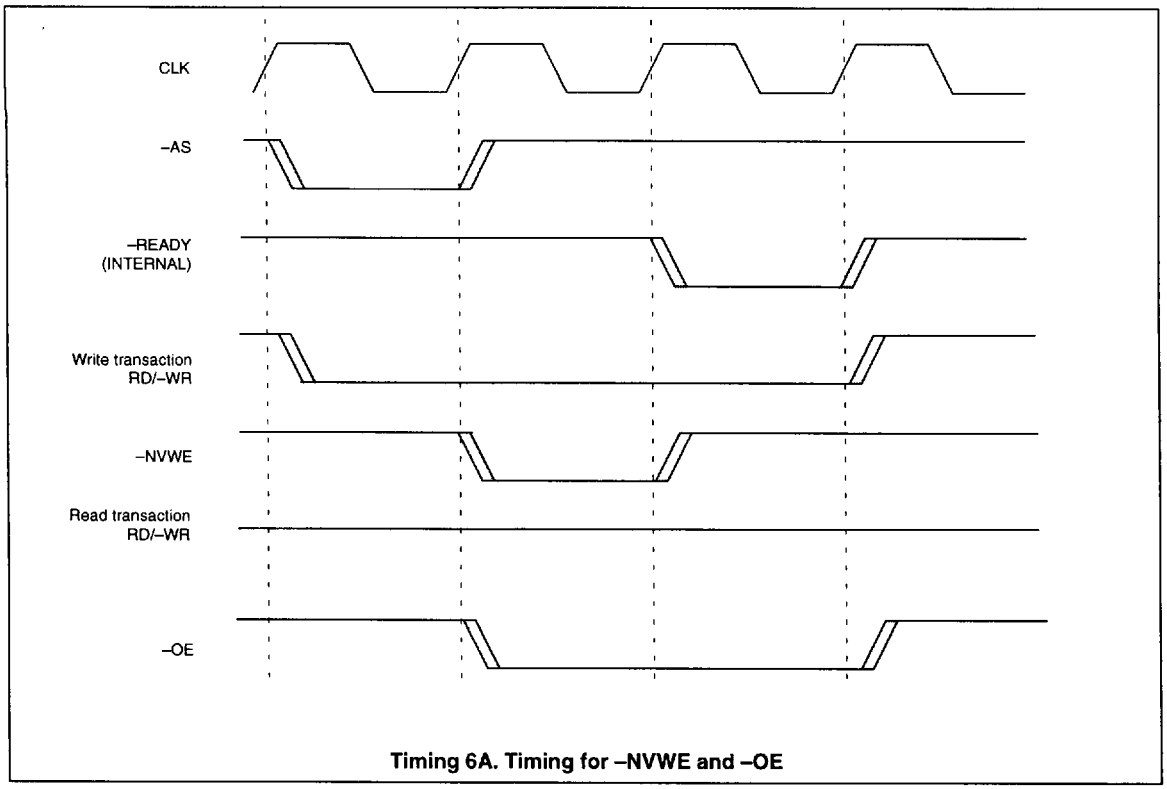


Timing 4. Store with Exception

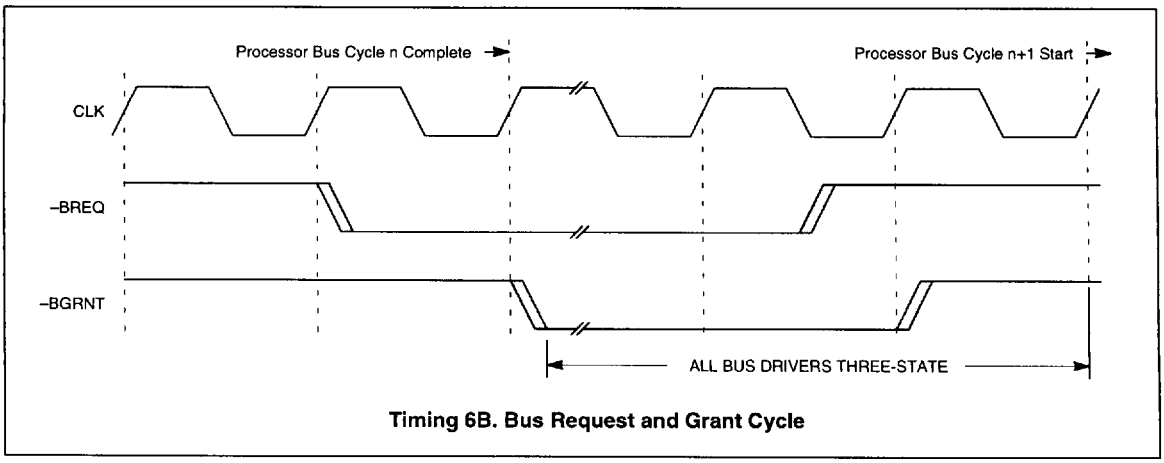


Note: A load followed by a store requires an intervening clock cycle on the bus while a store followed by a load can occur in consecutive clock cycles.

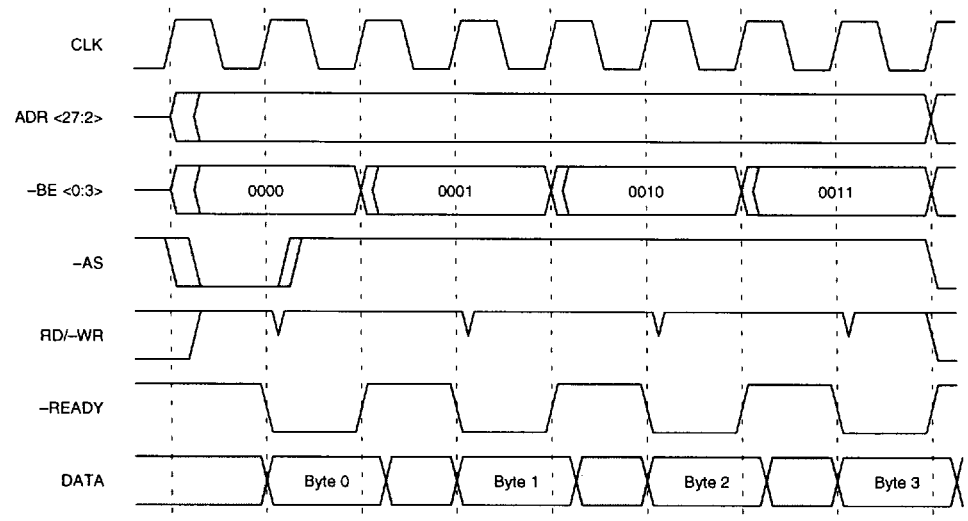
Timing 5. Atomic Operation



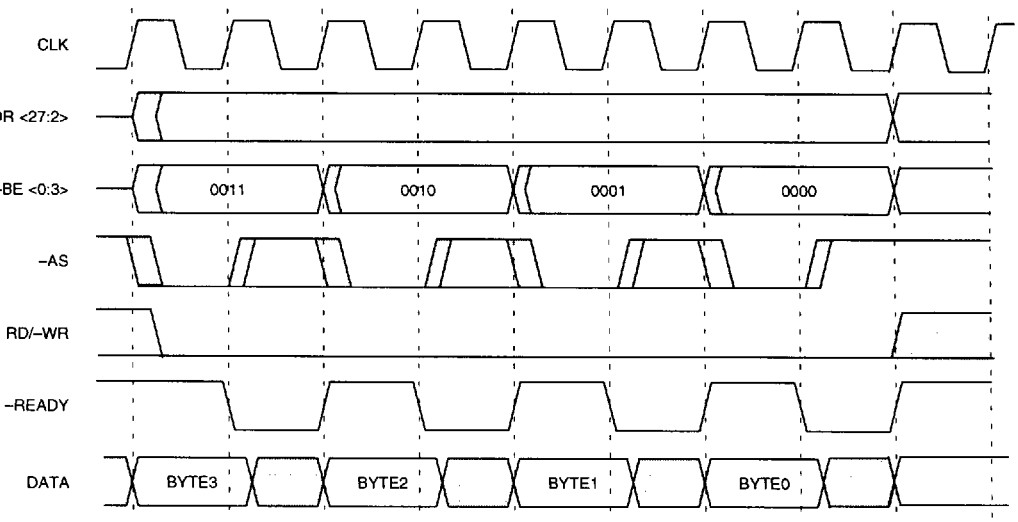
Timing 6A. Timing for –NVWE and –OE



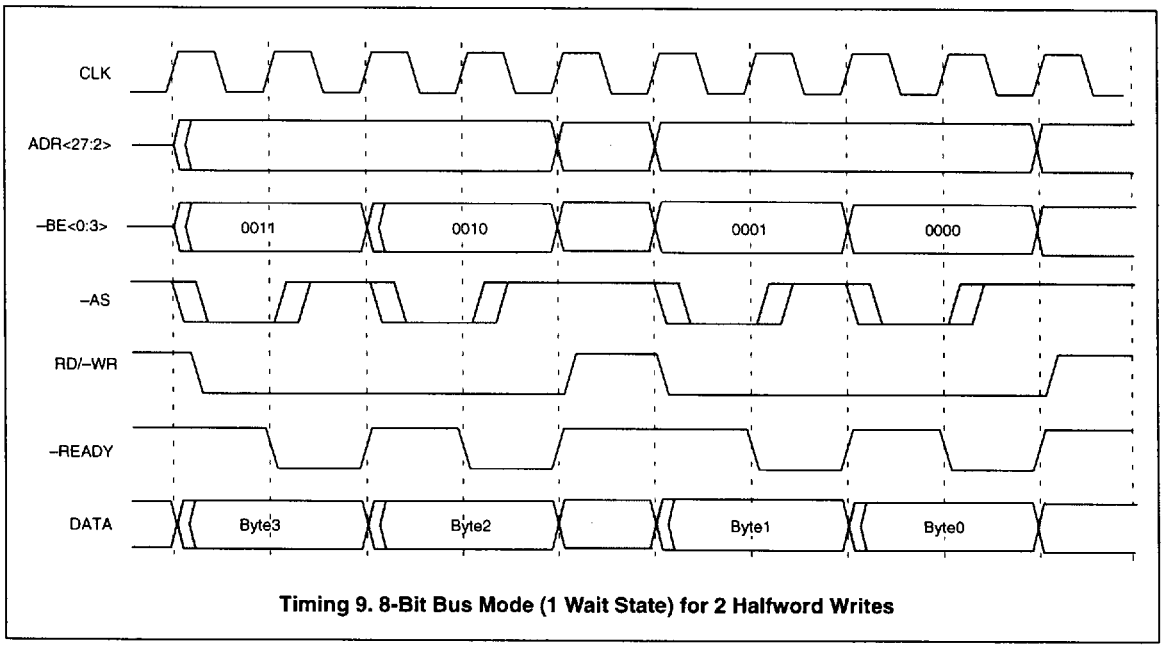
Timing 6B. Bus Request and Grant Cycle



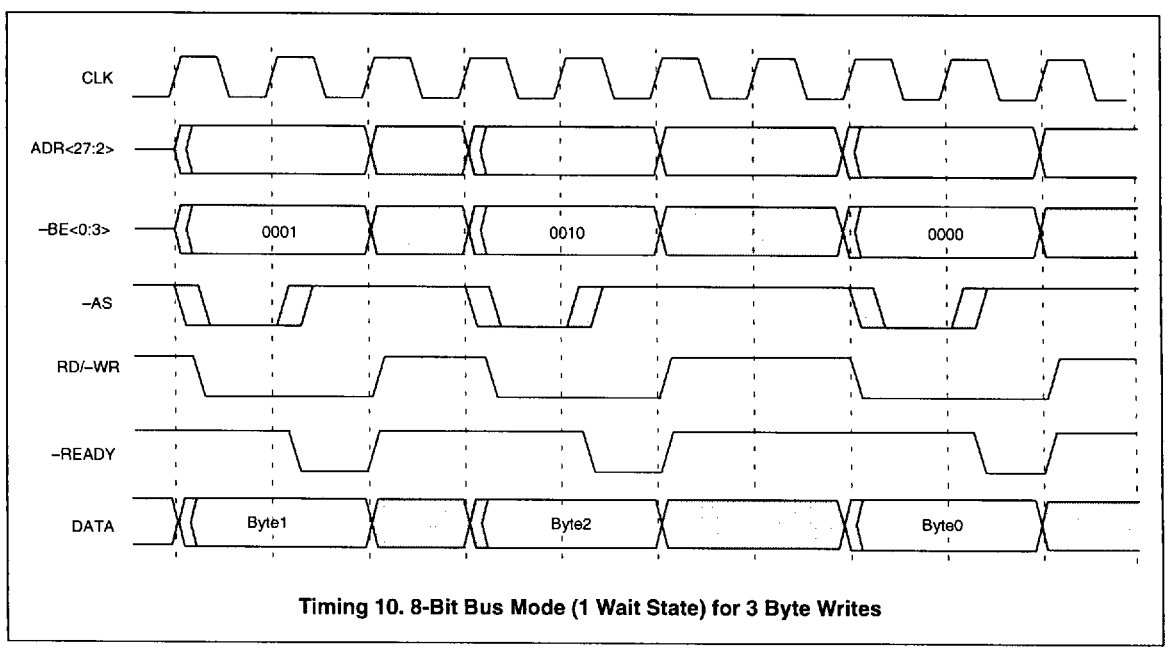
Timing 7. 8-Bit Bus Mode (1 Wait State) for Read only



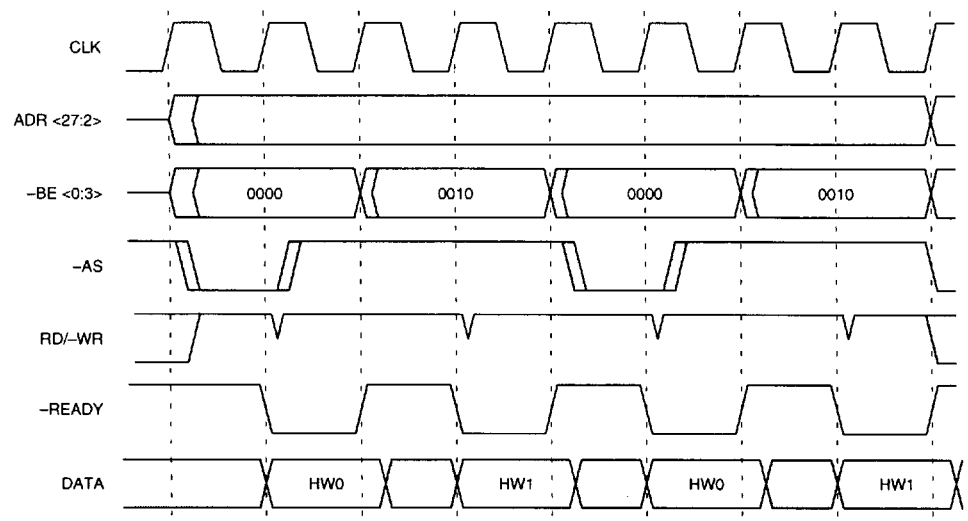
Timing 8. 8-Bit Bus Mode (1 Wait State) for Word Write



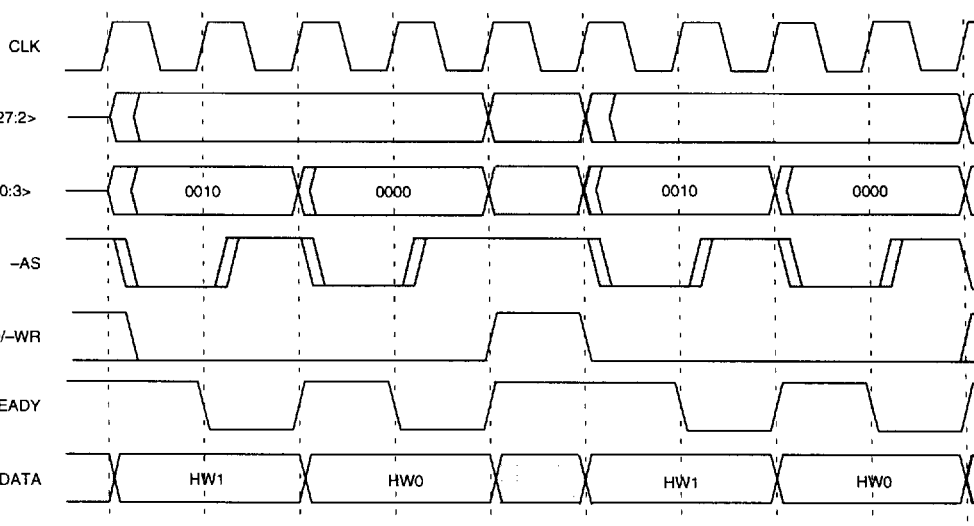
Timing 9. 8-Bit Bus Mode (1 Wait State) for 2 Halfword Writes



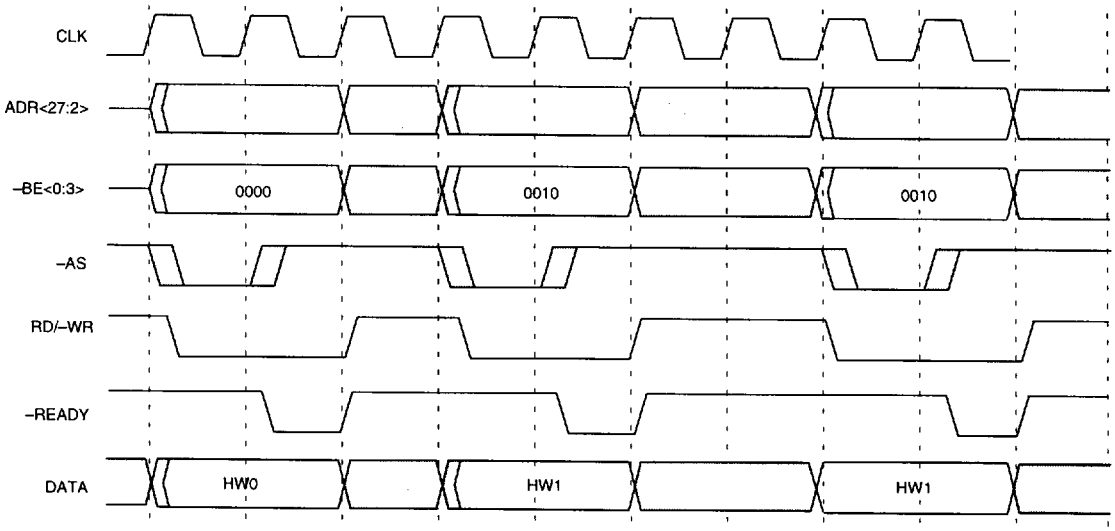
Timing 10. 8-Bit Bus Mode (1 Wait State) for 3 Byte Writes



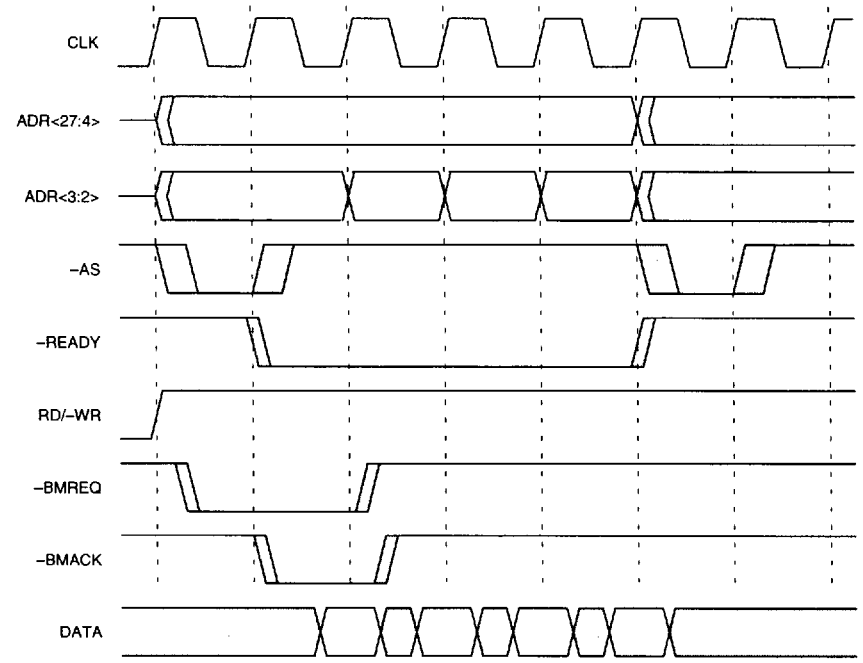
Timing 11. 16-Bit Bus Mode (1 Wait State) for Read only



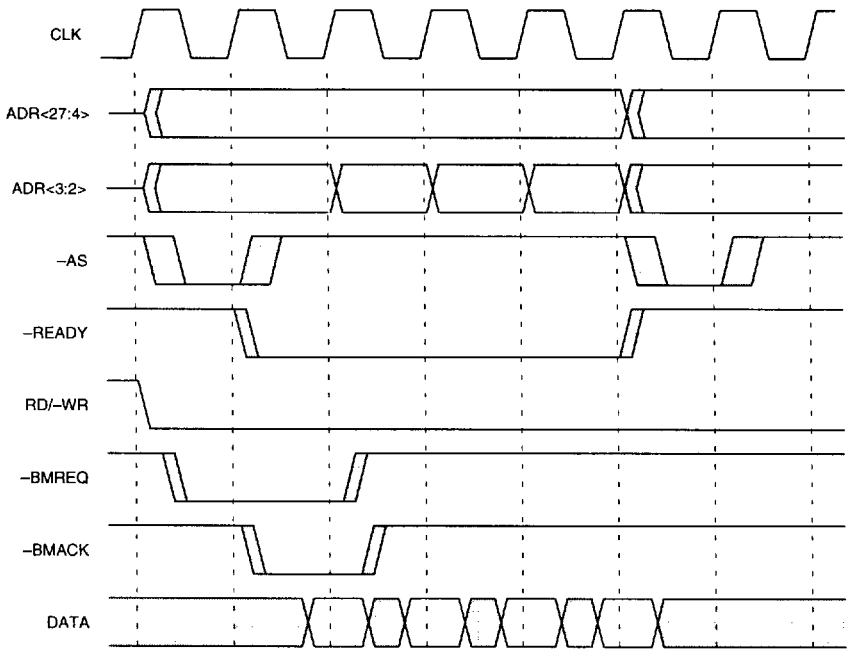
Timing 12. 16-Bit Bus Mode (1 Wait State) for Word Write



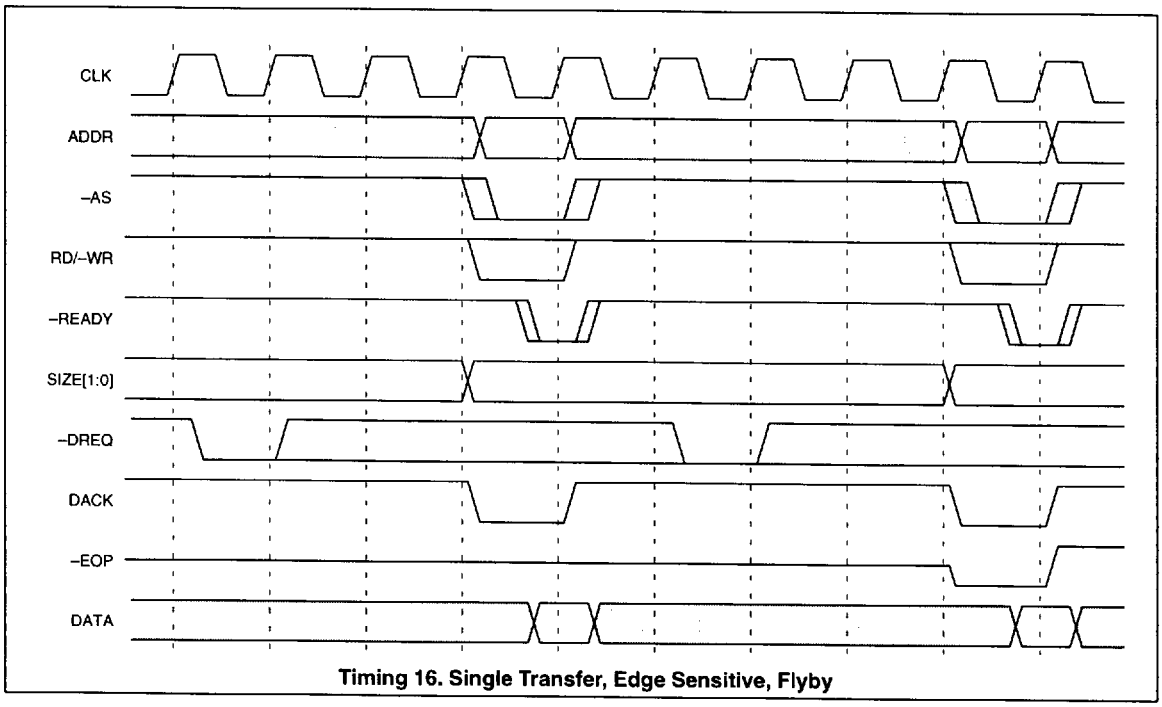
Timing 13. 16-Bit Bus Mode (1 Wait State) for 3 Halfword Writes



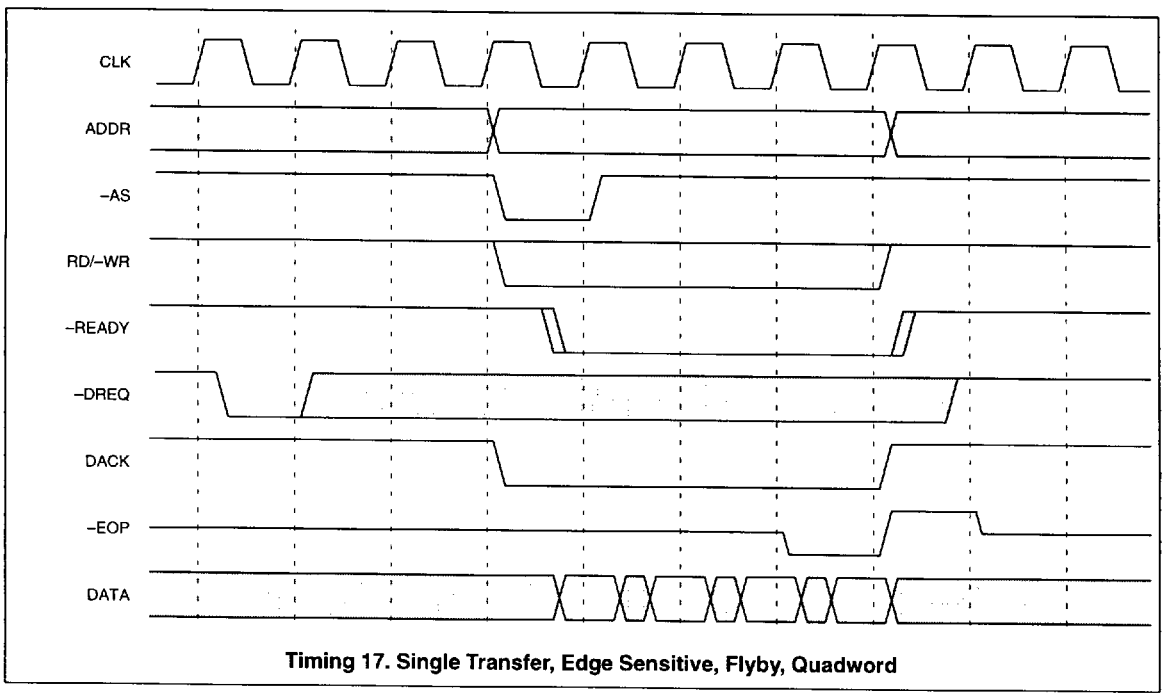
Timing 14. Burst Mode Read



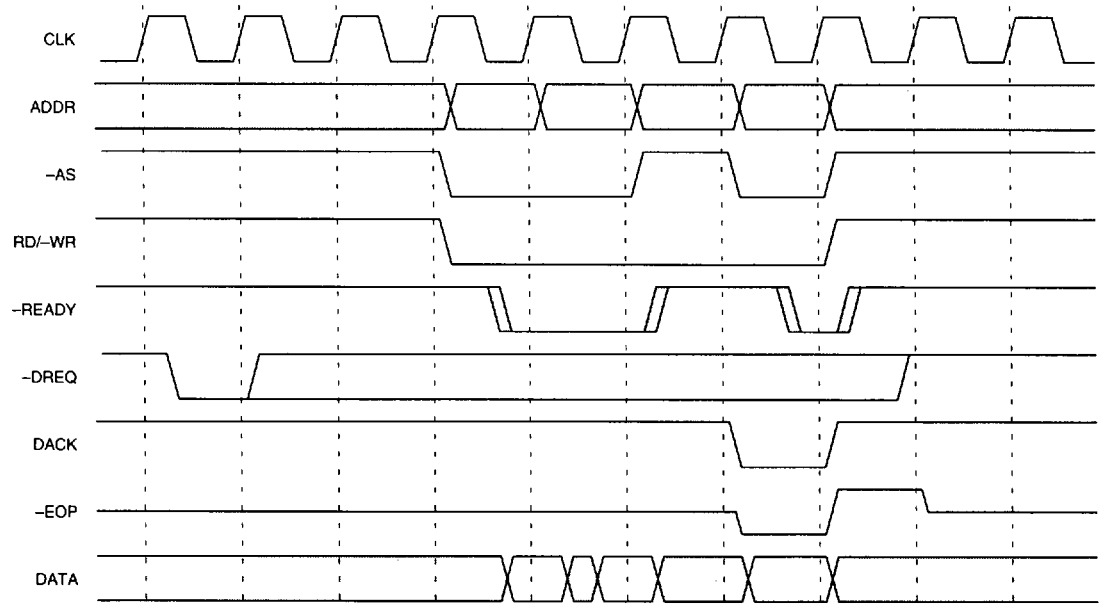
Timing 15. Burst Mode Write (DMA Only)



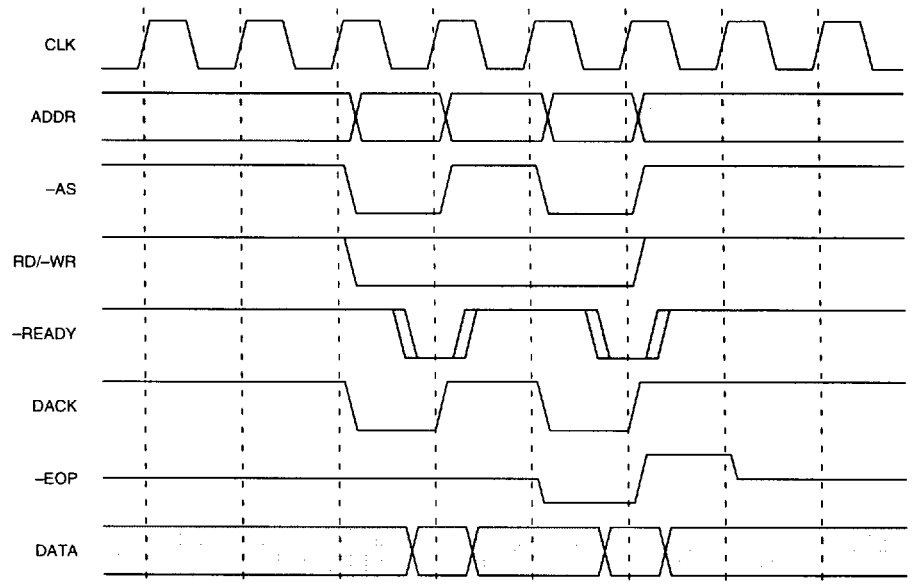
Timing 16. Single Transfer, Edge Sensitive, Flyby



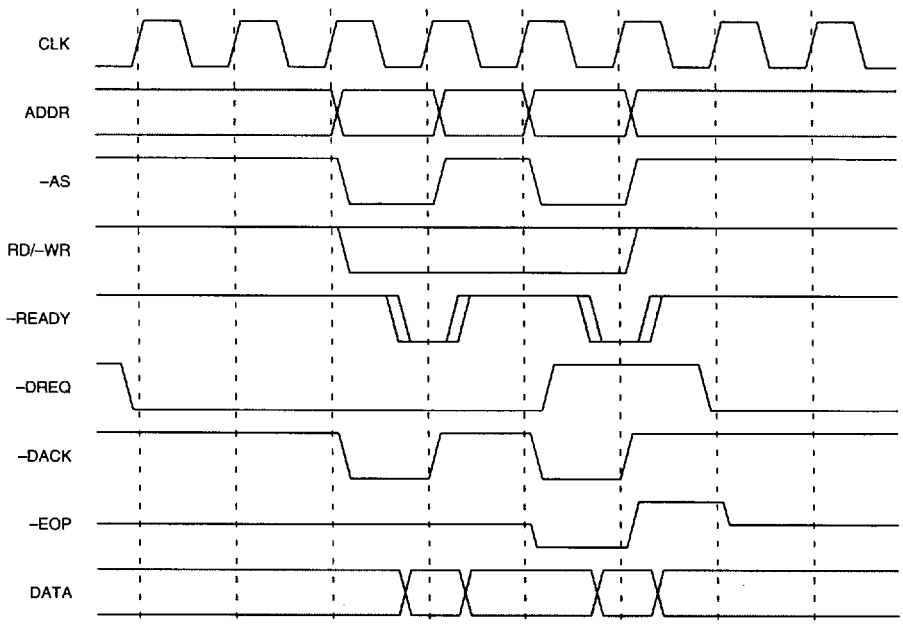
Timing 17. Single Transfer, Edge Sensitive, Flyby, Quadword



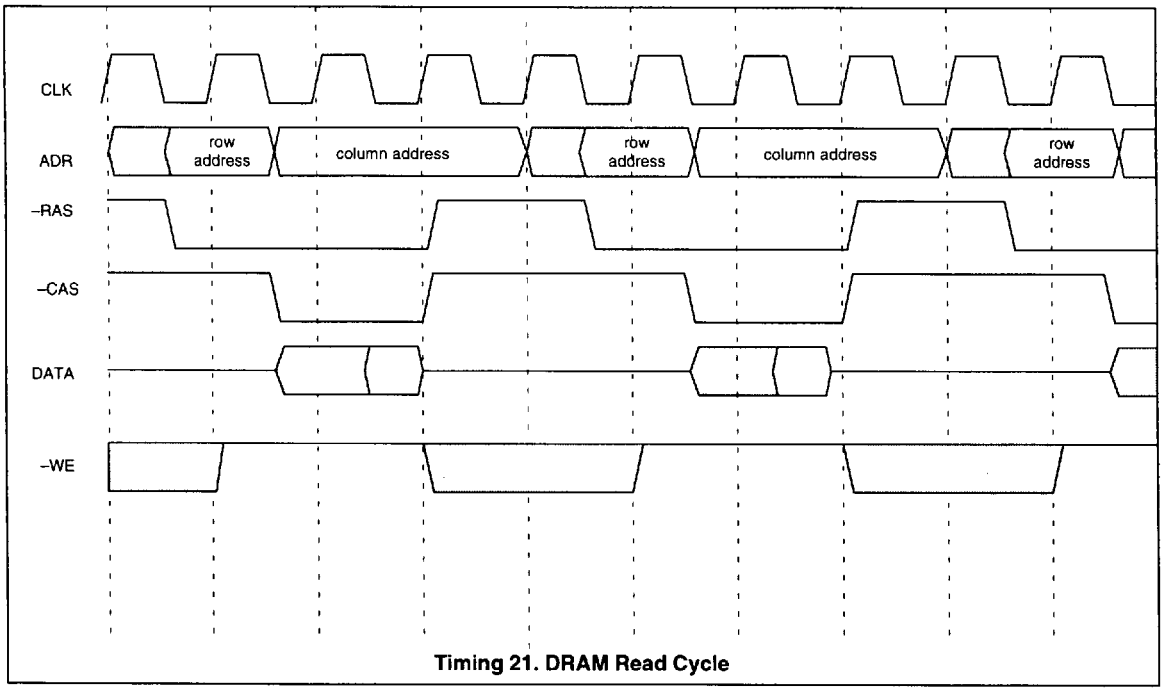
Timing 18. Single Transfer, Edge Sensitive, Flowthru, Dest Request (half-word source, word destination)



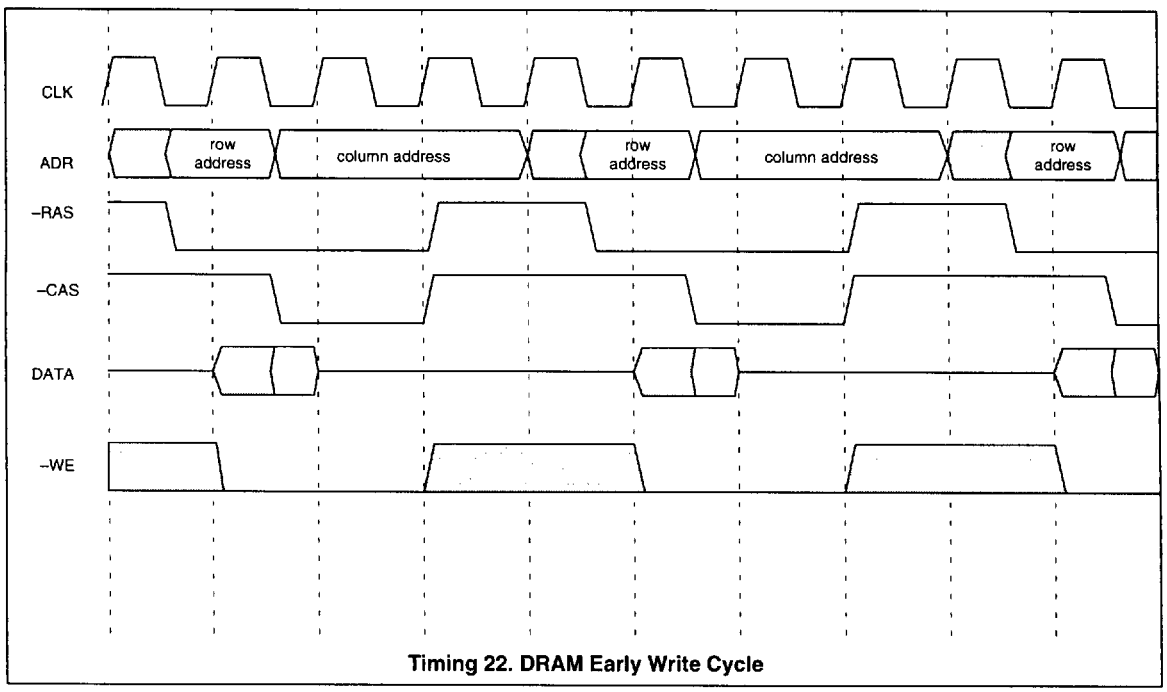
Timing 19. Block Transfer, Flyby



Timing 20. Demand Transfer, Flyby

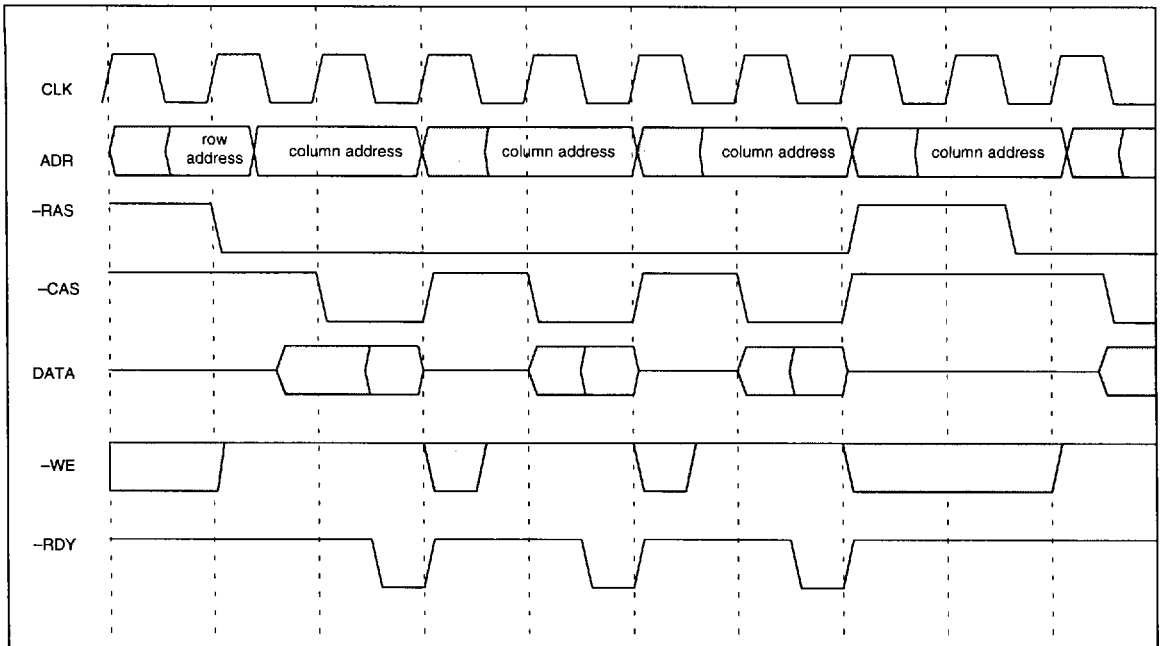


Timing 21. DRAM Read Cycle

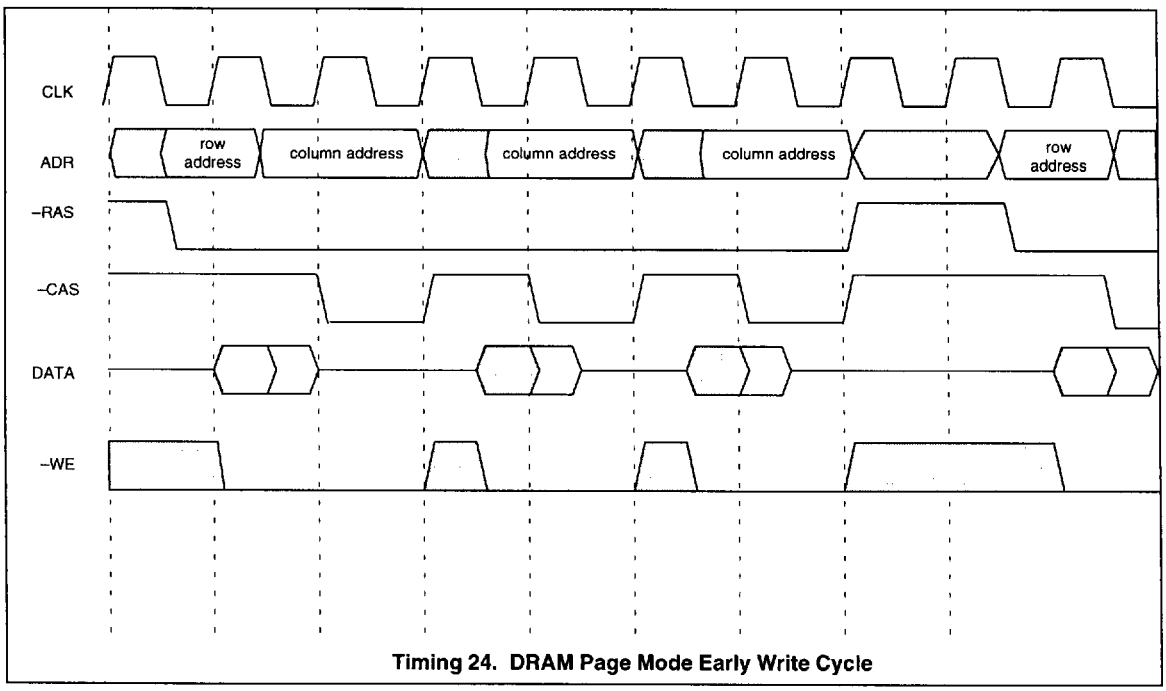


Timing 22. DRAM Early Write Cycle

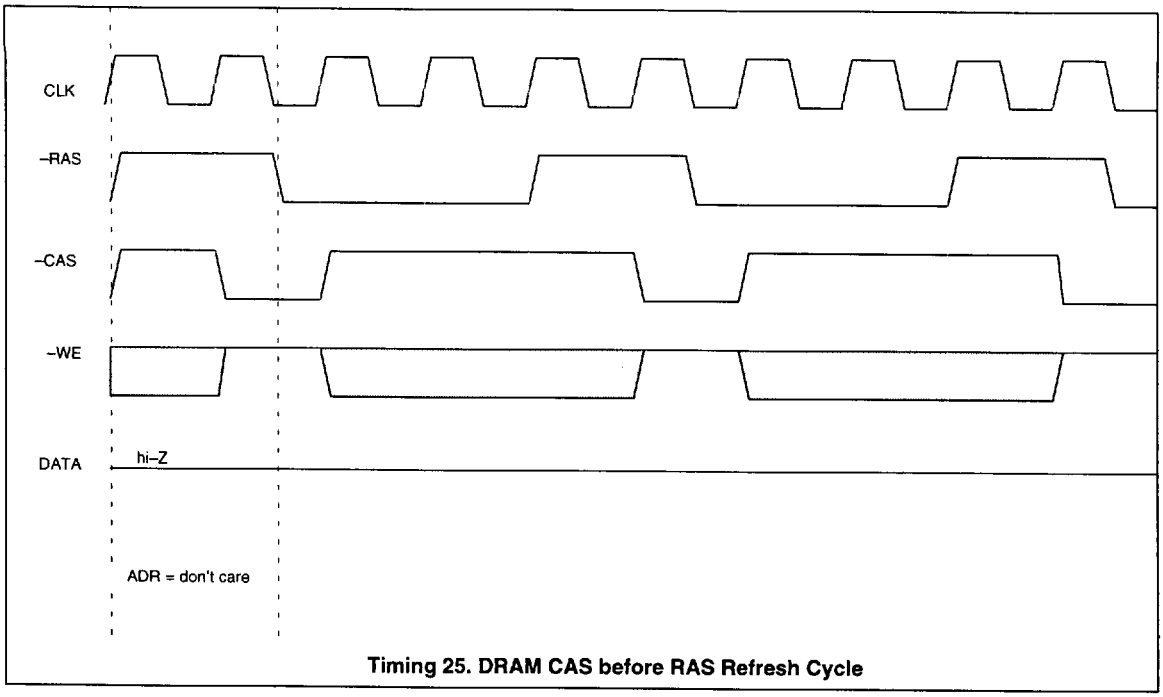
*Early Write – the assertion of WE precedes CAS



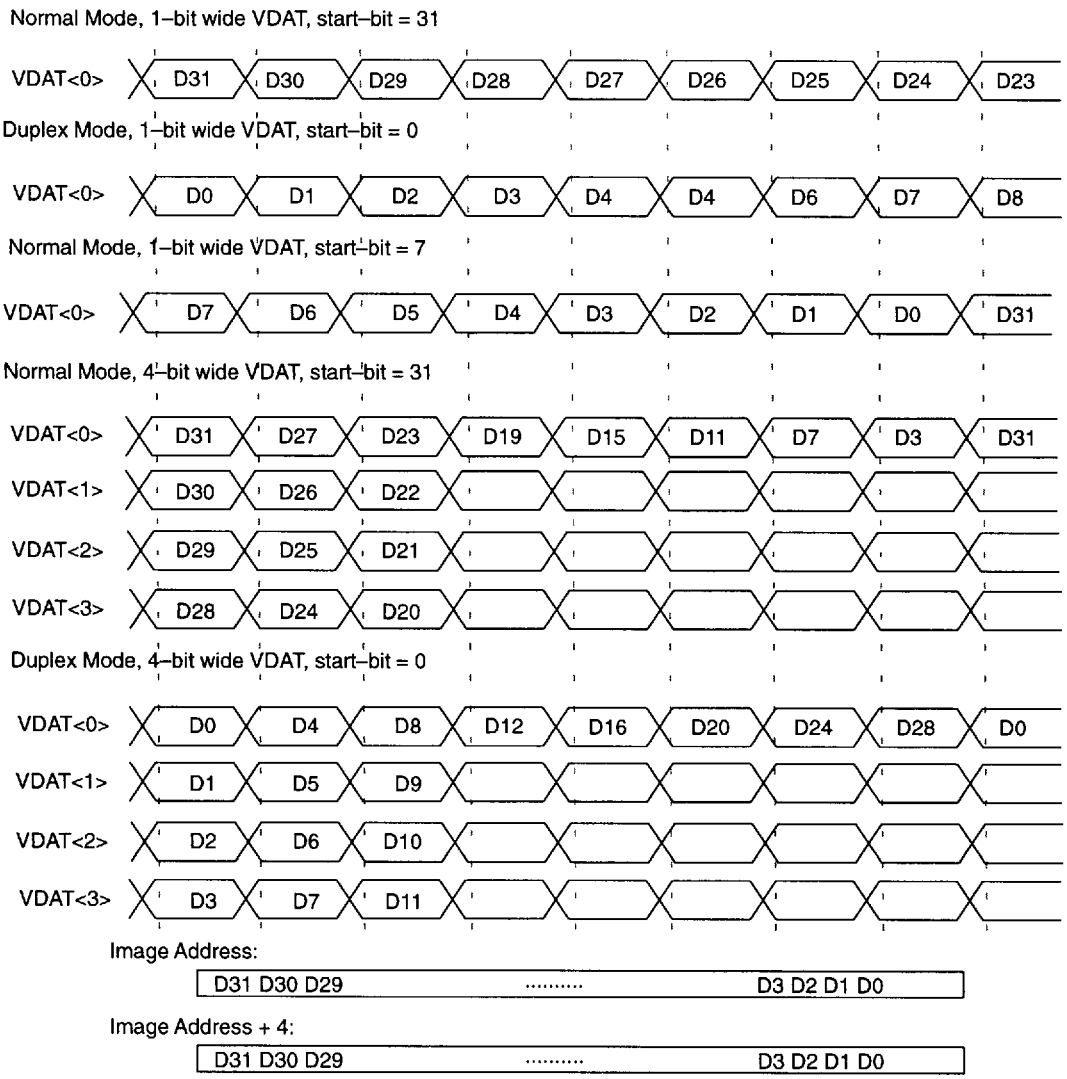
Timing 23. DRAM Page Mode Read Cycle



Timing 24. DRAM Page Mode Early Write Cycle



Timing 25. DRAM CAS before RAS Refresh Cycle



Timing 26. Video Data Order

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Conditions	Min.	Max.	Units
V_{DD}	Supply voltage (I/O)		−0.3	6	V
	Supply voltage (Core)		−0.3	4	
V_I	Input voltage		−0.3	VCC + 0.3	V
T_J	Operating junction temperature			125	°C

1. Stresses above those listed under Absolute Rating may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operation section of this specification is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods may affect device reliability.

Recommended Connections:

1. Power and ground connections must be made to multiple V_{CC} and V_{SS} pins. Every MB86936 based circuit board should include power (V_{CC}) and ground (V_{SS}) planes for power distribution. Every V_{CC} pin must be connected to the power plane, and every V_{SS} pin must be connected to the ground plane. Pins identified as "N.C." must not be connected in the system.
2. Liberal decoupling capacitance should be placed near the MB86936. The processor can cause transient power surges when its numerous output buffers transition, particularly when connected to large capacitive loads.
3. Low inductance capacitors and interconnections are recommended for best high frequency electrical performance. Inductance can be reduced by shortening the board traces between the processor and decoupling capacitors as much as possible. Capacitors specifically designed for the QFP package will offer the lowest possible inductance.
4. For reliable operation, alternate bus masters must drive any pins that are three-stated by the MB86936 when it has granted the bus, in particular –LOCK, ADR<27:2>, ASI<3:0>, –BE0-3, D<31:0>, –AS and RD/–WR must be driven by alternate bus masters. These pins are normally driven by the processor during active and idle bus states and don't require external pullups. N.C. pins must always remain unconnected.

PACKAGE THERMAL CHARACTERISTICS

Symbol	Parameter	Package	Value			Units
$\varnothing_{JC}$	Thermal resistance junction to case	208 Plastic QFP	5.0			°C/W
			0 m/s	1 m/s	3 m/s	
$\varnothing_{JA}$	Thermal resistance junction to ambient	208 Plastic SQFP Typical 208 Plastic SQFP Measured†	32 32	28 27	26 25	°C/W

DC SPECIFICATIONS[3] I/O V_{DD} = 5V ± 5%, CORE V_{DD} = 3.3V ± 5%

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IL}	Input low voltage		0	—	0.8	V
V_{IH}	Input high voltage (All pins except XTAL1)		2.0	—	V_{CC}	V
	Input high voltage (Pin XTAL1)		2.0	—	V_{CC}	V
V_{OL}	Output low voltage	I_{OL} = 3.2mA	0	—	0.45	V
V_{OH}	Output high voltage	I_{OH} = −0.4mA	2.4	—	V_{CC}	V
I_{LI}	Input leakage current	V_{IN} = 0 or V_{CC}	−10	—	10	µA
I_{LZ}	3–state output leakage current	V_{OUT} = 0 or V_{CC}	−10	—	10	µA
I_{CC}	Operating power supply current	50 MHz (internal clock)	—	450	675	mA
C_{PIN}	Pin capacitance (All pins except XTAL2)	V_{CC} = V_I = 0 f = 1 MHz	—	—	13	pF
	Pin capacitance (Pin XTAL2)		—	—	16	pF

† Measured in 4-layer PCB

AC CHARACTERISTICS[1,2,4,5] I/O V_{DD} = 5V ± 5%, CORE V_{DD} = 3.3V ± 5%, T_A 0–70°C

Symbol	Parameter Description		Min.	Max.	Units
t1	CLKIN period (in clock doubler mode)		40	100	ns
t2	CLKIN high Time		10		ns
t3	CLKIN low time		10		ns
t4	CLKIN rise time			3	ns
t5	CLKIN fall time			3	ns
t6	CLKIN to CLKOUT1 delay		0	3	ns
t7	CLKIN to CLKOUT2 delay		0.5xPeriod	0.5xPeriod+3	ns
t8	CLKOUT1, CLKOUT2 high time		0.35xPeriod		ns
t9	CLKOUT1, CLKOUT2 low time		0.4xPeriod		ns
t10	CLKOUT1, CLKOUT2 fall time			3	ns
t11	CLKOUT1, CLKOUT2 rise time			4	ns
t12	D<31:0>	Output valid delay		22	ns
		Output hold	2		
	ADR<27:2>	Output valid delay		21	ns
		Output hold	2		
	–BE0–3	Output valid delay		24	ns
		Output hold	2		
	ASI<3:0>	Output valid delay		31	ns
		Output hold	2		
	–CS0–4	Output valid delay		20	ns
		Output hold	2		
	PARITY0–3	Output valid delay		21	ns
		Output hold	2		

AC CHARACTERISTICS[1,2,4,5] I/O V_{DD} = 5V ± 5%, CORE V_{DD} = 3.3V ± 5%, T_A 0–70°C

Symbol	Parameter Description		Min.	Max.	Units
t13	–AS	Output valid delay		15	ns
		Output hold	2		
	RD/–WR	Output valid delay		16	ns
		Output hold	2		
	–LOCK	Output valid delay		16	ns
		Output hold	2		
	–BGRNT	Output valid delay		16	ns
		Output hold	2		
	–PBREQ	Output valid delay		16	ns
		Output hold	2		
	–READYOUT	Output valid delay		17	ns
		Output hold	2		
t14	TIMEROUT0	Output valid delay		17	ns
		Output hold	2		
	EMU_SD<3:0>	Output valid delay		14	ns
		Output hold	2		
	EMU_D<3:0>	Output valid delay		14	ns
		Output hold	2		
	EMU_ENB	Output valid delay		14	ns
		Output hold	2		
	–BMREQ	Output valid delay		19	ns
		Output hold	2		
	–NVWE	Output valid delay		18	ns
		Output hold	2		
	–OE	Output valid delay		15	ns
		Output hold	2		
	–SAME_PAGE Note: same physical pin as RAS3	Output valid delay		18	ns
		Output hold	2		
	–TIMER_OVF Note: same physical pin as RAS2	Output valid delay		19	ns
		Output hold	2		

AC CHARACTERISTICS[1,2,4,5] I/O V_{DD} = 5V ± 5%, CORE V_{DD} = 3.3V ± 5%, T_A 0–70°C

Symbol	Parameter Description		Min.	Max.	Units
t15	–DACK0, –DACK1, –DACK2	Output valid delay		18	ns
		Output hold	2		
	–EOP0, –EOP1, –EOP2	Output valid delay		23	ns
		Output hold	2		
t16	–RAS0–3	Output valid delay		15	ns
		Output hold	2		
	–CAS0–3	Output valid delay		15	ns
		Output hold	2		
	–DWE	Output valid delay		15	ns
		Output hold	2		
t17	ADR<15:2> with internal DRAM Controller	Output valid delay		23	ns
		Output hold	2		
	PARITY with internal DRAM Controller	Output valid delay		24	ns
		Output hold	2		
t18	–CS5 Note: same physical pin as RAS1	Output valid delay		20	ns
		Output hold time	2		
t19	RD/–WR	Input setup time	9		ns
		Input hold time	2		
	–AS	Input setup time	9		ns
		Input hold time	2		
	–MEXC	Input Setup Time	14		ns
		Input hold time	2		
	–READY	Input Setup Time	16		ns
		Input hold time	2		
	–BREQ	Input Setup Time	8		ns
		Input hold time	2		
	–BMACK	Input Setup Time	9		ns
		Input hold time	2		
t20	–ASI<3:0>	Input setup time	9		ns
		Input hold time	2		
	ADR<27:2>	Input setup time	9		ns
		Input hold time	2		

AC CHARACTERISTICS[1,2,4,5] I/O V_{DD} = 5V ± 5%, CORE V_{DD} = 3.3V ± 5%, T_A 0–70°C

Symbol	Parameter Description		Min.	Max.	Units
t21	D<31:0> without parity	Input Setup Time	15		ns
		Input hold time	2		
t22	–DREQ0, –DREQ1, –DREQ2	Input Setup Time	9		ns
		Input hold time	2		
	–EOP0, –EOP1, –EOP2	Input valid delay	9		ns
		Input hold	2		
t23	VCLK Period		40	—	ns
t24	VCLK high time		10	—	ns
t25	VCLK low time		10	—	ns
t26	VCLK from xtal1	Output Timing	2	6.0	ns
t27	VDAT[8]	Output valid delay		29.0	ns
		Output hold time	2.0		
	PSYNC[8]	Output valid delay		20.0	ns
		Output hold time	2.0		
t28	VDAT[8]	Input Setup Time	22.0		ns
		Input hold time	8		
	PSYNC[8]	Input Setup Time	20.0		ns
		Input hold time	8		
	LSYNC[8]	Input Setup Time	20.0		ns
		Input hold time	8		

1. Parameters are valid over specified temperature range and supply voltage range unless otherwise noted.
2. All voltage measurements are referenced to ground. All time measurements are referenced at input and output levels of 1.5V. For testing, all inputs swing between 0.4V and 2.4V (Except XTAL1 which swings from 0.4V to 3.0V). Input rise and fall times are 2ns or less.
3. Not more than one output may be shorted at a time for a maximum duration of one second.
4. Timing specifications apply to 50 MHz operating frequency in Clock Doubler Mode (i.e. f_{CLK-IN} = 25 MHz).
5. All output timings are based on a 30pF load.
6. Timing with respect to VCLK pin.

Prescaler Output Clock Timing Parameter

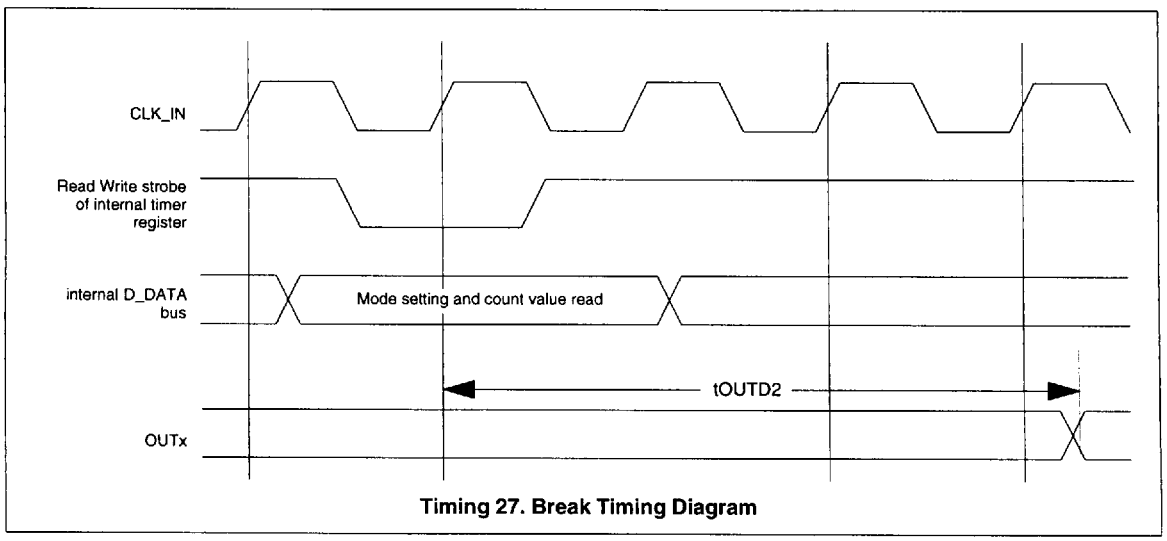
Symbol	Item	Typ.	Unit
t_{PSCLW}	Prescaler output "L" Width *1, *3, *4	1	tPCK
t_{PSCLW}	Prescaler output "H" Width *1, *3, *4	N–1	tPCK
t_{PSCLW}	Prescaler output "L" Width *2, *3, *4	$N \bullet 2^{M-1}$	tPCK
t_{PSCLW}	Prescaler output "H" Width *2, *3, *4	$N \bullet 2^{M-1}$	tPCK

1. Applicable when select field of prescaler register = 0.
2. Applicable when Select field of prescaler register is non zero. M= value of select field. N= Value of prescale value field.
3. If prescale value field is set to 1, PRSCKx output will be fixed to 0.
4. t_{PCK} is prescaler input clock period. Internal Clock Mode: $t_{PCK} = 2 \bullet t_{CLK}$.
5. PRSCKx is not available as output. This is for information only.

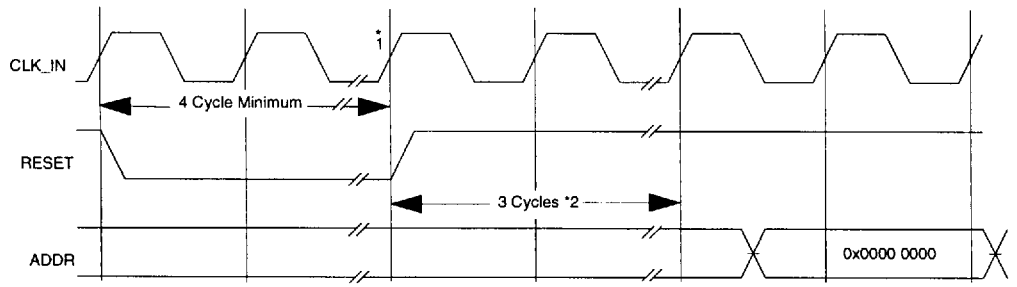
Timer Input

Symbol	Item	Min	Max	Unit
t_{OUTD2}	TIMEROUT0 output delay	—	3tCLK+30	ns

For the following modes
- Mode Setting (write to TCR).
- After set mode 0, write "RELOAD" register read/count
- After set mode 1, write "RELOAD" register read/count

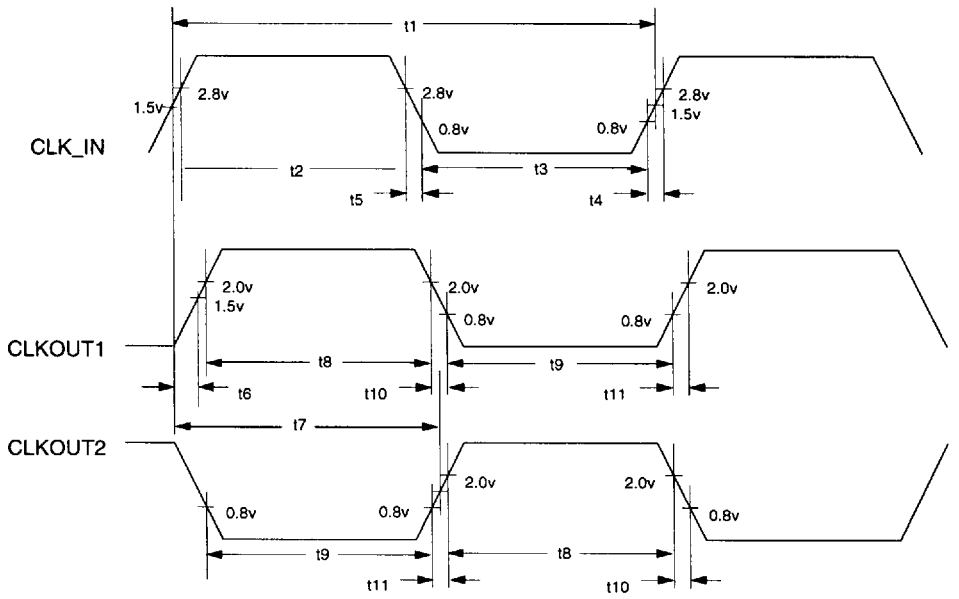


Timing 27. Break Timing Diagram



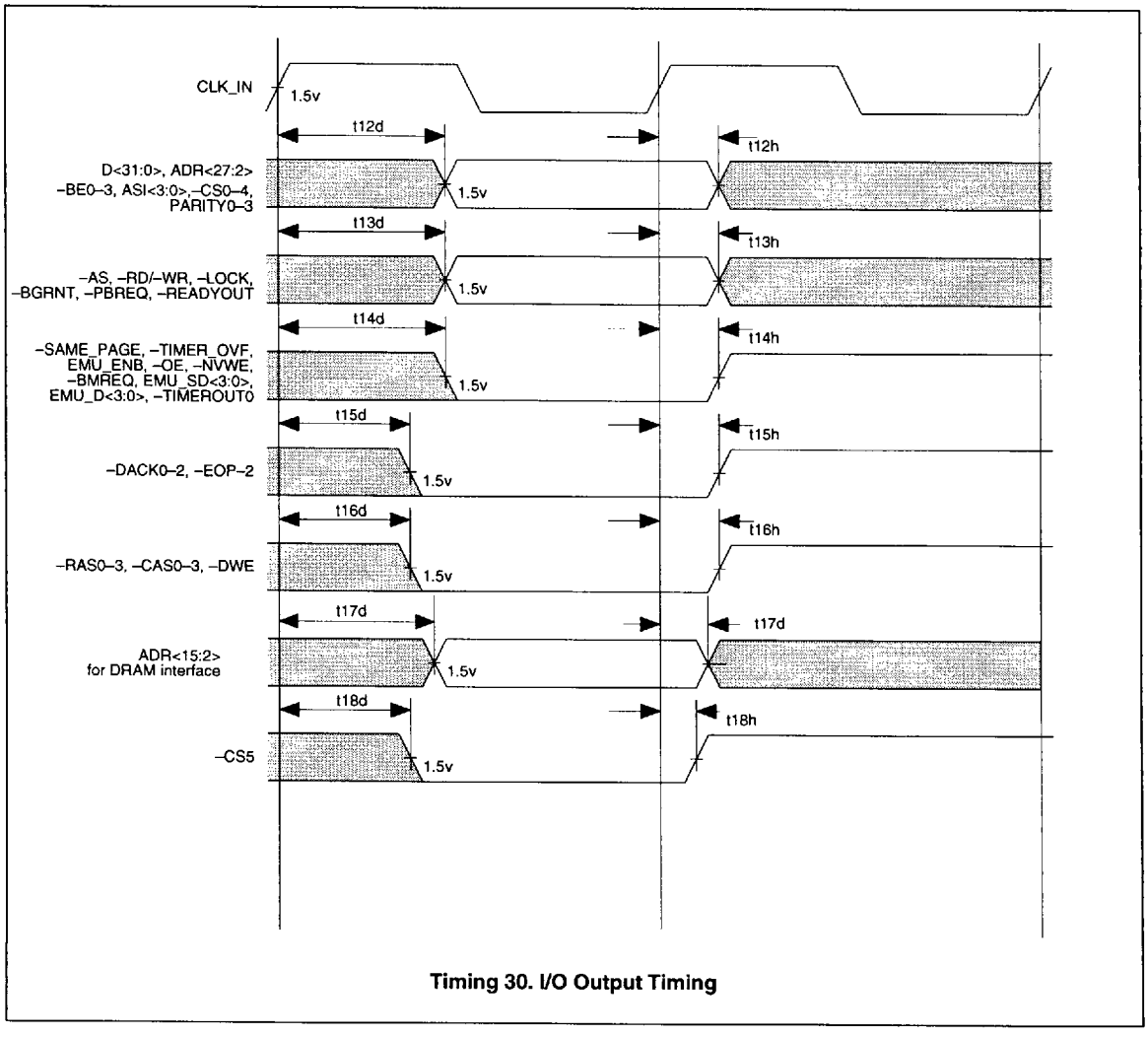
*1. CLK_IN must be stable for at least 100ms before RESET is de*asserted.
*2. When RESET hold time is met.

Timing 28. Reset Timing

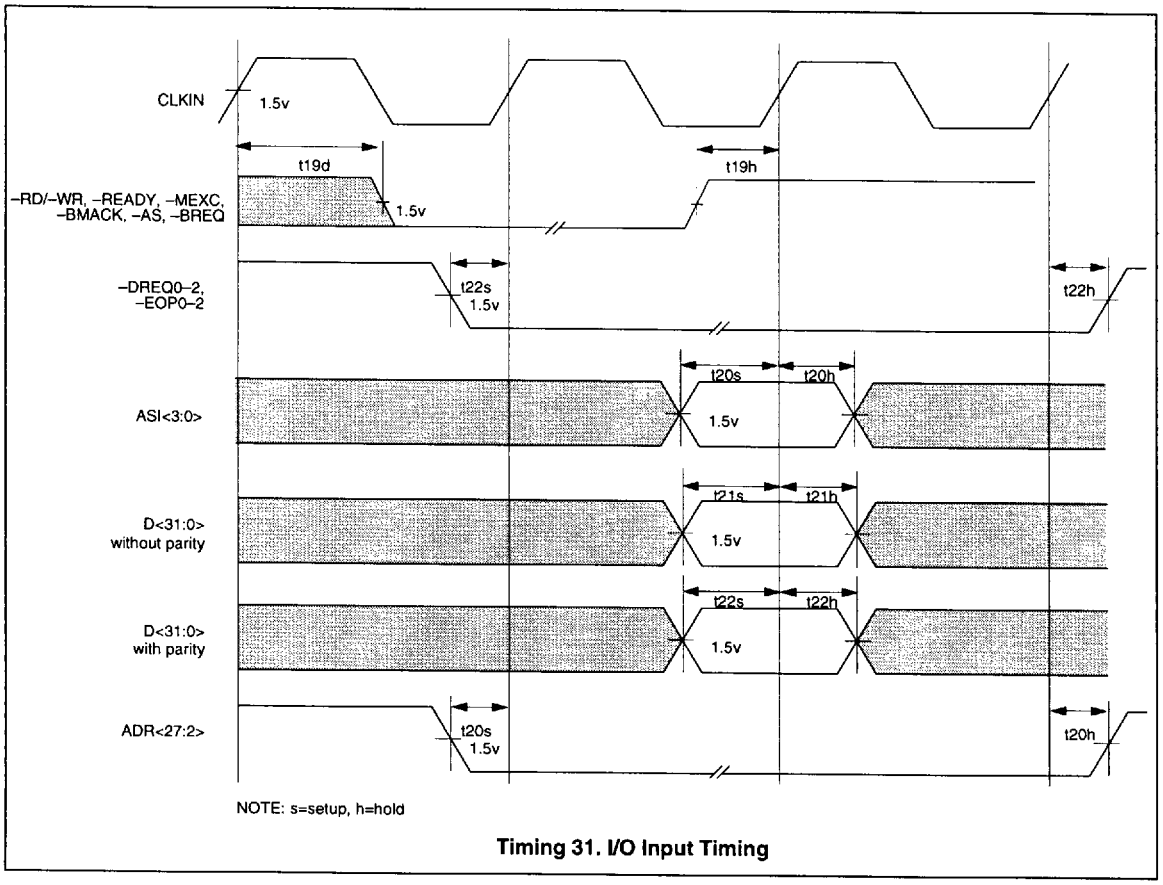


Note: *CLKOUT1 and CLKOUT2 are derived from non*overlapping internal clocks, however, the relative timing of these signals is not tested.

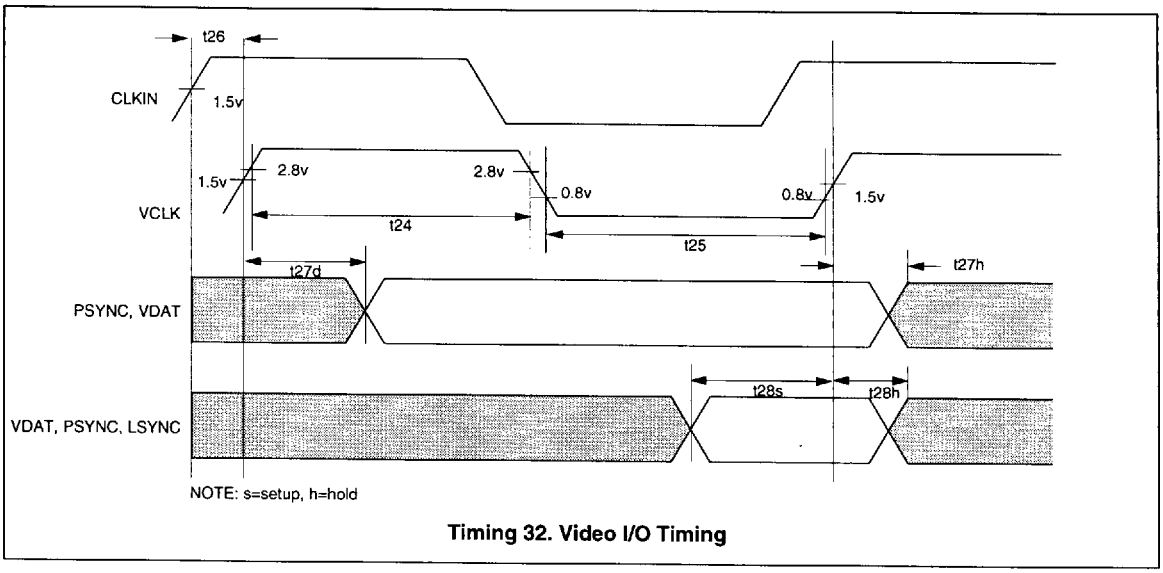
Timing 29. Clock Timing



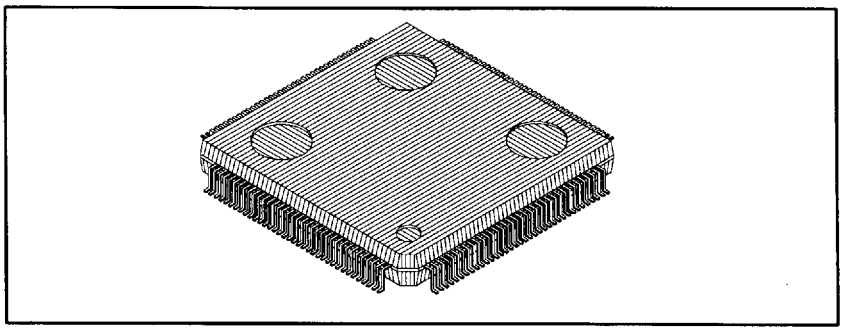
Timing 30. I/O Output Timing



Timing 31. I/O Input Timing



Timing 32. Video I/O Timing



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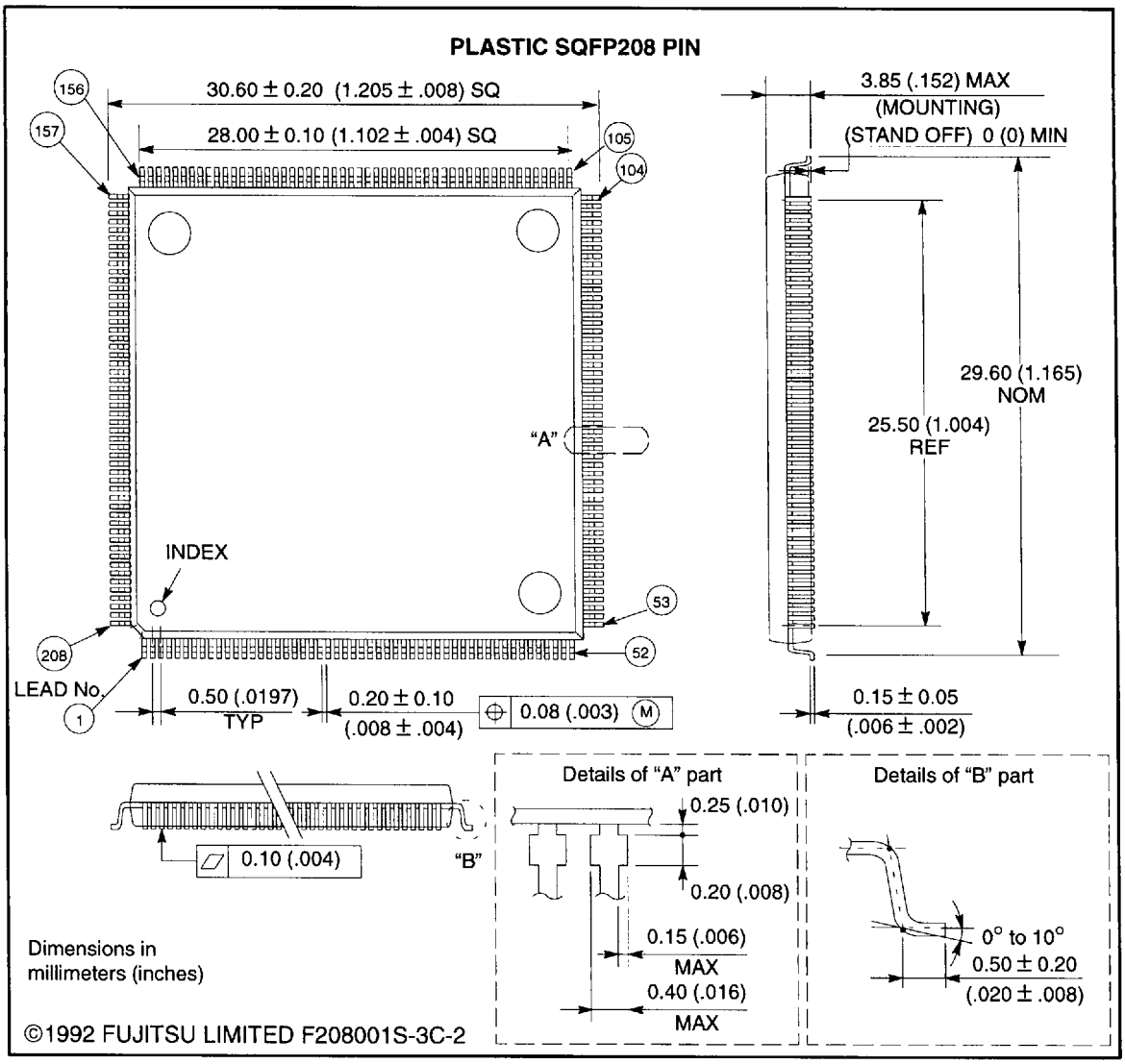

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