MB86962

10BASE-T TRANSCEIVER FOR TWISTED PAIR ETHERNET

PRELIMINARY DATA SHEET

FEBRUARY 1991

FEATURES

- Complete implementation of IEEE 802.3 10BASE-T Medium Attachment Unit (MAU)
- Automatic AUI/10BASE-T selection
- Direct interface to AUI and RJ45 connectors
- Reverse polarity detection for receiver and selectable correction
- On-chip jabber logic, link test, and SQE test with enable/disable options
- Programmable receive threshold for extended range
- LED drivers for transmit, receive, jabber, collision, link and reversed polarity indicators or for flashing status indicator
- Single 5 volt power supply, CMOS technology
- Available in 28-pin DIP and PLCC packages

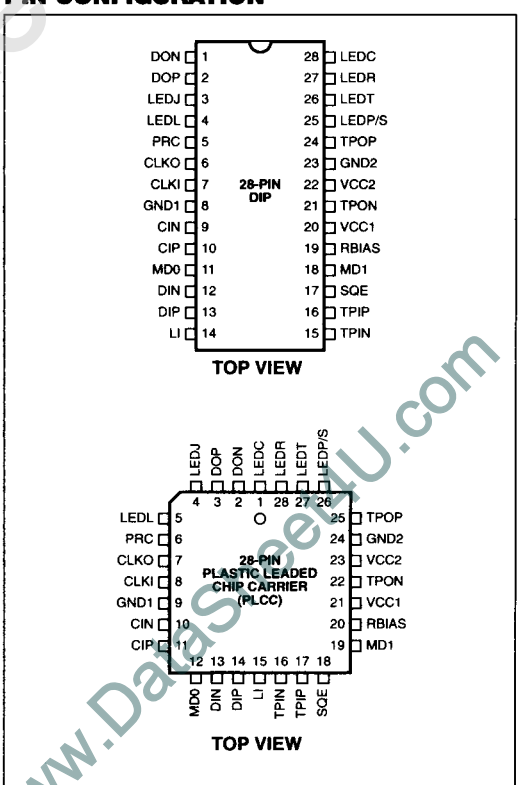
GENERAL DESCRIPTION

The MB86962 Twisted Pair Transceiver for Ethernet is fully compliant with the IEEE 802.3 10BASE-T specifications, and provides the electrical interface between the AUI (Attachment Unit Interface) and the twisted pair wiring. Functions provided by the MB86962 include level shifted data pass through from one transmission medium to another, collision detection, signal quality error (SQE) and link integrity testing, jabber control, loopback, and automatic correction of polarity reversal on the twisted pair input.

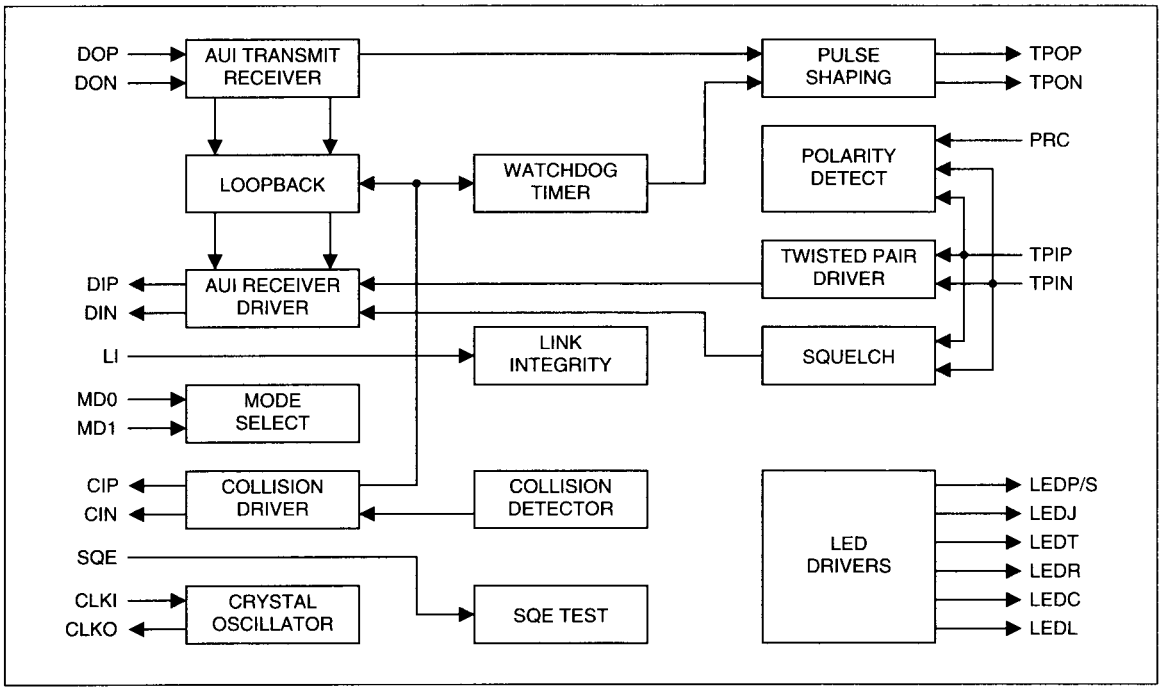
The transceiver uses a minimal number of external components and provides several unique features which make it an ideal device for both internal and external MAU (Medium Attachment Unit) applications. Its AUI/10BASE-T auto-sense circuity can automatically determine whether the local area network adapter is attached to an AUI cable or to twisted pair wiring, thus eliminating the need for jumpers to select between these two media. A high impedance AUI interface permits capacitive coupling to the external Manchester encoder/decoder, eliminating the isolation coupling transformer usually required at that interface. The receive threshold can be reduced to allow an extended range between nodes in low-noise environments. LED drivers are provided for transmit, receive, jabber, collision, link and reversed polarity indicators, or for a flashing status indicator.

The MB86962 is part of a complete family of Ethernet devices available from Fujitsu. It is fabricated in low-power CMOS technology and is available in 28-pin plastic DIP and PLCC packages.

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING CODE

PACKAGE STYLE	TEMPERATURE RANGE	ORDERING CODE
28-Pin Plastic Dual In-Line	0 to +70°C	MB86962P-G
28-Pin Plastic Leaded Chip Carrier	0 to +70°C	MB86962PD-G

SIGNAL DESCRIPTIONS[1]

SYMBOL	TYPE	DESCRIPTION
DON DOP	I	**DATA OUT NEGATIVE/POSITIVE:** Differential input pair connected to the AUI DO circuit.
LEDJ	I/O	**JABBER LED DRIVER:** Open drain driver for the Jabber indicator LED. Output goes active (low) when watchdog timer begins jab, and stays active until end of the unjab wait period (491 - 525 ms). When tied to ground, causes LEDP/S to act as a multi-function, blinking status indicator.
LEDL	O	**LINK LED DRIVER:** Open drain driver for the Link indicator LED. Output is active (low) except during Link Fail or when Link Integrity Test is disabled.
PRC	O	**POLARITY REVERSE CORRECTION:** The MB86962 automatically corrects reversed polarity at TPI when PRC is tied high. In Test mode, this pin is a 10 MHz output.
CLKO CLKI	-	**CRYSTAL OSCILLATOR:** The MB86962 requires either a 20 MHz crystal connected across these pins, or a 20 MHz clock applied at CLKI.
GND1 GND2	-	**GROUND.**
CIN CIP	O	**COLLISION NEGATIVE/POSITIVE:** Differential driver output pair tied to the collision presence pair of the Ethernet AUI cable. The collision presence signal is a 10 MHz square wave. This output is activated when a collision is detected on the network, during self-test by the SQE sequence, or after the watchdog timer has expired to indicate that the transmit wire pair has been disabled.
MD0 MD1	I	**MODE SELECT:** Selects operating mode. MD1 clock input between 2.0 and 2.5 MHz enables Test mode.
DIN DIP	O	**DATA IN NEGATIVE/POSITIVE:** Differential drive pair connected to the AUI DI circuit.
LI	I	**LINK INTEGRITY TEST ENABLE:** Link integrity testing is enabled when this pin is tied high. With link test enabled, the MB86962 sends the link integrity signal in the absence of transmit traffic. It also recognizes received link test pulses, indicating that the receive wire pair is present in the absence of transmit traffic.
TPIN TPIP	I	**TWISTED PAIR RECEIVE INPUTS:** Differential receive inputs from the twisted pair input filter.
SQE	I/O	**SIGNAL QUALITY ERROR TEST ENABLE:** SQE is enabled when this pin is tied high. When enabled, the MB86962 sends the signal quality error test sequence to the CI of the AUI cable after every successful transmission to the media. In Test mode, SQE becomes a 20 MHz output.
RBIAS	-	**RESISTOR BIAS CONTROL:** Bias control pin for the operating circuit. Bias set by an external resistor to ground. External resistor value = 12.4KΩ (±1%).

MD1	MD0	MODE
0	0	10BASE-T compliant MAU
0	1	Reduced squelch level
1	0	Half current AUI driver
1	1	DO, DI & CI ports disabled
Clock	0	Test Mode, Jabber enabled
Clock	1	Test Mode, Jabber disabled

1. In the following descriptions, signal names preceded by a minus sign (–) indicate an active low state. Dual function pins have two names separated by a slash (/).

SIGNAL DESCRIPTIONS (CONTINUED)

SYMBOL	TYPE	DESCRIPTION
VCC1 VCC2	I	**+5 VOLT POWER SUPPLY.**
TPON TPOP	O	**TWISTED PAIR TRANSMIT OUTPUTS:** Transmit drivers to the twisted-pair output filter. The output is Manchester encoded and pre-distorted to meet the 10BASE-T template.
LEDP/S	O	**POLARITY/STATUS LED DRIVER:** Open drain LED driver. In normal mode, LEDP/S is active (low) when reversed polarity is detected. If LEDJ is tied to ground, the output LEDP/S indicates multiple status conditions as shown in Figure 1. On solid = Normal, 1 blink = Link Down, 2 blinks = Jabber, 5 blinks = Polarity Reversed.
LEDT	O	**TRANSMIT LED DRIVER:** Open drain driver for the Transmit indicator LED. Output is active (low) during transmit.
LEDR	O	**RECEIVE LED DRIVER:** Open drain driver for the Receive indicator LED. Output is active (low) during transmit.
LEDC	O	**COLLISION LED DRIVER:** Open drain driver for the Collision indicator LED. Output is active (low) during transmit.

NOTE: I = Standard input
O = Standard output
I/O = Input or output

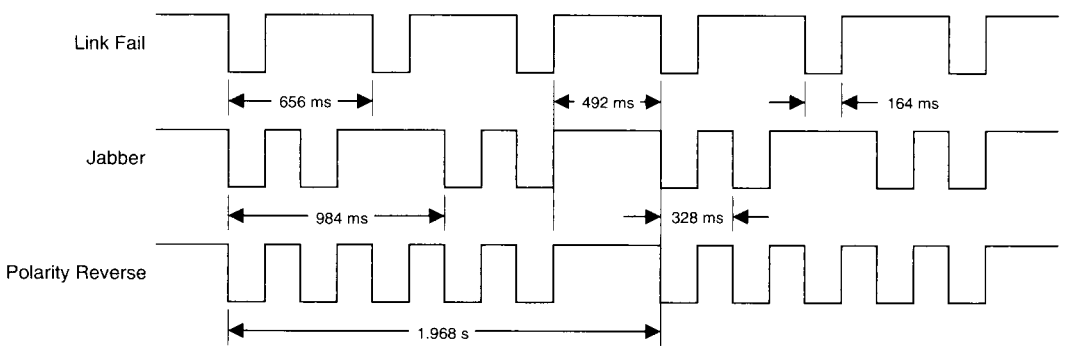
APPLICATIONS

Figure 2 shows the MB86962 in a typical external MAU application, interfacing between an AUI and the RJ45 connector of the twisted pair network. Figure 3 is the connection diagram for this application. A 20 MHz crystal or ceramic resonator connected across CLKI and CLKO provides the required clock signal. Transmit and receive filters are required in the TPO and TPI circuits. Details of these filters are shown in Figures 4 and 5, respectively. (Differential filters are also recommended).

Figures 6 and 7 show an internal MAU application which takes advantage of the MB86962's unique AUI/10BASE-T switching feature to select either the D-connector (AUI) or the RJ45 connector (10BASE-T). No termination resistors are used on the MB86962 side of the AUI interface to prevent impedance mismatch with the drop cable. The half current drive mode is used to maintain the same voltage levels in the absence of termination resistors. This application uses capacitive coupling instead of transformer coupling.

MD1 is tied high so MD0 functions as the mode control switch. When MD0 is low, the half current drive mode is selected. When MD0 is high the MB86962 is effectively removed from the circuit. The transceiver's AUI ports (DO, DI and CI) are disabled, isolating the MB86962 from the AUI. The MB86962 DI and CI ports go to a high impedance state and the DO port is ignored.

To implement an auto-select function, LEDL can be tied to MD0. This activates the transceiver/AUI interface when the TP link is active (data or link integrity pulses) and disables it when the link is inactive.



Note: LEDP/S status indications are shown in order of priority, i.e., Link Fail indication supersedes Jabber indication which supersedes Polarity Reverse (when PRC = 1). Reversed polarity conditions supersede Link Fail conditions when PRC = 0 (Polarity Correction Disabled). At the LEDL indicator, reversed polarity conditions are reported as Link Fail when PRC = 0. This allows the user to distinguish between actual link failure and apparent link failure due to polarity reversal.

Figure 1. LEDP/S Status indication Timing

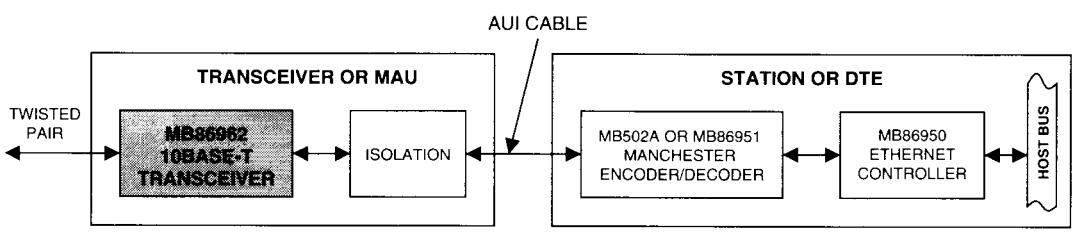


Figure 2. Typical System Diagram for External MAU

T-90-40

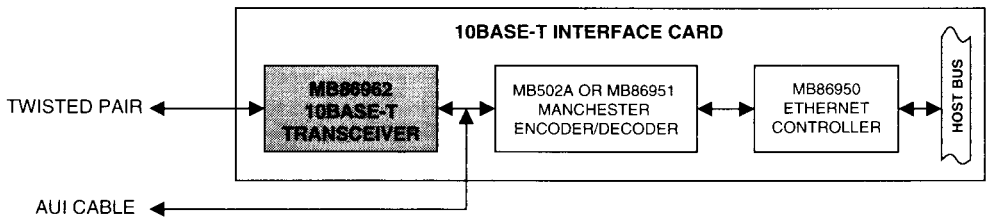


Figure 6. Typical System Diagram for Internal MAU

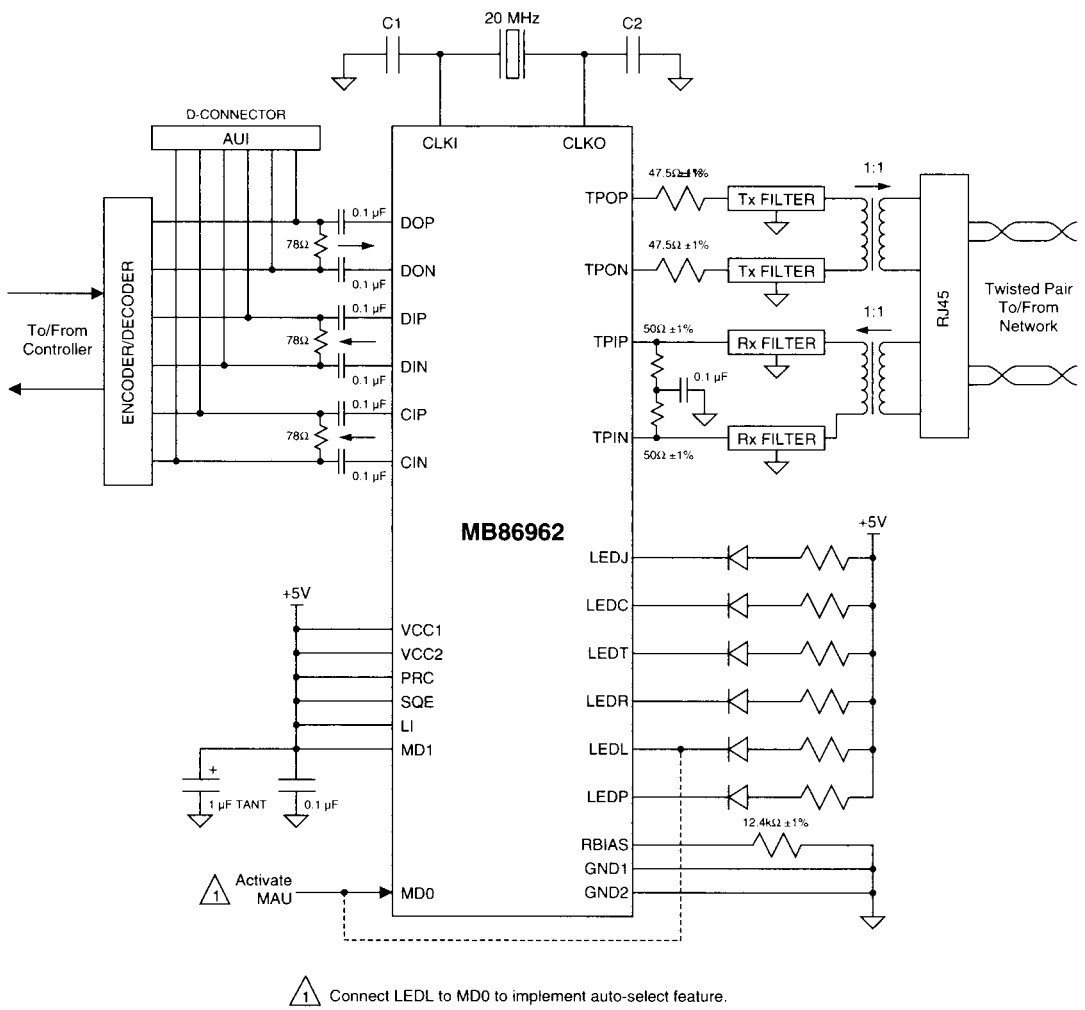


Figure 7. Connection Diagram for Internal MAU

FUNCTIONAL DESCRIPTION

The MB86962 interfaces the Attachment Unit Interface (AUI) to the unshielded twisted pair cables, transferring data in both directions between the two. The AUI side of the interface comprises three circuits: Data Output (DO), Data Input (DI) and Control Interface (CI). The twisted pair network side of the interface comprises two circuits: Twisted Pair Input (TPI) and Twisted Pair Output (TPO). In addition to the five basic circuits, the MB86962 contains an internal crystal oscillator, separate power and ground pins for analog and digital circuits, various logic controls and six LED drivers for status indications.

Functions are defined from the AUI side of the interface. The Transmit function refers to data transmitted by the Data Terminal Equipment (DTE) through the AUI and MAU to the twisted pair network. In addition to basic transmit and receive functions, the transceiver performs all required MAU functions defined by the IEEE 802.3 10BASE-T specifications such as collision detection, link integrity testing, Signal Quality Error (SQE), jabber control and loopback.

Several options are controlled by the MD0 and MD1 transceiver inputs. See Table 1 for a description of these functions.

TRANSMIT FUNCTION

The MB86962 transfers Manchester encoded data from the AUI port of the DTE (the DO circuit) to the twisted pair network (the TPO circuit). The output signal on TPON and TPOP is pre-distorted to meet the 10BASE-T jitter template, and filtered to meet FCC requirements. The output waveform (after the transmit filter) is shown in Figure 8. If the differential inputs at the DO circuit fall below 75% of the threshold level for eight bit times (typical), the MB86962 transmit function will enter the idle state. During idle periods, the MB86962 transmits link integrity test pulses on the TPO circuit.

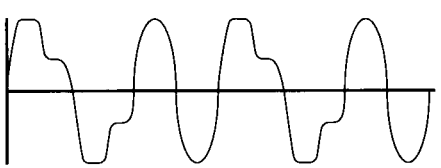


Figure 8. TPO Output Waveform

RECEIVE FUNCTION

The MB86962 receive function transfers serial data from the twisted pair network (the TPI circuit) to the DTE (over the DI circuit of the AUI). An internal squelch function discriminates noise from link test pulses and valid data streams. Only valid data streams activate the receive function. If the differential inputs at the TPI circuit fall below 75% of the threshold level (unsquelched) for eight bit times (typical), the MB86962 receive function will enter the idle state. The TPI threshold can be reduced by approximately 3 dB to allow for longer loops in low-noise environments. The reduced threshold is selected when MD1=0 and MD0=1.

POLARITY REVERSE FUNCTION

The MB86962 polarity reverse function uses both link pulses and end-of-frame data to determine the polarity of the received signal. A reversed polarity condition is detected when eight opposite receive link pulses are detected without receipt of a link pulse with the expected polarity. Reversed polarity is also detected if four frames are received with a reversed start-of-idle. Whenever polarity is reversed, these two counters are reset to zero. If the MB86962 enters the link fail state and no data or link pulses are received within 96 to 128 ms, the polarity is reset to the default non-flipped condition. (If Link Integrity is disabled, polarity detection is based only on received data pulses).

COLLISION DETECTION FUNCTION

The collision detection function operates on the twisted pair side of the interface. A collision is defined as the simultaneous presence of valid signals on both the TPI circuit and the TPO circuit. The MB86962 reports collisions to the AUI by sending a 10 MHz (CS0) signal over the CI circuit. The collision report signal is output no more than nine bit times after the chip detects a collision. If the TPI circuit becomes active while there is activity on the TPO circuit, the

Table 1. Mode Select Options

MD1	MD0	MODE
0	0	10BASE-T compliant MAU
0	1	Reduced squelch level
1	0	Half current AUI driver
1	1	DO, DI & CI ports disabled
Clock	0	Test Mode, Jabber enabled
Clock	1	Test Mode, Jabber disabled

TPI data is passed to the DTE over the DI circuit, disabling the loopback. Figure 9 is a state diagram of the MB86962 collision detection function (refer to IEEE 802.3 10BASE-T specification).

LOOPBACK FUNCTION

The loopback function operates in conjunction with the transmit function. Data transmitted by the DTE is internally looped back within the transceiver from the DO pins to the DI pins and returned to the DTE. The loopback function is disabled when a data collision occurs, clearing the DI circuit for the TPI data. Loopback is also disabled during link fail and jabber states.

SQE TEST FUNCTION

Figure 10 is a state diagram of the SQE test function. The SQE test function is enabled when the SQE pin is tied high. When enabled, the SQE test sequence is transmitted to the controller after every successful transmission on the 10BASE-T network. When a successful transmission is completed, the MB86962 transmits the SQE signal to the AUI over the CI circuit for 10±5 bit times. The SQE function can be disabled for hub applications by tying the SQE pin to ground.

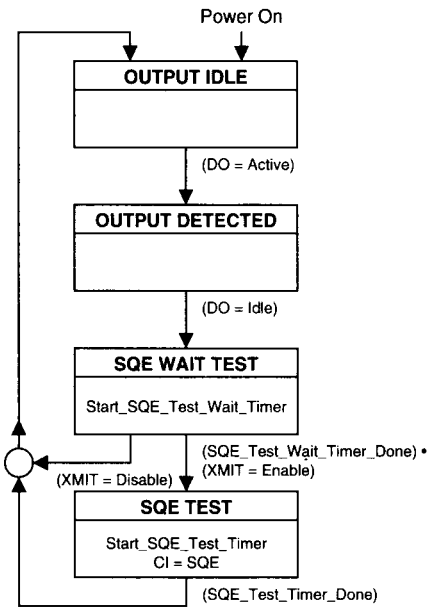


Figure 10. SQE Test Function

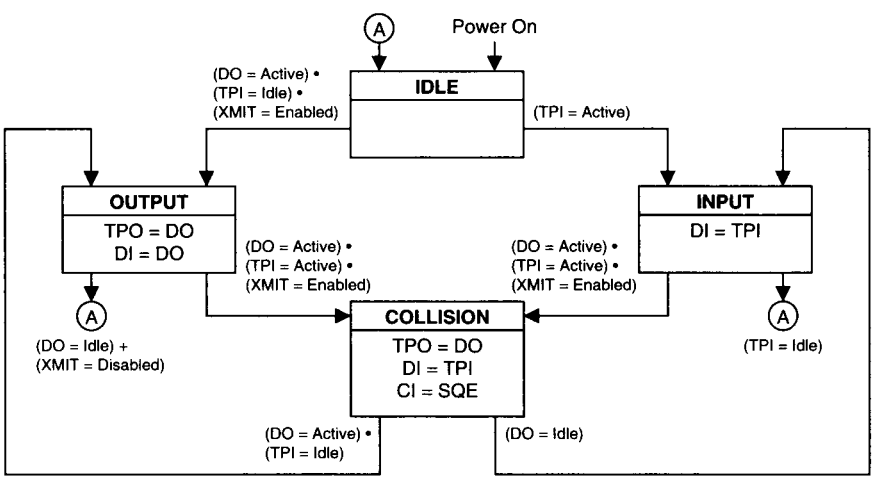


Figure 9. Collision Detection Function

JABBER CONTROL FUNCTION

Figure 11 is the state diagram for the MB86962 jabber control function. The MB86962 on-chip watchdog timer prevents the DTE from locking into a continuous transmit mode. When a transmission exceeds the time limit, the watchdog timer disables the transmit and loopback functions, and sends the SQE signal to the DTE over the CI circuit. Once the transceiver is in the jabber state, the DO circuit must remain idle for a period of 491 to 525 ms before it will exit the jabber state.

LINK INTEGRITY TEST FUNCTION

Figure 12 is the state diagram of the MB86962 link integrity test function. The link integrity test is used to determine the status of the receive side twisted pair cable and is enabled when the LI pin is tied high. When enabled, the receiver recognizes link integrity pulses which are transmitted in the absence of receive traffic. If no serial data stream or link integrity pulses are detected within 50 to 150 ms, the chip enters a link fail state and disables the transmit and loopback functions. The MB86962 ignores any link integrity pulse with an interval less than 2 to 7 ms. The MB86962 will remain in the link fail state until it detects either a serial data packet or two or more link integrity pulses.

TEST MODE

The MB86962 test mode is selected when a 2 to 2.5 MHz clock is input on the MD1 mode select pin. Test mode sets the internal counter chains to run at 1024 times their normal speed. The maximum transmit time, unjab time, link integrity timing and LED timing are reduced by a factor of 1024. During test operation, 10 MHz and 20 MHz signals are output on the PRC and SQE pins, respectively. When Test mode is selected, the SQE function cannot be disabled. In test mode the PRC function can be disabled by the LI pin. Jabber can be disabled by setting MD0=1.

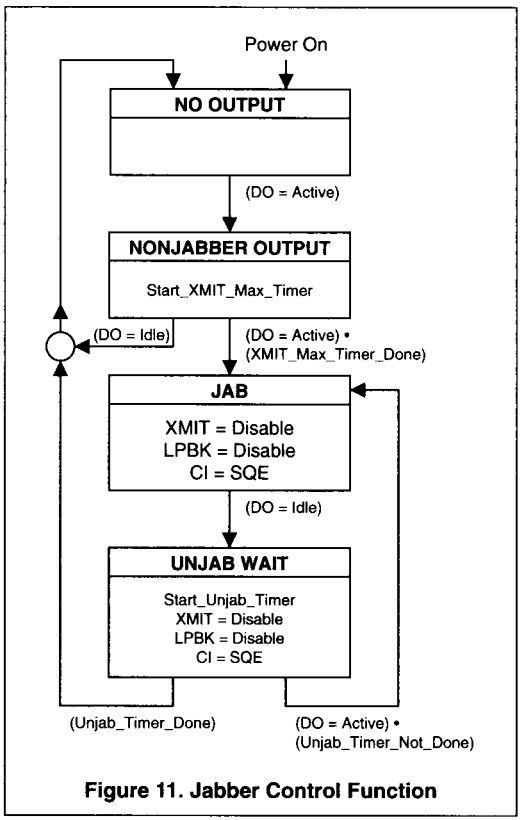


Figure 11. Jabber Control Function

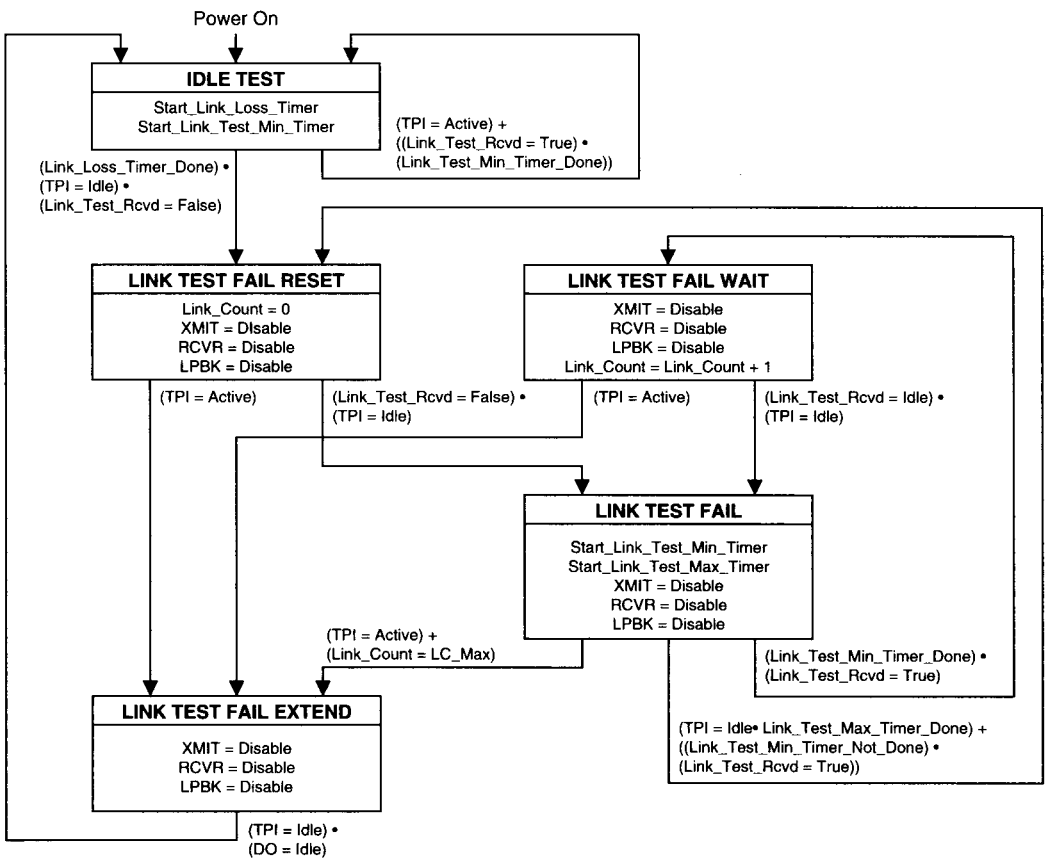


Figure 12. Link Integrity Test Function

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Conditions	Min.	Max.	Units
V_{CC}	Supply voltage		-0.3	6	V
V_I	Input voltage[2]		-0.5	V_{CC} + 0.5	V
V_O	Output voltage		-0.5	V_{CC} + 0.5	V
T_{STG}	Storage temperature		-65	150	°C

I/O DC SPECIFICATIONS T_A = 0°C to +70°C, V_{CC} = 5V ± 5%[3,4]

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IL}	Input low voltage[6]		-	-	0.8	V
V_{IH}	Input high voltage[6]		2.0	-	-	V
V_{OL}	Output low voltage (Open Drain LED Driver)[7]	R_{LOAD} = 2kΩ	-	-	0.13	V
I_{CC}	Power supply current (V_{CC1} = V_{CC2} = 5.25V)	Line Idle	-	60	69.3	mA
		Line Active, transmitting all ones	-	125	140	mA
I_{LI}	Input leakage current[8]	Input between V_{CC} and GND	-	±1	±10	µA
I_{LZ}	3-state leakage current	Output between V_{CC} and GND	-	±1	±10	µA

AUI DC SPECIFICATIONS T_A = 0°C to +70°C, V_{CC} = 5V ± 5%[3,4]

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{IL}	Input low current		-	-	-700	µA
I_{IH}	Input high current		-	-	500	µA
V_{OD}	Differential output voltage		±550	-	±1200	mV
V_{OB}	Differential voltage imbalance		-	-	±40	mV
V_{DS}	Differential squelch threshold		-	220	-	mV
R_Z	Receive input impedance	Between DOP and DON	-	20	-	kΩ

TRANSMIT SPECIFICATIONS T_A = 0°C to +70°C, V_{CC} = 5V ± 5%[3,4]

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Z_{OUT}	Transmit output impedance		-	5	-	Ω
V_{OD}	Peak differential output voltage	Load = 200Ω at TPOP and TPON	±4.5	-	±5.2	V
V_{OB}	Differential voltage imbalance	Load = 200Ω at TPOP and TPON	-	-	±40	mV
-	Transmit timing jitter addition	After Tx filter, 0 line length	-	-	±8	ns
		After Tx filter, line model as shown in 10BASE-T draft #10	-	-	±3.5	ns

RECEIVE SPECIFICATIONS T_A = 0°C to +70°C, V_{CC} = 5V ± 5%[3,4]

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Z_{IN}	Receive input impedance	Between TPIP/TPIN	-	20	-	kΩ
V_{DS}	Differential squelch threshold		-	420	-	mV
V_{DSR}	Reduced squelch threshold		-	300	-	mV
-	Receive timing jitter		-	-	1.5	ns

JABBER TIMING T_A = 0°C to +70°C, V_{CC} = 5V ± 5%[3,4]

Symbol	Parameter Description	Min.	Typ.	Max.	Units
t1	Maximum transmit time[5]	98.5	-	131	ms
t2	Unjab time[5]	491	-	525	ms
t3	Time from Jabber to CS0 on CIP/CIN	0	-	900	ns

LINK INTEGRITY TIMING T_A = 0°C to +70°C, V_{CC} = 5V ± 5%[3,4]

Symbol	Parameter Description	Min.	Typ.	Max.	Units
t1	Time link loss[5]	65	-	66	ms
t2	Time between Link Integrity Pulses[5]	9	-	11	ms
t3	Interval for valid receive Link Integrity Pulses[5]	4.1	-	65	ms

COLLISION TIMING T_A = 0°C to +70°C, V_{CC} = 5V ± 5%[3,4]

Symbol	Parameter Description	Min.	Typ.	Max.	Units
t1	Simultaneous TPI/TPO to CS0 state on CIN/CIP	0	-	900	ns
t2	DO loopback to TPI on DI	300	-	900	ns
t3	CS0 state delay after TPI/DO idle	-	-	900	ns
t3	CS0 high pulse width	40	-	60	ns
t3	CS0 low pulse width	40	-	60	ns
t3	CS0 frequency	-	10	-	MHz

SQE TIMING T_A = 0°C to +70°C, V_{CC} = 5V ± 5%[3,4]

Symbol	Parameter Description	Min.	Typ.	Max.	Units
t1	SQE signal duration	500	-	1500	ns
t2	Delay after last positive transition	0.6	-	1.6	µs

LED TIMING T_A = 0°C to +70°C, V_{CC} = 5V ± 5%[3,4]

Symbol	Parameter Description	Min.	Typ.	Max.	Units
t1	LEDC, LEDT, LEDR on time[5]	100	-	-	ms
t2	LEDP/S on time[5] (See Figure 1)	-	164	-	ms
t2	LEDP/S period[5] (See Figure 1)	-	328	-	ms

GENERAL TIMING T_A = 0°C to +70°C, V_{CC} = 5V ± 5%[3,4]

Symbol	Parameter Description	Min.	Typ.	Max.	Units
t1	Receive start-up delay	0	-	500	ns
t2	Transmit start-up delay	0	-	200	ns
t2	Loopback start-up delay	0	-	500	ns

Notes:

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operation section of this specification is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods may affect device reliability.
2. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is recommended that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
3. Parameters are valid over specified temperature range and supply voltage range unless otherwise noted. Typical parameters are at 25°C and are for design aid only.
4. Maximum voltage differential between V_{CC1} and V_{CC2} must not exceed 0.3V.
5. Switching times reduced by a factor of 1024 in test mode.
6. Applies to MD0, MD1, SQE, PRC and LI pins.
7. LED drivers can sink up to 10mA.
8. Not including TPIN, TPIP, DOP or DON.

NOTES

This document is published by the marketing department of Fujitsu Microelectronics, Inc., Advanced Products Division, 77 Rio Robles, San Jose, California, U.S.A. 95134-1807.