FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-22115-3E

ASSP IPsec Engine

High-Speed IPsec Processing Engine

MB86978

■ DESCRIPTION

MB86978 is IPsec accelerator engine of Inline Architecture. Once setup with appropriate parameters, the device can perform bi-directional 100 Mbps IPsec processing at full wire speed.

■ FEATURES

- Built-in RMII/MII interface of two ports

  One interface for WAN (internet) side and one for routing function side
  - Complies with IEEE802.3 (DIX format)
  - Supports 10/100BASE-T/TX, full/half-duplex, and auto-negotiation
  - IEEE 802.3x flow control supported
  - Half-duplex back pressure supported
  - SMI interface for PHY device control

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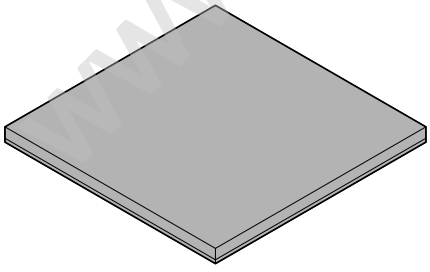
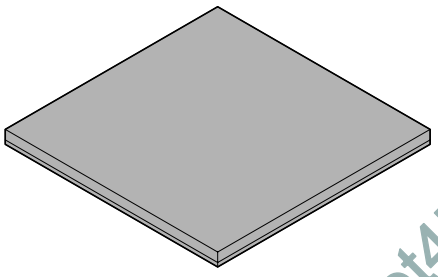
■ PACKAGE

337-pin plastic FBGA



BGA-337P-M02

288-pin plastic FBGA



BGA-288P-M13

- Built-in engine for IKE processing

  To speed up the calculation processing of IKE, the following functional block is built-in. When IPsec is processed in host CPU, this encryption engine and the authentication engine can be used.
  - DES/3DES : Encryption engine
  - AES : Encryption engine
  - SHA-1 : Authentication engine
  - MD5 : Authentication engine
  - IKE support : Surplus operation engine for RSA and DH processing acceleration

- Built-in Inline type IPsec processing engine

  To execute the IPsec processing of a full wire with Inline IPsec, the following functions are installed.

  (1) Full wire code engine

  DES/3DES (CBC mode)
  AES (CBC mode, Length of key128/192/256 bit)

  (2) Full wire attestation engine

  HMAC-SHA-1-96
  HMAC-MD5-96

- It provides with the SA (Security association) data base.
  - SA of 64 can be set. (direction of encode : 64 and decode direction : 64)
  - IPv4/IPv6 both correspondence
  - It is possible to correspond to the following modes.
    - Transport mode (ESP, AH, AH, ESP)
    - Tunnel mode (ESP, AH)
    - Transport over tunnel mode
  - The following parameters can be specified for a selector.
    Address Internet Protocol address, Transmission former Internet Protocol address, Address TCP/UDP port number, Transmission former TCP/UDP port number, Protocol in AH SPI, ESP SPI, and transport layer, IPsec protocol, TOS field, Flow label, Traffic class
  - Replay defense function supported
  - NAT-Traversal supported
  - IP over PPPoE frame supported
  - IP over VLAN frame supported
  - IV value count up mode/random mode supported

- The SA database can be expanded

  To connect the LSI (MB86979) for enhancing SADB externally, the SA database can be enhanced. Up to 4096 (512×8) SA can be supported (encode direction : 4096, decode direction : 4096) .

- F mode supported

  The routing function side can add the IPsec SA value to the Ethernet frame as an SA tag and pass this to the MB86978 for IPsec processing.

- Packet division supported

  The packet that does MTU exaggerated size by the IPsec processing is divided in LSI automatically. Processing is performed at wire speed.

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- Host interface

  Includes a general-purpose I/O interface for connection to a wide range of CPUs.
  Capable of switching between 16-bit bus mode and 32-bit bus mode.

- Speed-up of routing function part

  By connecting an external high-speed IP forwarding engine (MB86977) , IPsec processing and routing processing can both be performed bi-directionally at full wire speed.

- Others
  - Process : 0.18 µm process
  - Power-supply voltage : 1.8 V/3.3 V dual power supplies
  - Operation frequency : Max 66 MHz
  - Package : 337-pin plastic FBGA, 288-pin plastic FBGA

■ PIN ASSIGNMENT

• 337-pin FBGA

No.	Symbol	No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
A1	N.C.	AE16	CMDD	A19	VDDI	AC2	ADD6	H24	UPRID	P3	D27
B1	N.C.	AE17	GND	A18	TXENA	AD2	ADD9	G24	XMATCHD	R3	N.C.
C1	N.C.	AE18	CLD2E	A17	TXD0A	AD3	GND	F24	TDI	T3	GND
D1	GND	AE19	N.C.	A16	TXD2A	AD4	VDDI	E24	N.C.	U3	GND
E1	D0	AE20	VDDI	A15	TXENB	AD5	VDDI	D24	N.C.	V3	VDDI
F1	D2	AE21	CLD0D	A14	TXD2B	AD6	SAADD1	C24	N.C.	W3	VDDI
G1	D4	AE22	CLD2D	A13	VDDE	AD7	SAADD4	B24	TMS	Y3	N.C.
H1	D7	AE23	VDDI	A12	VDDE	AD8	SAADD6	B23	RXCLKA	AA3	VDDE
J1	D10	AE24	N.C.	A11	RXCLKB	AD9	SAADD9	B22	RXD0A	AB3	ADD4
K1	D13	AE25	GND	A10	RXD0B	AD10	SAADD12	B21	RXD2A	AC3	ADD7
L1	D16	AD25	VDDE	A9	RXD1B	AD11	SAADD15	B20	COLA	AC4	N.C.
M1	D19	AC25	N.C.	A8	RXD3B	AD12	SAADD18	B19	VDDE	AC5	N.C.
N1	D22	AB25	SAD0	A7	GND	AD13	XSARE	B18	VDDE	AC6	SAADD2
P1	D25	AA25	SAD2	A6	VDDI	AD14	XPKTE	B17	TXD1A	AC7	GND
R1	D28	Y25	SAD4	A5	N.C.	AD15	XPKTD	B16	TXD3A	AC8	SAADD7
T1	D30	W25	SAD7	A4	VDDI	AD16	VDDE	B15	TXD0B	AC9	SAADD10
U1	VDDI	V25	SAD10	A3	VDDI	AD17	VDDE	B14	TXD3B	AC10	SAADD13
V1	VDDI	U25	SAD13	A2	N.C.	AD18	CLD3E	B13	VDDI	AC11	SAADD16
W1	CLK	T25	SAD16	B2	N.C.	AD19	VDDE	B12	TXCLKB	AC12	N.C.
Y1	XCS	R25	SAD19	C2	N.C.	AD20	VDDE	B11	CRSB	AC13	XRSTOUT
AA1	XRE	P25	SAD22	D2	N.C.	AD21	CLD1D	B10	RXDVB	AC14	CMDE
AB1	ADD2	N25	SAD25	E2	D1	AD22	CLD3D	B9	RXD2B	AC15	GND
AC1	ADD5	M25	SAD28	F2	D3	AD23	N.C.	B8	MDCB	AC16	CLD0E
AD1	ADD8	L25	SAD30	G2	D5	AD24	N.C.	B7	VDDI	AC17	CLD1E
AE1	N.C.	K25	VDDE	H2	D8	AC24	GND	B6	MDIOA	AC18	N.C.
AE2	VDDE	J25	VDDE	J2	D11	AB24	SAD1	B5	VDDE	AC19	N.C.
AE3	ADD10	H25	UPRIE	K2	D14	AA24	SAD3	B4	VDDE	AC20	VDDI
AE4	VDDE	G25	XMATCHE	L2	D17	Y24	SAD5	B3	N.C.	AC21	N.C.
AE5	XINT	F25	XTCK	M2	D20	W24	SAD8	C3	N.C.	AC22	N.C.
AE6	SAADD0	E25	REFCLK	N2	D23	V24	SAD11	D3	N.C.	AC23	VDDI
AE7	SAADD3	D25	N.C.	P2	D26	U24	SAD14	E3	N.C.	AB23	GND
AE8	SAADD5	C25	N.C.	R2	D29	T24	SAD17	F3	GND	AA23	N.C.
AE9	SAADD8	B25	N.C.	T2	D31	R24	SAD20	G3	D6	Y23	SAD6
AE10	SAADD11	A25	N.C.	U2	GND	P24	SAD23	H3	D9	W23	SAD9

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No.	Symbol	No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
AE11	SAADD14	A24	TRST	V2	XRST	N24	SAD26	Y22	VDDI	D21	N.C.
AE12	SAADD17	A23	RXDVA	W2	MODE16	M24	SAD29	J3	D12	V23	SAD12
AE13	XSAWE	A22	RXD1A	Y2	XWE	L24	SAD31	K3	D15	U23	SAD15
AE14	XCMDDVE	A21	CRSA	AA2	GND	K24	VDDI	L3	D18	T23	SAD18
AE15	XCMDDVD	A20	TXCLKA	AB2	ADD3	J24	XSAINTE	M3	D21	R23	SAD21
N23	SAD27	C16	TDO	H4	N.C.	AB7	N.C.	N3	D24	P23	SAD24
M23	N.C.	C15	TXD1B	J4	GND	AB8	VDDE	W22	GND	D20	GND
L23	VDDI	C14	MDCA	K4	GND	AB9	GND	V22	VDDE	D19	GND
K23	GND	C13	VDDI	L4	VDDE	AB10	VDDI	U22	GND	D18	N.C.
J23	XSAINTD	C12	N.C.	M4	VDDI	AB11	N.C.	T22	GND	D17	N.C.
H23	N.C.	C11	COLB	N4	GND	AB12	GND	R22	N.C.	D16	GND
G23	VDDI	C10	RXERB	P4	GND	AB13	GND	P22	VDDI	D15	N.C.
F23	N.C.	C9	VDDE	R4	GND	AB14	N.C.	N22	VDDE	D14	VDDI
E23	N.C.	C8	N.C.	T4	N.C.	AB15	N.C.	M22	GND	D13	GND
D23	N.C.	C7	VDDE	U4	VDDE	AB16	N.C.	L22	N.C.	D12	GND
C23	TCK	C6	MDIOB	V4	VDDE	AB17	VDDI	K22	GND	D11	N.C.
C22	RXERA	C5	N.C.	W4	N.C.	AB18	VDDI	J22	GND	D10	N.C.
C21	RXD3A	C4	N.C.	Y4	N.C.	AB19	N.C.	H22	N.C.	D9	VPD
C20	N.C.	D4	N.C.	AA4	N.C.	AB20	GND	G22	VDDI	D8	N.C.
C19	VDDI	E4	VDDI	AB4	N.C.	AB21	GND	F22	N.C.	D7	N.C.
C18	N.C.	F4	GND	AB5	GND	AB22	VDDE	E22	GND	D6	GND
C17	VDDI	G4	N.C.	AB6	VDDI	AA22	GND	D22	VDDI	D5	GND

• 288-pin FBGA

No.	Symbol	No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
A1	N.C.	AB18	CLD2D	A9	RXDVB	AA13	XPKTD	B10	RXCLKB	Y16	GND
B1	D0	AB19	N.C.	A8	RXD2B	AA14	VDDI	B9	RXD0B	Y17	VDDE
C1	D1	AB20	VDDE	A7	RXERB	AA15	CLD1E	B8	RXD3B	Y18	VDDI
D1	D2	AB21	VDDI	A6	MDIOA	AA16	CLD3E	B7	MDCB	Y19	N.C.
E1	D4	AB22	N.C.	A5	VDDE	AA17	CLD1D	B6	MDIOB	Y20	GND
F1	D7	AA22	SAD0	A4	N.C.	AA18	CLD3D	B5	VDDE	W20	SAD5
G1	D10	Y22	SAD1	A3	N.C.	AA19	N.C.	B4	VDDI	V20	SAD8
H1	D13	W22	SAD3	A2	N.C.	AA20	GND	B3	N.C.	U20	SAD11
J1	D16	V22	SAD6	B2	GND	AA21	VDDE	C3	N.C.	T20	SAD14
K1	D19	U22	SAD9	C2	GND	Y21	SAD2	D3	VDDI	R20	VDDI
L1	D22	T22	SAD12	D2	D3	W21	SAD4	E3	D6	P20	VDDE
M1	D25	R22	SAD15	E2	D5	V21	SAD7	F3	D9	N20	SAD21
N1	D28	P22	SAD17	F2	D8	U21	SAD10	G3	D12	M20	SAD24
P1	D31	N22	SAD19	G2	D11	T21	SAD13	H3	D15	L20	SAD27
R1	XRST	M22	SAD22	H2	D14	R21	SAD16	J3	D18	K20	GND
T1	CLK	L22	SAD25	J2	D17	P21	SAD18	K3	D21	J20	VDDE
U1	XCS	K22	SAD28	K2	D20	N21	SAD20	L3	D24	H20	VDDI
V1	ADD2	J22	SAD30	L2	D23	M21	SAD23	M3	D27	G20	VDDI
W1	ADD5	H22	XSAINTE	M2	D26	L21	SAD26	N3	D30	F20	XMATCHD
Y1	ADD8	G22	UPRIE	N2	D29	K21	SAD29	P3	VDDE	E20	TDI
AA1	VDDE	F22	XMATCHE	P2	VDDE	J21	SAD31	R3	GND	D20	N.C.
AB1	N.C.	E22	REFCLK	R2	GND	H21	GND	T3	MODE16	C20	TRST
AB2	VDDI	D22	N.C.	T2	GND	G21	UPRID	U3	XRE	C19	VDDI
AB3	VDDI	C22	N.C.	U2	XWE	F21	XSAINTD	V3	ADD4	C18	CRSA
AB4	XINT	B22	N.C.	V2	ADD3	E21	XTCK	W3	ADD7	C17	COLA
AB5	SAADD0	A22	N.C.	W2	ADD6	D21	N.C.	Y3	ADD10	C16	VDDI
AB6	SAADD3	A21	RXERA	Y2	ADD9	C21	N.C.	Y4	GND	C15	TXD1A
AB7	SAADD6	A20	TCK	AA2	VDDE	B21	VDDI	Y5	SAADD2	C14	TDO
AB8	SAADD9	A19	RXDVA	AA3	VDDE	B20	TMS	Y6	SAADD5	C13	TXD1B
AB9	SAADD12	A18	RXD0A	AA4	GND	B19	RXCLKA	Y7	SAADD8	C12	VDDI
AB10	SAADD15	A17	RXD2A	AA5	SAADD1	B18	RXD1A	Y8	SAADD11	C11	VDDI
AB11	SAADD18	A16	TXCLKA	AA6	SAADD4	B17	RXD3A	Y9	SAADD14	C10	CRSB
AB12	XCMDDVE	A15	TXENA	AA7	SAADD7	B16	VDDI	Y10	SAADD17	C9	RXD1B
AB13	XCMDDVD	A14	TXD2A	AA8	SAADD10	B15	TXD0A	Y11	XSARE	C8	COLB
AB14	VDDE	A13	TXENB	AA9	SAADD13	B14	TXD3A	Y12	CMDE	C7	GND
AB15	CLD0E	A12	TXD2B	AA10	SAADD16	B13	TXD0B	Y13	CMDD	C6	GND
AB16	CLD2E	A11	MDCA	AA11	XSAWE	B12	TXD3B	Y14	VDDI	C5	GND
AB17	CLD0D	A10	TXCLKB	AA12	XPKTE	B11	GND	Y15	VDDE	C4	VDDI

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No.	Symbol	No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
D4	N.C.	P4	VDDI	W9	VDDI	W19	N.C.	J19	GND	D14	GND
E4	GND	R4	VDDI	W10	GND	V19	GND	H19	VDDI	D13	VDDI
F4	N.C.	T4	VDDI	W11	GND	U19	N.C.	G19	VDDE	D12	VDDE
G4	GND	U4	VDDI	W12	XRSTOUT	T19	GND	F19	VDDI	D11	VDDE
H4	GND	V4	GND	W13	GND	R19	GND	E19	GND	D10	GND
J4	VDDE	W4	N.C.	W14	GND	P19	GND	D19	N.C.	D9	VPD
K4	VDDI	W5	GND	W15	VDDE	N19	GND	D18	VDDE	D8	VDDE
L4	GND	W6	VDDI	W16	VDDI	M19	VDDI	D17	GND	D7	VDDE
M4	GND	W7	VDDE	W17	VDDI	L19	VDDE	D16	VDDE	D6	VDDI
N4	GND	W8	GND	W18	GND	K19	GND	D15	GND	D5	VDDI

■ PIN DESCRIPTION

• Host (SRAM) interface

Symbol	Pin name	I/O	Description
ADD2 to ADD10	Address Bus	I	Address input from host CPU
D0 to D31	Data input/output	I/O	Data bus of host CPU
XCS	Chip Select	I	Selection signal input from host CPU (Low active)
XWE	Write Enable	I	Write signal input from host CPU (Low active)
XRE	Read Enable	I	Read signal input from host CPU (Low active)
XINT	Host Interrupt	O	Interrupt output signal to host CPU (Low active)
MODE16	Host CPU Bus Mode	I	Host CPU bus width selection mode 1 : 16 bit mode, 0 : 32 bit mode

• Interface for extended SADB chip connection

Symbol	Pin name	I/O	Description
XRSTOUT	Reset for Ext-SADB	O	Reset output signal to extended SADB chip (Low active)
XCMDDVE	Encryption Command Valid Signal	O	Encode side command effective notification signal to extended SADB chip (Low active)
CMDE	Encryption Command Signal	O	Encode side command signal to extended SADB chip
XPKTE	Encryption Packet Valid Signal	O	Encode side packet effective notification signal to extended SADB chip (Low active)
XMATCHE	Ext-SADB Encryption Side Match Signal	I	Encode side match signal from extended SADB chip (Low active)
CLD0E CLD1E CLD2E CLD3E	Encryption Classifier Data	I/O	Data bus for encode side extended SADB Used when encoding to output the search data and to input the search result from the extended SADB chip.
XCMDDVD	Decryption Command Valid Signal	O	Decode side command effective notification signal to extended SADB chip (Low active)
CMDD	Decryption Command Signal	O	Decode side command signal to extended SADB chip
XPKTD	Decryption Packet Valid Signal	O	Decode side packet effective notification signal to extended SADB chip (Low active)
XMATCHD	Ext-SADB Decryption Side Match Signal	I	Decode side match signal from enhancing SADB chip (Low active)
CLD0D CLD1D CLD2D CLD3D	Decryption Classifier Data	I/O	Data bus for decode side extended SADB Used when decoding to output the search data and to input the search result from the extended SADB chip.
UPRIE	Ext-SADB Encryption Side First Match Signal	I	The first match signal from encode side of extended SADB chip (High active)
UPRID	Ext-SADB Decryption Side First Match Signal	I	The first match signal from decode side of extended SADB chip (High active)

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Symbol	Pin name	I/O	Description
XSAWE	Ext-SADB Write Enable Signal	O	Data write enable signal to extended SADB chip (Low active)
XSARE	Ext-SADB Read Enable Signal	O	Data read enable signal to extended SADB chip (Low active)
SAADD0 to SAADD18	Ext-SADB Address Bus	O	Address bus to extended SADB chip
SAD0 to SAD31	Ext-SADB Data Bus	I/O	Data bus to extended SADB chip
XSAINTE	Ext-SADB Encryption Side Interrupt	I	Interruption signal from encode side of extended SADB chip (Low active)
XSAINTD	Ext-SADB Decryption Side Interrupt	I	Interruption signal from decode side of extended SADB chip (Low active)

- RMII interface (2 port)

Symbol	Pin name	I/O	Description
REFCLK	Reference Clock	I	Reference clock input Synchronous signal of RMII when transmitting and receiving Frequency : 50 MHz
TXD0A TXD1A	Transmit Data for Router Side	O	Transmission data output bus of router side
TXD0B TXD1B	Transmit Data for WAN Side	O	Transmission data output bus of WAN side
TXENA	Transmit Enable for Router Side	O	Transmission enable output of router side (High active)
TXENB	Transmit Enable for WAN Side	O	Transmission enable output of WAN side (High active)
RXERA	Receive Error for Router Side	I	Reception error input of router side (High active)
RXERB	Receive Error for WAN Side	I	Reception error input of WAN side (High active)
RXD0A RXD1A	Receive Data for Router Side	I	Receive data input bus of router side
RXD0B RXD1B	Receive Data for WAN Side	I	Receive data input bus of WAN side
CRSA	Carrier Sense / Receive Data Valid for Router Side	I	Carrier sense/receive data effective signal input of router side (High active)
CRSB	Carrier Sense / Receive Data Valid for WAN Side	I	Carrier sense/receive data effective signal input of WAN side (High active)

Note : The detection of the collision in half duplex is achieved by taking AND of CRS and TXEN.

• MII interface (2 port)

Symbol	Pin name	I/O	Description
TXCLKA	TX CLOCK for Router Side	I	Clock input for transmission of router side 2.5 MHz at 10BASE, 25 MHz at 100BASE
TXCLKB	TX CLOCK for WAN Side	I	Clock input for transmission of WAN side 2.5 MHz at 10BASE, 25 MHz at 100BASE
TXD0A to TXD3A	Transmit Data for Router Side	O	Transmission data bus of router side The lower two bits are shared with RMII.
TXD0B to TXD3B	Transmit Data for WAN Side	O	Transmission data bus of WAN side The lower two bits are shared with RMII.
TXENA	Transmit Enable for Router Side	O	Transmission data effective signal output of router side (High active)
TXENB	Transmit Enable for WAN Side	O	Transmission data effective signal output of WAN side (High active)
RXCLKA	RX CLOCK for Router Side	I	Clock input for reception of router side 2.5 MHz at 10BASE, 25 MHz at 100BASE
RXCLKB	RX CLOCK for WAN Side	I	Clock input for reception of WAN side 2.5 MHz at 10BASE, 25 MHz at 100BASE
RXERA	Receive Error for Router Side	I	Reception error input of router side Shared with RMII. (High active)
RXERB	Receive Error for WAN Side	I	Reception error input of WAN side Shared with RMII. (High active)
RXDVA	Receive Data Valid for Router Side	I	Receive data effective signal input of router side (High active)
RXDVB	Receive Data Valid for WAN Side	I	Receive data effective signal input of WAN side (High active)
CRSA	Carrier Sense for Router Side	I	Carrier sense signal input of router side (High active)
CRSB	Carrier Sense for WAN Side	I	Carrier sense signal input of WAN side (High active)
RXD0A to RXD3A	Receive Data for Router Side	I	Receive data bus of router side The lower two bits are shared with RMII.
RXD0B to RXD3B	Receive Data for WAN Side	I	Receive data bus of WAN side The lower two bits are shared with RMII.
COLA	Collision Detect for Router Side	I	Collision detection input signal for router side (High active)
COLB	Collision Detect for WAN Side	I	Collision detection input signal for WAN side (High active)

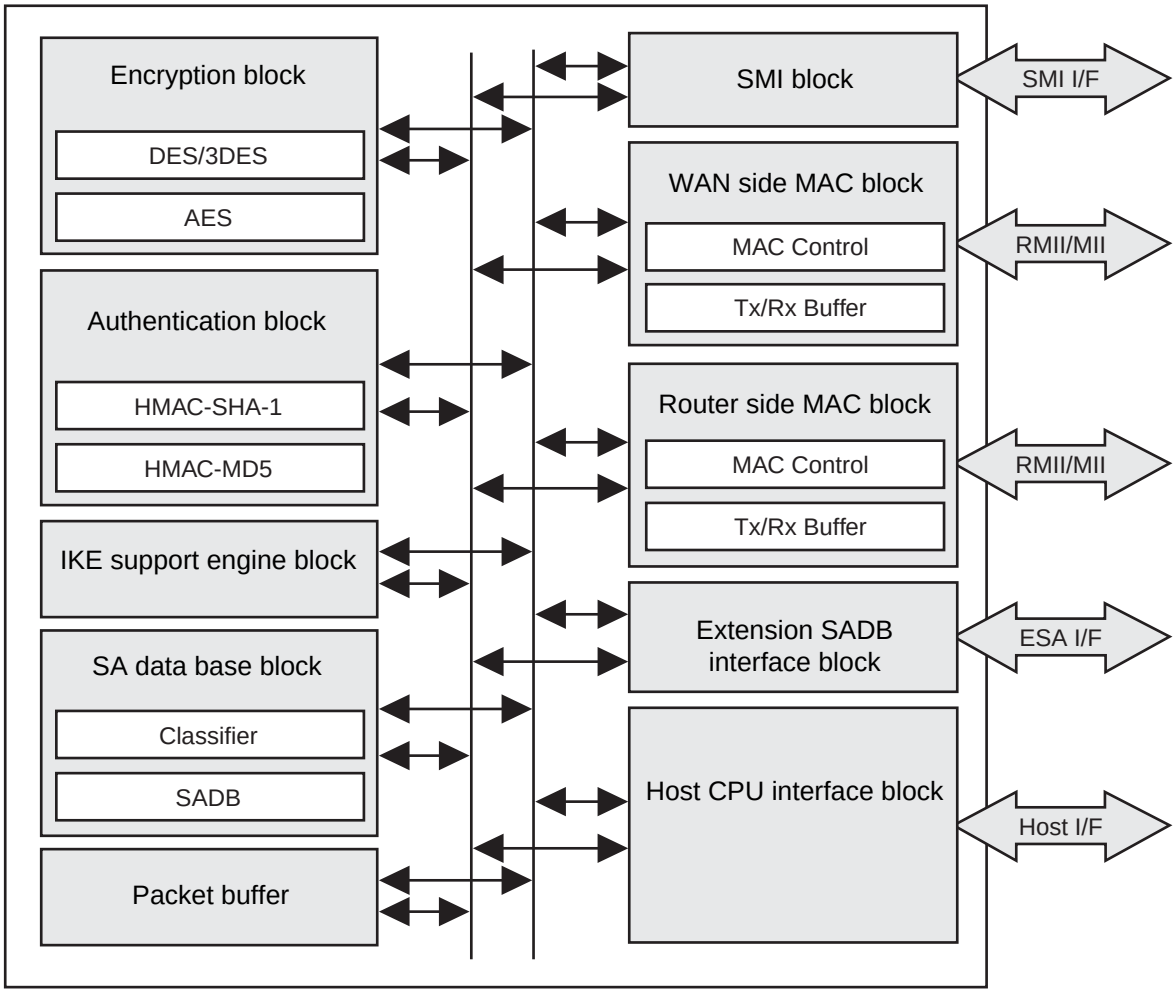
• SMI interface

Symbol	Pin name	I/O	Description
MDCA	Management Data Clock for PHY Device	O	SMI clock output Connect to the SMI clock of the PHY device.
MDIOA	Management Data input/output for PHY Device	I/O	SMI data input/output Connect to SMI data of the PHY device. This terminal is connected by wire to multiple PHY devices.
MDCB	Management Data Clock for Direct MII Connection	I	SMI clock input (direct MII) Used when connecting MII directly and not via PHY device. Input the SMI clock output from the opposing SMI controller.
MDIOB	Management Data input/output for Direct MII Connection	I/O	SMI data input/ output (direct MII) Used when connecting MII directly and not via PHY device. Connect it with the SMI data signal.

• Others

Symbol	Pin name	I/O	Description
XRST	System Reset	I	Reset input signal
CLK	System Clock	I	Clock input signal
TRST	JTAG Reset	I	Reset input signal for JTAG (33 kΩ Pull-up in the I/O cell). Input the same reset signal as XRST.
TMS	JTAG Mode	I	Mode setting signal for JTAG (33 kΩ Pull-up in the I/O cell).
TCK	JTAG Clock	I	Clock input signal for JTAG (33 kΩ Pull-up in the I/O cell).
TDI	JTAG Data Input	I	Data input signal for JTAG (33 kΩ Pull-up in the I/O cell).
TDO	JTAG Data Output	O	Data output for JTAG
VPD XTCK	—	I	Connect to ground.
VDDE	—	—	3.3 V system power supply terminal
VDDI	—	—	1.8 V system power supply terminal
GND	—	—	Grand terminal

■ BLOCK DIAGRAM



■ BLOCK DESCRIPTION

- Encryption block

  The block with the encoding function and the decoding function of DES, 3DES, and AES used when IPsec is processed.

- Authentication block

  The block with the HMAC-SHA-1-96 and HMAC-MD5-96 function used when IPsec is processed.

- IKE support engine block

  The block with the following each engine that host CPU uses in the IKE phase.

DES/3DES	: Encryption engine
AES	: Encryption engine
SHA-1	: Authentication engine
MD5	: Authentication engine
IKE support	: Surplus operation engine for RSA and DH processing acceleration

- SA data base block

  Contains an internal classifier table for selecting the IPsec SA. When a packet is received, the SA corresponding to the selector set in the classifier table is selected. An internal database (SADB table) is also provided to store the policy and parameters to use for IP processing based on the selected SA.

- Packet buffer

  This is the buffer to maintain the received packet and the packet before it transmits temporarily.

- Host CPU interface block

  This is the interface block for connecting to the host CPU. This block is also used for register read/write and handling of log data. An interrupt signal and status register are used to notify the host CPU when a packet is received.

- Extension SADB interface block

  This block controls the local interface used when an extension SADB is connected externally to increase the number of SAs.

- MAC block

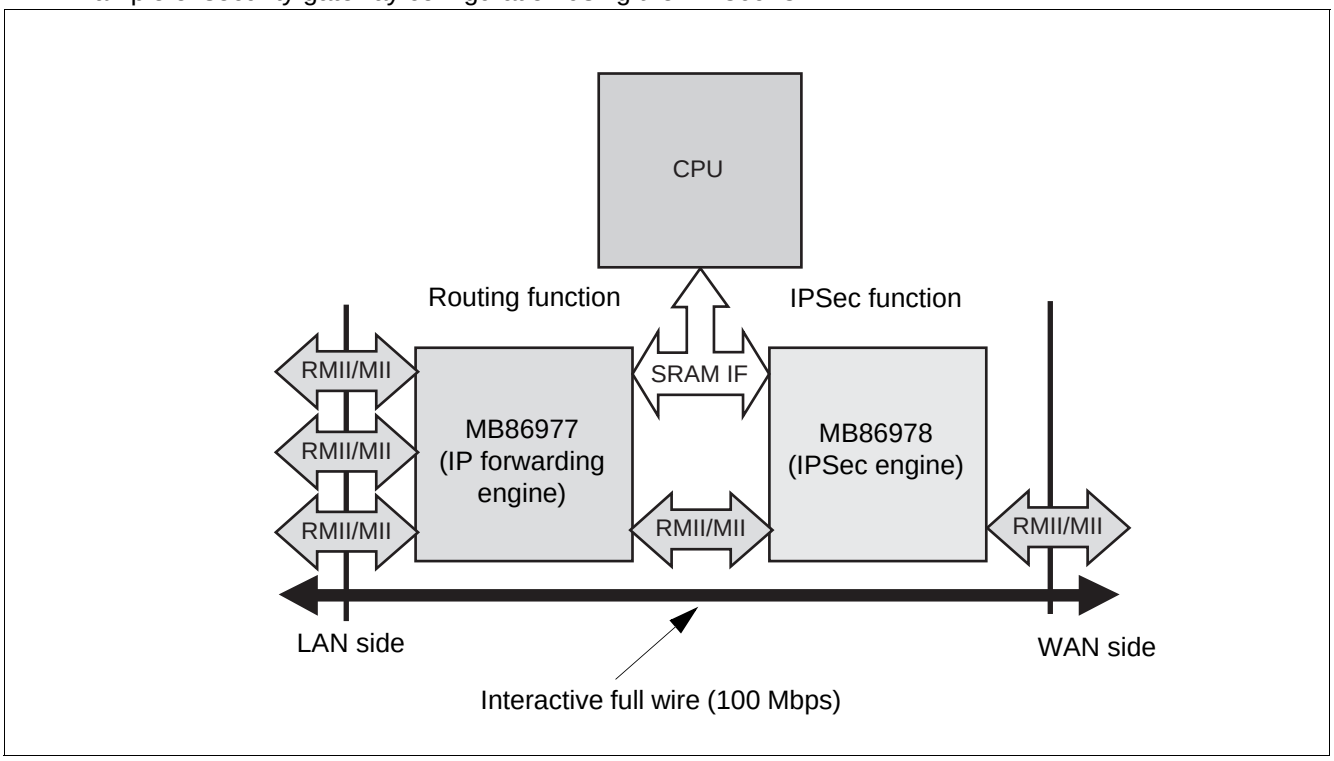
  Packets are transmitted and received via the RMII or MII interface. The Layer 2 (MAC) functions specified by IEEE 802.3 are executed. One port are on the WAN side and the router side.

- SMI block

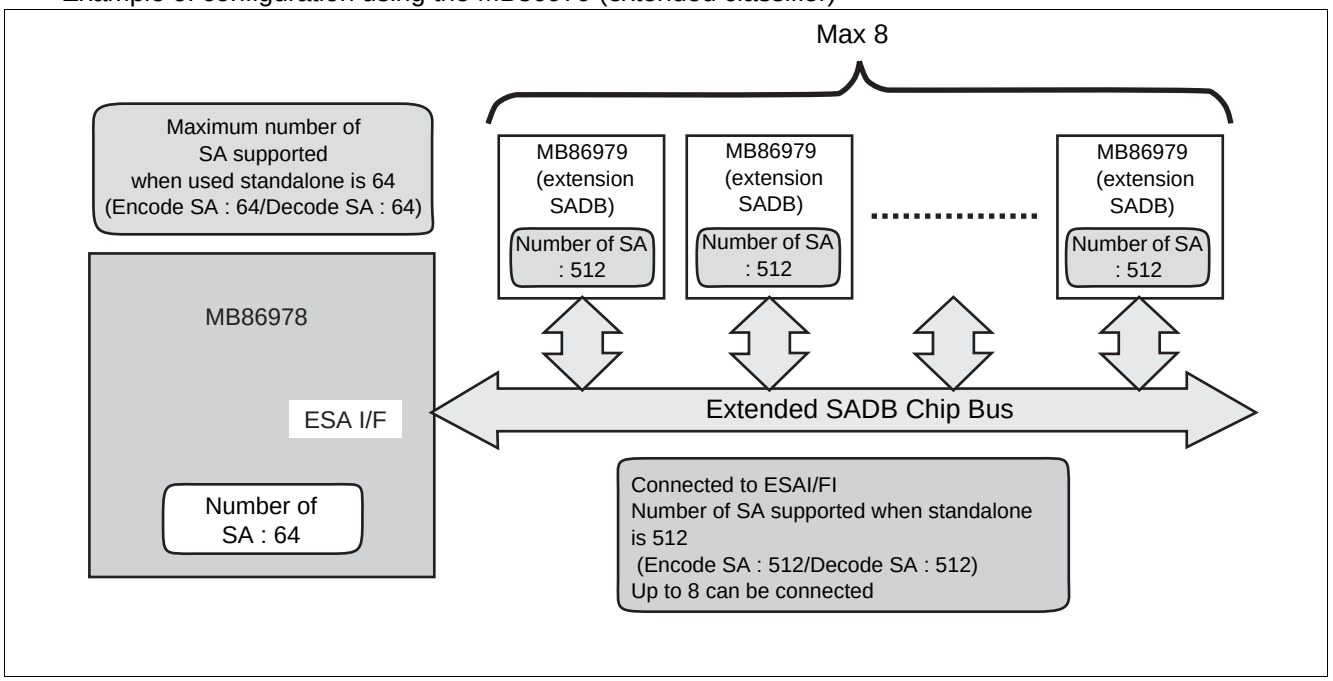
  This block reads from and writes to the PHY register via the SMI interface. The block is used to setup the PHY device as well as to retrieve status data (half/full duplex, link status, 10/100BASE-T/TX indicator, etc.) from the PHY register. The structure permits direct connection via the MII and CPU on the routing function side.

■ SYSTEM CONFIGURATION

- Example of security gateway configuration using the MB86978



- Example of configuration using the MB86979 (extended classifier)



Note : The SA database inside MB86978 cannot be used if eight MB86979s are used.

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Power supply voltage*1	V_{DDI}*2	V_{SS} – 0.5	+ 2.5	V
	V_{DDE}*3	V_{SS} – 0.5	+ 4.0	V
Input voltage*1	V_I	V_{SS} – 0.5	V_{DDE} + 0.5	V
Output voltage*1	V_O	V_{SS} – 0.5	V_{DDE} + 0.5	V
Storage temperature	Tstg	– 55	+ 125	°C
Operation junction temperature	Tj	– 40	+ 125	°C
Output current*4	I_O	– 10	+ 10	mA

*1 : This parameter is based on V_{SS} = 0 V.

*2 : 1.8 V system power supply

*3 : 3.3 V system power supply

*4 : DC current that persists for 10 ms or longer or average DC current.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power supply voltage	V_{DDI}	1.65	1.8	1.95	V
	V_{DDE}	3.0	3.3	3.6	V
“H” level input voltage	V_{IH}	2.0	—	V_{DDE} + 0.3	V
“L” level input voltage	V_{IL}	– 0.3	—	+ 0.8	V
Operating temperature	Ta	– 20	—	+ 85	°C

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device’s electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

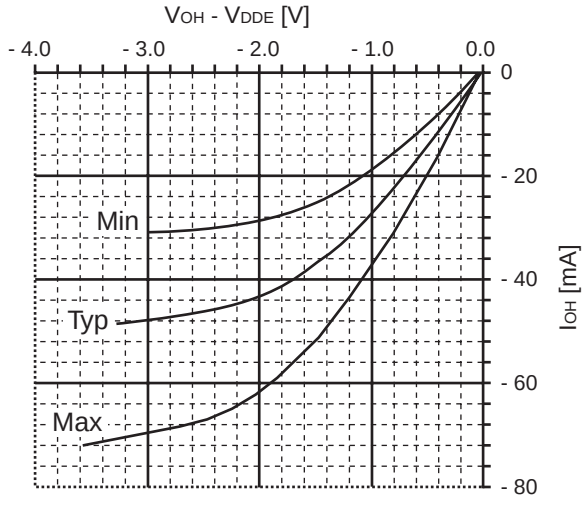
■ DC CHARACTERISTICS

(V_{DDE} = 3.3 V ± 0.3 V, V_{DDI} = 1.8 V ± 0.15 V, V_{SS} = 0 V, Ta = – 20 °C to + 85 °C)

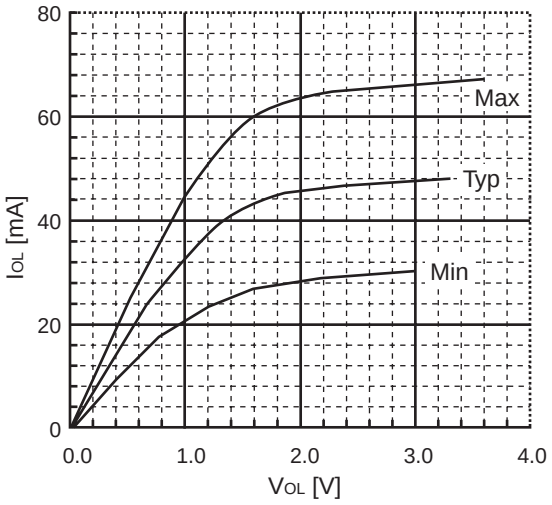
Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Power supply current	I_{DD}	State of operation	—	400	700	mA
	I_{DDS}	State of non-operation	—	—	10	mA
"H" level output voltage	V_{OH}	"H" output current I_{OH} = – 100 µA	V_{DDE} – 0.2	—	V_{DDE}	V
"L" level output voltage	V_{OL}	"L" output current I_{OL} = – 100 µA	0	—	0.2	V
"H" level output V-I characteristic	—	V_{DDE} = 3.3 V ± 0.3 V	*			—
"L" level output V-I characteristic	—	V_{DDE} = 3.3 V ± 0.3 V	*			—
Input leak current	I_L	—	– 5	—	+ 5	mA

* : Please refer to the figure below.

"H" level output V-I characteristic



"L" level output V-I characteristic



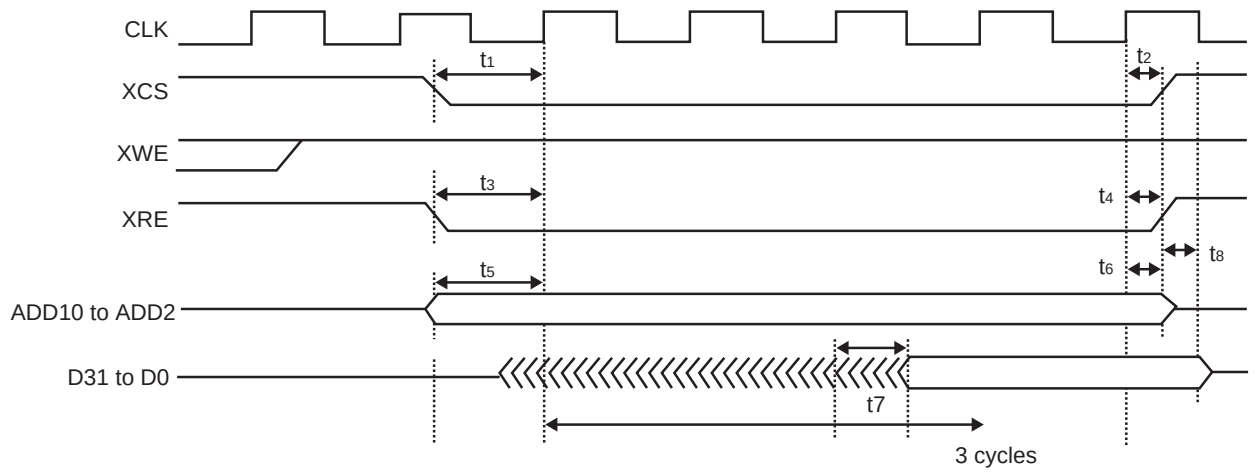
Note : Conditions : Min : Process = Slow, Tj = + 125 °C, V_{DDE} = 3.0 V
Typ : Process = Typical, Tj = + 25 °C, V_{DDE} = 3.3 V
Max : Process = Fast, Tj = – 40 °C, V_{DDE} = 3.6 V

■ AC CHARACTERISTICS

(1) Host interface data read timing

(V_{DDE} = 3.3 V ± 0.3 V, V_{DDI} = 1.8 V ± 0.15 V, V_{SS} = 0 V, Ta = – 20 °C to + 85 °C)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Chip selection input setup time	t_1	5	—	—	ns
Chip selection input holding time	t_2	5	—	—	ns
Read enable input setup time	t_3	5	—	—	ns
Read enable input hold time	t_4	5	—	—	ns
Address input setup time	t_5	5	—	—	ns
Address input holding time	t_6	5	—	—	ns
Read data output delay time	t_7	—	—	16	ns
Read data output hold time	t_8	—	—	5	ns

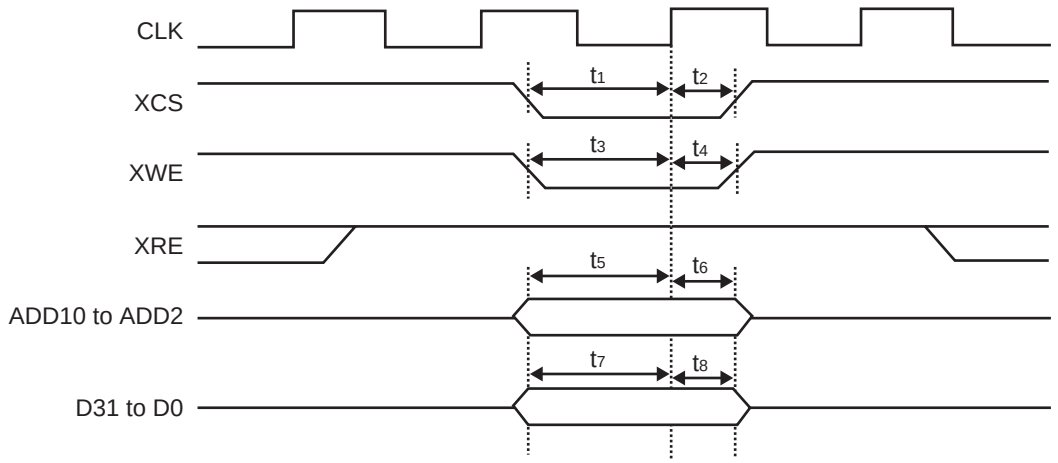


Note : When both XCS and XRE are Low, output enable.

(2) Host interface data write timing

(V_{DDE} = 3.3 V ± 0.3 V, V_{DDI} = 1.8 V ± 0.15 V, V_{SS} = 0 V, Ta = – 20 °C to + 85 °C)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Chip selection input setup time	t_1	5	—	—	ns
Chip selection input holding time	t_2	5	—	—	ns
Write enable input setup time	t_3	5	—	—	ns
Write enable input holding time	t_4	5	—	—	ns
Address input setup time	t_5	5	—	—	ns
Address input holding time	t_6	5	—	—	ns
Write data input setup time	t_7	5	—	—	ns
Write data input hold time	t_8	5	—	—	ns

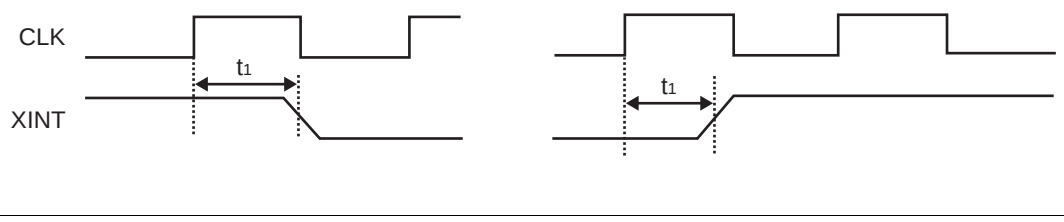


Note : D31 to D0 are decided by the rising edge of the first “CLK” which the “XWE” signal decided.

(3) Host interface and interruption timing

(V_{DDE} = 3.3 V ± 0.3 V, V_{DDI} = 1.8 V ± 0.15 V, V_{SS} = 0 V, Ta = – 20 °C to + 85 °C)

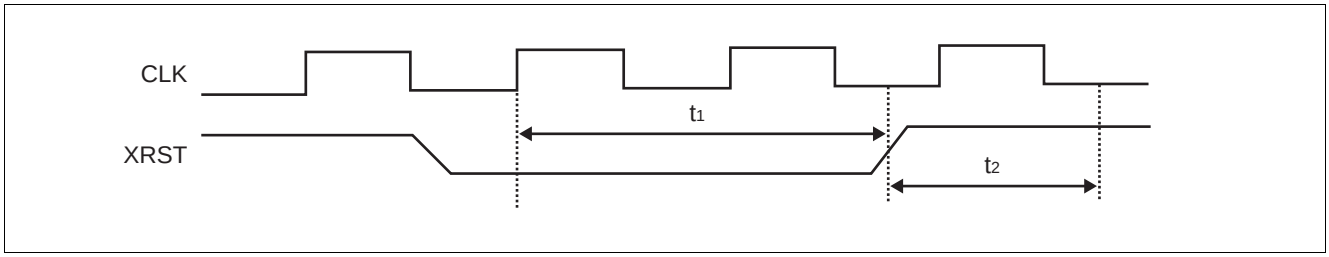
Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Interrupt signal output delay time	t_1	—	—	15	ns



(4) Reset Timings

(V_{DDE} = 3.3 V ± 0.3 V, V_{DDI} = 1.8 V ± 0.15 V, V_{SS} = 0 V, Ta = – 20 °C to + 85 °C)

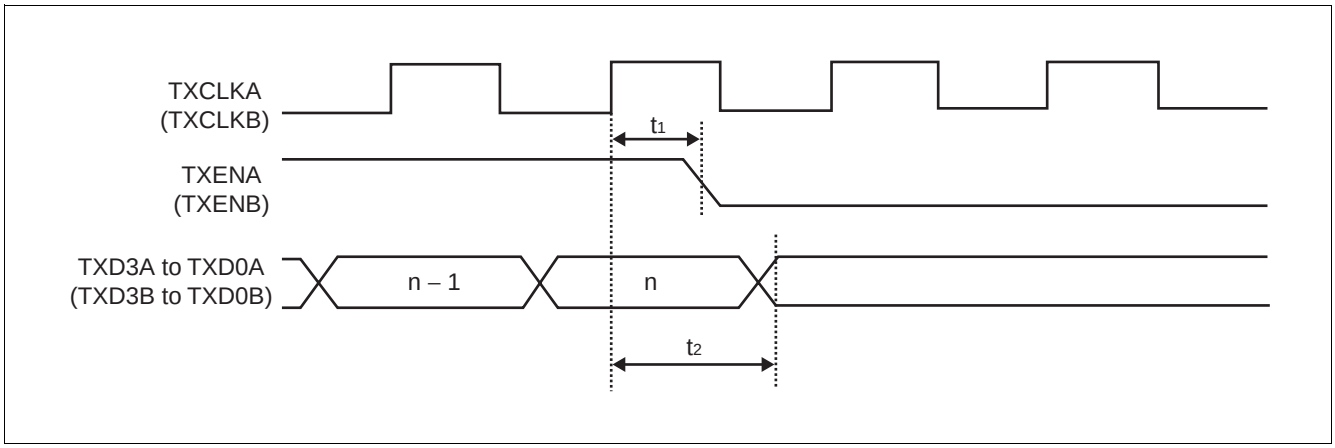
Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Reset assert time	t_1	5	—	—	clock cycle
Access barred time after reset deassertion	t_2	20000	—	—	clock cycle



(5) MII interface data transmission timing

(V_{DDE} = 3.3 V ± 0.3 V, V_{DDI} = 1.8 V ± 0.15 V, V_{SS} = 0 V, Ta = – 20 °C to + 85 °C)

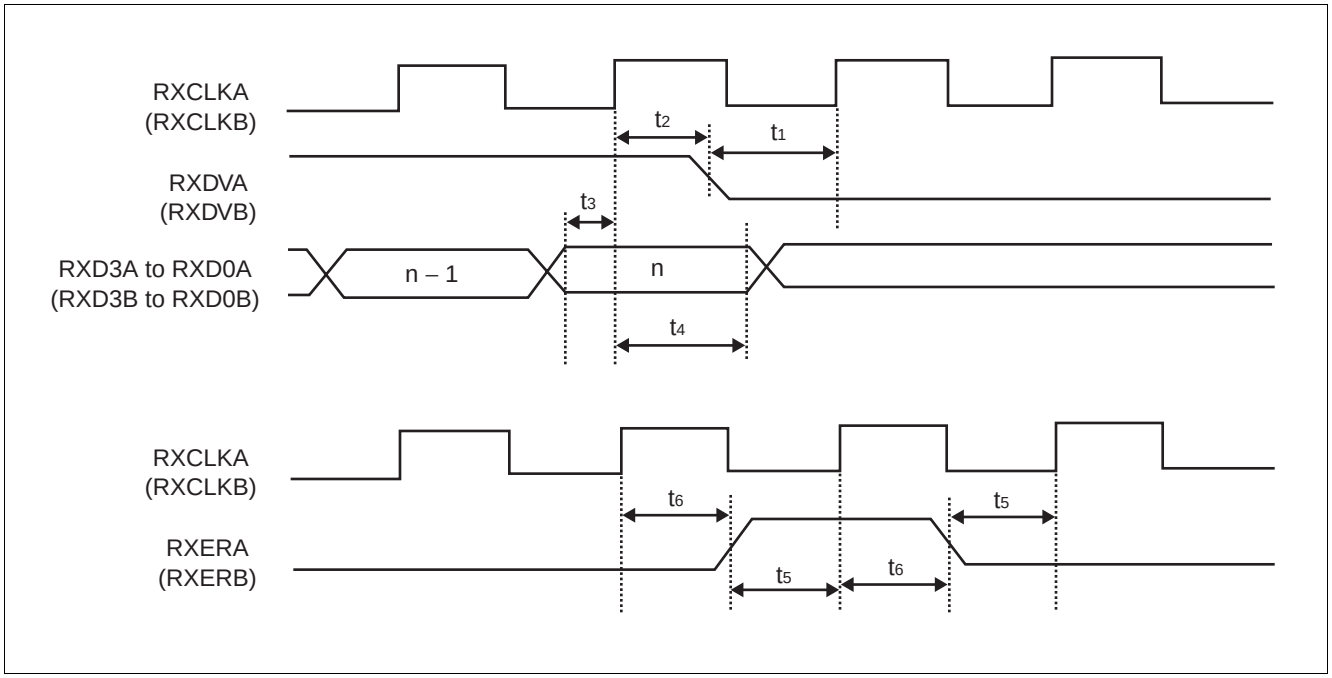
Parameter	Symbol	Value			Unit
		Min	Typ	Max	
TXENA, TXENB output delay time	t_1	—	—	20	ns
TXD3A to TXD0A, TXD3B to TXD0B output delay time	t_2	—	—	20	ns



(6) MII interface data reception timing

(V_{DDE} = 3.3 V ± 0.3 V, V_{DDI} = 1.8 V ± 0.15 V, V_{SS} = 0 V, Ta = – 20 °C to + 85 °C)

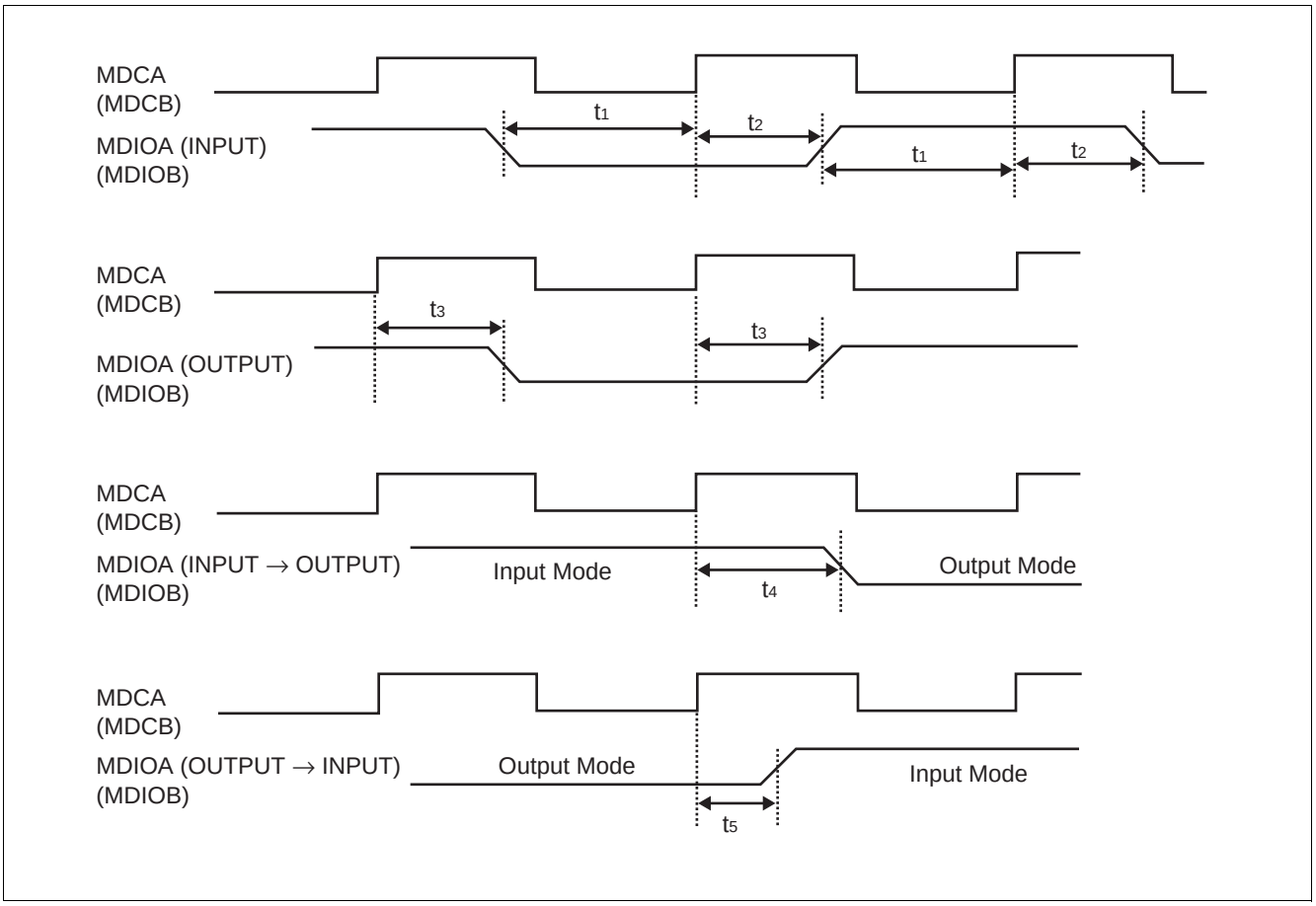
Parameter	Symbol	Value			Unit
		Min	Typ	Max	
RXDVA, RXDVB input setup time	t_1	3	—	—	ns
RXDVA, RXDVB input holding time	t_2	3	—	—	ns
RXD3A to RXD0A, RXD3B to RXD0B input setup time	t_3	3	—	—	ns
RXD3A to RXD0A, RXD3B to RXD0B input holding time	t_4	3	—	—	ns
RXERA, EXERB input setup time	t_5	3	—	—	ns
RXERA, EXERB input holding time	t_6	3	—	—	ns



(7) SMI interface

(V_{DDE} = 3.3 V ± 0.3 V, V_{DDI} = 1.8 V ± 0.15 V, V_{SS} = 0 V, Ta = – 20 °C to + 85 °C)

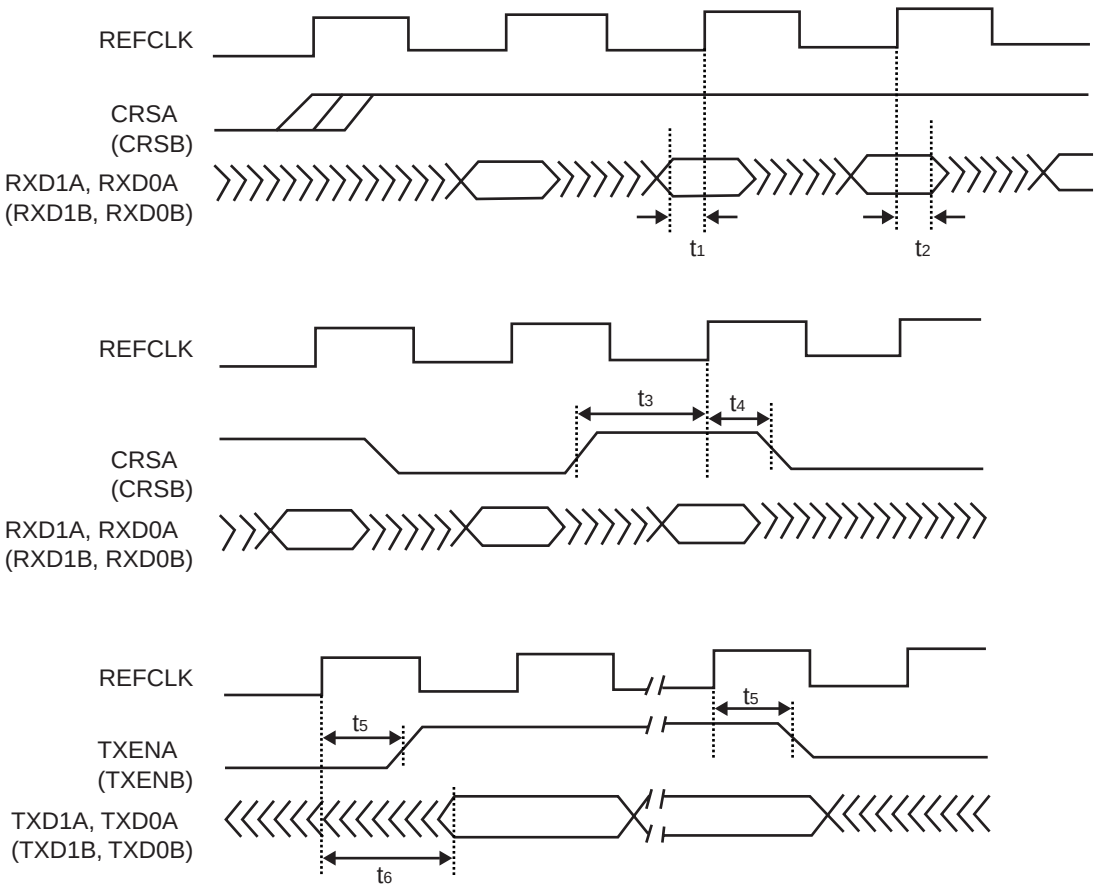
Parameter	Symbol	Value			Unit
		Min	Typ	Max	
SMI data input setup time	t_1	10	—	—	ns
SMI data input hold time	t_2	10	—	—	ns
SMI data output delay time	t_3	—	—	90	ns
SMI turning on delay time (Input mode → Output mode)	t_4	—	—	90	ns
SMI turning off delay time (Output mode → Input mode)	t_5	—	—	90	ns



(8) RMII interface

(V_{DDE} = 3.3 V ± 0.3 V, V_{DDI} = 1.8 V ± 0.15 V, V_{SS} = 0 V, Ta = – 20 °C to + 85 °C)

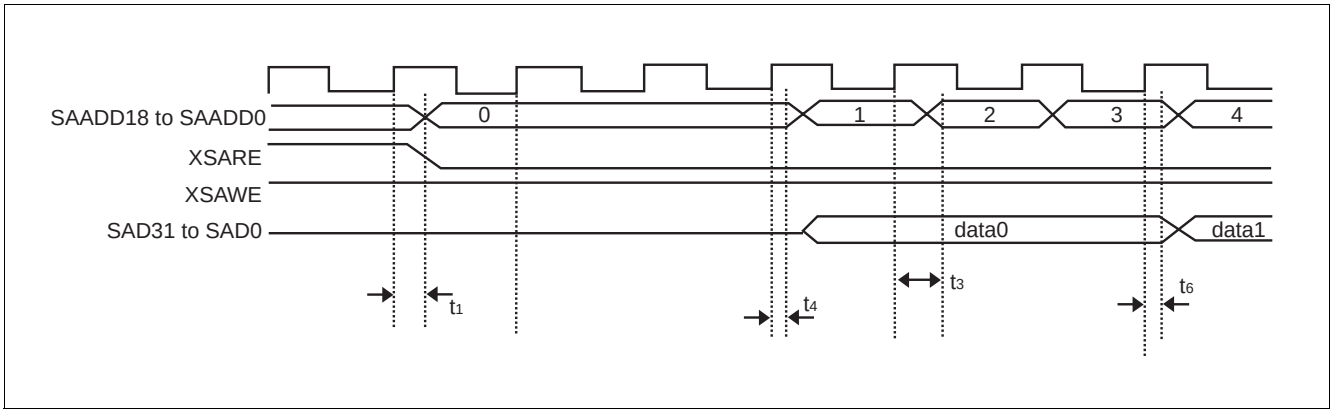
Parameter	Symbol	Value			Unit
		Min	Typ	Max	
RXD1A, RXD0A, RXD1B, RXD0B input setup time	t_1	4	—	—	ns
RXD1A, RXD0A, RXD1B, RXD0B input holding time	t_2	4	—	—	ns
CRSA, CRSB input setup time	t_3	4	—	—	ns
CRSA, CRSB input holding time	t_4	4	—	—	ns
TXENA, TXENB output delay time	t_5	—	—	15	ns
TXD1A, TXD0A, TXD1B, TXD0B output delay time	t_6	—	—	15	ns

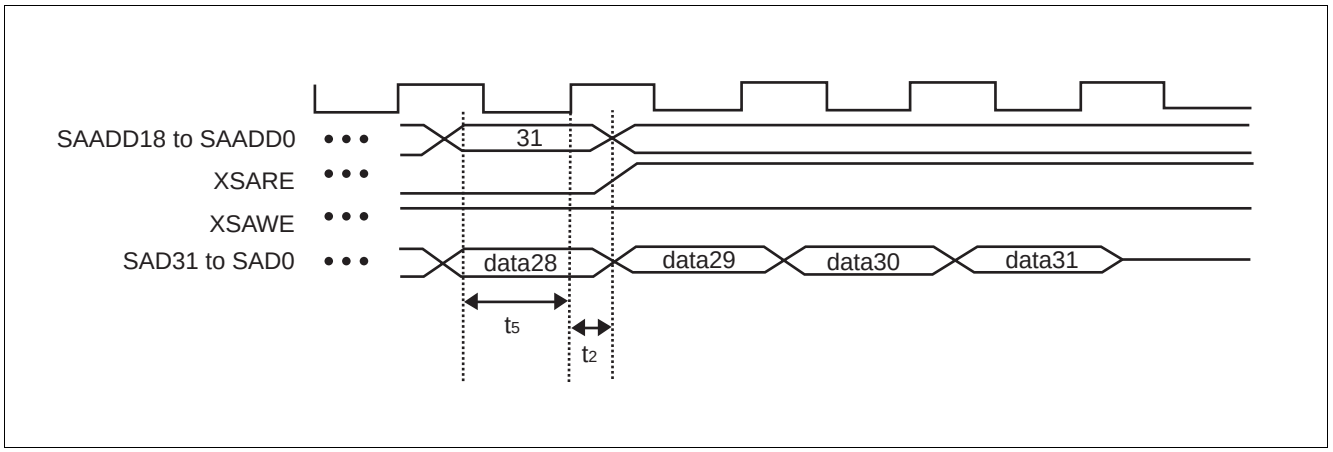


(9) Extended chip interface and SADB data read timing

(V_{DDE} = 3.3 V ± 0.3 V, V_{DDI} = 1.8 V ± 0.15 V, V_{SS} = 0 V, Ta = – 20 °C to + 85 °C)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Read enable output delay time	t_1	—	—	12	ns
Read enable output holding time	t_2	—	—	4.1	ns
Address output delay time	t_3	—	—	12	ns
Address output holding time	t_4	—	—	4.1	ns
Read data input setup time	t_5	0	—	—	ns
Read data input hold time	t_6	3.4	—	—	ns

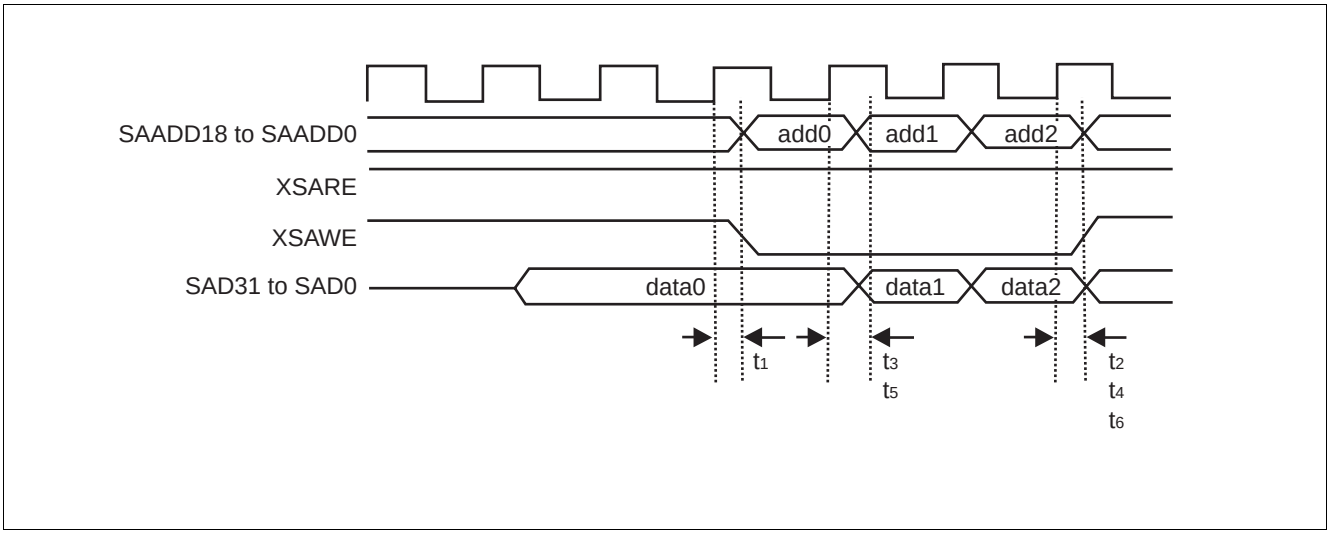




(10) Extended chip interface and SADB data write timing

(V_{DDE} = 3.3 V ± 0.3 V, V_{DDI} = 1.8 V ± 0.15 V, V_{SS} = 0 V, Ta = – 20 °C to + 85 °C)

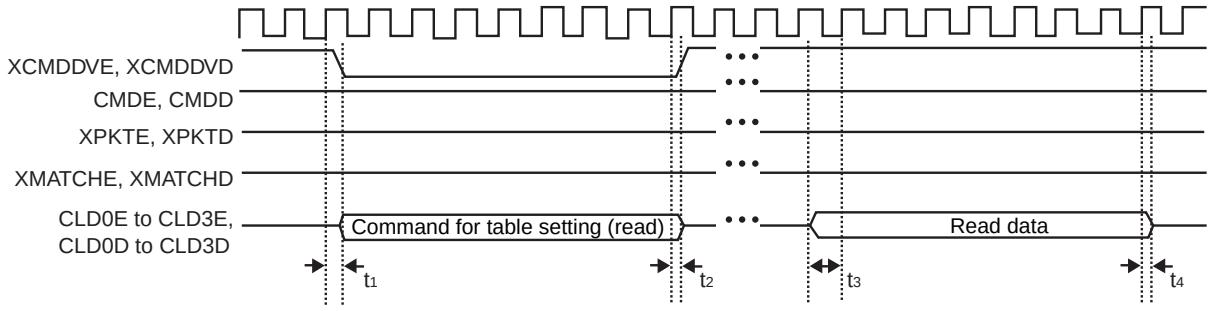
Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Write enable output delay time	t_1	12	—	—	ns
Write enable output holding time	t_2	4.1	—	—	ns
Address output delay time	t_3	12	—	—	ns
Address output holding time	t_4	4.1	—	—	ns
Write data output delay time	t_5	12	—	—	ns
Write data output holding time	t_6	4.1	—	—	ns



(11) Extended chip interface and classifier data read timing

(V_{DDE} = 3.3 V ± 0.3 V, V_{DDI} = 1.8 V ± 0.15 V, V_{SS} = 0 V, Ta = – 20 °C to + 85 °C)

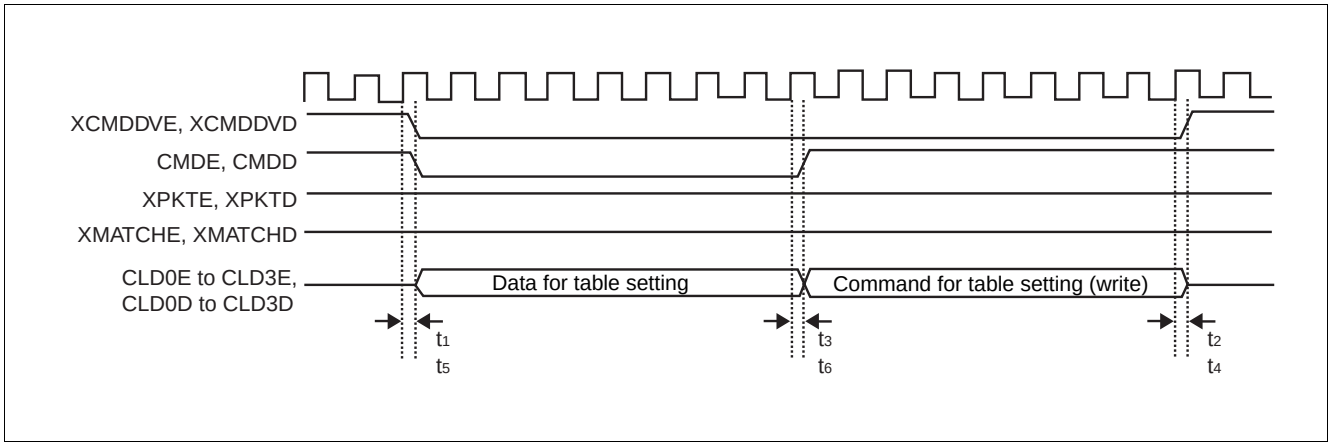
Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Command valid data output delay time	t_1	—	—	12	ns
Command valid data output holding time	t_2	—	—	4.1	ns
Classifier data input setup time	t_5	0	—	—	ns
Classifier data input holding time	t_6	4.7	—	—	ns



(12) Extended chip interface and classifier data write timing

(V_{DDE} = 3.3 V ± 0.3 V, V_{DDI} = 1.8 V ± 0.15 V, V_{SS} = 0 V, Ta = – 20 °C to + 85 °C)

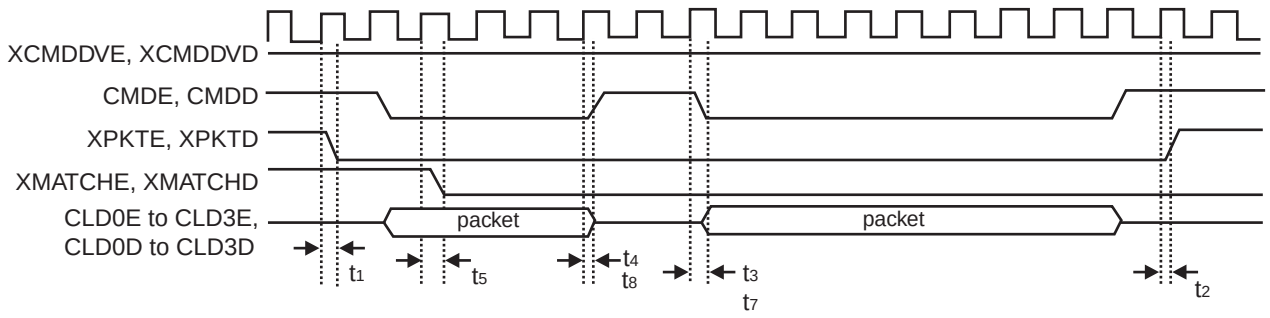
Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Command valid output delay time	t_1	—	—	12	ns
Command valid output holding time	t_2	—	—	4.1	ns
Write command output delay time	t_3	—	—	12	ns
Write command output holding time	t_4	—	—	4.1	ns
Data output delay time	t_5	—	—	12	ns
Data output holding time	t_6	—	—	4.1	ns



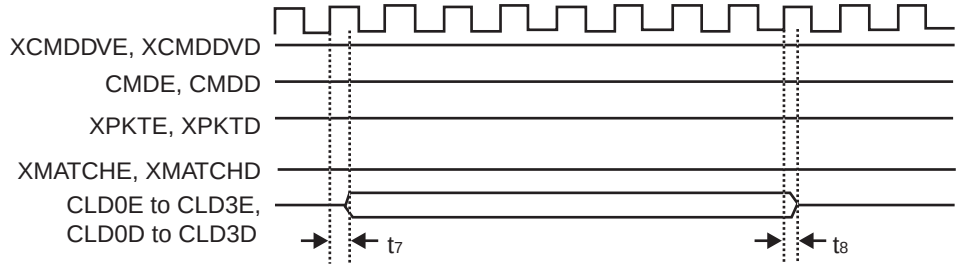
(13) Extended chip interface and classifier timing

(V_{DDE} = 3.3 V ± 0.3 V, V_{DDI} = 1.8 V ± 0.15 V, V_{SS} = 0 V, Ta = – 20 °C to + 85 °C)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Packet valid output delay time	t_1	—	—	12	ns
Packet valid output holding time	t_2	—	—	4.1	ns
Write command output delay time	t_3	—	—	12	ns
Write command output holding time	t_4	—	—	4.1	ns
Match signal input setup time	t_5	0	—	—	ns
Match signal input holding time	t_6	2.9	—	—	ns
Data output delay time	t_7	—	—	12	ns
Data output holding time	t_8	—	—	4.1	ns



Note : The match_n signal is asserted low when the packet classifier starts. De-asserted to high when matches are no longer present.



Note : The Valid signal of the result is generated in the main body chip. It doesn't exist outside of the chip.

■ NOTES ON HARDWARE SETTING

(1) Power on/off

Although no restrictions apply to the power on and off sequence, the following sequence is recommended.

- Power-ON sequence

  1) VDDI (internal)

  2) VDDE (external)

  3) Signal

- Power-OFF sequence

  1) Signal

  2) VDDE (external)

  3) VDDI (internal)

Take note of the following points relating to turning the power on and off.

- VDDE (external) should not be supplied with signals while VDDI (internal) is off; otherwise a through current may flow, causing potential reliability problems of the LSI.
- When VDDE (external) returns from the OFF state to the ON state, the circuit may fail to hold its internal state, for example, due to power supply noise.
- Initialize the device when turning the power on.

(2) Treatment of unused pin

When the only MB86978 is used (when the extended SADB LSI is not used) , the input pin for extended SADB and I/O pin should be treated as follows.

XMATCHE : pull-up
XMATCHD : pull-up
UPRIE : pull-down
UPRID : pull-down
XSAINTE : pull-up
XSAINTD : pull-up
CLD0 to CLD3E : pull-up
CLD0 to CLD3D : pull-up
SAD0 to CLD31 : pull-up

Also, following each output pin which is output from MB86978 to SADB is set to N.C.

XRSTOUT
XCMDDVE
CMDE
XPKTE
XCMDDVD
CMDD
XPKTD
XSAWE
XSARE
SAADD0 to SAADD18

(3) Connection method to execute MII direct connection in rooting function side (reference)

MB86978		Rooting function side MII I/F (opposite side)
TXENA	→	RX_DV
TXDA3 to TXDA0	⇒	RXD3 to RXD0
RXDA3 to RXDA0	⇐	TXD3 to TXD0
RXERA	←	GND
RXDVA	←	TX_EN
GND	→	RX_ER
COLA	←	GND
CRSA	←	GND
GND	→	CRS
GND	→	COL
MDCB	←	MDC
MDIOB	⇔	MDIO

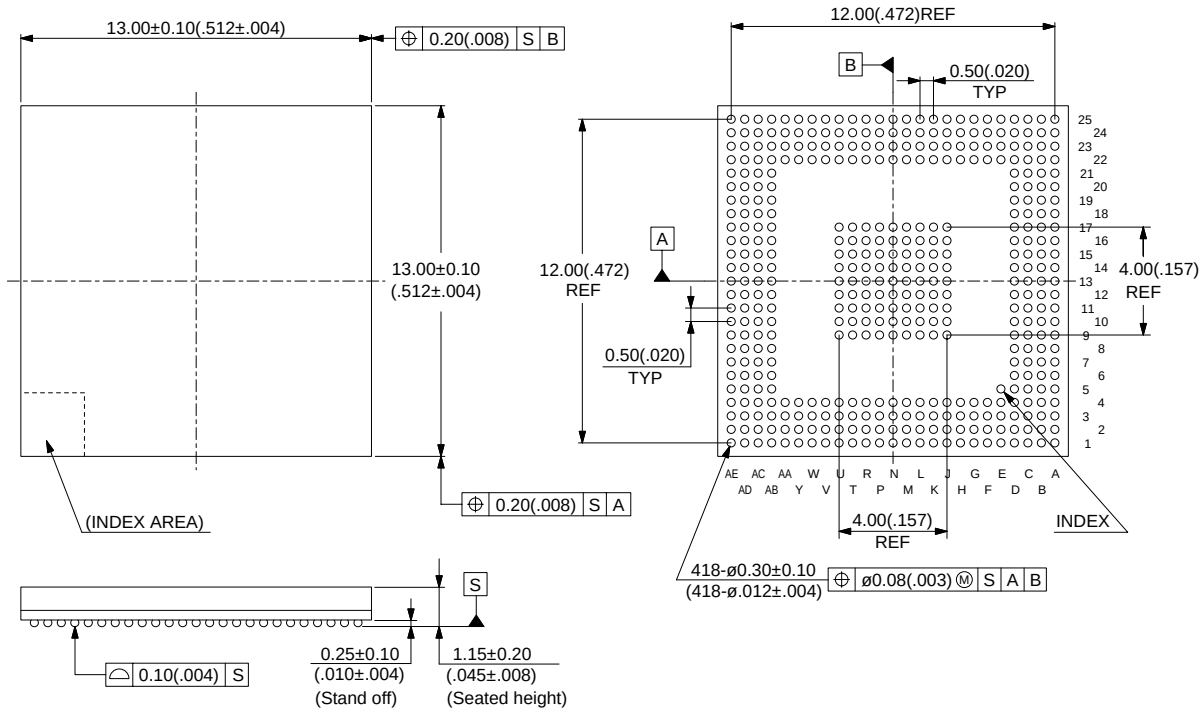
Please input the common clock (25 MHz) as corresponding RXCLK and TXCLK to RXCLKA and TXCLKA.

■ ORDERING INFORMATION

Part number	Package	Remarks
MB86978BGL-G	337-pin plastic FBGA (BGA-337P-M02)	
MB86978BGL2-G	288-pin plastic FBGA (BGA-288P-M13)	

■ PACKAGE DIMENSION

337-pin plastic FBGA
(BGA-337P-M02)

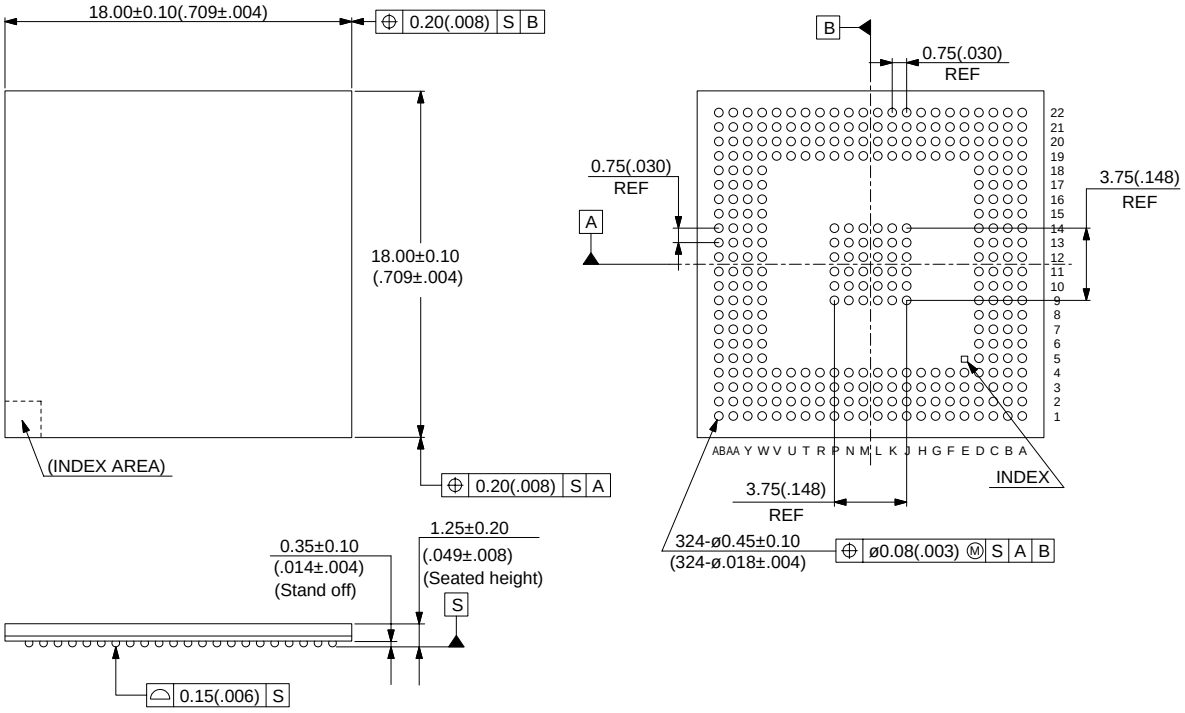


Dimensions in mm (inches) .
Note : The values in parentheses are reference values.

(Continued)

(Continued)

288-pin plastic FBGA
(BGA-288P-M13)



Dimensions in mm (inches) .
Note : The values in parentheses are reference values.

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