FUJITSU

SCSI PROTOCOL CONTROLLER

MB87030

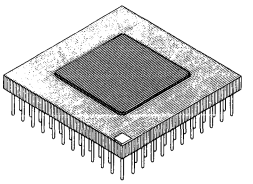
April 1986
Edition 1.0

DESCRIPTION

The MB87030 SCSI Protocol Controller (SPC) is a CMOS LSI circuit specifically designed to control a Small Computer Systems Interface (SCSI). The SPC can serve as either an Initiator or Target for the SCSI; thus, it can be used as an I/O controller or as a host adapter. To use the device in the most effective manner, it is recommended that the user be thoroughly familiar with the SCSI protocol. For detailed information in these areas, the user should request the "Users Guide for MB87030 SCSI" from the nearest Sales Office of Fujitsu.

The SPC is designed to control all SCSI interface signals and virtually all interface control procedures. Used as an 8- or 16-bit peripheral, the device provides high-level control for almost all SCSI configurations.

To achieve optimum performance and interface flexiblity, the SPC contains an 8-byte First In First Out (FIFO) data buffer register and a 24-bit transfer byte counter. Independent data busses for the CPU and the DMA controller plus separate input/output pins for all control signals greatly reduces the possiblity of a "busy" condition. Data transfers can be executed in either the synchronous or asynchronous mode with a maximum offset of 8-bytes.



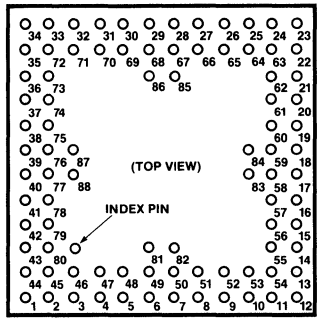
PGA-88C-A01

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

FEATURES

- Independent data transfer bus for CPU and DMA controller
- Full support for SCSI control
- Serves as either *Initiator* or *Target* device
- Synchronous mode transfer with a programmable offset of up to eight bytes
- In synchronous mode, data transfer speed programmable at four rates
- Data transfer rates of up to 4 megabytes per second
- Eight-byte data buffer register
- 24-bit transfer byte counter
- Compatible with single-ended and/or differential alternative for SCSI
- Single +5V supply
- Low power dissipation
- TTL-compatible I/O
- 88-Pin Ceramic Repeated Quad-In-Line Package

PIN ASSIGNMENTS



Pin No.	I/O	Signal Name	Pin No.	I/O	Signal Name	Pin No.	I/O	Signal Name	Pin No.	I/O	Signal Name
1	I	HIM	23	O	SDBOP	45	I	A1	67	O	SDBE5
2	I/O	HDB0	24	O	SDBE7	46	I	A2	68	O	SDBE4
3	I/O	1	25	I	SDBI7	47	I	A3	69	I	SDBI4
4	I/O	2	26	O	SDBE6	48	I/O	D4	70	O	SDBO3
5	I/O	3	27	O	SDBO5	49	I/O	D5	71	I	SDBI2
6	I/O	4	28	I	SDBI5	50	I/O	D6	72	O	SDBO1
7	I/O	5	29	O	SDBO4	51	I/O	D7	73	O	SDBE0
8	I/O	6	30	O	SDBE3	52	I/O	DP	74	I	SDBI0
9	I/O	7	31	I	SDBI3	53	O	INTR	75	I	$\overline{RST}$
10	I/O	P	32	O	SDBO2	54	I	I/OI	76	O	DREQ
11	O	INIT	33	O	SDBE2	55	I	C/DI	77	I	$\overline{WT}$
12	O	TARG	34	I	SDBI1	56	I	SELI	78	I	$\overline{WTG}$
13	O	I/OO	35	O	SDBE1	57	I	MSG1	79	I/O	D2
14	O	C/DO	36	O	SDBOO	58	I	REQI	80	I/O	D3
15	O	SELO	37	I	$\overline{CS}$	59	I	RSTI	81	Power Supply	VSS
16	O	MSGO	38	I	$\overline{CLK}$	60	I	ACKI	82	Power Supply	VDD
17	O	REQO	39	I	$\overline{RD}$	61	I	BSYI	83	Power Supply	VDD
18	O	RSTO	40	I	$\overline{RGD}$	62	I	ANTI	84	Power Supply	VSS
19	O	ACKO	41	I	DRESP	63	I	SDBIP	85	Power Supply	VSS
20	O	BSYO	42	I/O	D0	64	O	SDBO7	86	Power Supply	VDD
21	O	ATNO	43	I/O	D1	65	O	SDBO6	87	Power Supply	VDD
22	O	SDBEP	44	I	A0	66	I	SDBI6	88	Power Supply	VSS

PIN DESCRIPTIONS

Pin Number	Designator	Function
82, 83, 86, 87	V_{DD}	+5V power supply
81, 84, 85, 88	V_{SS}	Ground (0V)
38	$\overline{CLK}$	Input clock for controlling SPC internal operation and data transfer speed.
75	$\overline{RST}$	Asynchronous reset signal for clearing internal circuits of SPC.
37	$\overline{CS}$	Selection enable signal for accessing an internal register in SPC. When $\overline{CS}$ is active, the following input/output signals are valid: $\overline{RD}$, $\overline{RDG}$, $\overline{WT}$, $\overline{WTG}$, DP, A3–A0, and D7–D0.
47 46 45 44	A3 A2 A1 A0	Address input signals for selecting an internal register in SPC. MSB: A3, LSB: A0 When $\overline{CS}$ is active low, read/write is enabled and an internal register is selected by these address inputs via data bus lines D7–D0 and DP.
39 40	$\overline{RD}$ $\overline{RDG}$	Input strobes used for reading out the contents of the SPC internal register and are effective only when $\overline{CS}$ is active low. When $\overline{RDG}$ is active, the contents of an internal register selected by address inputs A3–A0 are placed on data bus lines D7–D0 and DP. For a data transfer cycle in the program transfer mode, the trailing edge of $\overline{RD}$ is used as a timing signal to indicate the end of data read.
77	$\overline{WT}$	Input strobe used for writing data into an SPC internal register and is only effective when $\overline{CS}$ is active low. On the trailing edge of $\overline{WT}$, data placed on data bus lines D7–D0 and DP are loaded into an internal register selected by address inputs A3 to A0, except when all address lines are high (A3–A0 = H). For a data transfer cycle in the program transfer mode, the trailing edge of $\overline{WT}$ is used as a timing signal to indiacte a data-ready state.
78	$\overline{WTG}$	When $\overline{WTG}$ is active low, data appearing on data bus lines D7–D0 and DP is output to HDB7–HDB0 and HDBP if the following input conditions are satisfied: $\overline{CS}$ = 'L' A3 = A2 = A1 = A0 = 'H' HIN = 'H'
51 50 49 48 80 79 43 42 52	D7 D6 D5 D4 D3 D2 D1 D0 DP	Used for writing-or-reading data into-or-from an internal register in SPC. This data bus is three-state and bidirectional. MSB: D7 LSB: D0 Odd Parity Bit: DP When the $\overline{CS}$ and $\overline{RDG}$ inputs are active, the contents of the internal register are output to the data bus (read operation). In operations other than read, this data bus is kept at a high impedance level.

PIN DESCRIPTIONS (Cont'd)

<table>
<tr><th>Pin Number</th><th>Designator</th><th>Function</th></tr>
<tr><td>53</td><td>INTR</td><td>Requests an interrupt to indicate completion of an SPC internal operation or the occurrence of an error.
Interrupt masking is allowed except for an interrupt caused by the RSTI input (reset condition is SCSI).
When an interrupt request is permitted, the INTR signal remains active until the cause of the interrupt is cleared.</td></tr>
<tr><td>25
66
28
69
31
71
34
74
63</td><td>SDBI7
SDBI6
SDBI5
SDBI4
SDBI3
SDBI2
SDBI1
SDBI0
SDBIP</td><td>Used as input for the SCSI data bus.
MSB: SDBI7
LSB: SDBI0
Odd parity bit: SDBIP
Parity checking for the SCSI data bus is programmable.</td></tr>
<tr><td>64
65
27
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70
32
72
36
23</td><td>SDBO7
SDBO6
SDBO5
SDBO4
SDBO3
SDBO2
SDBO1
SDBO0
SDBOP</td><td>Used as outputs to the SCSI data bus.
MSB: SDBO7
LSB: SDBO0
Odd parity bit: SDBOP
If the bus driver is an open collector device, these signals should be applied directly to the driver circuit.
If the bus driver is a three-state device, these signals are used as data and the SDBE7–SDBE0 and SDBEP signals are used as drive-enable signals.</td></tr>
<tr><td>24
26
67
68
30
33
35
73
22</td><td>SDBE7
SDBE6
SDBE5
SDBE4
SDBE3
SDBE2
SDBE1
SDBE0
SDBEP</td><td>Used as drive enable signals (corresponding to respective bit positions) when a three state-buffer is used for the SCSI data bus.
SDBE7–SDBE0 and SDBEP correspond to SDBO7–SDBO0 and SDBOP, respectively. The relationship with respect to the SCSI bus status is shown below.
<table>
<tr><th colspan="2" rowspan="2">SCSI bus status</th><th colspan="2">SDBOn</th><th colspan="2">SDBEn</th></tr>
<tr><th>(ID)</th><th>($\overline{ID}$)</th><th>(ID)</th><th>($\overline{ID}$)</th></tr>
<tr><td colspan="2">Bus Free</td><td>'L'</td><td>'L'</td><td>'L'</td><td>'L'</td></tr>
<tr><td colspan="2">Arbitration</td><td>'H'</td><td>'L'</td><td>'H'</td><td>'L'</td></tr>
<tr><td colspan="2">Selection/Reselection</td><td>D</td><td>D</td><td>'H'</td><td>'H'</td></tr>
<tr><td rowspan="2">Information Transfer</td><td>SPC → SCSI</td><td>D</td><td>D</td><td>'H'</td><td>'H'</td></tr>
<tr><td>SPC ← SCSI</td><td>'L'</td><td>'L'</td><td>'L'</td><td>'L'</td></tr>
</table>
• (ID) indicates a bit positions corresponding to the SCSI bus device ID, and ($\overline{ID}$) indicates the other bit position.
• D denotes that valid information is sent out.</td></tr>
</table>

PIN DESCRIPTIONS (Cont'd)

<table>
<tr><th>Pin Number</th><th>Designator</th><th>Function</th></tr>
<tr><td>56
61
58
60
57
55
54
62
59</td><td>SELI
BSYI
REQI
ACKI
MSGI
C/DI
I/OI
ATNI
RSTI</td><td>Used for receiving SCSI control signals. The outputs of the SCSI receiver can be directly connected.
Note: Waveform distortion or any other disturbance should not occur in the REQI and ACKI signals which are used as timing control signals for sequencing data transfer.</td></tr>
<tr><td>15
20
17
19
16
14
13
21
18</td><td>SELO
BSYO
REQO
ACKO
MSGO
C/DO
I/OO
ATNO
RSTO</td><td>Used to output SCSI control signals. The following signals become active only when SPC serves as a target; otherwise, these signals are always low: REQO, MSGO, C/DO and I/OO.
The following signals become active only when SPC serves as an initiator; otherwise, these signals are always low: ACKO and ATNO.</td></tr>
<tr><td>11
12</td><td>INIT
TARG</td><td>Used to indicate operating state of SPC. These signals are also available as control signals for the SCSI driver/receiver circuits.
<table>
<tr><th>Initiator</th><th>Target</th><th>Status</th></tr>
<tr><td>'L'</td><td>'L'</td><td>SPC is not connected to SCSI.</td></tr>
<tr><td>'L'</td><td>'H'</td><td>SPC is executing reselection phase or is operating as a target.</td></tr>
<tr><td>'H'</td><td>'L'</td><td>SPC is executing selection phase or is operating as an initiator.</td></tr>
</table></td></tr>
<tr><td>76</td><td>DREQ</td><td>When executing a data transfer cycle in DMA mode, the DREQ signal is used to indicate a request for data transfer between SPC and the external buffer memory.
In DMA mode, data is routed as shown below:
Output operation
External buffer memory
↓
HDB7 to HDB0, and HDBP pins
↓
SPC internal data buffer register (8 bytes)
↓
SDBO7 to SDBO0 and SDBOP pins
↓
(SCSI)</td></tr>
</table>

PIN DESCRIPTIONS (Cont'd)

Pin Number	Designator	Function
76	DREQ (cont'd)	**Input operation** (SCSI) ↓ SDBI7 to SDBI0 and SDBIP pins ↓ SPC internal data buffer register (8 bytes) ↓ HDB7 to HDB0, and HDBP pins ↓ External buffer memory In an output operation, DREQ becomes active to request a data transfer from the external buffer memory when the SPC internal data buffer register has free space available. In an input operation, it becomes active to request a data transfer to the external buffer memory when the SPC internal buffer memory contains valid data.
41	DRESP	Used as a response signal to the above data transfer request signal (DREQ) in DMA mode during a data transfer cycle. Pin DRESP must be refreshed with an applied pulse after each byte transferred. In an output operation, SPC uses the trailing edge of the DRESP signal for sampling data on the HDB7–HDB0 and HDBP bus lines. In an input operation, SPC holds data to be transferred onto HDB7–HDB0 and HDBP bus lines until the trailing edge of the DRESP signal.
9 8 7 6 5 4 3 2 10	HDB7 HDB6 HDB5 HDB4 HDB3 HDB2 HDB1 HDB0 HDBP	Three-state, bidirectional data bus for transferring data to-or-from the external buffer memory in DMA mode. MSB: HDB7 LSB: HDB0 Odd parity bit: HDBP The data transmission direction depends on the HIN input signal. **HIN** **HDBn** **Operation** 'L' Input mode Output 'H' Output mode Input
1	HIN	This signal indicates transmission direction along data bus lines HDB7–HDB0 and HDBP in DMA transfer mode. To be executed, transmission direction must be properly coordinated with internal operation of the SPC. When the HIN signal is Low, data bus lines HDB7–HDB0 and HDBP are put in the high impedance state (input mode). When the HIN signal is High, they are switched to the output mode.

ABSOLUTE MAXIMUM RATINGS[1]

Rating	Symbol	Values		Unit
		Min	Max	
Supply Voltage	V_{DD}	V_{SS}[2] - 0.5	7.0	V
Input Voltage	V_I	V_{SS}[2] - 0.5	V_{DD} + 0.5	V
Output Voltage	V_O	V_{SS}[2] - 0.5	V_{DD} + 0.5	V
Storage Temperature (Ceramic)	T_{stg}	-65	+150	°C
Temperature Under Bias (Ceramic)	T_{bias}	-40	+125	°C
Output Current[3]	I_{OS}	-40	+70	mA

Notes:
1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of the SCSI User's Guide. Absolute maximum rating conditions for extended periods may affect device reliability.
2. V_{SS} = 0V.
3. Not more than one output may be shorted at a time for a maximum duration of one second.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Values			Unit
		Min	Typ	Max	
Supply Voltage	V_{DD}	4.75	5.0	5.25	V
Input High Voltage	V_{IH}	2.2			V
Input Low Voltage	V_{IL}			0.8	V
Operating Temperature	T_A	0		70	°C

DC CHARACTERISTICS (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Condition	Values			Unit
			Min	Typ	Max	
Power Supply Current	I_{DDS}	Steady state[1]			100	μA
Power Dissipation	PD			300		mW
Output High Voltage	V_{OH}	I_{OH} = -0.4mA	4.2		V_{DD}	V
Output Low Voltage	V_{OL}	I_{OL} = 3.2mA	V_{SS}		0.4	V
Input High Voltage	V_{IH}		2.2			V
Input Low Voltage	V_{IL}				0.8	V
Input Leakage Current	I_{LI}	V_I = 0 - V_{DD}	-10		10	μA
Input Leakage Current	I_{LZ}	3-state V_I = 0 - V_{DD}	-10		10	μA

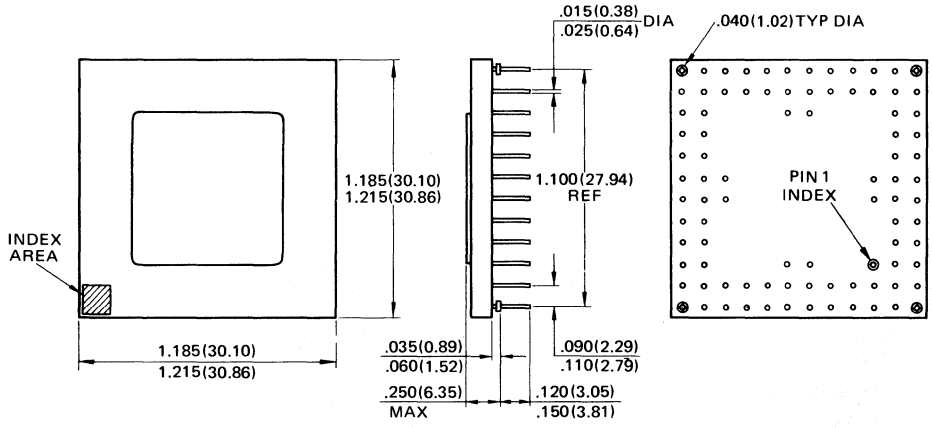
Note:
1. V_{IH} = V_{DD}, V_{IL} = V_{SS}

CAPACITANCE (T_A = 25°C, V_{DD} = V_I = 0V, f = 1 MHz)

Parameter	Symbol	Values			Unit
		Min	Typ	Max	
Input Pin Capacitance	C_{IN}			9	pF
Output Pin Capacitance	C_{OUT}			9	pF
I/O Pin Capacitance	$C_{I/O}$			11	pF

PACKAGE DIMENSIONS

88-Lead Ceramic (Metal Seal)
Repeated Quad In-Line Package
PGA-88C-A01



Dimensions in
inches (millimeters)

4