FUJITSU

Digital Signal Processor

MB87064

April 1986
Edition 1.0

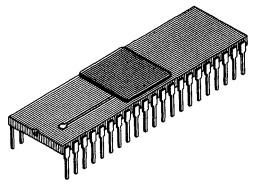
PRELIMINARY

DESCRIPTION

The Fujitsu MB87064 is a general-purpose LSI silicon gate Digital Signal Processor (DSP). The device is fabricated in low-power CMOS and features a high-speed pipelined multiplier, supports concurrent operations with compound instructions and multiple data paths, and offers flexible and expandable memory options. The MB87064 is housed in a 42-pin DIP.

Except for some changes in the instruction set and minor modifications in the hardware, the low-cost MB87064 DSP is a functional clone for Fujitsu's full-featured MB8764 DSP. The low-cost MB87064 is particularly useful in systems where the additional features of the MB8764 are simply not required. Since basic functions of the two parts are identical, this data sheet describes only those differences that affect system design. For complete functional detail pertaining to hardware and software, it is recommended that the user obtain data sheets for both parts (MB87064 and MB8764). If further information regarding Digital Signal Processing is desired, the user should request "Support Documentation for the MB8764" from the nearest Fujitsu sales office.

Both the MB87064 and the MB8764 are well suited for applications such as telecommunications, imaging work, and other signal-processing functions that require extensive computations and complex analysis.



DIP-42C-A01

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

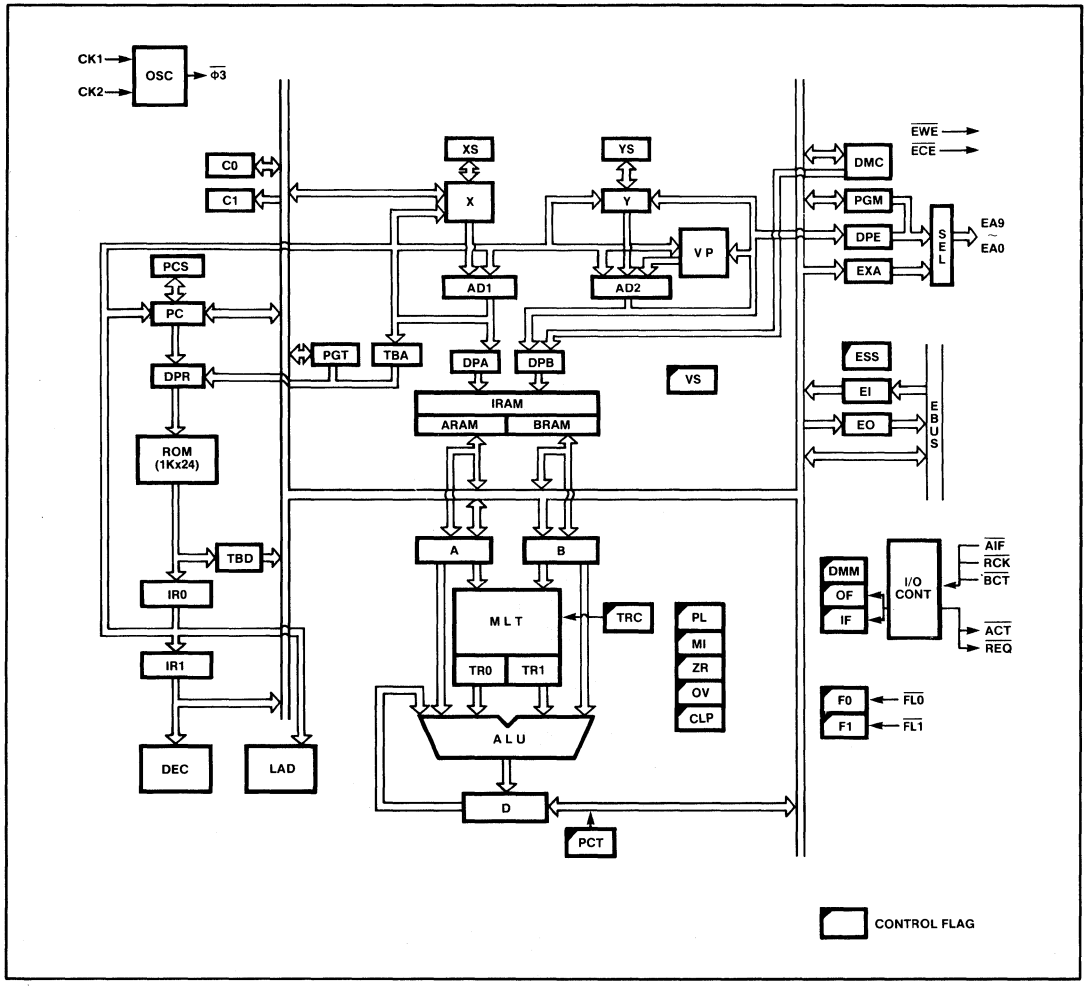
6

Table 1. Comparison of Features (MB87064 and MB8764)

Item	MB8764	MB87064
Hardware Architecture	Common Hardware Architecture • Parallel pipelined multiply function 16 bits x 16 bits → 26 bits • Divide function 26 bits ÷ 16 bits → 16 bits	
Instruction Set	MB8764 Instruction Set	Basically the same as the MB8764 but with few modifications
Operation Cycle Time	100ns	
Package	PGA88 Ceramic[1] LCC84 Ceramic	DIP42 Ceramic[1]
Program ROM	Internal (mask-programmable) ROM of 1024 words × 24 bits	
	External ROM of 1024 words × 24 bits selectable	No External ROM function
Data RAM	Built-in 2 blocks of 128 words × 16 bits Expansion RAM up to 1024 words × 16 bits	
I/O Functions	16-bit Parallel Interface	
	Three Input Modes Two Output Modes	Two Input Modes One Output Mode (Brand-new)
Addressing	Same Addressing Functions • Direct Addressing • Immediate Addressing • Indexed Addressing • Virtual Shift Addressing	
Support Tools	Common Support Tools • Evaluation Board • Softwares (Assemblers, Linkers, Software Simulators, Monitor) • In-Circuit Emulation Board[2]	
Applications	• Flexible system with external program memory • Small Volume Production with Internal/External ROM • System evaluation before Production	• High Volume Production with Mask ROM

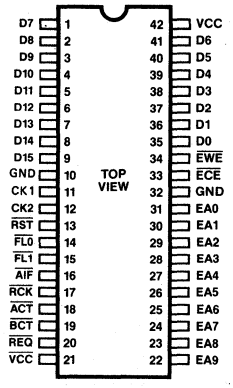
Notes:
1. Plastic package is scheduled for the future.
2. Soon to be available.

BLOCK DIAGRAM



6

PIN DESCRIPTIONS



Pin No.	Designator	Function	Pin No.	Designator	Function
		Input/Output Pins:			**Output Pins:**
09	D15	Data bus Bit 15 (MSB)	22	EA9	Expansion RAM Address MSB
08	D14	Data bus Bit 14	23	EA8	Expansion RAM Address Bit 8
07	D13	Data bus Bit 13	24	EA7	Expansion RAM Address Bit 7
06	D12	Data bus Bit 12	25	EA6	Expansion RAM Address Bit 6
05	D11	Data bus Bit 11	26	EA5	Expansion RAM Address Bit 5
04	D10	Data bus Bit 10	27	EA4	Expansion RAM Address Bit 4
03	D9	Data bus Bit 9	28	EA3	Expansion RAM Address Bit 3
02	D8	Data bus Bit 8	29	EA2	Expansion RAM Address Bit 2
01	D7	Data bus Bit 7	30	EA1	Expansion RAM Address Bit 1
41	D6	Data bus Bit 6	31	EA0	Expansion RAM address LSB
40	D5	Data bus Bit 5	34	$\overline{EWE}$	ERAM Write Clock Output
39	D4	Data bus Bit 4	33	$\overline{ECE}$	ERAM Chip Enable Output
38	D3	Data bus Bit 3	11	CK1	Master Clock Input Pin 1
37	D2	Data bus Bit 2	12	CK2	Master Clock Input Pin 2
36	D1	Data bus Bit 1	13	$\overline{RST}$	Initialization Input
35	D0	Data bus Bit 0 (LSB)	16	$\overline{AIF}$	Data Input Request
10	GND	Circuit Ground	17	$\overline{RCK}$	Data Read Clock Input
32	GND	Circuit Ground	18	$\overline{ACT}$	Data Input Enable Output
42	V_{CC}	+5V Power Supply	20	$\overline{REQ}$	Data Bus Request Output
21	V_{CC}	+5B Power Supply	19	$\overline{BCT}$	Data Bus Output Enable Input
			14	$\overline{FL0}$	Flag Input
			15	$\overline{FL1}$	Flag Input

PIN MODIFICATIONS

Based on the pin configuration of the MB8764, the following modifications have been made for the MB87064.

Removal of pins caused by no external ROM:

PA9 ~ PA0 (10 pins)
IRM (1 pin)
P23 ~ P0 (24 pins)
TST (1 pin)

Removal of pins caused by reduction/modification of input/output mode:

$\overline{ASL}$ (1 pin)
$\overline{AOF}$ (1 pin)
$\overline{WCK}$ (1 pin)

Removal of pins caused by modification of external RAM speed control (hardware → software):

$\overline{ESS}$ (1 pin)

Removal of unneeded power/ground pins:

GND (2 pins)
V_{CC} (2 pins)

FUNCTIONAL DESCRIPTION

Program Memory

The program for the MB87064 is provided from the internal (mask-programmed) ROM with a capacity of 1024 words × 24 bits. The MB87064 cannot access external ROM.

Input/Output Modes

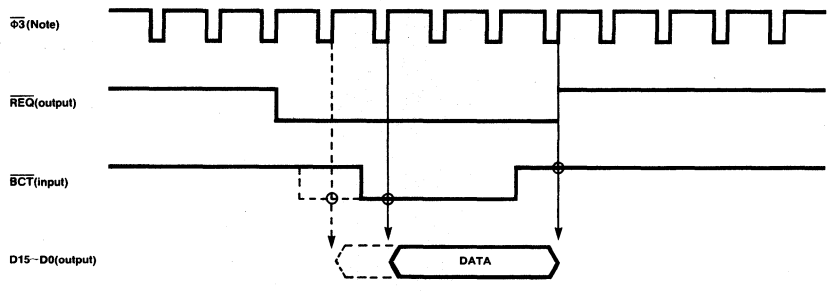
Input Modes

Two operating modes (D and P) are used to input data from an external device to the MB87064. The function and timing specification for the two input modes are the same as those in the MB8764. The selected input mode is loaded into the mode (DMM) register by the program.

Output Mode

Only one output mode is provided to transfer data from the MB87064 to an external peripheral. The output mode in the MB87064 is a modified version of the E mode in the MB8764. Output mode timing is shown in the following diagram.

Output Mode Timing



Note:
Φ3 is the cycle clock that controls internal operations of the DSP.

Registers/Flags

Register Omission

Input address register EIA, output address register EA, unit register U, and address mode register ADM are not required in the MB87064.

New Registers and Flags

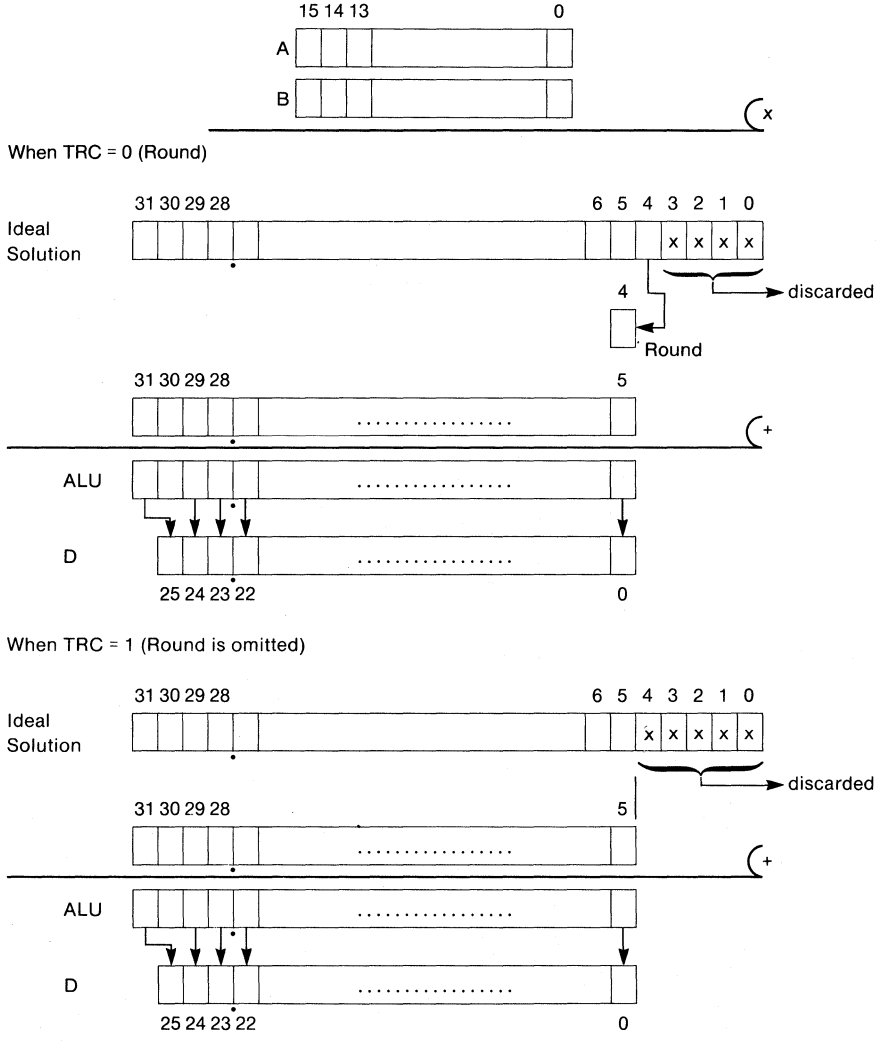
ESS Flag. Because the ESS pin has been removed, the MB87064 controls ERAM access speed by the ESS flag which, in turn, is controlled by the SET/CLR instructions. The low-speed mode (ESS = 1) is specified by the "SET ESS" instruction. It is cleared by the "CLR ESS" instruction and the high-speed mode (ESS = 0) is then specified. When the device is reset, the high-speed mode is selected by default.

Because the ESS pin has been removed, the MB87064 controls ERAM access speed through the ESS flag. A two cycle access is selected by setting the ESS flag (ESS = 1). and the single cycle access is selected by clearing the ESS flag (ESS = 0).

ESS is cleared upon reset (ESS = 0).

TRC Register. The TRC register is a 1-bit register used to control the truncation of the multiplication result. The TRC Register is controlled by the SET/CLR instructions.

When TRC is set to "1", the multiplication result is truncated to 26-bits without rounding. When TRC is set to "0", the result is rounded to 26-bits. (Same as the MB8764.)



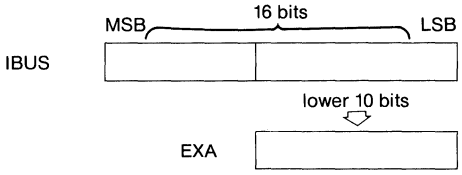
PCT Register. In the MB8764, even when operating in the CLIP mode with the overflow flag set, if two maximum negative numbers are multiplied together [(8000H) × (8000H)], the resulting output from the D register to IBUS is (0000H). Also, if positive or negative overflows occur, the resulting output may not be the maximum positive or negative values [(8000H) or (7FFFH)]. The MB87064 selects the PCT (protect mode) to avoid this overflow problem. The protect mode is controlled by the "PCT" flag. The "PCT" flag is set by the "SET PCT" instruction and cleared by the "CLR PCT" instruction.

The "PCT" flag is also cleared by a reset input. As with the MB8764, the normal mode is selected when the "PCT" flag is cleared.

EXA Register. The MB8764 outputs the contents of page register PGM and data pointer register DPE to the EA9 ~ EA0 pins regardless of ERAM access.

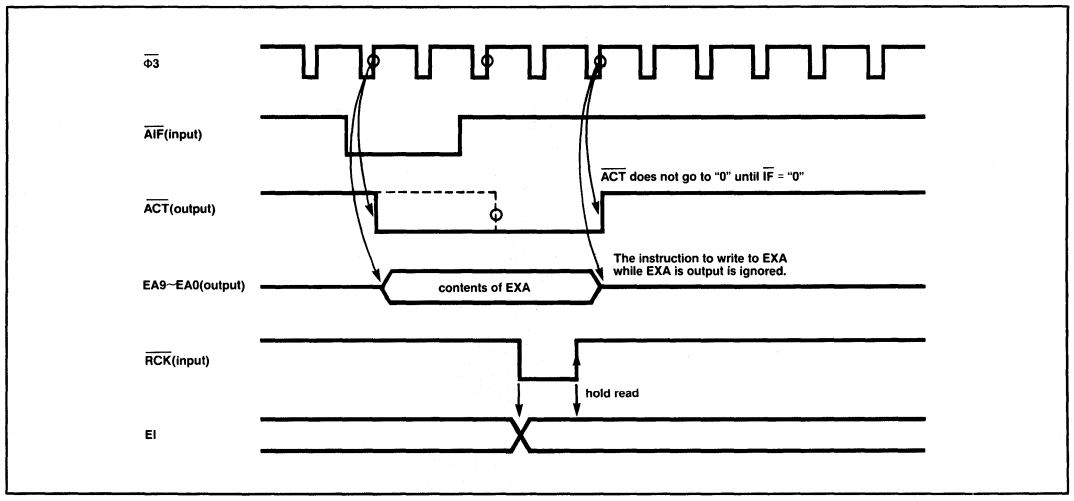
The MB87064 outputs the contents of PGM and DPE when ERAM is being accessed and outputs the contents of EXA when the I/O bus is being accessed for data transfer to-or-from an external circuit.

- The contents of EXA Register

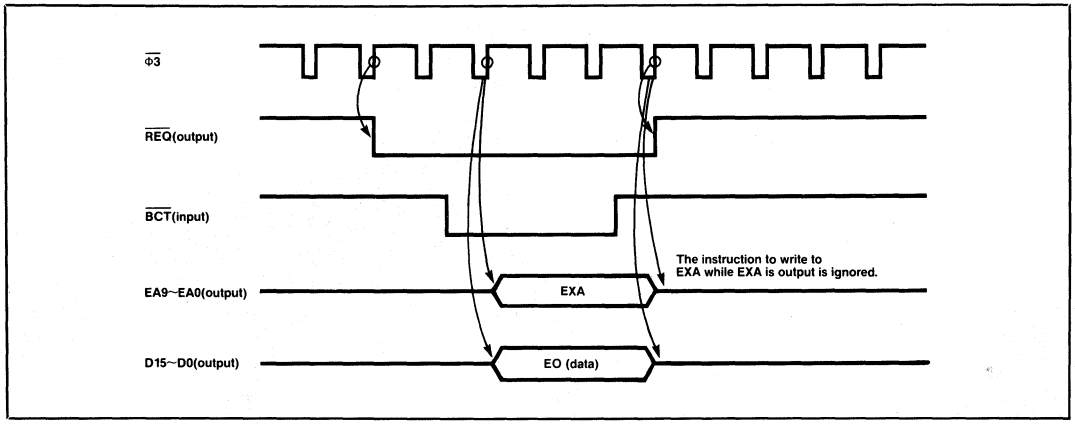


- Timing Specifications
- When ERAM is accessed:
  Same as MB8764 (input/output)
- When I/O bus is accessed:
  See the following timing diagram:

Input (P Mode/D Mode)



Output (New Mode)



6

Chip Enable Control Output ($\overline{ECE}$)

In the MB8764, $\overline{ECE}$ is always set to "0" (expansion RAM enable state) except when the I/O bus is being accessed for data transfer to-or-from an external circuit. In the MB87064, $\overline{ECE}$ is set to "0" only when ERAM is being accessed. This modification helps to reduce the power consumption of ERAM.

Hi-Impedance State of EA9 ~ EA0

Pins EA9 ~ EA0 are placed in the high-impedance state when neither ERAM nor I/O bus is accessed. This avoids address bus conflicts when multiple DSPs are used.

Reset Input According to $\overline{FL0}$ and $\overline{FL1}$ Status

The Reset signal ($\overline{RST}$) must be input while $\overline{FL0}$ and $\overline{FL1}$ are set to "1". The operation of the reset input flag is the same as the MB8764.

INSTRUCTION SET MODIFICATIONS

The MB87064 has the same instruction set as the MB8764 except for the following modifications to the SET/CLR and MOV instructions.

SET/CLR Instructions

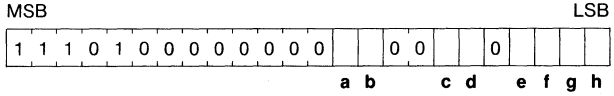
According to ADM flag removal, the following instructions are removed:

SET ADM
CLR ADM

The following instructions are added:

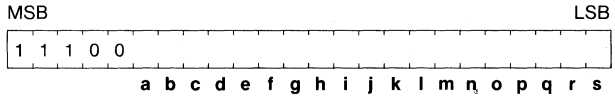
SET ESS	CLR ESS
SET TRC	CLR TRC
SET PCT	CLR PCT

Object code of SET instruction



a	b	c	d	e	f	g	h	set register	
1	0	0	0	0	0	0	0	DMM	
0	1	0	0	0	0	0	0	PCT	← new
0	0	1	0	0	0	0	0	VS	
0	0	0	1	0	0	0	0	ESS	← new
0	0	0	0	1	0	0	0	CLP	
0	0	0	0	0	1	0	0	TRC	← new

Object code of CLR instruction



a	b	c	d	e	f	g	h	i	j	k	l	m	n	o	p	q	r	s	cleared register	
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	D	
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	F0	
0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	F1	
0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	DMC	
0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	A	
0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	B	
0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	X	
0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	Y	
0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	DMM	
0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	PCT	← new
0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	IF	
0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	OF	
0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	VS	
0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	ESS	← new
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	OV	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	CLP	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	TRC	← new

- multiple registers can be specified
- execution cycle: one

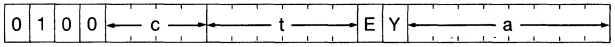
MOV Instruction

According to the EXA register addition, the destination of EXA register is added to the following MOV instruction:

MOV[:arithmetic/logic operation]$a(8)[([Y][E])],Reg[:Reg[:...]...]

machine code

MSB LSB



a: RAM address c: operation
t: destination

t						destination register	
1	0	0	0	0	0	EO	
0	1	0	0	0	0	A	
0	0	1	0	0	0	B	
0	0	0	1	0	0	D	
0	0	0	0	1	0	EXA (lower 10 bits of RAM data)	← new

- Two or more destination registers can be selected at once.

MOV Instruction (Cont.)

- An arithmetic/logic operation cannot be performed when the destination register is D.

According to EXA register addition, the processing of "d → EXA" is added.

MOV #$d,Reg

machine code

MSB LSB

t			processing	mnemonic	
0	0	0	d → EO	MOV #$d,EO	
0	0	1	output instruction	MOV #$d,EA(Note)	
0	1	0	d → D	MOV #$d,D	
0	1	1	d → B	MOV #$d,B	
1	0	1	d(lower ten bits) → EXA	MOV #$d,EXA	← new

Note:
Though the EA register does not exist, this instruction does exist in the MB87064 to maintain compatibility of output instruction with MB8764. This instruction is only effective as an output instruction and the processing of "d→EA" is ignored.

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS[1]

Parameter	Symbol	Value		Unit
		Min	Max	
Power Supply Voltage	V_{CC}	-0.3[2]	6.0	V
Input Voltage	V_I	-0.3[2]	V_{CC} + 0.3[2]	V
Output Voltage	V_O	-0.3[2]	V_{CC} + 0.3[2]	V
Operating Temperature	T_{OP}	-40	85	°C
Storage Temperature	T_{STG}	-55	150	°C

Notes:
1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. This value applies for a steady-state condition. The incremental voltage can be increased to a value of 0.5V for periods not to exceed 20-to-30 nanoseconds.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Operating Temperature	T_{OP}	-40		85	°C

DC CHARACTERISTICS

(Recommended Operating Conditions unless otherwise specified.)

Operating Temperature Range = 0°C to 70°C

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Input High Voltage	V_{IH}	Other than CK1, CK2	2.2		V_{CC} + 0.3	V
	V_{IHCK}	CK1, CK2	4.0		V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	Other than CK1, CK2	-0.3		0.8	V
	V_{ILCK}	CK1, CK2	-0.3		0.6	V
Output High Voltage	V_{OH}	I_{OH} = -0.4mA	2.7		V_{CC}	V
Output Low Voltage	V_{OL}	I_{OL} = 2mA	0		0.4	V
Input Leakage Current	I_{LI}	V_I = 0 to 5.5V	-10		10	μA
Input Leakage Current (Three-state Pin Input)	I_{LZ}	V_I = 0 to 5.5V	-20		20	μA
Static Power Supply Current	I_{CCS}			10		μA
Power Supply Current	I_{CC}	f_{OP} = 8MHz		50		mA

Operating Temperature Range = -40°C to 85°C

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Input High Voltage	V_{IH}	Other than CK1, CK2	2.8		V_{CC} + 0.3	V
	V_{IHCK}	CK1, CK2	4.0		V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	Other than CK1, CK2	-0.3		0.8	V
	V_{ILCK}	CK1, CK2	-0.3		0.6	V
Output High Voltage	V_{OH}	I_{OH} = -0.4mA	2.7		V_{CC}	V
Output Low Voltage	V_{OL}	I_{OL} = 2mA	0		0.4	V
Input Leakage Current	I_{LI}	V_I = 0 to 5.5V	-25		25	μA
Input Leakage Current (Three-state Pin Input)	I_{LZ}	V_I = 0 to 5.5V	-40		40	μA
Static Power Supply Current	I_{CCS}			50		μA
Power Supply Current	I_{CC}	f_{OP} = 8MHz		60		mA

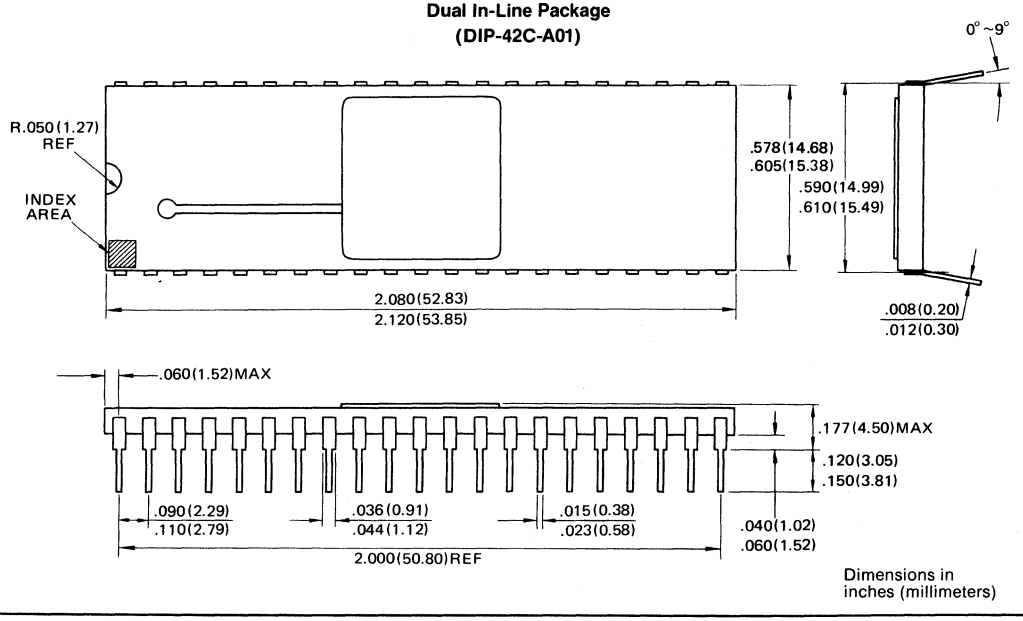
INPUT/OUTPUT CAPACITANCE

(V_{CC} = V_I = 0V, f_{OP} = 8MHz)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Input Pin	C_{IN}			6	pF
Output Pin	C_{OUT}			6	pF
I/O Pin	$C_{I/O}$			8	pF

Package Dimension

42-Lead Ceramic Multi
Dual In-Line Package
(DIP-42C-A01)



Dimensions in
inches (millimeters)