FUJITSU

ADPCM DIGITAL SIGNAL PROCESSOR

MB87067 MB87068

April 1996
Edition 1.0

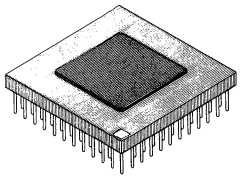
DESCRIPTION

The Fujitsu MB87067/MB87068 Digital Signal Processor (DSP) consists of two MB8764 DSPs each with an applications-specific program in the internal ROM. Together, the MB87067/MB87068 chip set provides all coding/decoding functions required to process Adaptive Pulse Code Modulation (ADPCM) signals. The MB87067 provides the encoding function and the MB87068 provides the decoding function. Under direction of the ADPCM programs stored in the two devices, the chip set allows the user to implement a CCITT standard ADPCM CODEC without any program development work. For complete electrical characteristics and functional detail of the MB8764 DSP, the user should refer to the current data sheet and, for additional DSP support, contact the nearest Sales Office of Fujitsu.

FEATURES

- High-performance design based on MB8764 DSP (Same electrical and timing specifications.)
- CCITT standard ADPCM coding/decoding (Selectable μ-law/A-law PCM).
- MB87067 provides u-law PCM bit-steal function: 7-bit decode function and bit-steal receiving function.
- ADPCM bit-steal function with transmit/receive signaling.
- TTL interface.
- Silicon gate CMOS fabrication process.
- Single 5-volt power supply.
- 88-pin grid array (PGA) package.

Advance Information



Ceramic Package
RIT-88C-A01

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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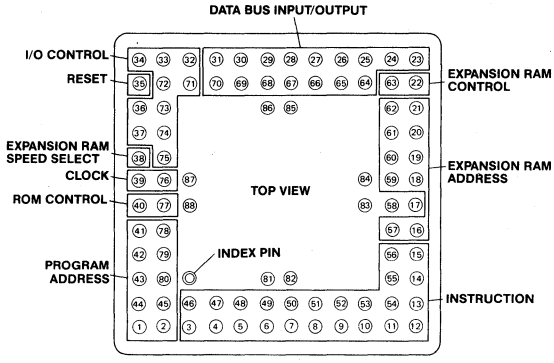
PIN ASSIGNMENTS



No.	Name	No.	Name	No.	Name	No.	Name	No.	Name	No.	Name
1	PA1	16	EA0	31	D14	46	P23	61	EA7	76	CK2
2	PA0	17	—	32	$\overline{\text{REQ}}$	47	P21	62	EA9	77	TST
3	P22	18	EA3	33	$\overline{\text{BCT}}$	48	P18	63	$\overline{\text{ECE}}$	78	PA9
4	P20	19	EA5	34	$\overline{\text{RCK}}$	49	P16	64	D2	79	PA6
5	P19	20	EA6	35	$\overline{\text{RST}}$	50	P15	65	D4	80	PA4
6	P17	21	EA8	36	$\overline{\text{FL0}}$	51	P13	66	D7	81	GND
7	P14	22	$\overline{\text{EWE}}$	37	$\overline{\text{WCK}}$	52	P10	67	D9	82	VCC
8	P12	23	D0	38	ESS	53	P8	68	D10	83	VCC
9	P11	24	D1	39	CK1	54	P6	69	D12	84	GND
10	P9	25	D3	40	IRM	55	P3	70	D15	85	GND
11	P7	26	D5	41	PA8	56	P1	71	$\overline{\text{ACT}}$	86	VCC
12	P5	27	D6	42	PA7	57	EA1	72	$\overline{\text{AIF}}$	87	VCC
13	P4	28	D8	43	PA5	58	—	73	$\overline{\text{FL1}}$	88	GND
14	P2	29	D11	44	PA3	59	EA2	74	$\overline{\text{AOF}}$		
15	P0	30	D13	45	PA2	60	EA4	75	$\overline{\text{ASL}}$		

PIN DESCRIPTIONS

Pin No.	Designator	Function	MB87067	MB87068
70	D15	Data Bus MSB	μ-law/A-law select	
31	D14	Data Bus BIT14	7-bit coding select	*/*
30	D13	Data Bus BIT13	*/*	*/*
69	D12	Data Bus BIT12	*/*	*/*
29	D11	Data Bus BIT11	*/*	*/*
68	D10	Data Bus BIT10	*/*	*/*
67	D9	Data Bus BIT9	*/*	*/*
28	D8	Data Bus BIT8	*/*	*/*
66	D7	Data Bus BIT7	PCM in/ *	* / PCM out
27	D6	Data Bus BIT6	PCM in/ *	* / PCM out
26	D5	Data Bus BIT5	PCM in/ *	* / PCM out
65	D4	Data Bus BIT4	PCM in/ *	* / PCM out
25	D3	Data Bus BIT3	PCM in/ADPCM out	ADPCM in/ PCM out
64	D2	Data Bus BIT2	PCM in/ADPCM out	ADPCM in/ PCM out
24	D1	Data Bus BIT1	PCM in/ADPCM out	ADPCM in/ PCM out
23	D0	Data Bus LSB	PCM in/ADPCM out	ADPCM in/ PCM out
34	$\overline{RCK}$	Data read clock		
33	$\overline{BCT}$	Data bus output enable	Control signal	
72	$\overline{AIF}$	Data input request		
37	$\overline{WCK}$	Data write clock		
74	$\overline{AOF}$	Output data type specification		
71	$\overline{ACT}$	Input enable		
62	EA9	Expansion RAM address MSB	PCM bit steal out	ADPCM bit steal out
36	$\overline{FL0}$	Flag input	Signaling input	Set to "1"
73	$\overline{FL1}$	Flag input	Signaling on/off	
35	$\overline{RST}$	Initialization	Reset	
39	CK1	Master clock input pin 1	20MHz clock	
76	CK2	Master clock input pin 2	20MHz clock	
40	IRM	Internal/External ROM switching	Set to "1"	
77	TST	Internal ROM test mode	Set to "0"	
75	$\overline{ASL}$	Data output type specification	Set to "1"	
38	ESS	ERAM speed select	Set to "0"	
22	$\overline{EWE}$	ERAM write clock	NC	
63	$\overline{ECE}$	ERAM chip enable	NC	
32	$\overline{REQ}$	Data bus request	NC	

Legend:
*Unused pin

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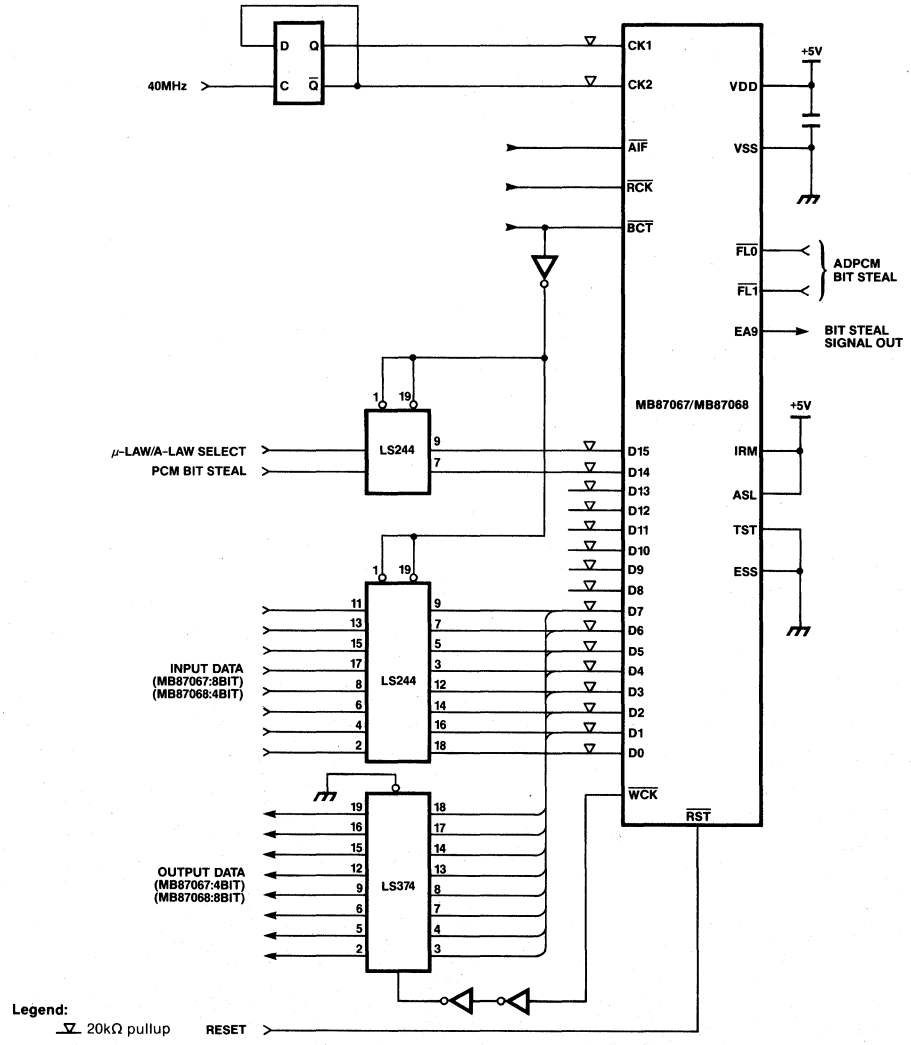
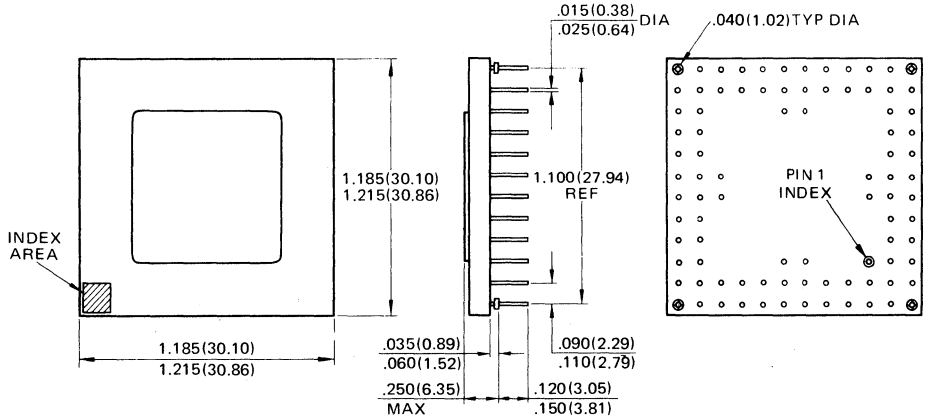
APPLICATIONS

Typical Coding/Decoding Configuration



PACKAGE DIMENSIONS

88-Lead Ceramic (Metal Seal)
Repeated Quad In-Line Package
RIT-88C-A01



Dimensions in
inches (millimeters)

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