FUJITSU

SERIAL INTERFACE ADAPTER (SIA)

MB87069

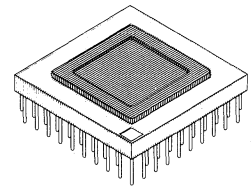
April 1986
Edition 1.0

DESCRIPTION

The Fujitsu MB87069 is a dedicated Serial Interface Adapter (SIA) that provides cost-effective interface support between the Fujitsu MB8764 Digital Signal Processor (DSP), PCM CODECs, and general purpose microprocessors. Some interface examples are shown later in this document.

FEATURES

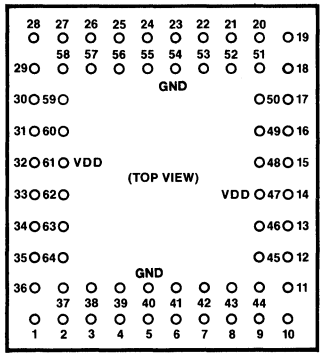
- Supports MB8764 for interface of PCM CODEC and microprocessor
- Serial I/O functions (dual input/output lines)
- Conversion circuits for μ-law/A-law data to linear data and vice-versa
- Interface circuit for microprocessor
- Software-controlled operations from MB8764 or microprocessor
- Silicon-gate CMOS process
- 64-pin Pin Grid Array (PGA) package



PGA-64C-A02

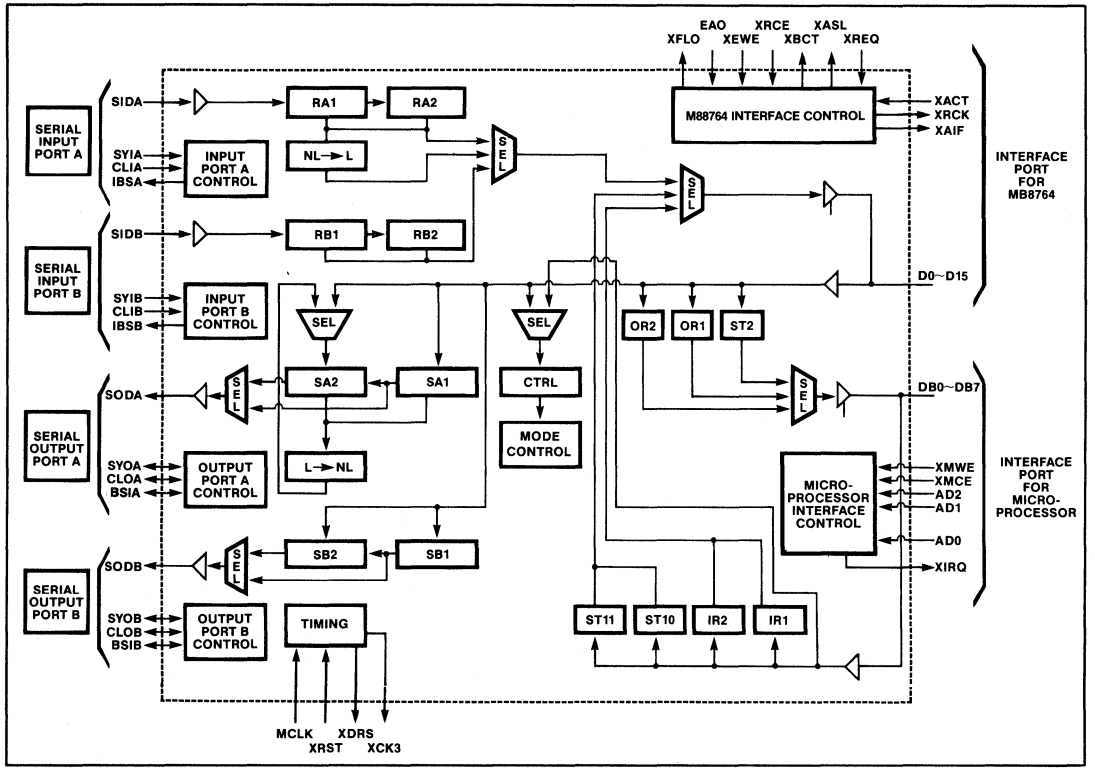
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

PIN ASSIGNMENTS



Pin No.	I/O	Pin Name	Pin No.	I/O	Pin Name	Pin No.	I/O	Pin Name	Pin No.	I/O	Pin Name
1	Output	XBCT	17	I/O	CLOB	33	Output	XCK3	49	Input	BSIA
2	Output	XAIF	18	I/O	SYOB	34	Output	XASL	50	Output	SODB
3	Input	XACT	19	Input	BSIB	35	Output	XFLO	51	Input	AD2
4	I/O	D15	20	Input	AD1	36	Output	XRCK	52	Input	XMCE
5	I/O	D12	21	Input	AD0	37	Inut	XREQ	53	Input	XMWE
6	I/O	D11	22	I/O	DB7	38	I/O	D14	54	—	GND
7	I/O	D8	23	I/O	DB6	39	I/O	D13	55	I/O	DB4
8	I/O	D6	24	I/O	DB5	40	—	GND	56	I/O	DB2
9	I/O	D5	25	I/O	DB3	41	I/O	D10	57	I/O	DB0
10	I/O	D3	26	I/O	DB1	42	I/O	D9	58	Input	SIDB
11	I/O	D2	27	Output	XIRQ	43	I/O	D7	59	Output	IBSA
12	I/O	D0	28	Output	IBSB	44	I/O	D4	60	Input	SIDA
13	Input	XEWE	29	Input	SYIB	45	I/O	D1	61	—	VCC
14	Input	EA0	30	Input	CLIB	46	Input	XRCE	62	Input	MCLK
15	I/O	SYOA	31	Input	CLIA	47	—	VCC	63	Input	XRST
16	I/O	CLOA	32	Input	SYIA	48	Output	SODA	64	Output	XDRS

BLOCK DIAGRAM



BLOCK ANALYSIS

Registers RA1 and RA2

These two 8-bit shift registers generate parallel data input from serial input port A. Register RA2 is only used for 16-bit inputs; the lower 8 bits are stored in RA1 and the upper 8 bits are stored in RA2.

Registers RB1 and RB2

These two registers perform the same function for serial input port B as RA1 and RA2 perform for port A.

Non-Linear to Linear Converter (NL → L)

Converts μ-law/A-law data to linear data.

Registers SA1 and SA2

When data is received from the MB8764, these registers perform a parallel-to-serial conversion and transfer the data to serial input port A. Register SA2 is only used for 16-bit data; in this case, the lower 8 bits are stored in SA1 and the upper 8 bits are stored in SA2.

Registers SB1 and SB2

These two registers perform the same function for serial input port B as SA1 and SA2 perform for port A.

Linear to Non-Linear Converter (L → NL)

Converts linear data to μ-law/A-law data.

Registers IR1 and IR2

Buffer interface registers for MB8764.

Registers OR1 and OR2

These two interface registers are used when data is transferred from the MB8764 DSP to the microprocessor.

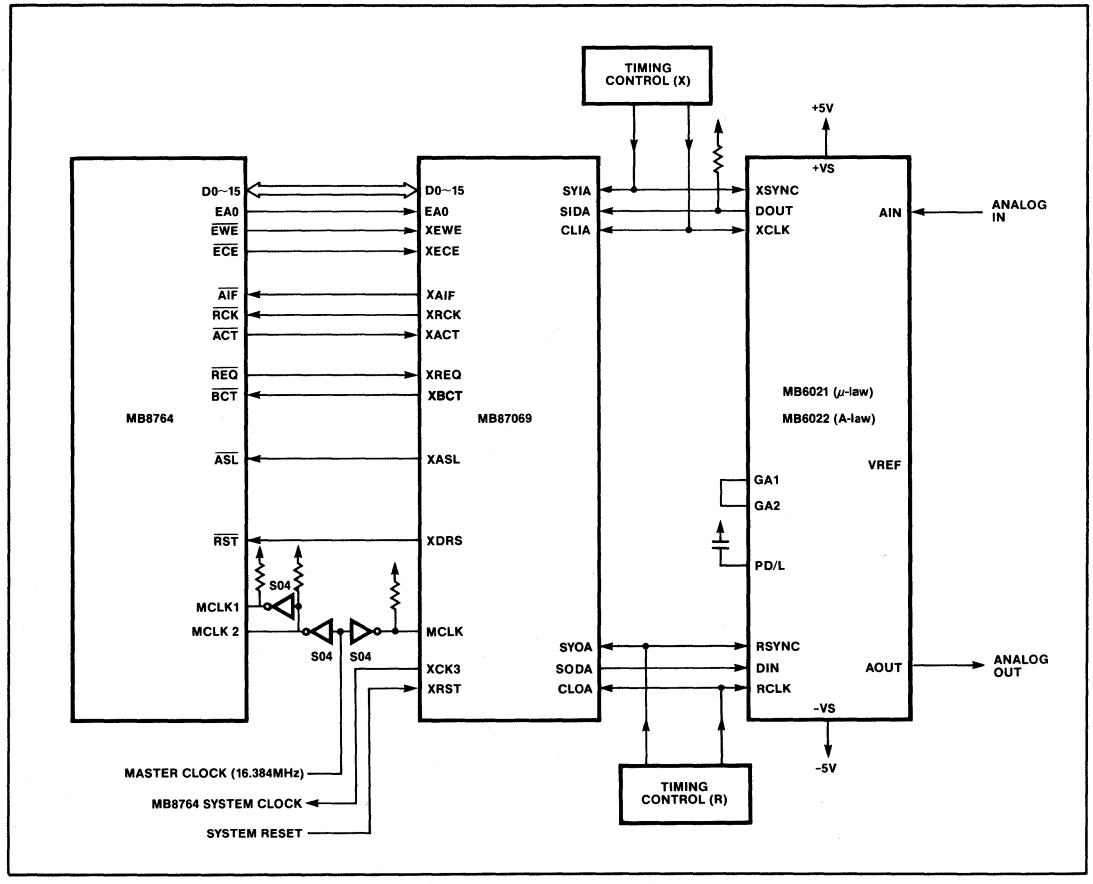
Registers ST2, ST10, and ST11

These registers perform handshake interface functions between the microprocessor and the SIA.

Control (CTRL) Register

This register specifies the operating mode of the SIA.

TYPICAL APPLICATIONS
Interface Between MB8764 (DSP) and MB6021/22 (CODEC) With MB87069 (SIA)



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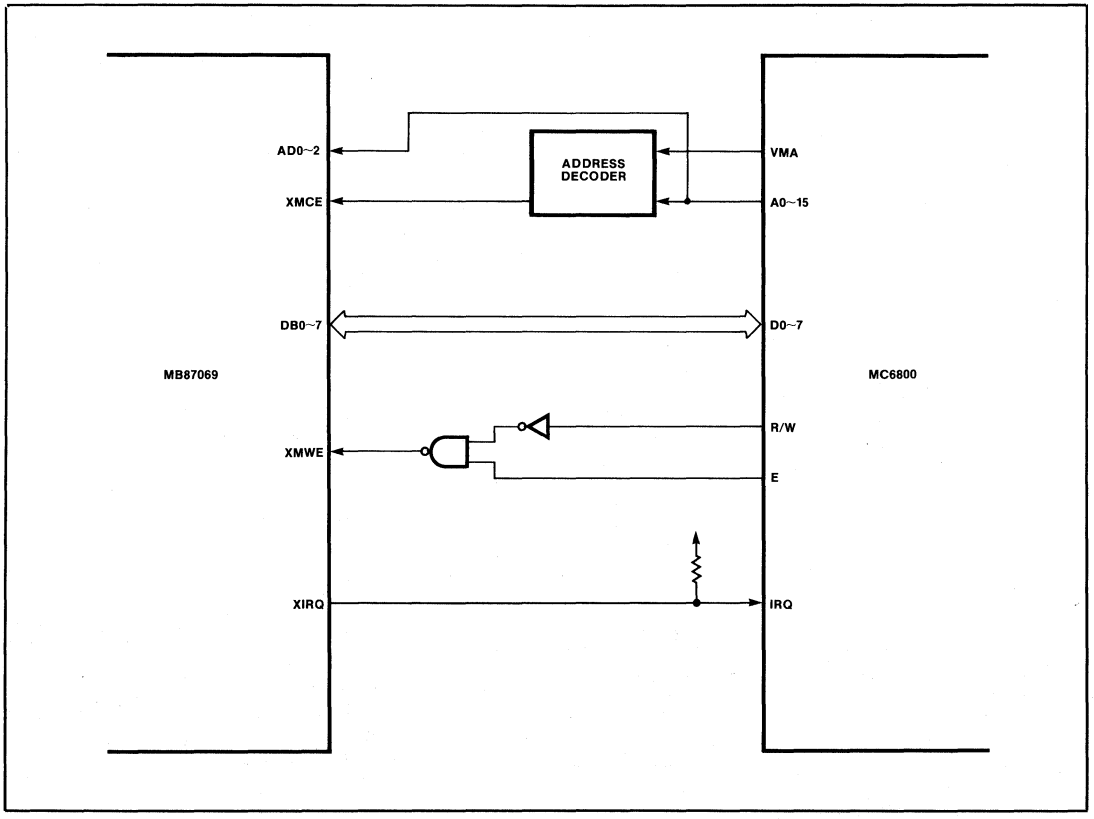
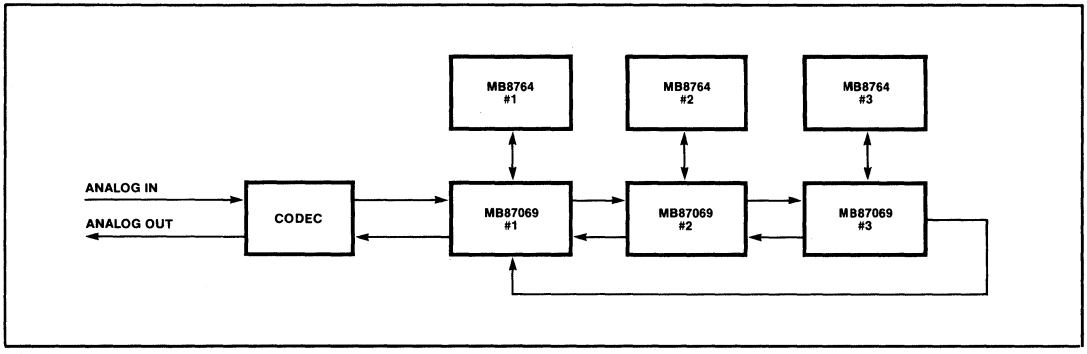
Interface Between MB87069 and Microprocessor (MC6800)

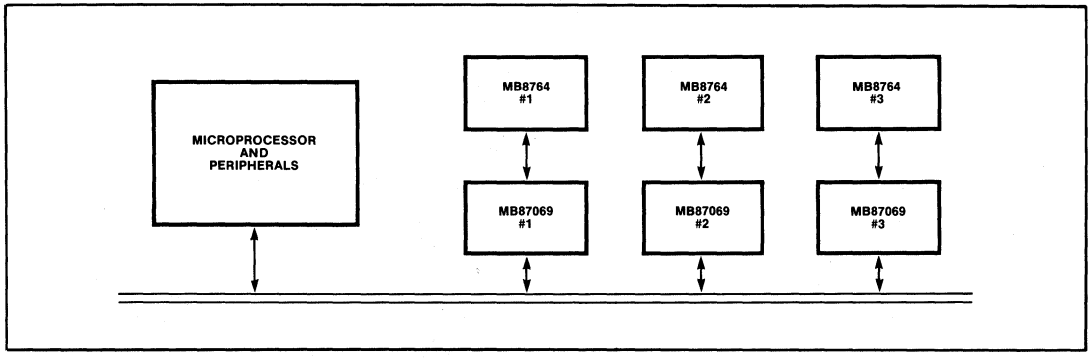


SYSTEM CONFIGURATIONS

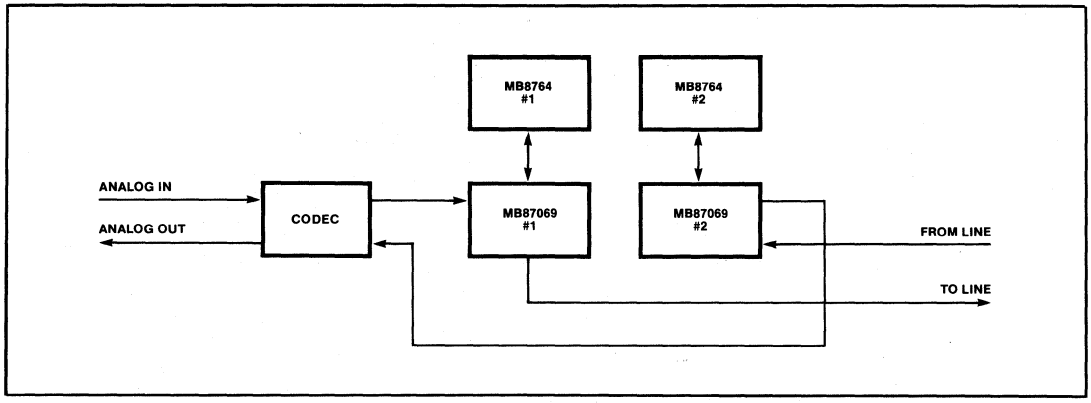
Echo Canceller



Microprocessor Interface Circuit



32 kbps ADPCM CODEC



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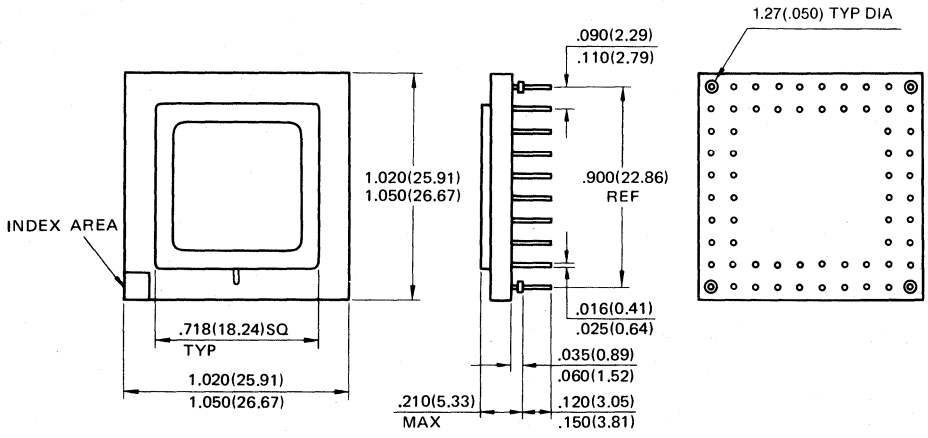
PACKAGE DIMENSIONS

64 Lead Ceramic (Metal Seal)
Repeated Quad In-Line Package
PGA-64C-A02



Dimensions in
inches (millimeters)