TM339-A872: February 1987

CMOS SINGLE-CHIP 4-BIT MICROCOMPUTER WITH A/D CONVERTER

The Fujitsu MB88210 series CMOS single-chip 4-bit microcomputer family is an economical low-end version of the conventional MB8850 series, as well as the MB88200 series. It is designed based on the MB88200 series architecture (that is a reduced architecture from the MB8850 series), and contains an A/D converter.

The currently available member of the MB88210 series is the MB88211 only. Its on-chip resources are almost same as the MB88202: The MB88211 contains a 1K x 8-bit program memory (mask ROM), 32 x 4-bit data memory (static RAM), 10 I/O lines (excluding analog input channel), 8-bit A/D converter, and a clock generator.

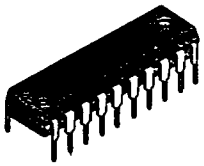
The MB88211 instruction set is a subset of the MB8850 series, and is a super set of the MB88200 series. Its instruction execution time is 3.0µs min. using a 4MHz clock (with a prescaler), as well as the MB8850/200 series.

The device is fabricated by the silicon-gate CMOS process, and packaged in a 20-pin plastic DIP (suffix -P). It operates with a single +5V power supply and a 4MHz clock with a prescaler over the temperature range of 0°C to 70°C.

CMOS technology allows the device to operate with low power dissipation (1mA typ. at Vcc=5V and fc= 1MHz).

For user's development of the MB88210 series based system, Fujitsu provides the MB88200 cross-assemblers which run on the CP/M-86 AND PC-DOS machines (cross-assembler also run on the Intellec series III MDS). the MB2115 series evaluation board system. These development tools enable users to minimizes their development time and cost.

MB88211-P



20-PIN PLASTIC DIP
(DIP-20P-M02)

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This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

FEATURES

- CMOS Single-chip 4-bit Microcomputer
- Program Memory: 1K x 8 bit mask ROM
- Data Memory: 32 x 4 bit static RAM
- 10 I/O Lines:
  - o R-Port: Two 4-bit and one 2-bit parallel, or 10 individual input/output ports
- Three Selectable Output Port Types for R-Port with Mask Option:
  - o Standard pull-up
  - o Standard open-drain
  - o Middle-current open-drain
- 8-bit Successive Approximation A/D Converter with One Analog Input
- On-chip Clock Generator:
  - o Crystal/ceramic resonator or external clock drive
- On-chip Divide-by-two Clock Prescaler for Expanding Clock Range
- Nesting Level: 4 levels
- Instruction Set: Super set of MB88200 series
  - o Number of instructions : 39
  - o Instruction length/cycle: 1 byte/1 cycle or 2 byte/2 cycle
  - o Execution time : 3.0μs min. using 4MHz clock with prescaler
- On-chip Power-on Reset Circuit
- Low-voltage Reset Function with Mask Option
- Output Port Level During Reset with Mask Option:
  - o High level
  - o Low level (R0-R3, R5-R8, R10)
- Low Power Dissipation: 1mA typ. at Vcc=5.0V and fc=1MHz
- Single +5V Power Supply: 4.5V to 5.5V
- Operating Temperature Range: T_A=0°C to +70°C
- Silicon-gate CMOS Process
- Package Type: 20-pin plastic DIP (Suffix: -P)
- Powerful Development Aupport:
  - o CP/M-86, PC-DOS, or Intellec series III MDS cross-assembler (SM07420-A012/SMXXXXXX-A010/SM05220-A010)
  - o CP/M-86 or PC-DOS host emulator software for monitoring evaluation board and symbolic debugging (SM07420-G022/SMXXXXX-G020)
  - o MB2115 series evaluating boards(MB2115-01, -02, -04, and -39) for software debugging/hardware emulation

Fig. 1: PIN ASSIGNMENT

MB88211-P (Top View)

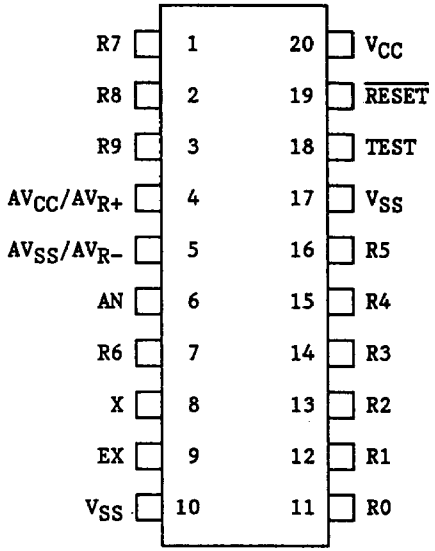


Fig. 2: LOGIC SYMBOL

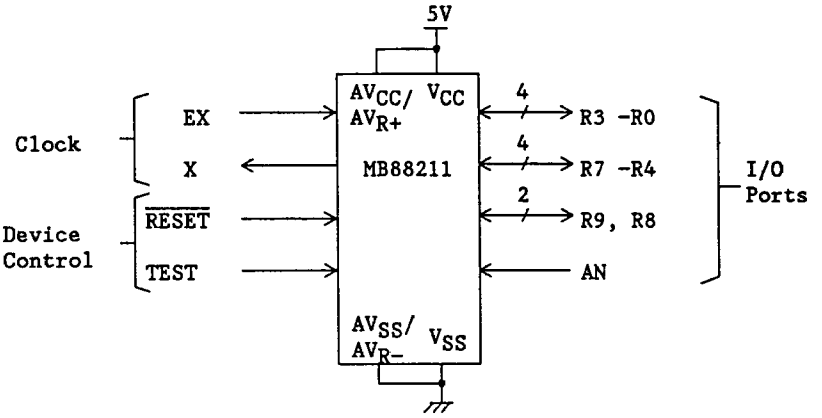
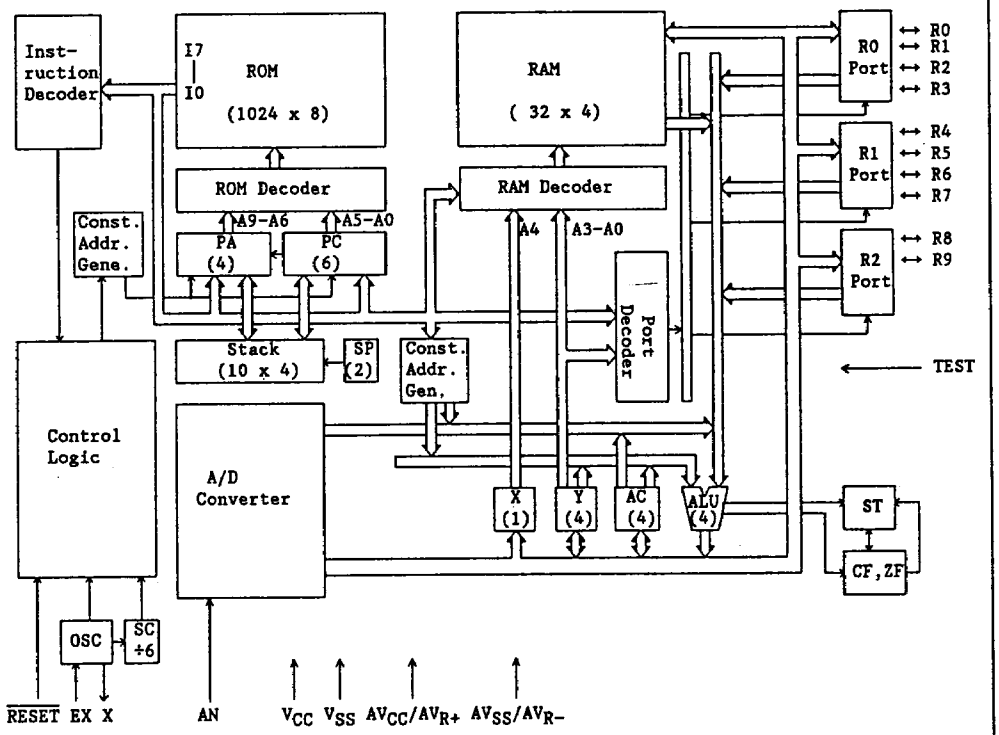


Fig. 3: BLOCK DIAGRAM



PIN DESCRIPTION

Fig. 1 and Table 1 show the pin assignment and pin description of the MB88210 series.

Table 1: PIN DESCRIPTION

Symbol	Pin No.	Type	Name & Function
• Power Supply			
V_{CC}	20	–	+5V DC power supply pin for the internal logic section.
V_{SS}	10, 17	–	Ground pin for the internal logic section.
AV_{CC}/AV_{R+}	4	–	+5V DC power supply pin for the internal A/D converter.
AV_{SS}/AV_{R-}	5	–	Ground pin for the internal A/D converter.
• Clock			
EX	9	I	**Oscillator Input:** Input to the inverting amplifier that forms the on-chip oscillator. An crystal/ceramic resonator is connected between the EX and X pins. When an external oscillator is used, the EX pin receives the external oscillator signal. This pin is a non-hysteresis input.
X	8	O	**Oscillator Output:** Output of the inverting amplifier that forms the on-chip oscillator, and input to the internal clock generator. An crystal/ceramic resonator is connected between the EX and X pins. When an external oscillator is used, the X pin should be left open.
• Device Control			
$\overline{RESET}$	19	I/O	**Reset:** This pin functions as an external reset input or power-on/low-voltage reset output. External reset input: A reset input to the internal reset circuit. A low level on the $\overline{RESET}$ pin forcedly stops the MCU's operations, and initializes its internal state. After the $\overline{RESET}$ pin returns high, the MCU restarts execution of program from address #0. The $\overline{RESET}$ pulse must be low for at least two instruction cycles (12 clock periodes: approximately 6µs using a 2MHz crystal without a prescaler) while the oscillator is stably running after power on. An external capacitor (and an internal pull-up resistor) or RC-network, whose time constant should be greater than the reset time required (12 clock periods), composes the external reset circuit. This pin is a hysteresis input with an internal pull-up resistor.

Table 1: PIN DESCRIPTION (Continued)

Symbol	Pin No.	Type	Name & Function
• Device Control (Continued)			
$\overline{\text{RESET}}$	19	I/O	Power-on/low-voltage reset output: A reset output from the on-chip reset control circuit. Normally this output is high during the active operation, except power-on/low-voltage reset. 1) Power-on reset output: The rising of the VCC voltage after power on outputs a negative pulse to the $\overline{\text{RESET}}$ pin. With an external RC-network at the $\overline{\text{RESET}}$ pin, whose time constant should be greater than the reset time reuired (the oscillator stabilization time, plus 12 clock periods), the power-on reset circuit is composed. 2) Low-voltage reset output: The $\overline{\text{RESET}}$ pin outputs a low level when the VCC voltage lowers below a threshold voltage during the active operating mode, and returns high when the VCC voltage recovers above the threshold voltage. With an external RC-network at the $\overline{\text{RESET}}$ pin, whose time constant should be greater than the reset time required (the oscillator stabilization time, plus 12 clock periods), the low-voltage reset circuit is provided. (The low-voltage reset function is mask optional.)
TEST	18	I	Test: A high level on the TEST pin forces the MCU into the test mode (which is used for the shipping test at Fujitsu) when the $\overline{\text{RESET}}$ pin is low. This pin is non-hysteresis input, and should externally be pulled down directly to the V_{SS} pin in the normal operation because it has no internal pull-down resistor.
• I/O Port			
R3 -R0, R7 -R4, R11-R8	14-11 15,16,7,1 3, 2	I/O	R-Port: This port functions as two 4-bit and one 2-bit parallel input (non-latched)/output (latched) ports, or 10 individual input (non-latched)/output (latched) lines, depending on instructions. Parallel I/O: Each 4-bit/2-bit port is named R-Port #0 (R3-R0), R-Port #1 (R7-R4), and R-Port #2 (R9-R8), and is indirectly addressed by the Y-register (Port #). 4-bit/2-bit data in the accumulator is output to an addressed port of R-Ports #0 to #2 by OUT instruction. 4-bit/2-bit data the addressed port is input into the accumulator by IN instruction. (Before IN instruction, the port to be addressed must be set up to "1" (input mode).)

Table 1: PIN DESCRIPTION (Continued)

Symbol	Pin No.	Type	Name & Function
• I/O Port(Continued)			
R3 -R0, R7 -R4, R11-R8	14-11 15,16,7,1 3, 2	I/O	Individual I/O: Each line from R9 to R0 is indirectly addressed by the Y-register (Bit #). An addressed line is individually set/reset by SETR/RSTR instruction, and is individually testable using TSTR instruction. (Before TSTR instruction, the line to be addressed must be set up to "1" (input mode).) R7, R8, and R9 have hysteresis inputs, while other lines have non-hysteresis inputs. For R-Port pins, one of the standard pull-up, standard open-drain, and middle-current open-drain output can be selected using mask option. The R-Port is set high (standard pull-up)/high-Z (standard or middle current drain), or low (except for R4 and R9), depending on mask option. For details, see Table 4 in page 13. * R10 and R11 have no external pins, but internally their I/O lines are still alive, and are connected to the internal A/D converter control circuit. They are used to control/monitor the A/D converter operation by software (SETR/RSTR and TSTR instructions). R10 and R11 are set high by reset.
AN	6	I	**Analog Port:** A dedicated analog input to the on-chip A/D converter. Analog signal on the AN pin is sampled and held at the falling edge of the first $\phi 1$ signal after initiating the A/D converter.

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DIFFERENCES BETWEEN MB88200 SERIES AND MB88210 SERIES

Table 2: DIFFERENCES BETWEEN MB88200 SERIES AND MB88210 SERIES

Item \ Device	MB88200 Series	MB88210 Series
ROM Size	· 1K x 8 bit: MB88202 · 512 x 8 bit: MB88201	· 1K x 8 bit
RAM Size	· 32 x 4 bit: MB88202 · 16 x 4 bit: MB88201	· 32 x 4 bit
Register	· Total 3: AC, X, Y: MB88202 · Total 2: AC, Y : MB88201	· Total 3: AC, X, Y
I/O Port	· 12-10 lines (R-Port) (Depending on oscillator and standby function options)	· 10 lines (R-Port)
Input Port Type (R-Port)	· Non-hysteresis input	· Non-hysteresis input: R6-R0 · Hysteresis input : R9-R7
Output Port Type (R-Port)	· Standard open-drain output · Standard pull-up output · Middle-current open-drain output (Planned) · 12V-Interface open-drain output (Mask option)	· Standard open-drain output · Standard pull-up output · Middle-current open-drain output (Mask option)
Stack Depth (Nesting Level)	· 4 levels: MB88202 · 2 levels: MB88201	· 4 levels
A/D Converter	· No	· Yes (8 bits x 1 channel)
Oscillator Type	· Crystal/ceramic oscillator · RC-network oscillator · Capacitor oscillator · External clock drive (Mask option)	· Crystal/ceramic oscillator or external clock drive (Fixed)
Clock Prescaler	· Yes · No (Mask option)	· Yes (Fixed)
Standby Function	· Yes (Software initiation) · No (Mask option)	· No
Operating Ambient Temperature	· -40°C to +85°C without low-voltage reset · -10°C to +70°C with low-voltage reset	· 0°C to +70°C regardless of low-voltage reset option
Number of Instructions	· 37: MB88201 · 38: MB88202	· 39
Package Type	· 16-pin plastic standard DIP: MB88201-P/202-P · 16-pin plastic flat pack: MB88201-PF/202-PF	· 20-pin plastic standard DIP: MB88211-P

Table 2: DIFFERENCES BETWEEN MB88200 SERIES AND MB88210 SERIES (Continued)

Item \ Device	MB88200 Series	MB88210 Series
Members	· MB88201-P/PF · MB88202-P/PF A-version are available	· MB88211-P

INPUT/OUTPUT CIRCUITS

All input-only pins are internally pulled up, and R-Port can have push-pull (standard pull-up) or open-drain (standard and middle-current open-drain) buffer using mask option.

Table 3: INPUT/OUTPUT CIRCUITS

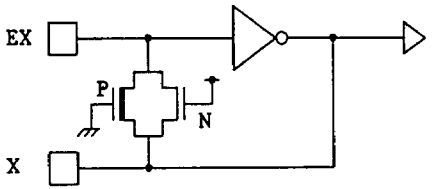
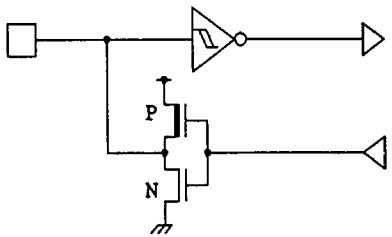
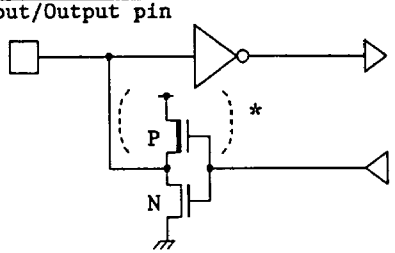
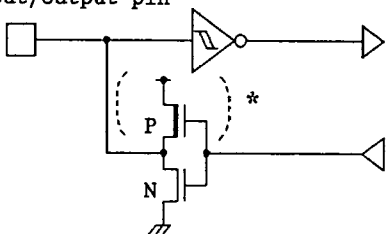
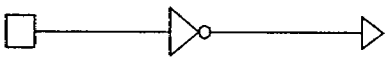
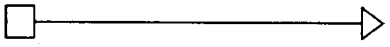
Pin	Circuit	Remarks
EX, X	• Crystal/Ceramic OSC 	· Non-hysteresis inverter · Feedback resistor: Approx. 2MΩ typ. (at V_{CC}=5V)
$\overline{RESET}$	• Input-only pin 	· Hysteresis inverter · Output pull-up resistor (P-ch. Tr.): Approx. 300kΩ typ. (V_{CC}=5V)
R6-R0	• Input/Output pin 	· Non-hysteresis inverter · Output port option -R1, R2, R4, R5: 1. Standard pull-up: Output pull-up resistor (P-ch. Tr.): Approx. 10kΩ typ. (at VCC=5V) -R6: 1. Standard pull-up: Output pull-up resistor (P-ch. Tr.): Approx. 1.5kΩ typ. (at VCC=5V) *2. Standard/Middle-current open-drain: Without P-ch. pull-up resistor -R0, R3: * Standard/Middle-current open-drain: Without P-ch. pull-up resistor

Table 3: INPUT/OUTPUT CIRCUITS(Continued)

Pin	Circuit	Remarks
R9-R7	• Input/Output pin 	· Hysteresis inverter · Output port option 1: Standard pull-up: Outtput pull-up resistor (P-ch. Tr.): Approx. 10kΩ typ. (at V_{CC}=5V) *2: Standard/Middle-current open-drain: Without P-ch. pull-up resistor
TEST	• Input-only pin 	· In the normal operation, should externally be pulled down.
AN	• Input-only pin 	· Analog input

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USER MASK OPTIONS

The MB88210 series has the following mask options, which must be specified by the customer on the attached data release form when devices are ordered.

Table 4: USER MASK OPTIONS

Optional Feature	Symbol	Option	Option No.	Note
Output Port Type*	PORT	Standard pull-up	M	Except R0 and R3: R0 and R3 are standard open-drain.
		Standard open-drain	L	
		Middle-current open-drain	K	10mA
Output Port Level During Reset **	RST	High level	0	
		Low level	1	Except R4 and R9: R4 and R9 are fixed high.
Low-Voltage Reset Function	PWR	No	1	
		Yes	2	

Notes:
* Only one of the four options can be selected. Mixed options are not permitted.
** Either "high level" or "low level" is applied to all R-Ports in a lump. Mixed options are not permitted.

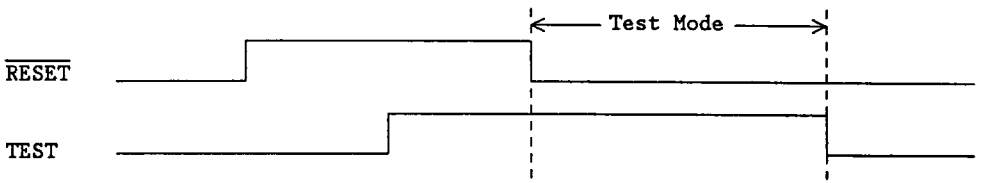
NOTES ON OPERATION

- **Latch-up Prevention**
  Latch-up may occur in CMOS devices when a voltage higher than V_{CC} or lower than V_{SS} is applied to input or output pin, or when a voltage exceeding the absolute maximum ratings is applied between V_{CC} and V_{SS} pins. If latch-up occurs, the supply current increases greatly, and the device may be thermally destroyed. Therefore, applied voltages should not exceed the maximum ratings.

- **Treatment of Unused Pins**
  Unused input pins should be externally pulled up or down with resistors because such unused input pins may cause some malfunction if they are left open.

- **TEST Pin**
  When the TEST pin is forced high while the $\overline{RESET}$ input is low, the MCU is placed to the test mode.

  Therefore, when the MCU is in normal operation and the test mode operation is not required, the TEST pin should not be forced high, even by noise, while the $\overline{RESET}$ input is low. For this purpose, normally the TEST pin should be externally be pulled down directly to the V_{SS} pin.



- **External Capacitance for Crystal Oscillation**
  The external capacitors should be adjusted to individual crystal resonators when precise oscillation frequency is required.

- **Supply Voltage**
  Malfunction may occur even within the recommended operating supply voltage if the supply voltage changes rapidly. Therefore, the supply voltage should be regulated as well as possible. The following conditions are recommended for the power supply:
  (1) V_{CC} ripple (peak-to-peak value) at commercial frequency (50Hz to 60Hz): Less than 10% of typical V_{CC} value.
  (2) V_{CC} transient change rate (such as at switching of power supply): Less than 0.1V/ms.

INSTRUCTION SET DESCRIPTION

The MB88210 series instruction set includes 39 instructions, 95% of which are single-byte and single-cycle, and 5% two-byte and two-cycle. The MB88210 series instruction set is a subset of the MB8850 series, and a super set of the MB88200 series. It is divided into nine functional groups:

- Register-to-register transfer
- Register-to-memory transfer
- Constant transfer
- Arithmetic and logical operations
- Bit manipulation
- Input/Output
- Branch
- Flag manipulation
- Other

Tables 5 and 6 summarize the MB88210 series instruction set.

Table 5: INSTRUCTION SET SUMMARY

	Mnemonic	Code (Hex.)	Flag/Status ZF	CF	ST	Byte/ Cycle	Operation
Register-to-Register Transfer	CLA	90	↓	·	·	1/1	AC←0 (Included by LI instruction)
	TAY	04	·	·	·	1/1	Y←(AC)
	TYA	14	↕	·	·	1/1	AC←(Y)
Register-to-Memory Transfer	L	0D		·	·	1/1	AC←{M(X,Y)}
	ST	1D	·	·	·	1/1	M(X,Y)←(AC)
	XD D	50-53*	↕*1	·	·	1/1	(AC)⇄{M(0,D)}; D=0 to 3
	XYD D	54-57*	↕*2	·	·	1/1	(Y) ⇄{M(0,D)}; D=4 to 7
Constant Transfer	LI imm	90-9F*	↕	·	·	1/1	AC←imm; imm=0 to 15
	LXI imm	58-59*	↕	·	·	1/1	X3 to X1←0, X0←imm; imm=0 or 1
	LYI imm	80-8F*	↕	·	·	1/1	Y←imm ; imm=0 to 15
Arithmetic & Logical Operations	ADC	0E	↕	↕	↓C	1/1	AC←(AC)+{M(X,Y)}+(CF)
	AI imm	70-7F*	↕	↕	↓C	1/1	AC←(AC)+imm; imm=0 to 15
	C	2E	↕	↕	↓Z	1/1	{M(X,Y)}-(AC)
	CI imm	B0-BF*	↕	↕	↓Z	1/1	imm-(AC); imm=0 to 15
	CYI imm	A0-AF*	↕	↕	↓Z	1/1	imm-(Y) ; imm=0 to 15
	DCA	7F	↕	↕	↓C	1/1	AC←(AC)+15 (Included by AI instruc-
	DCM	19	↕	·	↓C	1/1	M(X,Y)←{M(X,Y)}-1 tion)
	DCY	18	↕	·	↓C	1/1	Y←(Y)-1
	ICA	71	↕	↕	↓C	1/1	AC←(AC)+1 (Included by AI instruc-
	ICM	09	↕	·	↓C	1/1	M(X,Y)←{M(X,Y)}+1 tion)
	ICY	08	↕	·	↓C	1/1	Y←(Y)+1
	NEG	2D	·	·	↓Z	1/1	AC←(AC)+1
	SBC	1E	↕	↕	↓C	1/1	AC←{M(X,Y)}-(AC)-(CF)
Bit Manipulation	RBIT bp	34-37*	·	·	·	1/1	{M(X,Y)}bp←0; bp=0 to 3
	SBIT bp	30-33*	·	·	·	1/1	{M(X,Y)}bp←1; bp=0 to 3
	TBA bp	4C-4F*	·	·	↓C	1/1	(AC)bp-1 ; bp=0 to 3
	TBIT bp	38-3B*	·	·	↓C	1/1	{M(X,Y)}bp-1; bp=0 to 3
Input/ Output	IN	13	↕	·	·	1/1	AC←(R)Y ; Y=0 to 2 (Port #)
	INK	12	↕	·	·	1/1	AC←(DH) if R10=H AC←(DL) if R10=L
	OUT	03	·	·	·	1/1	(R)Y←(AC); Y=0 to 2 (Port #)
	RSTR	22	·	·	·	1/1	(R)Y←0; Y=0 to 11 (Bit #) *3
	SETR	20	·	·	·	1/1	(R)Y←1; Y=0 to 11 (Bit #) *3
	TSTR	24	·	·	↓C	1/1	(R)Y-1; Y=0 to 11 (Bit #) *3

Table 5: INSTRUCTION SET SUMMARY (Continued)

	Mnemonic	Code (Hex.)	Flag/Status ZF	CF	ST	Byte/ Cycle	Operation
Branch	CALL addr	6000-63FF*	·	·	·	2/2	If ST=1, Subroutine Call for addr; addr=0 to 1023 ST=0, Not Subroutine Call.
	JMP addr	C0-FF*	·	·	·	1/1	If ST=1, Branch to addr; addr=0 to 63 ST=0, Not Branch.
	JPL addr	6800-6BFF*	·	·	·	2/2	If ST=1, Branch to addr; addr=0 to 1023 ST=0, Not Branch.
	RTS	2C	·	·	·	1/1	Return From Subroutine
Flag Manipulations	RSTC	23	·	↕	·	1/1	CF←0
	SETC	21	·	↕	·	1/1	CF←1
	TSTC	28	·	·	↓CF	1/1	(CF)-1
	TSTZ	29	·	·	↓ZF	1/1	(ZF)-1
Other	NOP	00	·	·	·	1/1	No Operation

Notes:
* Code is variable depending on the operand.
*1: ZF is set or reset depending on contents of AC after instruction execution.
*2: ZF is set or reset depending on contents of Y after instruction execution.
*3: When Y=10 and 11, A/D converter's control/status register bits (ADC0=R10 and ADC1=R11) are addressed.

Symbols and Abreviations

Symbols	Meaning
←	Is transferred to
⇄	Is exchanged with
+	Arithmetic plus
−	Arithmetic minus
$\overline{\quad}$ (Overline)	Negation
( )	Contents of parenthesis
↑	Set to "1" always
↓	Set to "0" always
↕	Affected (set or reset) by operation results
↓C	Set to "0" due to carry (not carry flag)
↓CF	Set to "0" due to carry flag
↓Z	Set to "0" due to zero (not zero flag)
↓ZF	Set to "0" due to zero flag
·	Not affected

Abbreviations	Meaning
AC	Accumulator
addr	Jump address
bp	Bit pointer (that is part of the instruction code)
C	Carry
CF	Carry flag
D	Direct data memory address (that is part of the instruction code)
DH	A/D converter data register high nibble
DL	A/D converter data register low nibble
imm	Immediate data
LSB	Least significant bit
M(X,Y)	Data memory (RAM) location indirectly addressed by data pointer (X- and Y-registers)
M(0,D)	Data memory (RAM) location directly addressed by "D" bits in the instruction code, in page #0 (X=0)
MSB	Most significant bit
R	R-Port (#0: R3-R0, #1: R7-R4, #2: R9 and R8)
(R)Y; Y=n	① R-Port #n specified by Y-register (Y=0 to 2) ② R-Port bit n specified by Y-register (Y=0 to 11*) * 10 and 11 in Y-register address A/D converter's control/status bits.
ST	Status flag
X	X-register (that indicates page # in data memory RAM)
Xn	The n-th bit of X-register
Y	Y-register
Z	Zero
ZF	Zero flag

Table 6: INSTRUCTION CODE SUMMARY

H \ L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP			OUT	TAY				ICY	ICM				L	ADC	
1			INK	IN	TYA				DCY	DCM				ST	SBC	
2	SETR	SETC	RSTR	RSTC	TSTR				TSTC	TSTZ			RTS	NEG	C	
3	SBIT bp				RBIT bp				TBIT bp							
4													TBA bp			
5	XD D				XYD D				LXI imm							
6	CALL addr								JPL addr							
7	(ICA)	AI imm														(DCA)
8	LYI imm															
9	(CLA)	LI imm														
A	CYI imm															
B	CI imm															
C	JMP addr															
D																
E																
F																

Notes: : 1-byte/1-cycle instruction

: 2-byte/2-cycle instruction

PRODUCT LINEUP AND DEVELOPMENT TOOLS

The MB88210 series consists of the MB88211 only.

Table 7: MB88200 SERIES PRODUCT LINEUP & DEVELOPMENT TOOLS

	MB88211-P
ROM Size	1024 x 8 bits (On-chip mask ROM)
RAM Size (Directly addressed locations)	32 x 4 bits (0-7)
Register	Total 3: AC, X, Y
I/O Port: -Input-Only Port -Output-Only Port -I/O Port -Control Port	Total 10 lines 0 0 10 0
Input Port Type	Non-hysteresis : R6-R0 Hysteresis : R9-R7
Output Port Type	· Standard pull-up · Standard open-drain · Middle-current open-drain (Mask option)
A/D Converter: - Resoluation - Channel	 · 8-bit · 1 channel
Stack Depth	4
Clock Generator: -Oscillator Type -Clock Frequency	Yes · Crystal/External · 1MHz-4MHz
Clock Prescaler (1/2)	Yes (Fixed)
Reset Fuction: -External Reset -Power-on Reset Function -Low-volatge Reset Function -Output Port Level During Reset	 · Yes · Yes · Yes/No (Mask option) · High/Low (Mask option)
Standby Function:	· No
Instruction Set: -Number of Instruction -Length/Cycle	 39 1/1 or 2/2
Min. Instruction Execution Time	3.0μs min. at 4MHz (With Prescaler)
Power Supply	+5V
Ambient Temp. Range	T_A=0°C to 70°C
Process	CMOS
Package	20-pin DIP
Development Tools: -Hardware -Software 	 MB2115-01 : CRT unit (Common) MB2115-02 : Monitor board with keyboard (Common) MB2115-04 : EPROM writer (Common) MB2115-39 : DUE board SM05220-A010: Intellec series III MDS cross-assembler SM07420-A012: CP/M-86 cross-assembler SMXXXXX-A010: PC-DOS cross-assembler SM07420-G022: CP/M-86 host emulator SM0XXXX-G020: PC-DOS host emulator

ELECTRICAL CHARACTERISTICS

- **ABSOLUTE MAXIMUM RATINGS†**

Parameter	Symbol	Rating			Unit	Remarks
		Min.	Typ.	Max.		
Supply Voltage	V_{CC}	V_{SS}-0.3		V_{SS}+7.0	V	V_{SS}=AV_{SS}
Analog Power Supply Voltage	AV_{CC}/ AV_{R+}	V_{SS}-0.3		V_{SS}+7.0	V	V_{SS}=AV_{SS} Should not exceed AV_{SS}
Input Voltage	V_{IN}	V_{SS}-0.3		V_{SS}+7.0	V	V_{SS}=AV_{SS} Should not exceed V_{CC}+0.3V.
Output Voltage	V_{OUT}	V_{SS}-0.3		V_{SS}+7.0	V	V_{SS}=AV_{SS} Should not exceed V_{CC}(=AV_{CC})+0.3V.
Power Dissipation	P_D			200	mW	
Operating Ambient Temperature	T_A	0		+70	°C	
Storage Temperature	T_{STG}	-55		+150	°C	

† Permanent device damage may occur if the above ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

- **RECOMMENDED OPERATING CONDITIONS**

Parameter	Symbol	Value			Unit	Remarks
		Min.	Typ.	Max.		
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
	V_{SS}		0		V	
Analog Supply Volatge	AV_{CC}/ AV_{R+}	4.5	5.0	5.5	V	
	AV_{SS}/ AV_{R-}		0		V	
Input High Voltage	V_{IH}	0.7·V_{CC}		V_{CC}+0.3	V	R6-R0
	V_{IHS}	0.8·V_{CC}		V_{CC}+0.3	V	EX, $\overline{\text{RESET}}$, R9-R7
Input Low Voltage	V_{IL}	V_{SS}-0.3		0.3·V_{CC}	V	R6-R0
	V_{ILS}	V_{SS}-0.3		0.2·V_{CC}	V	EX, $\overline{\text{RESET}}$, R9-R7
Operating Ambient Temperature	T_A	0		70	°C	

- **DC CHARACTERISTICS** (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Pin/Port	Condition	Value			Unit
				Min.	Typ.	Max.	
Output High Voltage	V_{OH}	R1, R2, R4-R9 (Standard pull-up)	V_{CC}=4.5V I_{OH}=-200μA	2.4			V
			V_{CC}=4.5V I_{OH}=-10μA	4.0			V
Output Low Voltage	V_{OL}	R0-R9 (All output options)	V_{CC}=4.5V I_{OL}=1.8mA			0.4	V
		R0-R9 (Middle-current open-drain)	V_{CC}=4.5V I_{OL}=10mA			2.0	V
Input Leakage Current	I_{IL}	R1, R2, R4, R5, R7-R9(Standard pull-up)	V_{CC}=5.5V V_{IL}=0.4V		-0.6	-1.6	mA
		R6 (Standard pull-up)	V_{CC}=5.5V V_{IL}=0.4V		-3.5	-7.0	mA
		$\overline{\text{RESET}}$	V_{CC}=5.5V V_{IL}=0.4V			-60	μA
	I_{IH}	R0-R9 (All output options)	V_{CC}=5.5V V_{IH}=5.5V			10	μA
Output Leakage Current	I_{LEAK}	R0-R9 (All open-drains)	V_{CC}=5.5V V_{OH}=5.5V Output in high-Z			10	μA
Supply Current	I_{CC}	V_{CC}	V_{CC}=5.0V (Typ.) fc=4MHz Reset state All outputs open		1.0		mA

- **AC CHARACTERISTICS**

CLOCK TIMING (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Pin/ Port	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Clock Frequency	f_C	EX, X	Crystal/ceramic OSC or external clock drive: Fig. 4 and 5		4		MHz	With prescaler
Clock Cycle Time	t_{cyc}	EX, X	Fig. 4 and 5		0.25		µs	
Input Clock Pulse Width	P_{WCH}, P_{WCL}	EX	External clock drive (with X open): Fig. 4 and 5	100			ns	With prescaler
Input Clock Rise/Fall Time	t_{cr}, t_{cf}	EX	External clock drive (with X open): Fig. 4 and 5	5		100	ns	

Fig. 4: CLOCK TIMING

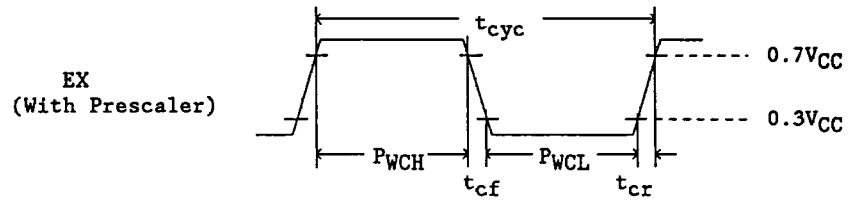
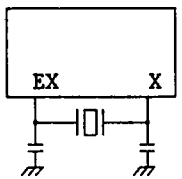
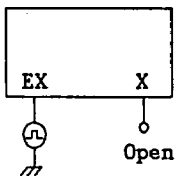


Fig. 5: CLOCK CIRCUIT CONFIGURATIONS

(1) Crystal/Ceramic Oscillation



(2) External Clock Drive



- **A/D CONVERTER CHARACTERISTICS**
  (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Pin	Value			Unit	Conditions
			Min.	Typ.	Max.		
Resolution *1					8	Bit	
Linearity Error *2					±1.0	LSB	T_A=25°C $AV_{CC}/AV_{R+}=V_{CC}$=5.0V $AV_{SS}/AV_{R-}=V_{SS}$=0V
Differential Linearity Error *3					±0.9	LSB	
Zero Transition Voltage	V_{OT}		-20	+10	+40	mV	
Full-Scale Transition Voltage	V_{FST}		+4910	+4970	+5030	mV	
Conversion Time	t_{CONV}			72		µs	f_C=4MHz
Analog Port Input Current	I_{AIN}	AN			5	µA	
Analog Input Voltage Range	V_{AIN}	AN	V_{SS}-0.3		V_{CC}+0.3	V	
Supply Current	I_A	AV_{CC}/AV_{R+}		2		mA	AV_{CC}=5.0V, AV_{SS}=0V fc=4MHz

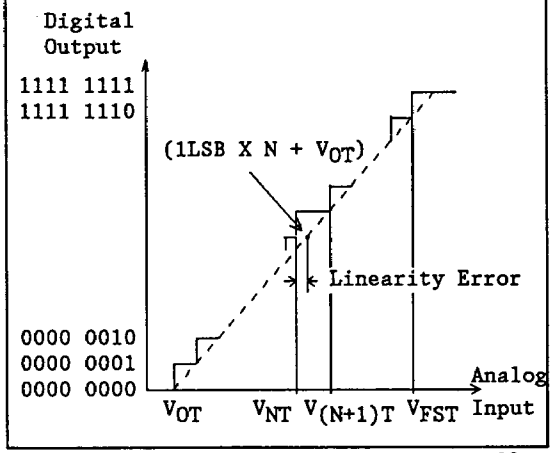
Notes:

*1: Resolution
The minimum variation in an analog signal that can be discriminated by the A/D converter. (An analog voltage can be divided into 2^8=256 parts.)

*2: Linearity Error
The difference between the line connecting the device zero transition point ("0000 0000" ↔ "0000 0001") with the full scale transition point ("1111 1111" ↔ "1111 1110"), and the actual conversion characteristics.

*3: Differential Linearity Error
The difference from ideal input voltage required to change the output voltage code by 1LSB.

Fig. 7: A/D TRANSFER CHARACTERISTICS



$$1LSB = \frac{V_{FST} - V_{OT}}{254}$$

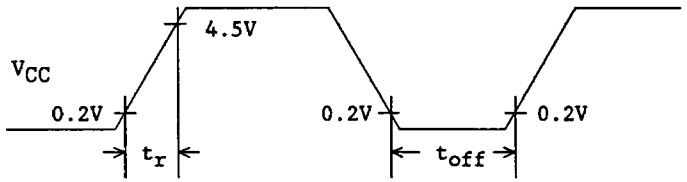
$$\text{Linearity Error} = \frac{V_{NT} - (1LSB \times N + V_{OT})}{1LSB} \quad [LSB]$$

$$\text{Differential Linearity Error} = \frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1 \quad [LSB]$$

- **POWER-ON RESET (BUILT-IN) CHARACTERISTICS**
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Condi-tions	Value		Unit	Remarks
			Min.	Max.		
Power Supply Rise Time	t_r	Fig. 8	0.05	50	ms	Required for operation of the power-on reset circuit
Power Supply Shout-off Time	t_{off}	Fig. 8	1		ms	Required for accurate circuit operation repeatability

Fig. 8: POWER-ON RESET TIMING

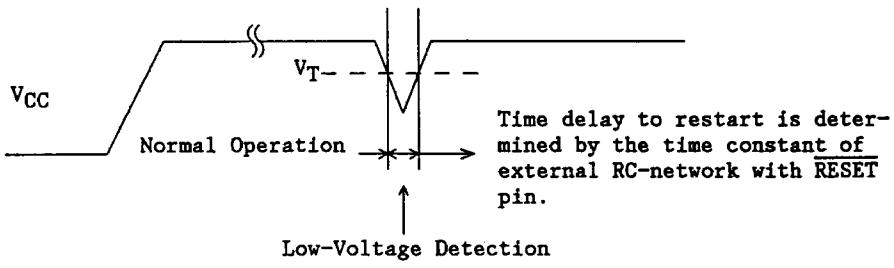


Note:
Power supply should be raised smoothly.

- **LOW-VOLTAGE RESET (MASK OPTION) CHARACTERISTICS**
(Recommended operating conditions unless otherwise noted.)

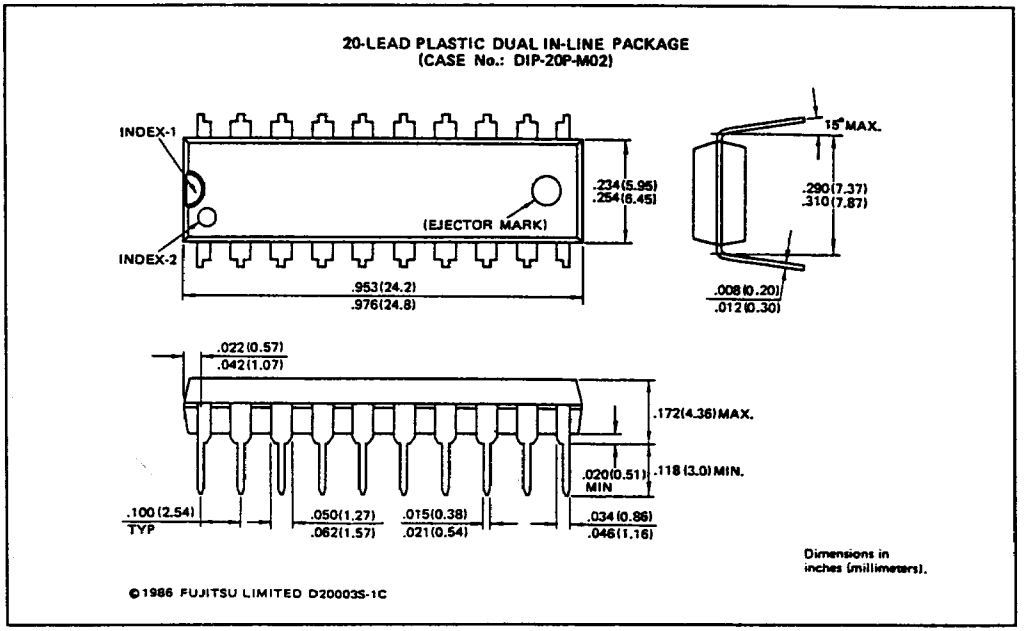
Parameter	Symbol	Condi-tions	Value		Unit	Remarks
			Min.	Max.		
Detection Voltage	V_T	Fig. 9	2.0	4.5	V	Reset is operational at less than V_T
Supply Voltage Rise/Fall Slope	$\Delta t/\Delta V$	Fig. 9	0.01		ms/V	

Fig. 9: LOW-VOLTAGE RESET TIMING



PACKAGE DIMENSIONS

• MB88211-P: 20-PIN PLASTIC DIP



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