# Preliminary

## Advanced Products

FUJITSU

# ■ MB88313

October 1986

## CMOS Television Display Controller (TVDC)

### DESCRIPTION

The Fujitsu MB88313 CMOS Television Display Controller (TVDC) is a programmable interface LSI device, which displays 16 alphanumeric and symbol characters of a 32-character set in four colors on a standard color TV (NTSC, PAL, SECAM, etc.) screen under control of a general 4 or 8-bit microcomputer.

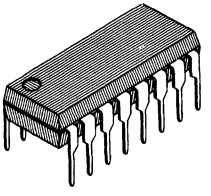
The MB88313 contains a display memory (16 x 8 bit static RAM), an address counter, six programmable control registers, a character generator (5 x 7 x 32-bit mask ROM), and a clock generator. 16 characters, of which codes are written into the display memory, and displayed on the TV screen, superimposed on the picture. Various screen features, such as screen format, character size, display start position, character attributes (color and blink), are controlled by programming the control registers using control commands serially loaded by the processor. The standard TVDC's character generator contains the Fujitsu standard character set. User designed character patterns are also acceptable on the mask ROM. The on-chip clock generator oscillates with an external RC or LC network.

The MB88313 is fabricated with the silicon-gate CMOS process, and packaged in a standard 16-pin plastic DIP or SOP. It operates with a single +5V power supply and 7 MHz clock over the ambient temperature range of −30°C to +70°C.

The MB88313 is suitable for display of simple character information on the TV screen, such as TV channel numbers, voice volume, VTR tape remainder and recording date and time, for which LCD or LED displays have been used.

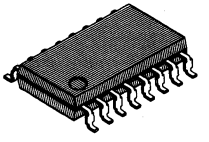
### FEATURES

- External synchronization type character display controller
- Display method: Characters are superimposed on the picture of a TV screen synchronized with TV $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ signals
- Command drive method: Display memory and internal registers are programmed by eight 8-bit control commands serially loaded by the processor
- Programmable screen format:
  —8 characters x 2 lines
  —16 characters x 1 line
- Fixed character format: 5 x 7 dot matrix with automatic rounding function
- 32 mask programmable character patterns:
  —Fujitsu standard character set
  —User-designed character set



8313-1

**Plastic DIP**
**(Suffix -P)**
**DIP-16P-M02**



8313-2

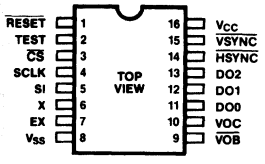
**Plastic SOP**
**(Suffix -PF)**
**FPT-16P-M02**

B38313

**FEATURES** (Continued)

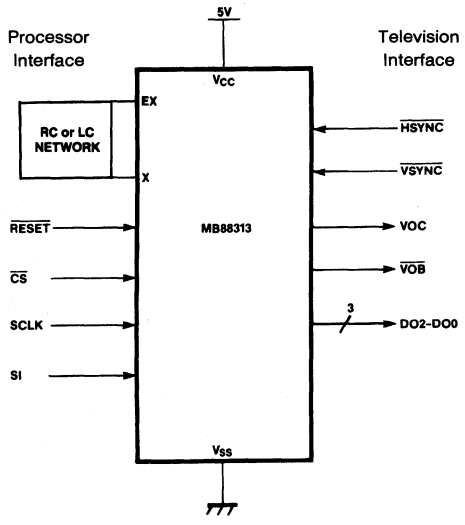
- Programmable character size:
  —4 selections for width
  —4 selections for height
- Programmable display position:
  —29 selections for horizontal position
  —31 selections for vertical position
- Programmable screen controls:
  —Screen format control
  —Background control
  —Blink control
  —Color control
- Interfaceable to general 4 & 8-bit microprocessors
- Interfaceable to standard color TV (NTSC, PAL, SECAM, etc.), standard monochrome TV sets, and interlace & non-interlace CRTs
- Seven programmable registers [address counter & control registers]
- 5 x 7 x 32-bit mask ROM [character generator]
- 16 x 8-bit static RAM [display memory]
- On-chip clock generator for external RC/LC components
- Silicon-gate CMOS process
- Single +5V power supply
- TTL compatible I/O ports
- Up to 7 MHz clock
- −30°C to +70°C operating temperature range
- Two package options:
  —16-pin DIP (Suffix -P)
  —16-pin SOP (Suffix -PF)

**PIN ASSIGNMENT AND LOGIC SYMBOL**




8313-3

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.




8313-4

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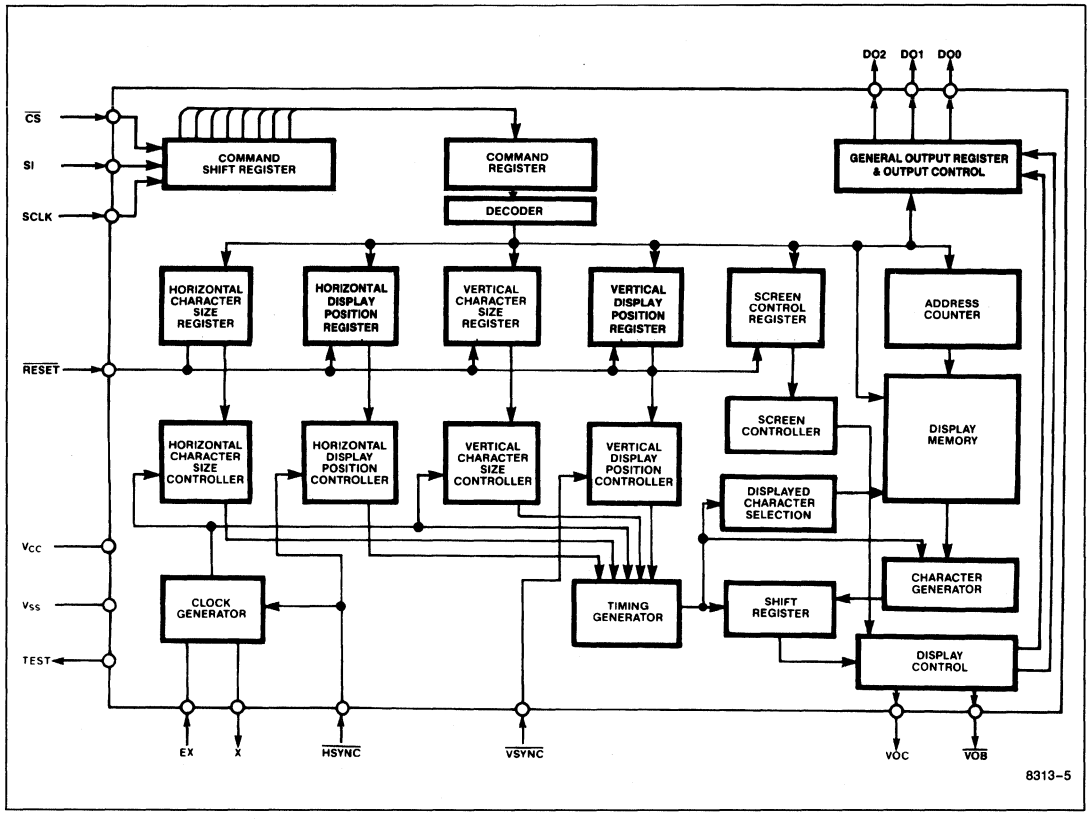
## BLOCK DIAGRAM



## PIN DESCRIPTION

The MB88313 TVDC has two interfaces: One is the processor interface consisting of, $\overline{CS}$, SCLK, and SI inputs which are used for the processor to serially load control commands into the TVDC. The other is the television interface, consisting of, $\overline{HSYNC}$ and $\overline{VSYNC}$ inputs and VOC, $\overline{VOB}$ and DO2–DO0 outputs which are used for the TVDC to display characters on the TV screen.

**Table 1. Pin Description**

| Symbol | Number | Type | Name & Function |
|---|---|---|---|
| **• Power Supply & Clock** | | | |
| $V_{CC}$ | 16 | — | +5 V dc power supply pin. |
| $V_{SS}$ | 8 | — | Power supply ground pin. |
| EX<br>X | 7<br>6 | I<br>O | Oscillator input/output: With an external capacitor (C) and resistor (R) or, inductor (L) and capacitors (C) connected to the EX and X pins, the on-chip oscillator generates the internal clock. A clock frequency is determined by the values of R and C, or L and C. |
| TEST | 2 | O | Test output: This output pin is enabled in the test mode, which is used for the shipping test purposes only at Fujitsu. In the normal operation mode, this output pin is low, and may be left open. |
| **• Processor Interface** | | | |
| $\overline{RESET}$ | 1 | I | Reset input: A low level on the $\overline{RESET}$ pin stops the TVDC's operations, initializes the internal control registers and clamps the outputs as follows:<br>1. Horizontal/vertical character size registers, horizontal/vertical display position registers, screen control register and general output register are all cleared.<br>2. All inputs are inactive.<br>3. VOC and DO2–DO0 output pins are clamped low, and $\overline{VOB}$ is clamped high.<br>The display memory is not affected by the $\overline{RESET}$. The command shift register, command register and address counter are undefined after a reset.<br>After the $\overline{RESET}$ pin is driven high, the TVDC restarts its display operations. *This pin is a hysteresis input.* |
| $\overline{CS}$ | 3 | I | Chip select input: A low level on the $\overline{CS}$ pin resets the internal SCLK counter, and enables the command shift register to receive serial data through the SI input pin. |
| SCLK | 4 | I | Shift clock input: The rising edge of the SCLK moves data on the SI pin into the command shift register, and also increments the internal SCLK counter. |
| SI | 5 | I | Serial command input: A command bit on the SI pin is shifted into the MSB of the command shift register at the rising edge of the SCLK. At the eighth rising edge, which is counted by the internal SCLK counter, an 8-bit command word is latched into the command register. |
| **• Television Interface** | | | |
| $\overline{HYSNC}$ | 14 | I | Horizontal sync input: Horizontal synchronization pulse signal (negative pulse) provided by TV set should be applied to this input pin. The TVDC outputs character and background signals (VOC and $\overline{VOB}$) synchronously with this signal. *This pin is a hysteresis input.* |
| $\overline{VSYNC}$ | 15 | I | Vertical sync input: Vertical synchronization pulse signal (negative pulse) provided by TV set should be applied to this input pin. The TVDC outputs character and background signals (VOC and $\overline{VOB}$) synchronously with this signal. *This pin is a hysteresis input.* |

4

**PIN DESCRIPTION** (Continued)

| Symbol | Number | Type | Name & Function |
|---|---|---|---|
| VOC | 10 | O | Video output for character: This pin outputs a high level for character dot patterns, and is clamped low during the reset mode, standby mode, and non-display mode, disabling character display on the TV screen. |
| $\overline{VOB}$ | 9 | O | Video output for background: This pin outputs a low level for background or edge portion of character dot matrix during the background or edge mode, respectively.<br>The $\overline{VOB}$ output is clamped high during the reset mode, standby mode, non-display mode, and non-background/edge mode, disabling background and edge displays on the TV screen. |
| DO2–DO0 | 13–11 | O | Data outputs: These outputs are controlled by the GOC bit: When GOC = 0 (i.e., the general output mode), a 3-bit data in the on-chip general output register is output at these output pins. These are used for general control outputs. When GOC = 1 (i.e., the color display mode), the attribute code bits AC1 and AC0 are output at the DO1 and DO0 pins, respectively. These are used as color control data. The remaining bit of the general output register appears at the DO2 pin. |

## BLOCK DESCRIPTION

Refer to Block Diagram on page 3.

The MB88313 TVDC contains the following main functional blocks:

- Clock generator
- Character generator
- Display memory
- Address counter
- Command shift register and command register
- Six control registers

(Address counter, Command shift register and command register, Six control registers) } Register Set

### Clock Generator

The MB88313 has an on-chip clock generator, which provides a basic timing clock to internal circuits. The clock frequency is determined by external RC or LC network.

For synchronization, the clock supply to the internal circuit is stopped while the $\overline{HSYNC}$ is low. The clock generator is stopped during the standby mode, which is initiated by software (Command 6).

### Character Generator

The MB88313 has a 5 x 7 x 32 bit mask ROM as a character generator, which stores thirty-two 5 x 7-dot character patterns encoded into character codes. The character generator defines a character set. The standard MB88313 has the Fujitsu standard character set shown in Figure 15. Those characters are indicated by character codes shown in Table 5. A user-designed character set is also programmed on the mask ROM using metal option. But character codes, (0F)H and (1F)H are reserved as "blank" and "background" codes.

### Display Memory

The MB88313 has a 16 x 8 bit static RAM as a display memory, which stores 16 character codes and their attribute codes to be displayed on the TV screen. The 16 memory locations are addressed by a 4-bit address counter (A3–A0). Figure 1 shows the display memory map: Each memory word is divided into two fields: The lower 5 bits (CH4–CH0) defines a character code, and the upper 3 bits (AC2–AC0) defines its attribute codes (color code and blink code). Each field of a word addressed by the address counter is written separately by the processor using Commands 0 and 6 respectively. See Table 1. The display memory is not affected by $\overline{RESET}$, and is retained during the standby mode.

### Register Set

The MB88313 contains a register set consisting of an address counter, command shift register, command register, and six control registers, which are programmed using control commands or directly loaded by the processor. See Table 1.

### Command Shift Register and Command Register (CM7–CM0)

The command shift register is an 8-bit serial-in/parallel-out shift register that assembles serial command bits (provided by the processor through the SI input synchronously with the SCLK input) into an 8-bit command word during the command load operation.

The command register is an 8-bit write-only register that holds control commands transferred in parallel from the command shift register. The transferred 8-bit command word is output to

**BLOCK DESCRIPTION** (Continued)

the command decoder to generate internal control signals. Figure 2 shows the command shift register and command register configuration.

Both registers are undefined after a reset, and hold the current state during the standby mode.

**Address Counter (A3–A0)**

The address counter is a 4-bit binary counter which addresses a display data memory location written by Commands 0 and 6. The address counter is preset by Command 1, and is automatically incremented by Command 0. Figure 3 shows the address counter format. The address counter is undefined after a reset, and holds the current state during the standby mode.

**Horizontal Display Position Register (HP4–HP0)**

The horizontal display position register is a 5-bit write-only register which selects one of 29 horizontal positions from where the first character (including blank and background) begins to appear on the screen. This control register is programmed by the processor using Command 2, and cleared by $\overline{\text{RESET}}$. Figure 4 shows the horizontal position register format. During the standby mode, this register holds the current state.

**Figure 1. Display Memory Map**

| | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| Address (Hex) | AC2 | AC1 | AC0 | CH4 | CH3 | CH2 | CH1 | CH0 |
| 0 | | | | | | | | |
| 1 | | | | | | | | |
| 2 | | | | | | | | |
| 3 | | | | | | | | |
| 4 | | | | | | | | |
| 5 | | | | | | | | |
| 6 | | | | | | | | |
| 7 | | | | | | | | |
| 8 | | | | | | | | |
| 9 | | | | | | | | |
| A | | | | | | | | |
| B | | | | | | | | |
| C | | | | | | | | |
| D | | | | | | | | |
| E | | | | | | | | |
| F | | | | | | | | |
| | Attribute Code Field | | | Character Code Field | | | | |

**Notes:**

1. Address is indicated by Address Counter, which is setup using Command 1.
2. Attribute code field is written by Command 6.
3. Character code field is written by Command 0.

**Table 2. Display Memory & Register Set Summary**

| Register Name | | Bit Symbol | Programming Method |
|---|---|---|---|
| Display Memory | | AC2–AC0: CH4–CH0 | Command 0, Command 6 |
| Command Shift Register & Command Register | | CM7–CM0 | Serial Load & Parallel Latch |
| Address Counter | | A3–A0 | Command 1 |
| Control Registers | Horizontal Display Position Register | HP4–HP0 | Command 2 |
| | Vertical Display Position Register | VP4–VP0 | Command 3 |
| | Horizontal Character Size Register | HS1–HS0 | Command 4 |
| | Vertical Character Size Register | VS1–VS0 | Command 4 |
| | Screen Control Register | SC4–SC0 | Command 5 |
| | General Output Register | GO2–GO0 | Command 7 |

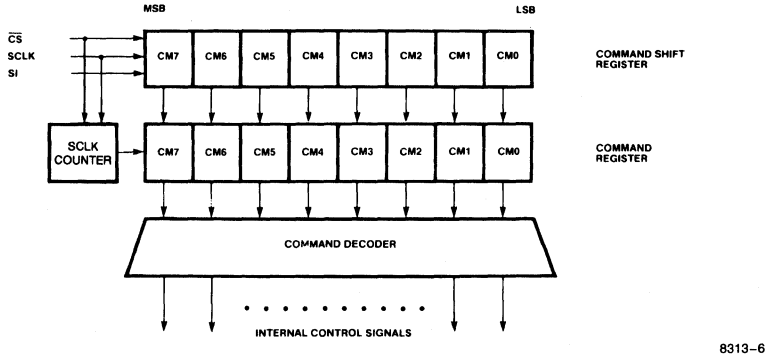
4

**BLOCK DESCRIPTION** (Continued)

### Vertical Display Position Register (VP4–VP0)

The vertical display position register is a 5-bit write-only register which selects one of 31 vertical positions from which the first character (including blank and background) begins to appear on the screen. This control register is programmed by the processor using Command 3, and is cleared by $\overline{\text{RESET}}$. Figure 5 shows the vertical position register format. During the standby mode, this register holds the current state.

**Figure 2. Command Register Configuration**




**Note:**
Command register is written by the processor through command shift register.

**Figure 3. Address Counter Format**

| MSB | | | LSB |
|---|---|---|---|
| A3 | A2 | A1 | A0 |

**Note:**
Address counter is programmed by Command 1.

**Figure 4. Horizontal Position Register Format**

| MSB | | | | LSB |
|---|---|---|---|---|
| HP4 | HP3 | HP2 | HP1 | HP0 |

**Notes:**

1. $HP = T \times (4 \times (2^5HP4 + 2^4HP3 + 2^3HP2 + 2^2HP1 + 2HP0) + P)$
   Where, P = 10, 11, 12 and 13 for (HS1, HS0) = (0,0), (0,1), (1,0) and (1,1), respectively
   HP: Horizontal display start position; referenced to the rising edge of $\overline{\text{HSYNC}}$
   T: Clock Cycle time; T(S) = 1/fc [Hz]
2. Horizontal position register is programmed by Command 2.

**Figure 5. Vertical Position Register Format**

| MSB | | | | LSB |
|---|---|---|---|---|
| VP4 | VP3 | VP2 | VP1 | VP0 |

**Notes:**

1. $VP = H \times 4 \times (2^5VP4 + 2^4VP3 + 2^3VP2 + 2^2VP1 + 2VP0) + 1)$
   Where, VP: Vertical display start position; referred to the rising edge of $\overline{\text{VSYNC}}$
   H: Horizontal sync cycle time; H = 63.5 [μs]
2. Vertical position register is programmed by Command 3.

**Table 3. DO Outputs in Color Display Mode**

| Video Signal | | DO Outputs | | | Display |
|---|---|---|---|---|---|
| $\overline{\text{VOB}}$ | VOC | DO2 = GO2 | DO2 = AC1 | DO0 = AC0 | |
| X | 1 | X | 0 | 0 | Character |
| | | | 0 | 1 | |
| | | | 1 | 0 | |
| | | | 1 | 1 | |
| 1 | 0 | 0 | 0 | X | Blank |
| 0 | | | | | Black (Background) |

**BLOCK DESCRIPTION** (Continued)

### Horizontal Character Size Register (HS1 and HS0)

The horizontal character size register is a 2-bit write-only register which selects one of 4 character widths. This control register is programmed by the processor using Command 4, and cleared by $\overline{\text{RESET}}$. Figure 6 shows the horizontal character size register format. During the standby mode, this register holds the current state.

### Vertical Character Size Register (VS1 and VS0)

The vertical character size register is a 2-bit write-only register which selects one of 4 character heights. This control register is programmed by the processor using Command 4, and cleared by $\overline{\text{RESET}}$. Figure 7 shows the vertical character size register format. During the standby mode, this register holds the current state.

### Screen Control Register (SC4–SC0)

The screen control register is a 5-bit write-only register which controls screen features: Screen format, display mode, and blinking. This control register is programmed by the processor using Command 5, and cleared by $\overline{\text{RESET}}$. Figure 8 shows the screen control register format and bit functions. During the standby mode, this register holds the current state.

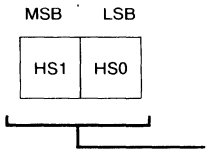
**Note:**

When the display is disabled (SC0 = 0), the background must be also disabled (SC1 = 0).

### General Output Register (GO2–GO0)

The general output register is a 3-bit write-only output register which latches 3-bit output data written into by Command 7. Depending on the general output register control bit GOC, the TVDC has two output modes for the DO2–DO0 pins. During the general output mode (GOC = "0"), the latched data appears at

**Figure 6. Horizontal Character Size Register Format**

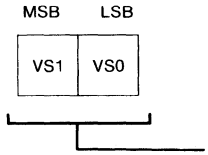



| Horizontal Size Code | | Horizontal Character Size (Width) | Horizontal Dot Size |
|---|---|---|---|
| HS1 | HS0 | | |
| 0 | 0 | 10T | 2T |
| 0 | 1 | 20T | 4T |
| 1 | 0 | 30T | 6T |
| 1 | 1 | 40T | 8T |

8313-7

**Notes:**
1. T: Clock cycle time; T[s] = 1/fc [Hz]
2. Horizontal character size register is programmed by Command 4.

**Figure 7. Vertical Character Size Register Format**




| Vertical Size Code | | Vertical Character Size (Height) | Vertical Dot Size |
|---|---|---|---|
| VS1 | VS0 | | |
| 0 | 0 | 14H | 2H |
| 0 | 1 | 28H | 4H |
| 1 | 0 | 42H | 6H |
| 1 | 1 | 56H | 8H |

8313-8

**Notes:**
1. H: Horizontal sync cycle time; H = 63.5 [μs]
2. Vertical character size register is programmed by Command 4.

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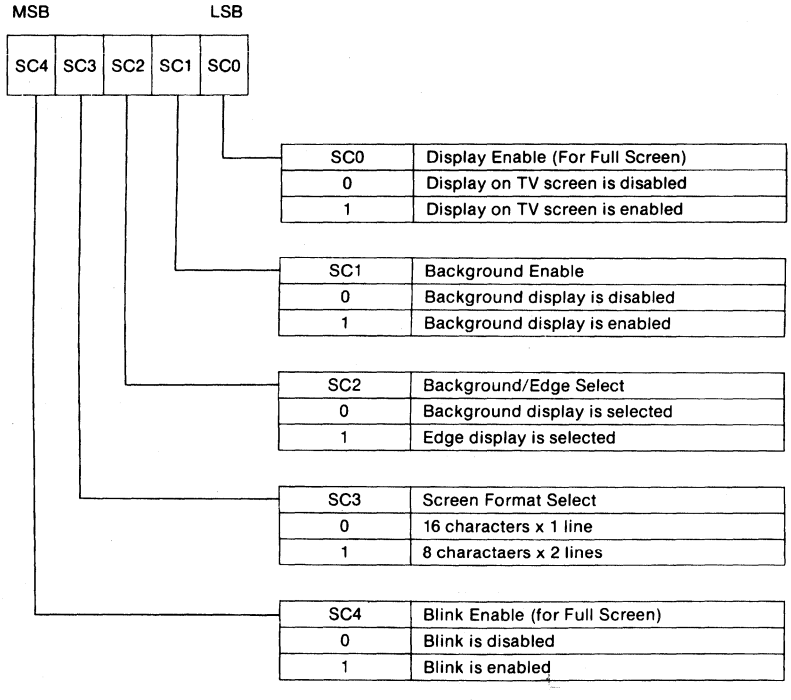
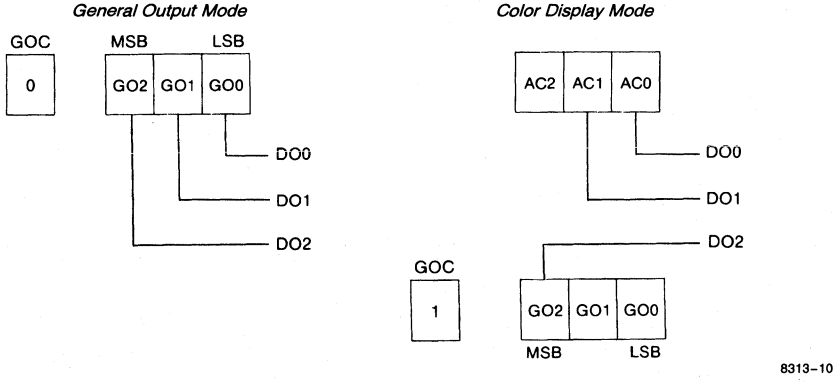
**BLOCK DESCRIPTION** (Continued)

**Figure 8. Screen Control Register Format**




**Note:**
Screen control register is programmed by Command 5.

**Figure 9. General Output Register Format**




**Note:**
General output register is programmed by Command 7.

**BLOCK DESCRIPTION** (Continued)

the DO2–DO0 output pins. During the color display mode (GOC = "1"), the color code bits AC1 and AC0 stored in each attribute field of the display memory are automatically output on the DO1 and the DO0 pins respectively while the VOC output is high. When the VOC is low, the DO1 and DO0 pins are clamped low. The GO2 bit only appears at the DO2 in the color display mode. See Table 3. Controlling RGB signals by the DO1 and DO0 and VOC, four-colored characters can be displayed.

This control register and control bit GOC are programmed by the processor using Command 7, and cleared by $\overline{\text{RESET}}$. Figure 9 shows the general output register format. During the standby mode and non-display mode, the DO2–DO0 output are clamped low, regardless of the general output mode or the color display mode.

**FUNCTIONAL DESCRIPTION**

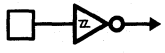
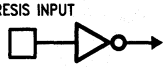
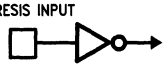
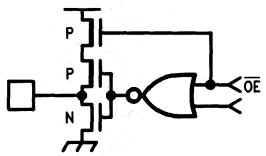
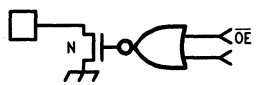
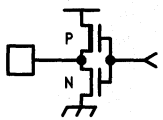
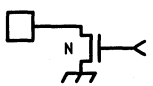
The MB88313 TVDC is an external synchronization type programmable character display controller. Under control of a 4 or 8-bit general microprocessor, it displays 16 characters of 32-character set with various character attributes (color and blink) and screen features (screen format, character size, and display position) on a standard monochrome or color TV screen, superimposed on the picture. The MB88313 can interface to NTSC, PAL and SECAM standard color TV set, and also to the raster scan type CRT, regardless of interlace or noninterlace scan.

The MB88313 has three operation modes; the active mode, standby mode and reset mode. The active mode operations are described on pages 10–16. Both Standby mode operations, and Reset mode operations are described starting on page 17.

*Active Operations*

Character & attribute codes and feature control codes are written into the on-chip display memory and control registers by the processor using control commands, respectively. The control commands are serially loaded into the on-chip command register through the processor interface pins, $\overline{\text{CS}}$, SCLK, and SI. According to the programmed character & attribute codes and control codes, the MB88313 issues the character & background video signals from the VOC and $\overline{\text{VOB}}$ pins synchronously with $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$, signals provided by the TV set. Also, the DO2–DO0 outputs are used as color control or other general control signals to the TV set.

**INPUT/OUTPUT CIRCUITS**

| TYPE | PIN | MB88306/308 | MB88307/309 |
|---|---|---|---|
| INPUTS | $\overline{\text{LOAD}}$<br>SC ($\overline{\text{SC}}$)<br>$\overline{\text{RESET}}$ | HYSTERESIS INPUT  | HYSTERESIS INPUT  |
| | $\overline{\text{OE}}$<br>SI | NON-HYSTERESIS INPUT  | NON-HYSTERESIS INPUT  |
| OUTPUTS | $O_7 - O_0$ | CMOS 3-STATE OUTPUT   | NMOS OPEN-DRAIN OUTPUT   |
| | SO | CMOS OUTPUT   | NMOS OPEN-DRAIN OUTPUT   |

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**FUNCTIONAL DESCRIPTION** (Continued)

### Command Load Operation

The processor serially loads 8-bit commands into the TVDC's command shift register using the processor inputs, $\overline{CS}$, SCLK and SI. The loaded command is parallel latched into the command register. According to the command, control data is written into a designated memory location, address counter, or control register.

Figures 10 and 11 show the command register configuration and command load timing: A low level on the $\overline{CS}$ pin initializes the SCLK counter and enables the command shift register to receive command words. Then, synchronously with the SCLK shift clock input, an 8-bit command word is serially loaded into the command shift register through the SI input pin. At the rising edge of SCLK, a command bit on the SI pin is shifted into the MSB of the command shift register and at the same time the command shift register bits are right shifted. The rising edge of SCLK is counted by the SCLK counter, and at the eighth rising edge, the 8-bit command word is latched into the command register, where the first-in bit is the LSB and the last-in bit is the MSB. After that, the command is decoded to generate internal control signals.

**Note:**

In successive command loading a few hundred ns after completion of one command loading, the next loading should not be made.

### Display Operations

According to programmed display memory and control registers, the MB88313 issues video signals, VOC and $\overline{VOB}$ for character patterns synchronously with $\overline{HSYNC}$ and $\overline{VSYNC}$ signals supplied by the TV set, and also outputs feature control signals on the DO2–DO0 pins.

**Figure 10. Command Register Configuration**

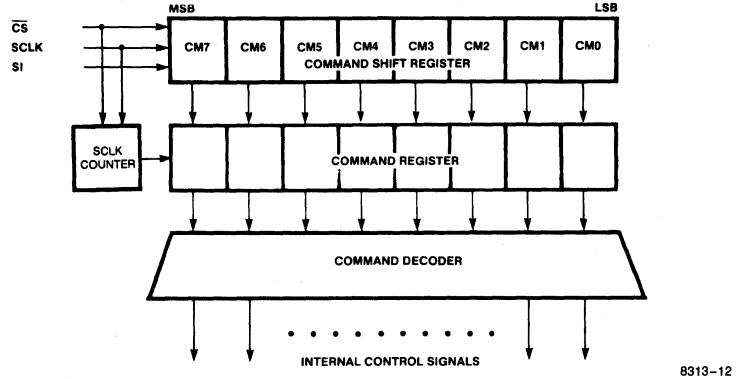
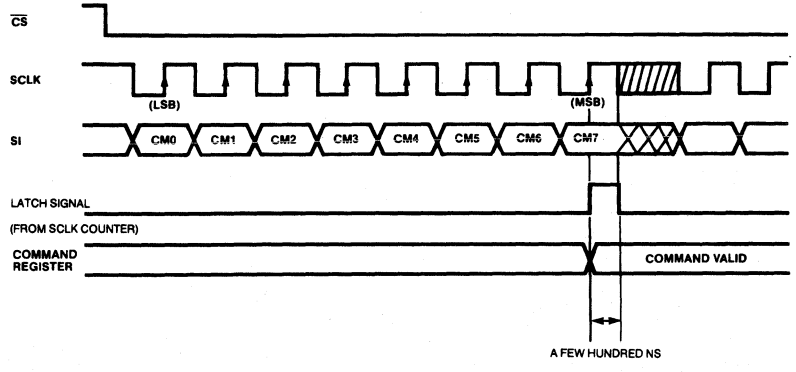



**Figure 11. Command Load Timing**



**FUNCTIONAL DESCRIPTION** (Continued)

*Screen Format Control*

The MB88313 can display 16 characters in the format of 16 characters x 1 line (with one-dot horizontal spacing) or 8 characters x 2 lines (with one-dot horizontal & two-dot vertical spacings) on the TV screen. Either format can be selected by controlling the SC3 bit using Command 5: SC3 = "1" for 16 characters x 1 line, and SC3 = "0" for 8 characters x 2 lines. Figure 12 shows the two screen formats.

*Character Format and Automatic Rounding Function*

The character patterns are formatted as 5 x 7 dot matrix, stored in the on-chip character generator mask ROM. Figure 13 shows the character format. But, on the actual TV screen, this format is modified by the automatic rounding function. See Figure 14-1: When the internal original dot pattern (i.e., raw output signal from the character generator) contains diagonally aligned dots, a dot is automatically inserted between every diagonal dot to smooth the character form. Figure 14-2 shows an example of this rounding function.

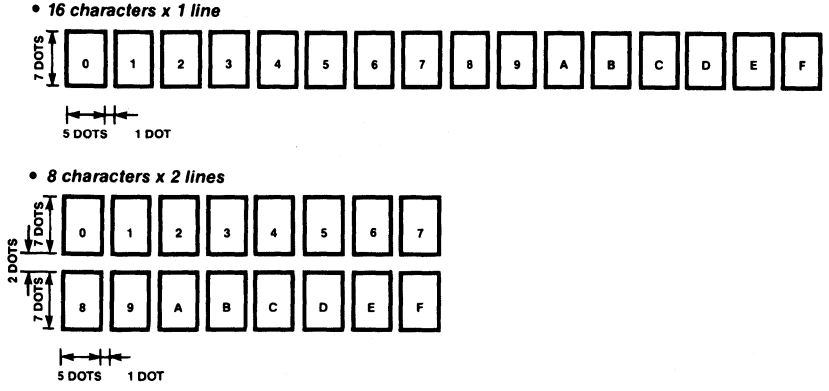
*Character Patterns and Codes*

The MB88313 has a character set of 32 character patterns, which is defined by the on-chip character generator mask ROM. Figure 15 shows the standard character set. Each character pattern is encoded as shown in Table 5. The MB88313 can also have user-designed character set (except blank and background) by programming the mask ROM.

*Display Mode Control (Character/Background Control)*

One of four display modes can be selected by the five screen control bits SC4–SC0 using Command 5, as shown in Table 4. Figure 16 shows examples of the display states, as well as the VOC and $\overline{VOB}$ output timing signals on line AA' for character codes of 1, 2, blank, background, 3, and 4 in the three display modes, except the non-display mode.

**Figure 12. Screen Format**




**Note:**
Each box represents one character display area (5 x 7 dots). The hexadecimals represent display memory addresses.

**Table 4. Display Mode Control**

| Screen Control Bits | | | | | Display Modes |
|---|---|---|---|---|---|
| SC4 | SC3 | SC2 | SC1 | SC0 | |
| X | X | X | X | 0 | Non Display Mode: No characters nor background are displayed |
| X | 0 | X | 0 | 1 | Non-Background/Edge Mode: Characters are displayed, nor background |
| X | 0 | 0 | 1 | 1 | Edge Mode: Edged characters are displayed |
| X | 0 | 1 | 1 | 1 | Background Mode: Characters with black background are displayed |

**FUNCTIONAL DESCRIPTION** (Continued)

*Display Start Position Control*

The horizontal and vertical display start positions on the TV screen are defined by the horizontal and vertical display position registers. Programming these control registers using Commands 2 and 4, the display start position (HP, VP) can be determined. For the horizontal position, 29 selections, and for the vertical position, 31 selections are possible. Figure 17 shows the definition of the display start position.

The horizontal display start position HP (from the rising edge of $\overline{HSYNC}$ to the falling edge of $\overline{VOB}$) and the vertical display start position VP (from the rising edge of $\overline{VSYNC}$ to the falling edge of $\overline{VOB}$) are calculated from programmed values of HP5 to HP0 and VP5 to VP0 using the following equations:

$$HP = T \times 4 \times [(2^5 \times HP5 + 2^4 \times HP4 + 2^3 \times HP3 + 2^2 \times HP2 + 2 \times HP1 + HP0) + P]$$

$$VP = H \times 4 \times (2^5 \times VP5 + 2^4 \times VP4 + 2^3 \times VP3 + 2^2 \times VP2 + 2 \times VP1 + VP0)$$

Where: P = 9, 10, 11, 12 for (HS1, HS0) = (0,0), (0,1), (1,0), and (1,1) respectively
T = Clock (oscillation) cycle time [7 MHz max.]
H = Horizontal sync cycle time [63.5 $\mu$s typ.]

*Character Size Control*

The character width and height on the TV screen are defined by the horizontal and vertical character size registers. Programming these control registers using Command 4, the character size can be determined. As shown in Tables 6 and 7, 4 selections are possible for each of the horizontal and vertical sizes.

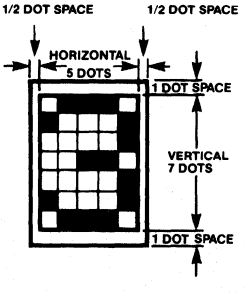
*Blink Control*

The MB88313 can blink any desired character(s) on the TV screen. Blinking function is enabled when the SC4 bit of the screen control register is set to "1". Blinking effects only those characters for which the AC2 bit (blink control bit) is set to "1". Blinking characters appear for approximately 0.5s and disappear for the same period (vertical sync pulse cycle time × 64).

Blinking can be set as follows:

1. Preset a display memory address where the character blink is required, using Command 1.
2. Set the AC2 bit (blink control bit) of the location of the address, using Command 6.
3. Set the SC4 bit (blink enable bit) of the screen control register, using Command 5.

**Figure 13. Character Format**




**Note:**
Each box presents one dot, and hatched boxes indicate displayed dots.

**Figure 14-1. Automatic Rounding Function (Algorithm)**

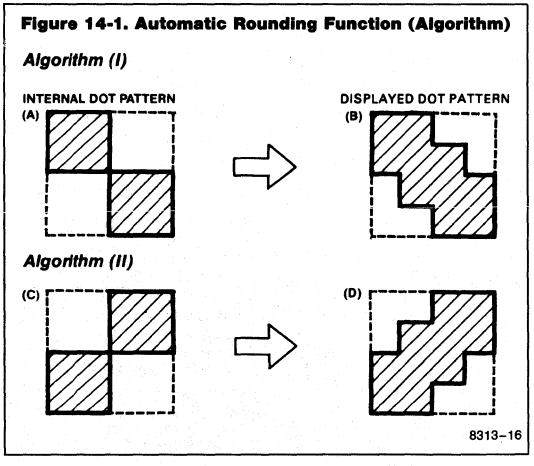
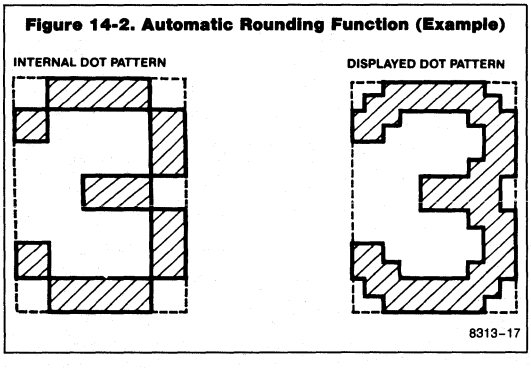
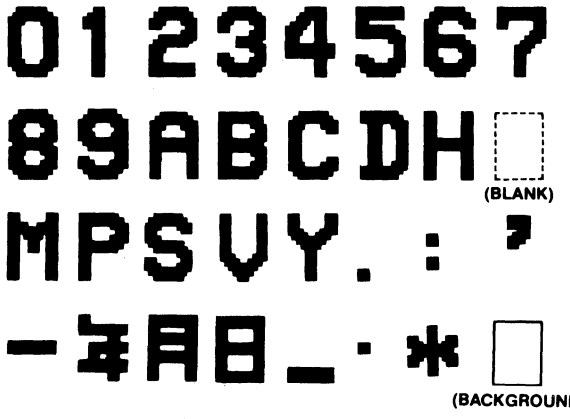



**Figure 14-2. Automatic Rounding Function (Example)**



**FUNCTIONAL DESCRIPTION** (Continued)

**Figure 15. Standard Character Set (Character Patterns)**




8313-18

**Table 5. Standard Character Codes**

| CH4 / CJ3-CH0 | 0 | 1 |
|---|---|---|
| 0 | 0 | M |
| 1 | 1 | P |
| 2 | 2 | S |
| 3 | 3 | V |
| 4 | 4 | Y |
| 5 | 5 | . (Period) |
| 6 | 6 | : (Colon) |
| 7 | 7 | ' (Apostrophe) |
| 8 | 8 | - (Hyphen) |
| 9 | 9 | 年 Kanji (Year) |
| A | A | 月 Kanji (Month) |
| B | B | 日 Kanji (Day) |
| C | C | _ (Underline) |
| D | D | • (Dot) |
| E | H | * (Asterisk) |
| F | ▨ (Blank) | □ (Background) |

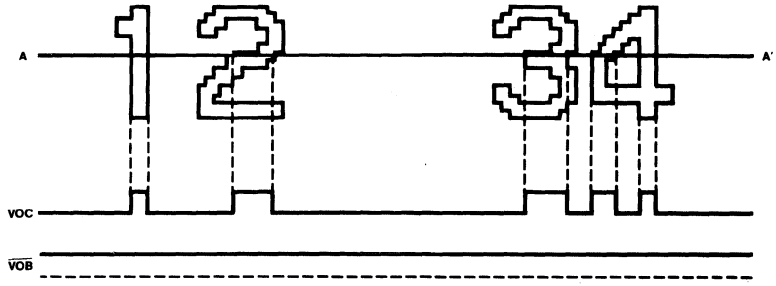
8313-19

4

**FUNCTIONAL DESCRIPTION** (Continued)

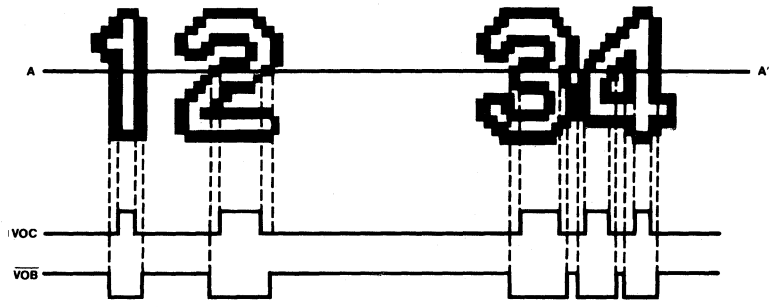
**Figure 16. Display Modes and VOC & $\overline{VOB}$ Output Timing**

*Non-Background/Edge Mode*



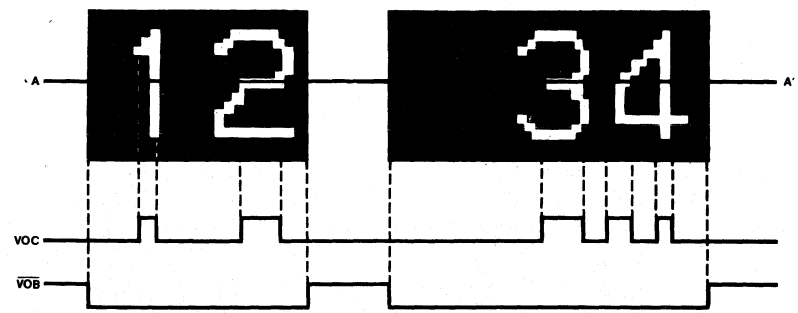

8313-20

*Edge Mode*




8313-21

*Background Mode*




8313-22

**Note:**
During the non-display mode, the VOC and $\overline{VOB}$ outputs are clamped low and high, respectively, disabling display on TV screen.

**FUNCTIONAL DESCRIPTION** (Continued)

**Figure 17. Display Start Position**

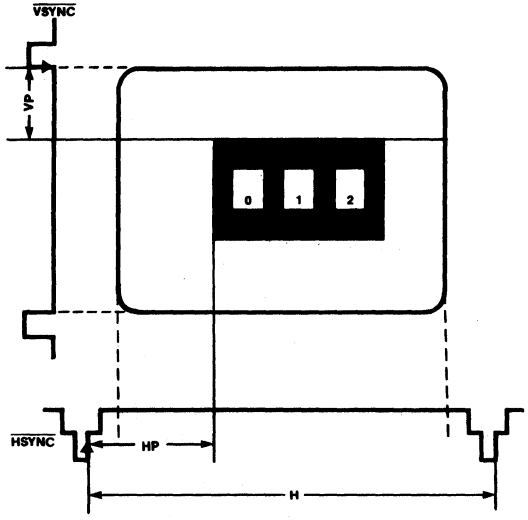



**Table 6. Horizontal Character Size**

| Horizontal Size Code | | Horizontal Character Size (Width) | Horizontal Dot Size |
|---|---|---|---|
| HS1 | HS0 | | |
| 0 | 0 | 10T | 2T |
| 0 | 1 | 20T | 4T |
| 1 | 0 | 30T | 6T |
| 1 | 1 | 40T | 8T |

**Note:**
T: Clock cycle time
T [s] = 1/fc [Hz]

**Table 7. Vertical Character Size**

| Vertical Size Code | | Vertical Character Size (Height) | Vertical Dot Size |
|---|---|---|---|
| VS1 | VS0 | | |
| 0 | 0 | 14H | 2H |
| 0 | 1 | 28H | 4H |
| 1 | 0 | 42H | 6H |
| 1 | 1 | 56H | 8H |

**Note:**
H: Horizontal sync cycle time
H = 63.5 [μs]

**Functional Description** (Continued)

*Color Control*

The MB88313 has a color display mode, in which color control signals are output on the DO1 and DO0 pins, in addition to the VOC and $\overline{VOB}$ signals. The color display mode is initiated by setting the GOC bit to "1" using Command 7. During this mode, the color code bits AC1 and AC0 stored in each attribute field of the display memory are automatically output on the DO1 and DO0 pins respectively, while the VOC output is high. When the VOC is low, the color control signals are clamped low. Controlling RGB signals of the color TV set by the VOC, DO1 and DO0 signals, characters are displayed in four of eight colors shown in Table 8. One of four colors is selected for each character by writing color codes to each attribute field of the display memory. Four colors to be displayed are selected by a combination of connections between MB88313's VOC/DO1/DO0 and TV's RGB pins.

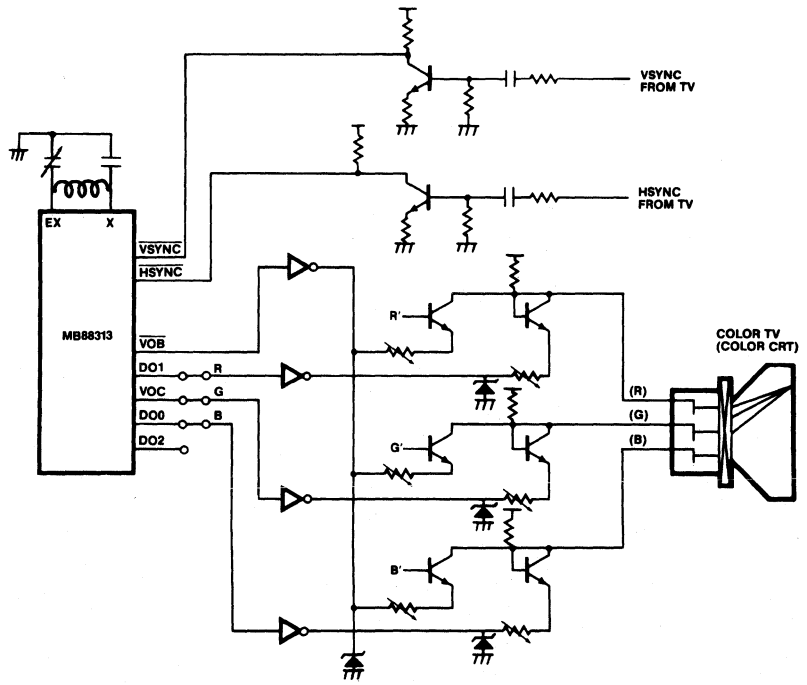
Figure 18 shows an example circuit for selecting character colors: green, cyanogen, yellow and white.

In this example circuit, the $\overline{VOB}$ (background) signal is used to inhibit all TV color video signals R'G'B' simultaneously. When the $\overline{VOB}$ is low, the R'G'B' signals are all disabled to create a black background. When the $\overline{VOB}$ is high, the R'G'B' signals are enabled to display TV signal. The VOC (character) signal and the DO1 & DO0 (i.e., AC1 & AC0) color code outputs are used to enable color character signals R, G, B, respectively, RGB and R'G'B' signals control (R)(G)(B) signals of the CRT in parallel.

**Table 8. Displayable Colors**

| R | G | B | Displayed Colors |
|---|---|---|---|
| 0 | 0 | 0 | Black |
| 0 | 0 | 1 | Blue |
| 0 | 1 | 0 | Green |
| 0 | 1 | 1 | Cyanogen |
| 1 | 0 | 0 | Red |
| 1 | 0 | 1 | Magenta |
| 1 | 1 | 0 | Yellow |
| 1 | 1 | 1 | White |

**Figure 18. TV Interface Configuration (Example)**




**Note:**
R'G'B' are TV RGB signals.

**FUNCTIONAL DESCRIPTION** (Continued)

**Table 9. Color Control (in Color Display Mode: GOC = "1")**

| Video Signals | | Color Control Codes | | |
|---|---|---|---|---|
| $\overline{VOB}$ | VOC (G) | AC1 = DO1 (R) | AC0 = DO0 (B) | Displayed Colors |
| X | 1 | 0 | 0 | Green (RB: disabled) |
| | | 0 | 1 | Cyanogen (R: disabled) |
| | | 1 | 0 | Yellow (B: disabled) |
| | | 1 | 1 | White (RGB: enabled) |
| 1 | 0 | 0 | 0 | Blank (RGB: disabled, R'G'B': enabled) |
| 0 | | 0 | 0 | Black (Background) (RGB and R'G'B': disabled) |

**Standby Operation**

The MB88313 has a low power standby mode (i.e., clock stop mode) which is initiated by software. A logic "1" on the STP bit stops the on-chip clock generator, reducing the power dissipation, and sets the internal states and input/output pin states, as follows:

1. All internal control registers, display memory, address counter, and command shift & command registers keep their current states.
2. All input pins are inactive.
3. Output pins hold the states before the standby mode.

During the standby mode, characters disappear on the TV screen.

When the STP bit is reset to "0", the clock generator restarts, and characters reappear on the screen. The STP is controlled by Command 6.

**Notes:**

1. When the STP bit is reset and the clock generator restarts, the vertical display position of each character is disturbed in the first screen field. To avoid this problem, the following procedure is recommended when resetting the STP bit:
   1) Before resetting, disable the screen display, resetting the SC0 bit with Command 5.
   2) Reset the STP bit using Command 6.
   3) At least 16.7 ms after resetting the STP bit, set the SC0 bit, enabling the screen display.
2. When set/reset the STP bit using Command 6, the AC2–AC0 bits addressed by the current address counter may change also.

**Reset Operation**

A low level on the $\overline{RESET}$ pin stops the TVDC's operations, and initializes its internal control registers and input/output pins to the following states:

1. All internal control registers are cleared.
2. All input pins are inactive.
3. VOC and DO2–DO1 output pins are clamped low, and $\overline{VOB}$, clamped high.

The display memory data is not affected by $\overline{RESET}$. The command shift register, command register, and address counter are undefined after $\overline{RESET}$.

During the reset mode, characters are not displayed on the TV screen because the output pins are deactivated as mentioned in item 3 above.

After the $\overline{RESET}$ pin is driven high, the TVDC restarts its normal operations. But, VOC, $\overline{VOB}$, and DO2–DO1 outputs remain deactivated, that is, no character is displayed on the TV screen, until the SC0 screen enable bit is set in the screen control register.

4

## COMMAND DESCRIPTION

### Command Set

The MB88313's display memory, address counter, and control registers are programmed using control commands. The MB88313 can accept eight 8-bit display control commands. These commands are serially loaded into the command register by the processor, and write their operand field data (control codes) into the display memory, address counter, and control registers. According to the programmed registers and memory, the MB88313 displays characters on the TV screen. The command format and functions are shown in Table 10. The upper 3 bits define op code, and the lower 5 bits are operand (control code).

### Command 0 (Character Code Set)

Command 0 writes its lower 5 bits (character code: CH4–CH0) into character code field of a display memory location indicated by the address counter, and then increments the address counter. For the command format, see Table 6.

### Command 1 (Address Preset)

Command 1 writes the lower 4 bits (display memory address: A3–A0) into the address counter, which addresses a display memory location into which Commands 0 and 6 write character and attribute codes. For the command format, see Table 10.

**Note:**
Bit 4 should be "0".

### Command 2 (Horizontal Display Position Control)

Command 2 writes its lower 5 bits (horizontal display position code: HP4–HP0) into the horizontal display position register. Values of (00000) to (00010) can not be used as HP4–HP0. For the command format, see Table 10.

### Command 3 (Vertical Display Position Control)

Command 3 writes its lower 5 bits (vertical display position code: VP4–VP0) into the vertical display position register. For the command format, see Table 10.

### Command 4 (Character Size Control)

Command 4 writes its lower 2 bits (horizontal character size code: HS1 and HS0) and the next 2 bits (vertical character size code: VS1 and VS0) into the horizontal character size register and the vertical character size register, respectively. For the command format, see Table 10.

**Note:**
Bit 4 should be "0".

### Command 5 (Screen Control)

Command 5 writes its lower 5 bits (screen control bits: SC4–SC0) into the screen control register to control various screen features. For the command format, see Table 10.

### Command 6 (Attribute Control)

Command 6 writes its lower 3 bits (attribute codes: AC2 and AC1–AC0) into the attribute field of a display memory location indicated by the address counter. Note that this command does not increment the address counter, differently from Command 0. This command sets/resets Bit 4 to initiate/release the standby mode (clock stop mode). Bit 3 should be "0". For the command format, see Table 10.

### Command 7 (General Output Control)

Command 7 writes its lower 3 bits (general output data: GO2–GO0) into the general output register, and sets/resets Bit 4 (general output control bit: GOC). For the command format, see Table 10.

## NOTICE

1. The test mode is initiated by test mode command (code = 00111XXX), and is released by a low level on the $\overline{\text{HSYNC}}$ pin. In the test mode, output operations of the VOC, $\overline{\text{VOB}}$ and DO2–DO1 pins are different from in the normal operation mode.
2. The MB88313 may enter the test mode when a control command, which is wrongly transferred due to noises, matches the test mode command.
3. When the command transmission from the processor to the MB88313 fails on the way due to noises, the command word must be retransferred after once making $\overline{\text{CS}}$ high and then returning low.

**COMMAND DESCRIPTION** (Continued)

**Table 10. Command Set Summary**

| Command Number | Command Word Format | | | | | | Name & Function |
|---|---|---|---|---|---|---|---|
| | Opecode Field | Operand Field | | | | | |
| | MSB | LSB | | | | | |
| 0 | 0 0 0 | CH4 | CH3 | CH2 | CH1 | CH0 | Character code set: Write operand field data (character code: CH4–CH0) into the character code field of the display memory. |
| 1 | 0 0 1 | 0 | A3 | A2 | A1 | A0 | Address preset: Write operand field data (display memory address: A3–A0) into the address counter to indicate memory locations. |
| 2 | 0 1 0 | HP4 | HP3 | HP2 | HP1 | HP0 | Horizontal display position control: Write operand field data (position code: HP4–HP0) into the horizontal display position register. |
| 3 | 0 1 1 | VP4 | VP3 | VP2 | VP1 | VP0 | Vertical display position control: Write operand field data (position code: VP4–VP0) into the vertical display position register. |
| 4 | 1 0 0 | 0 | VS1 | VS0 | HS1 | HS0 | Character size control: Write operand field data (horizontal & vertical character size codes: HS1 & 0, VS1 & 0) into the horizontal and vertical character size registers. |
| 5 | 1 0 1 | SC4 | SC3 | SC2 | SC1 | SC0 | Screen control: Write operand field data (screen control codes: SC4–SC0) into screen control register. |
| 6 | 1 1 0 | STP | 0 | AC2 | AC1 | AC0 | Attribute control: Write operand field data (clock stop code: STP, attribute codes: AC2–AC0) into the attribute field of the display memory, and the standby mode (clock stop mode) control bit. |
| 7 | 1 1 1 | GOC | 0 | GO2 | GO1 | GO0 | General output control: Write operand field data (GOC, GO2–GO0) into the general output register (GO2–GO0) and its control bit (GOC). |

**ABSOLUTE MAXIMUM RATINGS**†

| Parameter | Symbol | Rating | | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Supply Voltage | $V_{CC}$ | $V_{SS}-0.3$ | | $V_{SS}+7.0$ | V | |
| Input Voltage | $V_{IN}$ | $V_{SS}-0.3$ | | $V_{SS}+7.0$ | V | Should not exceed $V_{CC}+0.3V$ |
| Output Voltage | $V_{OUT}$ | $V_{SS}-0.3$ | | $V_{SS}+7.0$ | V | Should not exceed $V_{CC}+0.3V$ |
| Power Dissipation | $P_D$ | | | 600 | mW | |
| Operating Ambient Temperature | $T_A$ | −30 | | +70 | °C | |
| Storage Temperature | $T_{STG}$ | −55 | | +150 | °C | |

†Permanent device damage may occur if the above ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

4

## RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Supply Voltage | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V | $V_{CC}$ |
| | $V_{SS}$ | | 0 | | V | |
| Input High Voltage | $V_{IH}$ | $0.8 \times V_{CC}$ | | $V_{CC}+0.3$ | V | $\overline{RESET}$, $\overline{CS}$, SCLK, SI $\overline{HSYNC}$, $\overline{VSYNC}$ |
| Input Low Voltage | $V_{IL}$ | $V_{SS}-0.3$ | | $0.2 \times V_{CC}$ | V | $\overline{RESET}$, $\overline{CS}$, SCLK, SI $\overline{HSYNC}$, $\overline{VSYNC}$ |
| Operating Ambient Temperature | $T_A$ | −30 | | 70 | °C | |

## DC CHARACTERISTICS

(Recommended operating conditions, unless otherwise noted.)

| Parameter | Symbol | Pin | Condition | Value | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| Output High Voltage | $V_{OH}$ | DO2–DO0, VOC, $\overline{VOB}$ | $V_{CC}$ = 4.5V $I_{OH}$ = −200 μA | 2.4 | | | V |
| | | | $V_{CC}$ = 4.5V $I_{OH}$ = −10 μA | 4.0 | | | V |
| Output Low Voltage | $V_{OL}$ | DO2–DO0, VOC, $\overline{VOB}$ | $V_{CC}$ = 4.5V $I_{OL}$ = 1.8 mA | | | 0.4 | V |
| | | | $V_{CC}$ = 4.5V $I_{OL}$ = 3.2 mA | | | 0.6 | V |
| Input Leakage Current | $I_{IL}$ | $\overline{RESET}$ | $V_{CC}$ = 5.5V $V_{IL}$ = 0.4V | | −20 | −60 | μA |
| | | $\overline{CS}$, SCLK, SI $\overline{HSYNC}$, $\overline{VSYNC}$ | $V_{CC}$ = 5.5V $V_{IL}$ = 0.4V | | −20 | −60 | μA |
| | | EX | $V_{CC}$ = 5.5V $V_{IL}$ = 0.4V | | −10 | −20 | μA |
| Supply Current | $I_{CC}$ | $V_{CC}$ | $V_{CC}$ = 5.0V (Typ.) fc = 6 MHz (Active) Reset state All outputs open | | 8.0 | | mA |

## AC CHARACTERISTICS
(Recommended operating conditions, unless otherwise noted.)

### Clock Timing

| Parameter | Symbol | Pin/Port | Condition | Value | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| Clock Frequency | $f_C$ | EX, X | RC-network OSC, LC-network OSC Figure 19 | 4.0 | | 7.0 | MHz |

### Input Timing

| Parameter | Symbol | Pin | Condition | Value | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min. | Max. | |
| Shift Clock Pulse Width | $t_{WCH}$ | SCLK | Figure 20 | 300 | | ns |
| | $t_{WCL}$ | | | 300 | | |
| Shift Clock Rise/Fall Times | $t_{cr}$ | SCLK | Figure 20 | | 200 | ns |
| | $t_{cf}$ | | | | 200 | |
| Shift Clock Cycle Time | $t_{CYC}$ | SCLK | Figure 20 | 1000 | | ns |
| Shift Clock Start Time | $t_{SS}$ | SCLK | Figure 20 | 200 | | ns |
| Shift Clock Hold Time | $t_{HS}$ | SCLK | Figure 20 | 1000 | | ns |
| Input Data Setup Time | $t_{SU}$ | SI | Figure 20 | 200 | | ns |
| Input Data Hold Time | $t_H$ | SI | Figure 20 | 50 | | ns |
| Chip Select End Time | $t_{EC}$ | $\overline{CS}$ | Figure 20 | 1000 | | ns |
| Chip Select Rise/Fall Times | $t_{crc}$ | $\overline{CS}$ | Figure 20 | | 200 | ns |
| | $t_{cfc}$ | | | | | |
| Horizontal Sync Valid Time | $t_{HSDF}$[1] | $\overline{HSYNC}$ | Figure 21 | 200 | | ns |
| | $t_{HSDR}$[2] | | | 200 | | |

**Notes:**
1. The rising edge of $\overline{HSYNC}$ is not counted during $t_{HSDF}$ period to calculate the vertical display position.
2. The rising edge of $\overline{HSYNC}$ is counted during $t_{HSDR}$ period to calculate the vertical display position.

### Output Timing

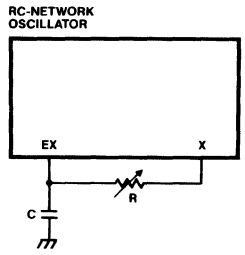
| Parameter | Symbol | Pin | Condition | Value | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min. | Max. | |
| General Output Delay Time | $t_{DD}$ | DO2–DO0 | 5 kΩ External Pull-Up Figure 22 | | 600 | ns |

4

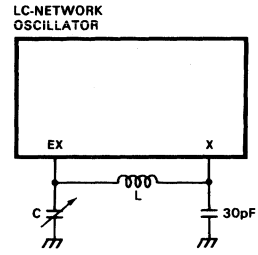
## AC CHARACTERISTICS

(Recommended operating conditions, unless otherwise noted.) (Continued)

**Figure 19. Clock Circuit Configurations**

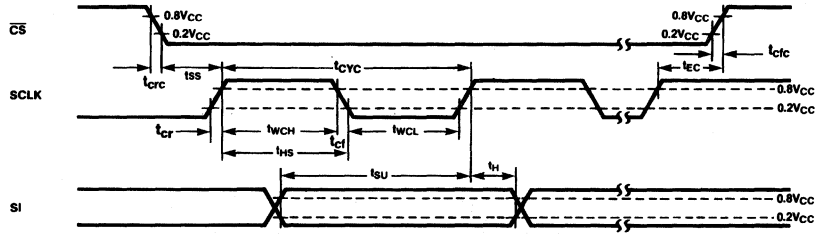



8313-25



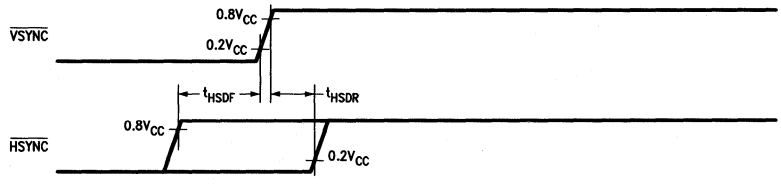

8313-26

**Figure 20. Input Timing (Processor Interface)**



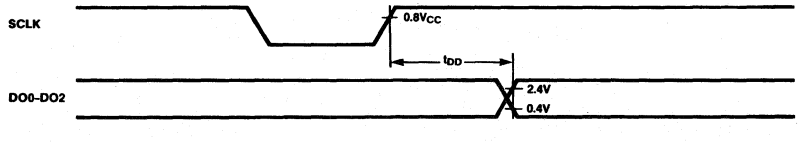

8313-27

**Figure 21. Input Timing (Television Interface)**




8313-29

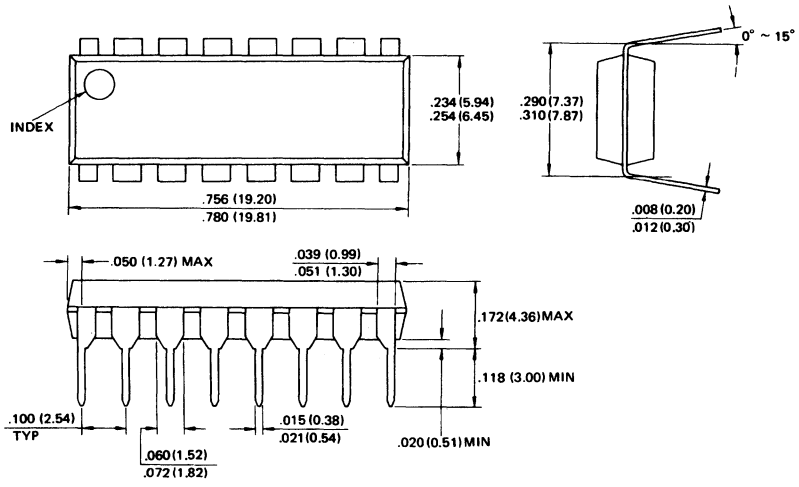
**Figure 22. Output Timing**




8313-28

## PACKAGE DIMENSIONS

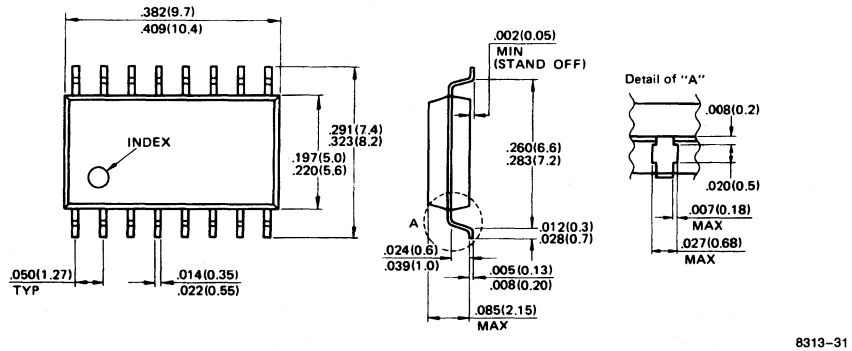
**16-LEAD PLASTIC**
**DUAL IN-LINE PACKAGE**
**DIP-16P-M02**




8313-30

Dimensions in inches (millimeters)

**16-LEAD PLASTIC**
**FLAT PACKAGE**
**FPT-16P-M02**




8313-31

Dimensions in inches (millimeters)