

8-bit Proprietary Microcontroller

CMOS

F²MC-8L MB89120/120A Series

MB89121/P131/123A/P133A/125A/P135A/ MB89PV130A

■ DESCRIPTION

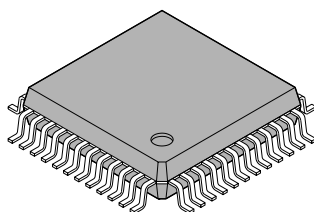
The MB89120 series is a line of single-chip microcontrollers containing a compact instruction set and a great variety of peripheral functions such as a timer, serial interface, and external interrupt. The MB89120A series is an extended variant of the MB89120, with a remote control transmission function and wake-up interrupt channels.

■ FEATURES

- F²MC-8L family CPU core
- Low-voltage operation
- Low current consumption (allowing for dual clock)
- Minimum execution time : 0.95 μ s at 4.2 MHz
- 21-bit timebase counter
- I/O ports : Max. 36 ports
- External interrupts : 3 channels
- External interrupts (wake-up function) : 8 channels (only in the MB89120A series)
- 8-bit serial I/O : 1 channel
- 8-/16-bit timer/counter : 1 channel
- Built-in remote-control transmitting frequency generator (only in the MB89120A series)
- Low-power consumption modes (stop mode, sleep mode, watch mode)
- Package : QFP-48
- CMOS technology

■ PACKAGE

48-pin plastic QFP



(FPT-48P-M13)

MB89120/120A Series

■ PRODUCT LINEUP

| Part number Item | MB89121 | MB89123A | MB89125A | MB89P133A | MB89P131 |
|---|--|--|--------------------------------------|--|--|
| Classification | Mass-produced products (Mask ROM products) | | | One-time products | |
| ROM size | 4 K × 8 bits (internal mask ROM) | 8 K × 8 bits (internal mask ROM) | 16 K × 8 bits (internal mask ROM) | 8 K × 8 bits (Internal PROM to be programmed with a general-purpose EPROM programmer) | 4 K × 8 bits (Internal PROM to be programmed with a general-purpose EPROM programmer) |
| RAM size | 128 × 8 bits | 256 × 8 bits | | | 128 × 8 bits |
| CPU functions | The number of instructions : 136 Instruction bit length : 8 bits Instruction length : 1 to 3 bytes Data bit length : 1, 8, 16 bits Minimum execution time : 0.95 μs at 4.2 MHz Minimum interrupt processing time : 8.57 μs at 4.2 MHz | | | | |
| Ports | Output ports (N-ch open-drain) : 4 (All also serves as peripherals.) Output ports (CMOS) : 8 I/O ports (CMOS) : 24 (8 ports also serve as peripherals.) Total : 36 | | | | |
| Timer/counter | 8-bit timer/counter × 2 channels or 16-bit event counter × 1 channel | | | | |
| Serial I/O | 8 bits LSB/MSB first selectable | | | | |
| External interrupt 1 | 3 Independent channels (edge selection, interrupt vector, source flag) Rising edge/falling edge/both edges selectable Also for wake-up from stop/sleep mode (edge detection is also permitted in stop mode) | | | | |
| External interrupt 2 (wake-up function) | — | 8 channels (only for level detection) | | | — |
| Remote control transmitting frequency generator | — | 1 channel (pulse width and frequency selectable by program) | | | — |
| Standby mode | Sleep mode, stop mode, watch mode | | | | |
| Process | CMOS | | | | |
| Operating voltage* | 2.2 V to 4.0 V (with the dual clock option) 2.2 V to 6.0 V (with the single clock option) | | | 2.7 V to 6.0 V | |
| EPROM for use | — | | | | |

* : Varies with conditions such as operating frequencies. (See "■ ELECTRICAL CHARACTERISTICS".)

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MB89120/120A Series

(Continued)

| Part number Item | MB89P135A | MB89PV130A |
|---|--|---------------------------------|
| Classification | One-time PROM products | Piggyback/evaluation product |
| ROM size | 16 K × 8 bits (internal PROM, to be programmed with general-purpose EPROM programmer) | 32 K × 8 bits (external ROM) |
| RAM size | 512 × 8 bits | 1 K × 8 bits |
| CPU functions | The number of instructions : 136 Instruction bit length : 8 bits Instruction length : 1 to 3 bytes Data bit length : 1, 8, 16 bits Minimum execution time : 0.95 μs/4.2 MHz Minimum interrupt processing time : 8.57 μs/4.2 MHz | |
| Ports | Output ports (N-ch open-drain ports) : 4 (All also serve as peripherals.) Output ports (CMOS) : 8 I/O ports (CMOS) : 24 (8 ports also serve as peripherals.) Total : 36 | |
| Timer/counter | 8-bit timer/counter × 2 channels or 16-bit event counter × 1 channel | |
| Serial I/O | 8 bits LSB/MSB first selectable | |
| External interrupt 1 | 3 independent channels (edge selection, interrupt vector, source flag) Rising/falling/both edges selectable Used also for wake-up from stop/sleep mode. (Edge detection is also permitted in stop mode.) | |
| External interrupt 2 (wake-up function) | 8 channels (only for level detection) | |
| Remote control transmitting fre- quency generator | 1 channel (Pulse width and cycle selectable by program) | |
| Standby mode | Sleep mode, stop mode, and clock mode | |
| Process | CMOS | |
| Operating voltage | 2.7 V to 6.0 V | 2.7 V to 6.0 V |
| EPROM for use | — | MBM27C256A-20TVM |

MB89120/120A Series

■ PACKAGE AND CORRESPONDING PRODUCTS

| Package | MB89121 | MB89123A | MB89125A | MB89P133A | MB89P131 |
|-------------|---------|----------|----------|-----------|----------|
| FPT-48P-M13 | ○ | ○ | ○ | ○ | ○ |
| MQP-48C-P01 | × | × | × | × | × |

| Package | MB89P135A | MB89PV130A |
|-------------|-----------|------------|
| FPT-48P-M13 | ○ | × |
| MQP-48C-P01 | × | ○ |

○ : Available, × : Not available

Note : Package details of OTPROM products and piggyback/evaluation products are common to those of MB89130/130A series. Refer to the MB89130/130A series data sheet for details.

■ DIFFERENCES AMONG PRODUCTS

1. Memory Size

Before evaluating using the one-time ROM product, verify its difference from the product that will actually be used. Take particular care on the following points :

- The number of register banks available is different between the MB89121 and the MB89123A/125A/P135A/PV130A.
- The stack area, etc., is set at the upper limit of the RAM.

2. Current Consumption

- When operated at low speed, a product with an OTPROM (EPROM) will consume more current than a product with a mask ROM. However, the same is current consumption in the sleep/stop mode is the same. (For more information, see “■ ELECTRICAL CHARACTERISTICS”.)
- In the case of the MB89PV130A, added is the current consumed by the EPROM which is connected to the top socket.

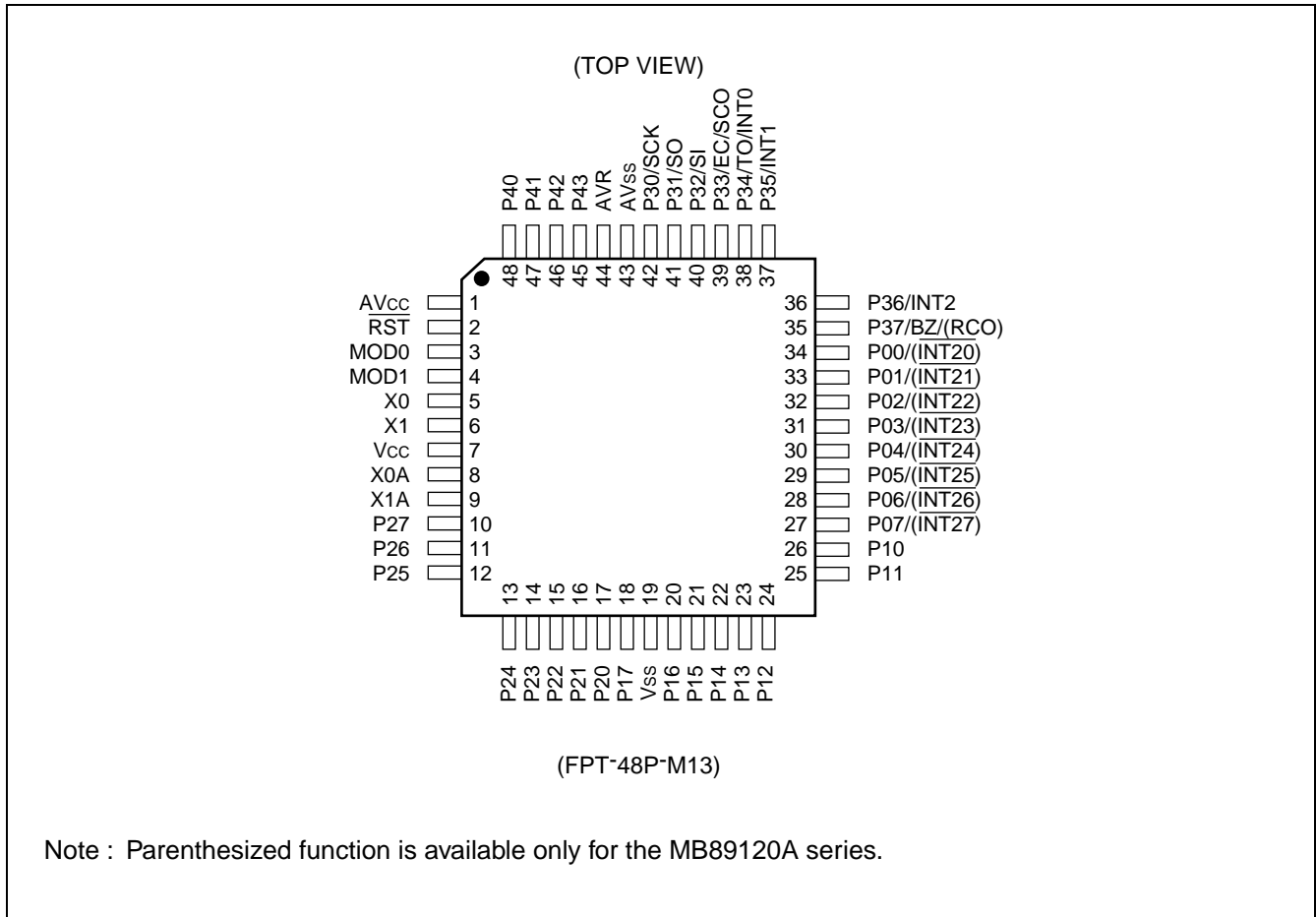
3. Mask Options

Functions that can be selected as options and how to designate these options vary with product. Before using options, check “■ MASK OPTIONS”.

Take particular care on the following point :

- Pull-up resistor can't be set for P40 to P43 on the MB89P135A.
- Options are fixed on the MB89PV130A.

■ PIN ASSIGNMENT



MB89120/120A Series

■ PIN DESCRIPTION

| Pin no. | Pin name | Circuit type | Function |
|--------------|---|--------------|---|
| 5 | X0 | A | Main clock crystal oscillator pins (max. 4.2 MHz) |
| 6 | X1 | | |
| 8 | X0A | B | Subclock crystal oscillator pins (for 32.768 kHz) |
| 9 | X1A | | |
| 3 | MOD0 | C | Operation mode select pins Connect these pins directly to V _{SS} . |
| 4 | MOD1 | | |
| 2 | $\overline{\text{RST}}$ | D | Reset I/O pin This port is of N-ch open-drain output type with pull-up resistor and a hysteresis input type. The internal circuit is initialized by the input of "L". "L" is output from this pin by an internal reset source as optional setting. |
| 27 to 34 | P07/ ($\overline{\text{INT27}}$) to P00/ ($\overline{\text{INT20}}$) | I | General-purpose I/O ports On the MB89120A series, these pins also serve as external interrupt input. External interrupt input is hysteresis input. |
| 18, 20 to 26 | P17 to P10 | E | General-purpose I/O ports |
| 10 to 17 | P27 to P20 | G | General-purpose output-only ports |
| 42 | P30/SCK | F | General-purpose I/O port Also serves as clock I/O for the 8-bit serial I/O interface. This port is of hysteresis input type. |
| 41 | P31/SO | F | General-purpose I/O port Also serves as a serial I/O data output. This port is of hysteresis input type. |
| 40 | P32/SI | F | General-purpose I/O port Also serves as a serial I/O data input. This port is of hysteresis input type. |
| 39 | P33/EC/SCO | F | General-purpose I/O port Also serves as the external clock input for the 8-bit timer/counter. This port is of hysteresis input type. System clock output is optional. |
| 38 | P34/TO/INT0 | F | General-purpose I/O port Also serves as the overflow output and external interrupt input for the 8-bit timer/counter. This port is of hysteresis input type. |
| 36, 37 | P36/INT2, P35/INT1 | F | General-purpose I/O ports Also serve as an external interrupt input. These ports are of hysteresis input type. |
| 35 | P37/BZ/ (RCO) | F | General-purpose I/O port Also serves as a buzzer output. This port is of hysteresis input type. On the MB89120A series, the pin also serves as a remote control output. |

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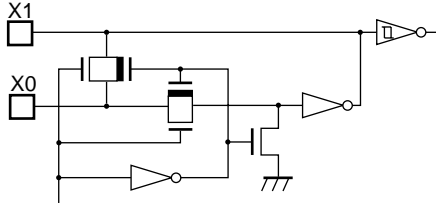
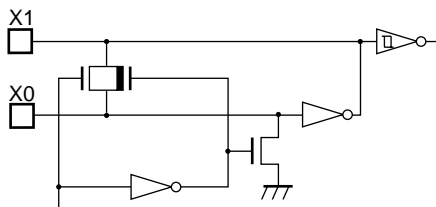
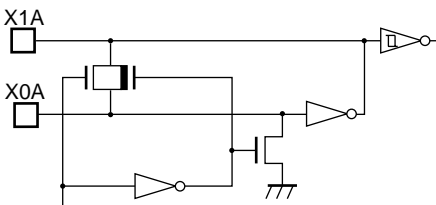
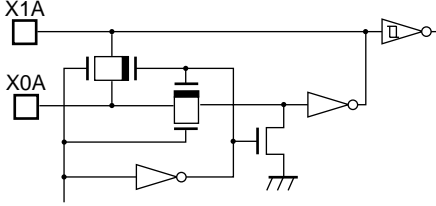
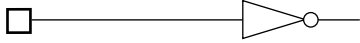
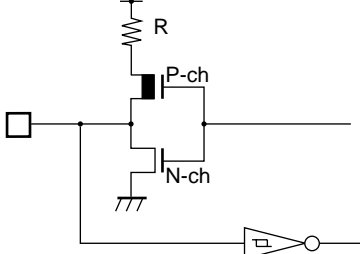
MB89120/120A Series

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| Pin no. | Pin name | Circuit type | Function |
|----------|------------------|--------------|---|
| 45 to 48 | P43 to P40 | H | N-ch open-drain output ports |
| 7 | V _{cc} | — | Power supply pin |
| 19 | V _{ss} | — | Power supply (GND) pin |
| 1 | AV _{cc} | — | Power supply (GND) pin Use this pin at the same voltage as V _{cc} . |
| 44 | AVR | — | Reference voltage input pin |
| 43 | AV _{ss} | — | Power supply (GND) pin Use this pin at the same voltage as V _{ss} . |

MB89120/120A Series

I/O CIRCUIT TYPE

| Type | Circuit | Remarks |
|------|---|--|
| A |  <p>Standby control signal</p> | <ul style="list-style-type: none"> Crystal and ceramic oscillation type (main clock) Circuit for the MB89P133A/P131/P135A/PV130A External clock input select versions of MB89121/123A/125A <p>At an oscillation feedback resistor of approximately 1 MΩ / 5 V</p> |
| |  <p>Standby control signal</p> | <ul style="list-style-type: none"> Crystal and ceramic oscillation type (main clock) Crystal or ceramic oscillator select versions of MB89121/123A/125A <p>At an oscillation feedback resistor of approximately 1 MΩ / 5 V</p> |
| B |  <p>Standby control signal</p> | <ul style="list-style-type: none"> Crystal and ceramic oscillation type (sub clock) <p>Circuit for the MB89121/123A/125A</p> <p>At an oscillation feedback resistor of approximately 4.5 MΩ / 5 V</p> |
| |  <p>Standby control signal</p> | <ul style="list-style-type: none"> Crystal and ceramic oscillation type (sub clock) <p>Circuit for the MB89P131/P133A/P135A/PV130A</p> <p>At an oscillation feedback resistor of approximately 4.5 MΩ / 5 V</p> |
| C |  | |
| D |  | <ul style="list-style-type: none"> Output pull-up resistor (P-ch) of approximately 50 kΩ / 5 V Hysteresis input |

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MB89120/120A Series

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| Type | Circuit | Remarks |
|------|-------------------------------------|---|
| E | | <ul style="list-style-type: none"> • CMOS output • CMOS input • Pull-up resistor optional |
| F | | <ul style="list-style-type: none"> • CMOS output • Hysteresis input • Pull-up resistor optional |
| G | | <ul style="list-style-type: none"> • CMOS output |
| H | | <ul style="list-style-type: none"> • N-ch open-drain output • Pull-up resistor optional |
| I | <p>Only for the MB89120A series</p> | <ul style="list-style-type: none"> • CMOS output • CMOS input • The interrupt input is a hysteresis input (available only on the MB89120A series) . • Pull-up resistor optional |

MB89120/120A Series

■ HANDLING DEVICES

1. Preventing Latchup

Latchup may occur on CMOS ICs if voltage higher than V_{CC} or lower than V_{SS} is applied to input and output pins other than medium- and high- voltage pins, or if higher than the voltage which shows on “1. Absolute Maximum Ratings” in “■ ELECTRICAL CHARACTERISTICS” is applied between V_{CC} and V_{SS} .

When latchup occurs, power supply current increases rapidly, and might thermally damage elements. When using, take great care not to exceed the absolute maximum ratings.

Also, take care to prevent the analog power supply (AV_{CC} and AVR) and analog input from exceeding the digital power supply (V_{CC}) when the analog system power supply is turned on and off.

2. Treatment of Unused Input Pins

Leaving unused input pins open could cause malfunctions. They should be connected to pull-up or pull-down resistor.

3. Treatment of N.C. Pins

Be sure to leave (internally connected) N.C. pins open.

4. Power Supply Voltage Fluctuations

Although operation is assured within the rated range of V_{CC} power supply voltage, a rapid fluctuation of the voltage could cause malfunctions, even if it occurs within the rated range. Stabilizing voltage supplied to the IC is therefore important. As stabilization guidelines, it is recommended to control power so that V_{CC} ripple fluctuations (P-P value) will be less than 10% of the standard V_{CC} value at the commercial frequency (50 to 60 Hz) and the transient fluctuation rate will be less than 0.1 V/ms at the time of a momentary fluctuation such as when power is switched.

5. Precautions when Using an External Clock

When an external clock is used, oscillation stabilization time is required even for power-on reset (optional) and release from stop mode.

6. Turning on the supply voltage (only for the MB89P135A)

When the power supply is turned on if MB89P135A is used, power on sharply up to 2.0 V within 13 clock cycles after starting of oscillation.

Further, various option may be set, if power supply up to keep this condition.

■ PROGRAMMING TO THE EPROM ON THE MB89P131

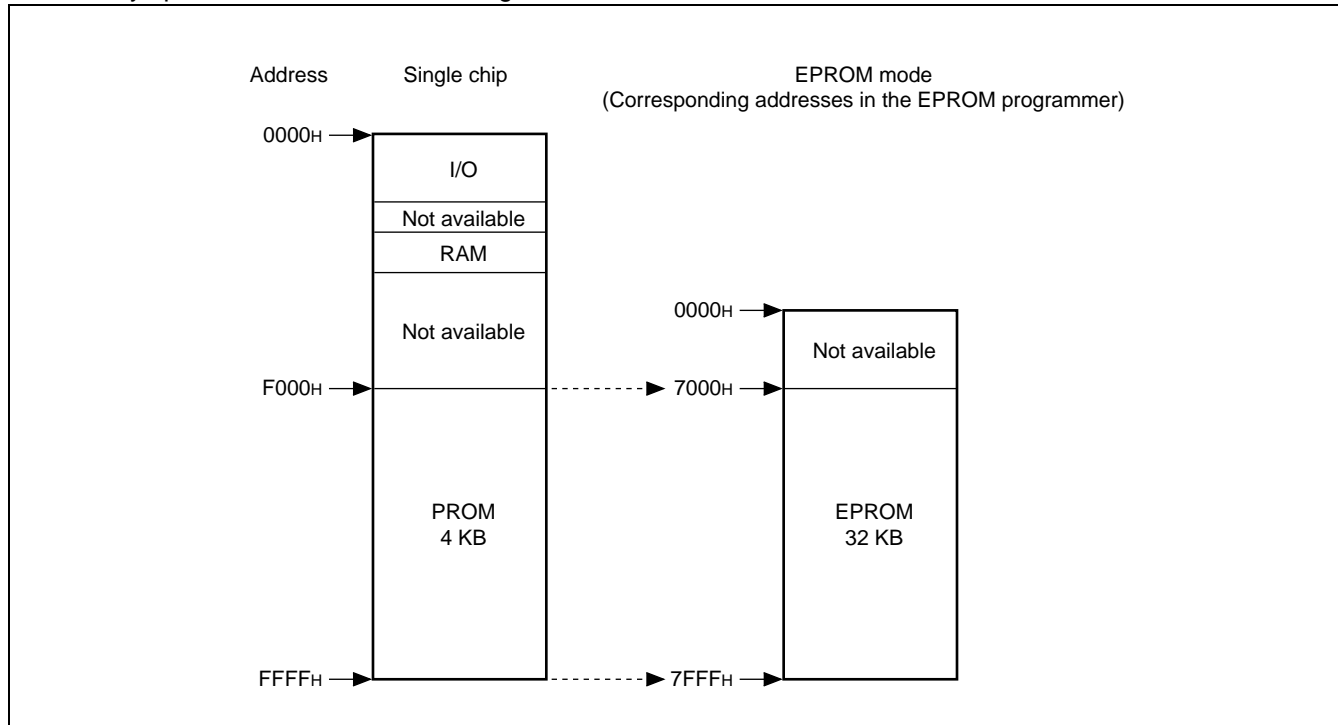
The MB89P131 is a one-time PROM version of the MB89121.

1. Features

- 4-Kbyte PROM on chip
- Equivalency to the MBM27C256A in EPROM mode (when programmed with the EPROM programmer)

2. Memory Space

Memory space in EPROM mode is diagrammed below :



3. Programming to the EPROM

In EPROM mode the MB89P131 functions equivalent to the MBM27C256A. This allows the EPROM to be programmed with a general-purpose EPROM programmer by using the dedicated socket adapter. Note, however, that the electronic signature mode cannot be used.

• Programming procedure

- (1) Set the EPROM programmer to MBM27C256A.
- (2) Load program data into the EPROM programmer at 7000H to 7FFFH (note that addresses F000H to FFFFH while operating as a single chip correspond to 7000H to 7FFFH in EPROM mode) .
- (3) Program with the EPROM programmer.

MB89120/120A Series

■ PROGRAMMING TO THE EPROM ON THE MB89P133A

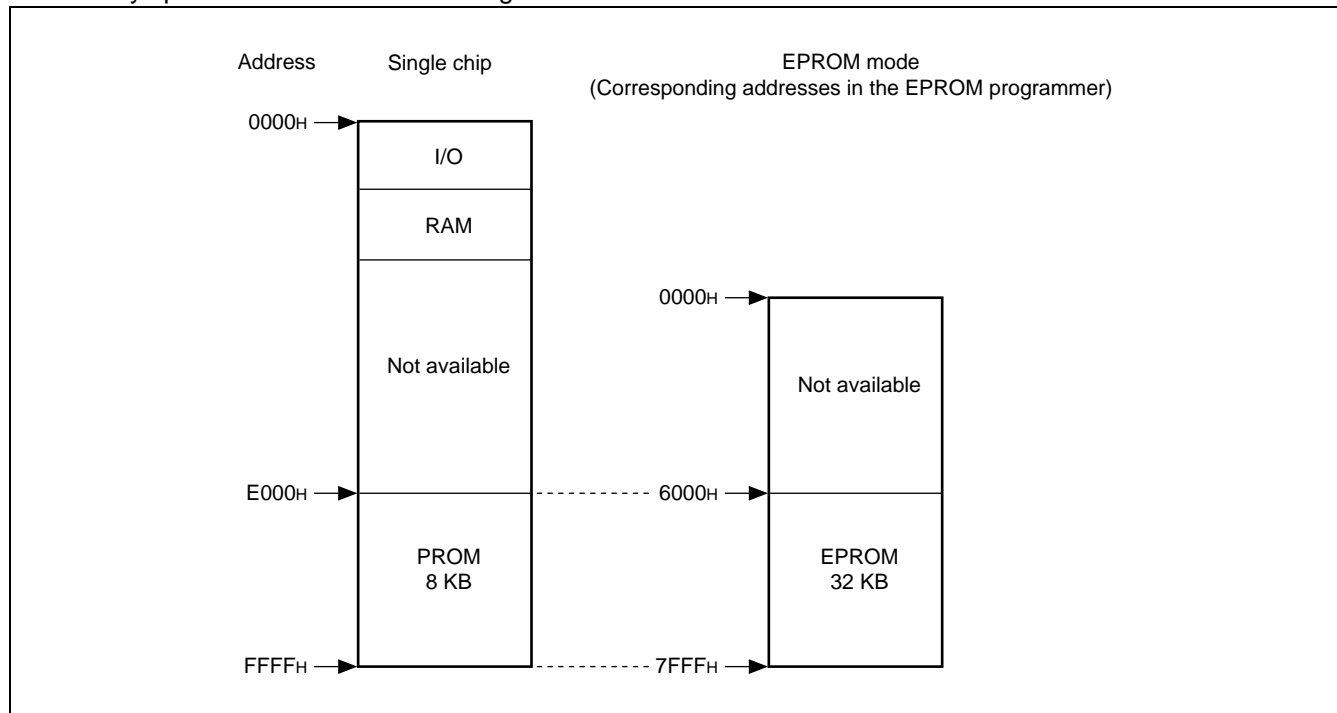
The MB89P133A is a one-time PROM version of the MP89123A.

1. Features

- 8-Kbyte PROM on chip
- Equivalency to the MBM27C256A in EPROM mode (when programmed with the EPROM programmer)

2. Memory Space

Memory space in EPROM mode is diagrammed below :



3. Programming to the EPROM

In EPROM mode the MB89P133A functions equivalent to the MBM27C256A, This allows the EPROM to be programmed with a general-purpose EPROM programmer by using the dedicated socket adapter. Note, however, that the MB89P133A cannot use the electronic signature mode.

• Programming procedure

- (1) Set the EPROM programmer to MBM27C256A.
- (2) Load program data into the EPROM programmer at 6000_H to 7FFF_H (note that addresses E000_H to FFFF_H while operating as a single chip correspond to 6000_H to 7FFF_H in EPROM mode) .
- (3) Program with the EPROM programmer.

■ PROGRAMMING TO THE EPROM ON THE MB89P135A

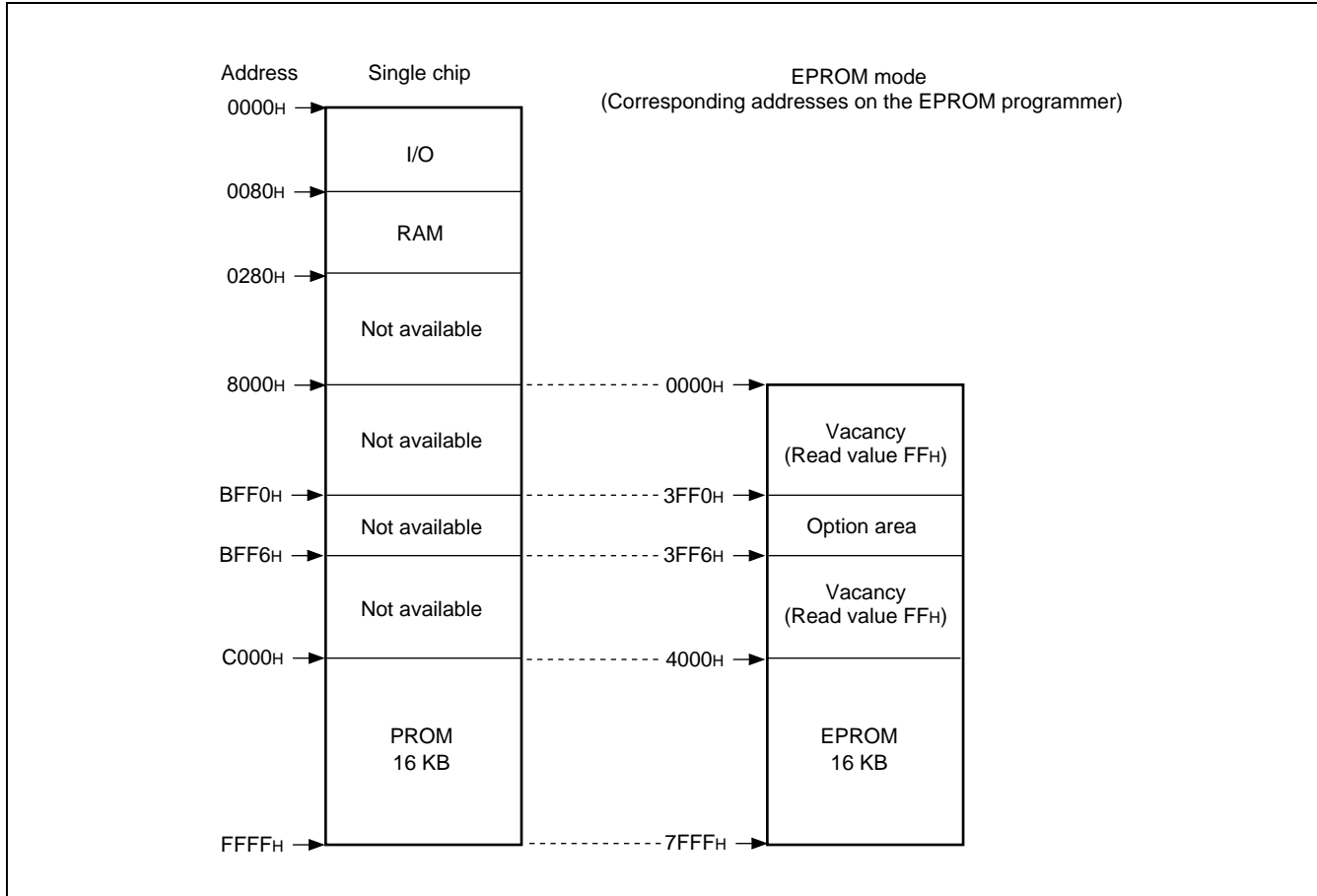
The MB89P135A is an OTPROM version of the MB89123A/125A.

1. Features

- 16-Kbyte PROM on chip
- Equivalency to the MBM27C256A in EPROM mode (when programmed with the EPROM programmer)

2. Memory Space

Memory space in EPROM mode is diagrammed below.



3. Programming to the EPROM

In EPROM mode, the MB89P135A functions equivalent to the MBM27C256A. This allows the PROM to be programmed with a general-purpose EPROM programmer (the electronic signature mode cannot be used) by using the dedicated socket adapter.

• Programming procedure

- (1) Set the EPROM programmer to the MBM27C256A.
- (2) Load program data into the EPROM programmer at 4000H to 7FFFH (note that addresses C000H to FFFFH while operating as a single chip correspond to 4000H to 7FFFH in EPROM mode) .
- (3) Load option data into the EPROM programmer at 3FF0H to 3FF6H.
- (4) Program with the EPROM programmer.

MB89120/120A Series

4. Setting OTPROM Options (MB89P135A Only)

The programming procedure is the same as that for the PROM. Options can be set by programming values at the addresses shown on the memory map. The relationship between bits and options is shown on the following bit map :

• **OTPROM option bit map**

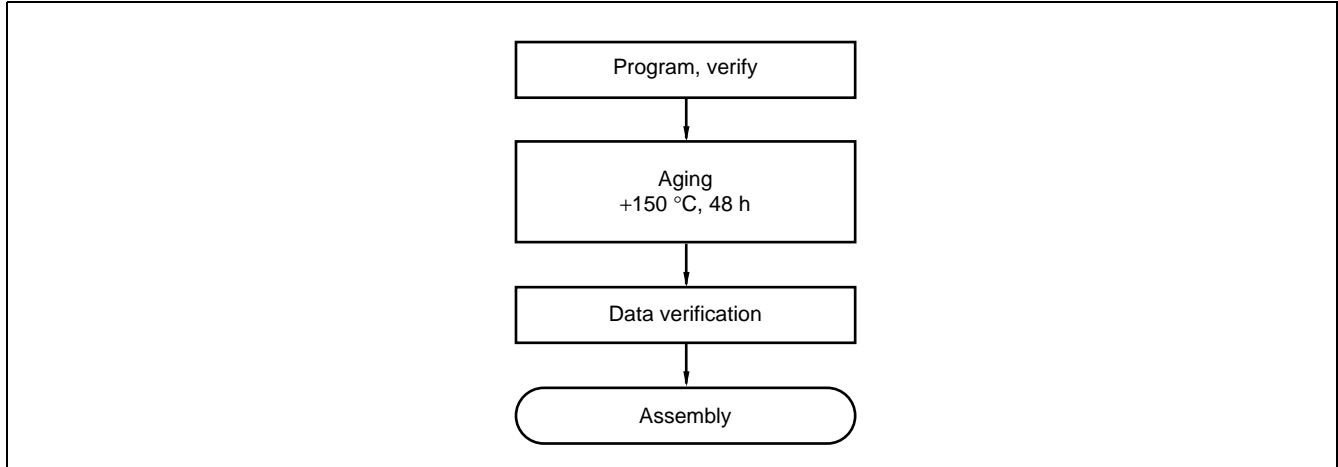
| Address | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------------------|-------------------------------------|-------------------------------------|-------------------------------------|-------------------------------------|-------------------------------------|-------------------------------------|---|--|
| 3FF0 _H | Vacancy | Vacancy | Vacancy | Clock mode selection | Reset pin output | Power-on reset | Oscillation stabilization time | |
| | Readable and writable | Readable and writable | Readable and writable | 1 : Single clock 0 : Dual clock | 1 : Yes 0 : No | 1 : Yes 0 : No | 00 : 2 ² /F _{CH} 01 : 2 ¹² /F _{CH} | 10 : 2 ¹⁶ /F _{CH} 11 : 2 ¹⁸ /F _{CH} |
| 3FF1 _H | P07 Pull-up 1 : Yes 0 : No | P06 Pull-up 1 : Yes 0 : No | P05 Pull-up 1 : Yes 0 : No | P04 Pull-up 1 : Yes 0 : No | P03 Pull-up 1 : Yes 0 : No | P02 Pull-up 1 : Yes 0 : No | P01 Pull-up 1 : Yes 0 : No | P00 Pull-up 1 : Yes 0 : No |
| 3FF2 _H | P17 Pull-up 1 : Yes 0 : No | P16 Pull-up 1 : Yes 0 : No | P15 Pull-up 1 : Yes 0 : No | P14 Pull-up 1 : Yes 0 : No | P13 Pull-up 1 : Yes 0 : No | P12 Pull-up 1 : Yes 0 : No | P11 Pull-up 1 : Yes 0 : No | P10 Pull-up 1 : Yes 0 : No |
| 3FF3 _H | P37 Pull-up 1 : Yes 0 : No | P36 Pull-up 1 : Yes 0 : No | P35 Pull-up 1 : Yes 0 : No | P34 Pull-up 1 : Yes 0 : No | P33 Pull-up 1 : Yes 0 : No | P32 Pull-up 1 : Yes 0 : No | P31 Pull-up 1 : Yes 0 : No | P30 Pull-up 1 : Yes 0 : No |
| 3FF4 _H | Vacancy Readable and writable | Vacancy Readable and writable | Vacancy Readable and writable | Vacancy Readable and writable | Vacancy Readable and writable | Vacancy Readable and writable | Vacancy Readable and writable | Vacancy Readable and writable |
| 3FF5 _H | Vacancy Readable and writable | Vacancy Readable and writable | Vacancy Readable and writable | Vacancy Readable and writable | Vacancy Readable and writable | Vacancy Readable and writable | Vacancy Readable and writable | Vacancy Readable and writable |
| 3FF6 _H | Vacancy Readable and writable | Vacancy Readable and writable | Vacancy Readable and writable | Vacancy Readable and writable | Vacancy Readable and writable | Vacancy Readable and writable | Vacancy Readable and writable | Vacancy Readable and writable |

Note : Each bit is set to "1" as the initialized value, therefore the pull-up option is not selected.

■ HANDLING MB89P131/P133A/P135A

1. Recommended Screening Conditions

High-temperature aging is recommended as the pre-assembly screening procedure.



2. Programming Yield

Due to its nature, bit programming test can't be conducted as Fujitsu delivery test. For this reason, a programming yeild of 100% cannot be assured at all times.

3. EPROM Programmer Socket Adapter and Recommended Programmer Manufacturer

| Part no. | Package | Compatible socket adapter Sun Hayato Co., Ltd. | Recommended programmer manufacturer and programmer name |
|--------------|---------|---|--|
| | | | Minato Electronics Inc. 1890A |
| MB89P131PF | QFP-48 | ROM-48QF2-28DP-8L | Recommended |
| MB89P133APFM | | | — |

Inquiry : Sun Hayato Co., Ltd. : TEL : (81) -3-3986-0403

FAX : (81) -3-5396-9106

Minato Electronics Inc. : TEL : USA (1) -916-348-6066

JAPAN (81) -45-591-5611

MB89120/120A Series

■ PROGRAMMING TO THE EPROM WITH PIGGYBACK/EVALUATION DEVICE

1. EPROM for Use

MBM27C256A-20TVM

2. Programming Socket Adapter

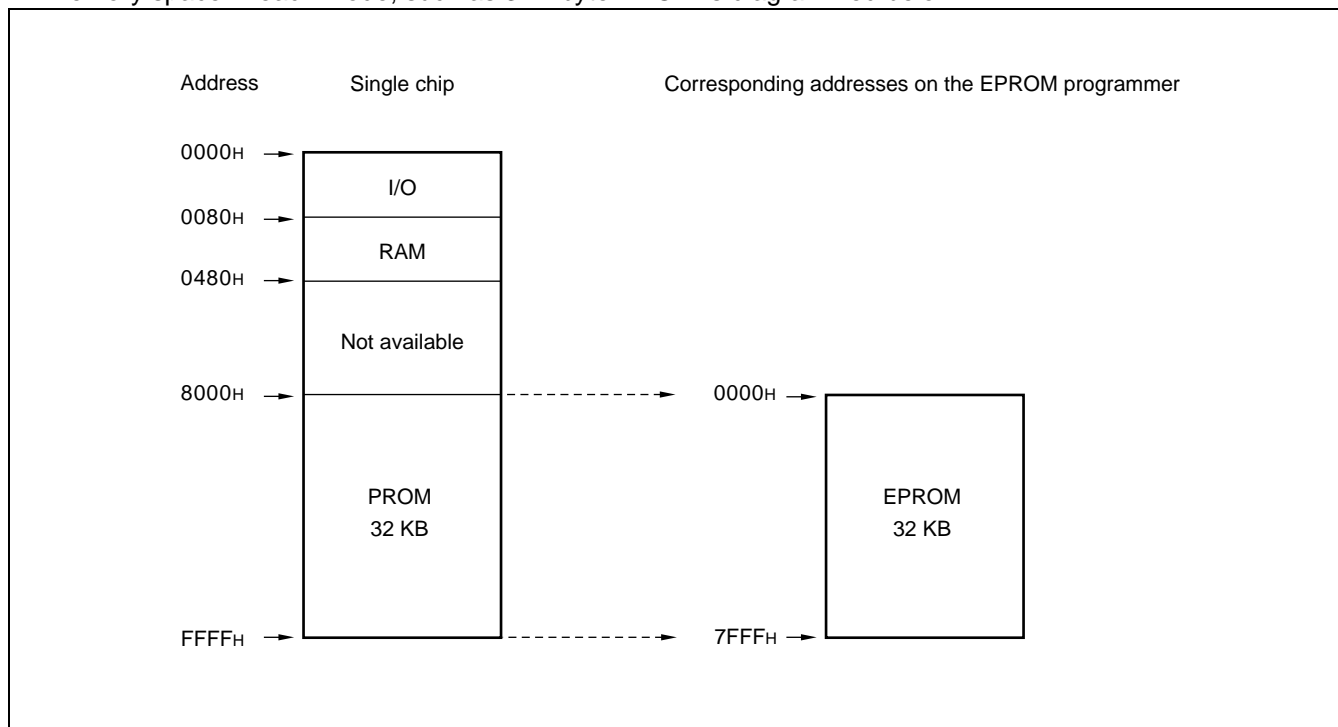
To program to the PROM using an EPROM programmer, use the socket adapter (manufacturer : Sun Hayato Co., Ltd.) listed below :

| Package | Adapter socket part number |
|-----------------|----------------------------|
| LCC-32 (Square) | ROM-32LC-28DP-S |

Inquiry : Sun Hayato Co., Ltd. : TEL (81) -3-3986-0403
FAX (81) -3-5396-9106

3. Memory Space

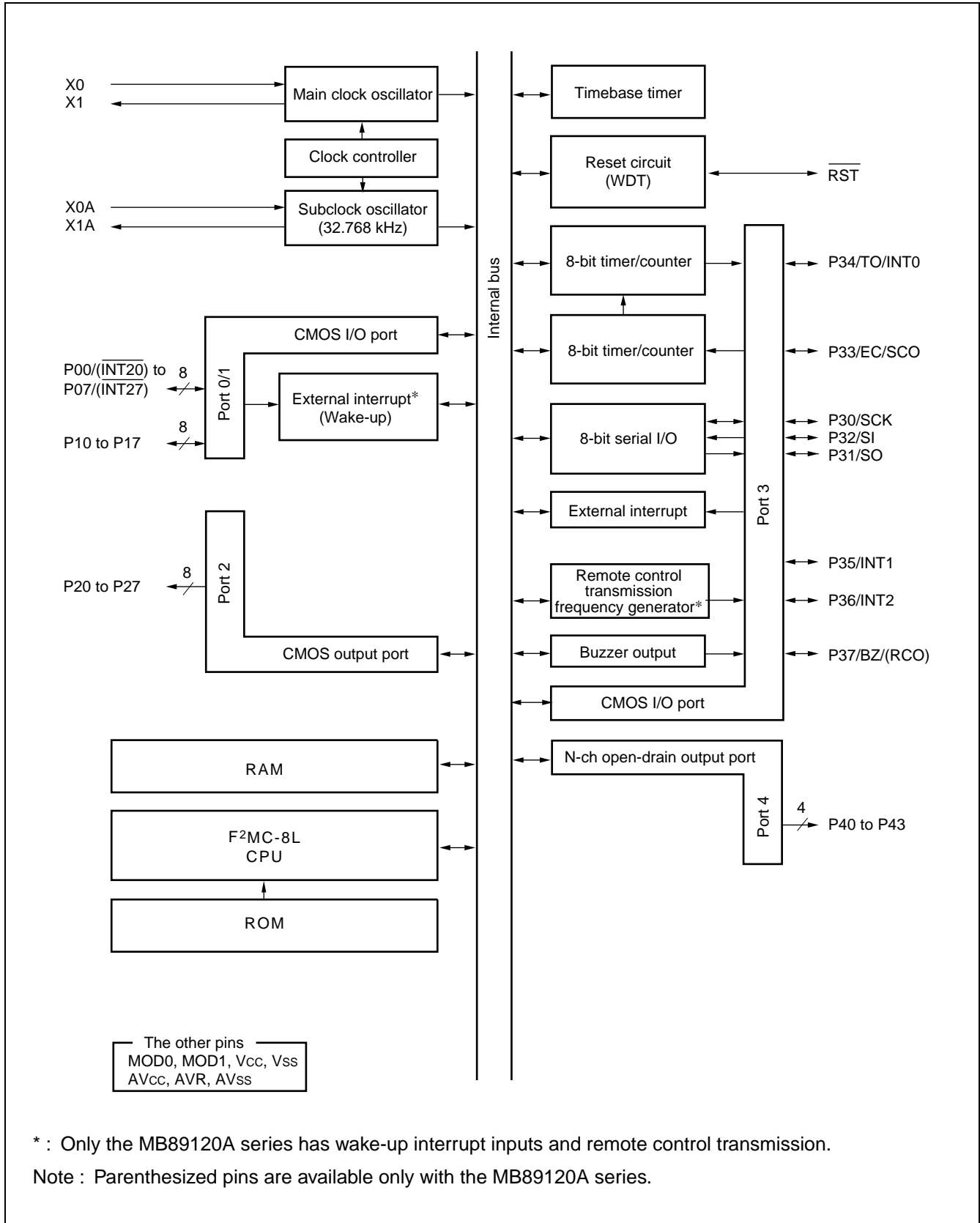
Memory space in each mode, such as 32-Kbyte PROM is diagrammed below.



4. Programming to the EPROM

- (1) Set the EPROM programmer for the MBM27C256A.
- (2) Load program data into the EPROM programmer at 0000H to 7FFFH.
- (3) Program with the EPROM programmer.

■ BLOCK DIAGRAM

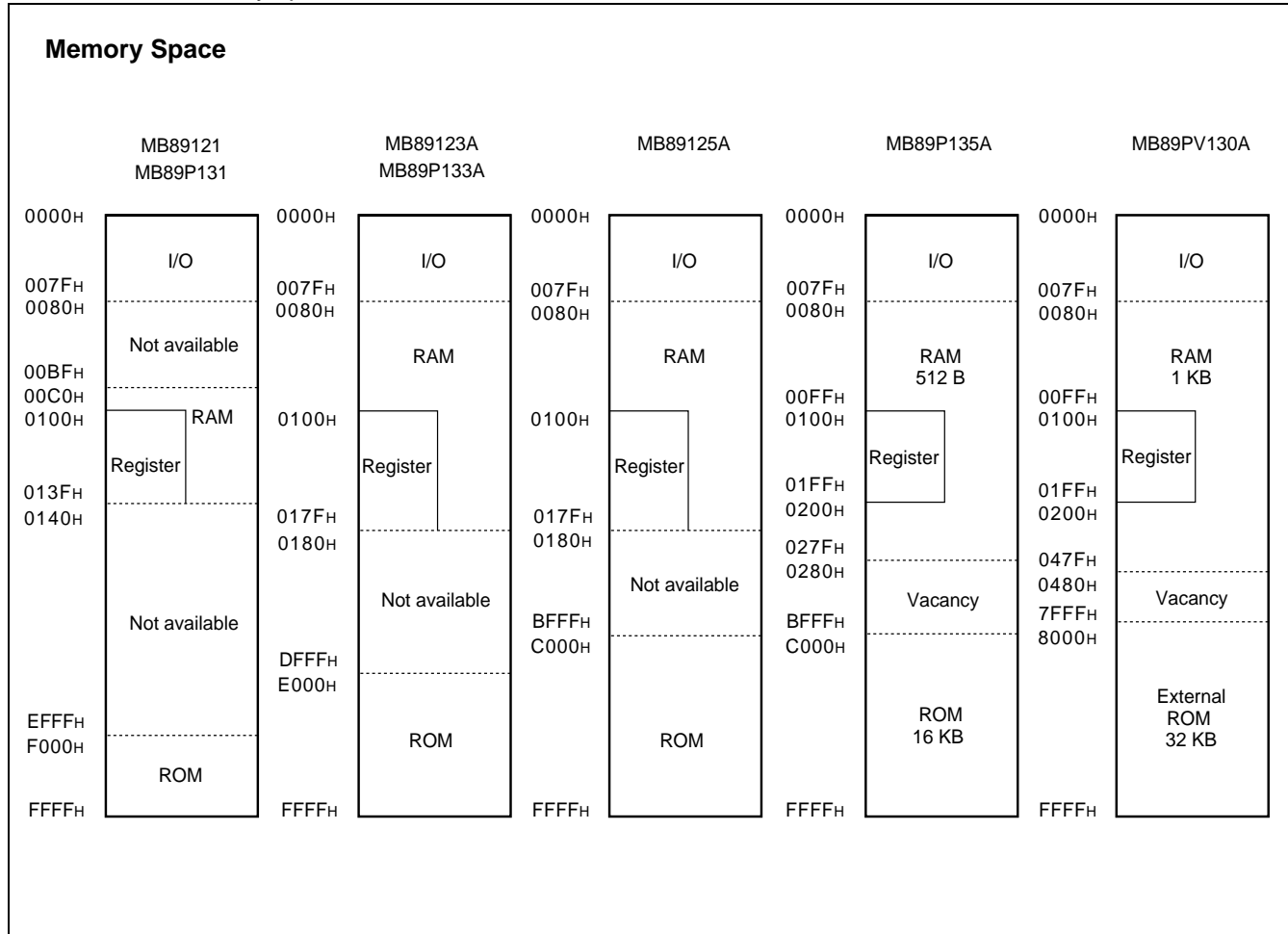


MB89120/120A Series

■ CPU CORE

1. Memory Space

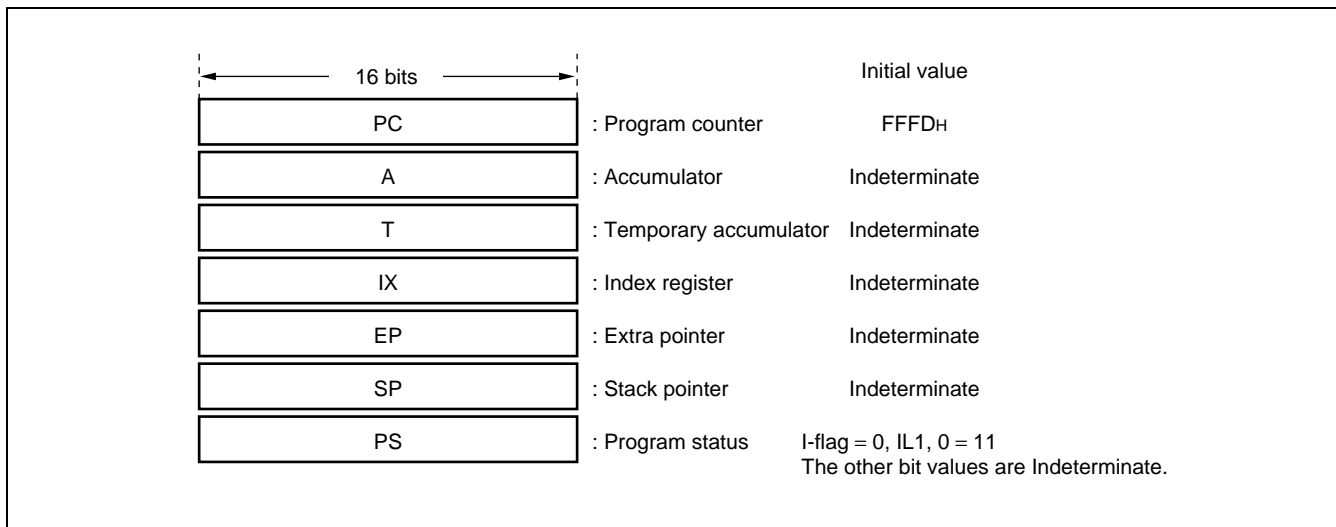
The microcontrollers of the MB89120/A series offer 64 Kbytes of memory for storing all of I/O, data, and program areas. The I/O area is allocated from the lowest address. The data area is allocated immediately above the I/O area. The data area can be divided into register, stack, and direct areas according to the application. The program area is allocated from exactly the opposite end of I/O area, that is, near the highest address. The tables of interrupt reset vectors and vector call instructions are allocated from the highest address with the program area. The memory space of the MB89120/A series is structured as illustrated below :



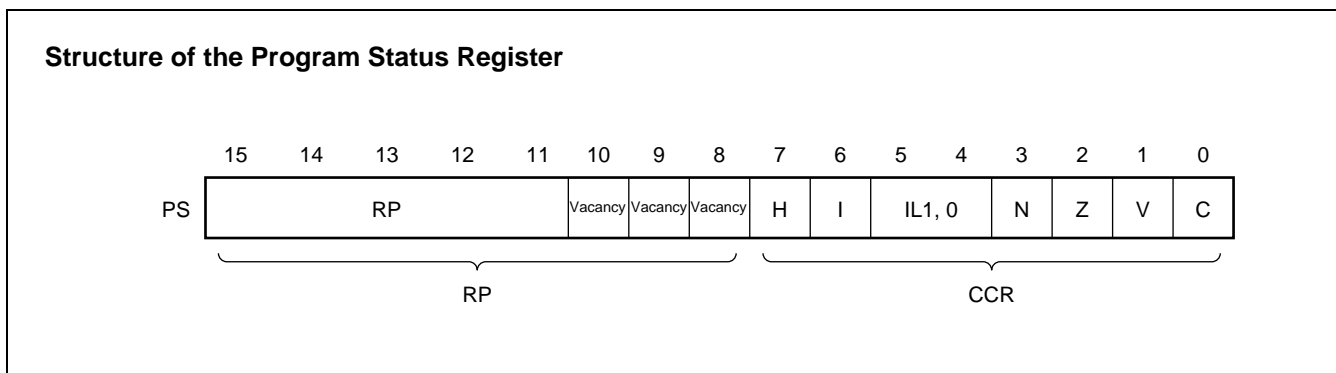
2. Registers

The F²MC-8L family has two types of registers; dedicated hardware registers and general-purpose memory registers. The following dedicated registers are provided :

- Program counter (PC) : A 16-bit-long register for indicating the instruction storage positions
- Accumulator (A) : A 16-bit-long temporary register for arithmetic operations, etc. When the instruction is an 8-bit data processing instruction, the lower byte is used.
- Temporary accumulator (T) : A 16-bit-long register which is used for arithmetic operations with the accumulator. When the instruction is an 8-bit data processing instruction, the lower byte is used.
- Index register (IX) : A 16-bit-long register for index modification
- Extra pointer (EP) : A 16-bit-long pointer for indicating a memory address
- Stack pointer (SP) : A 16-bit-long pointer for indicating a stack area
- Program status (PS) : A 16-bit-long register for storing a register pointer, a condition code



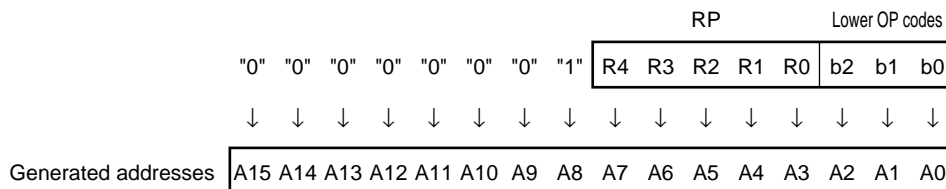
The PS can further be divided into higher 8 bits for use as a register bank pointer (RP) and the lower 8 bits for use as a condition code register (CCR) (see the diagram below) .



MB89120/120A Series

The RP indicates the address of the register bank currently in use. The relationship between the pointer contents and the actual address is based on the conversion rule illustrated below.

Rule for Conversion of Actual Addresses of the General-purpose Register Area



The CCR consists of bits indicating the results of arithmetic operations and the contents of transfer data, and bits for control of CPU operations at the time of an interrupt.

- H-flag : Set to "1" when a carry or a borrow from bit 3 to bit 4 occurs as a result of an arithmetic operation. Cleared "0" otherwise. This flag is for decimal adjustment instructions.
- I-flag : Interrupt is enabled when this flag is set to "1". Interrupt is disabled when the flag is cleared to "0". Cleared to "0" at the reset.
- IL1, 0 : Indicates the level of the interrupt currently allowed. Processes an interrupt only if its request level is higher than the value indicated by this bit.

| IL1 | ILO | Interrupt level | High-low |
|-----|-----|-----------------|----------|
| 0 | 0 | 1 | High |
| 0 | 1 | | ↑ |
| 1 | 0 | 2 | ↓ |
| 1 | 1 | 3 | Low |

- N-flag : Set to "1" if the MSB becomes "1" as the result of an arithmetic operation. Cleared to "0" otherwise.
- Z-flag : Set to "1" when an arithmetic operation results in 0. Cleared to "0" otherwise.
- V-flag : Set to "1" if the complement on "2" overflows as a result of an arithmetic operation. Cleared to "0" if the overflow does not occur.
- C-flag : Set to "1" when a carry or a borrow from bit 7 occurs as a result of an arithmetic operation. Cleared to "0" otherwise. Set to the shift-out value in the case of a shift instruction.

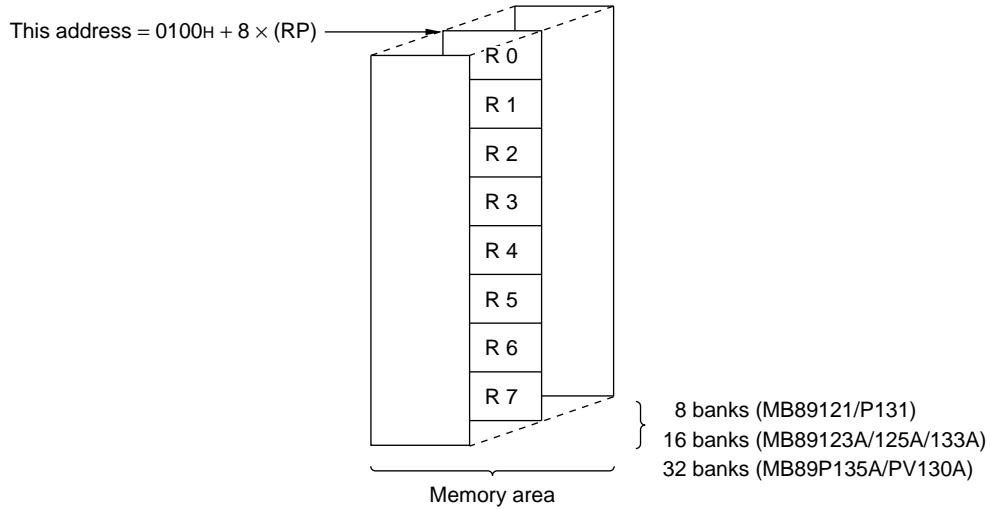
The following general-purpose registers are provided :

General-purpose registers : An 8-bit-long register for storing data

The general-purpose registers are of 8 bits and located in the register banks of the memory. One bank contains eight registers and up to a total of 8 banks can be used on the MB89121/P131, and a total of 16 banks can be used on the MB89123A/125A/P133A and a total of 32 banks can be used on the MB89P135A/PV130A.

The bank currently in use is indicated by the register bank pointer (RP) .

Register Bank Configuration



MB89120/120A Series

■ I/O MAP

| Address | Read/write | Register name | Register description |
|---------|------------|---------------|---|
| 00H | (R/W) | PDR0 | Port 0 data register |
| 01H | (W) | DDR0 | Port 0 data direction register |
| 02H | (R/W) | PDR1 | Port 1 data register |
| 03H | (W) | DDR1 | Port 1 data direction register |
| 04H | (R/W) | PDR2 | Port 2 data register |
| 05H | | | Vacancy |
| 06H | | | Vacancy |
| 07H | (R/W) | SYCC | System clock control register |
| 08H | (R/W) | STBC | Standby control register |
| 09H | (R/W) | WDTC | Watchdog control register |
| 0AH | (R/W) | TBTC | Time-base timer control register |
| 0BH | (R/W) | WPCR | Watch prescaler control register |
| 0CH | (R/W) | PDR3 | Port 3 data register |
| 0DH | (W) | DDR3 | Port 3 data direction register |
| 0EH | (R/W) | PDR4 | Port 4 data register |
| 0FH | (R/W) | BZCR | Buzzer register |
| 10H | | | Vacancy |
| 11H | | | Vacancy |
| 12H | (R/W) | SCGC | Peripheral control clock register |
| 13H | | | Vacancy |
| 14H | (R/W) | RCR1 | Remote control transmission control register 1* |
| 15H | (R/W) | RCR2 | Remote control transmission control register 2* |
| 16H | | | Vacancy |
| 17H | | | Vacancy |
| 18H | (R/W) | T2CR | Timer 2 control register |
| 19H | (R/W) | T1CR | Timer 1 control register |
| 1AH | (R/W) | T2DR | Timer 2 data register |
| 1BH | (R/W) | T1DR | Timer 1 data register |
| 1CH | (R/W) | SMR1 | Serial mode register |
| 1DH | (R/W) | SDR1 | Serial data register |
| 1EH | | | Vacancy |
| 1FH | | | Vacancy |

(Continued)

MB89120/120A Series

(Continued)

| Address | Read/write | Register name | Register description |
|------------------------------------|------------|---------------|---------------------------------------|
| 20 _H | | | Vacancy |
| 21 _H | | | Vacancy |
| 22 _H | | | Vacancy |
| 23 _H | (R/W) | EIC1 | External interrupt control register 1 |
| 24 _H | (R/W) | EIC2 | External interrupt control register 2 |
| 25 _H | | | Vacancy |
| 26 _H to 31 _H | | | Vacancy |
| 32 _H | (R/W) | EIE2 | External interrupt 2 enable register* |
| 33 _H | (R/W) | EIF2 | External interrupt 2 flag register* |
| 34 _H to 7B _H | | | Vacancy |
| 7C _H | (W) | ILR1 | Interrupt level register 1 |
| 7D _H | (W) | ILR2 | Interrupt level register 2 |
| 7E _H | (W) | ILR3 | Interrupt level register 3 |
| 7F _H | | | Vacancy |

* : Only in the MB89120A series

Note : Do not use vacancies.

MB89120/120A Series

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

($AV_{SS} = V_{SS} = 0.0\text{ V}$)

| Parameter | Symbol | Value | | Unit | Remarks |
|--|--------------------------------|----------------|-----------------|------|---|
| | | Min. | Max. | | |
| Power supply voltage | V_{CC} AV_{CC} AVR | $V_{SS} - 0.3$ | $V_{SS} + 7.2$ | V | Use V_{CC} , AV_{CC} , and AVR set to the same voltage. |
| Program voltage | V_{PP} | $V_{SS} - 0.6$ | $V_{SS} + 13.0$ | V | MOD1 pin on the MB89P131/P133A/P135A |
| Input voltage | V_I | $V_{SS} - 0.3$ | $V_{CC} + 0.3$ | V | |
| Output voltage | V_O | $V_{SS} - 0.3$ | $V_{CC} + 0.3$ | V | |
| “L” level maximum output current | I_{OL} | — | 10 | mA | |
| “L” level average output current | I_{OLAV} | — | 4 | mA | Average value (operating current × operating rate) |
| “L” level total maximum output current | ΣI_{OL} | — | 100 | mA | |
| “L” level total average output current | ΣI_{OLAV} | — | 20 | mA | Average value (operating current × operating rate) |
| “H” level maximum output current | I_{OH} | — | -10 | mA | |
| “H” level average output current | I_{OHAV} | — | -2 | mA | Average value (operating current × operating rate) |
| “H” level total maximum output current | ΣI_{OH} | — | -30 | mA | |
| “H” level total average output current | ΣI_{OHAV} | — | -10 | mA | Average value (operating current × operating rate) |
| Power consumption | P_D | — | 200 | mW | |
| Operating temperature | T_A | -40 | +85 | °C | |
| Storage temperature | T_{stg} | -55 | +150 | °C | |

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

($V_{SS} = V_{SS} = 0.0\text{ V}$)

| Parameter | Symbol | Value | | Unit | Remarks |
|-----------------------|----------|-------|------|------|---|
| | | Min. | Max. | | |
| Power supply voltage | V_{CC} | 2.2* | 6.0* | V | Normal operation assurance range Applied to "MB89P131/P133A/P135A/PV130A, and single-clock MB89121/123A/125A**" |
| | | 2.7* | 6.0* | V | Normal operation assurance range Applied to "Dual-clock MB89121/123A/125A**" |
| | | 1.5 | 6.0 | V | Retains the RAM state in stop mode |
| Operating temperature | T_A | -40 | +85 | °C | |

* : These values vary with the operating conditions. See "**Operating Voltage vs. Main Clock Operating Frequency.**"

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

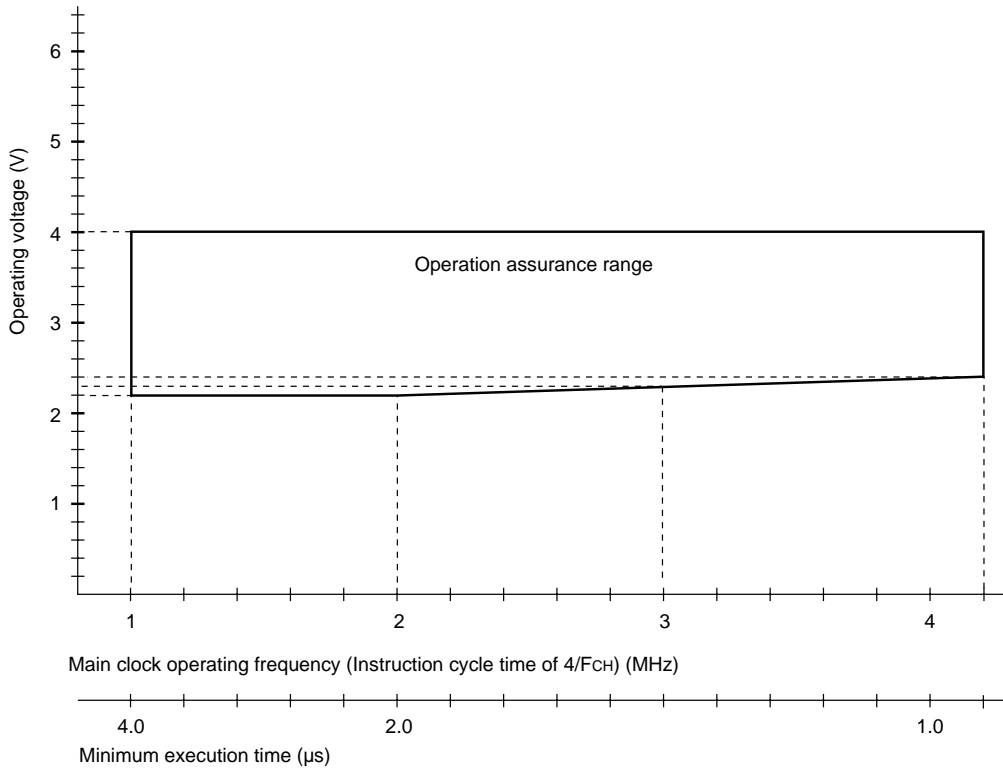
Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

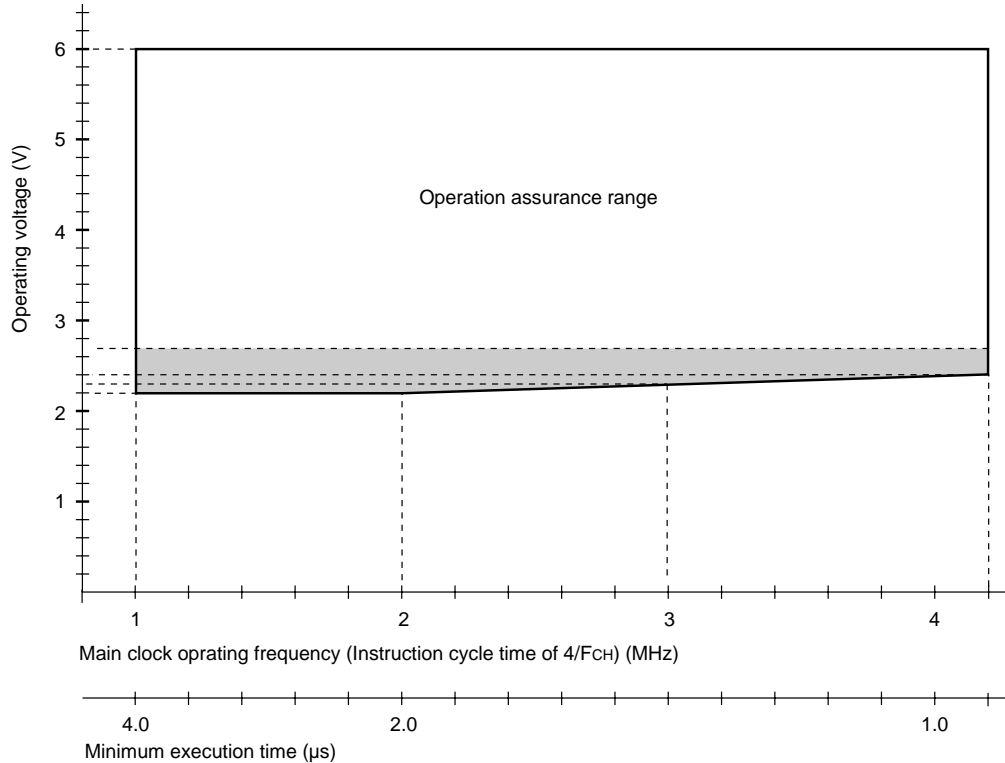
MB89120/120A Series

• Operating Voltage vs. Main Clock Operating Frequency

Dual-clock MB89121/123A/125A



MB89P131/P133A/P135A/PV130A, and single-clock MB89121/123A/125A



Note : The shaded area is assured only for the MB89121/123A/125A (instruction cycle time of $4/F_{CH}$) .

MB89120/120A Series

3. DC Characteristics

($A_{V_{CC}} = V_{CC} = +5.0\text{ V}$, $A_{V_{SS}} = V_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$)

| Parameter | Symbol | Pin | Condition | Value | | | Unit | Remarks |
|---|------------|--|--------------------------------|----------------|------|----------------|------------------|---|
| | | | | Min. | Typ. | Max. | | |
| “H” level input voltage | V_{IH} | P00 to P07, P10 to P17 | — | $0.7 V_{CC}$ | — | $V_{CC} + 0.3$ | V | |
| | V_{IHS} | $\overline{\text{RST}}$, P30 to P37, $\overline{\text{INT20}}$ to $\overline{\text{INT27}}$ | — | $0.8 V_{CC}$ | — | $V_{CC} + 0.3$ | V | $\overline{\text{INT20}}$ to $\overline{\text{INT27}}$ are available only in the MB89120A series. |
| “L” level input voltage | V_{IL} | P00 to P07, P10 to P17 | — | $V_{SS} - 0.3$ | — | $0.3 V_{CC}$ | V | |
| | V_{ILS} | $\overline{\text{RST}}$, P30 to P37, $\overline{\text{INT20}}$ to $\overline{\text{INT27}}$ | — | $V_{SS} - 0.3$ | — | $0.2 V_{CC}$ | V | $\overline{\text{INT20}}$ to $\overline{\text{INT27}}$ are available only in the MB89120A series. |
| Open-drain output pin applied voltage | V_D | P40 to P43 | — | $V_{SS} - 0.3$ | — | $V_{CC} + 0.3$ | V | |
| “H” level output voltage | V_{OH} | P00 to P07, P10 to P17, P20 to P27, P30 to P37 | $I_{OH} = -2.0\text{ mA}$ | 2.4 | — | — | V | |
| “L” level output voltage | V_{OL} | P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P43 | $I_{OL} = 1.8\text{ mA}$ | — | — | 0.4 | V | |
| | V_{OL2} | $\overline{\text{RST}}$ | $I_{OL} = 4.0\text{ mA}$ | — | — | 0.6 | V | |
| Input leakage current (Hi-z output leakage current) | I_{LI} | P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P43, MOD0, MOD1 | $0.45\text{ V} < V_I < V_{CC}$ | — | — | ± 5 | μA | Without pull-up resistor |
| Pull-up resistance | R_{PULL} | P00 to P07, P10 to P17, P30 to P37, P40 to P43, $\overline{\text{RST}}$ | $V_I = 0.0\text{ V}$ | 25 | 50 | 100 | $\text{k}\Omega$ | |

(Continued)

MB89120/120A Series

(Continued)

($AV_{CC} = V_{CC} = +5.0\text{ V}$, $AV_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$)

| Parameter | Symbol | Pin | Condition | Value | | | Unit | Remarks |
|-----------------------------|--|--|--|-------|------|------|------------------------------|-----------------------|
| | | | | Min. | Typ. | Max. | | |
| Power supply current*1 | I _{CC1} | V _{CC} (External clock operation) | V _{CC} = 5.0 V F _{CH} = 4.00 MHz t _{inst} *2 = 1.0 μs | — | 4 | 7 | mA | MB89121/ 123A/125A |
| | | | — | 6 | 10 | mA | MB89P131/ P133A/ P135A | |
| | I _{CCS1} | | V _{CC} = 5.0 V F _{CH} = 4.00 MHz Main sleep mode t _{inst} *2 = 1.0 μs | — | 2 | 5 | mA | |
| | I _{CCL} | | V _{CC} = 3.0 V F _{CL} = 32.768 kHz Subclock mode | — | 50 | 100 | μA | MB89121/ 123A/125A |
| | | | — | 1 | 3 | mA | MB89P131/ P133A/ P135A | |
| | I _{CCLS} | | V _{CC} = 3.0 V F _{CL} = 32.768 kHz Subclock sleep mode | — | 25 | 50 | μA | |
| | I _{CC_T} | | V _{CC} = 3.0 V F _{CL} = 32.768 kHz • Watch mode • Main clock stop mode at dual clock system | — | — | 15 | μA | |
| I _{CC_H} | T _A = +25 °C • Subclock stop mode • Main clock stop mode at single clock system | — | — | 1 | μA | | | |
| Input capacitance | C _{IN} | Other than AV _{CC} , AV _{SS} , V _{CC} , and V _{SS} | f = 1 MHz | — | 10 | — | pF | |

*1 : The measurement conditions of power supply current is external clock. ($V_{CC} = 5.0\text{ V}$, $V_{CC} = 3.0\text{ V}$)

*2 : For information on t_{inst}, see “(4) Instruction Cycle” in “4. AC Characteristics.”

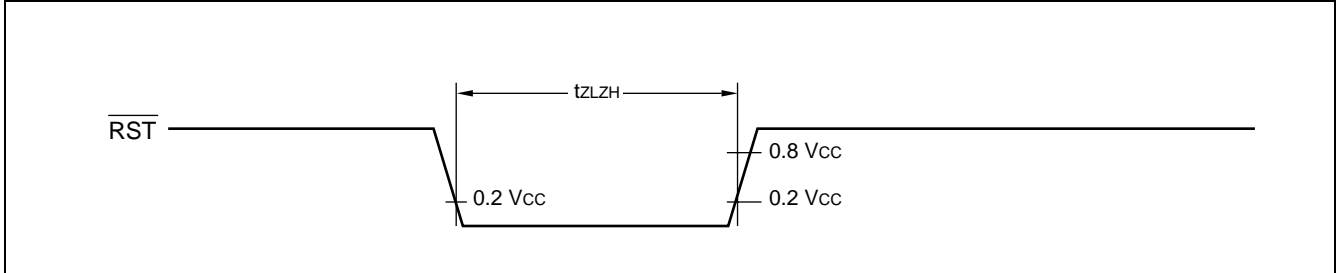
4. AC Characteristics

(1) Reset Timing

($V_{CC} = +5.0\text{ V} \pm 10\%$, $AV_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$)

| Parameter | Symbol | Condition | Value | | Unit | Remarks |
|---|-------------------|-----------|------------------------|------|------|---------|
| | | | Min. | Max. | | |
| $\overline{\text{RST}}$ "L" pulse width | t_{ZLZH} | — | 48 t_{HCYL}^* | — | ns | |

* : t_{HCYL} is the oscillation cycle ($1/F_{\text{CH}}$) input to the X0.



(2) Power-on Reset

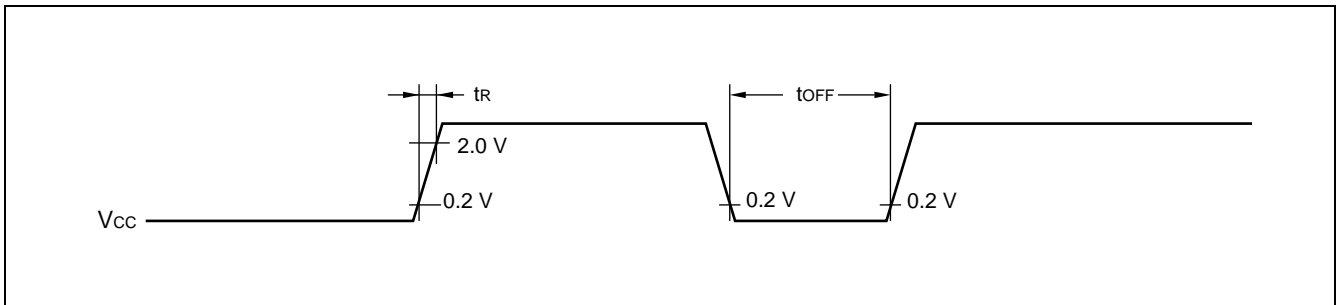
($AV_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$)

| Parameter | Symbol | Condition | Value | | Unit | Remarks |
|---------------------------|------------------|-----------|-------|------|------|------------------------------|
| | | | Min. | Max. | | |
| Power supply rising time | t_{R} | — | — | 50 | ms | Power-on reset function only |
| Power supply cut-off time | t_{OFF} | | 1 | — | ms | Due to repeated operations |

Note : Make sure that power supply rises within the oscillation stabilization time selected.

When the main clock is operating at $F_{\text{CH}} = 3\text{ MHz}$ and the oscillation stabilization time select option has been set to $2^{12}/F_{\text{CH}}$, for example, the oscillation settling time is 1.4 ms and accordingly the maximum value of power supply rising time is about 1.4 ms.

Keep in mind that rapid changes in power supply voltage may cause a power-on reset. If power supply voltage needs to be varied in the course of operation, a smooth voltage rise is recommended.



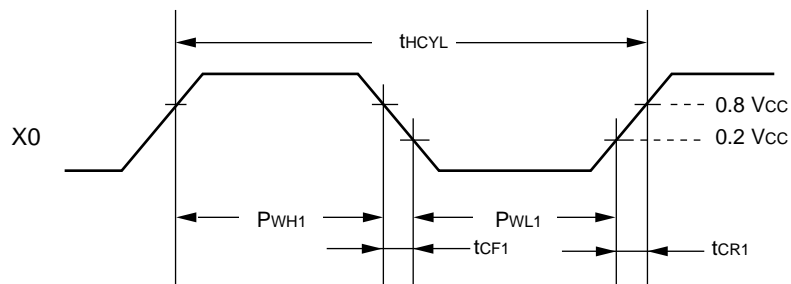
MB89120/120A Series

(3) Clock Timings

($V_{SS} = 0.0 \text{ V}$, $T_A = -40 \text{ }^\circ\text{C}$ to $+85 \text{ }^\circ\text{C}$)

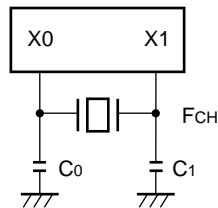
| Parameter | Symbol | Pin | Value | | | Unit | Remarks |
|---------------------------------|------------------------|----------|-------|--------|------|---------------|----------------|
| | | | Min. | Typ. | Max. | | |
| Clock frequency | F_{CH} | X0, X1 | 1 | — | 4.2 | MHz | Main clock |
| | F_{CL} | X0A, X1A | — | 32.768 | — | kHz | Subclock |
| Clock cycle time | t_{HCYL} | X0, X1 | 238 | — | 1000 | ns | Main clock |
| | t_{LCYL} | X0A, X1A | — | 30.5 | — | μs | Subclock |
| Input clock pulse width | P_{WH1} P_{WL1} | X0 | 72 | — | — | ns | External clock |
| Input clock rising/falling time | t_{CR1} t_{CF1} | X0 | — | — | 24 | ns | External clock |

X0, X1 Timings and Conditions of Applied Voltage

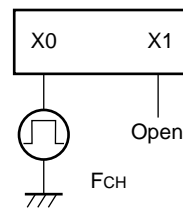


Main Clock Conditions of Applied Voltage

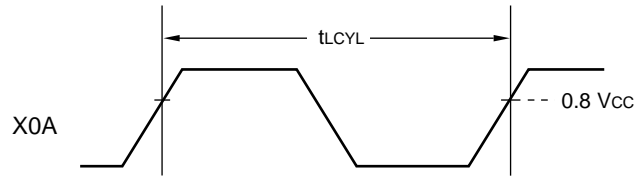
When a crystal or ceramic resonator is used



When an external clock is used

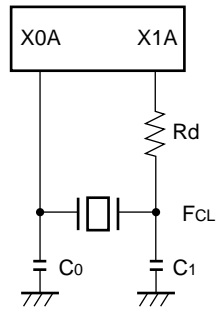


X0A, X1A Timings and Conditions of Applied Voltage

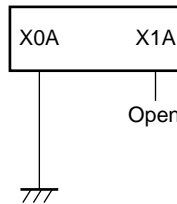


Subclock Conditions of Applied Voltage

When a crystal or ceramic resonator is used



Single-clock option is used



(4) Instruction Cycles

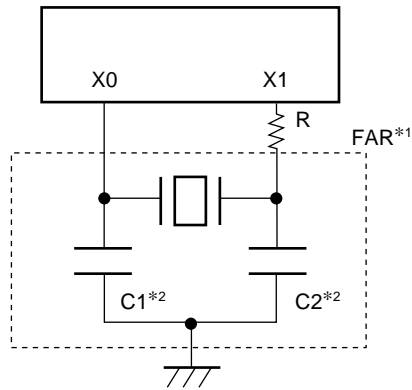
(V_{SS} = 0.0 V, T_A = -40 °C to +85 °C)

| Parameter | Symbol | Value (typical) | Unit | Remarks |
|--|-------------------|---|------|---|
| Instruction cycle (minimum execution time) | t _{inst} | 4/F _{CH} , 8/F _{CH} , 16/F _{CH} , 64/F _{CH} | μs | (4/F _{CH}) t _{inst} = 1.0 μs when operating at F _{CH} = 4 MHz |
| | | 2/F _{CL} | μs | t _{inst} = 61.036 μs when operating at F _{CL} = 32.768 kHz |

MB89120/120A Series

(5) Recommended Resonator Manufacturers

Sample Application of Piezoelectric Resonator (FAR Series) for Main Clock Oscillation Circuit (Only in the MB89120A Series)

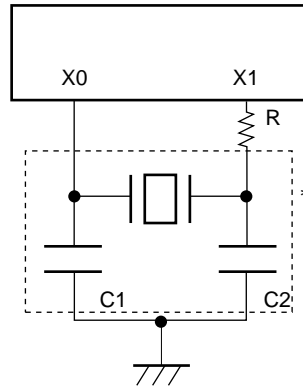


*1 : FUJITSU MEDIA DEVICE LIMITED

| FAR part number (built-in capacitor type) | Frequency (MHz) | Dumping resistor | Initial deviation of FAR frequency ($T_A = +25\text{ }^\circ\text{C}$) | Temperature characteristics of FAR frequency ($T_A = -20\text{ }^\circ\text{C}$ to $+60\text{ }^\circ\text{C}$) | Loading capacitors*2 |
|--|--------------------|---------------------|--|--|-------------------------|
| FAR-C4CC-02000-L00 | 2.00 | 1000 | $\pm 0.5\%$ | $\pm 0.5\%$ | Built-in |
| | | 510 | | | |
| FAR-C4□A-03580-□01 | 3.58 | — | | | |
| FAR-C4CB-04000-M00 | 4.00 | | | | |

Inquiry : FUJITSU MEDIA DEVICES LIMITED

Sample Application of Ceramic Resonator for Main Clock Oscillation Circuit



• Mask ROM products

| Resonator manufacturer* | Resonator | Frequency (MHz) | C1 (pF) | C2 (pF) | R (kΩ) |
|----------------------------------|----------------|-----------------|----------|----------|--------------|
| Kyocera Corporation | KBR-4.0MKS | 4.00 | 33 | 33 | Not required |
| Matsushita Electronic Components | EFOV4004B | 4.00 | Built-in | Built-in | 1.5 |
| Murata Mfg. Co. Ltd. | CSBF1000J | 1.00 | 100 | 100 | 6.8 |
| | CSTCS4.00MG800 | 4.00 | Built-in | Built-in | Not required |
| | CSA4.00MG040 | | 100 | 100 | Not required |
| | CST4.00MGW040 | | Built-in | Built-in | Not required |

Inquiry : Kyocera Corporation

- AVX Corporation
North American Sales Headquarters : TEL (803) 448-9411
- AVX Limited
European Sales Headquarters : TEL (01252) 770000
- AVX/Kyocera H.K. Ltd.
Asian Sales Headquarters : TEL 363-3303

Matsushita Electronic Components Co., Ltd.

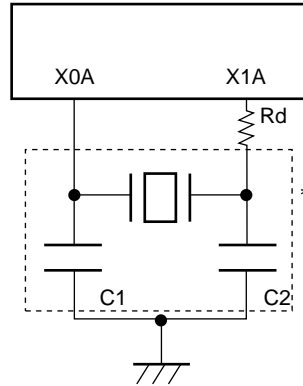
- Ceramic Division : TEL 81-6-908-1101

Murata Mfg Co., Ltd.

- Murata Electronics North America, Inc. : TEL 1-404-436-1300
- Murata Europe Management GmbH : TEL 49-911-66870
- Murata Electronics Singapore (Pte.) Ltd. : TEL 65-758-4233

MB89120/120A Series

Sample Application of Crystal Resonator for Subclock Oscillation Circuit



• Mask ROM product

| Resonator manufacturer* | Resonator | Frequency (kHz) | C1 (pF) | C2 (pF) | Rd (kΩ) |
|-------------------------|-----------|-----------------|---------|---------|---------|
| SII | DS-VT-200 | 32.768 | 24 | 24 | 680 |

Inquiry : SII

Seiko Instruments Inc. (Japan) : TEL 81-43-211-1219

Seiko Instruments U.S.A. Inc. : TEL 310-517-7770

Seiko Instruments GmbH : TEL 49-6102-297-122

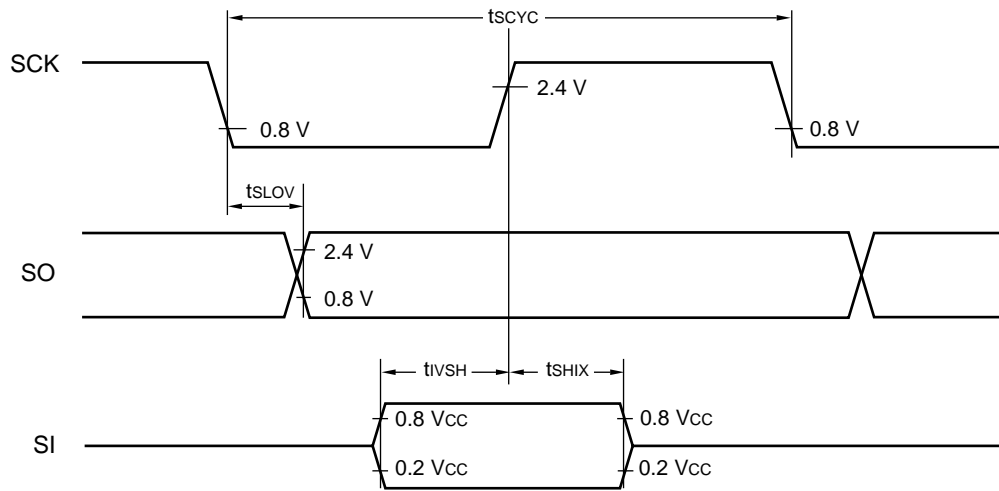
(6) Serial I/O Timings

($V_{CC} = +5.0\text{ V} \pm 10\%$, $AV_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$)

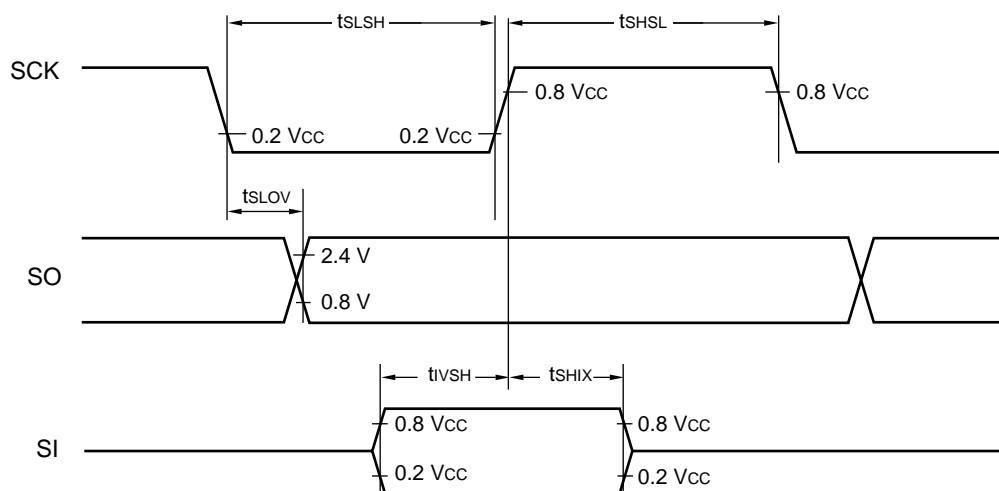
| Parameter | Symbol | Pin | Condition | Value | | Unit | Remarks |
|---|------------|---------|--------------------------|----------------|------|---------------|---------|
| | | | | Min. | Max. | | |
| Serial clock cycle time | t_{SCYC} | SCK | Internal clock operation | $2 t_{inst}^*$ | — | μs | |
| SCK $\downarrow \rightarrow$ SO time | t_{SLOV} | SCK, SO | | -200 | 200 | ns | |
| Valid SI \rightarrow SCK \uparrow | t_{IVSH} | SI, SCK | | 200 | — | ns | |
| SCK $\uparrow \rightarrow$ Valid SI hold time | t_{SHIX} | SCK, SI | | 200 | — | ns | |
| Serial clock "H" pulse width | t_{SHSL} | SCK | External clock operation | t_{inst}^* | — | μs | |
| Serial clock "L" pulse width | t_{SLSH} | | | t_{inst}^* | — | μs | |
| SCK $\downarrow \rightarrow$ SO time | t_{SLOV} | SCK, SO | | 0 | 200 | ns | |
| Valid SI \rightarrow SCK \uparrow | t_{IVSH} | SI, SCK | | 200 | — | ns | |
| SCK $\uparrow \rightarrow$ Valid SI hold time | t_{SHIX} | SCK, SI | 200 | — | ns | | |

* : For information on t_{inst} , see "(4) Instruction Cycles."

Internal Shift Clock Mode



External Shift Clock Mode



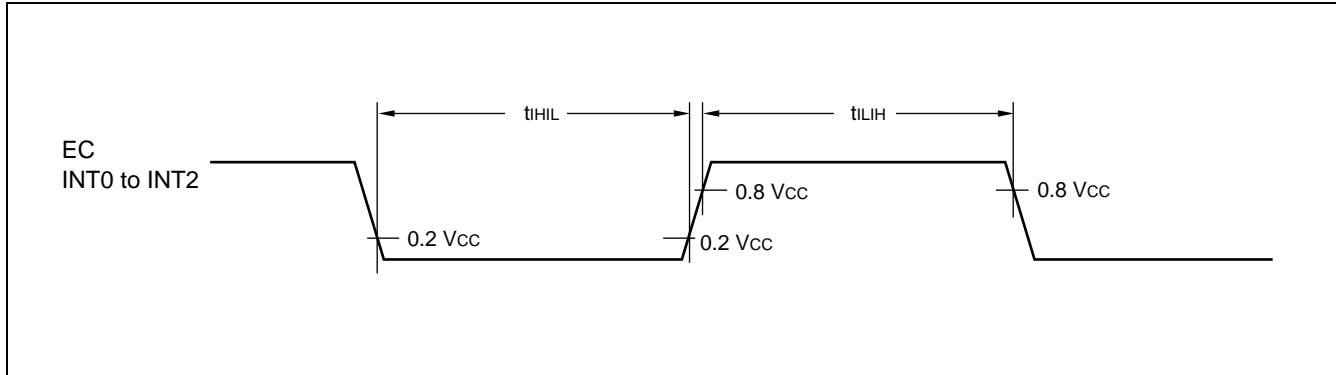
MB89120/120A Series

(7) Peripheral Input Timings

($V_{CC} = +5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$)

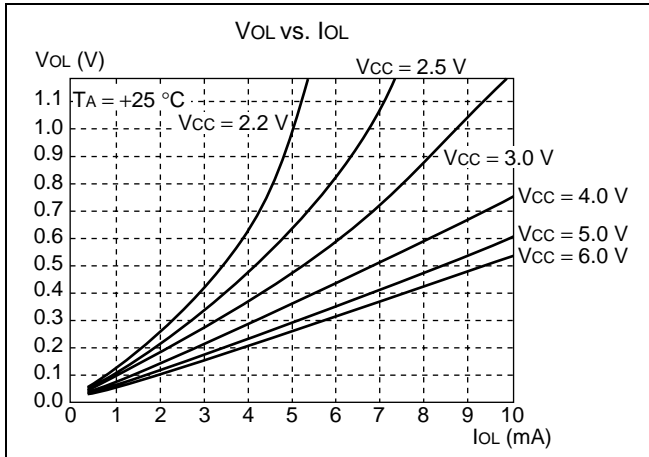
| Parameter | Symbol | Pin | Value | | Unit | Remarks |
|----------------------------------|----------|------------------|----------------|------|---------------|---------|
| | | | Min. | Max. | | |
| Peripheral input "H" pulse width | t_{LH} | EC, INT0 to INT2 | $2 t_{inst}^*$ | — | μS | |
| Peripheral input "L" pulse width | t_{HL} | | $2 t_{inst}^*$ | — | μS | |

* : For information on t_{inst} , see "(4) Instruction Cycle."

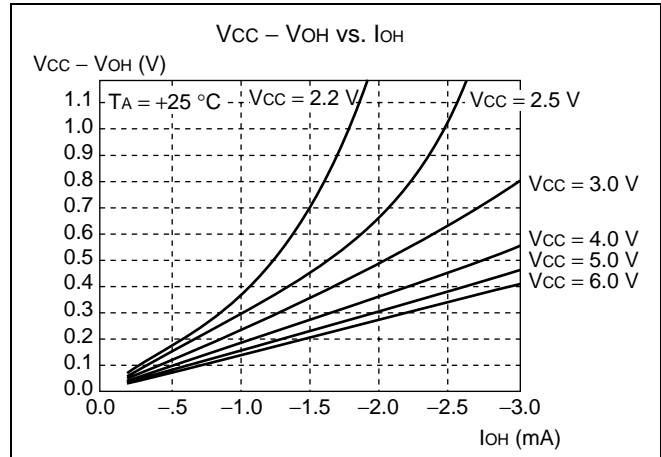


EXAMPLE CHARACTERISTICS

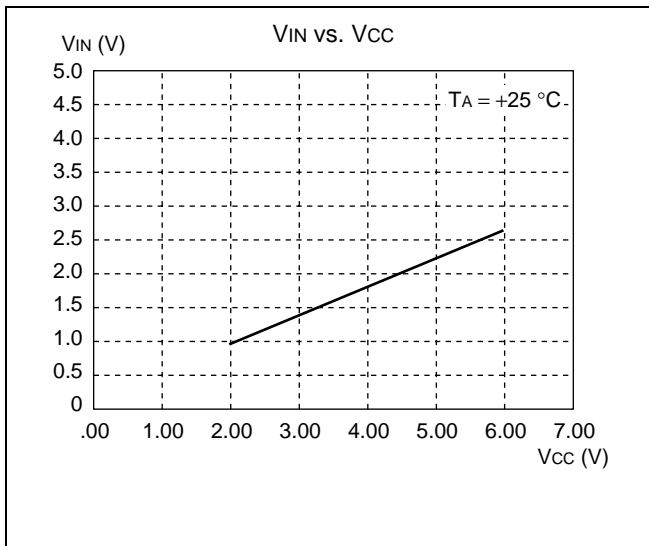
(1) "L" Level Output Voltage



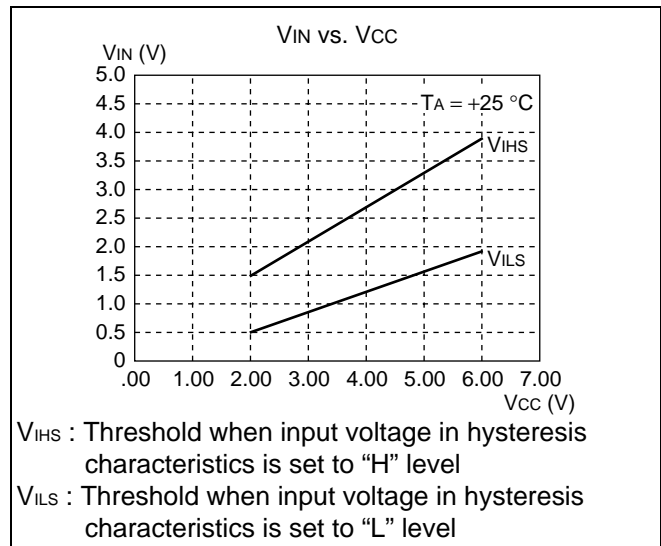
(2) "H" Level Output Voltage



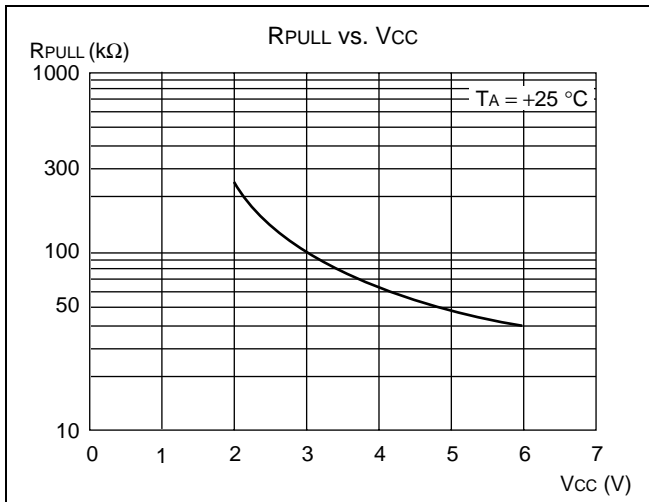
(3) "H" Level Input Voltage/"L" Level Input Voltage (CMOS Input)



(4) "H" Level Input Voltage/"L" Level Input Voltage (Hysteresis Input)

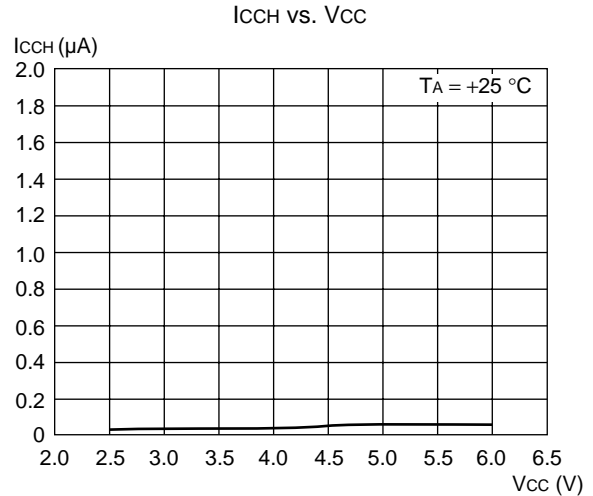
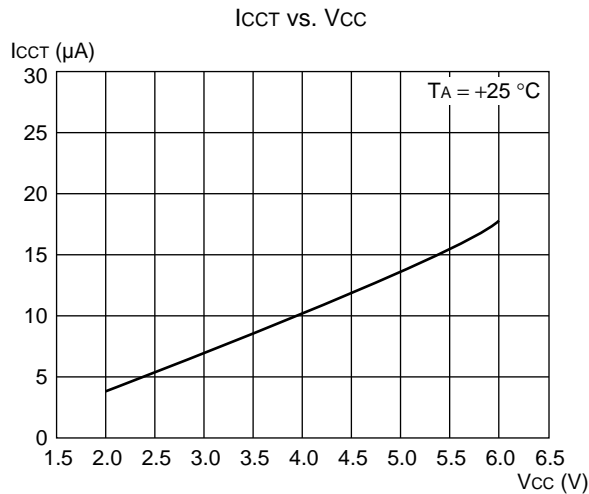
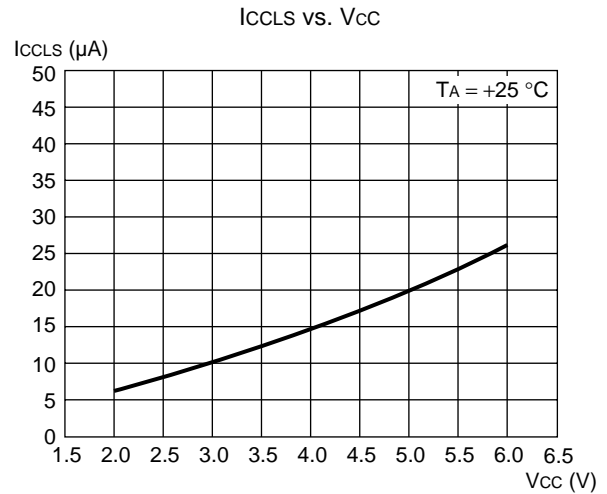
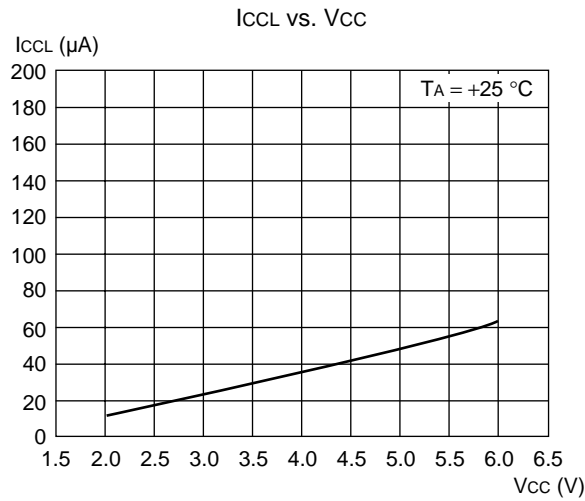
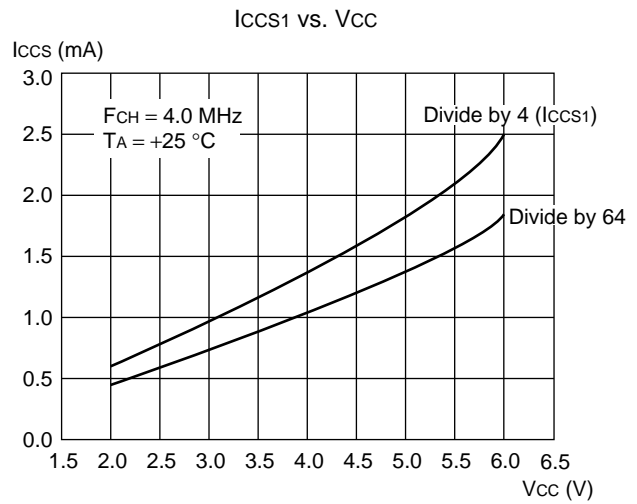
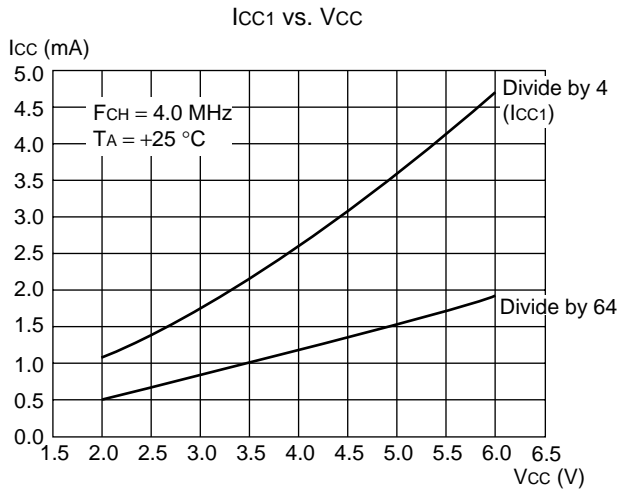


(5) Pull-up Resistance



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(6) Power Supply Current



■ INSTRUCTIONS (136 INSTRUCTIONS)

Execution instructions can be divided into the following four groups:

- Transfer
- Arithmetic operation
- Branch
- Others

Table 1 lists symbols used for notation of instructions.

Table 1 Instruction Symbols

| Symbol | Meaning |
|--------|---|
| dir | Direct address (8 bits) |
| off | Offset (8 bits) |
| ext | Extended address (16 bits) |
| #vct | Vector table number (3 bits) |
| #d8 | Immediate data (8 bits) |
| #d16 | Immediate data (16 bits) |
| dir: b | Bit direct address (8:3 bits) |
| rel | Branch relative address (8 bits) |
| @ | Register indirect (Example: @A, @IX, @EP) |
| A | Accumulator A (Whether its length is 8 or 16 bits is determined by the instruction in use.) |
| AH | Upper 8 bits of accumulator A (8 bits) |
| AL | Lower 8 bits of accumulator A (8 bits) |
| T | Temporary accumulator T (Whether its length is 8 or 16 bits is determined by the instruction in use.) |
| TH | Upper 8 bits of temporary accumulator T (8 bits) |
| TL | Lower 8 bits of temporary accumulator T (8 bits) |
| IX | Index register IX (16 bits) |
| EP | Extra pointer EP (16 bits) |
| PC | Program counter PC (16 bits) |
| SP | Stack pointer SP (16 bits) |
| PS | Program status PS (16 bits) |
| dr | Accumulator A or index register IX (16 bits) |
| CCR | Condition code register CCR (8 bits) |
| RP | Register bank pointer RP (5 bits) |
| Ri | General-purpose register Ri (8 bits, i = 0 to 7) |
| × | Indicates that the very × is the immediate data. (Whether its length is 8 or 16 bits is determined by the instruction in use.) |
| (×) | Indicates that the contents of × is the target of accessing. (Whether its length is 8 or 16 bits is determined by the instruction in use.) |
| ((×)) | The address indicated by the contents of × is the target of accessing. (Whether its length is 8 or 16 bits is determined by the instruction in use.) |

Columns indicate the following:

Mnemonic: Assembler notation of an instruction

~: The number of instructions

#: The number of bytes

Operation: Operation of an instruction

TL, TH, AH: A content change when each of the TL, TH, and AH instructions is executed. Symbols in the column indicate the following:

- “-” indicates no change.
- dH is the 8 upper bits of operation description data.
- AL and AH must become the contents of AL and AH prior to the instruction executed.
- 00 becomes 00.

N, Z, V, C: An instruction of which the corresponding flag will change. If + is written in this column, the relevant instruction will change its corresponding flag.

OP code: Code of an instruction. If an instruction is more than one code, it is written according to the following rule:
Example: 48 to 4F ← This indicates 48, 49, ... 4F.

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Table 2 Transfer Instructions (48 instructions)

| Mnemonic | ~ | # | Operation | TL | TH | AH | NZVC | OP code |
|------------------|---|---|---|----|----|----|-------|----------|
| MOV dir,A | 3 | 2 | (dir) ← (A) | - | - | - | ----- | 45 |
| MOV @IX +off,A | 4 | 2 | ((IX) +off) ← (A) | - | - | - | ----- | 46 |
| MOV ext,A | 4 | 3 | (ext) ← (A) | - | - | - | ----- | 61 |
| MOV @EP,A | 3 | 1 | ((EP)) ← (A) | - | - | - | ----- | 47 |
| MOV Ri,A | 3 | 1 | (Ri) ← (A) | - | - | - | ----- | 48 to 4F |
| MOV A,#d8 | 2 | 2 | (A) ← d8 | AL | - | - | ++-- | 04 |
| MOV A,dir | 3 | 2 | (A) ← (dir) | AL | - | - | ++-- | 05 |
| MOV A,@IX +off | 4 | 2 | (A) ← ((IX) +off) | AL | - | - | ++-- | 06 |
| MOV A,ext | 4 | 3 | (A) ← (ext) | AL | - | - | ++-- | 60 |
| MOV A,@A | 3 | 1 | (A) ← ((A)) | AL | - | - | ++-- | 92 |
| MOV A,@EP | 3 | 1 | (A) ← ((EP)) | AL | - | - | ++-- | 07 |
| MOV A,Ri | 3 | 1 | (A) ← (Ri) | AL | - | - | ++-- | 08 to 0F |
| MOV dir,#d8 | 4 | 3 | (dir) ← d8 | - | - | - | ----- | 85 |
| MOV @IX +off,#d8 | 5 | 3 | ((IX) +off) ← d8 | - | - | - | ----- | 86 |
| MOV @EP,#d8 | 4 | 2 | ((EP)) ← d8 | - | - | - | ----- | 87 |
| MOV Ri,#d8 | 4 | 2 | (Ri) ← d8 | - | - | - | ----- | 88 to 8F |
| MOVW dir,A | 4 | 2 | (dir) ← (AH), (dir + 1) ← (AL) | - | - | - | ----- | D5 |
| MOVW @IX +off,A | 5 | 2 | ((IX) +off) ← (AH), ((IX) +off + 1) ← (AL) | - | - | - | ----- | D6 |
| MOVW ext,A | 5 | 3 | (ext) ← (AH), (ext + 1) ← (AL) | - | - | - | ----- | D4 |
| MOVW @EP,A | 4 | 1 | ((EP)) ← (AH), ((EP) + 1) ← (AL) | - | - | - | ----- | D7 |
| MOVW EP,A | 2 | 1 | (EP) ← (A) | - | - | - | ----- | E3 |
| MOVW A,#d16 | 3 | 3 | (A) ← d16 | AL | AH | dH | ++-- | E4 |
| MOVW A,dir | 4 | 2 | (AH) ← (dir), (AL) ← (dir + 1) | AL | AH | dH | ++-- | C5 |
| MOVW A,@IX +off | 5 | 2 | (AH) ← ((IX) +off), (AL) ← ((IX) +off + 1) | AL | AH | dH | ++-- | C6 |
| MOVW A,ext | 5 | 3 | (AH) ← (ext), (AL) ← (ext + 1) | AL | AH | dH | ++-- | C4 |
| MOVW A,@A | 4 | 1 | (AH) ← ((A)), (AL) ← ((A) + 1) | AL | AH | dH | ++-- | 93 |
| MOVW A,@EP | 4 | 1 | (AH) ← ((EP)), (AL) ← ((EP) + 1) | AL | AH | dH | ++-- | C7 |
| MOVW A,EP | 2 | 1 | (A) ← (EP) | - | - | dH | ----- | F3 |
| MOVW EP,#d16 | 3 | 3 | (EP) ← d16 | - | - | - | ----- | E7 |
| MOVW IX,A | 2 | 1 | (IX) ← (A) | - | - | - | ----- | E2 |
| MOVW A,IX | 2 | 1 | (A) ← (IX) | - | - | dH | ----- | F2 |
| MOVW SP,A | 2 | 1 | (SP) ← (A) | - | - | - | ----- | E1 |
| MOVW A,SP | 2 | 1 | (A) ← (SP) | - | - | dH | ----- | F1 |
| MOV @A,T | 3 | 1 | ((A)) ← (T) | - | - | - | ----- | 82 |
| MOVW @A,T | 4 | 1 | ((A)) ← (TH), ((A) + 1) ← (TL) | - | - | - | ----- | 83 |
| MOVW IX,#d16 | 3 | 3 | (IX) ← d16 | - | - | - | ----- | E6 |
| MOVW A,PS | 2 | 1 | (A) ← (PS) | - | - | dH | ----- | 70 |
| MOVW PS,A | 2 | 1 | (PS) ← (A) | - | - | - | ++++ | 71 |
| MOVW SP,#d16 | 3 | 3 | (SP) ← d16 | - | - | - | ----- | E5 |
| SWAP | 2 | 1 | (AH) ↔ (AL) | - | - | AL | ----- | 10 |
| SETB dir: b | 4 | 2 | (dir): b ← 1 | - | - | - | ----- | A8 to AF |
| CLRB dir: b | 4 | 2 | (dir): b ← 0 | - | - | - | ----- | A0 to A7 |
| XCH A,T | 2 | 1 | (AL) ↔ (TL) | AL | - | - | ----- | 42 |
| XCHW A,T | 3 | 1 | (A) ↔ (T) | AL | AH | dH | ----- | 43 |
| XCHW A,EP | 3 | 1 | (A) ↔ (EP) | - | - | dH | ----- | F7 |
| XCHW A,IX | 3 | 1 | (A) ↔ (IX) | - | - | dH | ----- | F6 |
| XCHW A,SP | 3 | 1 | (A) ↔ (SP) | - | - | dH | ----- | F5 |
| MOVW A,PC | 2 | 1 | (A) ← (PC) | - | - | dH | ----- | F0 |

Note: During byte transfer to A, T ← A is restricted to low bytes.

Operands in more than one operand instruction must be stored in the order in which their mnemonics are written. (Reverse arrangement of F²MC-8 family)

Table 3 Arithmetic Operation Instructions (62 instructions)

| Mnemonic | ~ | # | Operation | TL | TH | AH | NZVC | OP code |
|-----------------|----|---|---|----|----|----|--------|----------|
| ADDC A,Ri | 3 | 1 | $(A) \leftarrow (A) + (Ri) + C$ | - | - | - | ++++ | 28 to 2F |
| ADDC A,#d8 | 2 | 2 | $(A) \leftarrow (A) + d8 + C$ | - | - | - | ++++ | 24 |
| ADDC A,dir | 3 | 2 | $(A) \leftarrow (A) + (dir) + C$ | - | - | - | ++++ | 25 |
| ADDC A,@IX +off | 4 | 2 | $(A) \leftarrow (A) + ((IX) + off) + C$ | - | - | - | ++++ | 26 |
| ADDC A,@EP | 3 | 1 | $(A) \leftarrow (A) + ((EP)) + C$ | - | - | - | ++++ | 27 |
| ADDCW A | 3 | 1 | $(A) \leftarrow (A) + (T) + C$ | - | - | dH | ++++ | 23 |
| ADDC A | 2 | 1 | $(AL) \leftarrow (AL) + (TL) + C$ | - | - | - | ++++ | 22 |
| SUBC A,Ri | 3 | 1 | $(A) \leftarrow (A) - (Ri) - C$ | - | - | - | ++++ | 38 to 3F |
| SUBC A,#d8 | 2 | 2 | $(A) \leftarrow (A) - d8 - C$ | - | - | - | ++++ | 34 |
| SUBC A,dir | 3 | 2 | $(A) \leftarrow (A) - (dir) - C$ | - | - | - | ++++ | 35 |
| SUBC A,@IX +off | 4 | 2 | $(A) \leftarrow (A) - ((IX) + off) - C$ | - | - | - | ++++ | 36 |
| SUBC A,@EP | 3 | 1 | $(A) \leftarrow (A) - ((EP)) - C$ | - | - | - | ++++ | 37 |
| SUBCW A | 3 | 1 | $(A) \leftarrow (T) - (A) - C$ | - | - | dH | ++++ | 33 |
| SUBC A | 2 | 1 | $(AL) \leftarrow (TL) - (AL) - C$ | - | - | - | ++++ | 32 |
| INC Ri | 4 | 1 | $(Ri) \leftarrow (Ri) + 1$ | - | - | - | +++- | C8 to CF |
| INCW EP | 3 | 1 | $(EP) \leftarrow (EP) + 1$ | - | - | - | ---- | C3 |
| INCW IX | 3 | 1 | $(IX) \leftarrow (IX) + 1$ | - | - | - | ---- | C2 |
| INCW A | 3 | 1 | $(A) \leftarrow (A) + 1$ | - | - | dH | +- - - | C0 |
| DEC Ri | 4 | 1 | $(Ri) \leftarrow (Ri) - 1$ | - | - | - | +++- | D8 to DF |
| DECW EP | 3 | 1 | $(EP) \leftarrow (EP) - 1$ | - | - | - | ---- | D3 |
| DECW IX | 3 | 1 | $(IX) \leftarrow (IX) - 1$ | - | - | - | ---- | D2 |
| DECW A | 3 | 1 | $(A) \leftarrow (A) - 1$ | - | - | dH | +- - - | D0 |
| MULU A | 19 | 1 | $(A) \leftarrow (AL) \times (TL)$ | - | - | dH | ---- | 01 |
| DIVU A | 21 | 1 | $(A) \leftarrow (T) / (AL), MOD \rightarrow (T)$ | dL | 00 | 00 | ---- | 11 |
| ANDW A | 3 | 1 | $(A) \leftarrow (A) \wedge (T)$ | - | - | dH | ++ R - | 63 |
| ORW A | 3 | 1 | $(A) \leftarrow (A) \vee (T)$ | - | - | dH | ++ R - | 73 |
| XORW A | 3 | 1 | $(A) \leftarrow (A) \nabla (T)$ | - | - | dH | ++ R - | 53 |
| CMP A | 2 | 1 | $(TL) - (AL)$ | - | - | - | ++++ | 12 |
| CMPW A | 3 | 1 | $(T) - (A)$ | - | - | - | ++++ | 13 |
| RORC A | 2 | 1 | $\begin{array}{c} \rightarrow C \rightarrow A \\ \boxed{} \end{array}$ | - | - | - | ++ - + | 03 |
| ROLC A | 2 | 1 | $\begin{array}{c} \boxed{} \\ \leftarrow C \leftarrow A \leftarrow \end{array}$ | - | - | - | ++ - + | 02 |
| CMP A,#d8 | 2 | 2 | $(A) - d8$ | - | - | - | ++++ | 14 |
| CMP A,dir | 3 | 2 | $(A) - (dir)$ | - | - | - | ++++ | 15 |
| CMP A,@EP | 3 | 1 | $(A) - ((EP))$ | - | - | - | ++++ | 17 |
| CMP A,@IX +off | 4 | 2 | $(A) - ((IX) + off)$ | - | - | - | ++++ | 16 |
| CMP A,Ri | 3 | 1 | $(A) - (Ri)$ | - | - | - | ++++ | 18 to 1F |
| DAA | 2 | 1 | Decimal adjust for addition | - | - | - | ++++ | 84 |
| DAS | 2 | 1 | Decimal adjust for subtraction | - | - | - | ++++ | 94 |
| XOR A | 2 | 1 | $(A) \leftarrow (AL) \nabla (TL)$ | - | - | - | ++ R - | 52 |
| XOR A,#d8 | 2 | 2 | $(A) \leftarrow (AL) \nabla d8$ | - | - | - | ++ R - | 54 |
| XOR A,dir | 3 | 2 | $(A) \leftarrow (AL) \nabla (dir)$ | - | - | - | ++ R - | 55 |
| XOR A,@EP | 3 | 1 | $(A) \leftarrow (AL) \nabla ((EP))$ | - | - | - | ++ R - | 57 |
| XOR A,@IX +off | 4 | 2 | $(A) \leftarrow (AL) \nabla ((IX) + off)$ | - | - | - | ++ R - | 56 |
| XOR A,Ri | 3 | 1 | $(A) \leftarrow (AL) \nabla (Ri)$ | - | - | - | ++ R - | 58 to 5F |
| AND A | 2 | 1 | $(A) \leftarrow (AL) \wedge (TL)$ | - | - | - | ++ R - | 62 |
| AND A,#d8 | 2 | 2 | $(A) \leftarrow (AL) \wedge d8$ | - | - | - | ++ R - | 64 |
| AND A,dir | 3 | 2 | $(A) \leftarrow (AL) \wedge (dir)$ | - | - | - | ++ R - | 65 |

(Continued)

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(Continued)

| Mnemonic | ~ | # | Operation | TL | TH | AH | NZVC | OP code |
|------------------|---|---|--|----|----|----|------|----------|
| AND A,@EP | 3 | 1 | $(A) \leftarrow (AL) \wedge (EP)$ | - | - | - | ++R- | 67 |
| AND A,@IX +off | 4 | 2 | $(A) \leftarrow (AL) \wedge ((IX) + \text{off})$ | - | - | - | ++R- | 66 |
| AND A,Ri | 3 | 1 | $(A) \leftarrow (AL) \wedge (Ri)$ | - | - | - | ++R- | 68 to 6F |
| OR A | 2 | 1 | $(A) \leftarrow (AL) \vee (TL)$ | - | - | - | ++R- | 72 |
| OR A,#d8 | 2 | 2 | $(A) \leftarrow (AL) \vee d8$ | - | - | - | ++R- | 74 |
| OR A,dir | 3 | 2 | $(A) \leftarrow (AL) \vee (\text{dir})$ | - | - | - | ++R- | 75 |
| OR A,@EP | 3 | 1 | $(A) \leftarrow (AL) \vee (EP)$ | - | - | - | ++R- | 77 |
| OR A,@IX +off | 4 | 2 | $(A) \leftarrow (AL) \vee ((IX) + \text{off})$ | - | - | - | ++R- | 76 |
| OR A,Ri | 3 | 1 | $(A) \leftarrow (AL) \vee (Ri)$ | - | - | - | ++R- | 78 to 7F |
| CMP dir,#d8 | 5 | 3 | $(\text{dir}) - d8$ | - | - | - | ++++ | 95 |
| CMP @EP,#d8 | 4 | 2 | $(EP) - d8$ | - | - | - | ++++ | 97 |
| CMP @IX +off,#d8 | 5 | 3 | $((IX) + \text{off}) - d8$ | - | - | - | ++++ | 96 |
| CMP Ri,#d8 | 4 | 2 | $(Ri) - d8$ | - | - | - | ++++ | 98 to 9F |
| INCW SP | 3 | 1 | $(SP) \leftarrow (SP) + 1$ | - | - | - | ---- | C1 |
| DECW SP | 3 | 1 | $(SP) \leftarrow (SP) - 1$ | - | - | - | ---- | D1 |

Table 4 Branch Instructions (17 instructions)

| Mnemonic | ~ | # | Operation | TL | TH | AH | NZVC | OP code |
|----------------|---|---|--|----|----|----|---------|----------|
| BZ/BEQ rel | 3 | 2 | If $Z = 1$ then $PC \leftarrow PC + \text{rel}$ | - | - | - | ---- | FD |
| BNZ/BNE rel | 3 | 2 | If $Z = 0$ then $PC \leftarrow PC + \text{rel}$ | - | - | - | ---- | FC |
| BC/BLO rel | 3 | 2 | If $C = 1$ then $PC \leftarrow PC + \text{rel}$ | - | - | - | ---- | F9 |
| BNC/BHS rel | 3 | 2 | If $C = 0$ then $PC \leftarrow PC + \text{rel}$ | - | - | - | ---- | F8 |
| BN rel | 3 | 2 | If $N = 1$ then $PC \leftarrow PC + \text{rel}$ | - | - | - | ---- | FB |
| BP rel | 3 | 2 | If $N = 0$ then $PC \leftarrow PC + \text{rel}$ | - | - | - | ---- | FA |
| BLT rel | 3 | 2 | If $V \vee N = 1$ then $PC \leftarrow PC + \text{rel}$ | - | - | - | ---- | FF |
| BGE rel | 3 | 2 | If $V \vee N = 0$ then $PC \leftarrow PC + \text{rel}$ | - | - | - | ---- | FE |
| BBC dir: b,rel | 5 | 3 | If $(\text{dir: } b) = 0$ then $PC \leftarrow PC + \text{rel}$ | - | - | - | -+--- | B0 to B7 |
| BBS dir: b,rel | 5 | 3 | If $(\text{dir: } b) = 1$ then $PC \leftarrow PC + \text{rel}$ | - | - | - | -+--- | B8 to BF |
| JMP @A | 2 | 1 | $(PC) \leftarrow (A)$ | - | - | - | ---- | E0 |
| JMP ext | 3 | 3 | $(PC) \leftarrow \text{ext}$ | - | - | - | ---- | 21 |
| CALLV #vct | 6 | 1 | Vector call | - | - | - | ---- | E8 to EF |
| CALL ext | 6 | 3 | Subroutine call | - | - | - | ---- | 31 |
| XCHW A,PC | 3 | 1 | $(PC) \leftarrow (A), (A) \leftarrow (PC) + 1$ | - | - | dH | ---- | F4 |
| RET | 4 | 1 | Return from subroutine | - | - | - | ---- | 20 |
| RETI | 6 | 1 | Return from interrupt | - | - | - | Restore | 30 |

Table 5 Other Instructions (9 instructions)

| Mnemonic | ~ | # | Operation | TL | TH | AH | NZVC | OP code |
|----------|---|---|-----------|----|----|----|-------|---------|
| PUSHW A | 4 | 1 | | - | - | - | ---- | 40 |
| POPW A | 4 | 1 | | - | - | dH | ---- | 50 |
| PUSHW IX | 4 | 1 | | - | - | - | ---- | 41 |
| POPW IX | 4 | 1 | | - | - | - | ---- | 51 |
| NOP | 1 | 1 | | - | - | - | ---- | 00 |
| CLRC | 1 | 1 | | - | - | - | ----R | 81 |
| SETC | 1 | 1 | | - | - | - | ----S | 91 |
| CLRI | 1 | 1 | | - | - | - | ---- | 80 |
| SETI | 1 | 1 | | - | - | - | ---- | 90 |

INSTRUCTION MAP

| L | H | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
|---|-------------|-------------|--------------|--------------|-------------|-------------|-------------|-------------|------------|---------------|---------------|-------------|----------------|--------------|--------------|--------------|-----------|
| 0 | NOP | SWAP | RET | RETI | PUSHW A | PUSHW A | POPW A | MOV A,ext | MOVW A,PS | CLR | SETI | CLRB dir: 0 | BBC dir: 0,rel | INCW A | DECW A | JMP @A | MOVW A,PC |
| 1 | MULU A | DIVU A | JMP addr16 | CALL addr16 | PUSHW IX | PUSHW IX | POPW PS,A | MOV ext,A | MOVW PS,A | CLRC | SETC | CLRB dir: 1 | BBC dir: 1,rel | INCW SP | DECW SP | MOVW SPA | MOVW A,SP |
| 2 | ROLC A | CMP A | ADDC A | SUBC A | XCH A,T | XCH A,T | XOR A | AND A | OR A | MOV @A,T | MOV A,@A | CLRB dir: 2 | BBC dir: 2,rel | INCW IX | DECW IX | MOVW IX,A | MOVW A,IX |
| 3 | RORC A | CMPW A | ADDCW A | SUBCW A | XCHW A,T | XCHW A,T | XORW A | ANDW A | ORW A | MOVW @A,T | MOVW A,@A | CLRB dir: 3 | BBC dir: 3,rel | INCW EP | DECW EP | MOVW EPA | MOVW A,EP |
| 4 | MOV A,#d8 | CMP A,#d8 | ADDC A,#d8 | SUBC A,#d8 | XOR A,#d8 | XOR A,#d8 | XOR A,#d8 | AND A,#d8 | OR A,#d8 | DAA | DAS | CLRB dir: 4 | BBC dir: 4,rel | MOVW A,ext | MOVW ext,A | MOVW A,#d16 | XCHW A,PC |
| 5 | MOV A,dir | CMP A,dir | ADDC A,dir | SUBC A,dir | XOR A,dir | MOV dir,A | XOR A,dir | AND A,dir | OR A,dir | MOV dir,#d8 | CMP dir,#d8 | CLRB dir: 5 | BBC dir: 5,rel | MOVW A,dir | MOVW dir,A | MOVW SP,#d16 | XCHW A,SP |
| 6 | MOV A,@IX+d | CMP A,@IX+d | ADDC A,@IX+d | SUBC A,@IX+d | XOR A,@IX+d | MOV @IX+d,A | XOR A,@IX+d | AND A,@IX+d | OR A,@IX+d | MOV @IX+d,#d8 | CMP @IX+d,#d8 | CLRB dir: 6 | BBC dir: 6,rel | MOVW A,@IX+d | MOVW @IX+d,A | MOVW IX,#d16 | XCHW A,IX |
| 7 | MOV A,@EP | CMP A,@EP | ADDC A,@EP | SUBC A,@EP | XOR A,@EP | MOV @EPA | XOR A,@EP | AND A,@EP | OR A,@EP | MOV @EP,#d8 | CMP @EP,#d8 | CLRB dir: 7 | BBC dir: 7,rel | MOVW A,@EP | MOVW @EPA | MOVW EP,#d16 | XCHW A,EP |
| 8 | MOV A,R0 | CMP A,R0 | ADDC A,R0 | SUBC A,R0 | XOR R0,A | MOV R0,A | XOR A,R0 | AND A,R0 | OR A,R0 | MOV R0,#d8 | CMP R0,#d8 | SETB dir: 0 | BBS dir: 0,rel | INC R0 | DEC R0 | CALLV #0 | BNC rel |
| 9 | MOV A,R1 | CMP A,R1 | ADDC A,R1 | SUBC A,R1 | MOV R1,A | MOV A,R1 | XOR A,R1 | AND A,R1 | OR A,R1 | MOV R1,#d8 | CMP R1,#d8 | SETB dir: 1 | BBS dir: 1,rel | INC R1 | DEC R1 | CALLV #1 | BC rel |
| A | MOV A,R2 | CMP A,R2 | ADDC A,R2 | SUBC A,R2 | MOV R2,A | MOV A,R2 | XOR A,R2 | AND A,R2 | OR A,R2 | MOV R2,#d8 | CMP R2,#d8 | SETB dir: 2 | BBS dir: 2,rel | INC R2 | DEC R2 | CALLV #2 | BP rel |
| B | MOV A,R3 | CMP A,R3 | ADDC A,R3 | SUBC A,R3 | MOV R3,A | MOV A,R3 | XOR A,R3 | AND A,R3 | OR A,R3 | MOV R3,#d8 | CMP R3,#d8 | SETB dir: 3 | BBS dir: 3,rel | INC R3 | DEC R3 | CALLV #3 | BN rel |
| C | MOV A,R4 | CMP A,R4 | ADDC A,R4 | SUBC A,R4 | MOV R4,A | MOV A,R4 | XOR A,R4 | AND A,R4 | OR A,R4 | MOV R4,#d8 | CMP R4,#d8 | SETB dir: 4 | BBS dir: 4,rel | INC R4 | DEC R4 | CALLV #4 | BNZ rel |
| D | MOV A,R5 | CMP A,R5 | ADDC A,R5 | SUBC A,R5 | MOV R5,A | MOV A,R5 | XOR A,R5 | AND A,R5 | OR A,R5 | MOV R5,#d8 | CMP R5,#d8 | SETB dir: 5 | BBS dir: 5,rel | INC R5 | DEC R5 | CALLV #5 | BZ rel |
| E | MOV A,R6 | CMP A,R6 | ADDC A,R6 | SUBC A,R6 | MOV R6,A | MOV A,R6 | XOR A,R6 | AND A,R6 | OR A,R6 | MOV R6,#d8 | CMP R6,#d8 | SETB dir: 6 | BBS dir: 6,rel | INC R6 | DEC R6 | CALLV #6 | BGE rel |
| F | MOV A,R7 | CMP A,R7 | ADDC A,R7 | SUBC A,R7 | MOV R7,A | MOV A,R7 | XOR A,R7 | AND A,R7 | OR A,R7 | MOV R7,#d8 | CMP R7,#d8 | SETB dir: 7 | BBS dir: 7,rel | INC R7 | DEC R7 | CALLV #7 | BLT rel |

MB89120/120A Series

■ MASK OPTIONS

| No. | Part number | MB89121 MB89123A MB89125A | MB89P131 MB89P133A | MB89P135A | MB89PV130A |
|-----|--|---------------------------------|--|---------------------------|--|
| | Specifying procedure | Specify when ordering masking | | Set with EPROM programmer | Specification impossible |
| 1 | Pull-up resistors <ul style="list-style-type: none"> • P00 to P07, P10 to P17, • P30 to P37, P40 to P43 | Selectable by pin | Selectable by pin (P40 to P43 must be set to without a pull-up resistor.) | | All pins fixed to no pull-up resistor optional |
| 2 | Power-on reset <ul style="list-style-type: none"> • Power-on reset provided • No power-on reset | Selectable | Selectable | Selectable | With power-on reset |
| 3 | Selection of oscillation stabilization wait time <ul style="list-style-type: none"> • The oscillation stabilization wait time initial value is selectable from 4 types given below. 0 : Oscillation stabilization $2^2/F_{CH}$ 1 : Oscillation stabilization $2^{12}/F_{CH}$ 2 : Oscillation stabilization $2^{16}/F_{CH}$ 3 : Oscillation stabilization $2^{18}/F_{CH}$ | Selectable | Selectable | Selectable | Oscillation stabilization $2^{18}/F_{CH}$ |
| 4 | Reset pin output <ul style="list-style-type: none"> • Reset output provided • No reset output | Selectable | Selectable | Selectable | With reset output |
| 5 | Clock mode selection <ul style="list-style-type: none"> • Single-clock mode • Dual-clock mode | Selectable | Selectable | Selectable | Dual-clock mode |
| 6 | Main clock oscillation circuit type <ul style="list-style-type: none"> • External clock input • Oscillation resonator | Selectable | Not required*1 | | |
| 7 | Peripheral control clock output function*2 <ul style="list-style-type: none"> • Not used • Used | Selectable | Not required*3 | | |

*1 : Both external clock and oscillation resonator is usable on the one-time product.

*2 : "Used" must be selected when P33 (39 pin) is used as SCO for the peripheral control clock output.

*3 : The peripheral control clock function can be used only by software.

MB89120/120A Series

■ MB89P131/P133A STANDARD OPTIONS

| No. | Product option | MB89P131-101 | MB89P133A-201 |
|-----|---|---|---|
| 1 | Pull-up resistor | Not provided for any port | Not provided for any port |
| 2 | Power-on reset | Provided | Provided |
| 3 | Selection of oscillation stabilization time | 2 : Oscillation stabilization $2^{16}/F_{CH}$ | 2 : Oscillation stabilization $2^{16}/F_{CH}$ |
| 4 | Reset pin output | Provided | Provided |
| 5 | Clock mode selection | Dual-clock mode | Dual-clock mode |

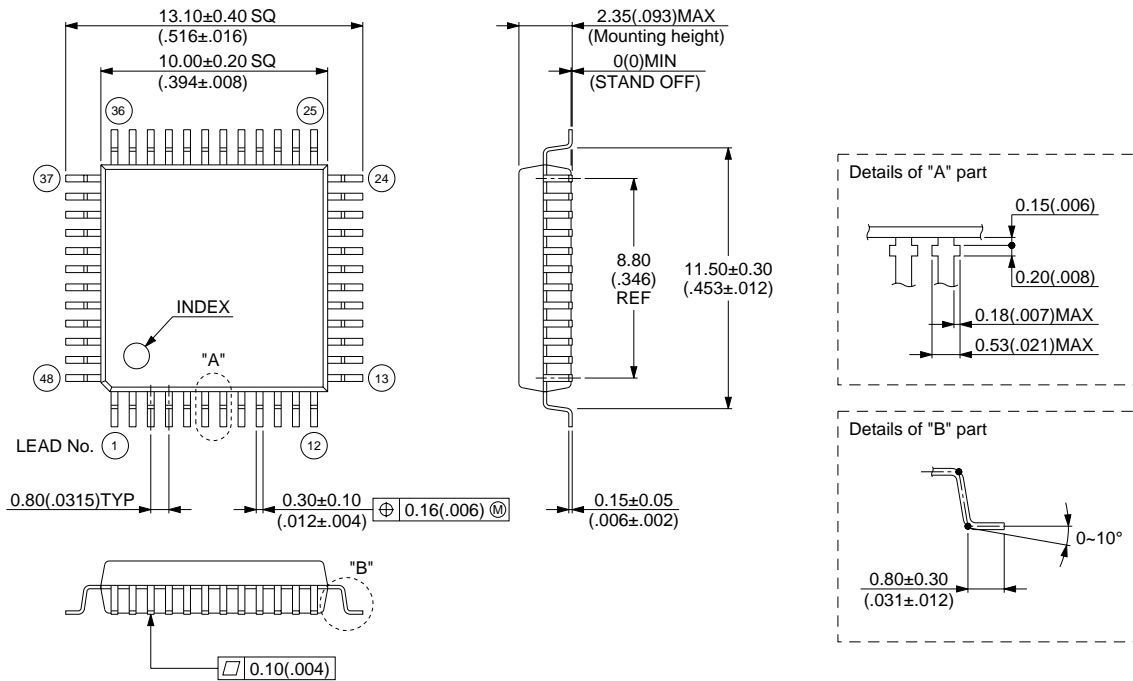
■ ORDERING INFORMATION

| Part number | Package | Remarks |
|---|--------------------------------------|---------|
| MB89121PFM MB89123APFM MB89125APFM | 48-pin Plastic QFP (FPT-48P-M13) | |
| MB89P131PFM-101 MB89P133APFM-201 MB89P135APFM | | |
| MB89PV130ACF-ES | 48-pin Ceramic MQFP (MQP-48C-P01) | |

MB89120/120A Series

■ PACKAGE DIMENSION

48-pin Plastic QFP
(FPT-48P-M13)



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Dimensions in mm (inches)

MB89120/120A Series

FUJITSU LIMITED

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