

TM417-A878: August 1987

DESCRIPTION

The Fujitsu MB89395 is a highly integrated peripheral device for MBL8086/8088 (or equivalents) 16-bit microprocessors. The MB89395 integrates the most common MBL8086/8088 (or equivalents) system components - a bus controller (MB89288 equivalent), an interrupt controller (MB89259A equivalent), a DMA controller (MB89237A equivalent), an interval timer (MB89254 equivalent), etc. With only external address latches (MB89282/3 or equivalents), data transceivers (MB89286/7 or equivalents), and a clock generator (MB89284A or equivalent), the MB89395 can realize a compact 8086/8088 microprocessor system.

The MB89395 is suitable for OA (Office Automation) applications, such as personal computers, word processors, etc. It is especially effective for system integration of MBL8086/8088 microprocessor based system. The address assignment of the on-chip resources are compatible with IBM™ PC/XT™ system, as well as the MB89393.

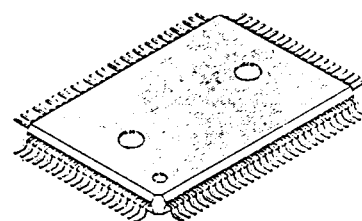
The MB89395 was designed with building block method using hardware macrocells equivalent to the MB89200 Series CMOS peripheral LSI devices. It is fabricated with the single polysilicon and double metal layered CMOS technology, and packaged in a 100-pin plastic flatpack. The MB89395 operates with a single +5V power supply up to 8MHz over the temperature range from 0°C to 70°C.

FEATURES

- High Integration Peripheral LSI:
 - Bus controller (MB89288 equivalent)
 - Interrupt Controller (MB89259A Equivalent)
 - DMA Controller (MB89237A Equivalent)
 - IntervalTimer (MB89254 Equivalent)
 - DMA Page Register
- IBM™ PC/XT™ Compatible Address Assignment for On-Chip Resources
- Connectable to MBL8086/8088 or Equivalents
- Operatable up to 8MHz
- Low Power Dissipation
- Single +5V Power Supply
- CMOS Process
- 100-Pin Plastic Flatpack

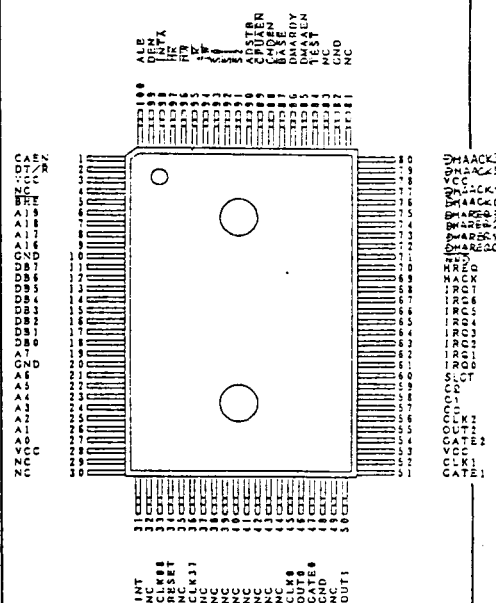
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MB89395PF



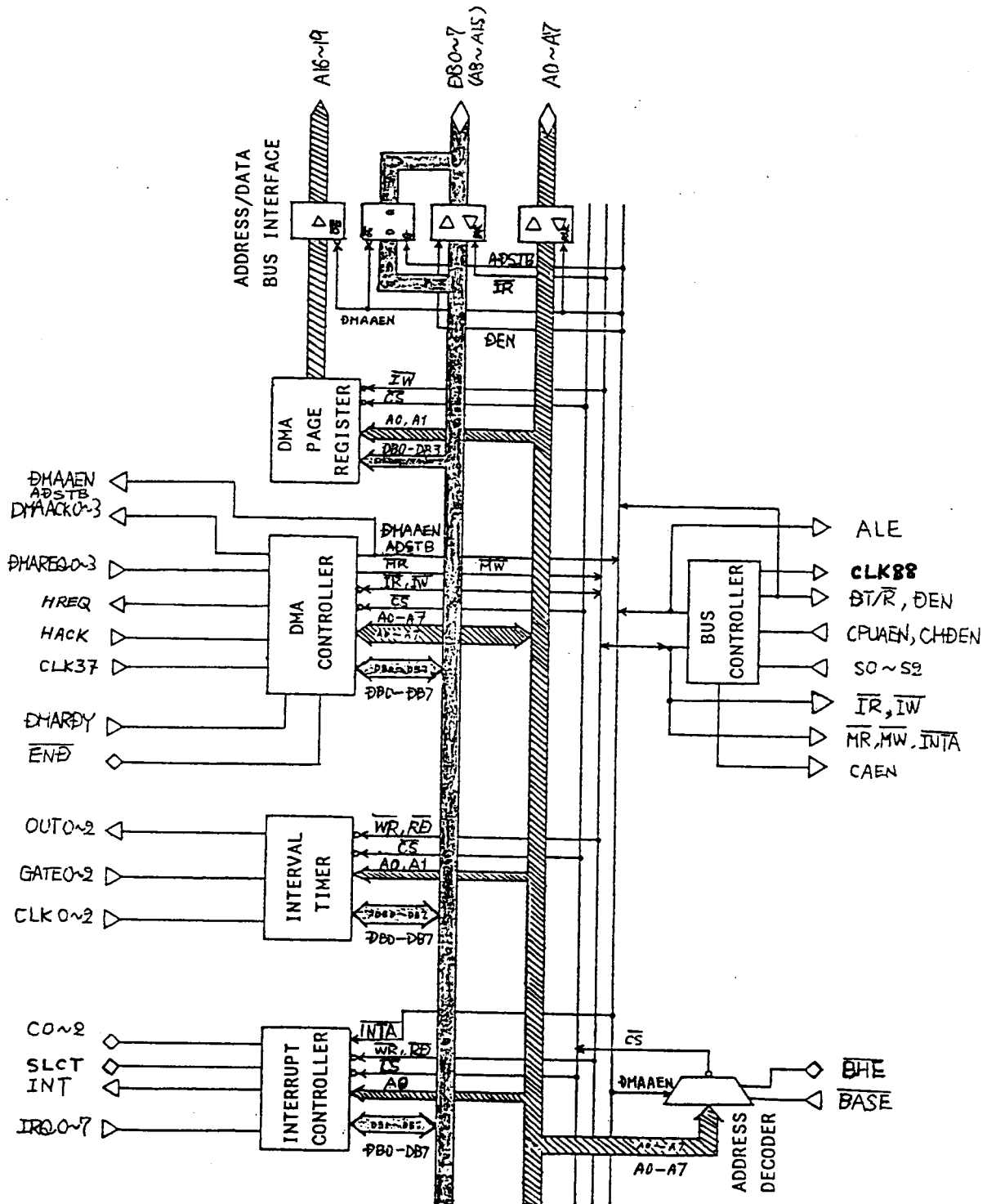
100-PIN PLASTIC FLATPACK
FPT-100P-M01

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

BLOCK DIAGRAM



PIN DESCRIPTION

Power Supply Related Pins

Symbol	Pin No.	Pin Name	I/O	Description
VCC	3,28, 53,78	-	-	+5Vdc power supply pin.
GND	10,20, 48,82	-	-	Ground pin.

Device Control Pins

Symbol	Pin No.	Pin Name	I/O	Description
RESET	34	Reset	I	Reset input (active high) from an external reset circuit: A high level on RESET initializes each of the internal functional blocks of the MB89395.
$\overline{\text{TEST}}$	84	Test	I	Test input (active low): A low level on $\overline{\text{TEST}}$ makes the device enter a test mode, which is used for the shipping test purpose only at Fujitsu. In the normal operation mode, this pin must be pulled up or open. This pin contains a pullup resistor.

Address Decoder Related Pins

Symbol	Pin No.	Pin Name	I/O	Description
$\overline{\text{BASE}}$	87	MB89395 Chip Select	I	Select input (active low) from the CPU: A low level on $\overline{\text{BASE}}$ selects MB89395 as an I/O device. This signal should be generated by decoding only address outputs (normally A15-A8) from the CPU.
$\overline{\text{BHE}}$	5	Byte High Enable	O	Status output (active low): In the idle mode $\overline{\text{BHE}}$ is in high impedance state. In the DMA, $\overline{\text{BHE}}$ is activated only when in the internal DMA accesses odd addresses.

PIN DESCRIPTION

Address Bus and Data Bus Interface Pins

Symbol	Pin No.	Pin Name	I/O	Description
A19-A16	6-9	Address Bus	0	Address outputs: In the idle mode, these pins are in high impedance state. In the DMA mode, they output higher 4 bits (A19-A16) of DMA address programmed for each channel in the DMA page register.
DB7-DB0 (A15-A8)	11-18	Data Bus (Address Bus)	I/O	These pins have dual functions: In the idle mode, these pins are configured as bidirectional 8-bit data bus (DB7-DB0) for the CPU to access MB89395's internal registers. In the DMA mode, these pins function as DMA address outputs, and output middle 8 bits (A15-A8) of DMA address programmed for each channel in the DMA controller.
A7-A0	19,21-27	Address Bus	I/O	These pins have dual functions: In the idle mode, these pins are configured as 8-bit address bus inputs (A7-A0) for the CPU to access MB89395's internal registers. In the DMA mode, these pins function as DMA address outputs, and output lower 8 bits (A7-A0) of DMA address programmed for each channel in the DMA controller.

PIN DESCRIPTION

Bus Controller Related Pins

Symbol	Pin No.	Pin Name	I/O	Description
CLK88	33	Clock for Bus Controller	I	Clock input from an external clock generator to the internal bus controller block of the MB89395.
$\overline{S2-S0}$	91-93	Status	I	Status inputs ($\overline{S2-S0}$) from the CPU (MBL8086/8088 or equivalents). MB89393 decodes $\overline{S2-S0}$ signals, and issues command ($\overline{IR}$, $\overline{IW}$, $\overline{MR}$, $\overline{MW}$, and $\overline{INTA}$) and control (ALE, $\overline{DT/R}$, and $\overline{DEN}$) signals for external I/O devices and memory devices located on the system bus. These pins contains pull-up resistors.
$\overline{IR}$	95	I/O Read	0	Read strobe output (active low) to external I/O devices located on the system bus.
$\overline{IW}$	94	I/O Write	0	Write strobe output (active low) to external I/O devices located on the system bus.
$\overline{MR}$	97	Memory Read	0	Read strobe output (active low) to external memory devices located on the system bus.
$\overline{MW}$	96	Memory Write	0	Write strobe output (active low) to external memory devices located on the system bus.
$\overline{INTA}$	98	Interrupt Acknowledge	0	Acknowledge output (active low) to an external I/O device or interrupt controller device (MB89259A or equivalent) which is requesting the interrupt service: A low level indicates the CPU has acknowledged the interrupt request and tells the interrupting device should issue an interrupt vector address to the system data bus.
ALE	100	Address Latch Enable	0	Address strobe output to external address latches located between the local bus and system bus: At the rising edge, the address latches capture address on the address/data multiplexed lines of the local bus. In the DMA mode, the ALE pin is in high-Z state during DMAEN period.

PIN DESCRIPTION

Bus Controller Related Pins (Continued)

Symbol	Pin No.	Pin Name	I/O	Description
DT/ $\bar{R}$	2	Data Trans- mit/Receive	0	Directional control output to external data transceivers located between the local bus and the system bus: A high level on DT/$\bar{R}$ indicates the CPU transmits (writes) data to I/O or memory devices located on the system data bus. A low level indicates the CPU receives (reads) data from I/O or memory devices. In the DMA mode, a low level is output during $\bar{I}R$ active, and a high level is output during $\bar{I}R$ inactive.
DEN	99	Data Enable	0	Enable output (active high) to external data transceivers located between the local bus and the system bus: A high level on DEN serves to enable the transreceives.
CAEN	1	Cascade Address Enable	0	Enable output (active high), which becomes active during an interrupt acknowledge sequence: A high level on CAEN serves to enable a cascade address, which is issued by a master interrupt controller, on the local bus.
$\overline{CPUAEN}$	89	Address Enable	I	Enable input (active low) for the command outputs ($\bar{I}R$, $\bar{I}W$, $\bar{M}R$, $\bar{M}W$, and $\bar{I}NTA$): A low level on $\overline{CPUAEN}$ enables I/O command ($\bar{I}R$ and $\bar{I}W$) and Memory command ($\bar{M}R$ and $\bar{M}W$) outputs. Reversely, a high level forces I/O command and Memory command outputs in high impedance state. $\overline{CPUAEN}$ input is provided for the CPU to access the multi-master system bus. In the multi-master system configuration, $\overline{CPUAEN}$ input is provided from the bus arbiter (MB89289 or equivalent). In non multi-master bus configuration, $\overline{CPUAEN}$ is grounded.
CMDEN	88	Command Enable	I	Enable input (active high) for the command outputs ($\bar{I}R$, $\bar{I}W$, $\bar{M}R$, $\bar{M}W$, and $\bar{I}NTA$) and DEN control output: A high level on CMDEN enables all command and DEN control outputs. A low level deactivates them.

PIN DESCRIPTION

Interrupt Controller Related Pins

Symbol	Pin No.	Pin Name	I/O	Description
IRQ7-0	68-61	Interrupt Request	I	Interrupt request inputs from external I/O devices: In the edge-trigger mode, the interrupt request is processed at the rising of IRQ, while in the level-trigger mode, the interrupt request is executed by a high level on IRQ. In both modes, IRQ inputs must be held high until the acknowledge signal (an $\overline{INTA}$ negative pulse) from the CPU. The mode selection for the above interrupt request must be made in the MB89395's initialize sequence.
INT	31	Interrupt	O	Interrupt output (active high) to the CPU: A high level is output on INT whenever interrupt inputs is applied on IRQ.
C2-0	59-57	Cascade Line	I/O	These lines are used to cascade MB89395's (MB89259A's). Through these lines a master MB89395 designates slave MB89395s (MB89259As). The master's C lines are outputs, and slave's C lines are outputs.
SLCT	60	Slave Program/Enable Buffer	I/O	In the normal mode, SLCT is used as a select input to designate either master MB89395 (SLCT=High) or slave MB89395 (MB89259A) (SLCT=Low). In the buffer mode, SLCT is used as a control output to external buffer transceivers.

PIN DESCRIPTION

DMA Controller Related Pins

Symbol	Pin No.	Pin Name	I/O	Description
CLK37	36	Clock for DMA Controller	I	Clock input from an external clock generator to the internal DMA controller block of the MB89395.
ADSTB	90	Address Strobe	O	Address strobe output (active high) to the internal DMA address latch. ADSTB signal is issued during the DMA transfer cycle. Normally this signal is not used externally.
DMAAEN	85	DMA Address Enable	O	Enable output (active high) to an external address latch. DMAAEN enables the address latch to output upper 8 bits of DMA address onto the system address bus. During the DMA transfer cycle, DMAAEN is in a high level to inhibit the address latch.
DMARDY	86	DMA Ready	I	Ready input (active high) to indicate one DMA transfer cycle has completed: While DMARDY is inactive, MB89395 continues to stay in the wait state and expands read/write pulses. This feature is useful when low speed memory and I/O devices are used. For proper operation, DMARDY signal must be kept unchanged during the setup and hold times.
$\overline{\text{END}}$	71	End of Process	I/O	DMA terminate input/output (active low): A low level on END pin during DMA transfer cycle terminates the DMA service. When a DMA service completes (i.e., a programmed DMA transfer count = terminal count (TC) is reached.), a negative pulse is issued on END pin. Occurrence of either external or internal END resets the request, and loads the base register contents into the corresponding current register if the auto-initialization is enabled. The mask bit and the TC bit in the status register remains cleared if the auto-initialization is enabled. Otherwise, they are set for the channel on which the END occurred. This pin has an open drain output buffer, which requires an external pull up resistor.

PIN DESCRIPTION

DMA Controller Related Pins (Continued)

Symbol	Pin No.	Pin Name	I/O	Description
HREQ	70	Hold Request	O	Hold request output (active high) to the CPU for getting the system bus control: HREQ signal is issued, if a DMA request mask bit remains cleared, when the corresponding DMA request signal (DREQx) is activated. At least one clock cycle is required for HACK signal to become active after HREQ has been issued.
HACK	69	Hold Acknowledge	I	Acknowledge input (active high) from the CPU to indicate that the CPU has accepted the hold request (HREQ) issued by the MB89395.
DMAREQ 3-0	75-72	DMA Request	I	DMA service request inputs from external peripheral devices: DMAREQ3-0 inputs corresponds to DMA channels 0-3, and each of them are independent. DMA request is made by activating DMAREQ line and acceptance of the request is acknowledged by DMAACK activated. For proper operation, DMAREQ input must be kept active until the corresponding DMAACK output is activated. The active level of these pins are programmable by software.
DMAACK 3-0	80-76	DMA Acknowledge	O	Acknowledge output to DMA service requesting peripheral devices: DMAACK signal notifies the device of MB89395's acceptance of the request. The active level of this pin is programmable by software, and initialized as active low.

PIN DESCRIPTION

Interval Timer Related Pins

Symbol	Pin No.	Pin Name	I/O	Description
CLK2-0	56,52,45	Clock In	I	Clock pulse inputs to the counters 2-0.
GATE2-0	54,51,47	Gate In	I	Control inputs to the counters 2-0.
OUT2-0	55,50,46	Count Out	O	Outputs from the counters 2-0.

Other Pins

Symbol	Pin No.	Pin Name	I/O	Description
NC	4,29,30, 32,35,37, 44,49,81, 83,	No Connection	-	No connection.

FUNCTIONAL DESCRIPTION

The MB89395 integrates the most common MBL8086/8088 (or equivalents) system components - Bus Controller, Interrupt Controller, DMA Controller, DMA Page Register, Interval Timer and so on. All functional blocks except the address decoder, address/data bus interface, DMA page registers are equivalent to MB89200 Series devices. The interrupt controller, DMA controller, DMA page register and interval timer are programmable by software, and their internal register organization is the same as the equivalent MB89200 Series devices. However, there are some unprogrammable parameters in part of the registers because some functional block's operation mode is fixed. The internal registers of each functional block are mapped onto the I/O space of the CPU through the on-chip address decoder, as shown below.

Address Assignments

Functional Block	Equivalent	Address								
		BASE	A7	A6	A5	A4	A3	A2	A1	A0
Address Decoder	-	Not programmable								
Address and Data Bus Interface	-	Not programmable								
Bus Controller	MB89288	Not programmable								
Interrupt Controller	MB89259A	0	0	0	1	X	X	X	X	0 1
DMA Controller	MB89237A	0	0	0	0	X	0	0	0	0
							:	:	:	:
							:	:	:	:
							1	1	1	1
DMA Page Register	-	0	1	0	0	X	X	X	0	0
									0	1
									1	0
									1	1
Interval Timer	MB89254	0	0	1	0	X	X	X	0	0
									0	1
									1	0
									1	1

FUNCTIONAL DESCRIPTION

FUNCTIONAL BLOCK DESCRIPTION

Address Decoder

This block is designed for MB89395. This block decodes address to generate internal chip select signal and BHE signal.

Address and Data Bus Interface

The MB89395 has two operating modes - Idle Mode and DMA Mode. The Idle Mode is for CPU to access MB89395's internal registers, and in this mode address/data bus is configured as 8-bit address (A7-A0) and 8-bit data (DB7-DB8) lines. The DMA Mode is for DMA transfer, and in this mode address/data bus is configured as 20-bit DMA address (A19-A16, DB7-DB0, and A7-A0) lines.

Bus Controller

This block is functionally compatible with MB89288, but the operation mode is fixed at the single bus mode.

Interrupt Controller

This block is functionally compatible with MB89259A, except that this block has no 8080/8085 mode. The register setting for this block must be made as 8086/8088 mode.

DMA Controller

This block is functionally compatible with MB89237A, except that this block doesn't provide memory-to-memory transfer capability.

DMA Page Register

This block is designed for MB89395. This consists of four 4-bit write-only registers each of which holds higher 4 bits (A19-A16) of DMA address for each channel. The register contents are output on A19-A16 pins during the DMA mode (i.e., during DACK active). This register is cleared by reset (i.e., RESET active).

Interval Timer

This block is functionally compatible with MB89254.

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Remark
Power Supply Voltage	VCC	GND-3.0 to +7.0	V	
Input Voltage	VIN	GND-0.3 to +7.0	V	Should not exceed VCC+0.3V.
Output Voltage	VOU _T	GND-0.3 to +7.0	V	Should not exceed VCC+0.3V.
Operating Temperature	T _A	0 to +70	°C	
Storage Temperature	T _{STG}	-55 to +150	°C	

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Remark
		Min.	Typ.	Max.		
Power Supply Voltage	VCC	4.5	5.0	5.5	V	
	GND	0			V	
Operating Temperature	T _A	0		+70	°C	

DC CHARACTERISTICS (VCC = +5V±10%, GND = 0V; TA = 0°C to +70°C)

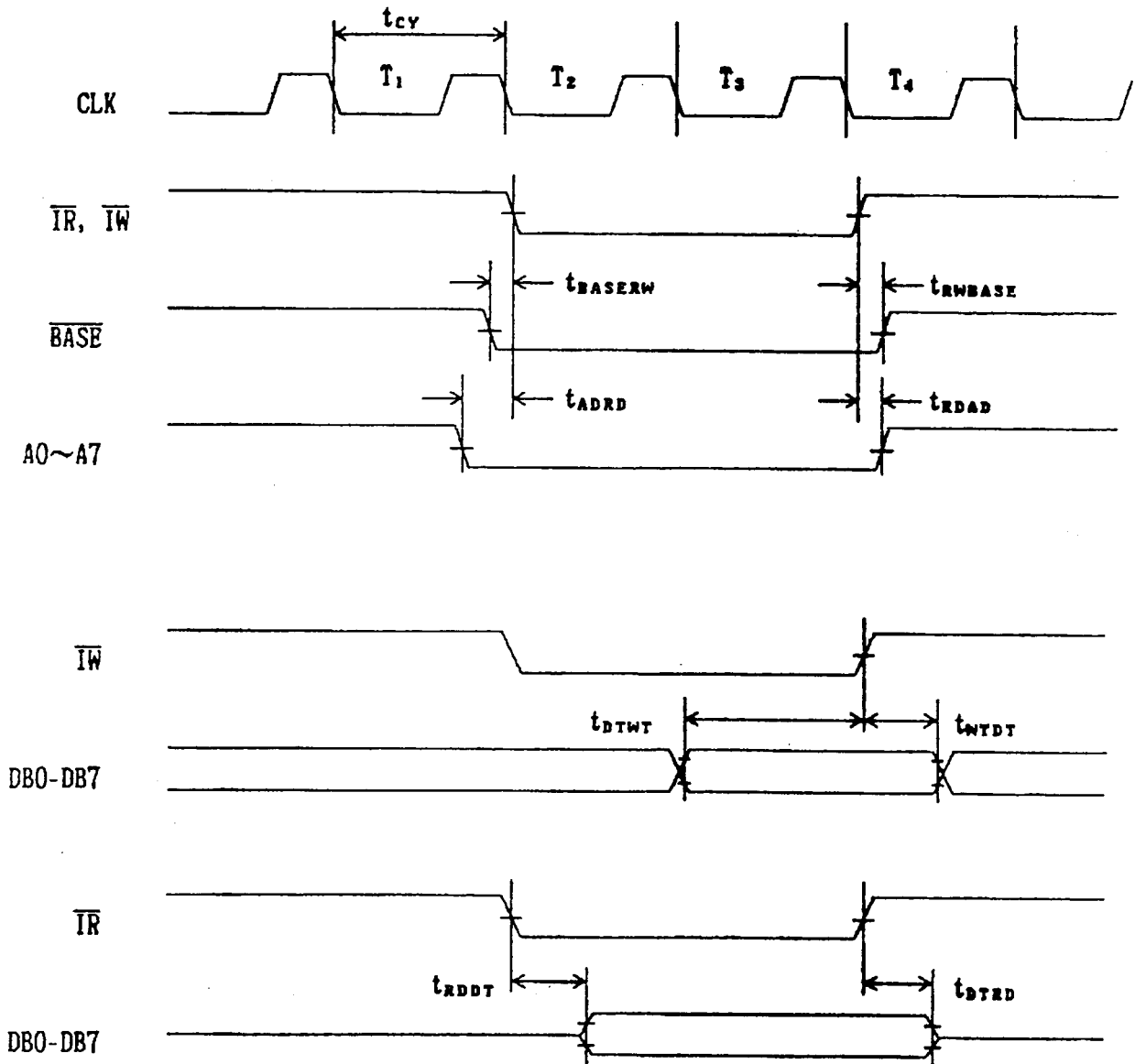
Parameter	Symbol	Value			Unit	Conditions
		Min.	Typ.	Max.		
Input Low Voltage	VIL	GND -0.3		0.8	V	
Input High Voltage (Except RESET)	VIH1	2.2		VCC +0.3	V	
Input High Voltage (RESET)	VIH2	4.0			V	
Output High Voltage (MR, MW, IR, IW, INTA)	VOL1			0.4	V	IOL = 8.0mA
Output High Voltage (Other Outputs)	VOL2			0.4	V	IOL = 2.0mA
Output High Voltage (MR, MW, IR, IW, INTA)	VOH1	3.4			V	IOH = -2.0mA
Output High Voltage (CLK)	VOH2	3.4			V	IOH = -0.4mA
Input Leakage Current	IILK	-10		+10	μA	VIN = GND to VCC
Output Leakage Current	IOFL	-10		+10	μA	VIN = 0.45V to VCC
Load Characteristics of Pulled Up Inputs	ILIR			-300	μA	VIN = GND
				+10	μA	VIN = VCC
Power Supply Current	ICC			30	mA	

AC CHARACTERISTICS (VCC = +5V±10%, GND = 0V; TA = 0°C to +70°C)

Bus Interface Timing (Read/Write Timing)

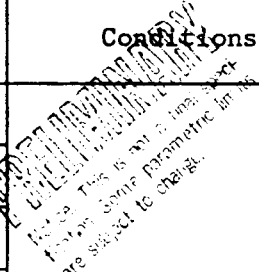
Parameter	Symbol	Value			Unit	Conditions
		Min.	Typ.	Max.		
Clock Cycle Time	tCY				ns	
BASE Setup Time (BASE↓ to IR/IW↓)	tBASERW	10			ns	
BASE Hold Time	tRWBASE	0			ns	
Address Setup Time (Addr Valid to IR/IW↓)	tADRD	30			ns	
Address Hold Time	tRDAD	0			ns	
Data Setup Time	tDTWT	50			ns	
Data Hold Time	tWTDT	20			ns	
Access Time (IR↓ to Data Valid)	tRDDT			tCYx2/3 +50	ns	
Data Bus Float Time (IR↑ to DB Float)	tDTRD	5		50	ns	

Bus Interface Timing



AC CHARACTERISTICS (VCC = +5V±10%, GND = 0V; TA = 0°C to +70°C)

Bus Controller Timing

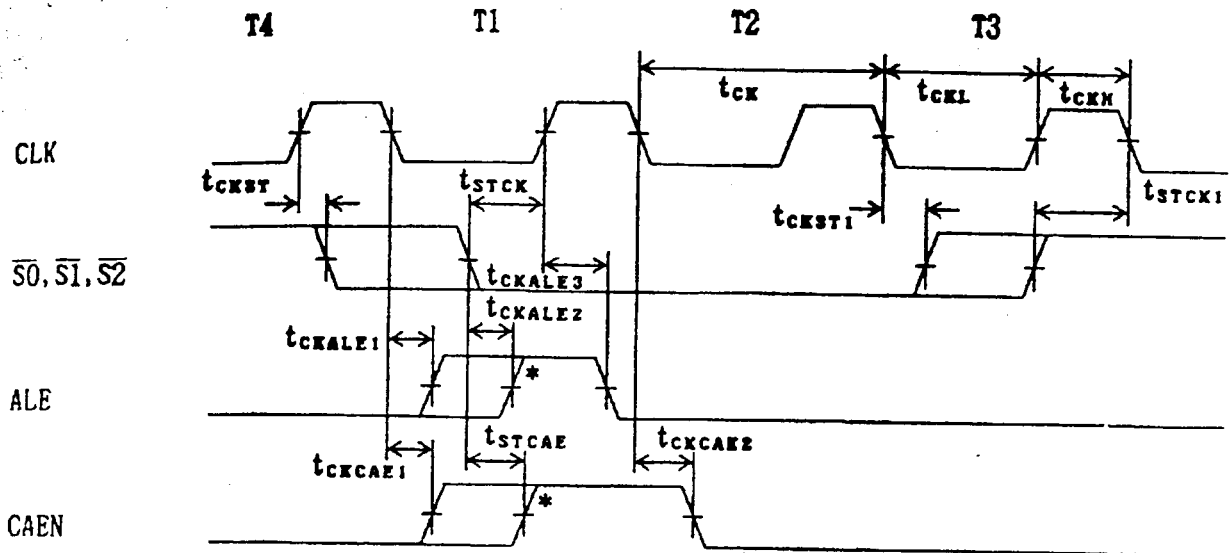
Parameter	Symbol	Value			Unit	Conditions
		Min.	Typ.	Max.		
Setup Status Active Time	tSTCK	35			ns	 This is not a final spec. All parameters are subject to change.
Hold Status Active Time	tCKST	10			ns	
Setup Status Inactive Time	tSTCK1	35			ns	
Hold Status Inactive Time	tCKST1	10			ns	
Control Active Delay	tCKCTR	5		45	ns	
Control Inactive Delay	tCKCAE2	10		45	ns	
ALE High Pulse Width	tALEH	Note				
ALE Active Delay1	tCKALE1			30	ns	
ALE Active Delay2	tCKALE2			35	ns	
ALE Active Delay3	tCKALE3	4		25	ns	
CAEN Active Delay1	tCKCAE1			30	ns	
CAEN Active Delay2	tSTCAE			35	ns	
Command Active Delay	tCKCMD1	5		35	ns	
Command Inactive Delay	tCKCMD2	5		35	ns	
DT/ $\overline{R}$ Active Delay	tCKDTR1			50	ns	
DT/ $\overline{R}$ Inactive Delay	tCKDTR2			30	ns	
Command Enable Time	tAENCMD1			40	ns	
Command Delay Time	tAENCMD2	90		250	ns	
Command Disable Time	tAENCMD3			40	ns	
$\overline{AEN} \rightarrow DEN$	tAENDEN			35	ns	
CMDEN $\rightarrow$ DEN, IOEN	tCMDECTR			35	ns	
CMDEN $\rightarrow$ Command	tCMDECMD	10		35	ns	

Notes:

1. tALEH (Min. value) = tCK - (tCKST (Max. value) + tCKALE2) + tCKALE3 (Min. value).
2. tCKST (Max. value) is the value of the output delay time of MBL8086.

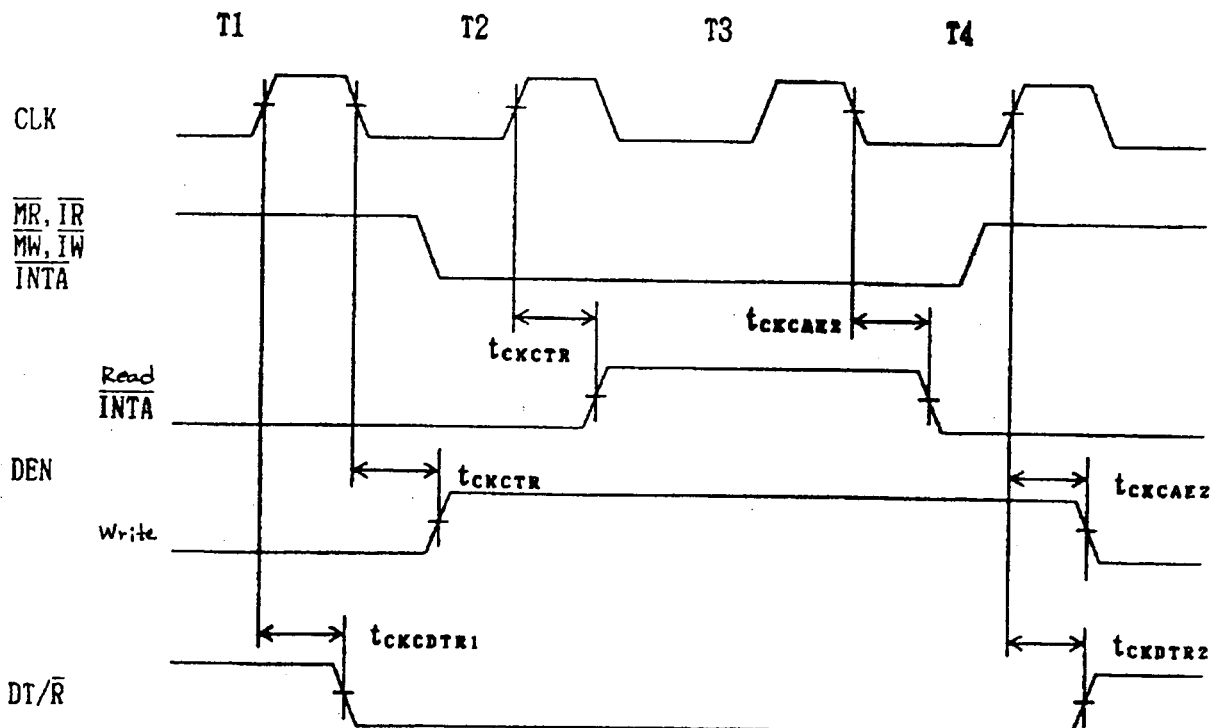
Bus Controller Timing

CLK, STATUS, ALE AND CAEN



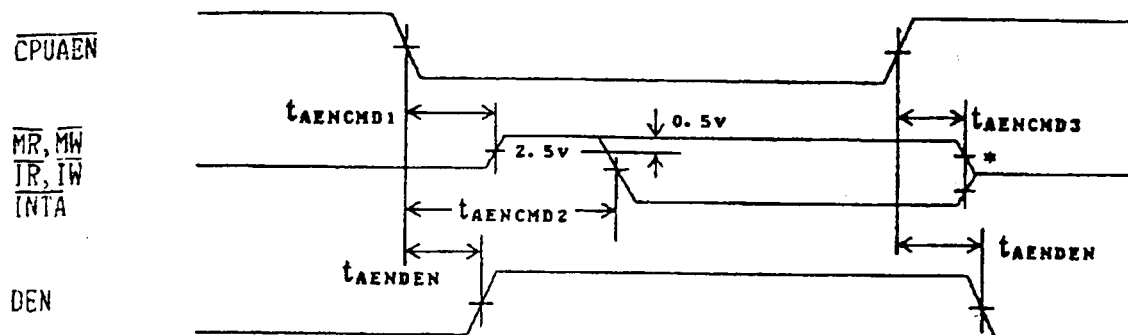
*: Delay time after the latest falling edge of ALE, CAEN, CLK or Status.

COMMAND, DEN, $\overline{IOEN}$ AND DT/ $\overline{R}$



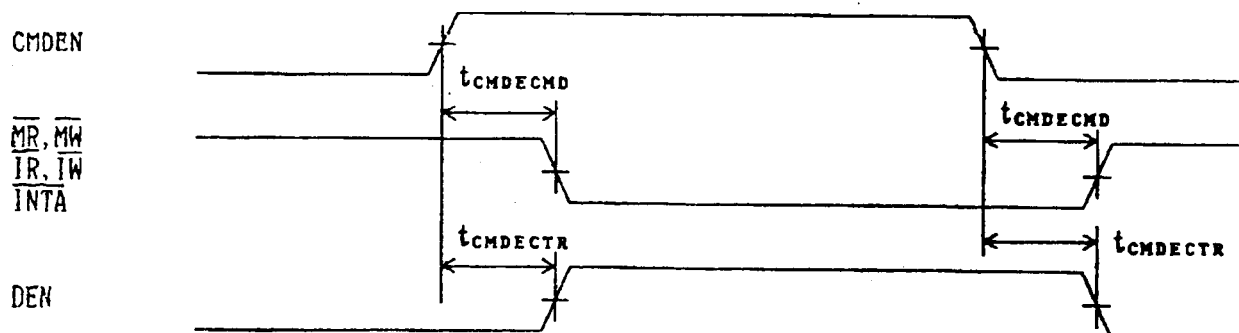
Bus Controller Timing

CPUAEN



* Measured at the point where output voltage changes 0.5V.

CMDEN



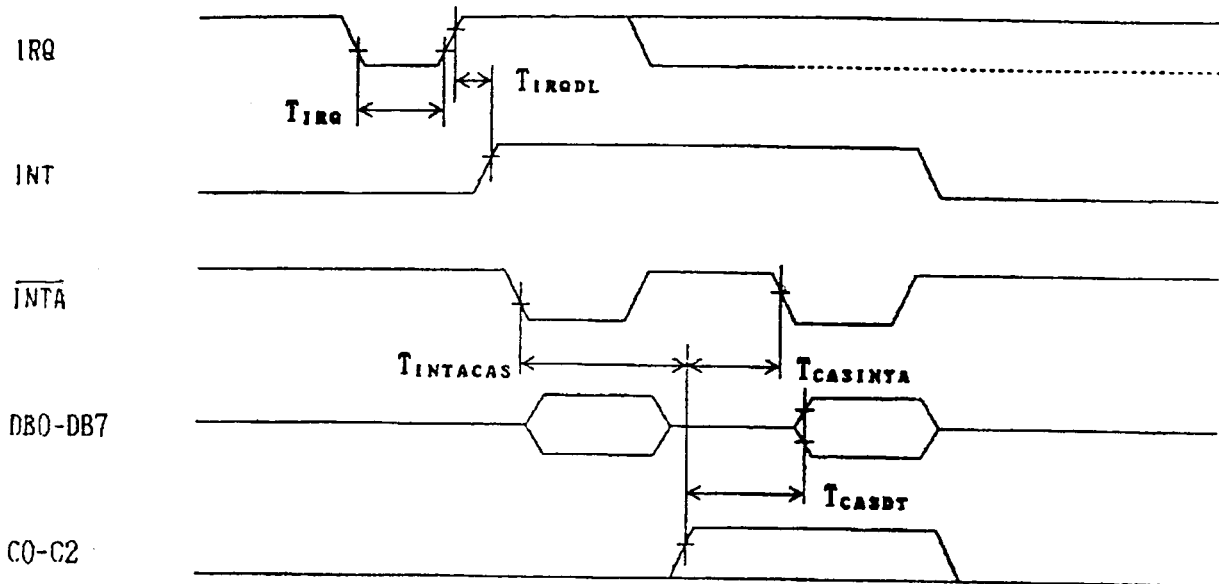
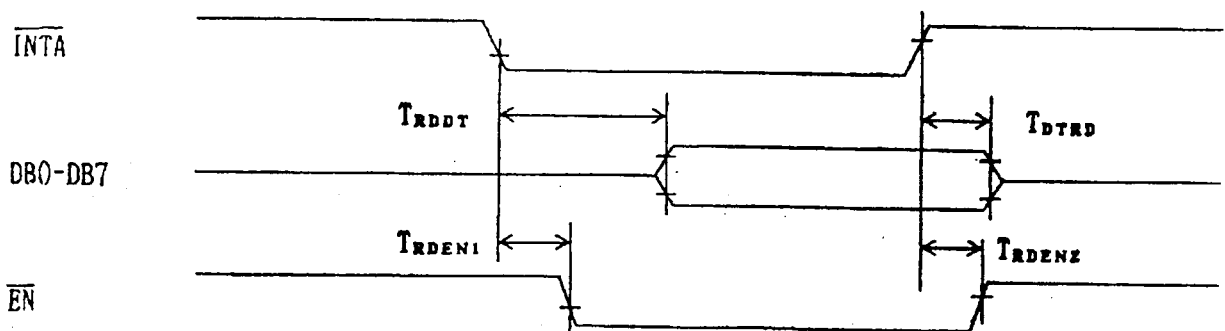
Not to generate a command, CMDEN must be Low before T2 state.

AC CHARACTERISTICS (VCC = +5V±10%, GND = 0V; TA = 0°C to +70°C)

Interrupt Controller Timing

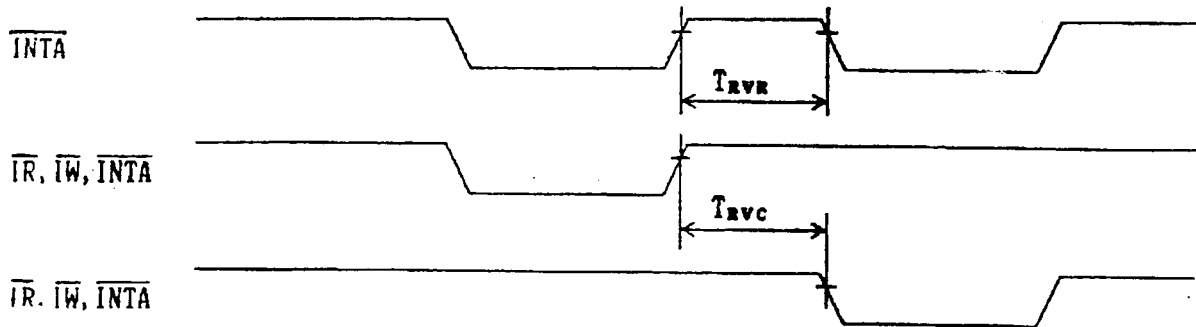
Parameter	Symbol	Value			Unit	Conditions
		Min.	Typ.	Max.		
IRQ Pulse Width	TIRQ	100			ns	
Setup INTA↓ → Cascade Time	TCASINTA	30			ns	
INTA → Next INTA	TRVINTA	160			ns	
Command Terminate → Next Command	TRVC	250			ns	
INTA↓ → Data Valid	TRDDT			120	ns	
INTA↑ → Data Float	TDTRD	10		85	ns	
INT Output Delay	TIRQDL			270	ns	
Cascade Data Fisrt INTA → Valid	TINTACAS			290	ns	
INTA↓ → $\overline{EN}$ Active	TRDEN1			100	ns	
INTA↑ → $\overline{EN}$ Inactive	TRDEN2			150	ns	
CAS Valid → Data Valid	TCASDT			200	ns	

Interrupt Controller Timing

INTERRUPT SEQUENCE MODEINTERRUPT RESPONSE MODE

$\overline{\text{EN}}$: Enable signal for a buffer of SLCT pin

Interrupt Controller Timing

OTHER TIMINGS

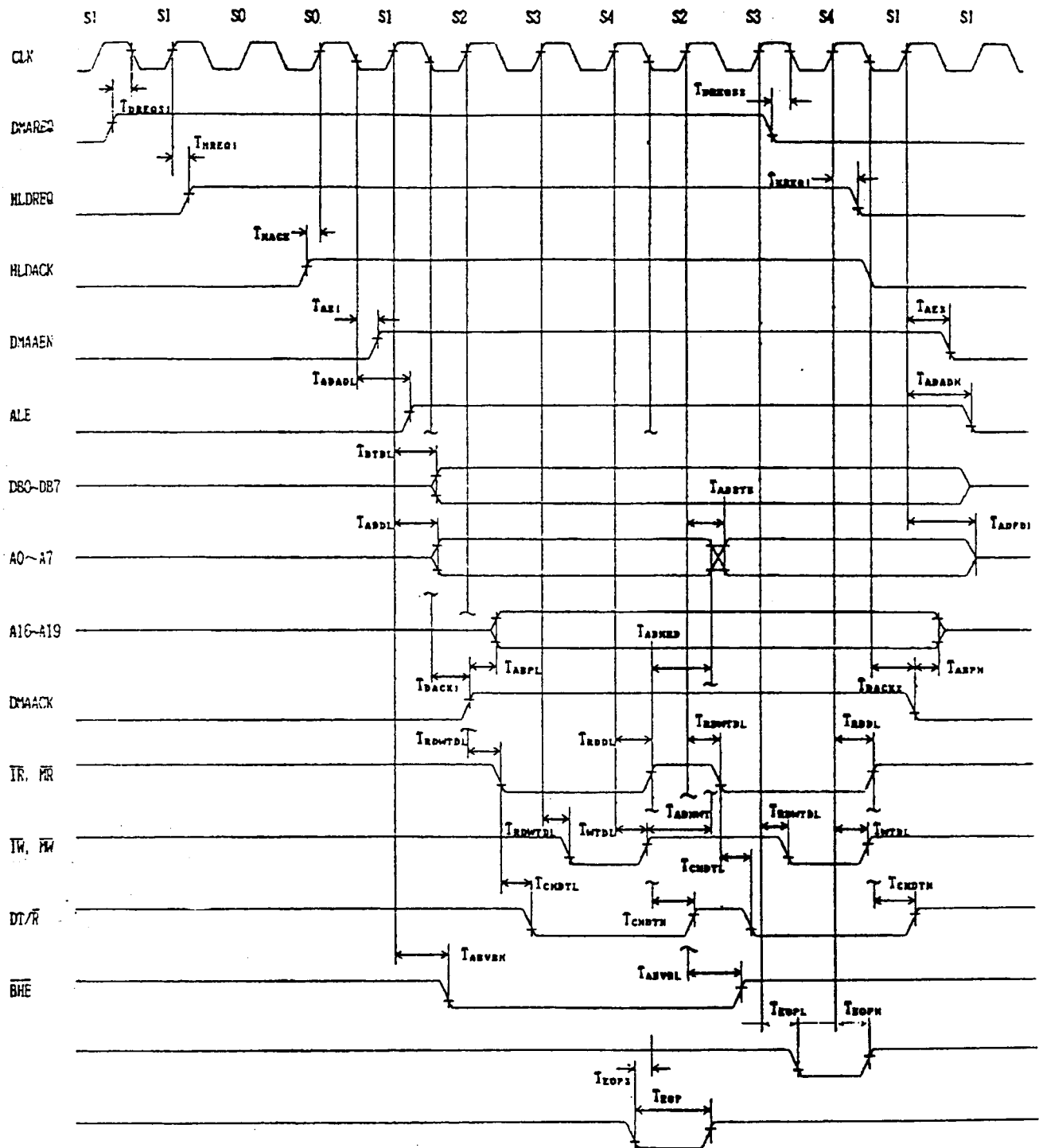
AC CHARACTERISTICS (VCC = +5V±10%, GND = 0V; TA = 0°C to +70°C)

DMA Controller Timing

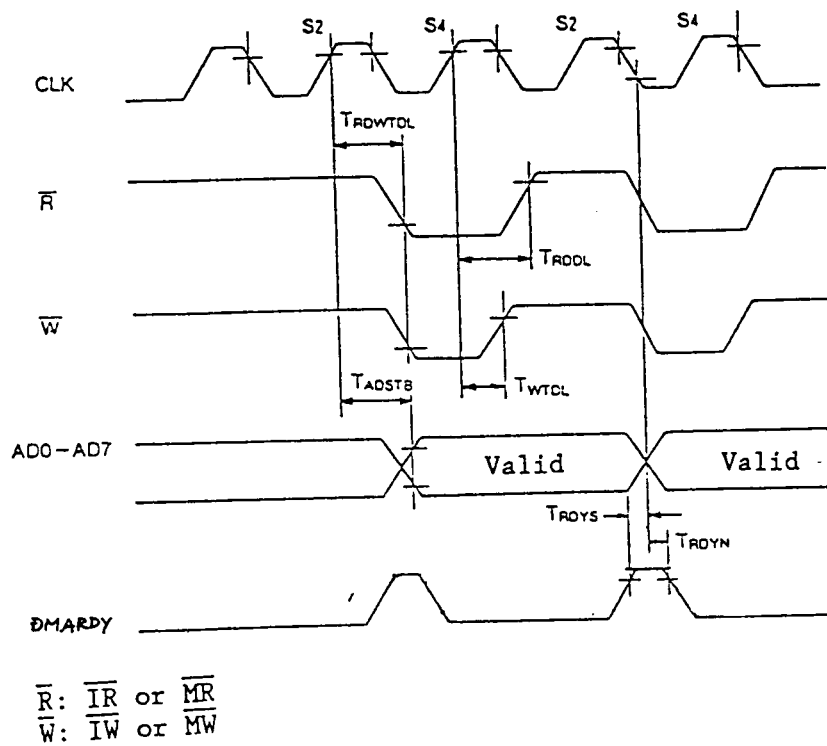
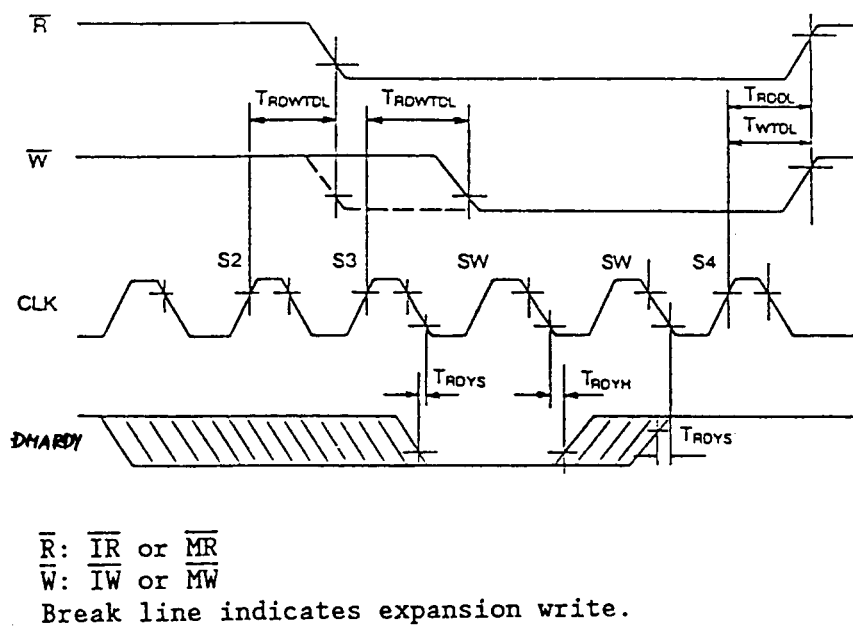
Parameter	Symbol	Value			Unit	Conditions
		Min.	Typ.	Max.		
CLK↓ → AEN↑ Delay	TAE1			100	ns	
CLK↑ → AEN↓ Delay	TAE2			70	ns	
CLK↑ → ADR Float	TADFDL			80	ns	
$\bar{R}$ ↑ → Address Hold	TADHRD	65			ns	
$\bar{W}$ ↑ → Address Hold	TADHWT	85			ns	
CLK↓ → DMAACK Valid	TDACK1			130	ns	
CLK↓ → DMAACK Low	TDACK2			130	ns	
CLK↓ → $\bar{END}$ ↑ Delay Time	TENDH			90	ns	
CLK↑ → $\bar{END}$ ↓ Delay Time	TENDL			90	ns	
CLK↑ → Address Valid	TADSTB			100	ns	
CLK↑ → $\bar{R}$ ↓, $\bar{W}$ ↓	TRDWTDL			100	ns	
CLK↑ → $\bar{R}$ ↑	TRDDL			100	ns	
CLK↑ → $\bar{W}$ ↑	TWTDL			75	ns	
Active CLK↑ → Address Delay	TADDL			100	ns	
CLK↑ → DB Active Delay	TDTD			110	ns	
CLK↓ → $\bar{END}$ ↓ Setup Time	TENDS	25			ns	
$\bar{END}$ Pulse Width	TEND	100			ns	
DMAREQ Setup Time	TDREQS1	0			ns	
	TDREQS2	0			ns	
CLK↓ → READY Hold Time	TRDYH	20			ns	
Setup CLK↓ → READY Time	TRDYS	40			ns	
CLK↑ → HLDREQ Valid	THREQ1			85	ns	
	THREQ2			85	ns	
HLDACK Setup Time (HLDACK Valid → CLK↑)	THACK	50			ns	
CLK↑ → $\bar{BHE}$ Active Time	TBHEL			100	ns	
Inactive CLK↑ → $\bar{BHE}$ Time	TBHEH			80	ns	
$\bar{R}$ ↓ → DT/ $\bar{R}$ Active Time	TDTRL			110	ns	
Inactive $\bar{R}$ ↑ → DT/ $\bar{R}$ Time	TDTRH			110	ns	
Delay DMAACK↑ → AB16-19 Time	TDACKAD1			60	ns	
Invalid DMAACK↓ → AB16-19 Time	TDACKAD2			110	ns	
CLK↓ → ALE↑ Delay Time	TALE1			20	ns	
CLK↑ → ALE↓ Delay Time	TALE2			20	ns	
$\bar{GT}$ Setup Time	TGT	20			ns	

DMA Controller Timing

DMA TRANSFER



DMA Controller Timing

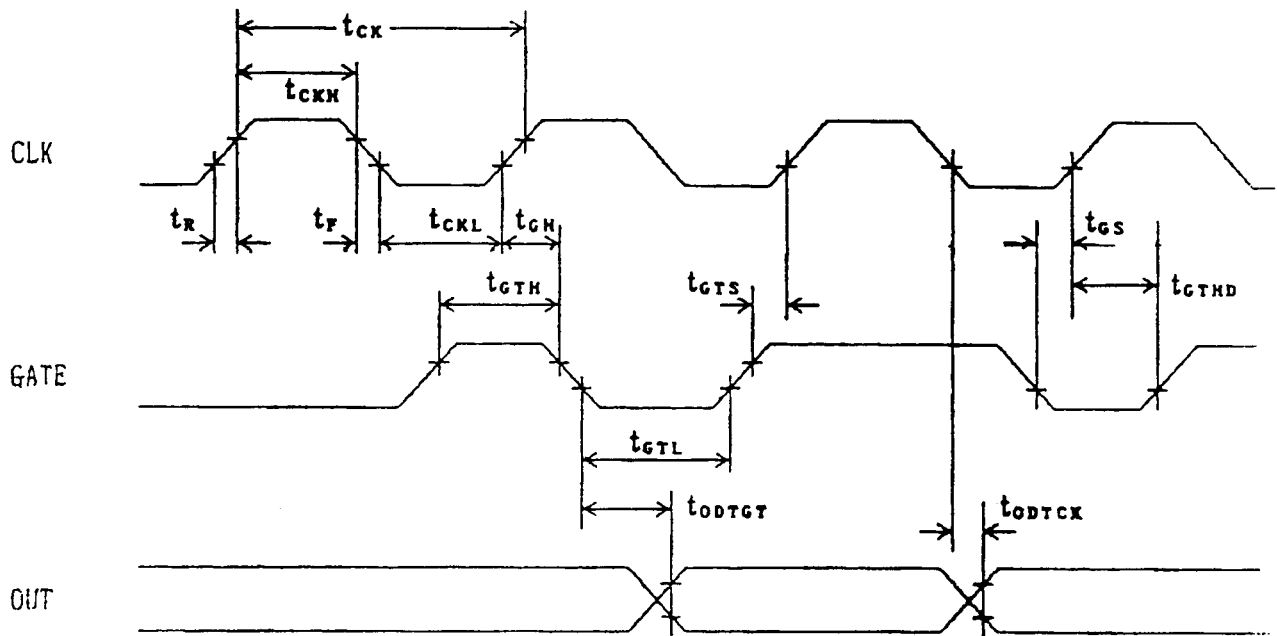
READYCOMPRESSED TRANSFER

AC CHARACTERISTICS (VCC = +5V±10%, GND = 0V; TA = 0°C to +70°C)

Interval Timer Timing

Parameter	Symbol	Value			Unit	Conditions
		Min.	Typ.	Max.		
CLK Cycle Time	tCK	125			ns	
CLK Low Pulse Width	tCKL	60			ns	
CLK High Pulse Width	tCKH	60			ns	
CLK Rise Time	tR			100	ns	
CLK Fall Time	tF			100	ns	
Gate Low Pulse Width	tGTL	50			ns	
Gate High Pulse Width	tGTH	50			ns	
Gate Setup Time	tGTS	50			ns	
Gate Hold Time	tGTHD	50			ns	
Read Recovery Time	tRVRD	200			ns	
Write Recovery Time	tRVWT	200			ns	
Output Delay Time	tDDTGT			120	ns	
Output Delay Time	tDDTCK			150	ns	

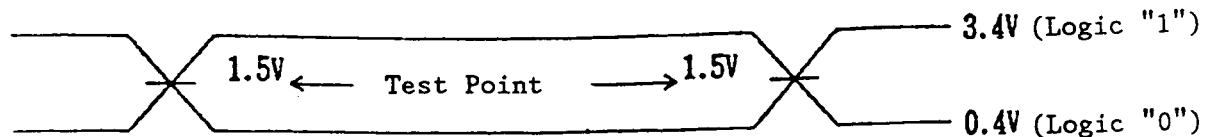
Interval Timer Timing



AC TEST CONDITIONS

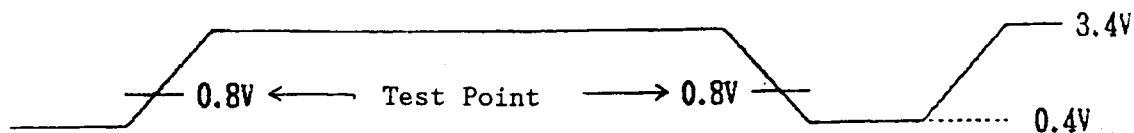
Test Input Waveforms

- For All except Clock Pins

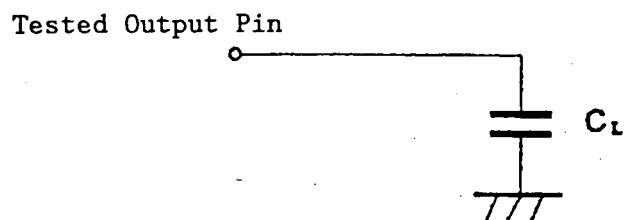


Note: Clock pins are driven at 0.25V-4.3V.

- For Clock Pins



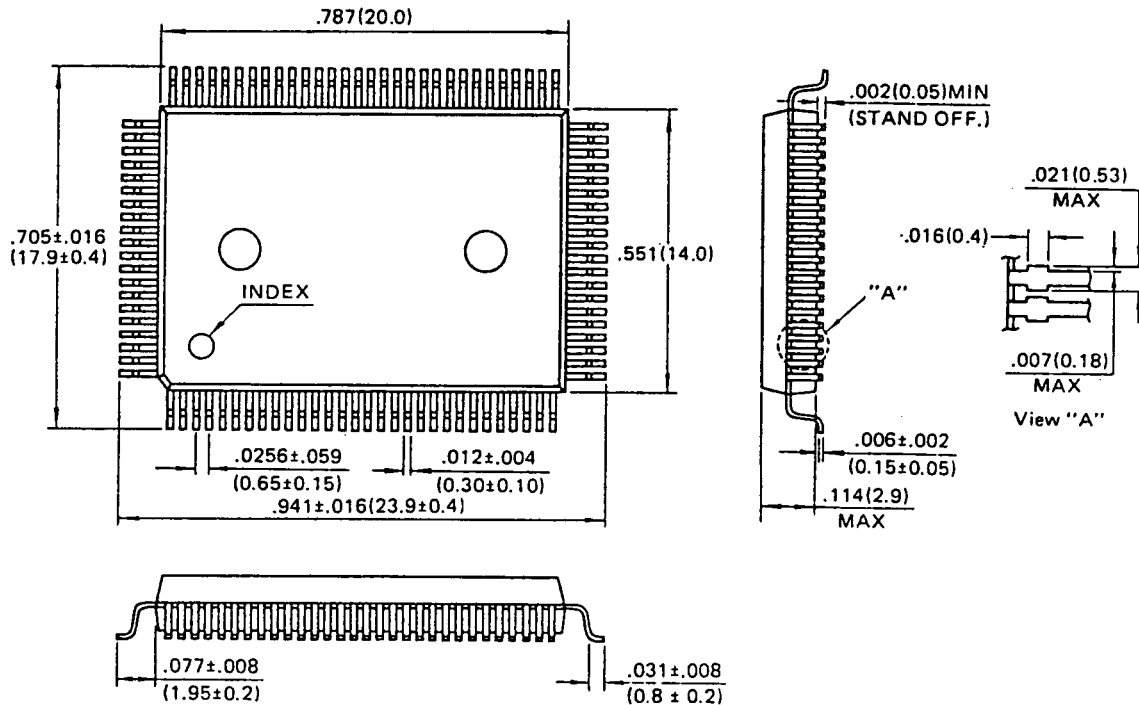
Test Load Circuit



CL=100pF including stray capacitance (for clock pins and bus controller pins)
 CL= 50pF including stary capacitance (for other pins)

PACKAGE DIMENSIONS

PLASTIC FLATPACK (SUFFIX PF)

100-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-100P-M01)

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Dimensions in
inches (millimeters)