FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-28821-1E

ASSP

ON-SCREEN DISPLAY CONTROLLER

MB90089

■ DESCRIPTION

The MB90089 CMOS On-screen Display Controller (OSDC) is a peripheral LSI that displays 288 alphanumeric characters (24 rows × 12 lines) and figures on TV screen by a microcontroller. Since the MB90089 contains a character generator ROM (CGROM) which is capable to store 256 characters including special characters "Kanji characters" and "Kana characters", it can be used even for Japanese display, in addition to the standard alphanumeric display.

The MB90089 contains a video signal generator for NTSC/PAL system, so that the characters and figures can be displayed synthesizing with this internally generated video signal even no external video signal present. Also the MB90089 incorporates video signal analog switches to synthesize characters with a video signal.

Three video outputs are available on the MB90089; a composite video, a Y/C separate video, and a RGB digital outputs. Also the device has two video inputs; a composite video and a Y/C separate video inputs. The superimposed display function is possible at either composite video input or Y/C separate video input.

The MB90089 is fabricated by the silicon-gate CMOS process, and housed in a 28-pin plastic SOP (Suffix: PF) package.

Because the MB90089 OSDC device has these powerful character display and control abilities, it is suitable for on-screen display on such applicable audio-video equipment as VCRs.

■ FEATURES

- Character display controller available for NTSC and PAL TV sets
- 24 rows × 12 lines screen format (Max. 288 characters/screen)
- 12 × 18-dot matrix high-quality character format
- 256-character set capability in character generator ROM (CGROM) (including the blank code FF_H)
- Programmable display control
  - Character size: 1 width × 1 height, 1 width × 2 heights, 2 widths × 1 height, or 2 widths × 2 heights per line
  - Character display position: horizontal: per 1/4-character, vertical: per 2 rasters, line space: per raster (0 to rasters)
  - 8 kinds of color/monochrome for under-color/character by internal video signal generator
- Patterned (Bordered) or filled background character display
- Shaded-background display

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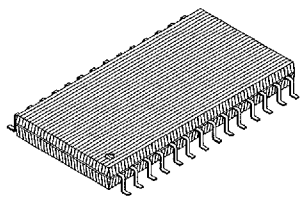
- Sprite character display (8 characters can be specified as sprite character (codes: $8F_H$ to FF_H) and one character can be displayed.)
- On-chip display data RAM (VRAM)
- Analog Video Inputs
  - Composite video signal
  - Y/C separate video signal
- Three-channel Video Output
  - Composite video signal
  - Y/C separate video signal
  - RGB digital signal
- On-chip video signal generator conforming to NTSC and PAL systems
- Separate or composite sync signal input/output
- 8-bit serial input to interface with microcontroller
- On-chip two clock generators
  - Display dot clock
  - Color burst clock
- Internal color burst phase signal output (to allow superimposed display in color adding the external components.)
- Power-on reset function
- Single +5 V power supply
- Wide operating temperature range: –45°C to +85°C
- Silicon-gate CMOS process
- Package:
  28-pin plastic SOP (Suffix: PF)

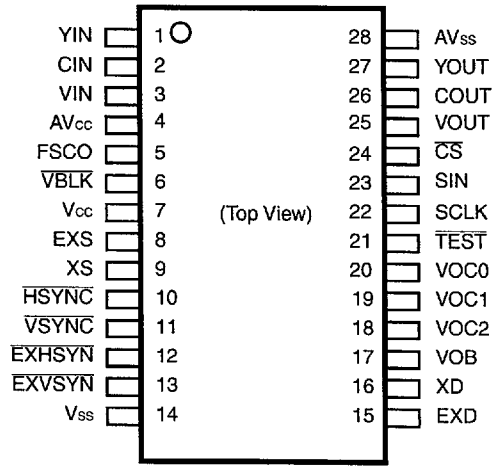
MB90089-PF



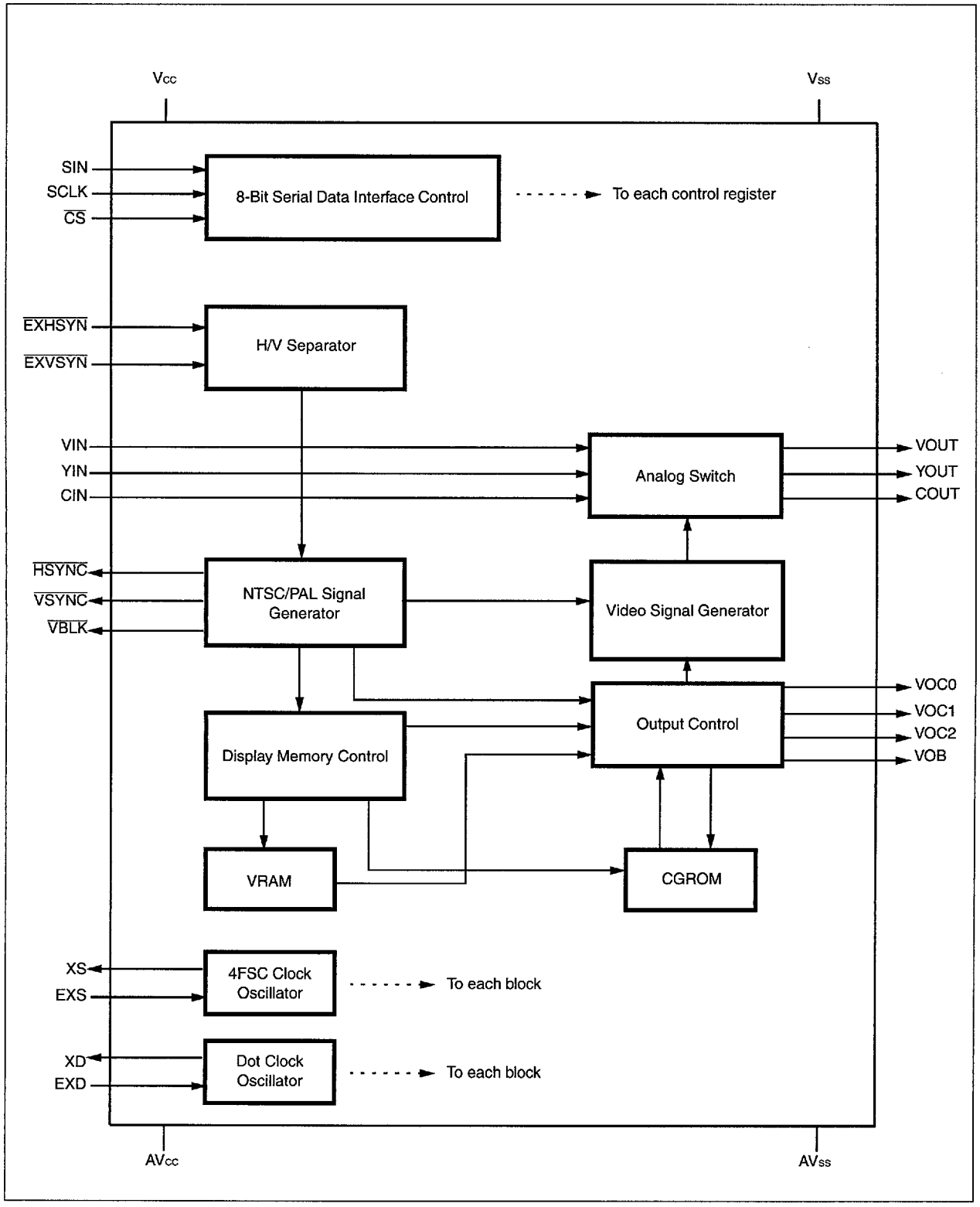
28-PIN PLASTIC SOP
(FPT-28P-M02)

■ PIN ASSIGNMENT

MB90089-PF



■ BLOCK DIAGRAM



■ PIN DESCRIPTION

Figure 1 and Table 1 show the pin assignment and pin description of the MB90089.

Table 1. Pin Description

Symbol	Pin No.	Type	Name & Function
Power Supply			
V_{CC}	7	—	Power supply pin.
V_{SS}	14	—	Ground pin.
AV_{CC}	4	—	Power supply pin for analog block. The voltage level applied to this pin must be the same as V_{CC}.
AV_{SS}	28	—	Ground pin for analog block. The ground level must be the same as V_{SS}.
Clock			
EXS	8	I	Input to the internal oscillator running with an external crystal resonator and capacitors for color burst clock (NTSC: 14.31818 MHz and PAL: 17.734475 MHz).
XS	9	O	Output from the internal oscillator running with an external crystal resonator and capacitors for color burst clock (NTSC: 14.31818 MHz and PAL: 17.734475 MHz)
EXD	15	I	Input to the internal oscillator running with an external LC network circuit for display dot clock
XD	16	O	Output from the internal oscillator running with an external LC network circuit for display dot clock
Device Test			
$\overline{TEST}$	21	I	Test signal input pin. Normally, input a high level to this pin. When a low level is input, be sure not to issue commands.
Serial Interface			
$\overline{CS}$	24	I	Chip select pin A low level on the $\overline{CS}$ pin activates serial data transfer to the device. Also, this pin can be used to release the power-on reset. This pin is hysteresis input and pulled up internally.
SIN	23	I	SIN is for serial data input. 8-bit serial data including command data and character data is input to this pin while the $\overline{CS}$ is active. This pin is hysteresis input and pulled up internally.
SCLK	22	I	SCLK is for shift clock input to the internal register. At the rising edge of SCLK, data on the SIN pin is shifted into the internal register. This pin is hysteresis input and pulled up internally.
Analog I/O Port			
YIN	1	I	Luminance signal (Y-signal) input for the superimposed display. A DC-restored (DC-clamped) 2 Vp-p signal with sync tip level = 1 V and pedestal level = 1.57 V is input to this pin.
CIN	2	I	Chroma signal (C-signal) input for the superimposed display. Input a signal with a DC 1.57 V and color burst signal amplitude = 0.57 Vp-p.
VIN	3	I	Composite video signal input for the superimposed display. Input a DC-restored (DC-clamped) 2 Vp-p signal with sync tip level = 1 V and pedestal level = 1.57 V.

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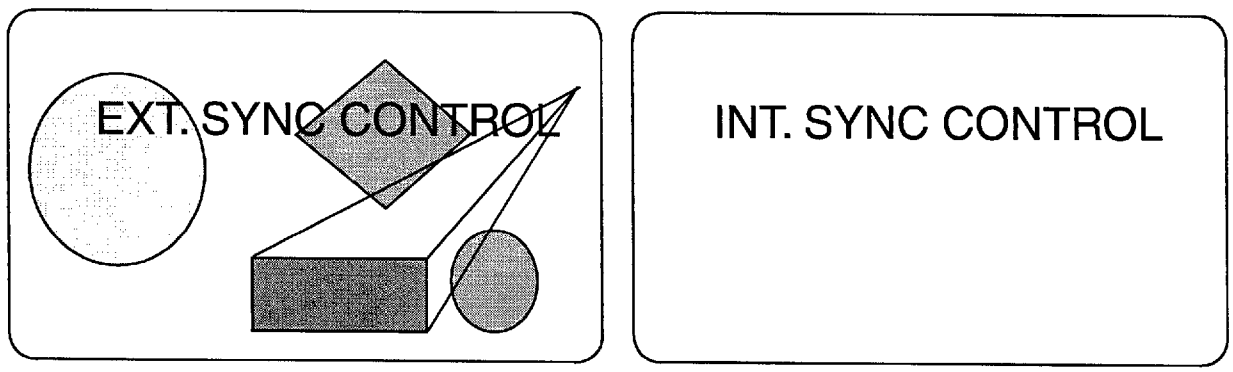
Symbol	Pin No.	Type	Name & Function
Analog I/O Port (continued)			
VOUT	25	O	Composite video signal output pin. This pin outputs 2 Vp-p signal with sync tip level = 1 V and pedestal level = 1.57 V.
COUT	26	O	Chroma signal output pin. This pin outputs a signal with a DC 1.57 V and a color burst amplitude = 0.57 Vp-p.
YOUT	27	O	Luminance signal output pin. This pin outputs 2 Vp-p signal with sync tip level = 1 V and pedestal level = 1.57 V.
$\overline{\text{VBLK}}$	6	O	Vertical blanking signal output pin. This pin outputs a low level during the vertical blanking interval.
Output Port			
VOB	17	O	This is a character and its background signals output pin. While this pin outputs a high level, character and patterned or filled background information are output.
VOC2-VOC0	18-20	O	These are character signal output pins. These pins output a character color, character background color and under-color.
FSCO	5	O	Internal color burst phase signal output pin. While the device is operating in external sync control mode; superimposed color display is possible controlling the EXS pin input clock to match the signal phase between the output signal from this pin and the color burst signal of the externally input video signal. This pin functions with the FO bit setting in the internal register by command #7.
Sync Signal Related Port			
$\overline{\text{HSYNC}}$	10	O	Horizontal sync signal output pin. This pin is also used for composite sync signal output. Furthermore, by forcing the $\overline{\text{TEST}}$ pin low, this pin outputs a fsc clock.
$\overline{\text{VSYNC}}$	11	O	Vertical sync signal output pin. Also, by forcing the $\overline{\text{TEST}}$ pin low, this pin outputs an oscillation clock for the dot clock.
$\overline{\text{EXHSYN}}$	12	I	External horizontal sync signal input pin. This pin is also used for composite sync signal input. This is a hysteresis input and internally pulled-up.
$\overline{\text{EXVSYN}}$	13	I	External vertical sync signal input pin. This is a hysteresis input and internally pulled-up.

■ DISPLAY FUNCTIONS

The MB90089 provides two types of screen display: external sync controlled operation and internal sync controlled operation. External sync controlled operation is used for the superimposed display of an externally input video signal and characters. Internal sync controlled operation is used to display characters after superimposing them with the internally generated video signal generated by the built-in video signal generator. In internal sync controlled operation, the MB90089 allows 8-color color display.

Figure 1 shows display examples in each video mode.

Fig. 1 – Video Modes



External sync controlled operation
(Superimposed display)

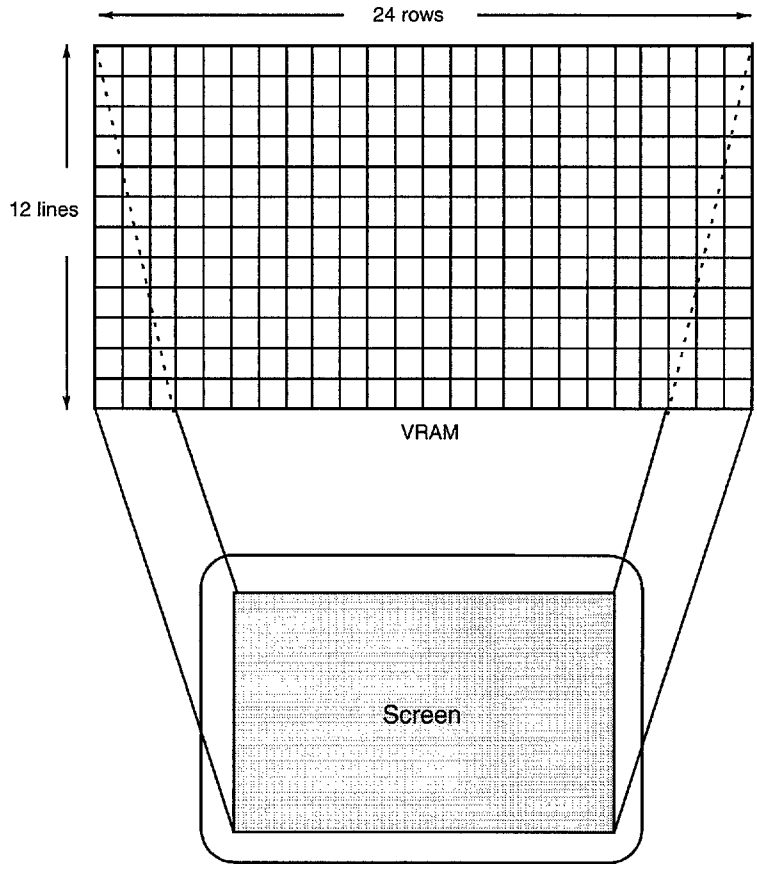
Internal sync controlled operation
(Color/monochrome gray scale display)

Note: For external sync controlled operation, characters are always displayed with monochrome gray scale.

■ DISPLAY SCREEN CONFIGURATION

The MB90089 has a 288-character display memory (VRAM) so that when using the standard character size, it can display characters in up to 24 rows × 12 lines (= 288 characters) on one screen. When using enlarged characters, the number of characters that can be displayed on a screen is reduced depending on how much they are enlarged. Four character sizes (called standard size and 3 kinds of enlarged size) can be set and specified either size for each line. So, the MB90089 can display characters of four different sizes together on the same screen. Figure 2 shows the display screen configuration.

Fig. 2 – Display Screen Configuration



■ CHARACTER CONFIGURATION

The MB90089 incorporates character generator ROM (CGROM) that can store up to 256 characters including the end code. Each character generated by CGROM consists of a 12 × 18 dot matrix.

Each character is displayed with a dot matrix consisting of 12 dots in the horizontal direction (row) and 18 dots in the vertical direction (line) as shown in Figure 3.

Also, four types of character size are available on MB90089: A standard size which consists of 12 × 18 dot matrix and other 3 kinds of enlarged size. These four types of character size can be specified for each line on the screen. Figure 4 shows an example of character display with coexisting two types of size.

Fig. 3 – Character Dot Configuration

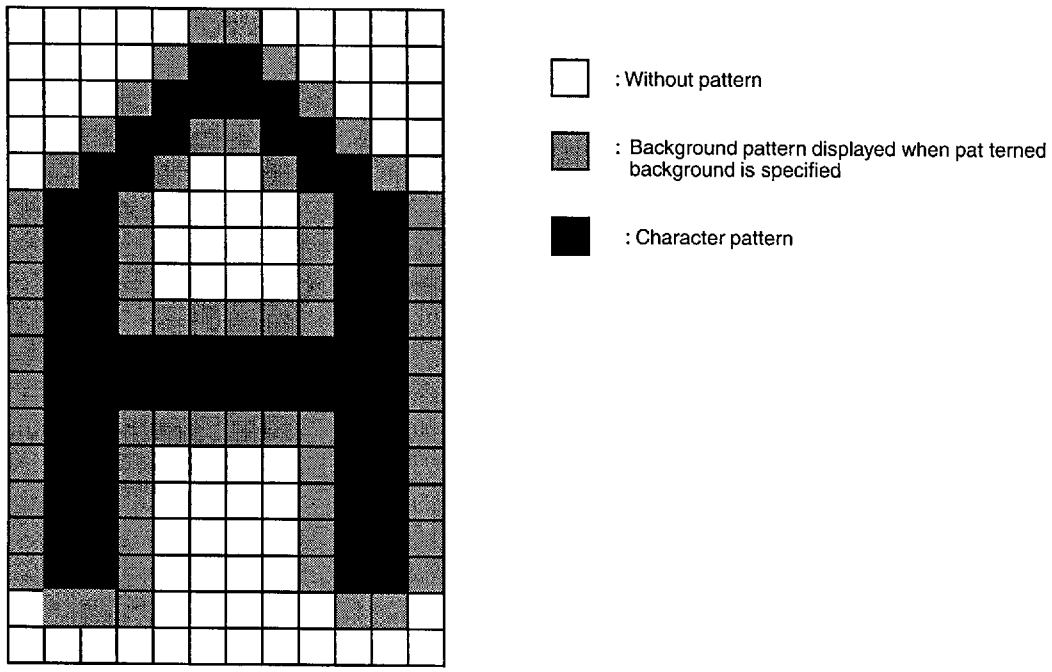
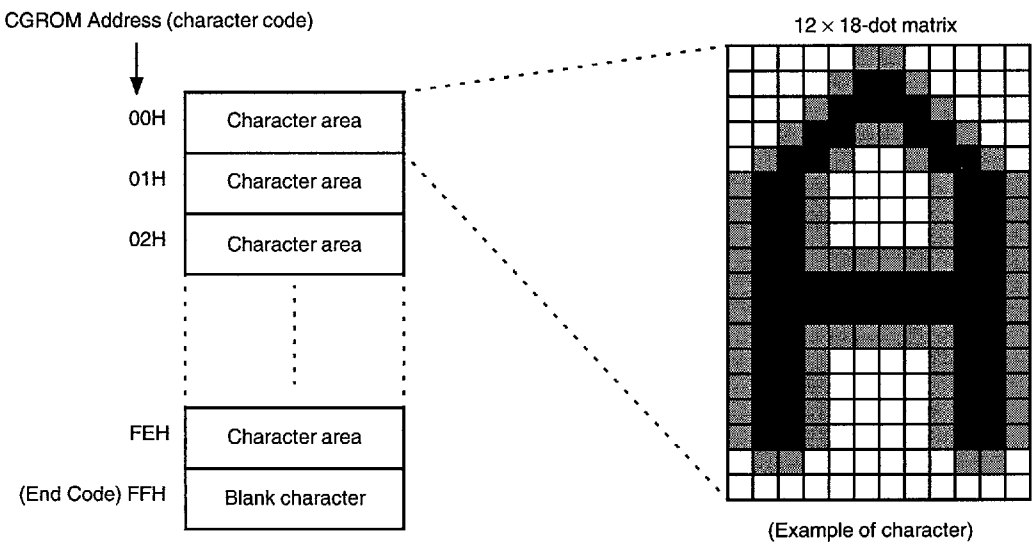


Fig. 4 – Example of Enlarged and Standard Size Characters Display

■ CONFIGURATION OF CGROM

The Character Generator ROM (CGROM) is configured with 12 dots horizontal × 18 dots vertical. It has a storage capacity for up to 256 character including the end code. The CGROM's address is corresponding to the character's code. Figure 5 shows the CGROM's configuration.

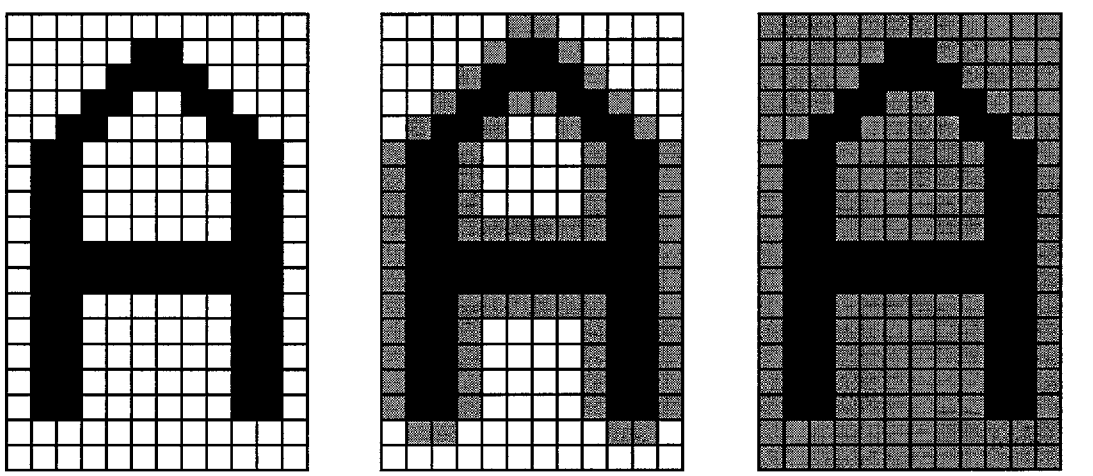
Fig. 5 – CGROM Configuration



■ CHARACTER DISPLAY FORMAT

The MB90089 allows to select a character display format from "character-only", "patterned background (border)", "filled background" displays for each line and also character-background displays for each character by setting the internal registers. Figure 6 shows an example for each of the character display formats.

Fig. 6 – Character Display Format



■ SHADED-BACKGROUND DISPLAY

The MB90089 also has the shaded-background display (shadowing background) function that adds black & white line along the character's rectangle area to display the character like in three-dimension. The shaded-background can be set for character unit. The shaded-background color (black & white) can be exchanged (reversed).

■ SPRITE CHARACTER DISPLAY

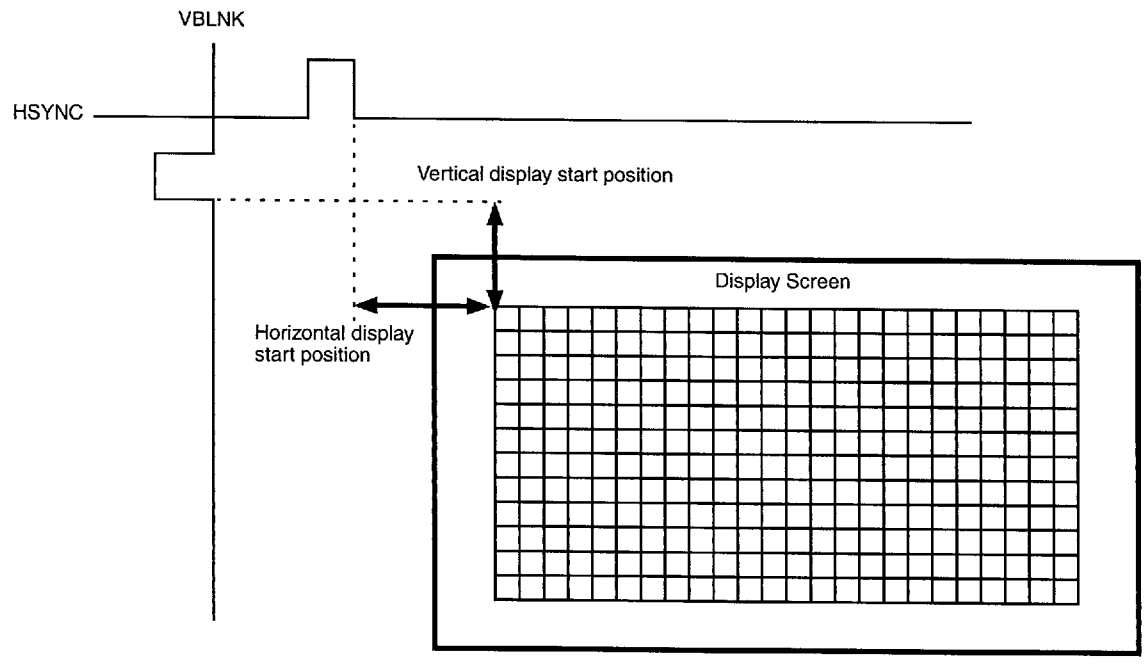
The MB90089 has another unique function called "sprite character display" that makes a character motion smooth. The sprite character can be displayed on screen synthesizing with the normal characters being displayed. The sprite character motion can be set in character dot unit and one character can be displayed on one screen. The sprite character codes are specified in the CGROM codes $8F_H$ to FF_H. 8 kinds of color or 8 gray-scale level can be specified for the sprite character.

■ CHARACTER DISPLAY START POSITION

The MB90089 allows to choose from 64 display start positions in the horizontal and 32 positions in the vertical directions by setting each internal register. Also, line space can be set in raster unit (0 to 7 rasters). By setting the appropriate display start positions depending on the screen configuration, you can arrange character placement so it is balanced across the screen.

To set the display start position of characters, specify the dot position at the upper left corner of the character at the upper left part of the screen. The display start position can be set in units of 3 dots (1/4-character) in the horizontal direction, and in units of 2 dots (2 rasters) in the vertical direction. Figure 7 shows how the start position is specified in the horizontal and the vertical directions.

Fig. 7 – Character Display Start Position



■ DATA TRANSFER

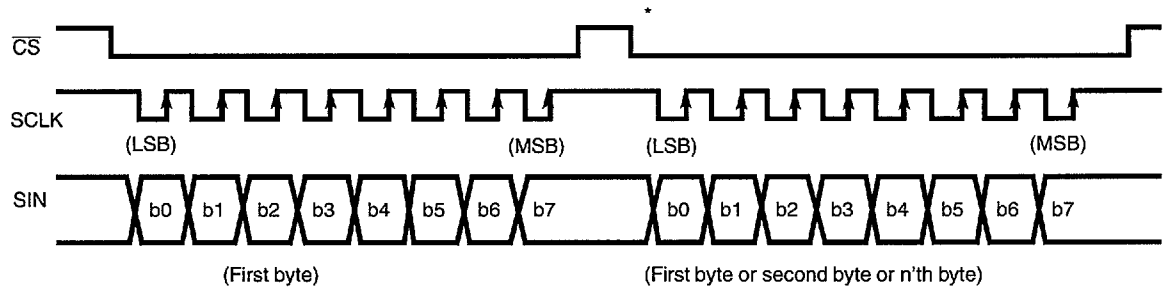
Display control commands and data are written to the MB90089 via 8-bit serial transfer block. This serial transfer is done by using three signals: $\overline{CS}$ (chip select), SCLK (shift clock), and SIN (serial data input). Figure 8 shows the timing of serial transfer. The $\overline{CS}$ pin is for the chip select signal, and is set Low for serial transfer. The SCLK pin is for the shift clock signal for data reception. The SIN pin is for the serial data input signal.

The data is eight bits length, and sequentially shifted into the SIN pin beginning with the least significant bit (LSB). The data is latched and shifted in on each rising edge of the shift clock input to the SCLK pin as shown in Figure 10. The transferred data is loaded into the internal FIFO (First- In, First-Out) 1-byte buffer on the shift clock rising edge at the eighth bit. The data is read from FIFO and processed at times other than the display memory write period. Thus, commands and data can be written to the MB90089 at any time regardless of its display operation (i.e., asynchronously with display) by using the FIFO buffer.

In serial transfer, the number of received bits is counted by shift clock counts. Serial transfer may be reset by forcing the $\overline{CS}$ pin High; the reset can be cleared by driving the $\overline{CS}$ pin from High to Low, so that the subsequent eight bits of data (eight shift clock counts) are handled as byte data. In this way, byte synchronization can be maintained by using the $\overline{CS}$ pin.

If the $\overline{CS}$ signal goes High before eight bits of data are transferred, the data becomes invalid.

Fig. 8 – Serial Transfer Timing



* : To maintain byte synchronization, the $\overline{CS}$ pin should be temporarily returned High before serial data transfer and set Low level to initiate data transfer.

■ LIST OF CONTROL COMMANDS

The MB90089 control (display control) is done by writing data to the internal registers and display memory via serial data transfer. Table 2 lists the display control commands of the MB90089.

Table 2. Display Control Commands

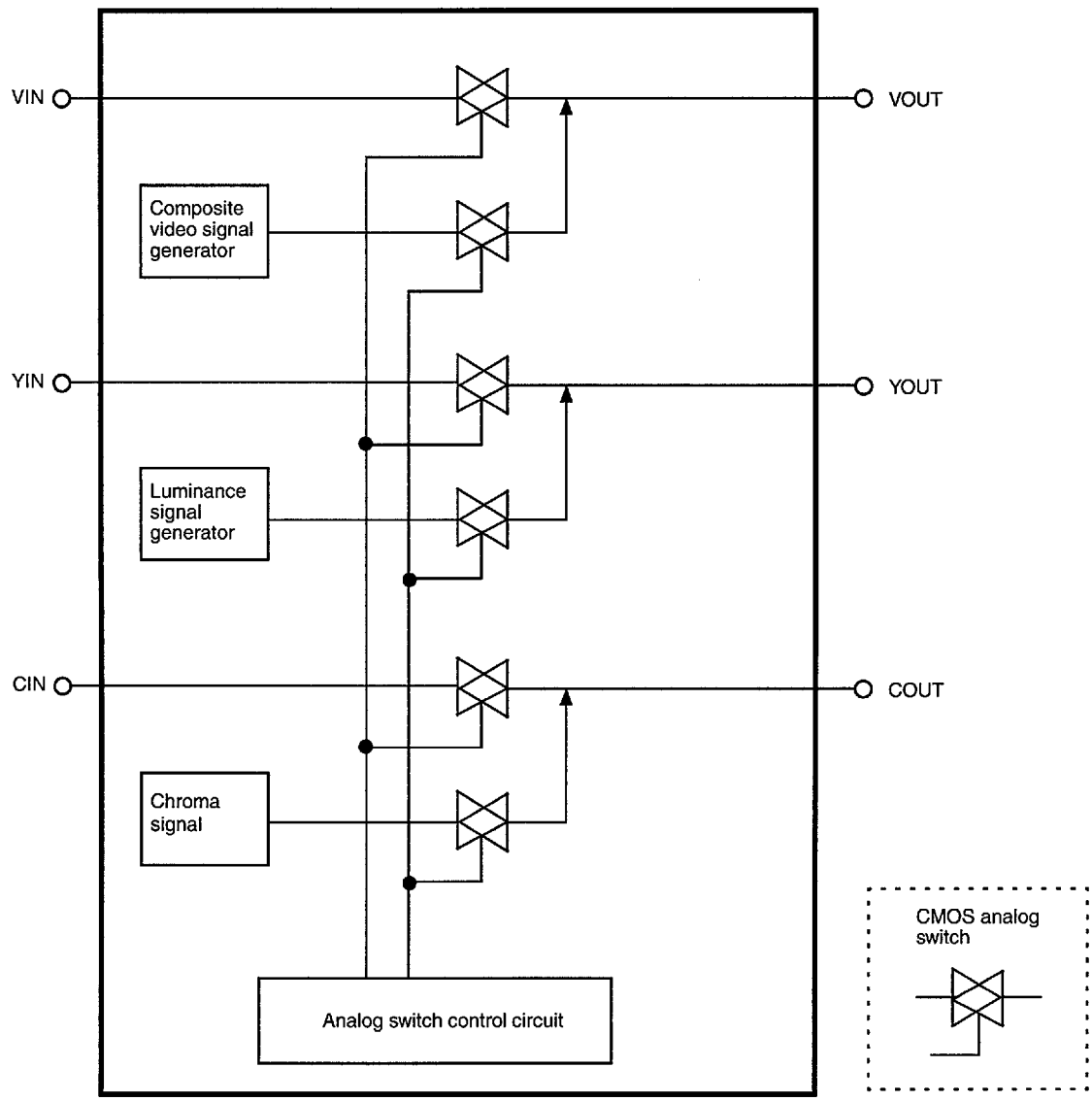
Command No.	First Byte (Command ID code + Data)								Second Byte (Data)								Function
	b7	b6	b5	b4	b3	b2	b1	b0	b7	b6	b5	b4	b3	b2	b1	b0	
0	1	0	0	0	0	FL	A8	A7	0	A6	A5	A4	A3	A2	A1	A0	Preset VRAM address.
1	1	0	0	0	1	D2	D1	D0	0	C2	C1	C0	BS	B2	B1	B0	Set character and character background color
2	1	0	0	1	0	AT	0	M7	0	M6	M5	M4	M3	M2	M1	M0	Write character code to VRAM.
3	1	0	0	1	1	S2	S1	S0	0	SC2	SC1	SC0	0	SB2	SB1	SB0	Sprite Control 1
4	1	0	1	0	0	IE	IN	EB	0	MM	CM	MP	NP	0	0	DC	Screen Control 1
5	1	0	1	0	1	LP	DM	SG	0	FM	SV	SD	0	W2	W1	W0	Screen Control 2
6	1	0	1	1	0	BK	G1	G0	0	BC	VD	DG	N3	N2	N1	N0	Line Control
7	1	0	1	1	1	EC	XE	FO	0	0	0	Y4	Y3	Y2	Y1	Y0	Set vertical display start position.
8	1	1	0	0	0	SC	XS	FC	0	0	X5	X4	X3	X2	X1	X0	Set horizontal display start position.
9	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	Reserved command.
10	1	1	0	1	0	XC	XB	RA	0	R2	R1	R0	RS	U2	U1	U0	Set under-color.
11	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	Reserved commands.
12	1	1	1	0	0	0	XC4	XC3	0	XC2	XC1	XC0	XD3	XD2	XD1	XD0	Sprite Control 2
13	1	1	1	0	1	0	YC3	YC2	0	YC1	YC0	YD4	YD3	YD2	YD1	YD0	Sprite Control 3
14	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	Reserved commands.
15	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	

Notice that Reserved Commands (Command #9, 11, 14, and 15) are not effective for the device control. Do not issue these commands.

■ ANALOG SWITCH CIRCUIT

Figure 9 shows a functionally equivalent circuit of the analog switch section used to synthesize character information with an externally input or internally generated video signal.

Fig. 9 – Equivalent Circuit of Analog Switch Block



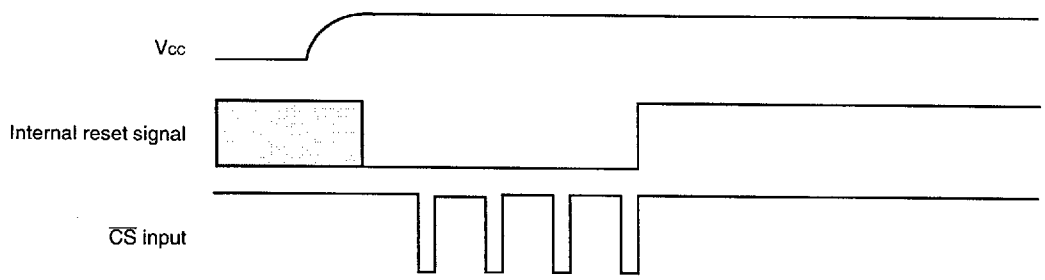
■ POWER-ON RESET

A power-on reset means that the device generates an internal reset signal to initialize its operation upon detection of power-on.

Input the $\overline{CS}$ signal four times to clear a power-on reset.

Figure 10 shows a timing of how a power-on reset is cleared.

Fig. 10 – Clearing Power-on Reset



DEVICE INITIALIZATION

When reset at power-on, the MB90089's screen control register has its IE (internal/external sync control) bit and DC (display control) bit cleared to 0, and screen display is turned off under internal sync control.

After power-on, clear a power-on reset first. Then, set the screen control register's DC bit to 1 to turn display on after setting all register data and all VRAM contents to be displayed.

■ ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (See NOTE)

Parameter	Symbol	Rating			Unit	Condition
		Min.	Typ.	Max.		
Power Supply Voltage	V_{CC}	V_{SS} −0.3	—	V_{SS} +7.0	V	Make sure no different voltage level between AV_{CC} and V_{CC}.
	AV_{CC}	V_{SS} −0.3	—	V_{SS} +7.0	V	Make sure no different voltage level between AV_{CC} and V_{CC}.
	AV_{SS}	V_{SS} −0.3	—	V_{SS} +7.0	V	Make sure no different voltage level between AV_{CC} and V_{CC}. Should not exceed V_{CC} +0.3 V
Input Voltage	V_{IN}	V_{SS} −0.3	—	V_{SS} +7.0	V	Should not exceed V_{CC} +0.3 V
Output Voltage	V_{OUT}	V_{SS} −0.3	—	V_{SS} +7.0	V	Should not exceed V_{CC} +0.3 V
Power Dissipation	P_D	—	—	600	mW	
Operating Ambient Temperature	T_A	−40	—	+85	°C	
Storage Temperature	T_{STG}	−55	—	+150	°C	

NOTE: Permanent device damage may occur if the above **ABSOLUTE MAXIMUM RATINGS** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Rating			Unit	Condition
		Min.	Typ.	Max.		
Power Supply Voltage	V_{CC}	4.5	—	5.5	V	Operation guaranteed range
	V_{SS}	—	0	—		
	AV_{CC}	4.5	—	5.5		Make sure no different voltage level between V_{CC} and AV_{CC}.
	AV_{SS}	—	0	—		
Input High Voltage	V_{IHS}	0.8•V_{CC}	—	V_{CC} +0.3	V	
Input Low Voltage	V_{ILS}	V_{SS} −0.3	—	0.2•V_{CC}	V	
Analog Input Voltage	AV_{IN}	0	—	V_{CC}	V	
Operating Ambient Temperature	T_A	−40	—	+85	°C	

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Pin/Port	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Output High Voltage	V_{OH}	VOC2, VOC1, VOC0, VOB, $\overline{VBLK}$, FSCO, $\overline{HSYNC}$, $\overline{VSYNC}$	V_{CC} = 4.5 V I_{OH} = –200 µA	4.0	4.4	—	V	
Output Low Voltage	V_{OL}	VOC2, VOC1, VOC0, VOB, $\overline{VBLK}$, FSCO, $\overline{HSYNC}$, $\overline{VSYNC}$	V_{CC} = 4.5 V I_{OL} = 3.2 mA	—	0.2	0.6	V	
Input Current	I_{IL}	SIN, SCLK, $\overline{CS}$, $\overline{EXHSYN}$, $\overline{EXVSYN}$, $\overline{TEST}$	V_{CC} = 5.5 V V_{IL} = 0.4 V	—	–14	–60	µA	
Supply Current	I_{CC}	V_{CC}, AV_{CC}	V_{CC} = 5.5 V f_C = 4f_{SC} = 17.734475 MHz, f_{DC} = 8 MHz Unloaded	—	45	60	mA	
ON resistance	R_{VON}	VIN-VOUT	V_{CC} = AV_{CC} = 4.5 V I_{OL} = 100 µA	—	100	320	Ω	
	R_{YON}	YIN-YOUT	V_{CC} = AV_{CC} = 4.5 V I_{OL} = 100 µA	—	100	320	Ω	
	R_{CON}	CIN-COUT	V_{CC} = AV_{CC} = 4.5 V I_{OL} = 100 µA	—	100	320	Ω	
OFF Leakage Current	I_{VOFF}	VIN	V_{CC} = AV_{CC} = 5.5 V V_{IN} = 5.5 V	—	0.1	10	µA	
	I_{YOFF}	YIN	V_{CC} = AV_{CC} = 5.5 V Y_{IN} = 5.5 V	—	0.1	10	µA	
	I_{COFF}	CIN	V_{CC} = AV_{CC} = 5.5 V C_{IN} = 5.5 V	—	0.1	10	µA	
Color 6 Upper Level	V_{CL6H}	V_{OUT}	V_{CC} = AV_{CC} = 5.0 V	2.66	2.77	2.88	V	
Color 6 Lower Level	V_{CL6L}			2.09	2.20	2.31	V	
Color 5 Upper Level	V_{CL5H}	V_{OUT}	V_{CC} = AV_{CC} = 5.0 V	2.77	2.88	2.99	V	
Color 5 Lower Level	V_{CL5L}			1.75	1.86	1.97	V	
Color 4 Upper Level	V_{CL4H}	V_{OUT}	V_{CC} = AV_{CC} = 5.0 V	2.15	2.26	2.37	V	
Color 4 Lower Level	V_{CL4L}			2.15	2.26	2.37	V	

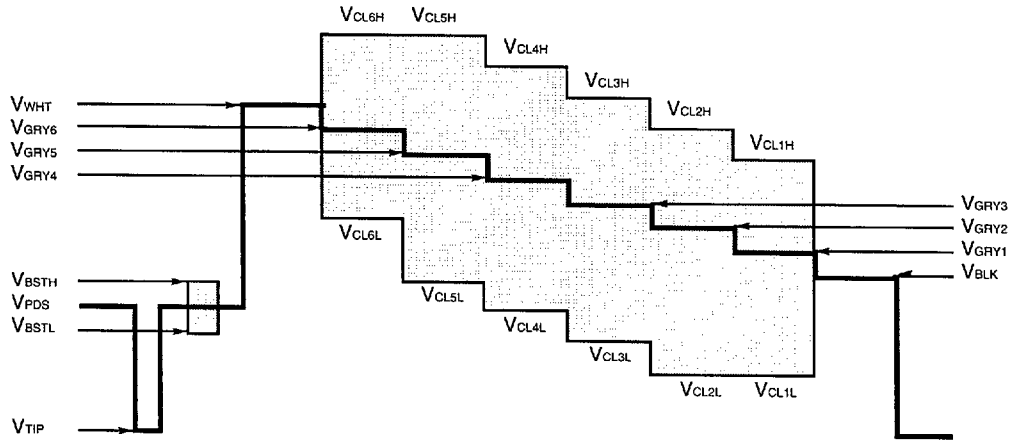
(Continued)

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Pin/Port	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Color 3 Upper Level	V_{CL3H}	V_{OUT}	V_{CC} = AV$_{CC}$ = 5.0 V	1.92	2.03	2.14	V	
Color 3 Lower Level	V_{CL3L}			1.92	2.03	2.14	V	
Color 2 Upper Level	V_{CL2H}	V_{OUT}	V_{CC} = AV$_{CC}$ = 5.0 V	2.32	2.43	2.54	V	
Color 2 Lower Level	V_{CL2L}			1.29	1.40	1.51	V	
Color 1 Upper Level	V_{CL1H}	V_{OUT}	V_{CC} = AV$_{CC}$ = 5.0 V	1.98	2.09	2.20	V	
Color 1 Lower Level	V_{CL1L}			1.35	1.46	1.57	V	
Color Burst Upper Level	V_{BSTH}	V_{OUT}	V_{CC} = AV$_{CC}$ = 5.0 V	1.80	1.91	2.02	V	
Color Burst Lower Level	V_{BSTL}			1.12	1.23	1.34	V	
White Level	V_{WHT}	V_{OUT}	V_{CC} = AV$_{CC}$ = 5.0 V	2.78	2.89	3.00	V	
Black Level	V_{BLK}	V_{OUT}	V_{CC} = AV$_{CC}$ = 5.0 V	1.57	1.68	1.79	V	
Gray Level 1	V_{GRY1}	V_{OUT}	V_{CC} = AV$_{CC}$ = 5.0 V	1.69	1.80	1.91	V	
Gray Level 2	V_{GRY2}			1.86	1.97	2.08	V	
Gray Level 3	V_{GRY3}			1.98	2.09	2.20	V	
Gray Level 4	V_{GRY4}			2.20	2.31	2.42	V	
Gray Level 5	V_{GRY5}			2.32	2.43	2.54	V	
Gray Level 6	V_{GRY6}			2.49	2.60	2.71	V	
Pedestal Level	V_{PDS}	V_{OUT}	V_{CC} = AV$_{CC}$ = 5.0 V	1.46	1.57	1.68	V	
SYNC Level	V_{TIP}	V_{OUT}	V_{CC} = AV$_{CC}$ = 5.0 V	0.84	1.00	1.16	V	

Fig. 11 – Outputs on V_{OUT}



DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

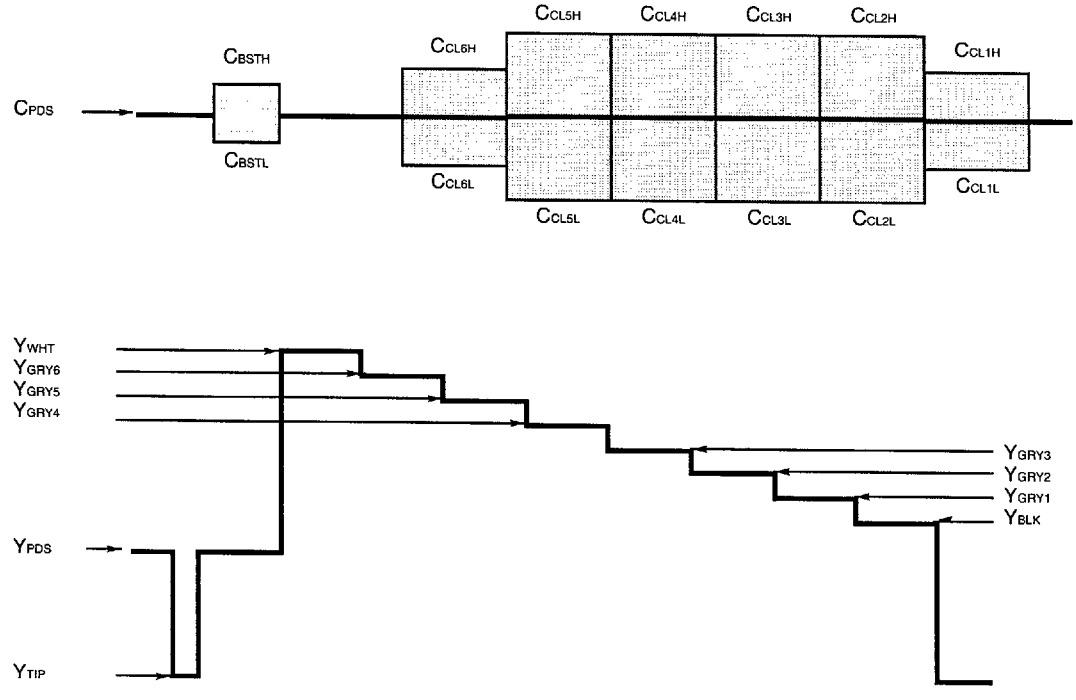
Parameter	Symbol	Pin/Port	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Color 6 Upper Level	C_{CL6H}	C_{OUT}	V_{CC} = AV_{CC} = 5.0 V	1.75	1.86	1.97	V	
Color 6 Lower Level	C_{CL6L}			1.17	1.28	1.39	V	
Color 5 Upper Level	C_{CL5H}	C_{OUT}	V_{CC} = AV_{CC} = 5.0 V	1.97	2.08	2.19	V	
Color 5 Lower Level	C_{CL5L}			0.95	1.06	1.17	V	
Color 4 Upper Level	C_{CL4H}	C_{OUT}	V_{CC} = AV_{CC} = 5.0 V	1.46	1.57	1.68	V	
Color 4 Lower Level	C_{CL4L}			1.46	1.57	1.68	V	
Color 3 Upper Level	C_{CL3H}	C_{OUT}	V_{CC} = AV_{CC} = 5.0 V	1.46	1.57	1.68	V	
Color 3 Lower Level	C_{CL3L}			1.46	1.57	1.68	V	
Color 2 Upper Level	C_{CL2H}	C_{OUT}	V_{CC} = AV_{CC} = 5.0 V	1.97	2.08	2.19	V	
Color 2 Lower Level	C_{CL2L}			0.95	1.06	1.17	V	
Color 1 Upper Level	C_{CL1H}	C_{OUT}	V_{CC} = AV_{CC} = 5.0 V	1.75	1.86	1.97	V	
Color 1 Lower Level	C_{CL1L}			1.17	1.28	1.39	V	
Color Burst Upper Level	C_{BSTH}	C_{OUT}	V_{CC} = AV_{CC} = 5.0 V	1.80	1.91	2.02	V	
Color Burst Lower Level	C_{BSTL}			1.12	1.23	1.34	V	
Pedestal Level	V_{PDS}	C_{OUT}	V_{CC} = AV_{CC} = 5.0 V	1.46	1.57	1.68	V	

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Pin/Port	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
White Level	Y_{WHT}	Y_{OUT}	V_{CC} = AV$_{CC}$ = 5.0 V	2.78	2.89	3.00	V	
Black Level	Y_{BLK}	Y_{OUT}	V_{CC} = AV$_{CC}$ = 5.0 V	1.57	1.68	1.79	V	
Gray Level 1	Y_{GRY1}	Y_{OUT}	V_{CC} = AV$_{CC}$ = 5.0 V	1.69	1.80	1.91	V	
Gray Level 2	Y_{GRY2}			1.81	1.92	2.03	V	
Gray Level 3	Y_{GRY3}			1.92	2.03	2.14	V	
Gray Level 4	Y_{GRY4}			2.15	2.26	2.37	V	
Gray Level 5	Y_{GRY5}			2.27	2.38	2.49	V	
Gray Level 6	Y_{GRY6}			2.38	2.49	2.60	V	
Pedestal Level	Y_{PDS}	Y_{OUT}	V_{CC} = AV$_{CC}$ = 5.0 V	1.46	1.57	1.68	V	
SYNC Level	Y_{TIP}	Y_{OUT}	V_{CC} = AV$_{CC}$ = 5.0 V	0.84	1.00	1.16	V	

Fig. 12 – Outputs on C_{OUT} and Y_{OUT}



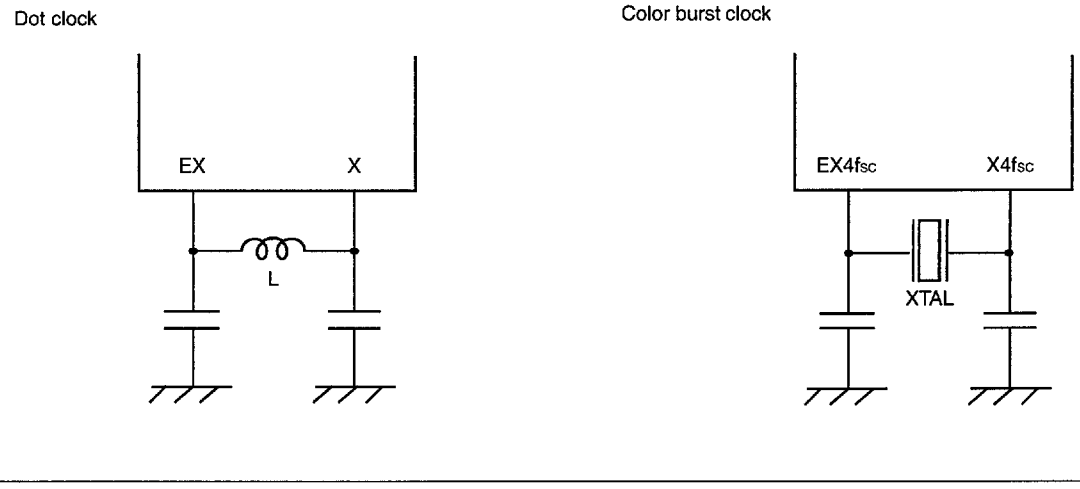
AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Oscillator Characteristics

Parameter	Symbol	Pin/Port	Value			Unit	Remarks
			Min.	Typ.	Max.		
Display Dot Clock Frequency	f_{DC}	EXD, XD	6	—	8	MHz	Input signal with duty 50% is required.
Color Burst Clock Frequency	$4f_{SC}$	EXS, XS	—	14.31818	—	MHz	Input signal with duty 50% is required. NTSC system
			—	17.734475	—	MHz	Input signal with duty 50% is required. PAL system
			—	14.302446	—	MHz	Input signal with duty 50% is required. PAL-M system

Fig. 13 – Clock Circuit Configuration



AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

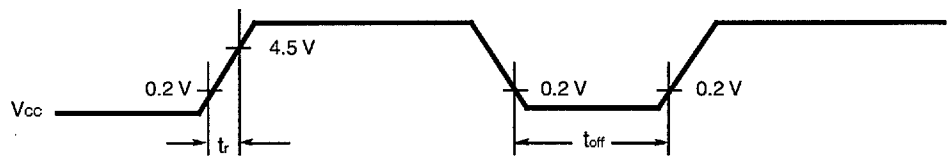
Serial I/O Interface Timing

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min.	Typ.	Max.		
Shift Clock Cycle Time	t_{CYC}	SCLK	1000	—	—	ns	
Shift Clock Pulse Width	t_{WCH}	SCLK	450	—	—	ns	
	t_{WCL}		450	—	—	ns	
Shift Clock Rise Time	t_{CR}	SCLK	—	—	200	ns	
Shift Clock Fall Time	t_{CF}	SCLK	—	—	200	ns	
Shift Clock Start Time	t_{SS}	SCLK	200	—	—	ns	
Data Setup Time	t_{SU}	SIN	200	—	—	ns	
Data Hold Time	t_H	SIN	100	—	—	ns	
Chip Select End TIme	t_{EC}	$\overline{CS}$	500	—	—	ns	
Chip Select Rise Time	t_{CRC}	$\overline{CS}$	—	—	200	ns	
Chip Select Fall Time	t_{CFC}	$\overline{CS}$	—	—	200	ns	
Horizontal Sync Rise Time	t_{HR}	$\overline{EXHSYN}$	—	—	200	ns	
Horizontal Sync Fall Time	t_{HF}	$\overline{EXHSYN}$	—	—	200	ns	
Vertical Sync Rise Time	t_{VR}	$\overline{EXVSYN}$	—	—	200	ns	
Vertical Sync Fall Time	t_{VF}	$\overline{EXVSYN}$	—	—	200	ns	
Horizontal Sync Signal Pulse Width	t_{WH}	$\overline{EXHSYN}$	4.1	—	5.7	µs	When H/V separate sync signals are input.
Vertical Sync Signal Pulse Width	t_{WV}	$\overline{EXVSYN}$	1	—	5	H	When H/V separate sync signals are input.
Horizontal Sync Signal Detective Pulse Width	t_{WCSH}	$\overline{EXHSYN}$	4.1	—	5.7	µs	When H/V composite sync signal is input.
Vertical Sync Signal Detective Pulse Width	t_{WCSV}	$\overline{EXVSYN}$	13	—	28	µs	When H/V composite sync signal is input.

Power-On Reset Timing

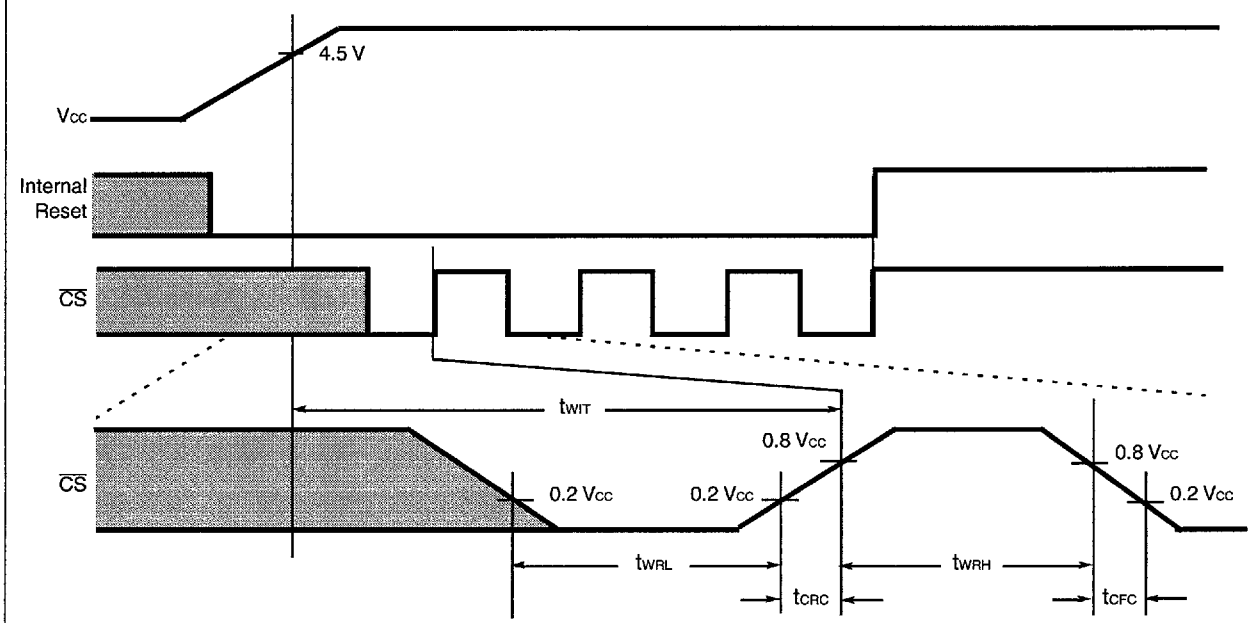
Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power Supply RIsing Time	t_r	0.05	50	ms	Required for the operation of the power-on reset circuit
Power Supply Shut-off Time	t_{off}	1.0	—	ms	Required for the accurate circuit operation repeatly.
$\overline{CS}$ rise time after power supply rising	t_{WIT}	450	—	ns	See Figure 17.
Power-on reset release pulse width	t_{WRH}	450	—	ns	See Figure 17.
	t_{WRL}	450	—		

Fig. 14 – Power-On Reset Timing



Power supply should be raised smoothly.

Fig. 15 – Power-On Reset Release Timing



RECOMMENDED EXTERNAL SYNC SIGNAL INPUT TIMING

Composite Sync Signal Input Timing

Parameter	NTSC	PAL-M	PAL	Unit	Remarks
Number of frame scanning lines	525		625	H	Note 1
Field frequency	59.94		50	Hz	
Line frequency	15734.264		15625	Hz	
Vertical blanking interval	19 to 21		25	H	Note 1
First equalizing pulse interval	3		2.5	H	Note 1
Vertical sync pulse interval	3		2.5	H	Note 1
Second equalizing pulse interval	3		2.5	H	Note 1
Equalizing pulse width	2.29 to 2.54	2.30 ±0.1	2.35 ±0.1	µs	
Equalizing pulse period	0.5		0.5	H	Note 1
Serrated pulse width	3.81 to 5.34	4.7 ±0.1	4.7 ±0.2	µs	
Serrated pulse period	0.5		0.5	H	Note 1
Horizontal sync signal period	63.555		64	µs	
Horizontal sync signal pulse width	4.7 ±0.1		4.7 ±0.2	µs	
Horizontal blanking time	10.5 to 11.4	10.9 ±0.2	12 ±0.3	µs	

Note 1: H is counted in units of horizontal sync signal periods (i.e., 1H = one horizontal sync signal period).

H/V Separation Sync Signal Input Timing

Parameter	NTSC	PAL-M	PAL	Unit	Remarks
Vertical sync signal frequency	59.94		50	Hz	
Vertical sync signal pulse width	1 to 5		1 to 4	H	Note 1
Horizontal sync signal period	63.555		64	µs	
Horizontal sync signal pulse width	4.7 ±0.1		4.7 ±0.2	µs	

Note 1: H is counted in units of horizontal sync signal periods (i.e., 1H = one horizontal sync signal period).

INTERNAL SYNC SIGNAL OUTPUT TIMING

Horizontal Timing

Parameter	NTSC Standard	PAL-M Standard	PAL Standard	Unit	Remarks
HPS	0	0	0	4•fsc Clock	See Figure 16.
EP1E	34	34	42	4•fsc Clock	
HPE	68	68	84	4•fsc Clock	
HBSTS	76	98	100	4•fsc Clock	
HBSTE	112	134	140	4•fsc Clock	
HBLKE	143	143	186	4•fsc Clock	
SP1S	388	388	484	4•fsc Clock	
EP2S	455	455	568	4•fsc Clock	
EP2E	489	489	610	4•fsc Clock	
SP2S	842	842	1050	4•fsc Clock	
HBLKS	888	888	1106	4•fsc Clock	
HPS	910	909	1135 (1137)*	4•fsc Clock	

* : The value in the parentheses is applied at the final raster.

Vertical Timing

Parameter		NTSC Standard	PAL-M Standard	PAL Standard	Unit	Remarks
VPS		0	0	0	0.5H	
VPE		6	6	5	0.5H	
EQPE		12	12	10	0.5H	
VBLKE		36	36	45	0.5H	
VBLKS		519	519	620	0.5H	
VPS	Interlace	525	525	625	0.5H	
	Non-interlace	526	524	624	0.5H	

The 0.5H in the above table indicate the count values of 1/2H on the horizontal sync signal.

Fig. 16 – NTSC/PAL/PAL-M Horizontal Timing

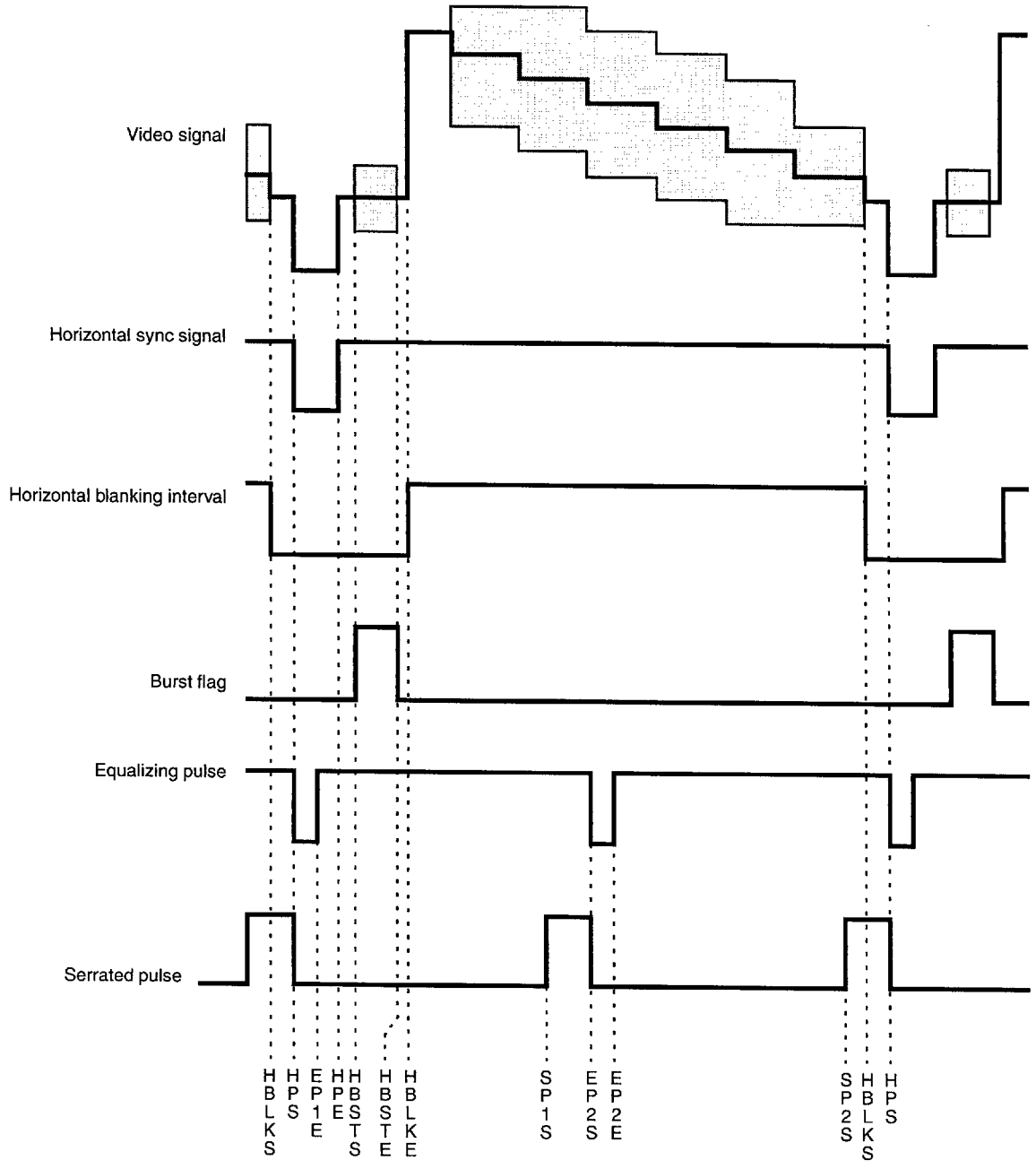


Fig. 17 – NTSC Vertical Timing

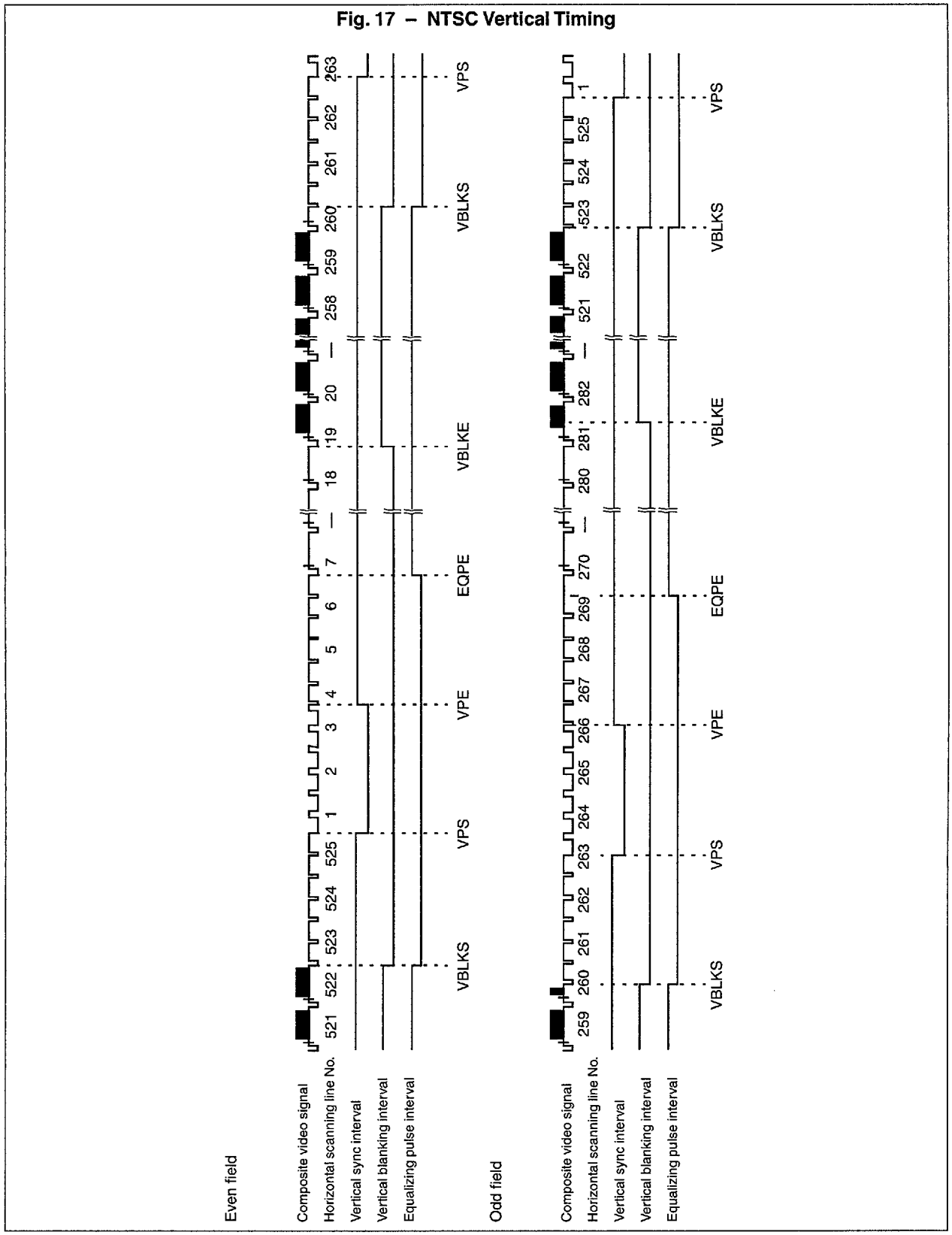
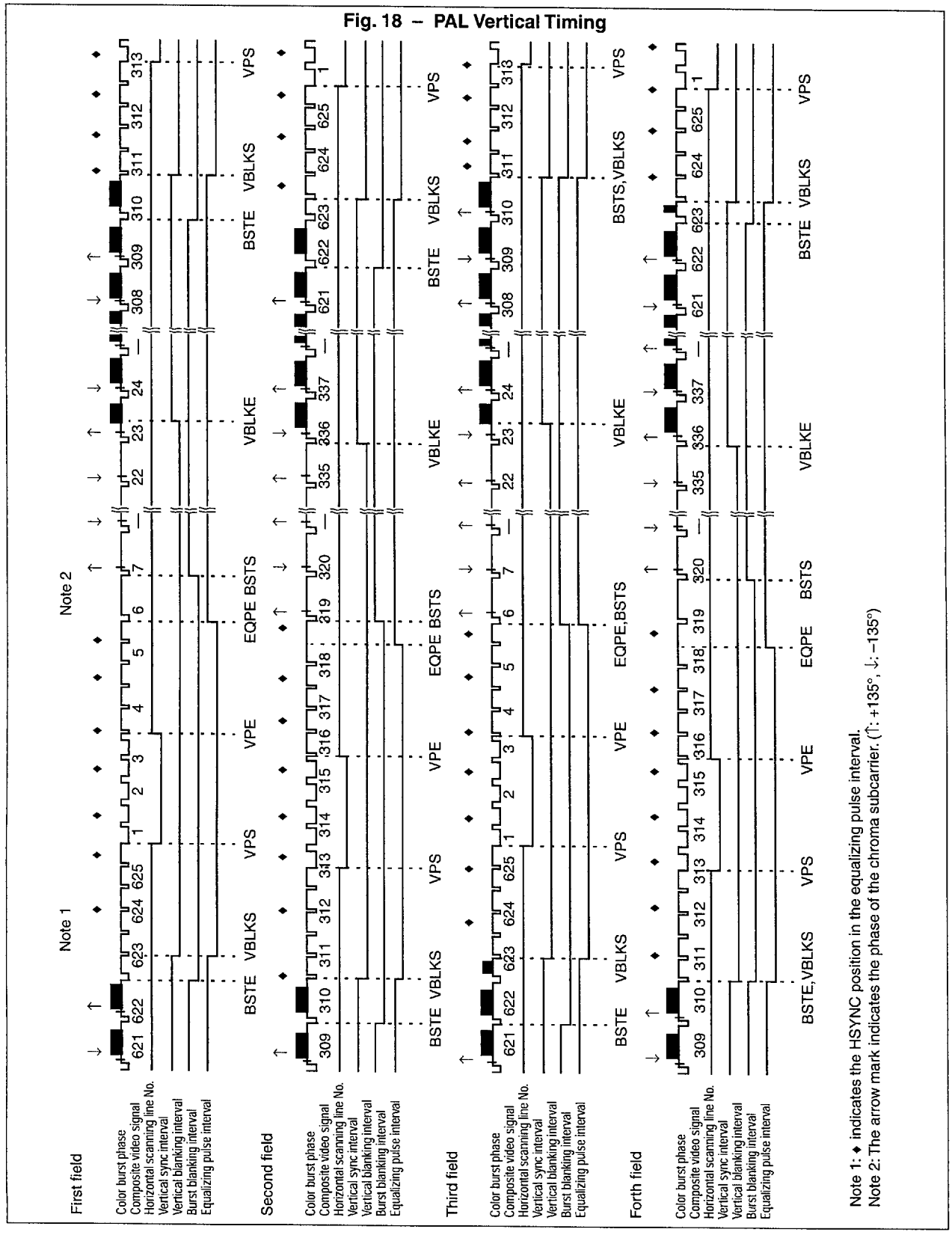


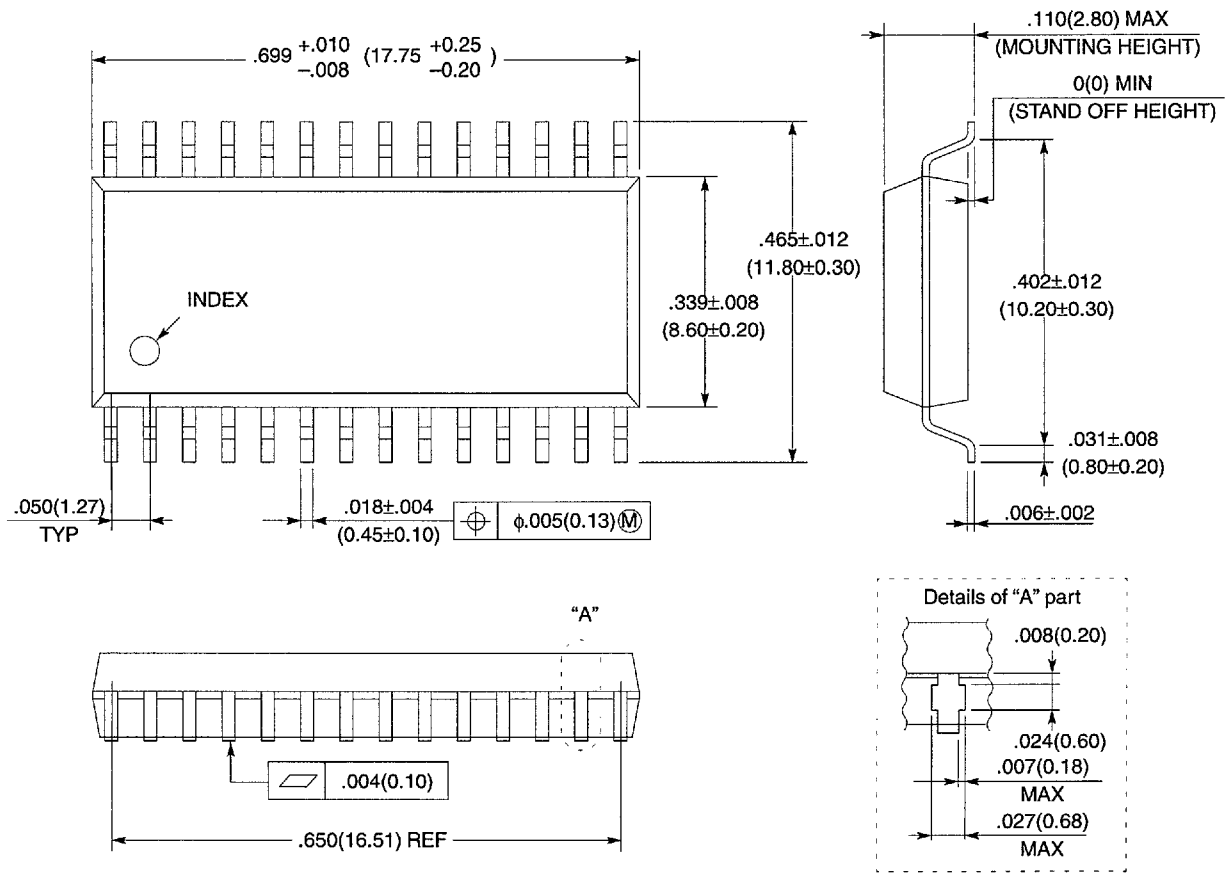
Fig. 18 – PAL Vertical Timing



■ PACKAGE DIMENSIONS

MB90089PF

28-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-28P-M02)



Dimensions in inches (millimeters)