FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-13502-5E

16-bit Proprietary Microcontroller

CMOS

F^2MC-16F MB90220 Series

MB90223/224/P224A/W224A
MB90P224B/W224B/V220

■ OUTLINE

The MB90220 series of general-purpose high-performance 16-bit microcontrollers has been developed primarily for applications that demand high-speed real-time processing and is suited for industrial applications, office automation equipment, process control, and other applications. The F^2MC-16F CPU is based on the F^2MC*-16 Family with improved high-level language support functions and task switching functions, as well as additional addressing modes.

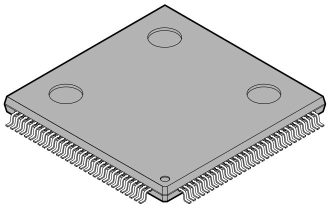
On-chip peripheral resources include a 4-channel PWC timer, a 4-channel ICU (Input Capture Unit), a 1-channel 24-bit timer counter, an 8-channel OCU (Output Compare Unit), a 6-channel 16-bit reload timer, a 2-channel 16-bit PPG timer, a 10-bit A/D converter with 16 inputs, and a 4-channel serial port with a UART function (one channel includes the CTS function).

The MB90P224B, MB90W224B, MB90224 is under development.

*: F^2MC stands for FUJITSU Flexible Microcontroller.

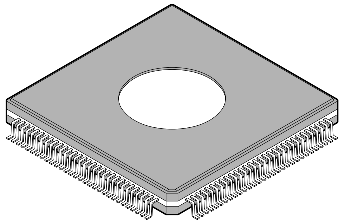
■ PACKAGE

120-pin Plastic QFP



(FPT-120P-M03)

120-pin Ceramic QFP



(FPT-120C-C02)

■ FEATURES

F²MC-16F CPU

- Minimum execution time: 62.5 ns/16 MHz oscillation (using a duty control system)
- Instruction sets optimized for controllers
  Upward object-compatible with the F²MC-16(H)
  Various data types (bit, byte, word, and long-word)
  Instruction cycle improved to speed up operation
  Extended addressing modes: 25 types
  High coding efficiency
  Access method (bank access with linear pointer)
  Enhanced multiplication and division instructions (with signed instructions added)
  Higher-precision operation using a 32-bit accumulator
- Extended intelligent I/O service (automatic transfer function independent of instructions)
  Access area expanded to 64 Kbytes
- Enhanced instruction set applicable to high-level language (C) and multitasking
  System stack pointer
  Enhanced pointer-indirect instructions
  Barrel shift instruction
  Stack check function
- Increased execution speed: 8-byte instruction queue
- Powerful interrupt functions: 8 levels and 28 sources

Peripheral resources

- Mask ROM : 64 Kbytes (MB90223)
  96 Kbytes (MB90224)
  EPROM : 96 Kbytes (MB90W224A/W224B)
- One-time PROM : 96 Kbytes (MB90P224A/P224B)
- RAM: 3 Kbytes (MB90223)
  4.5 Kbytes (MB90224/MB90W224A/P224A/W224B/P224B)
  5 Kbytes (MB90V220)
- General-purpose ports: max. 102 channels
- ICU (Input Capture Unit): 4 channels
- 24-bit timer counter: 1 channel
- OCU (Output Compare Unit): 8 channels
- PWC timer with time measurement function: 4 channels
- 10-bit A/D converter: 16 channels
- UART: 4 channels (one channel includes CTS function)
- 16-bit reload timer
  Toggled output, external clock, and gate functions: 6 channels
- 16-bit PPG timer: 2 channels
- DTP/External-interrupt inputs: 8 channels (of which five have edge detection function only)
- Write-inhibit RAM: 0.5 Kbytes (1 Kbyte for MB90V220)
- Timebase counter: 18 bits
- Clock gear function
- Low-power consumption mode
  Sleep mode
  Stop mode
  Hardware standby mode

Product description

- MB90223/224 are mask ROM product.
- MB90P224A/P224B are one-time PROM products.
- MB90W224A/W224B are EPROM products. ES only.
- Operating temperature of MB90P224A/W224A is –40°C to +85°C. (However, the AC characteristics is assured in –40°C to +70°C)
- Operation clock cycle of MB90223 is 10 MHz to 12 MHz.
- MB90V220 is a evaluation device for the program development. ES only.

■ PRODUCT LINEUP

Item \ Part number	MB90223	MB90224	MB90P224A MB90P224B	MB90W224A MB90W224B	MB90V220
Classification	Mask ROM product	Mask ROM product	One-time PROM product	EPROM product	Evaluation device
ROM size	64 Kbytes	96 Kbytes	96 Kbytes	96 Kbytes	None
RAM size	3 Kbytes	4.5 Kbytes	4.5 Kbytes	4.5 Kbytes	5 Kbytes
CPU functions	The number of instructions: 412 Instruction bit length: 8 or 16 bits Instruction length: 1 to 7 bytes Data bit length: 1, 4, 8, 16, or 32 bits Minimum execution time: 62.5 ns/16 MHz Interrupt processing time: 1.0 µs/16 MHz (min.)				
Ports	I/O ports (N-ch open-drain): 16 I/O ports (CMOS): 86 Total: 102				
ICU (Input Capture Unit)	Number of channels: 4 Rising edge/falling edge/both edges selectable				
24-bit timer counter	Number of channels: 1 Overflow interrupt, intermediate bit interrupt				
OCU (Output Compare Unit)	Number of channels: 8 Pin change source (match signal causes register value transfer/general-purpose port)				
PWC timer	Number of channels: 4 16-bit reload timer operation (operation clock cycle: 0.25 µs to 1.31 ms) 16-bit pulse-width count operation (Allowing continuous/one-shot measurement, H/L width measurement, inter-edge measurement, and divided-frequency measurement)				
10-bit A/D converter	Resolution: 10 bits Number of inputs: 16 Single conversion mode (conversion of each channel) Scan conversion mode (continuous conversion for up to 16 consecutive channels) Continuous conversion mode (repeated conversion of specified channel) Stop conversion mode (conversion every fixed cycle)				
UART	Number of channels: 4 (1 channel with CTS function) Clock-synchronous transfer mode (full-duplex double buffering, 7 to 9-bit data length, 2400 to 62500 bps) Asynchronous transfer mode (full-duplex double buffering, 7 to 9-bit data length, 2400 to 62500 bps)				
16-bit reload timer	Number of channels: 6 16-bit reload timer operation (operation clock cycle: 0.25 µs to 1.05 s)				

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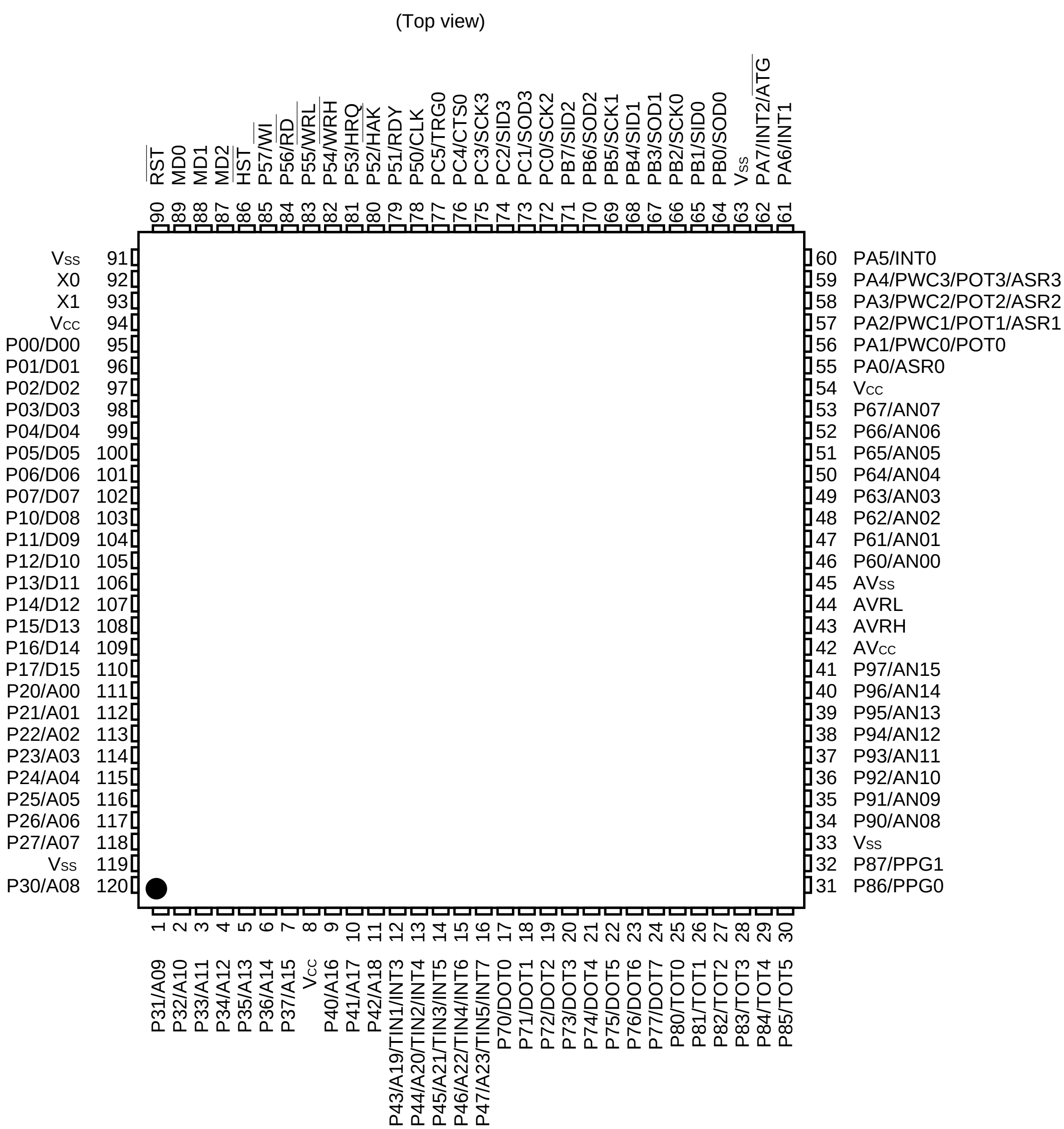
Item \ Part number	MB90223	MB90224	MB90P224A MB90P224B	MB90W224A MB90W224B	MB90V220
16-bit PPG timer	Number of channels: 2 16-bit PPG operation (operation clock cycle: 0.25 µs to 6 s)				
DTP/External interrupts	Number of inputs: 8 (of which five have edge detection function only) External interrupt mode (allowing interrupts to activate at four different request levels) Simple DMA transfer mode (allowing extended I^2OS to activate at two different request levels)				
Write-inhibited RAM	RAM size: 512 bytes (1 Kbyte for MB90V220) RAM write-protectable with $\overline{\text{WI}}$ pin				
Standby mode	stop mode (activated by software or hardware) and sleep mode				
Gear function	Machine clock operation frequency switching: 16 MHz, 8 MHz, 4 MHz, 1 MHz (at 16-MHz oscillation)				
Package	FPT-120P-M03			FPT-120C-C02	PGA-256C-A02

Note: MB90V220 is a evaluation device, therefore, the electrical characteristics are not assured.

■ DIFFERENCES BETWEEN MB90223/224 (MASK ROM PRODUCT) AND MB90P224A/W224A/P224B/W224B

Item \ Part number	MB90223	MB90224	MB90P224A MB90P224B	MB90W224A MB90W224B
ROM	Mask ROM 64 Kbytes	Mask ROM 96 Kbytes	OTPROM 96 Kbytes	EPROM 96 Kbytes
Pin functions: pin 87	MD2 pin		MD2/V_{PP} pin	

■ PIN ASSIGNMENT



(FPT-120P-M03)
(FPT-120C-C02)

■ PIN DESCRIPTION

Pin no. QFP*	Pin name	Circuit type	Function
92, 93	X0, X1	A	Crystal oscillation pins (16 MHz)
89 to 87	MD0 to MD2	D	Operation mode specification input pins Connect directly to V_{CC} or V_{SS}.
90	$\overline{RST}$	G	External reset request input
86	$\overline{HST}$	E	Hardware standby input pin
95 to 102	P00 to P07	C	General-purpose I/O ports This function is valid only in single-chip mode.
	D00 to D07		Output pins for low-order 8 bits of the external address bus. This function is valid only in modes where the external bus is enabled.
103 to 110	P10 to P17	C	General-purpose I/O ports This function is valid only in single-chip mode or when the external bus is enabled and the 8-bit data bus specification has been made.
	D08 to D15		I/O pins for higher-order 8 bits of the external data bus This function is valid only when the external bus is enabled and the 16-bit bus specification has been made.
111 to 118	P20 to P27	C	General-purpose I/O ports This function is valid only in single-chip mode.
	A00 to A07		Output pins for lower-order 8 bits of the external address bus This function is valid only in modes where the external bus is enabled.
120, 1 to 7	P30, P31 to P37	C	General-purpose I/O ports This function is valid either in single-chip mode or when the address mid-order control register specification is “port”.
	A08, A09 to A15		Output pins for mid-order 8 bits of the external address bus This function is valid in modes where the external bus is enabled and the address mid-order control register specification is “address”.
9 to 11	P40 to P42	C	General-purpose I/O ports This function is valid either in single-chip mode or when the address high-order control register specification is “port”.
	A16 to A18		Output pins for higher-order 8 bits of the external address bus This function is valid in modes where the external bus is enabled and the address high-order control register specification is “address”.
12 to 16	P43 to P47	C	General-purpose I/O ports This function is valid when either single-chip mode is enabled or the address higher-order control register specification is “port”.
	A19 to A23		Output pins for higher-order 8 bits of the external address bus This function is valid in modes where the external bus is enabled and the address higher-order control register specification is “address”.
	TIN1 to TIN5		16-bit reload timer input pins This function is valid when the timer input specification is “enabled”. The data on the pins is read as timer input (TIN1 to TIN5).

* : FPT-120P-M03, FPT-120C-C02

(Continued)

Pin no. QFP*	Pin name	Circuit type	Function
12 to 16	INT3 to INT7	C	External interrupt request input pins When external interrupts are enabled, these inputs may be used suddenly at any time; therefore, it is necessary to stop output by other functions on these pins, except when using them for output deliberately.
78	P50	C	General-purpose I/O port This function is valid in single-chip mode and when the CLK output specification is disabled.
	CLK		CLK output pin This function is valid in modes where the external bus is enabled and the CLK output specification is enabled.
79	P51	C	General-purpose I/O port This function is valid in single-chip mode or when the ready function is disabled.
	RDY		Ready input pin This function is valid in modes where the external bus is enabled and the ready function is enabled.
80	P52	C	General-purpose I/O port This function is valid in single-chip mode or when the hold function is disabled.
	$\overline{\text{HAK}}$		Hold acknowledge output pin This function is valid in modes where the external bus is enabled and the hold function is enabled.
81	P53	C	General-purpose I/O port This function is valid in single-chip mode or external bus mode and when the hold function is disabled.
	HRQ		Hold request input pin This function is valid in modes where the external bus is enabled and the hold function is enabled. During this operation, the input may be used suddenly at any time; therefore, it is necessary to stop output by other fuctions on this pin, except when using it for output deliberately.
82	P54	C	General-purpose I/O port This function is valid in single-chip mode, when the external bus is in 8-bit mode, or when $\overline{\text{WRH}}$ pin output is disabled.
	$\overline{\text{WRH}}$		Write strobe output pin for the high-order 8 bits of the data bus This function is valid in modes where the external bus is enabled, the external bus is in 16-bit mode, and $\overline{\text{WRH}}$ pin output is enabled.
83	P55	C	General-purpose I/O port This function is valid in single-chip mode or when $\overline{\text{WRL}}$ pin output is disabled.
	$\overline{\text{WRL}}$		Write strobe output pin for the low-order 8 bits of the data bus This function is valid in modes where the external bus is enabled and $\overline{\text{WRL}}$ pin output is enabled.

* : FPT-120P-M03, FPT-120C-C02

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Pin no. QFP*	Pin name	Circuit type	Function
84	P56	C	General-purpose I/O port This function is valid in single-chip mode. This function is valid in modes where the external bus is valid.
	$\overline{RD}$		Read strobe output pin for the data bus This function is valid in modes where the external bus is enabled.
85	P57	B	General-purpose I/O port This function is always valid. When these pins are open in input mode, through current may leak in stop mode/reset mode, be sure to fix these pins to V_{CC}/V_{SS} level to use these pins in input mode.
	$\overline{WI}$		RAM write disable request input During this operation, the input may be used suddenly at any time; therefore, it is necessary to stop output by other fuctions on this pin, except when using it for output deliberately.
46 to 53	P60 to P67	F	Open-drain I/O ports This function is valid when the analog input enable register specification is “port”.
	AN00 to AN07		10-bit A/D converter analog input pins This function is valid when the analog input enable register specification is “analog input”.
17 to 24	P70 to P77	C	General-purpose I/O ports This function is valid when the output specification for DOT0 to DOT7 is “disabled”.
	DOT0 to DOT7		This function is valid when OCU (output compare unit) output is enabled.
25 to 30	P80 to P85	C	General-purpose I/O ports This function is valid when the output specification for TOT0 to TOT5 is “disabled”.
	TOT0 to TOT5		16-bit reload timer output pins (TOT0 to TOT5)
31, 32	P86, P87	C	General-purpose I/O ports This function is valid when the PPG0, and PPG1 output specification is “disabled”.
	PPG0, PPG1		16-bit PPG timer output pins This function is valid when the PPG control/status register specification is “PPG output pins”.
34 to 41	P90 to P97	F	Open-drain I/O ports This function is valid when the analog input enable register specification is “port”.
	AN08 to AN15		10-bit A/D converter analog input pins This function is valid when the analog input enable register specification is “analog input”.

* : FPT-120P-M03, FPT-120C-C02

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Pin no. QFP*	Pin name	Circuit type	Function
55	PA0	C	General-purpose I/O port This function is always valid.
	ASR0		ICU (input capture unit) input pin This function is valid during ICU (input capture unit) input operations.
56	PA1	C	General-purpose I/O port This function is always valid.
	PWC0		PWC input pin During PWC0 input operations, this input may be used suddenly at any time; therefore, it is necessary to stop output by other functions on this pin, except when using it for output deliberately.
	POT0		PWC output pin This function is valid during PWC output operations.
57 to 59	PA2 to PA4	C	General-purpose I/O ports This function is always valid.
	PWC1 to PWC3		PWC input pins This function is valid during PWC input operations. During PWC1 to PWC3 input operations, this input may be used suddenly at any time; therefore, it is necessary to stop output by other functions on this pin, except when using it for output deliberately.
	POT1 to POT3		PWC output pins This function is valid during PWC output operations.
	ASR1 to ASR3		ICU (input capture unit) input pins This function is valid during ICU (input capture unit) input operations.
60, 61	PA5, PA6	B	General-purpose I/O ports This function is always valid. When these pins are open in input mode, through current may leak in stop mode/reset mode, be sure to fix these pins to V_{CC}/V_{SS} level to use these pins in input mode.
	INT0, INT1		DTP/External interrupt request input pins When DTP/external interrupts are enabled, these inputs may be used suddenly at any time; therefore, it is necessary to stop output by other functions on these pins, except when using them for output deliberately. When these pins are open in input mode, through current may leak in stop mode/reset mode, be sure to fix these pins to V_{CC}/V_{SS} level to use these pins in input mode.
62	PA7	B	General-purpose I/O port This function is always valid. When these pins are open in input mode, through current may leak in stop mode/reset mode, be sure to fix these pins to V_{CC}/V_{SS} level to use these pins in input mode.

* : FPT-120P-M03, FPT-120C-C02

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Pin no. QFP*	Pin name	Circuit type	Function
62	INT2	B	DTP/External interrupt request input pin When DTP/external interrupts are enabled, these inputs may be used suddenly at any time; therefore, it is necessary to stop output by other functions on these pins, except when using them for output deliberately. When these pins are open in input mode, through current may leak in stop mode/reset mode, be sure to fix these pins to V_{CC}/V_{SS} level to use these pins in input mode.
	$\overline{ATG}$		10-bit A/D converter external trigger input pin When these pins are open in input mode, through current may leak in stop mode/reset mode, be sure to fix these pins to V_{CC}/V_{SS} level to use these pins in input mode.
64	PB0	C	General-purpose I/O port This function is valid when the UART0 (ch.0) serial data output specification is “disabled”.
	SOD0		UART0 (ch.0) serial data output This function is valid when the UART0 (ch.0) serial data output specification is “enabled”.
65	PB1	C	General-purpose I/O port This function is always valid.
	SID0		UART0 (ch.0) serial data input pin During UART0 (ch.0) input operations, this input may be used suddenly at any time; therefore, it is necessary to stop output by other functions on this pin, except when using it for output deliberately.
66	PB2	C	General-purpose output port This function is valid when the UART0 (ch.0) clock output specification is “disabled”.
	SCK0		UART0 (ch.0) clock output pin The clock output function is valid when the UART0 (ch.0) clock output specification is “enabled”. UART0 (ch.0) external clock input pin. This function is valid when the port is in input mode and the UART0 (ch.0) specification is external clock mode.
67	PB3	C	General-purpose I/O port This function is valid when the UART0 (ch.1) serial data output specification is “disabled”.
	SOD1		UART0 (ch.1) serial data output pin This function is valid when the UART0 (ch.1) serial data output specification is “enabled”.
68	PB4	C	General-purpose I/O port This function is always valid.
	SID1		UART0 (ch.1) serial data input pin During UART0 (ch.1) input operations, this input may be used suddenly at any time; therefore, it is necessary to stop output by other functions on this pin, except when using it for output deliberately.

* : FPT-120P-M03, FPT-120C-C02

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Pin no. QFP*	Pin name	Circuit type	Function
69	PB5	C	General-purpose I/O port This function is valid when the UART0 (ch.1) clock output specification is “disabled”.
	SCK1		UART0 (ch.1) clock output pin The clock output function is valid when the UART0 (ch.1) clock output specification is “enabled”. UART0 (ch.1) external clock input pin This function is valid when the port is in input mode and the UART0 (ch.1) specification is external clock mode.
70	PB6	C	General-purpose I/O port This function is valid when the UART0 (ch.2) serial data output specification is “disabled”.
	SOD2		UART0 (ch.2) serial data output pin This function is valid when the UART0 (ch.2) serial data output specification is “enabled”.
71	PB7	C	General-purpose I/O port This function is always valid.
	SID2		UART0 (ch.2) serial data input pin During UART0 (ch.2) input operations, this input may be used suddenly at any time; therefore, it is necessary to stop output by other functions on this pin, except when using it for output deliberately.
72	PC0	C	General-purpose I/O port This function is valid when the UART0 (ch.2) clock output specification is “disabled”.
	SCK2		UART0 (ch.2) clock output pin The clock output function is valid when the UART0 (ch.2) clock output specification is “enabled”. UART0 (ch.2) external clock input pin This function is valid when the port is in input mode and the UART0 (ch.2) specification is external clock mode.
73	PC1	C	General-purpose I/O port This function is valid when the UART1 serial data output specification is “disabled”.
	SOD3		UART1 serial data output pin This function is valid when the UART1 serial data output specification is “enabled”.
74	PC2	C	General-purpose I/O port This function is always valid.
	SID3		UART1 serial data input pin During UART1 input operations, this input may be used suddenly at any time; therefore, it is necessary to stop output by other functions on this pin, except when using it for output deliberately.

* : FPT-120P-M03, FPT-120C-C02

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Pin no. QFP*	Pin name	Circuit type	Function
75	PC3	C	General-purpose I/O port This function is valid when the UART1 clock output specification is “disabled”.
	SCK3		UART1 clock output pin The clock output function is valid when the UART1 clock output specification is “enabled”. UART1 external clock input pin This function is valid when the port is in input mode and the UART1 specification is external clock mode.
76	PC4	C	General-purpose I/O port This function is always valid.
	CTS0		UART0 (ch.0) Clear To Send input pin When the UART0 (ch.0) CTS function is enabled, this input may be used suddenly at any time; therefore, it is necessary to stop output by other functions on this pin, except when using it for output deliberately.
77	PC5	C	General-purpose I/O port This function is always valid.
	TRG0		16-bit PPG timer trigger input pin This function is valid when the 16-bit PPG timer trigger input specification is enabled. The data on this pin is read as 16-bit PPG timer trigger input (TRG0). During this operation, the input may be used suddenly at any time; therefore, it is necessary to stop output by other functions on this pin, except when using it for output deliberately.
8, 54, 94	V_{CC}	Power supply	Power supply for digital circuitry
33, 63, 91, 119	V_{SS}	Power supply	Ground level for digital circuitry
42	AV_{CC}	Power supply	Power supply for analog circuitry When turning this power supply on or off, always be sure to first apply electric potential equal to or greater than AV_{CC} to V_{CC}. During normal operation AV_{CC} should be equal to V_{CC}.
43	AVRH	Power supply	Reference voltage input for analog circuitry When turning this pin on or off, always be sure to first apply electric potential equal to or greater than AVRH to AV_{CC}.
44	AVRL	Power supply	Reference voltage input for analog circuitry
45	AV_{SS}	Power supply	Ground level for analog circuitry

* : FPT-120P-M03, FPT-120C-C02

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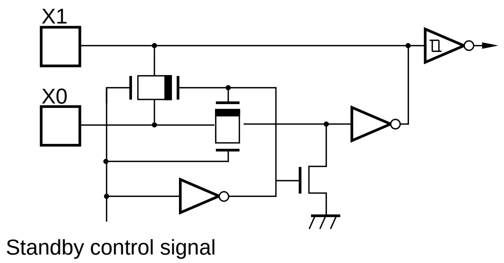
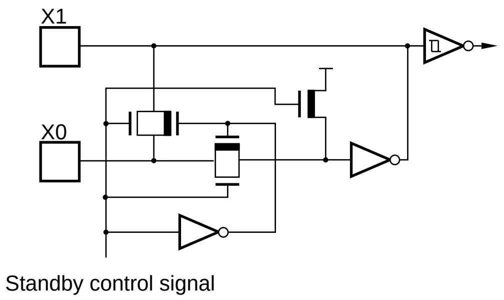
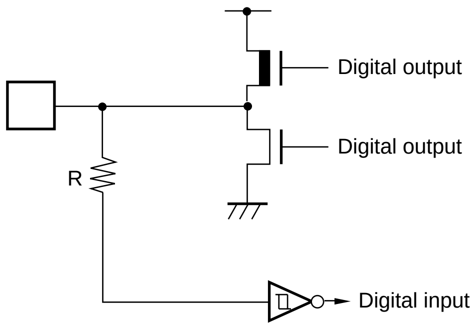
■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		• Oscillation feedback resistor: Approx. 1 MΩ MB90223 MB90224 MB90P224B MB90W224B
		• Oscillation feedback resistor: Approx. 1 MΩ MB90P224A MB90W224A
B		• CMOS-level output • CMOS-level hysteresis input with no standby control

Note: The pull-up and pull-down resistors are always connected, regardless of the state.

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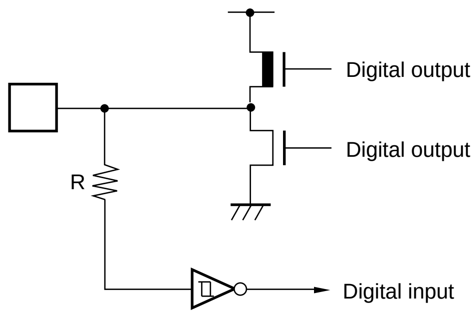
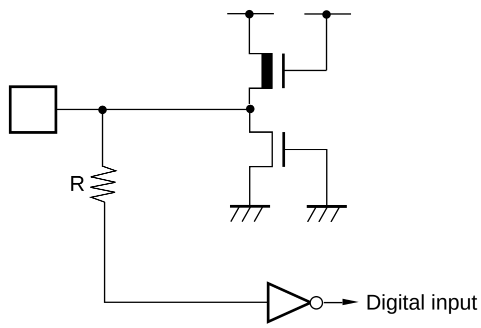
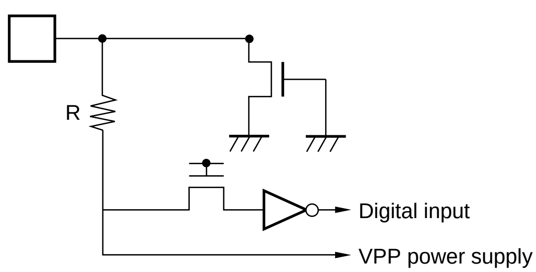
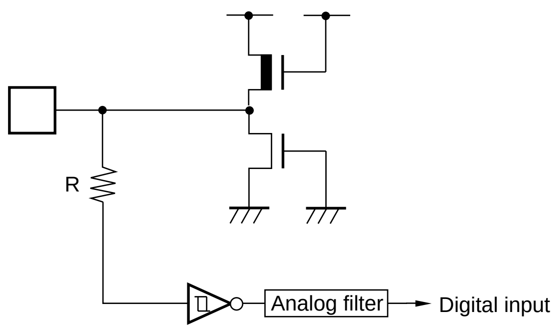
Type	Circuit	Remarks
C		• CMOS-level output • CMOS-level hysteresis input with standby control
D		• CMOS-level input with no standby control Mask ROM products only: MD2: with pull-down resistor MD1: with pull-up resistor MD0: with pull-down resistor
		• CMOS-level input with no standby control MD2 of OTPROM products/EPROM products only
E		• CMOS-level hysteresis input with no standby control • With input analog filter (40 ns Typ.)

Note: The pull-up and pull-down resistors are always connected, regardless of the state.

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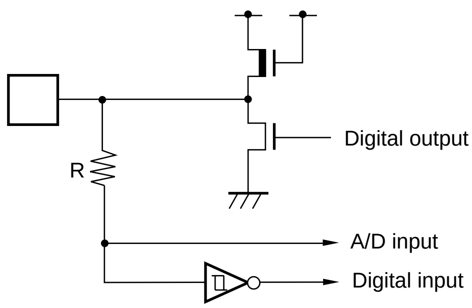
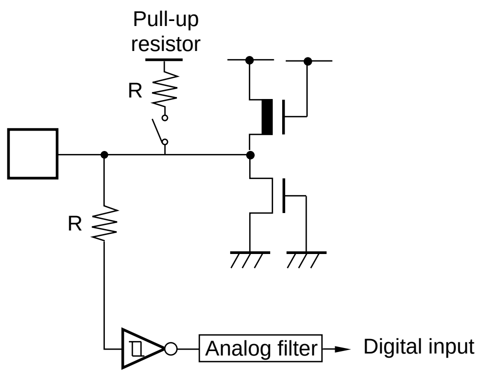
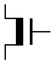
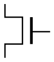
Type	Circuit	Remarks
F		• N-channel open-drain output • CMOS-level hysteresis input with A/D control and with standby control
G		• CMOS-level hysteresis input with no standby control and with pull-up resistor • With input analog filter (40 ns Typ.) MB90223, MB90224: $\overline{\text{RST}}$ pin can be set to with or without a pull-up resistor by a mask option. MB90P224A: With pull-up resistor MB90W224A: With pull-up resistor MB90P224B: With no pull-up resistor MB90W224B: With no pull-up resistor

 : P-type transistor  : N-type transistor

Note: The pull-up and pull-down resistors are always connected, regardless of the state.

■ HANDLING DEVICES

1. Preventing Latchup

CMOS ICs may cause latchup when a voltage higher than V_{CC} or lower than V_{SS} is applied to input or output pins other than medium-and high-voltage pins, or when a voltage exceeding the rating is applied between V_{CC} and V_{SS}.

If latch-up occurs, the power supply current increases rapidly, sometimes resulting in thermal breakdown of the device. Use meticulous care not to let any voltage exceed the maximum rating.
Also, take care to prevent the analog power supply (AV_{CC} and AVRH) and analog input from exceeding the digital power supply (V_{CC}) when the analog system power supply is turned on and off.

2. Treatment of Unused Input Pins

Leaving unused input pins open could cause malfunctions. They should be connected to a pull-up or pull-down resistor.

3. Treatment of Pins when A/D is not Used

Connect to be AV_{CC} = AVRH = V_{CC} and AV_{SS} = AVRL = V_{SS} even if the A/D converter is not in use.

4. Precautions when Using an External Input

To reset the internal circuit properly by the “L” level input to the $\overline{RST}$ pin, the “L” level input to the $\overline{RST}$ pin must be maintained for at least five machine cycles. Pay attention to it if the chip uses external clock input.

5. V_{CC} and V_{SS} Pins

Apply equal potential to the V_{CC} and V_{SS} pins.

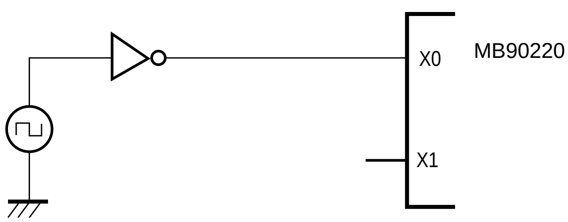
6. Supply Voltage Variation

The operation assurance range for the V_{CC} supply voltage is as given in the ratings. However, sudden changes in the supply voltage can cause misoperation, even if the voltage remains within the rated range. Therefore, it is important to supply a stable voltage to the IC. The recommended power supply control guidelines are that the commercial frequency (50 to 60 Hz) ripple variation (P-P value) on V_{CC} should be less than 10% of the standard V_{CC} value and that the transient rate of change during sudden changes, such as during power supply switching, should be less than 0.1 V/ms.

7. Notes on Using an External Clock

When using an external clock, drive the X0 pin as illustrated below. When an external clock is used, oscillation stabilization time is required even for power-on reset and wake-up from stop mode.

- **Use of External Clock**



Note: When using an external clock, be sure to input external clock more than 6 machine cycles after setting the $\overline{HST}$ pin to “L” to transfer to the hardware standby mode.

8. Power-on Sequence for A/D Converter Power Supplies and Analog Inputs

Be sure to turn on the digital power supply (V_{CC}) before applying voltage to the A/D converter power supplies (AV_{CC}, AVRH, and AVRL) and analog inputs (AN00 to AN15).

When turning power supplies off, turn off the A/D converter power supplies (AV_{CC}, AVRH, and AVRL) and analog inputs (AN00 to AN15) first, then the digital power supply (V_{CC}).

When turning AVRH on or off, be careful not to let it exceed AV_{CC}.

■ PROGRAMMING FOR MB90P224A/P224B/W224A/W224B

In EPROM mode, the MB90P224A/P224B/W224A/W224B functions equivalent to the MBM27C1000. This allows the EPROM to be programmed with a general-purpose EPROM programmer by using the dedicated socket adapter (do not use the electronic signature mode).

1. Program Mode

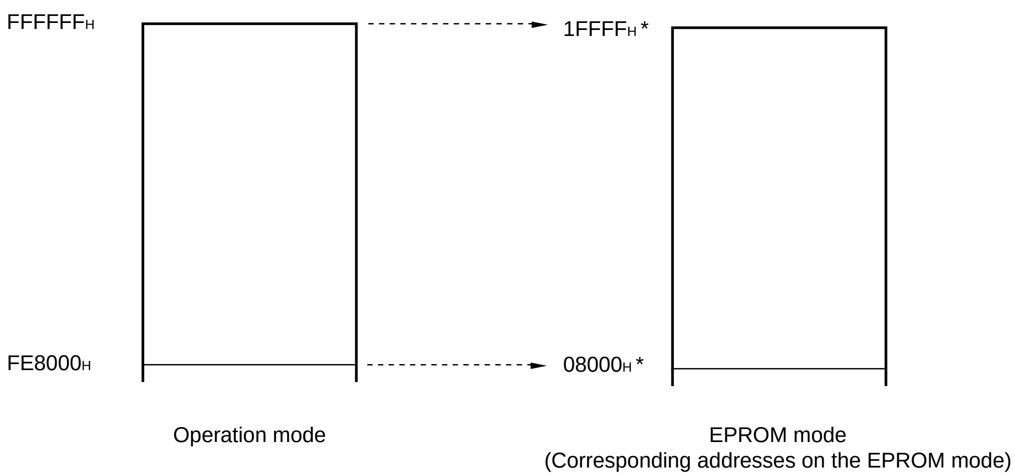
When shipped from Fujitsu, and after each erasure, all bits (96 K × 8 bits) in the MB90P224A/P224B/W224A/W224B are in the “1” state. Data is written to the ROM by selectively programming “0’s” into the desired bit locations. Bits cannot be set to “1” electrically.

2. Programming Procedure

(1) Set the EPROM programmer to MBM27C1000.

(2) Load program data into the EPROM programmer at 08000_H to $1FFFF_H$.

Note that ROM addresses $FE8000_H$ to $FFFFFF_H$ in the operation mode in the MB90P224A/P224B/W224A/W224B series assign to 08000_H to $1FFFF_H$ in the EPROM mode (on the EPROM programmer).



* : Be sure to set the programming, the start address and the stop address on the EPROM programmer to 08000_H/$1FFFF_H$.

(3) Mount the MB90P224A/P224B/W224A/W224B on the adapter socket, then fit the adapter socket onto the EPROM programmer. When mounting the device and the adapter socket, pay attention to their mounting orientations.

(4) Start programming the program data to the device.

(5) If programming has not successfully resulted, connect a capacitor of approx. 0.1 µF between V_{CC} and GND, between V_{PP} and GND.

Note: The mask ROM products (MB90223, MB90224) does not support EPROM mode. Data cannot, therefore, be read by the EPROM programmer.

3. EPROM Programmer Socket Adapter and Recommended Programmer Manufacturer

Part No.			MB90P224B
Package			QFP-120
Compatible socket adapter Sun Hayato Co., Ltd.			ROM-120QF-32DP-16F
Recommended programmer manufacturer and programmer name	**Advantest corp.**	**R4945A (main unit) + R49451A (adapter)**	Recommended

Inquiry: Sun Hayato Co., Ltd.: TEL: (81)-3-3986-0403
FAX: (81)-3-5396-9106
Advantest Corp.: TEL: Except JAPAN (81)-3-3930-4111

4. Erase Procedure

Data written in the MB90W224A/W224B is erased (from “0” to “1”) by exposing the chip to ultraviolet rays with a wavelength of 2,537 Å through the translucent cover.

Recommended irradiation dosage for exposure is 10 Wsec/cm^2. This amount is reached in 15 to 20 minutes with a commercial ultraviolet lamp positioned 2 to 3 cm above the package (when the package surface illuminance is 1200 µW/cm^2).

If the ultraviolet lamp has a filter, remove the filter before exposure. Attaching a mirrored plate to the lamp increases the illuminance by a factor of 1.4 to 1.8, thus shortening the required erasure time. If the translucent part of the package is stained with oil or adhesive, transmission of ultraviolet rays is degraded, resulting in a longer erasure time. In that case, clean the translucent part using alcohol (or other solvent not affecting the package).

The above recommended dosage is a value which takes the guard band into consideration and is a multiple of the time in which all bits can be evaluated to have been erased. Observe the recommended dosage for erasure; the purpose of the guard band is to ensure erasure in all temperature and supply voltage ranges. In addition, check the life span of the lamp and control the illuminance appropriately.

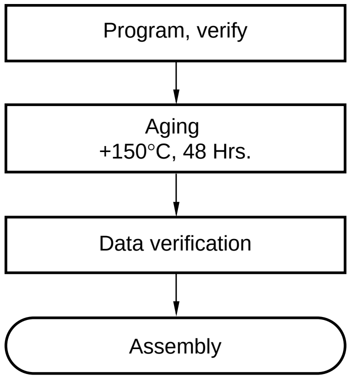
Data in the MB90W224A/W224B is erased by exposure to light with a wavelength of 4,000 Å or less.

Data in the device is also erased even by exposure to fluorescent lamp light or sunlight although the exposure results in a much lower erasure rate than exposure to 2,537 Å ultraviolet rays. Note that exposure to such lights for an extended period will therefore affect system reliability. If the chip is used where it is exposed to any light with a wavelength of 4,000 Å or less, cover the translucent part, for example, with a protective seal to prevent the chip from being exposed to the light.

Exposure to light with a wavelength of 4,000 to 5,000 Å or more will not erase data in the device. If the light applied to the chip has a very high illuminance, however, the device may cause malfunction in the circuit for reasons of general semiconductor characteristics. Although the circuit will recover normal operation when exposure is stopped, the device requires proper countermeasures for use in a place exposed continuously to such light even though the wavelength is 4,000 Å or more.

5. Recommended Screening Conditions

High temperature aging is recommended as the pre-assembly screening procedure.



6. Programming Yeild

MB90P224A/P224B cannot be write-tested for all bits due to their nature. Therefore the write yield cannot always be guaranteed to be 100%.

7. Pin Assignments in EPROM Mode

(1) Pins Compatible with MBM27C1000

MBM27C1000		MB90P224A/P224B/ MB90W224A/W224B	
Pin no.	Pin name	Pin no.	Pin name
1	V_{PP}	87	MD2 (V_{PP})
2	OE	83	P55
3	A15	7	P37
4	A12	4	P34
5	A07	118	P27
6	A06	117	P26
7	A05	116	P25
8	A04	115	P24
9	A03	114	P23
10	A02	113	P22
11	A01	112	P21
12	A00	111	P20
13	D00	95	P00
14	D01	96	P01
15	D02	97	P02
16	GND	33, 63, 91,119	V_{SS}

MBM27C1000		MB90P224A/P224B/ MB90W224A/W224B	
Pin no.	Pin name	Pin no.	Pin name
32	V_{CC}	8, 54, 94	V_{CC}
31	PGM	84	P56
30	N.C.	—	—
29	A14	6	P36
28	A13	5	P35
27	A08	120	P30
26	A09	1	P31
25	A11	3	P33
24	A16	9	P40
23	A10	2	P32
22	CE	82	P54
21	D07	102	P07
20	D06	101	P06
19	D05	100	P05
18	D04	99	P04
17	D03	98	P03

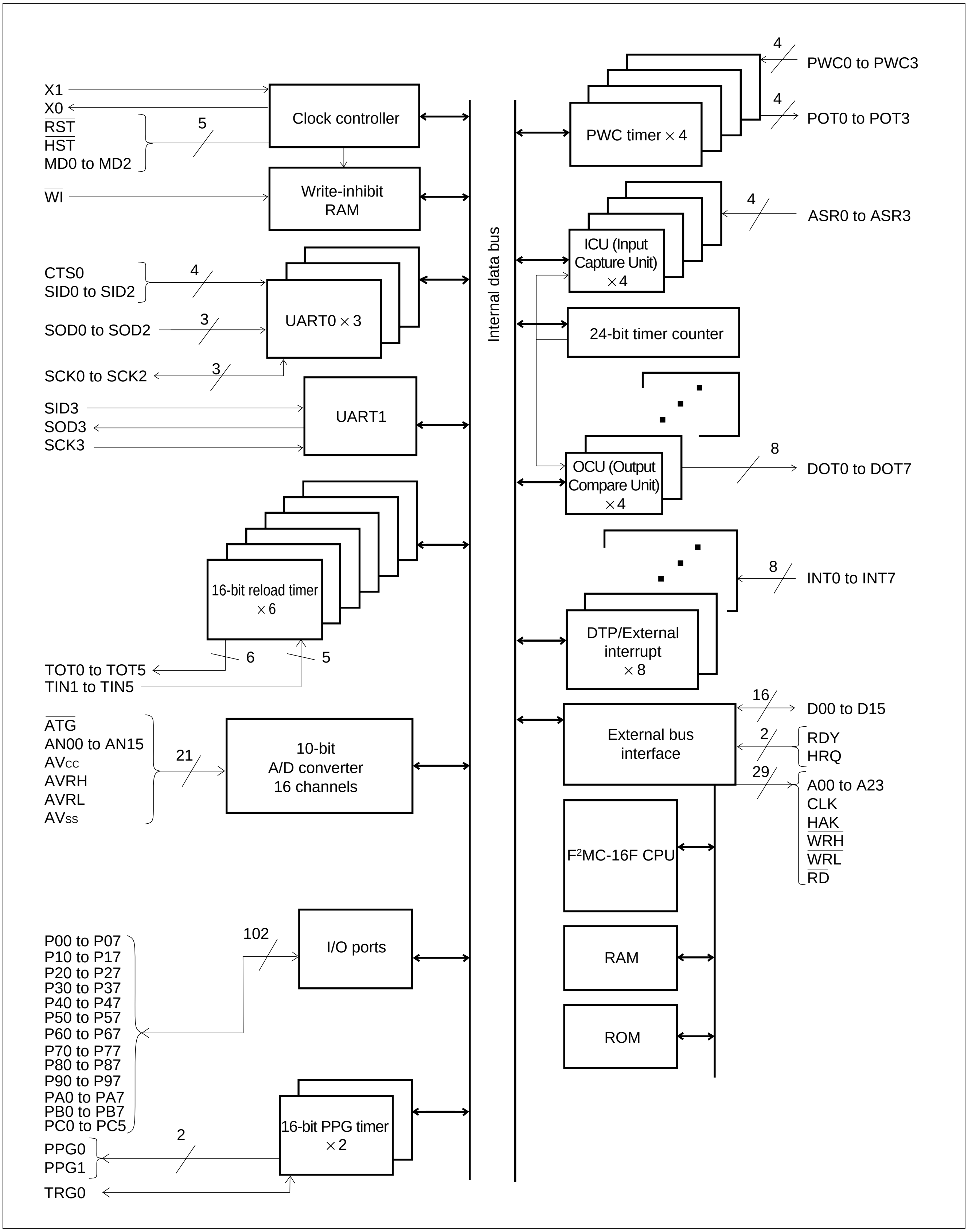
(2) Power Supply and GND Connection Pins

Type	Pin no.	Pin name
Power supply	89 88 86 8, 54, 94	MD0 MD1 $\overline{\text{HST}}$ V_{CC}
GND	33, 63, 91, 119 44 45 80 81 90	V_{SS} AVRL AV_{SS} P52 P53 $\overline{\text{RST}}$

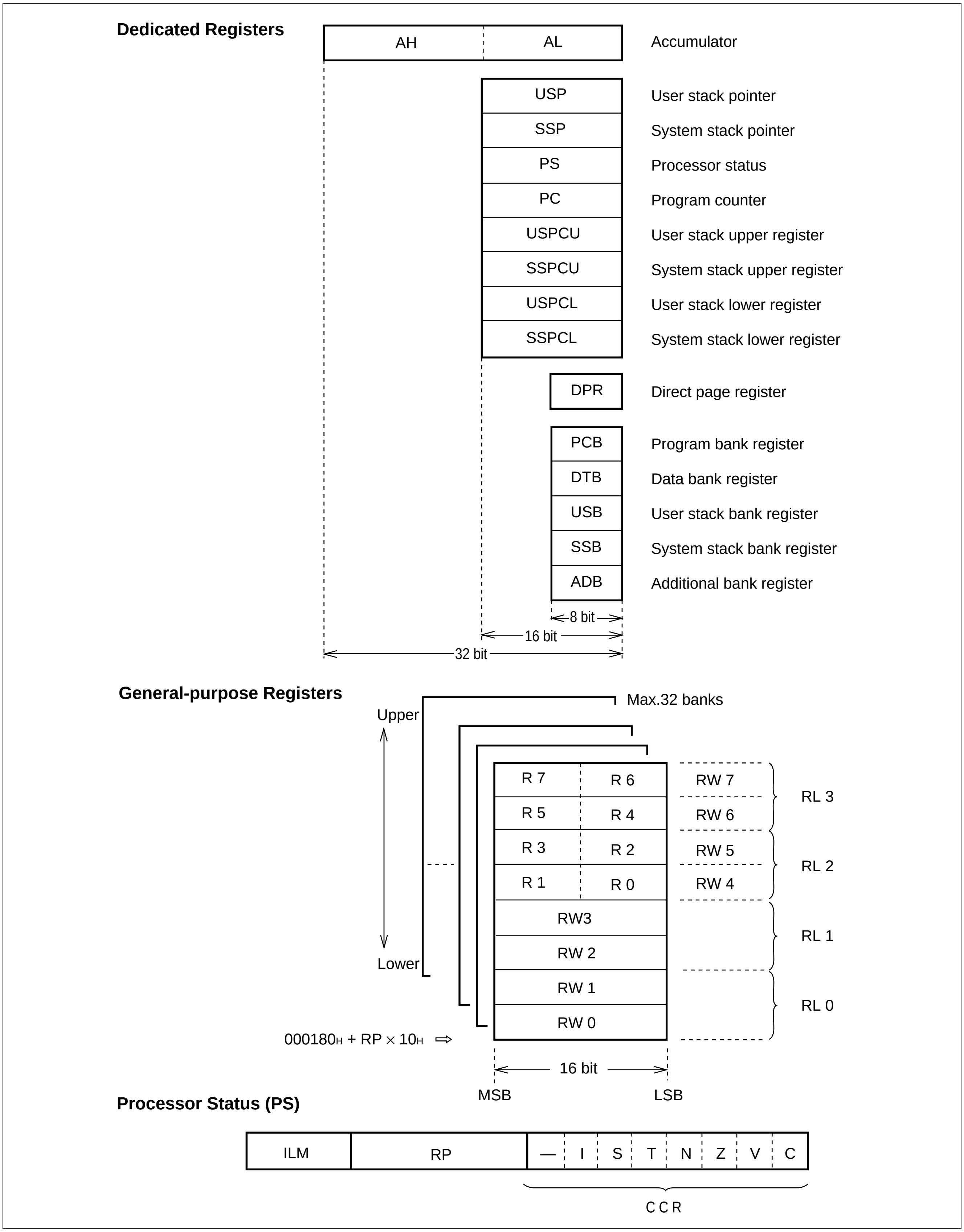
(3) Pins other than MBM27C1000-compatible Pins

Pin no.	Pin name	Treatment
92	X0	Pull up with 4.7 KΩ resistor
93	X1	OPEN
109 110 10 to 16 42 43 46 47 48 to 53 17 to 24 25 to 32 34 to 41 55 to 61 63 to 70 71 to 76 78 79 85 103 to 108	P16 P17 P41 to P47 AV_{CC} AVRH P60 P61 P62 to P67 P70 to P77 P80 to P82 P90 to P97 PA0 to PA7 PB0 to PB7 PC0 to PC5 P50 P51 P57 P10 to P15	Connect pull-up resistor of about 1 MΩ to each pin

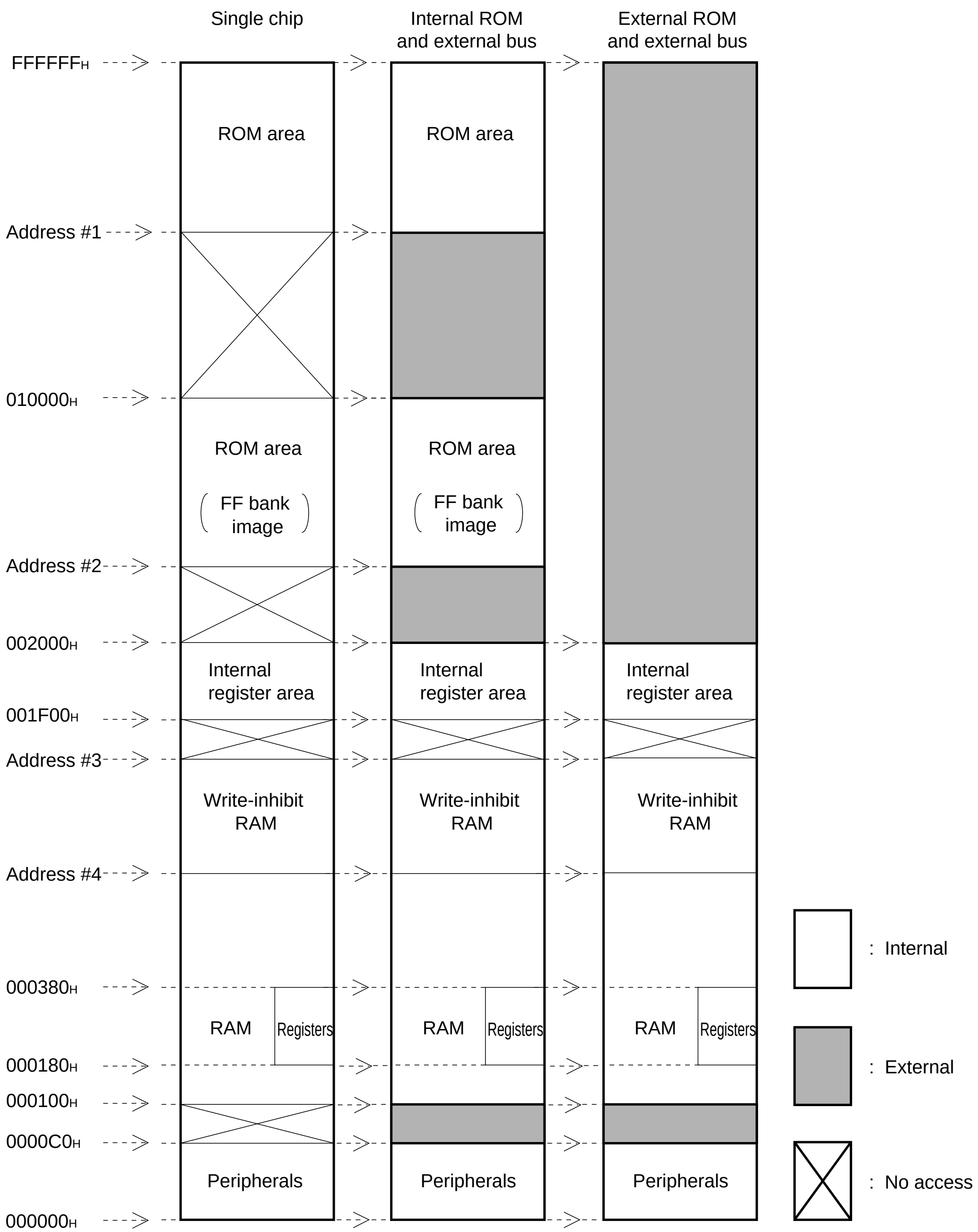
■ BLOCK DIAGRAM



■ PROGRAMMING MODEL



■ MEMORY MAP



Type	Address #1	Address #2	Address #3	Address #4
MB90223	FF0000H	004000H	000F00H	000D00H
MB90224 MB90P224A/P224B MB90W224A/W224B	FE8000H	004000H	001500H	001300H
MB90V220	(FE0000H)	004000H	001900H	001500H

■ I/O MAP

Address	Register	Register name	Access	Resouce name	Initial value
000000H*3	Port 0 data register	PDR0	R/W	Port 0	XXXXXXXX
000001H*3	Port 1 data register	PDR1	R/W	Port 1	XXXXXXXX
000002H*3	Port 2 data register	PDR2	R/W	Port 2	XXXXXXXX
000003H*3	Port 3 data register	PDR3	R/W	Port 3	XXXXXXXX
000004H*3	Port 4 data register	PDR4	R/W	Port 4	XXXXXXXX
000005H*3	Port 5 data register	PDR5	R/W	Port 5	XXXXXXXX
000006H	Port 6 data register	PDR6	R/W	Port 6	11111111
000007H	Port 7 data register	PDR7	R	Port 7	XXXXXXXX
000008H	Port 8 data register	PDR8	R/W	Port 8	XXXXXXXX
000009H	Port 9 data register	PDR9	R/W	Port 9	11111111
00000AH	Port A data register	PDRA	R/W	Port A	XXXXXXXX
00000BH	Port B data register	PDRB	R/W	Port B	XXXXXXXX
00000CH	Port C data register	PDRC	R/W	Port C	– – XXXXXX
00000DH to 0FH	(Reserved area)*1				
000010H*3	Port 0 data direction register	DDR0	R/W	Port 0	00000000
000011H*3	Port 1 data direction register	DDR1	R/W	Port 1	00000000
000012H*3	Port 2 data direction register	DDR2	R/W	Port 2	00000000
000013H*3	Port 3 data direction register	DDR3	R/W	Port 3	00000000
000014H*3	Port 4 data direction register	DDR4	R/W	Port 4	00000000
000015H*3	Port 5 data direction register	DDR5	R/W	Port 5	00000000
000016H	Port 6 analog input enable register	ADER0	R/W	Port 6	11111111
000017H	Port 7 data direction register	DDR7	R/W	Port 7	11111111
000018H	Port 8 data direction register	DDR8	R/W	Port 8	00000000
000019H	Port 9 analog input enable register	ADER1	R/W	Port 9	11111111
00001AH	Port A data direction register	DDRA	R/W	Port A	00000000
00001BH	Port B data direction register	DDRB	R/W	Port B	00000000
00001CH	Port C data direction register	DDRC	R/W	Port C	– – 000000
00001DH to 1FH	(Reserved area)*1				
000020H	Mode control register 0	UMC0	R/W	UART 0 (ch.0)	00000100
000021H	Status register 0	USR0	R/W		00010000
000022H	Input data register 0 /output data register 0	UIDR0 /UODR0	R/W		XXXXXXXX

(Continued)

Address	Register	Register name	Access	Resouce name	Initial value
000023H	Rate and data register 0	URD0	R/W	UART0 (ch.0)	0 0 0 0 0 0 0 X
000024H	Mode control register 1	UMC1	R/W	UART0 (ch.1)	0 0 0 0 0 1 0 0
000025H	Status register 1	USR1	R/W		0 0 0 1 0 0 0 0
000026H	Input data register 1 /output data register 1	UIDR1 /UODR1	R/W		X X X X X X X X
000027H	Rate and data register 1	URD1	R/W		0 0 0 0 0 0 0 X
000028H	Mode control register 2	UMC2	R/W	UART0 (ch.2)	0 0 0 0 0 1 0 0
000029H	Status register 2	USR2	R/W		0 0 0 1 0 0 0 0
00002AH	Input data register 2 /output data register 2	UIDR2 /UODR2	R/W		X X X X X X X X
00002BH	Rate and data register 2	URD2	R/W		0 0 0 0 0 0 0 X
00002CH	UART CTS control register	UCCR	R/W	UART0 (ch.0)	– – – 0 0 0 – –
00002DH	(Reserved area)*1				
00002EH	Mode register	SMR	R/W	UART1	0 0 0 0 0 0 0 0
00002FH	Control register	SCR	R/W		0 0 0 0 0 1 0 0
000030H	Input data register /output data register	SIDR /SODR	R/W		X X X X X X X X
000031H	Status register	SSR	R/W		0 0 0 0 1 – 0 0
000032H	A/D channel setting register	ADCH	R/W	10-bit A/D converter	0 0 0 0 0 0 0 0
000033H	A/D mode register	ADMD	R/W		– – – X 0 0 0 0
000034H	A/D control status register	ADCS	R/W		0 0 0 0 – – 0 0
000035H	(Reserved area)*1				
000036H	A/D data register	ADCD	R	10-bit A/D converter	X X X X X X X X
000037H					0 0 0 0 0 0 X X
000038H	(Reserved area)*1				
000039H					
00003AH	DTP/interrupt enable register	ENIR	R/W	DTP/external interrupt	0 0 0 0 0 0 0 0
00003BH	DTP/interrupt source register	EIRR	R/W		0 0 0 0 0 0 0 0
00003CH	Request level setting register	ELVR	R/W		0 0 0 0 0 0 0 0
00003DH					0 0 0 0 0 0 0 0
00003EH to 3FH	(Reserved area)*1				
000040H	Timer control status register 0	TMCSR0	R/W	16-bit reload timer 0	0 0 0 0 0 0 0 0
000041H					– – – – 0 0 0 0

(Continued)

Address	Register	Register name	Access	Resouce name	Initial value
000042H	Timer control status register 1	TMCSR1	R/W	16-bit reload timer 1	0 0 0 0 0 0 0 0
000043H					– – – – 0 0 0 0
000044H	Timer control status register 2	TMCSR2	R/W	16-bit reload timer 2	0 0 0 0 0 0 0 0
000045H					– – – – 0 0 0 0
000046H	Timer control status register 3	TMCSR3	R/W	16-bit reload timer 3	0 0 0 0 0 0 0 0
000047H					– – – – 0 0 0 0
000048H	Timer control status register 4	TMCSR4	R/W	16-bit reload timer 4	0 0 0 0 0 0 0 0
000049H					– – – – 0 0 0 0
00004AH	Timer control status register 5	TMCSR5	R/W	16-bit reload timer 5	0 0 0 0 0 0 0 0
00004BH					– – – – 0 0 0 0
00004CH	PPG control status register 0	PCNT0	R/W	16-bit PPG timer 0	0 0 0 0 0 0 0 0
00004DH					0 0 0 0 0 0 0 0
00004EH	PPG control status register 1	PCNT1	R/W	16-bit PPG timer 1	0 0 0 0 0 0 0 0
00004FH					0 0 0 0 0 0 0 0
000050H	PWC control status register 0	PWCSR0	R/W	PWC timer 0	0 0 0 0 0 0 0 0
000051H					0 0 0 0 0 0 0 0
000052H	PWC control status register 1	PWCSR1	R/W	PWC timer 1	0 0 0 0 0 0 0 0
000053H					0 0 0 0 0 0 0 0
000054H	PWC control status register 2	PWCSR2	R/W	PWC timer 2	0 0 0 0 0 0 0 0
000055H					0 0 0 0 0 0 0 0
000056H	PWC control status register 3	PWCSR3	R/W	PWC timer 3	0 0 0 0 0 0 0 0
000057H					0 0 0 0 0 0 0 0
000058H	ICU control register 0	ICC0	R/W	ICU (Input Capture Unit)	0 0 0 0 0 0 0 0
000059H	(Reserved area)*1				
00005AH	Input capture control register 1	ICC1	R/W	ICU (Input Capture Unit)	0 0 0 0 0 0 0 0
00005BH	(Reserved area)*1				
00005CH					
00005DH					
00005EH					
00005FH					
000060H	OCU control register 00	CCR00	R/W	OCU (Output Compare Unit)	1 1 1 1 0 0 0 0
000061H					– – – – 0 0 0 0

(Continued)

Address	Register	Register name	Access	Resouce name	Initial value
000062H	OCU0 control register 01	CCR01	R/W	OCU (Output Compare Unit)	1 1 1 1 0 0 0 0
000063H					– – – – 0 0 0 0
000064H	(Reserved area)*1				
000065H					
000066H					
000067H					
000068H	OCU0 control register 10	CCR10	R/W	OCU (Output Compare Unit)	– – – – 0 0 0 0
000069H					0 0 0 0 0 0 0 0
00006AH	OCU0 control register 11	CCR11	R/W		– – – – 0 0 0 0
00006BH					0 0 0 0 0 0 0 0
00006CH	(Reserved area)*1				
00006DH					
00006EH					
00006FH					
000070H	Free-run timer control register	TCCR	R/W	24-bit timer counter	1 1 0 0 0 0 0 0
000071H					– – 1 1 1 1 1 1
000072H	Free-run timer lower-order data register	TCRL	R		0 0 0 0 0 0 0 0
000073H					0 0 0 0 0 0 0 0
000074H	Free-run timer upper-order data register	TCRH			0 0 0 0 0 0 0 0
000075H					0 0 0 0 0 0 0 0
000076H	(Reserved area)*1				
000077H					
000078H					
000079H					
00007AH	PWC divider ratio control register 0	DIVR0	R/W	PWC timer 0	– – – – – – 0 0
00007BH	Reserved area*1				
00007CH	PWC divider ratio control register 1	DIVR1	R/W	PWC timer 1	– – – – – – 0 0
00007DH	Reserved area*1				
00007EH	PWC divider ratio control register 2	DIVR2	R/W	PWC timer 2	– – – – – – 0 0
00007FH	Reserved area*1				
000080H	PWC divider ratio control register 3	DIVR3	R/W	PWC timer 3	– – – – – – 0 0
000081H to 8DH	(Reserved area)*1				

(Continued)

Address	Register	Register name	Access	Resouce name	Initial value
00008E$_H$	WI control register	WICR	R/W	Write-inhibit RAM	– – – X – – – –
00008F$_H$	(Reserved area)[*1]				
000090$_H$ to 9E$_H$					
00009F$_H$	Delay interrupt source generation /release register	DIRR	R/W	Delay interrupt generation module	– – – – – – – 0
0000A0$_H$	Standby control register	STBYC	R/W	Low power consumption	0 0 0 1 * * * *
0000A3$_H$	Address mid-order control register	MACR	W	External pin	# # # # # # # #
0000A4$_H$	Address higher-order control register	HACR	W	External pin	# # # # # # # #
0000A5$_H$	External pin control register	EPCR	W	External pin	# # 0 – 0 # 0 0
0000A8$_H$	Watchdog timer control register	WDTC	R/W	Watchdog timer	X X X X X X X X
0000A9$_H$	Timebase timer control register	TBTC	R/W	Timebase timer	– – – 0 0 0 0 0
0000B0$_H$	Interrupt control register 00	ICR00	R/W	Interrupt controller	0 0 0 0 0 1 1 1
0000B1$_H$	Interrupt control register 01	ICR01	R/W		0 0 0 0 0 1 1 1
0000B2$_H$	Interrupt control register 02	ICR02	R/W		0 0 0 0 0 1 1 1
0000B3$_H$	Interrupt control register 03	ICR03	R/W		0 0 0 0 0 1 1 1
0000B4$_H$	Interrupt control register 04	ICR04	R/W		0 0 0 0 0 1 1 1
0000B5$_H$	Interrupt control register 05	ICR05	R/W		0 0 0 0 0 1 1 1
0000B6$_H$	Interrupt control register 06	ICR06	R/W		0 0 0 0 0 1 1 1
0000B7$_H$	Interrupt control register 07	ICR07	R/W		0 0 0 0 0 1 1 1
0000B8$_H$	Interrupt control register 08	ICR08	R/W		0 0 0 0 0 1 1 1
0000B9$_H$	Interrupt control register 09	ICR09	R/W		0 0 0 0 0 1 1 1
0000BA$_H$	Interrupt control register 10	ICR10	R/W		0 0 0 0 0 1 1 1
0000BB$_H$	Interrupt control register 11	ICR11	R/W		0 0 0 0 0 1 1 1
0000BC$_H$	Interrupt control register 12	ICR12	R/W		0 0 0 0 0 1 1 1
0000BD$_H$	Interrupt control register 13	ICR13	R/W		0 0 0 0 0 1 1 1
0000BE$_H$	Interrupt control register 14	ICR14	R/W		0 0 0 0 0 1 1 1
0000BF$_H$	Interrupt control register 15	ICR15	R/W		0 0 0 0 0 1 1 1
0000C0$_H$ to FF$_H$	(External area)[*2]				
001F00$_H$	PWC data buffer register 0	PWCR0	R/W	PWC timer 0	0 0 0 0 0 0 0 0
001F01$_H$					0 0 0 0 0 0 0 0

(Continued)

Address	Register	Register name	Access	Resouce name	Initial value
001F02H	PWC data buffer register 1	PWCR1	R/W	PWC timer 1	0 0 0 0 0 0 0 0
001F03H	PWC data buffer register 1	PWCR1	R/W	PWC timer 1	0 0 0 0 0 0 0 0
001F04H	PWC data buffer register 2	PWCR2	R/W	PWC timer 2	0 0 0 0 0 0 0 0
001F05H	PWC data buffer register 2	PWCR2	R/W	PWC timer 2	0 0 0 0 0 0 0 0
001F06H	PWC data buffer register 3	PWCR3	R/W	PWC timer 3	0 0 0 0 0 0 0 0
001F07H	PWC data buffer register 3	PWCR3	R/W	PWC timer 3	0 0 0 0 0 0 0 0
001F08H to 1F0FH	(Reserved area)*1				
001F10H	OCU compare lower-order data register 00	CPR00L	R/W	Output compare 00	0 0 0 0 0 0 0 0
001F11H	OCU compare lower-order data register 00	CPR00L	R/W	Output compare 00	0 0 0 0 0 0 0 0
001F12H	OCU compare higher-order data register 00	CPR00	R/W	Output compare 00	0 0 0 0 0 0 0 0
001F13H	OCU compare higher-order data register 00	CPR00	R/W	Output compare 00	0 0 0 0 0 0 0 0
001F14H	OCU compare lower-order data register 01	CPR01L	R/W	Output compare 01	0 0 0 0 0 0 0 0
001F15H	OCU compare lower-order data register 01	CPR01L	R/W	Output compare 01	0 0 0 0 0 0 0 0
001F16H	OCU compare higher-order data register 01	CPR01	R/W	Output compare 01	0 0 0 0 0 0 0 0
001F17H	OCU compare higher-order data register 01	CPR01	R/W	Output compare 01	0 0 0 0 0 0 0 0
001F18H	OCU compare lower-order data register 02	CPR02L	R/W	Output compare 02	0 0 0 0 0 0 0 0
001F19H	OCU compare lower-order data register 02	CPR02L	R/W	Output compare 02	0 0 0 0 0 0 0 0
001F1AH	OCU compare higher-order data register 02	CPR02	R/W	Output compare 02	0 0 0 0 0 0 0 0
001F1BH	OCU compare higher-order data register 02	CPR02	R/W	Output compare 02	0 0 0 0 0 0 0 0
001F1CH	OCU compare lower-order data register 03	CPR03L	R/W	Output compare 03	0 0 0 0 0 0 0 0
001F1DH	OCU compare lower-order data register 03	CPR03L	R/W	Output compare 03	0 0 0 0 0 0 0 0
001F1EH	OCU compare higher-order data register 03	CPR03	R/W	Output compare 03	0 0 0 0 0 0 0 0
001F1FH	OCU compare higher-order data register 03	CPR03	R/W	Output compare 03	0 0 0 0 0 0 0 0
001F20H	OCU compare lower-order data register 04	CPR04L	R/W	Output compare 10	0 0 0 0 0 0 0 0
001F21H	OCU compare lower-order data register 04	CPR04L	R/W	Output compare 10	0 0 0 0 0 0 0 0
001F22H	OCU compare higher-order data register 04	CPR04	R/W	Output compare 10	0 0 0 0 0 0 0 0
001F23H	OCU compare higher-order data register 04	CPR04	R/W	Output compare 10	0 0 0 0 0 0 0 0
001F24H	OCU compare lower-order data register 05	CPR05L	R/W	Output compare 11	0 0 0 0 0 0 0 0
001F25H	OCU compare lower-order data register 05	CPR05L	R/W	Output compare 11	0 0 0 0 0 0 0 0
001F26H	OCU compare higher-order data register 05	CPR05	R/W	Output compare 11	0 0 0 0 0 0 0 0
001F27H	OCU compare higher-order data register 05	CPR05	R/W	Output compare 11	0 0 0 0 0 0 0 0

(Continued)

Address	Register	Register name	Access	Resouce name	Initial value
001F28H	OCU compare lower-order data register 06	CPR06L	R/W	Output compare 12	0 0 0 0 0 0 0 0
001F29H					0 0 0 0 0 0 0 0
001F2AH	OCU compare higher-order data register 06	CPR06			0 0 0 0 0 0 0 0
001F2BH					0 0 0 0 0 0 0 0
001F2CH	OCU compare lower-order data register 07	CPR07L	R/W	Output compare 13	0 0 0 0 0 0 0 0
001F2DH					0 0 0 0 0 0 0 0
001F2EH	OCU compare higher-order data register 07	CPR07			0 0 0 0 0 0 0 0
001F2FH					0 0 0 0 0 0 0 0
001F30H	16-bit timer register 0	TMR0	R	16-bit reload timer 0	X X X X X X X X
001F31H					X X X X X X X X
001F32H	16-bit reload register 0	TMRLR0	W		X X X X X X X X
001F33H					X X X X X X X X
001F34H	16-bit timer register 1	TMR1	R	16-bit reload timer 1	X X X X X X X X
001F35H					X X X X X X X X
001F36H	16-bit timer reload register 1	TMRLR1	W		X X X X X X X X
001F37H					X X X X X X X X
001F38H	16-bit timer register 2	TMR2	R	16-bit reload timer 2	X X X X X X X X
001F39H					X X X X X X X X
001F3AH	16-bit timer reload register 2	TMRLR2	W		X X X X X X X X
001F3BH					X X X X X X X X
001F3CH	16-bit timer register 3	TMR3	R	16-bit reload timer 3	X X X X X X X X
001F3DH					X X X X X X X X
001F3EH	16-bit timer reload register 3	TMRLR3	W		X X X X X X X X
001F3FH					X X X X X X X X
001F40H	16-bit timer register 4	TMR4	R	16-bit reload timer 4	X X X X X X X X
001F41H					X X X X X X X X
001F42H	16-bit timer reload register 4	TMRLR4	W		X X X X X X X X
001F43H					X X X X X X X X
001F44H	16-bit timer register 5	TMR5	R	16-bit reload timer 0	X X X X X X X X
001F45H					X X X X X X X X
001F46H	16-bit timer reload register 5	TMRLR5	W		X X X X X X X X
001F47H					X X X X X X X X

(Continued)

(Continued)

Address	Register	Register name	Access	Resouce name	Initial value
001F48H	PPG cycle setting register 0	PCSR0	W	16-bit PPG timer 0	XXXXXXXX
001F49H					XXXXXXXX
001F4AH	PPG duty setting register 0	PDUT0	W		XXXXXXXX
001F4BH					XXXXXXXX
001F4CH	PPG cycle setting register 1	PCSR1	W	16-bit PPG timer 1	XXXXXXXX
001F4DH					XXXXXXXX
001F4EH	PPG duty setting register 1	PDUT1	W		XXXXXXXX
001F4FH					XXXXXXXX
001F50H	ICU lower-order data register 0	ICRL0	R	Input capture 0	XXXXXXXX
001F51H					XXXXXXXX
001F52H	ICU higher-order data register 0	ICRH0	R		XXXXXXXX
001F53H					00000000
001F54H	ICU lower-order data register 1	ICRL1	R	Input capture 1	XXXXXXXX
001F55H					XXXXXXXX
001F56H	ICU higher-order data register 1	ICRH1	R		XXXXXXXX
001F57H					00000000
001F58H	ICU lower-order data register 2	ICRL2	R	Input capture 2	XXXXXXXX
001F59H					XXXXXXXX
001F5AH	ICU higher-order data register 2	ICRH2	R		XXXXXXXX
001F5BH					00000000
001F5CH	ICU lower-order data register 3	ICRL3	R	Input capture 3	XXXXXXXX
001F5DH					XXXXXXXX
001F5EH	ICU higher-order data register 3	ICRH3	R		XXXXXXXX
001F5FH					00000000
001F60H to 1FFFH	(Reserved area)*1				

Initial value
0: The initial value of this bit is “0”.
1: The initial value of this bit is “1”.
X: The initial value of this bit is undefined.
–: This bit is not used. The initial value is undefined.
*: The initial value of this bit varies with the reset source.
#: The initial value of this bit varies with the operation mode.
*1: Access prohibited
*2: Only this area is open to external access in the area below address 0000FFH (inclusive). All addresses which are not described in the table are reserved areas, and accesses to these areas are handled in the same manner as for internal areas. The access signal for the external bus is not generated.
*3: When an external bus is enable mode, never access to resisters which are not used as general ports in areas address 000000H to 000005H or 000010H to 000015H.

■ INTERRUPT SOURCES AND INTERRUPT VECTORS/INTERRUPT CONTROL REGISTERS

Interrupt source	EI^{2}OS support	Interrupt vector			Interrupt control register	
		No.		Address	ICR	Address
Reset	×	#08	08$_H$	FFFFDC$_H$	—	—
INT9 instruction	×	#09	09$_H$	FFFFD8$_H$	—	—
Exception	×	#10	0A$_H$	FFFFD4$_H$	—	—
External interrupt #0	△	#11	0B$_H$	FFFFD0$_H$	ICR00	0000B0$_H$
External interrupt #1	△	#12	0C$_H$	FFFFCC$_H$		
External interrupt #2	△	#13	0D$_H$	FFFFC8$_H$	ICR01	0000B1$_H$
Input capture 0	△	#14	0E$_H$	FFFFC4$_H$		
PWC0 count completed/overflow	△	#15	0F$_H$	FFFFC0$_H$	ICR02	0000B2$_H$
PWC1 count completed/overflow/input capture 1	△	#16	10$_H$	FFFFBC$_H$		
PWC2 count completed/overflow/input capture 2	△	#17	11$_H$	FFFFB8$_H$	ICR03	0000B3$_H$
PWC3 count completed/overflow/input capture 3	△	#18	12$_H$	FFFFB4$_H$		
24-bit timer, overflow	△	#19	13$_H$	FFFFB0$_H$	ICR04	0000B4$_H$
24-bit timer, intermediate bit/timebase timer, interval interrupt	△	#20	14$_H$	FFFFAC$_H$		
Compare 0	△	#21	15$_H$	FFFFA8$_H$	ICR05	0000B5$_H$
Compare 1	△	#22	16$_H$	FFFFA4$_H$		
Compare 2	△	#23	17$_H$	FFFFA0$_H$	ICR06	0000B6$_H$
Compare 3	△	#24	18$_H$	FFFF9C$_H$		
Compare 4/6	△	#25	19$_H$	FFFF98$_H$	ICR07	0000B7$_H$
Compare 5/7	△	#26	1A$_H$	FFFF94$_H$		
16-bit timer 0/1/2, overflow/PPG0	△	#27	1B$_H$	FFFF90$_H$	ICR08	0000B8$_H$
16-bit timer 3/4/5, overflow/PPG1	△	#28	1C$_H$	FFFF8C$_H$		
10-bit A/D converter count completed	□	#29	1D$_H$	FFFF88$_H$	ICR09	0000B9$_H$
UART1 transmission completed	△	#31	1F$_H$	FFFF80$_H$	ICR10	0000BA$_H$
UART1 reception completed	△	#32	20$_H$	FFFF7C$_H$		
UART0 (ch.1) transmission completed	△	#33	21$_H$	FFFF78$_H$	ICR11	0000BB$_H$
UART0 (ch.2) transmission completed	△	#34	22$_H$	FFFF74$_H$		
UART0 (ch.1) reception completed	○	#35	23$_H$	FFFF70$_H$	ICR12	0000BC$_H$
UART0 (ch.2) reception completed	△	#36	24$_H$	FFFF6C$_H$		
UART0 (ch.0) transmission completed	◎	#37	25$_H$	FFFF68$_H$	ICR13	0000BD$_H$

(Continued)

(Continued)

Interrupt source	EI²OS support	Interrupt vector			Interrupt control register	
		No.		Address	ICR	Address
UART0 (ch.0) reception completed	◎	#39	27_H	$FFFF60_H$	ICR14	$0000BE_H$
Delay interrupt generation module	×	#42	$2A_H$	$FFFF54_H$	ICR15	$0000BF_H$
Stack fault	×	#255	FF_H	$FFFC00_H$	—	—

◎ : EI²OS is supported (with stop request).
□ : EI²OS is supported (without stop request).
○ : EI²OS is supported; however, since two interrupt sources are allocated to a single ICR, in case EI²OS is used for one of the two, EI²OS and ordinary interrupt are not both available for the other (with stop request).
△ : EI²OS is supported; however, since two interrupt sources are allocated to a single ICR, in case EI²OS is used for one of the two, EI²OS and ordinary interrupt are not both available for the other (without stop request).
× : EI²OS is not supported.

Note: Since the interrupt sources having interrupt vector Nos. 15 to 18, 20, and 25 to 28 are OR'ed, respectively, select them by means of the interrupt enable bits of each resource.

If EI²OS is used with the above-mentioned interrupt sources OR'ed with the interrupt vector Nos. 15 to 18, 20, and 25 to 28, be sure to activate one of the interrupt sources.

Also in this case, a request flag in the same series as the one interrupt source is likely to be cleared automatically by EI²OS.

Assume for example that an interrupt for compare 4 of the interrupt vector No. 25 is activated at this time by ICR07, so that the compare 6 is disabled. If EI²OS is activated at this time by ICR07, so that the compare 6 interrupt takes place during generation of or simultaneously with the compare 4 interrupt, not only the interrupt flag for the compare 4 but also that for the compare 6 will be automatically cleared after EI²OS is automatically transferred due to the compare 4 interrupt.

■ PERIPHERAL RESOURCES

1. Parallel Ports

The MB90220 series has 86 I/O pins and 16 open-drain I/O pins.

(1) Register Configuration

• **Port 0 to C Data Register (PDR0 to PDRC)**

Register name	Address
PDR1	000001 H
PDR3	000003 H
PDR5	000005 H
PDR7	000007 H
PDR9	000009 H
PDRB	00000B H

bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	Initial value
PD x 7	PD x 6	PD x 5	PD x 4	PD x 3	PD x 2	PD x 1	PD x 0	XXXXXXXX B
(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(PDR9 only: 11111111)
PDR7 only: (R)	(R)	(R)	(R)	(R)	(R)	(R)	(R)	

Register name	Address
PDR0	000000 H
PDR2	000002 H
PDR4	000004 H
PDR6	000006 H
PDR8	000008 H
PDRA	00000A H
PDRC	00000C H

bit7	bit6	bit5	bit 4	bit3	bit2	bit1	bit0	Initial value
PD x 7	PD x 6	PD x 5	PD x 4	PD x 3	PD x 2	PD x 1	PD x 0	XXXXXXXX B
(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(PDR6 only: 11111111)

Note: There are no register bits for bits 7 and 6 of port C.

• **Port 0 to C Data Register (PDR0 to PDRC)**

Register name	Address
DDR1	000011 H
DDR3	000013 H
DDR5	000015 H
DDR7	000017 H
DDRB	00001B H

bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	Initial value
DD x 7	DD x 6	DD x 5	DD x 4	DD x 3	DD x 2	DD x 1	DD x 0	00000000 B
(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(PDR7 only: 11111111)

Register name	Address
DDR0	000010 H
DDR2	000012 H
DDR4	000014 H
DDR8	000018 H
DDRA	00001A H
DDRC	00001C H

bit7	bit6	bit5	bit 4	bit3	bit2	bit1	bit0	Initial value
DD x 7	DD x 6	DD x 5	DD x 4	DD x 3	DD x 2	DD x 1	DD x 0	00000000 B
(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

Note: There are no register bits for bits 7 and 6 of port C.

• **Port 6, 9 Analog Input Enable Register (ADER0, ADER1)**

Register name	Address
ADER0	000016 H

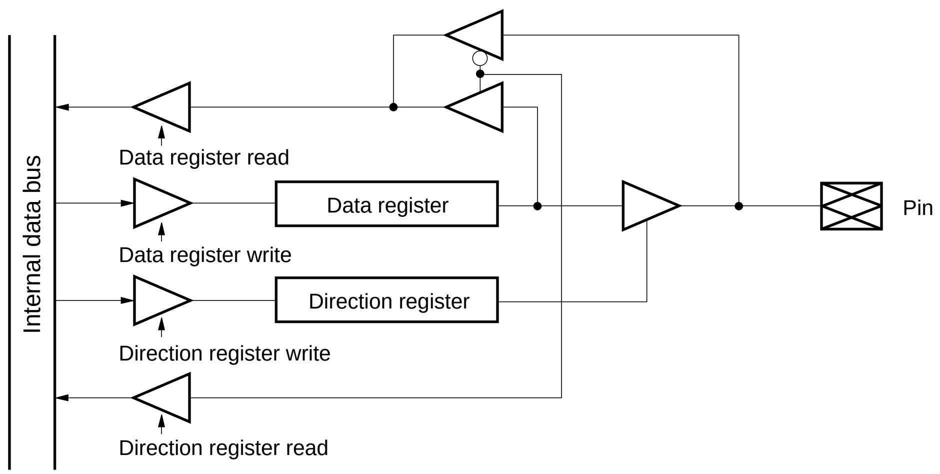
bit7	bit6	bit5	bit 4	bit3	bit2	bit1	bit0	Initial value
AE07	AE06	AE05	AE04	AE03	AE02	AE01	AE00	11111111 B
(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

Register name	Address
ADER1	000019 H

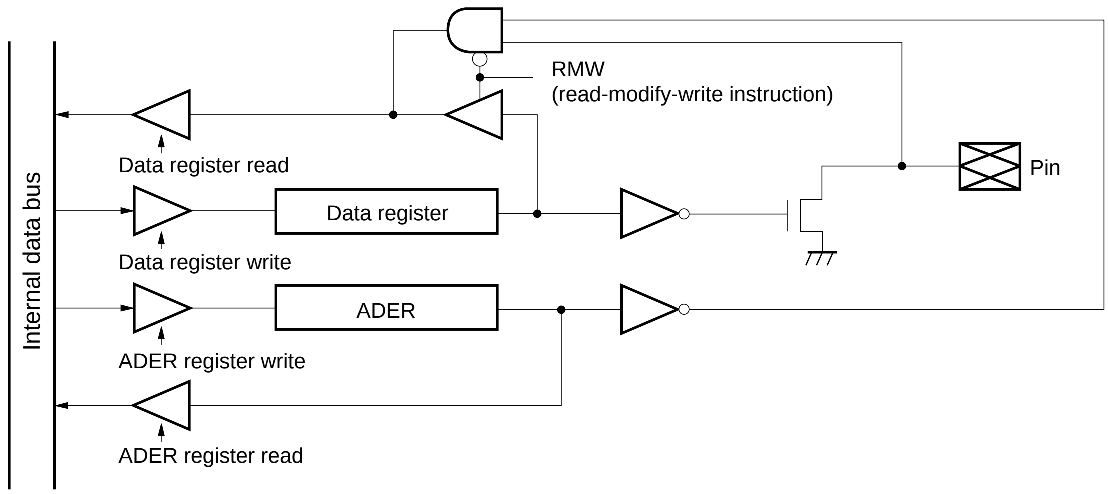
bit7	bit6	bit5	bit 4	bit3	bit2	bit1	bit0	Initial value
AE15	AE14	AE13	AE12	AE11	AE10	AE09	AE08	11111111 B
(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

(2) Block Diagram

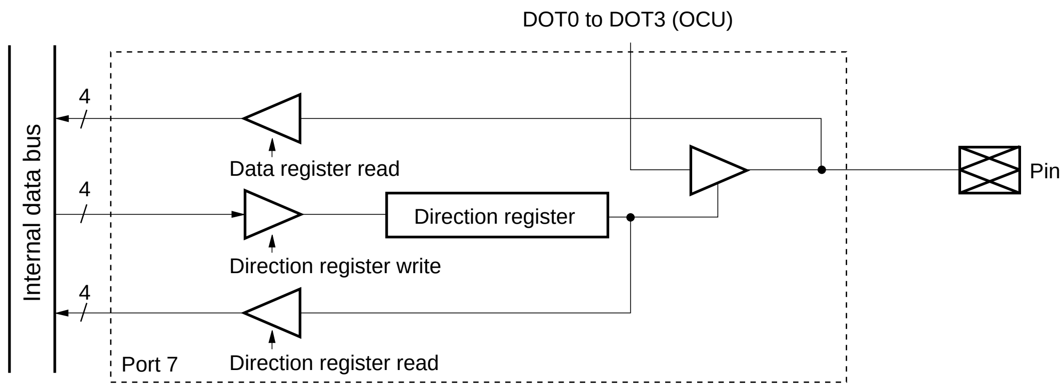
- **I/O Port (Port 0 to 5, 8, and A to C)**



- **I/O Ports with an Open-drain output (Port 6, and 9)**



- **I/O Port (Port 7)**



Note: Port 7 is input port. This pin also usable as I/O port for OCU internal function.

2. 16-bit Reload Timer (with Event Count Function)

The 16-bit reload timer 1 consists of a 16-bit down counter, a 16-bit reload register, an input pin (TIN), an output pin (TOT), and a control register. The input clock can be selected from among three internal clocks and one external clock. At the output pin (TOT), the pulses in the toggled output waveform are output in the reload mode; the rectangular pulses indicating that the timer is counting are in the single-shot mode. The input pin (TIN) can be used for event input in the event count mode, and for trigger input or gate input in the internal clock mode.

The MB90220 series has six channels for this timer.

(1) Register Configuration

- **Timer Control Status Register 0 to 5 (TMCSR0 to TMCSR5)**

Register name	Address
TMCSR0	000041 H
TMCSR1	000043 H
TMCSR2	000045 H
TMCSR3	000047 H
TMCSR4	000049 H
TMCSR5	00004B H

bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	Initial value
—	—	—	—	CSL1	CSL0	MOD2	MOD1	- - - - 0000 B
(—)	(—)	(—)	(—)	(R/W)	(R/W)	(R/W)	(R/W)	

Register name	Address
TMCSR0	000040 H
TMCSR1	000042 H
TMCSR2	000044 H
TMCSR3	000046 H
TMCSR4	000048 H
TMCSR5	00004A H

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
MOD0	OUTE	OUTL	RELD	INTE	UF	CNTE	TRG	00000000 B
(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

- **16-bit Timer Register 0 to 5 (TMR0 to TMR5)**

Register name	Address
TMR0	001F31 H
TMR1	001F35 H
TMR2	001F39 H
TMR3	001F3D H
TMR4	001F41 H
TMR5	001F45 H

bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	Initial value
								XXXXXXXX B
(R)	(R)	(R)	(R)	(R)	(R)	(R)	(R)	

Register name	Address
TMR0	001F30 H
TMR1	001F34 H
TMR2	001F38 H
TMR3	001F3C H
TMR4	001F40 H
TMR5	001F44 H

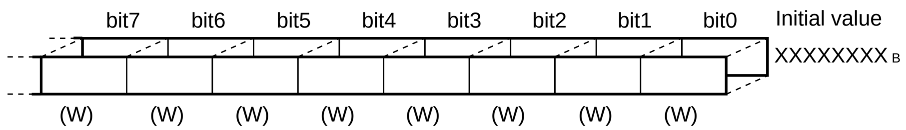
bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
								XXXXXXXX B
(R)	(R)	(R)	(R)	(R)	(R)	(R)	(R)	

- **16-bit Timer Reload Register 0 to 5 (TMRLR0 to TMRLR5)**

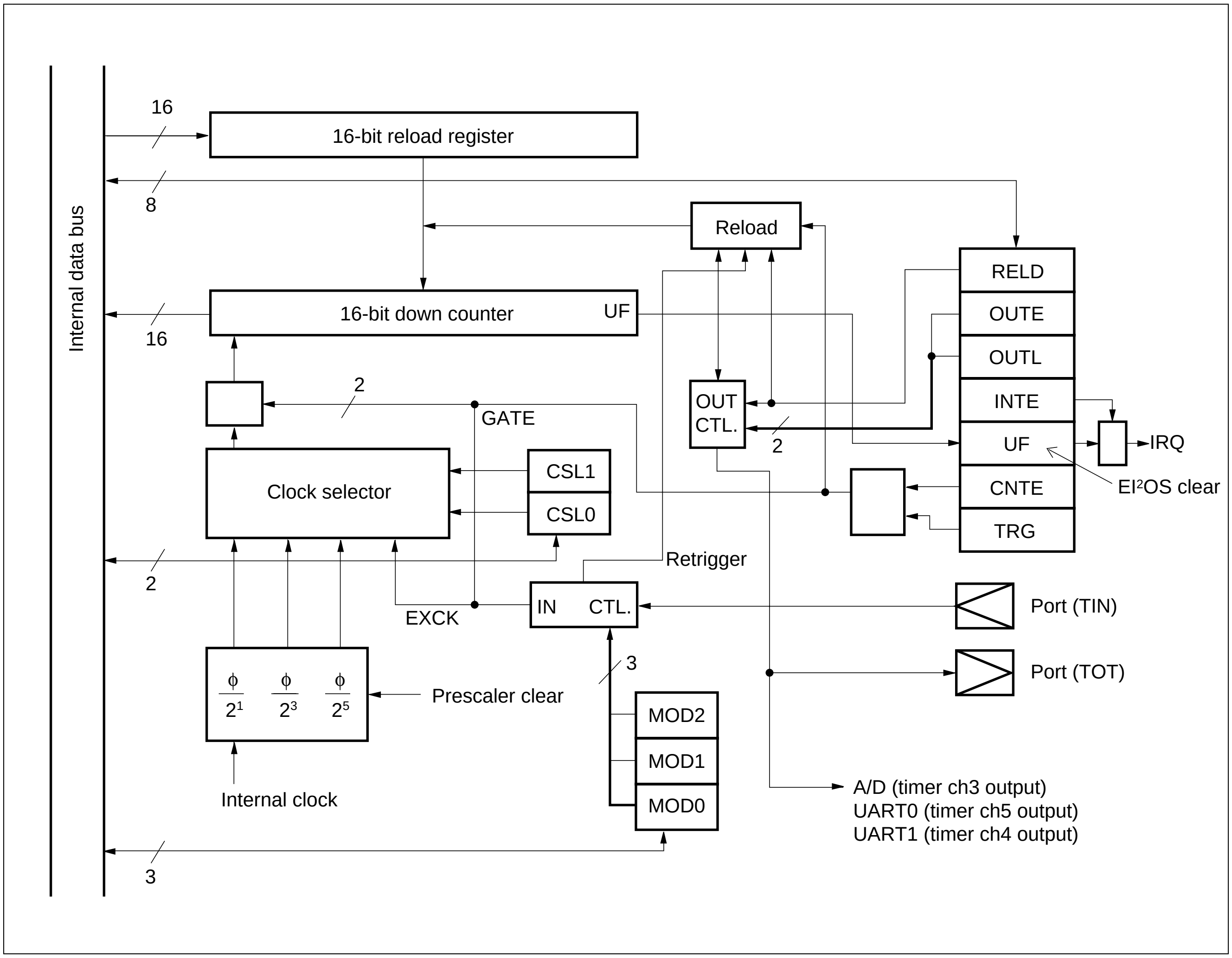
Register name	Address
TMRLR0	001F33 H
TMRLR1	001F37 H
TMRLR2	001F3B H
TMRLR3	001F3F H
TMRLR4	001F43 H
TMRLR5	001F47 H

bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	Initial value
								XXXXXXXX B
(W)	(W)	(W)	(W)	(W)	(W)	(W)	(W)	

Register name	Address
TMRLR0	001F32 H
TMRLR1	001F36 H
TMRLR2	001F3A H
TMRLR3	001F3E H
TMRLR4	001F42 H
TMRLR5	001F46 H



(2) Block Diagram



3. UART0

UART0 is a serial I/O port for synchronous or asynchronous communication with external resources. It has the following features:

- Full duplex double buffer
- CLK synchronous and CLK asynchronous data transfers capable
- Multiprocessor mode support (Mode 2)
- Built-in dedicated baud-rate generator (12 rates)
- Arbitrary baud-rate setting from external clock input or internal timer
- Variable data length (7 to 9 bits (without parity bit); 6 to 8 bits (with parity bit))
- Error detection function (Framing, overrun, parity)
- Interrupt function (Two sources for transmission and reception)
- Transfer in NRZ format

The MB90220 has three of these modules on chip.

(1) Register Configuration

- **Mode Control Register 0 to 2 (UMC0 to UMC2)**

Serial mode control register

Register name	Address
UMC0	000020 H
UMC1	000024 H
UMC2	000028 H

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
PEN	SBL	MC1	MC0	SMDE	RFC	SCKE	SOE
(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)

Initial value 00000100 B

- **Status Register 0 to 2 (USR0 to USR2)**

Register name	Address
USR0	000021 H
USR1	000025 H
USR2	000029 H

bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8
RDRF	ORFE	PE	TDRE	RIE	TIE	RBF	TBF
(R)	(R)	(R)	(R)	(R/W)	(R/W)	(R)	(R)

Initial value 00001000 B

- **Input Data Register 0 to 2 (UIDR0 to UIDR2)/Ouput Data Register 0 to 2 (UODR0 to UODR2)**

Register name	Address
UIDR0/UODR0	000022 H
UIDR1/UODR1	000026 H
UIDR2/UODR2	00002A H

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
D7	D6	D5	D4	D3	D2	D1	D0
(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)

Initial value XXXXXXXX B

- **Rate and Data Register 0 to 2 (URD0 to URD2)**

Register name	Address
URD0	000023 H
URD1	000027 H
URD2	00002B H

bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8
BCH	RC3	RC2	RC1	RC0	BCH0	P	D8
(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)

Initial value 0000000X B

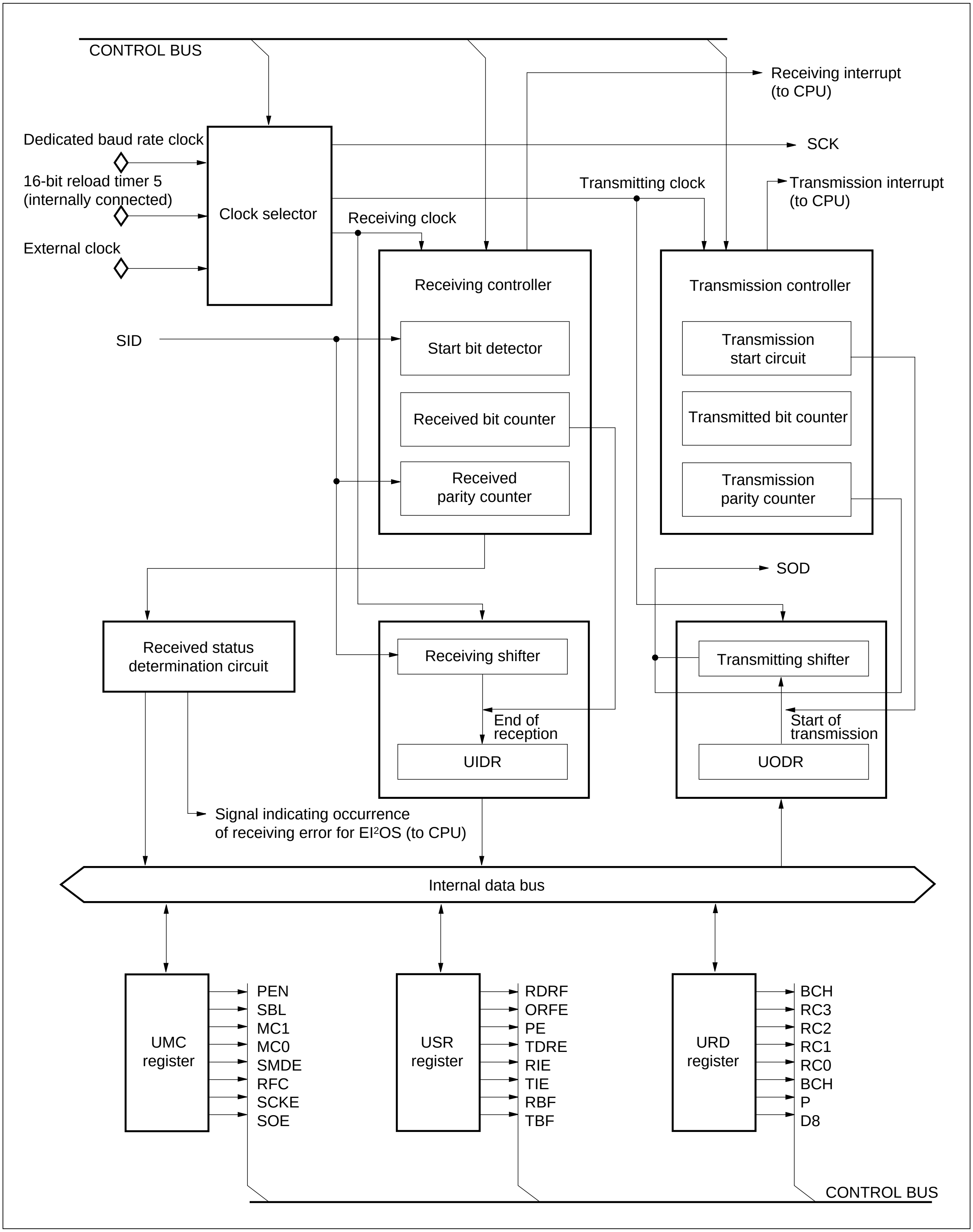
- **UART CTS Control Register (UCCR)**

Register name	Address
UCCR	00002C H

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
—	—	—	CTE	CSP	CTSE	—	—
(—)	(—)	(—)	(R/W)	(R/W)	(R/W)	(—)	(—)

Initial value - - - 000 - - B

(2) Block Diagram



4. UART1

The UART1 is a serial I/O port for asynchronous communications (start-stop synchronization) or CLK synchronized communications. It has the following features:

- Full-duplex double buffering
- Permits asynchronous (start-stop synchronization) and CLK synchronous communications
- Multiprocessor mode support
- Built-in dedicated baud rate generator
  Asynchronous: 9615, 31250, 4808, 2404, and 1202 bps
  CLK synchronization: 1 M, 500 K, 250 K bps
- Arbitray baud-rate setting from external clock input or internal timer
- Error detection function (parity errors, framing errors, and overrun errors)
- Transfer in format NRZ
- Extended supports intelligent I/O service

(1) Register Configuration

- **Mode Register (SMR)**

Register name	Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
SMR	00002E H	MD1	MD0	CS2	CS1	CS0	BCH	SCKE	SOE	00000000B
		(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

- **SCR (Control Register)**

Register name	Address	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	Initial value
SCR	00002F H	PEN	P	SBL	CL	A/D	REC	RXE	TXE	00000100B
		(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R)	(R/W)	(R/W)	

- **Input Data Register (SIDR)/Serial Output Data Register (SODR)**

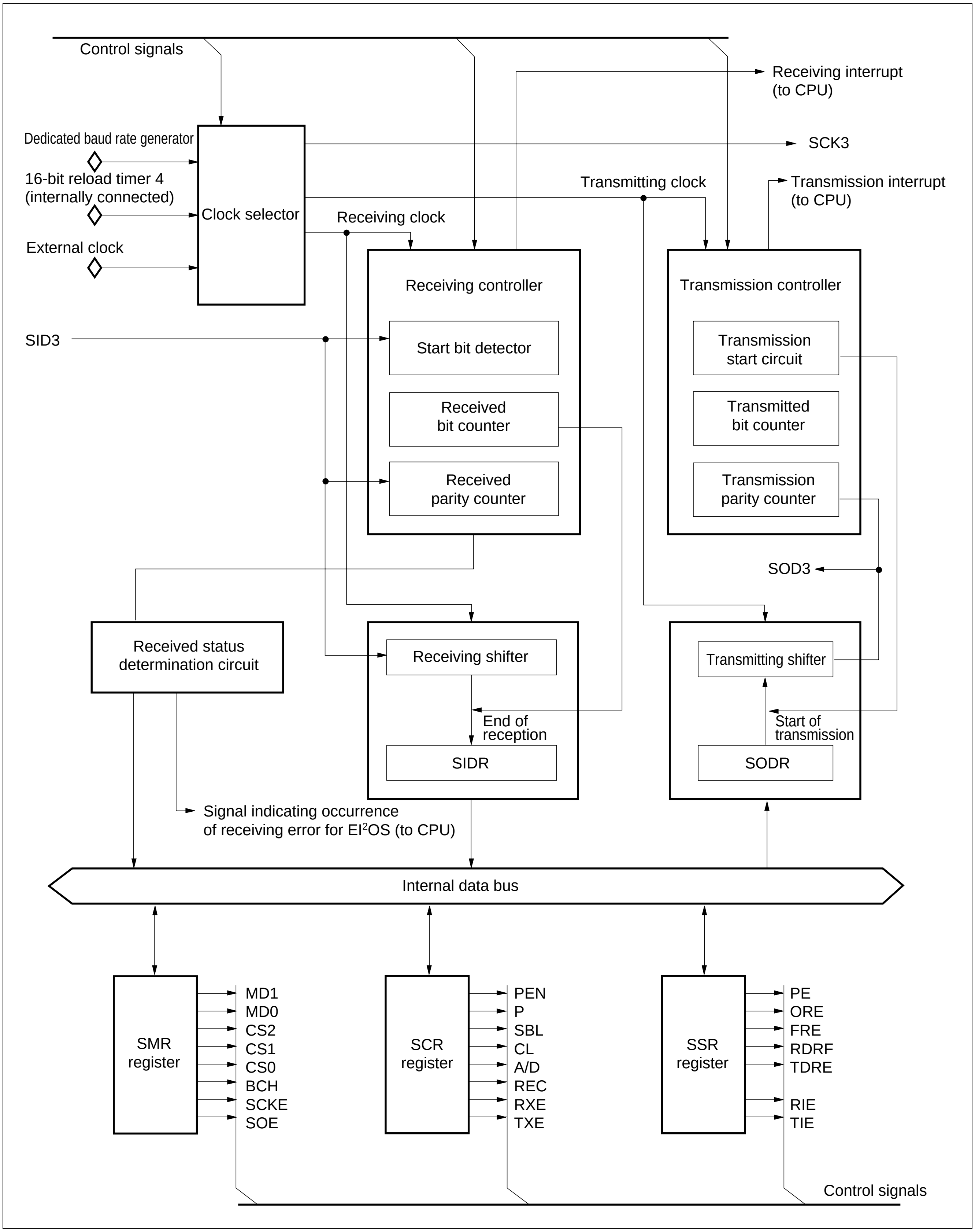
Register name	Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
SIDR	000030 H	D7	D6	D5	D4	D3	D2	D1	D0	XXXXXXXXB
		(R)	(R)	(R)	(R)	(R)	(R)	(R)	(R)	

Register name	Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
SODR	000030 H	D7	D6	D5	D4	D3	D2	D1	D0	XXXXXXXXB
		(W)	(W)	(W)	(W)	(W)	(W)	(W)	(W)	

- **SSR (Status Register)**

Register name	Address	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	Initial value
SSR	000031 H	PE	ORE	FRE	RDRF	TDRE	—	RIE	TIE	00001-00B
		(R)	(R)	(R)	(R)	(R)		(R/W)	(R/W)	

(2) **Block Diagram**



5. 10-bit A/D Converter

The 10-bit A/D converter converts analog input voltage into a digital value. The features of this module are described below:

- Conversion time: 6.125 µs/channel (min.) (with machine clock running at 16 MHz)
- Uses RC-type sequential comparison and conversion method with built-in sample and hold circuit
- 10-bit resolution
- Analog input can be selected by software from among 16 channels
  Single-conversion mode: Selects and converts one channel.
  Scan conversion mode: Converts several consecutive channels (up to 16 can be programmed).
  One-shot mode: Converts the specified channel once and terminates.
  Continuous conversion mode: Repeatedly converts the specified channel.
  Stop conversion mode: Pauses after converting one channel and waits until the next startup (permits synchronization of start of conversion).
- When A/D conversion is completed, an "A/D conversion complete" interrupt request can be issued to the CPU. Because the generation of this interrupt can be used to start up the EI²OS and transfer the A/D conversion results to memory, this function is suitable for continuous processing.
- Startup triggers can be selected from among software, an external trigger (falling edge), and a timer (rising edge).

(1) Register Configuration

• A/D Channel Setting Register (ADCH)

This register specfies the A/D converter conversion channel.

Register name	Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
ADCH	000032H	ANS3	ANS2	ANS1	ANS0	ANE3	ANE2	ANE1	ANE0	00000000 B
		(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

• A/D Mode Register (ADMD)

This register specfies the A/D converter operation mode and the startup source.

Register name	Address	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	Initial value
ADMD	000033H	—	—	—	Reserved	MOD1	MOD0	STS1	STS0	- - - X0000 B
		(—)	(—)	(—)	(W)	(R/W)	(R/W)	(R/W)	(R/W)	

Note: Program "0" to bit 12 when write. Read value is indeterminated.

• A/D Control Status Register (ADCS)

This register is the A/D converter control and status register.

Register name	Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
ADCS	000034H	BUSY	INT	INTE	PAUS	—	—	STRT	Reserved	0000 - - 00 B
		(R/W)	(R/W)	(R/W)	(R/W)	(—)	(—)	(W)	(R/W)	

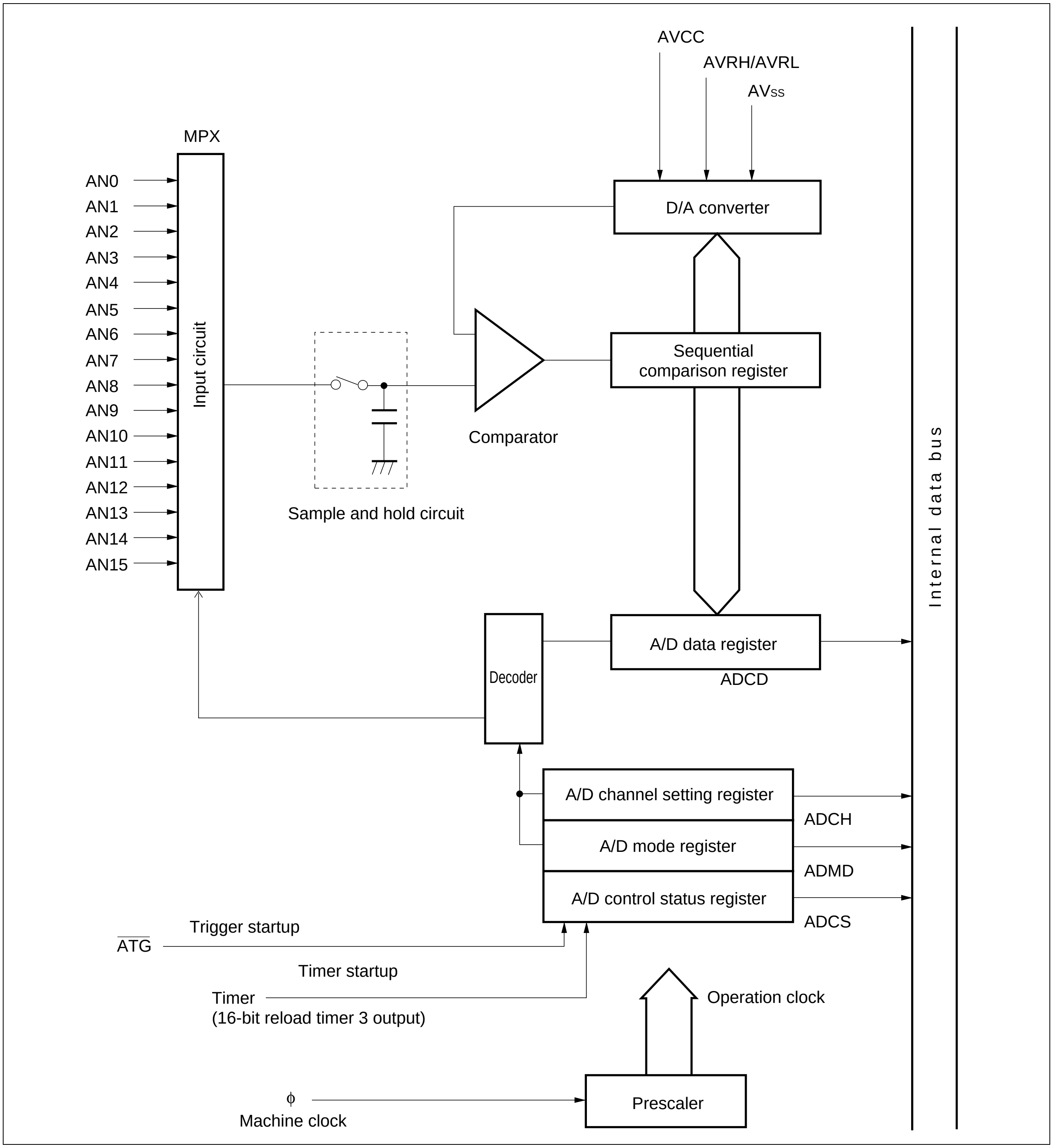
• A/D Data Register (ADCD)

This register stores the A/D converter conversion data.

Register name	Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
ADCD	000036H	D7	D6	D5	D4	D3	D2	D1	D0	XXXXXXXX B
		(R)	(R)	(R)	(R)	(R)	(R)	(R)	(R)	

Register name	Address	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	Initial value
ADCD	000037H	—	—	—	—	—	—	D9	D8	000000XX B
		(R)	(R)	(R)	(R)	(R)	(R)	(R)	(R)	

(2) Block Diagram



6. PWC (Pulse Width Count) Timer

The PWC (pulse width count) timer is a 16-bit multifunction up-count timer with an input-signal pulse-width count function and a reload timer function. The hardware configuration of this module is a 16-bit up-count timer, an input pulse divider with divide ratio control register, four count input pins, and a 16-bit control register. Using these components, the PWC timer provides the following features:

- Timer functions: An interrupt request can be generated at set time intervals.
  Pulse signals synchronized with the timer cycle can be output.
  The reference internal clock can be selected from among three internal clocks.
- Pulse-width count functions: The time between arbitrary pulse input events can be counted.
  The reference internal clock can be selected from among three internal clocks.
  Various count modes:
  "H" pulse width (↑ to ↓)/"L" pulse width (↓ to ↑)
  Rising-edge cycle (↑ to ↑/Falling-edge cycle (↓ to ↓)
  Count between edges (↑ or ↓ to ↓ or ↑)
  Cycle count can be performed by 2^{2n} division (n = 1, 2, 3, 4) of the input pulse, with an 8 bit input divider.
  An interrupt request can be generated once counting has been performed.
  The number of times counting is to be performed (once or subsequently) can be selected.

The MB90220 series has four channels for this module.

(1) Register Configuration

- **PWC Control Status Register 0 to 3 (PWCSR0 to PWCSR3)**

Register name	Address	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	Initial value
PWCSR0	000051 H	STRT	STOP	EDIR	EDIE	OVIR	OVIE	ERR	POUT	00000000B
PWCSR1	000053 H	(R/W)	(R/W)	(R)	(R/W)	(R/W)	(R/W)	(R)	(R/W)	
PWCSR2	000055 H									
PWCSR3	000057 H									

Register name	Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
PWCSR0	000050 H	CKS1	CKS0	PIS1	PIS0	S/C	MOD1	MOD1	MOD0	00000000B
PWCSR1	000052 H	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
PWCSR2	000054 H									
PWCSR3	000056 H									

- **PWC Data Buffer Register 0 to 3 (PWCR0 to PWCR3)**

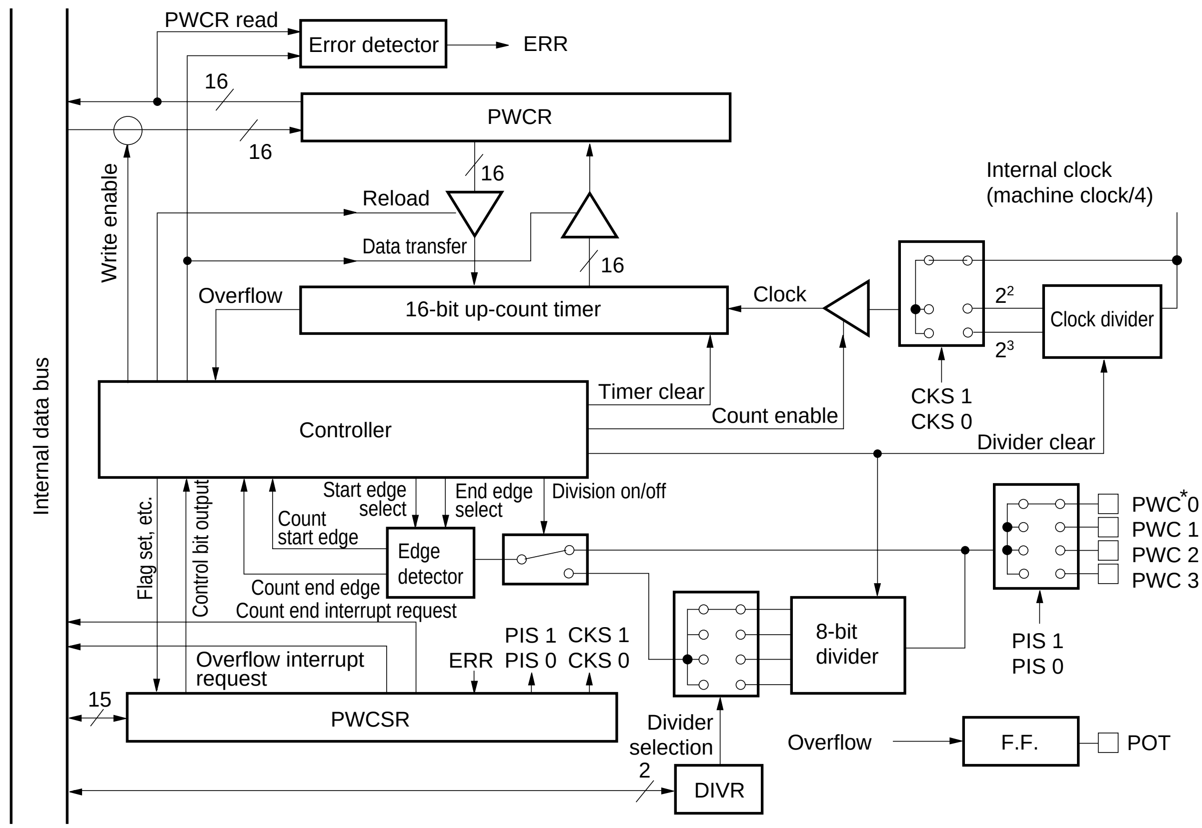
Register name	Address	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	Initial value
PWCR0	001F01 H									00000000B
PWCR1	001F03 H	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
PWCR2	001F05 H									
PWCR3	001F07 H									

Register name	Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
PWCR0	001F00 H									00000000B
PWCR1	001F02 H	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
PWCR2	001F04 H									
PWCR3	001F06 H									

• **PWC Division Ratio Control Register 0 to 3 (DIVR0 to DIVR3)**

Register name	Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
DIVR0	00007A H	—	—	—	—	—	—	MOD1	MOD0	00B
DIVR1	00007C H									
DIVR2	00007E H									
DIVR3	000080 H	(—)	(—)	(—)	(—)	(—)	(—)	(R/W)	(R/W)	

(2) Block Diagram



*: In the MB90220 series, only the module input PWC 0 of each channel is connected to the respective external pins.

Channel	POT pin
PWC ch. 0	PA 1/PWC 0/POT 0
PWC ch. 1	PA 2/PWC 1/POT 1/ASR 1
PWC ch. 2	PA 3/PWC 2/POT 2/ASR 2
PWC ch. 3	PA 4/PWC 3POT 3/ASR 3

7. DTP/External Interrupts

DTP (Data Transfer Peripheral) is located between external peripherals and the F²MC-16F CPU. It receives a DMA request or an interrupt request generated by the external peripherals and reports it to the F²MC-16F CPU to activate the extended intelligent I/O service or interrupt handler. The user can select two request levels of "H" and "L" for extended intelligent I/O service or, and four request levels of "H," "L," rising edge and falling edge for external interrupt requests. In MB90220, only parts corresponding to INT2 to INT0 are usable as external interrupt/DTP request.

Parts corresponding to INT7 to INT3 cannot be used as external interrupt/DTP request, but only for edge detection at external terminals.

Note: INT7 to INT3 are not usable as DTP/external interrupts.

(1) Register Configuration

• DTP/Interrupt Enable Register (ENIR)

Register name ENIR, Address 00003A H, Initial value 00000000B

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
EN7	EN6	EN5	EN4	EN3	EN2	EN1	EN0
(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)

• DTP/Interrupt Source Register (EIRR)

Register name EIRR, Address 00003B H, Initial value 00000000B

bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8
ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0
(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)

• Request Level Setting Register (ELVR)

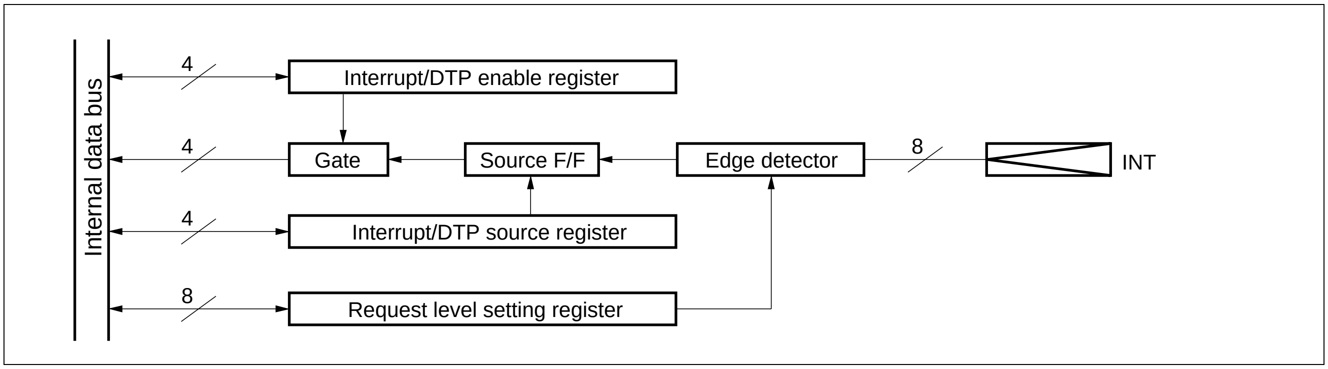
Register name ELVR, Address 00003D H, Initial value 00000000B

bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8
LB7	LA7	LB6	LA6	LB5	LA5	LB4	LA4
(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)

Register name ELVR, Address 00003C H, Initial value 00000000B

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
LB3	LA3	LB2	LA2	LB1	LA1	LB0	LA0
(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)

(2) Block Diagram



8. 24-bit Timer Counter

The 24-bit timer counter consists of a 24-bit up-counter, an 8-bit output buffer register, and a control register. The count value output by this timer counter is used to generate the base time used for input capture and output compare.

The interrupt functions provided are timer overflow interrupts and timer intermediate bit interrupts. The intermediate bit interrupt permits four time settings.

The 24-bit timer counter value is cleared to all zeroes by a reset.

(1) Register Configuration

- **Free-run Timer Control Register (TCCR)**

Register name	Address	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	Initial value
TCCR	000071H	—	—	Reserved	Reserved	Reserved	Reserved	Reserved	PR0	- - 111111B
		(—)	(—)	(W)	(W)	(R/W)	(R/W)	(R/W)	(R/W)	

Register name	Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
TCCR	000070H	CLR2	CLR	IVF	IVFE	TIM	TIME	TIS1	TIS0	11000000B
		(W)	(W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

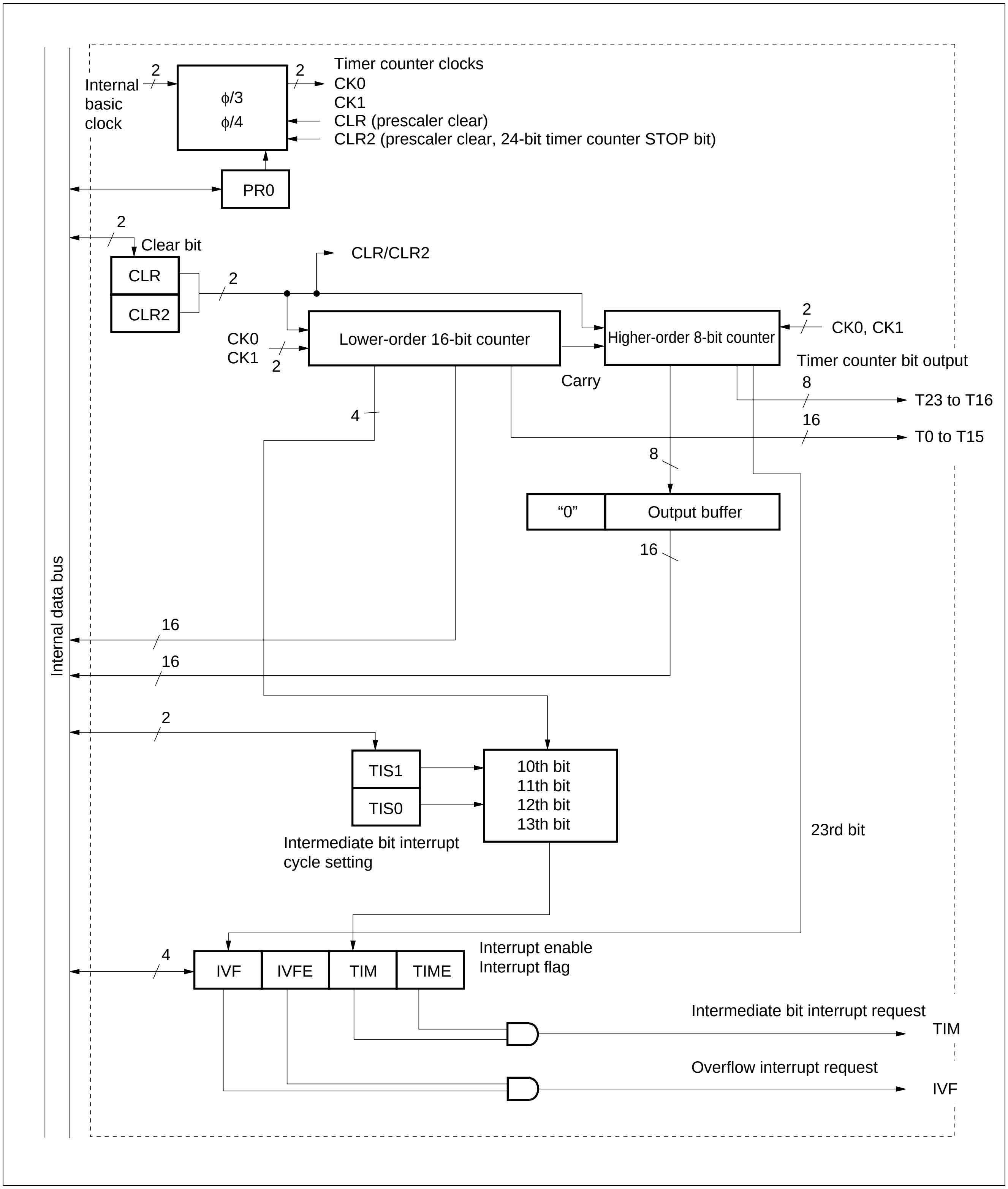
- **Free-run Timer Low-order Data Register (TCRL)**

Register name	Address	bit15 … bit0	Initial value	Access
TCRL	000072H 000073H	TCRL	00000000B	R

- **Free-run Timer High-order Data Register (TCRH)**

Register name	Address	bit15 … bit8	bit7 … bit0	Initial value	Access
TCRH	000074H 000075H	—	TCRH	00000000B	R

(2) Block Diagram



9. OCU (Output Compare Unit)

The OCU (Output Compare Unit) consists of a 24-bit output compare register, a comparator, and a control register.

The match detection signal is output when the contents of the output compare register match the contents of the 24-bit timer counter. This match detection signal can be used to change the output value of the corresponding pin, or can be used to generate an interrupt. One block consists of four output compare units, and the four output compare registers use one comparator to perform time division comparisons.

(1) Register Configuration

- **OCUO Control Register 00, 01 (CCR00, CCR01)**

Register name	Address	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	Initial value
CCR00 CCR02	000061 H 000063 H	—	—	—	—	MD3	MD2	MD1	MD0	- - - - 0000
		(—)	(—)	(—)	(—)	(R/W)	(R/W)	(R/W)	(R/W)	

Register name	Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
CCR00 CCR02	000060 H 000062 H	SEL3	SEL2	SEL1	SEL0	CPE3	CPE2	CPE1	CPE0	11110000
		(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

- **OCUO Control Register 10, 11 (CCR10, CCR11)**

Register name	Address	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	Initial value
CCR10 CCR11	000069 H 00006B H	ICE3	ICE2	ICE1	ICE0	IC3	IC2	IC1	IC0	00000000
		(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

Register name	Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
CCR10 CCR11	000068 H 00006A H	—	—	—	—	DOT3	DOT2	DOT1	DOT0	- - - - 0000
		(—)	(—)	(—)	(—)	(R/W)	(R/W)	(R/W)	(R/W)	

- **OCU Compare Low-order Data Register 00 to 07 (CPR00L to CPR07L)**

Register name	Address	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	Initial value
CPR00L CPR01L CPR02L CPR03L CPR04L CPR05L CPR06L CPR07L	001F11 H 001F15 H 001F19 H 001F1D H 001F21 H 001F25 H 001F29 H 001F2D H									00000000
		(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

Register name	Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
CPR00L CPR01L CPR02L CPR03L CPR04L CPR05L CPR06L CPR07L	001F10 H 001F14 H 001F18 H 001F1C H 001F20 H 001F24 H 001F28 H 001F2C H							—	—	00000000
		(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

- **Output Compare High-order Data Register 00 to 07 (CPR00H to CPR07H)**

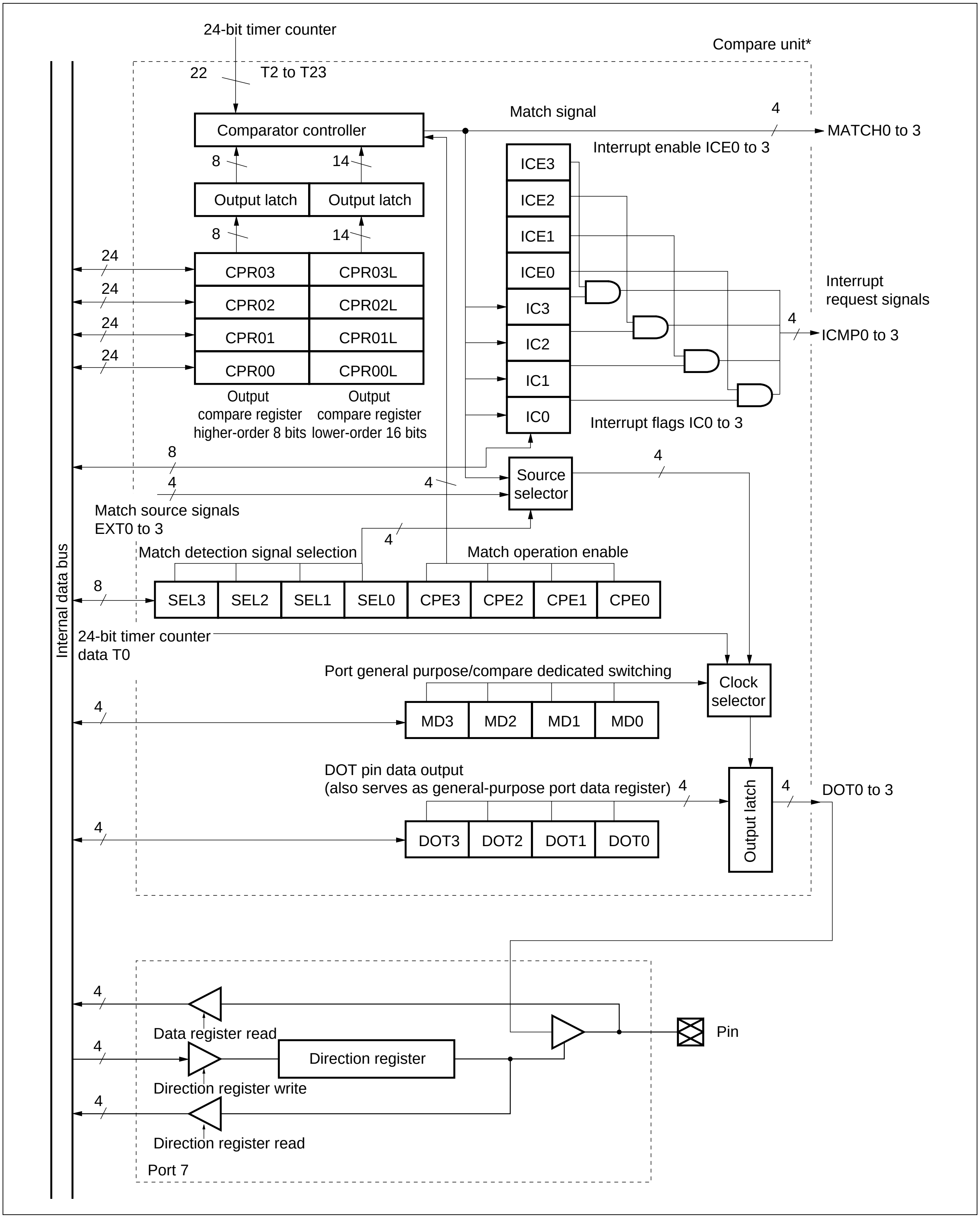
Register name	Address
CPR00	001F13 H
CPR01	001F17 H
CPR02	001F1B H
CPR03	001F1F H
CPR04	001F23 H
CPR05	001F27 H
CPR06	001F2B H
CPR07	001F2F H

bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	
								Initial value 00000000
(R)	(R)	(R)	(R)	(R)	(R)	(R)	(R)	

Register name	Address
CPR00	001F12 H
CPR01	001F16 H
CPR02	001F1A H
CPR03	001F1E H
CPR04	001F22 H
CPR05	001F26 H
CPR06	001F2A H
CPR07	001F2E H

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
						—	—	Initial value 00000000
(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

(2) Block Diagram



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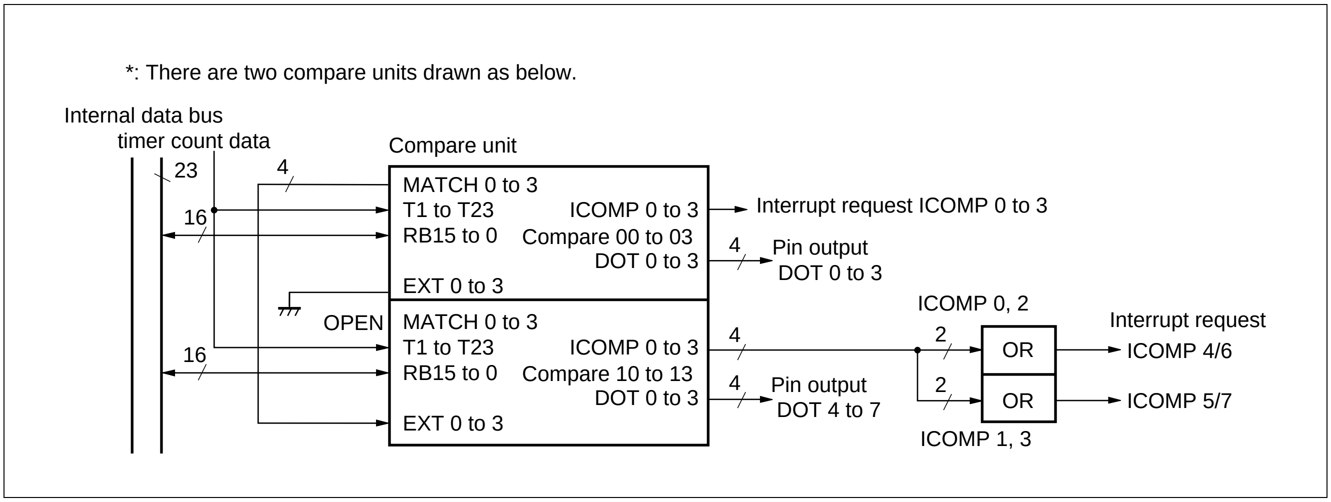

*: There are two compare units drawn as below.
Internal data bus
timer count data
23
4
16
16
OPEN
Compare unit
MATCH 0 to 3
T1 to T23
RB15 to 0
EXT 0 to 3
ICOMP 0 to 3
Compare 00 to 03
DOT 0 to 3
MATCH 0 to 3
T1 to T23
RB15 to 0
EXT 0 to 3
ICOMP 0 to 3
Compare 10 to 13
DOT 0 to 3
Interrupt request ICOMP 0 to 3
4
Pin output
DOT 0 to 3
4
4
Pin output
DOT 4 to 7
ICOMP 0, 2
2
2
OR
OR
ICOMP 1, 3
Interrupt request
ICOMP 4/6
ICOMP 5/7

10. ICU (Input Capture Unit)

This module detects either the rising edge, falling edge, or both edges of an externally input waveform and holds the value of the 24-bit timer counter at that time, while at the same time the module generates an interrupt request for the CPU. The module consists of a 24-bit input capture data register and a control register. There are four external input pins (ASR0 to ASR3); the operation of each input is described below.

ASR0 to ASR3: Each of these input pins has a corresponding input capture register. When the specified valid edge (↑ or ↓ or ↑ ↓) is detected, the register can be used to store the 24-bit timer counter value.

(1) Register Configuration

• **ICU Control Register 0 (ICC0)**

Register name	Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
ICCO	000058 H	EG3B	EG3A	EG2B	EG2A	EG1B	EG1A	EG0B	EG0A	00000000B
		(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

• **ICU Control Register 1 (ICC1)**

Register name	Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
ICCI	00005A H	IRE3	IRE2	IRE1	IRE0	IR3	IR2	IR1	IR0	00000000B
		(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

• **ICU Low-order Data Register (ICRL0 to ICRL3)**

Register name	Address	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	Initial value
ICRL0 ICRL1 ICRL2 ICRL3	001F50 H 001F54 H 001F58 H 001F5C H	D15	D14	D13	D12	D11	D10	D09	D08	XXXXXXXXB
		(R)	(R)	(R)	(R)	(R)	(R)	(R)	(R)	

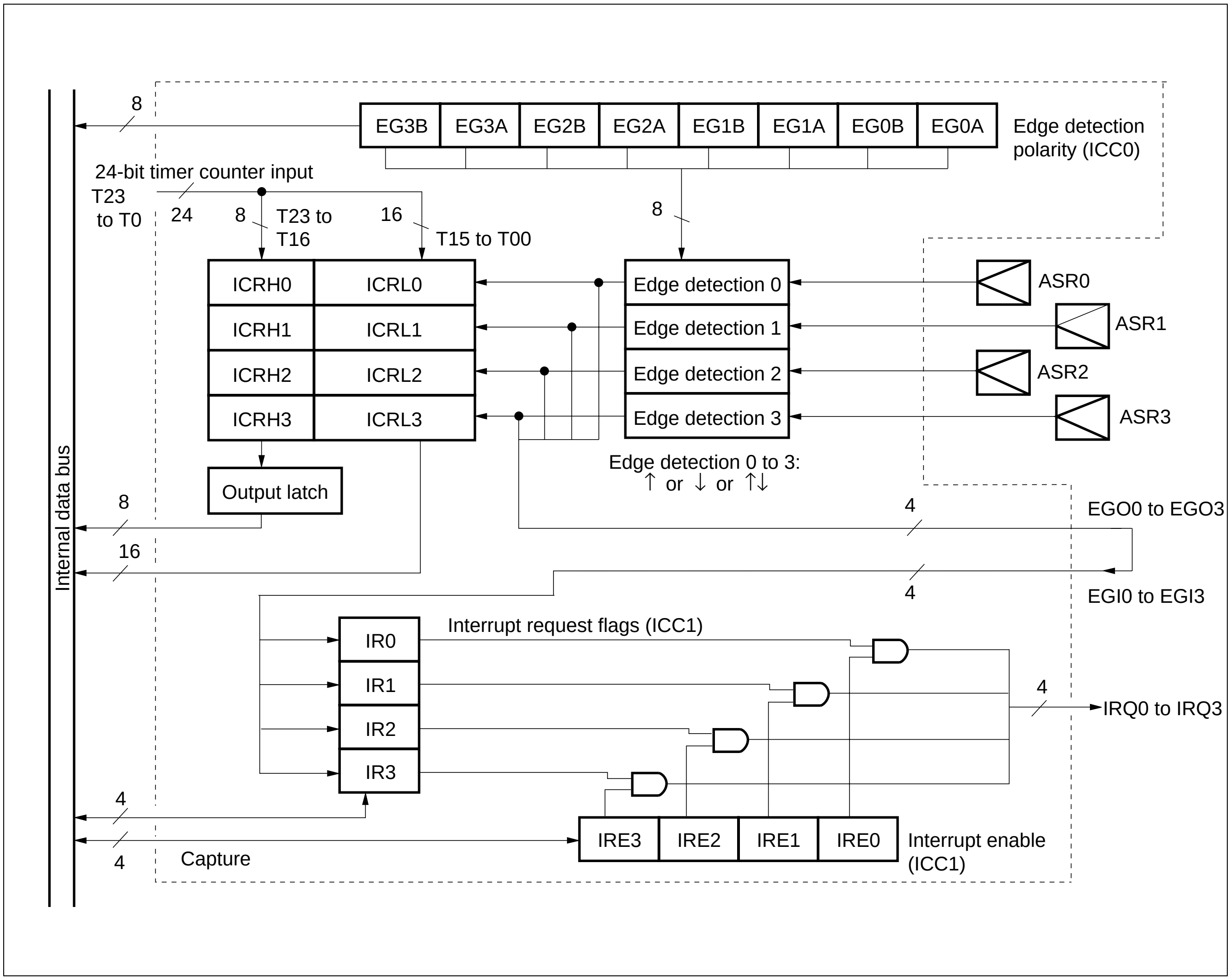
Register name	Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
ICRL0 ICRL1 ICRL2 ICRL3	001F51 H 001F55 H 001F59 H 001F5D H	D07	D06	D05	D04	D03	D02	D01	D00	XXXXXXXXB
		(R)	(R)	(R)	(R)	(R)	(R)	(R)	(R)	

• **ICU High-order Data Register (ICRH0 to ICRH3)**

Register name	Address	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	Initial value
ICRH0 ICRH1 ICRH2 ICRH3	001F52 H 001F56 H 001F5A H 001F5E H	—	—	—	—	—	—	—	—	XXXXXXXXB
		(R)	(R)	(R)	(R)	(R)	(R)	(R)	(R)	

Register name	Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
ICRH0 ICRH1 ICRH2 ICRH3	001F53 H 001F57 H 001F5B H 001F5F H	D23	D22	D21	D20	D19	D18	D17	D16	00000000B
		(R)	(R)	(R)	(R)	(R)	(R)	(R)	(R)	

(2) Block Diagram



11. 16-bit PPG Timer

This module can output a pulse synchronized with an external trigger or a software trigger. In addition, the cycle and duty ratio of the output pulse can be changed as desired by overwriting the two 16-bit register values.

PWM function: Synchronizes pulse with trigger, and permits programming of the pulse output by overwriting the register values mentioned above.
This function permits use as a D/A converter with the addition of external circuits.

One-shot function: Detects the edge of trigger input, and permits single-pulse output. There is no trigger input for PPG1.

This module consists of a 16-bit down-counter, a prescaler, a 16-bit synchronization setting register, a 16-bit duty register, a 16-bit control register, one external trigger input pin, and one PPG output pin.

(1) Register Configuration

- **PPG Control Status Register (PCNT0, PCNT1)**

Register name	Address
PCNT0	0004DH
PCNT1	0004FH

	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8
	CNTE	STGR	MDSE	RTRG	CKS1	CKS0	PGMS	—
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Overwrite during operation→	○	○	×	×	×	×	○	

Initial value 00000000B

Register name	Address
PCNT0	0004CH
PCNT1	0004EH

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	EGS1	EGS0	IREN	IRQF	IRS1	IRS0	POEN	OSEL
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
Overwrite during operation→	×	×	○	○	×	×	×	×

Initial value 00000000B

- **PPG0, PPG1 Cycle Setting Register (PCSP0, PCSP1)**

Register name	Address
PCSP0	001F49H
PCSP1	001F4DH

bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8
(W)	(W)	(W)	(W)	(W)	(W)	(W)	(W)

Initial value XXXXXXXXB

Register name	Address
PCSP0	001F48H
PCSP1	001F4CH

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
(W)	(W)	(W)	(W)	(W)	(W)	(W)	(W)

Initial value XXXXXXXXB

- **PPG0, PPG1 Duty Setting Register (PDUT0, PDUT1)**

Register name	Address
PDUT0	001F4BH
PDUT1	001F4FH

bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8
(W)	(W)	(W)	(W)	(W)	(W)	(W)	(W)

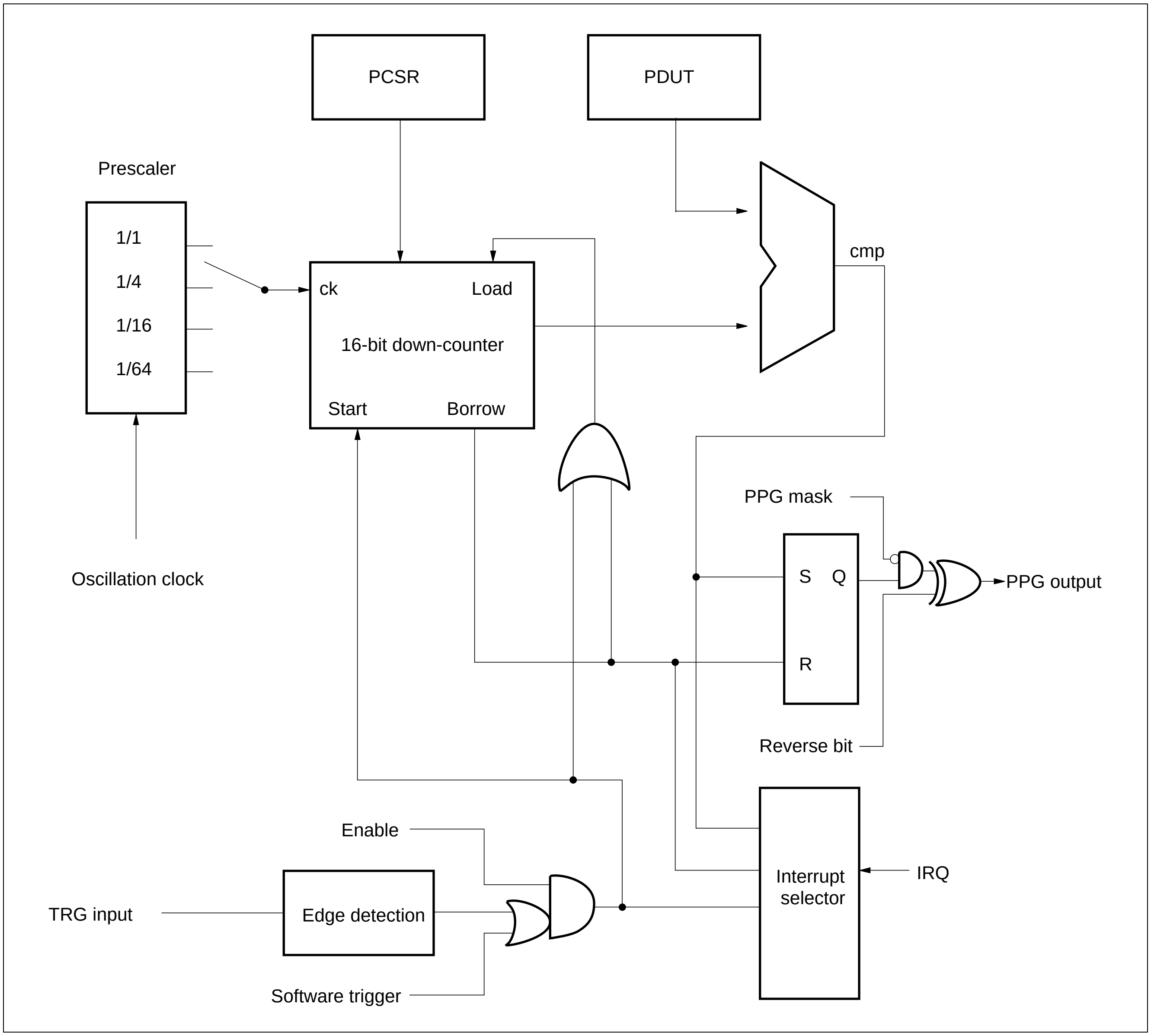
Initial value XXXXXXXXB

Register name	Address
PDUT0	001F4AH
PDUT1	001F4EH

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
(W)	(W)	(W)	(W)	(W)	(W)	(W)	(W)

Initial value XXXXXXXXB

(2) Block Diagram



12. Watchdog Timer and Timebase Timer Functions

The watchdog timer consists of a 2-bit watchdog counter using carry from an 18-bit timebase timer as the clock source, a control register, and a watchdog reset control section. The timebase timer consists of an 18-bit timer and an interval interrupt control circuit.

(1) Register Configuration

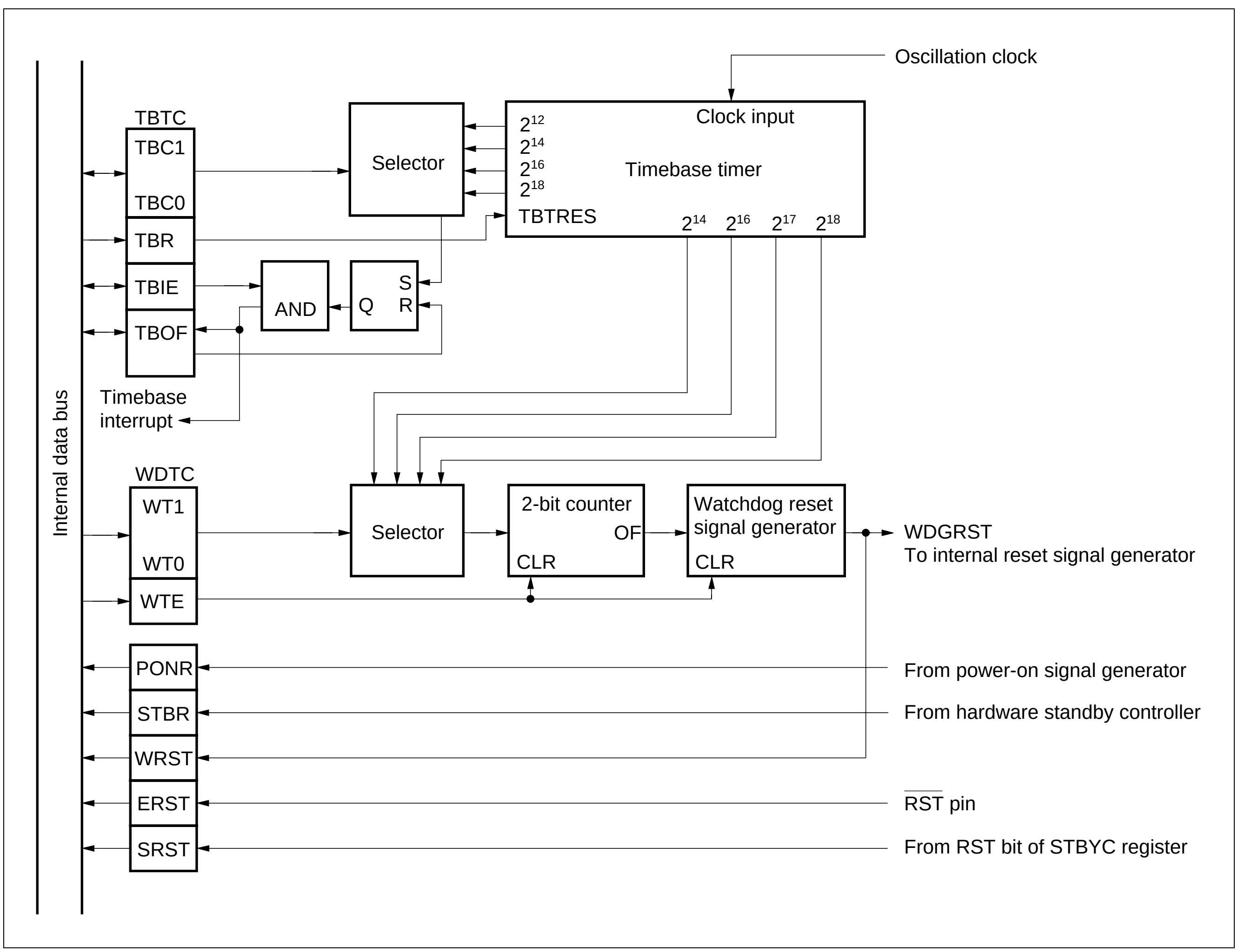
- **Watchdog Timer Control Register (WDTC)**

Register name	Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
WDTC	0000A8 H	PONR	STBR	WRST	ERST	SRST	WTE	WT1	WT0	XXXXXXXX
		(R)	(R)	(R)	(R)	(R)	(W)	(W)	(W)	

- **Timebase Timer Control Register (TBTC)**

Register name	Address	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	Initial value
TBTC	0000A9 H	—	—	—	TBIE	TBOF	TBR	TBC1	TBC0	- - - XXXXX
		(—)	(—)	(—)	(R/W)	(R/W)	(R)	(R/W)	(R/W)	

(2) Block Diagram



13. Delay Interruupt Generation Module

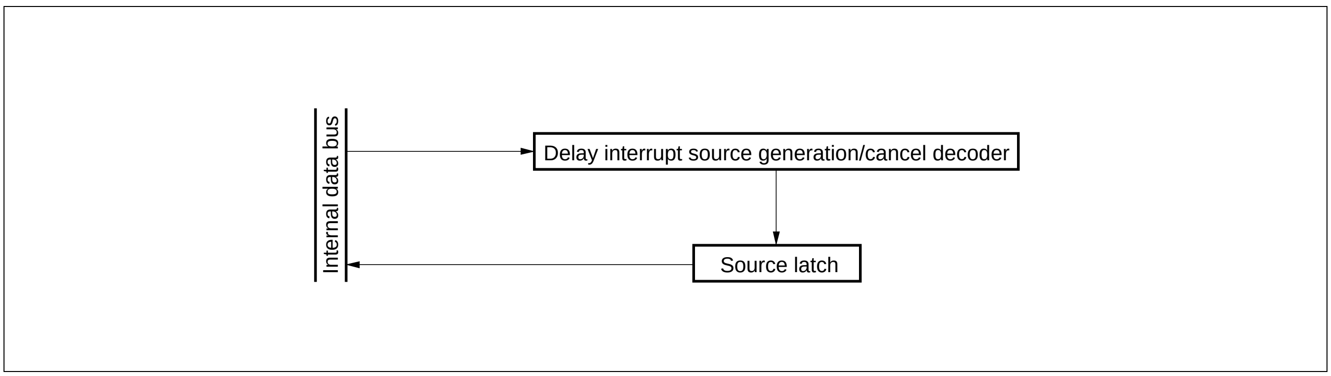
The delayed interrupt generation module is used to generate an interrupt task switching. Using this module allows an interrupt request to the F²MC-16F CPU to generated or cancel by software.

(1) Register Configuration

- **Delay Interrupt Source Generation/Cancel Register (DIRR)**

Register name	Address	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	Initial value
DIRR	00009F H	—	—	—	—	—	—	—	R0	- - - - - - - 0
		(—)	(—)	(—)	(—)	(—)	(—)	(—)	(R/W)	

(2) Block Diagram



14. Write-inhibit RAM

The write-inhibit RAM is write-protectable with the $\overline{WI}$ pin input. Maintaining the “L” level input to the $\overline{WI}$ pin prevents a certain area of RAM from being written. The $\overline{WI}$ pin has a 4-machine-cycle filter.

(1) Register Configuration

- **WI Control Register (WICR)**

Register name	Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
WICR	00008E H	—	—	—	WI	—	—	—	—	- - - X - - - -
		(—)	(—)	(—)	(R/W)	(—)	(—)	(—)	(—)	

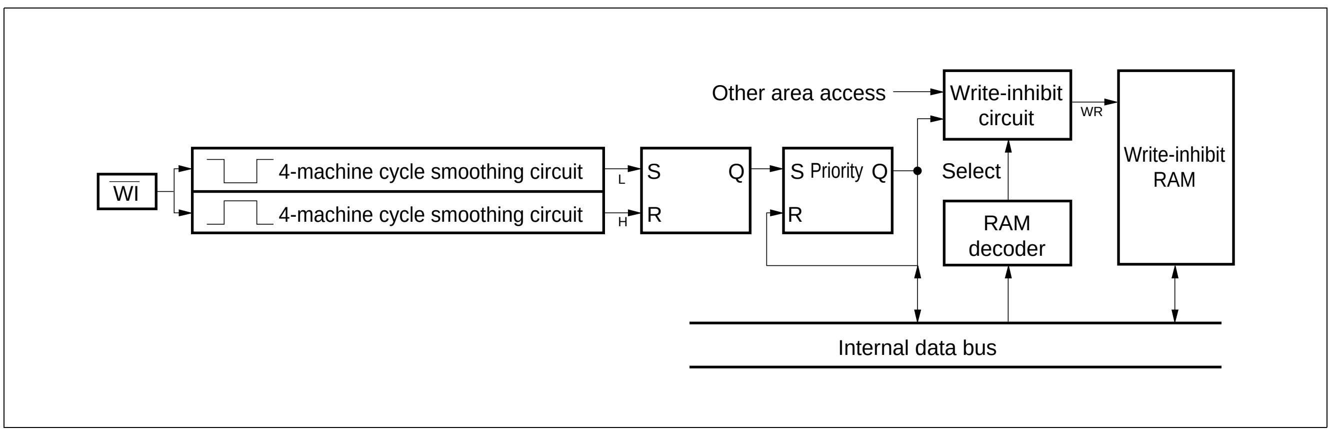
(2) Write-inhibit RAM Areas

Write-inhibit RAM areas: 000D00H to 000EFFH (MB90223)

001300H to 0014FFH (MB90224/P224A/P224B/W224A/W224B)

001500H to 0018FFH (MB90V220)

(3) Block Diagram



15. Low-power Consumption Modes, Oscillation Stabilization Delay Time, and Gear Function

The MB90220 series has three low-power consumption modes: the sleep mode, the stop mode, the hardware standby mode, and gear function.

Sleep mode is used to suspend only the CPU operation clock; the other components remain in operation. Stop mode and hardware standby mode stop oscillation, minimizing the power consumption while holding data.

The gear function divides the external clock frequency, which is used usually as it is, to provide a lower machine clock frequency. This function can therefore lower the overall operation speed without changing the oscillation frequency. The function can select the machine clock as a division of the frequency of crystal oscillation or external clock input by 1, 2, 4, or 16.

The OSC1 and OSC0 bits can be used to set the oscillation stabilization delay time for wake-up from stop mode or hardware standby mode.

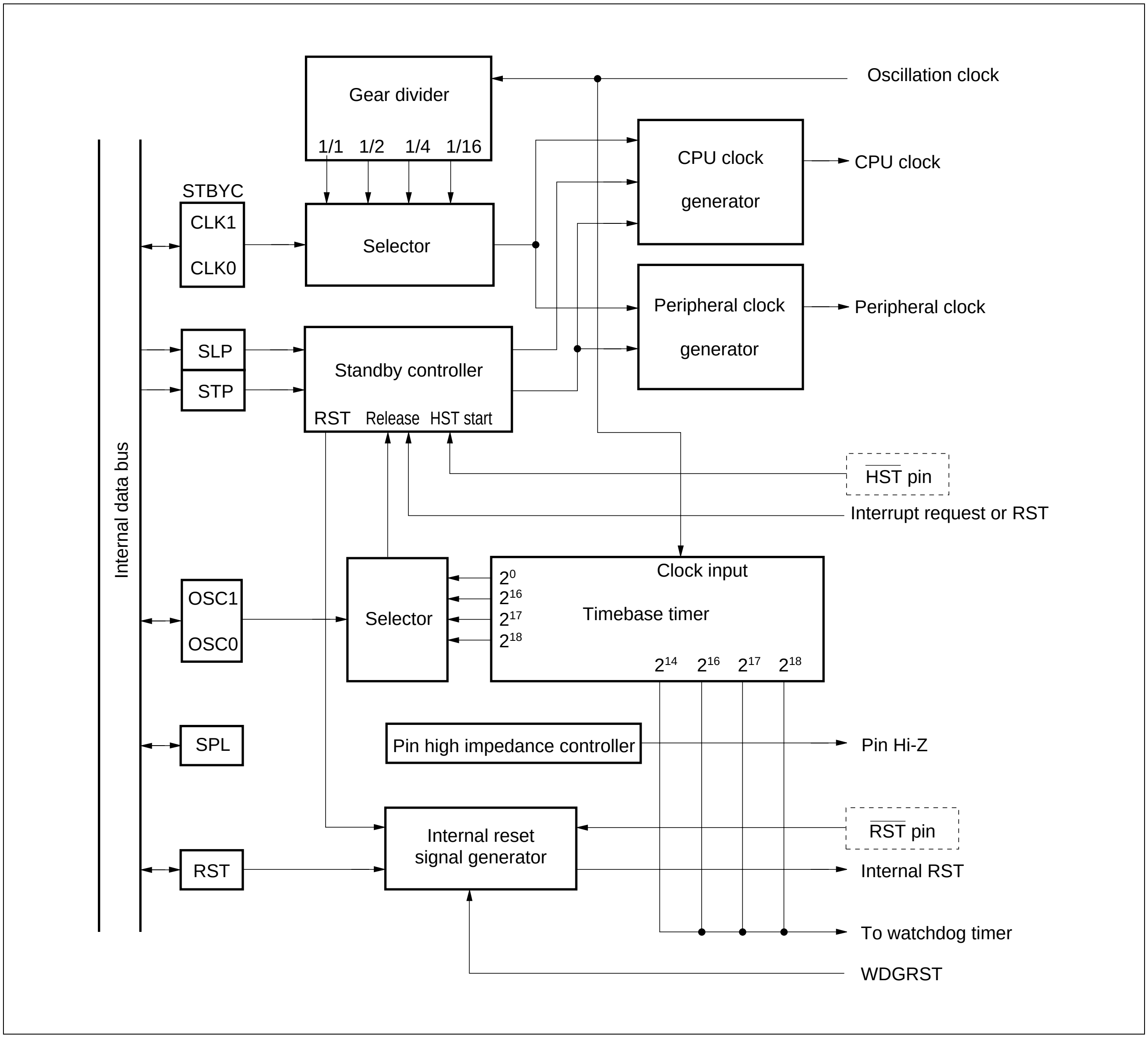
(1) Register Configuration

- **Standby Control Register (STBYC)**

Register name	Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
STBYC	0000A0 H	STP	SLP	SPL	RST	OSC1	OSC0	CLK1	CLK0	0001* * * *
		(W)	(W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

Note: The initial value (*) of bit0 to bit3 is changed by reset source.

(2) Block Diagram



■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

(V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min.	Max.		
Power supply voltage	V_{CC}	V_{CC}	V_{SS} – 0.3	V_{SS} + 7.0	V	
Program voltage	V_{PP}	V_{PP}	V_{SS} – 0.3	13.0	V	MB90P224A/P224B MB90W224A/W224B
Analog power supply voltage	AV_{CC}	AV_{CC}	V_{SS} – 0.3	V_{CC} + 0.3	V	Power supply voltage for A/D converter
	AVRH AVRL	AVRH AVRL	V_{SS} – 0.3	AV_{CC}	V	Reference voltage for A/D converter
Input voltage	V_I*1	—	V_{SS} – 0.3	V_{CC} + 0.3	V	
Output voltage	V_O	*2	V_{SS} – 0.3	V_{CC} + 0.3	V	
"L" level output current	I_{OL}	*3	—	20	mA	Rush current
"L" level total output current	ΣI_{OL}	*3	—	50	mA	Total output current
"H" level output current	I_{OH}	*2	—	–10	mA	Rush current
"H" level total output current	ΣI_{OH}	*2	—	–48	mA	Total output current
Power consumption	P_D	—	—	650	mW	
Operating temperature	T_A	—	–40	+105	°C	MB90223/224/P224B /W224B
			–40	+85	°C	MB90P224A/W224A
Storage temperature	Tstg	—	–55	+150	°C	

*1: V_I must not exceed V_{CC} + 0.3 V.

*2: Output pins: P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P70 to P77, P80 to P87, PA0 to PA7, PB0 to PB7, PC0 to PC5

*3: Output pins: P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, PA0 to PA7, PB0 to PB7, PC0 to PC5

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Condition

(V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min.	Max.		
Power supply voltage	V_{CC}	V_{CC}	4.5	5.5	V	When operating
			3.0	5.5	V	Retains the RAM state in stop mode
Analog power supply voltage	AV_{CC}	AV_{CC}	4.5	V_{CC} + 0.3	V	Power supply voltage for A/D converter
	AVRH	AVRH	AVRL	AV_{CC}	V	Reference voltage for A/D converter
	AVRL	AVRL	AV_{SS}	AVRH	V	
Clock frequency	F_C	—	10	16	MHz	MB90224/P224A/W224A MB90P224B/W224B
			10	12	MHz	MB90223
Operating temperature	T_A*	—	–40	+105	°C	Single-chip mode MB90223/224/P224B/W224B
			–40	+85	°C	Single-chip mode MB90P224A/W224A
			–40	+70	°C	External bus mode

* : Excluding the temperature rise due to the heat produced.

WARNING: Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representative beforehand.

3. DC Characteristics

Single-chip mode MB90223/224/P224B/W224B : (V_{CC} = +4.5 V to +5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +105°C)
MB90P224A/W224A : (V_{CC} = +4.5 V to +5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)
External bus mode : (V_{CC} = +4.5 V to +5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +70°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
"H" level input voltage	V_{IH}	X0	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	CMOS level input
	V_{IHS}	*1	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	Hysteresis input
	V_{IHM}	MD0 to MD2	—	V_{CC} – 0.3	—	V_{CC} + 0.3	V	
"L" level input voltage	V_{IL}	X0	—	V_{SS} – 0.3	—	0.3 V_{CC}	V	CMOS level input
	V_{ILS}	*1	—	V_{SS} – 0.3	—	0.2 V_{CC}	V	Hysteresis input
	V_{ILM}	MD0 to MD2	—	V_{SS} – 0.3	—	V_{SS} + 0.3	V	
"H" level output voltage	V_{OH}	*2	V_{CC} = 4.5 V I_{OH} = –4.0 mA	V_{CC} – 0.5	—	V_{CC}	V	
	V_{OH1}	X1	V_{CC} = 4.5 V I_{OH} = –2.0 mA	V_{CC} – 2.5	—	V_{CC}	V	
"L" level output voltage	V_{OL}	*3	V_{CC} = 4.5 V I_{OL} = 4.0 mA	0	—	0.4	V	
	V_{OL1}	X1	V_{CC} = 4.5 V I_{OL} = 2.0 mA	0	—	V_{CC} – 2.5	V	
Input leackage current	I_I	*1	V_{CC} = 5.5 V 0.2 V_{CC} < V_I < 0.8 V_{CC}	—	—	±10	µA	Hysteresis input Except pins with pull-up/pull-down resistor and $\overline{RST}$ pin
	I_{I2}	X0	V_{CC} = 5.5 V 0.2 V_{CC} < V_{I2} < 0.8 V_{CC}	—	—	±20	µA	
Pull-up resistor	R_{pulU}	$\overline{RST}$	—	22	50	110	kΩ	*4 MB90223/224 MB90P224A/W224A
		MD1	—	22	50	150	kΩ	*4 MB90223/224
Pull-down resistor	R_{pulD}	MD0 MD2	—	22	50	150	kΩ	*4 MB90223/224
Power supply voltage*8	I_{CC}	V_{CC}	F_C = 12 MHz	—	70*5	100	mA	MB90223
			F_C = 16 MHz	—	70*5	100	mA	MB90224
			F_C = 16 MHz	—	90*5	125	mA	MB90P224A/P224B MB90W224A/W224B
	I_{CCS}	V_{CC}	f_C = 16 MHz*9	—	—	60	mA	At sleep mode
	I_{CCH}	V_{CC}	—	—	5	10	µA	In stop mode T_A = +25°C At hardware standby

(Continued)

(Continued)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Analog power supply voltage	I_A	AV_{CC}	f_C = 16 MHz*9	—	3	7	mA	
	I_{AH}		—	—	—	5*6	µA	At stop mode
Input capacitance	C_{IN}	*7	—	—	10	—	pF	

*1: Hysteresis input pins
$\overline{RST}$, $\overline{HST}$, P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P80 to P87, P90 to P97, PA0 to PA7, PB0 to PB7, PC0 to PC5

*2: Ouput pins
P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P70 to P77, P80 to P87, PA0 to PA7, PB0 to PB7, PC0 to PC5

*3: Output pins
P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, PA0 to PA7, PB0 to PB7, PC0 to PC5

*4: A list of availabilities of pull-up/pull-down resistors

Pin name	MB90223/224	MB90P224A/W224A	MB90P224B/W224B
$\overline{RST}$	Availability of pull-up resistors is optionally defined.	Pull-up resistors available	Unavailable
MD1	Pull-up resistors available	Unavailable	Unavailable
MD0, MD2	Pull-up resistors available	Unavailable	Unavailable

*5: V_{CC} = +5.0 V, V_{SS} = 0.0 V, T_A = +25°C, F_C = 16 MHz
*6: The current value applies to the CPU stop mode with A/D converter inactive (V_{CC} = AV_{CC} = AVRH = +5.5 V).
*7: Other than V_{CC}, V_{SS}, AV_{CC} and AV_{SS}
*8: Measurement condition of power supply current; external clock pin and output pin are open.
Measurement condition of V_{CC}; see the table above mentioned.
*9: F_C = 12 MHz for MB90223

4. AC Characteristics

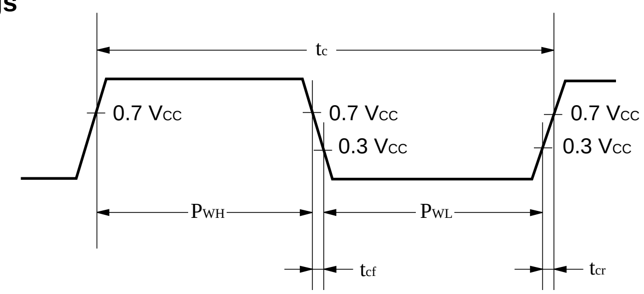
(1) Clock Timing Standards

Single-chip mode MB90223/224/P224B/W224B : (V_{CC} = +4.5 to +5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +105°C)
MB90P224A/W224A : (V_{CC} = +4.5 to +5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)
External bus mode : (V_{CC} = +4.5 to +5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +70°C)

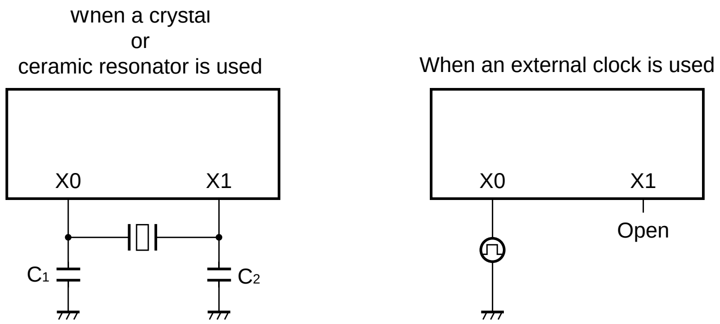
Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Clock frequency	F_C	X0, X1	—	10	—	16	MHz	MB90224/ P224A/P224B MB90W224A/ W224B
				10	—	12	MHz	MB90223
Clock cycle time	t_C	X0, X1	—	62.5	—	100	ns	MB90224/ P224A/P224B MB90W224A/ W224B
				83.4	—	100	ns	MB90223
Input clock pulse width	P_{WH} P_{WL}	X0	—	0.4 t_C	—	0.6 t_C	ns	Equivalent to 60% duty ratio
Input clock rising/falling times	t_{cr} t_{cf}	X0	—	—	—	8	ns	t_{cr} + t_{cf}

t_C = 1/f_C

- **Clock Input Timings**



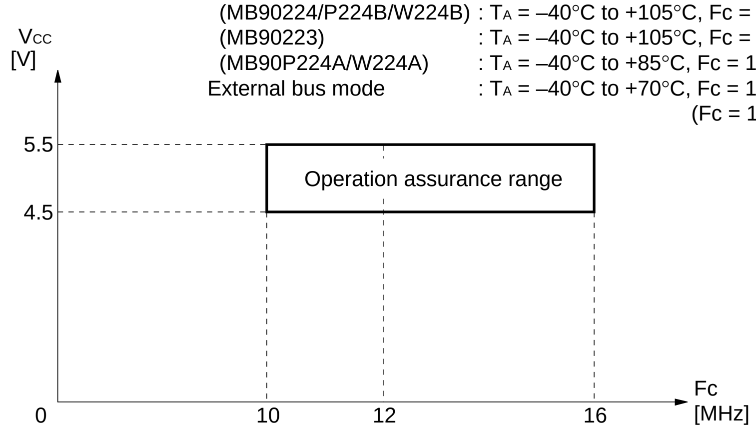
- **Clock Conditions**



C_1 = C_2 = 10 pF
Select the optimum capacity value for the resonator

- **Relationship between Clock Frequency and Supply Voltage**

Single-chip mode
(MB90224/P224B/W224B) : T_A = –40°C to +105°C, Fc = 10 to 16 MHz
(MB90223) : T_A = –40°C to +105°C, Fc = 10 to 12 MHz
(MB90P224A/W224A) : T_A = –40°C to +85°C, Fc = 10 to 16 MHz
External bus mode : T_A = –40°C to +70°C, Fc = 10 to 16 MHz
(Fc = 10 to 12 MHz, only for MB90223)

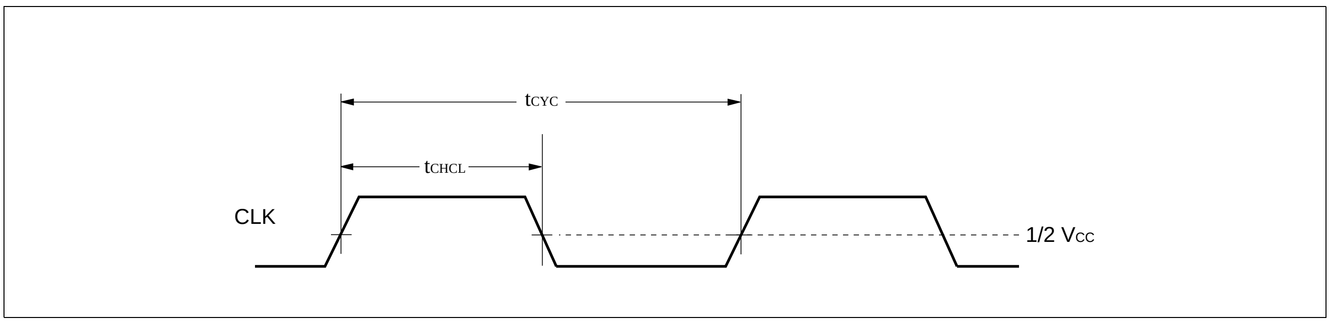


(2) Clock Output Timing

(External bus mode: V_{CC} = +4.5 V to +5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +70°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Machine cycle time	t_{CYC}	CLK	Load condition: 80 pF	62.5	—	1600	ns	MB90224/ P224A/P224B MB90W224A/ 224B
				83.4	—	1600	ns	MB90223
CLK ↑ → CLK↓	t_{CHCL}	CLK		$t_{CYC}/2 - 20$	—	$t_{CYC}/2$	ns	

$t_{CYC} = n/F_C$, n gear ratio (1, 2, 4, 16)

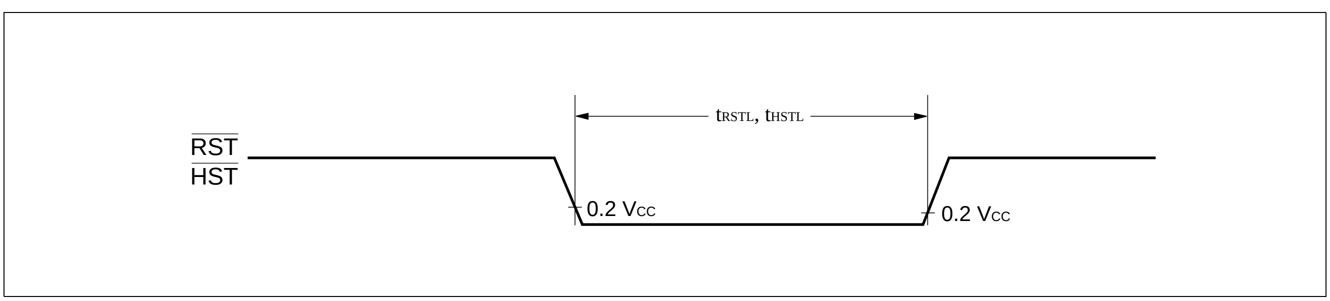


(3) Reset and Hardware Standby Input Standards

Single-chip mode MB90223/224/P224B/W224B: (V_{CC} = +4.5 V to +5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +105°C)
MB90P224A/W224A : (V_{CC} = +4.5 V to +5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)
External bus mode : (V_{CC} = +4.5 V to +5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +70°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Reset input time	t_{RSTL}	$\overline{RST}$	—	5 t_{CYC}	—	—	ns	
Hardware standby input time	t_{HSTL}	$\overline{HST}$		5 t_{CYC}	—	—	ns	*

*: The machine cycle time (t_{CYC}) at hardware standby is set to 1/16 divided oscillation.



(4) Power on Supply Specifications (Power-on Reset)

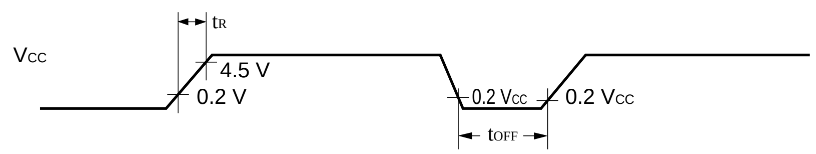
Single-chip mode MB90223/224/P224B/W224B: (V_{CC} = +4.5 V to +5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +105°C)
MB90P224A/W224A : (V_{CC} = +4.5 V to +5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)
External bus mode : (V_{CC} = +4.5 V to +5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +70°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Power supply rising time	t_R	V_{CC}	—	—	—	30	ms	*
Power supply cut-off time	t_{OFF}	V_{CC}	—	1	—	—	ms	

* : Before power supply rising, it is required to be V_{CC} < 0.2 V.

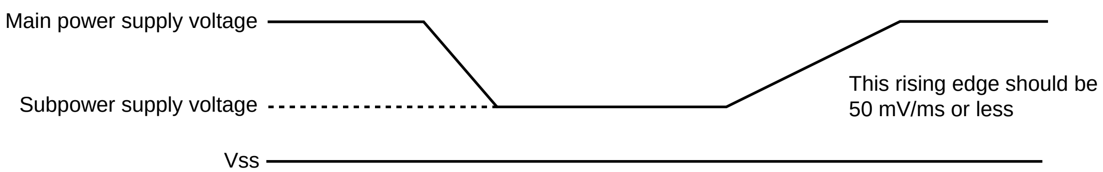
Notes: • Power-on reset assumes the above values.
• Whether the power-on reset is required or not, turn the power on according to these characteristics and trigger the power-on reset.
• There are internal registers (STBYC, etc.) which is initialized only by the power-on reset in the device.

• **Power-on Reset**



Note: Note on changing power supply
Even if above characteristics are not insufficient, abrupt changes in power supply voltage may cause a power-on reset. Therefore, at the time of a momentary changes such as when power is turned on, rise the power smoothly as shown below.

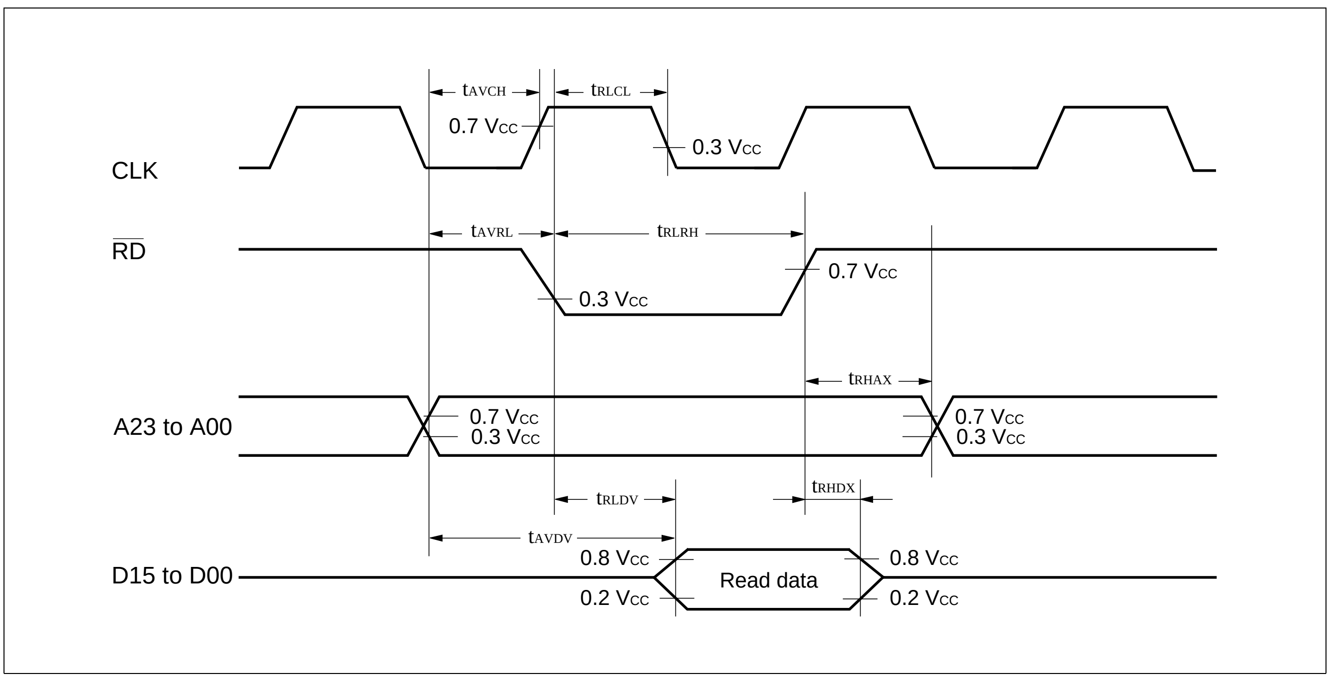
• **Changing Power Supply**



(5) Bus Read Timing

(V_{CC} = +4.5 V to +5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +70°C)

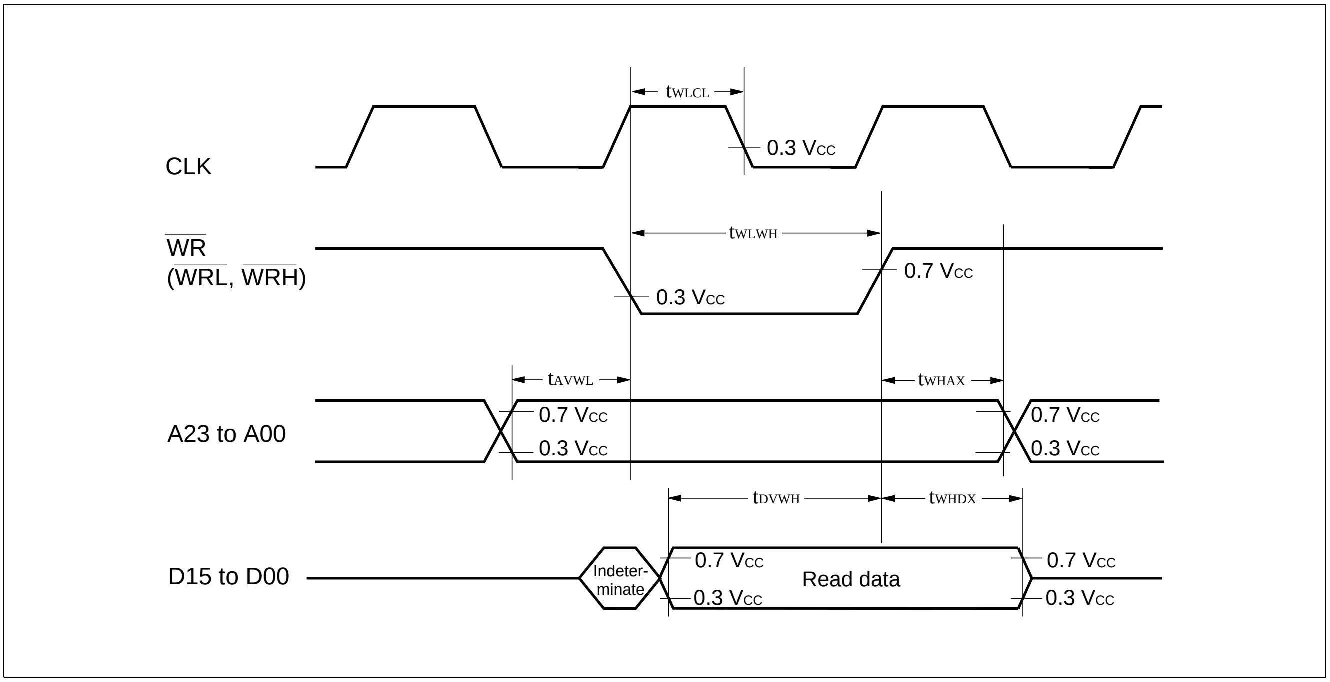
Parameter	Symbol	Pin name	Condition	Value Min.	Value Max.	Unit	Remarks
Valid address → $\overline{RD}$ ↓ time	t_{AVRL}	A23 to A00		$t_{CYC}/2 - 20$	—	ns	
$\overline{RD}$ pulse width	t_{RLRH}	$\overline{RD}$		$t_{CYC} - 25$	—	ns	
$\overline{RD}$ ↓ → Valid data input	t_{RLDV}			—	$t_{CYC} - 30$	ns	
$\overline{RD}$ ↑ → Data hold time	t_{RHDX}	D15 to D00	Load condition: 80 pF	0	—	ns	
Valid address → Valid data input	t_{AVDV}			—	$3\ t_{CYC}/2 - 40$	ns	
$\overline{RD}$ ↑ → Address valid time	t_{RHAX}	A23 to A00		$t_{CYC}/2 - 20$	—	ns	
Valid address → CLK ↑ time	t_{AVCH}	A23 to A00 CLK		$t_{CYC}/2 - 25$	—	ns	
$\overline{RD}$ ↓ → CLK ↓ time	t_{RLCL}	$\overline{RD}$, CLK		$t_{CYC}/2 - 25$	—	ns	



(6) Bus Write Timing

(V_{CC} = +4.5 V to +5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +70°C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Valid address → $\overline{WR}$ ↓ time	t_{AVWL}	A23 to A00	Load condition: 80 pF	$t_{CYC}/2 - 20$	—	ns	
$\overline{WR}$ pulse width	t_{WLWH}	$\overline{WRL}$, $\overline{WRH}$		$t_{CYC} - 25$	—	ns	
Valid data output → $\overline{WR}$ ↑ time	t_{DVWH}	D15 to D00		$t_{CYC} - 40$	—	ns	
$\overline{WR}$ ↑ → Data hold time	t_{WHDX}	D15 to D00		$t_{CYC}/2 - 20$	—	ns	
$\overline{WR}$ ↑ → Address valid time	t_{WHAX}	A23 to A00		$t_{CYC}/2 - 20$	—	ns	
$\overline{WR}$ ↓ → CLK ↓ time	t_{WLCL}	$\overline{WRL}$, $\overline{WRH}$, CLK		$t_{CYC}/2 - 25$	—	ns	

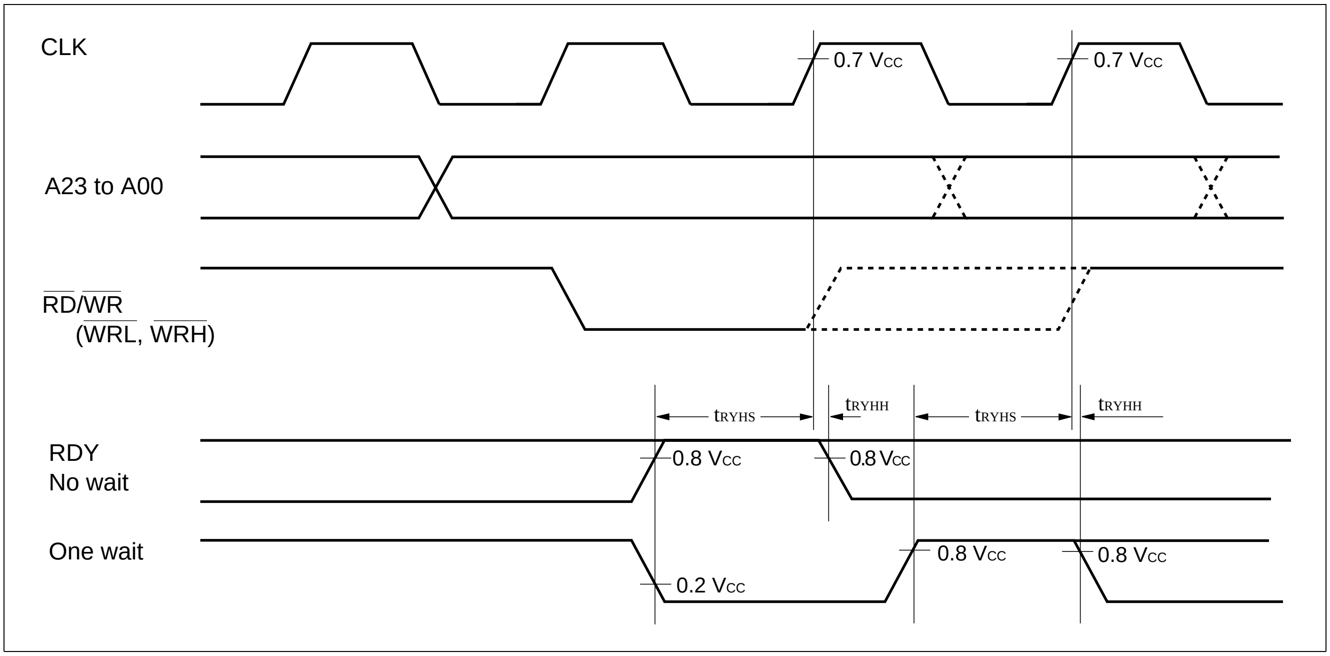


(7) Ready Input Timing

(V_{CC} = +4.5 V to +5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +70°C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
RDY setup time	t_{RYHS}	RDY	Load condition: 80 pF	40	—	ns	
RDY hold time	t_{RYHH}	RDY		0	—	ns	

Note: Use the auto-ready function if the RDY setup time is insufficient.

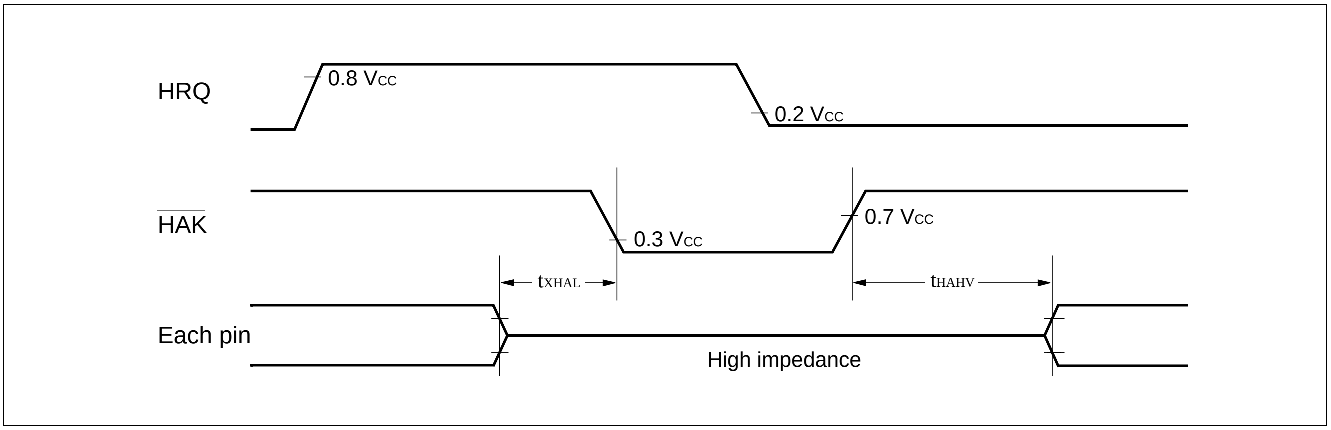


(8) Hold Timing

(V_{CC} = +4.5 V to +5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +70°C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Pin floating → $\overline{\text{HAK}}$ ↓ time	t_{XHAL}	$\overline{\text{HAK}}$	Load condition: 80 pF	30	t_{CYC}	ns	
$\overline{\text{HAK}}$ ↑ time → pin valid time	t_{HAHV}	$\overline{\text{HAK}}$		t_{CYC}	2 t_{CYC}	ns	

Note: It takes at least one machine cycle for $\overline{\text{HAK}}$ to vary after HRQ is fetched.



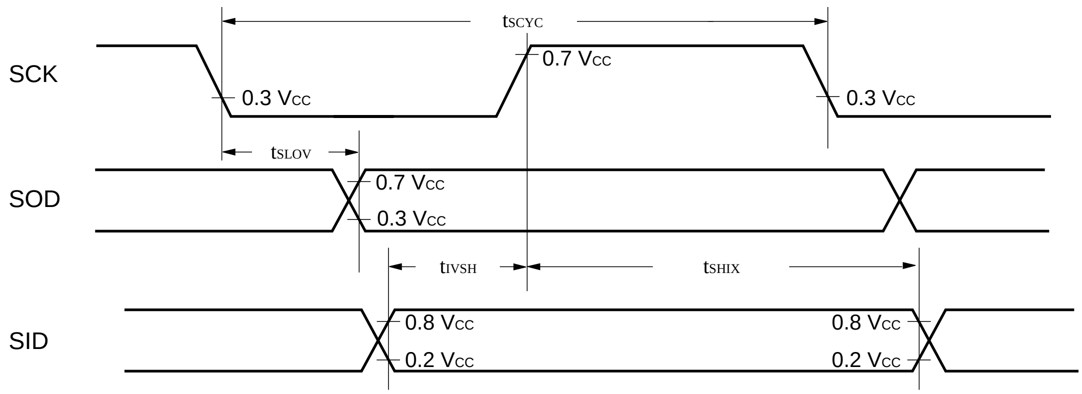
(9) UART Timing

Single-chip mode MB90223/224/P224B/W224B: (V_{CC} = +4.5 V to +5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +105°C)
MB90P224A/W224A : (V_{CC} = +4.5 V to +5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)
External bus mode : (V_{CC} = +4.5 V to +5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +70°C)

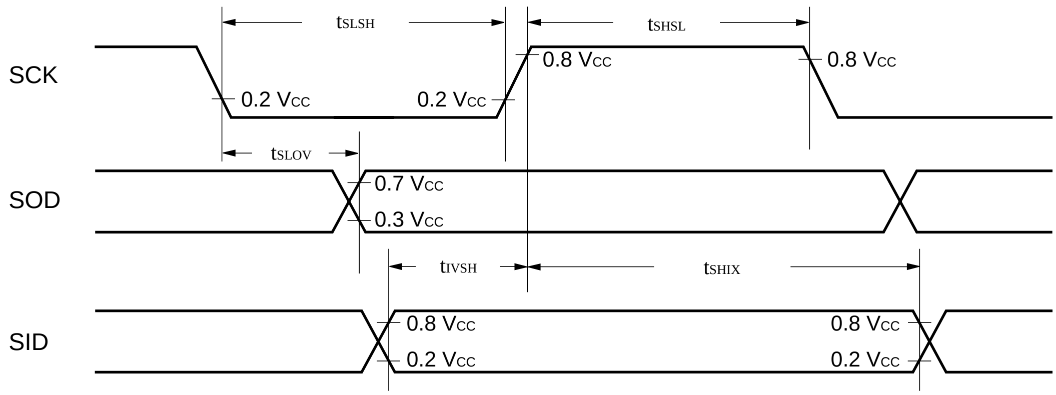
Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Serial clock cycle time	t_{SCYC}	—	Load condition: 80 pF	8 t_{CYC}	—	ns	Internal clock operation output pin
SCLK ↓ → SOUT delay time	t_{SLOV}	—		–80	80	ns	
Valid SIN → SCLK ↑	t_{IVSH}	—		100	—	ns	
SCLK ↑ → Valid SIN hold time	t_{SHIX}	—		60	—	ns	
Serial clock “H” pulse width	t_{SHSL}	—	Load condition: 80 pF	4 t_{CYC}	—	ns	External clock operation output pin
Serial clock “L” pulse width	t_{SLSH}	—		4 t_{CYC}	—	ns	
SCLK ↓ → SOUT delay time	t_{SLOV}	—		—	150	ns	
Valid SIN → SCLK ↑	t_{IVSH}	—		60	—	ns	
SCLK ↑ → valid SIN hold time	t_{SHIX}	—		60	—	ns	

Notes: • These AC characteristics assume in CLK synchronization mode.
• “t_{CYC}” is the machine cycle (unit: ns).

• **Internal Shift Clock Mode**



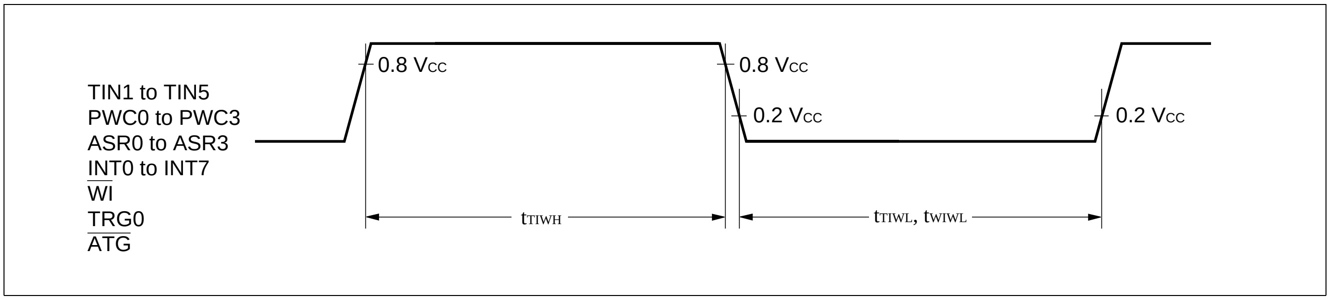
• **External Shift Clock Input Mode**



(10) Resourse Input Timing

Single-chip mode MB90223/224/P224B/W224B: (V_{CC} = +4.5 V to +5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +105°C)
MB90P224A/W224A : (V_{CC} = +4.5 V to +5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)
External bus mode : (V_{CC} = +4.5 V to +5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +70°C)

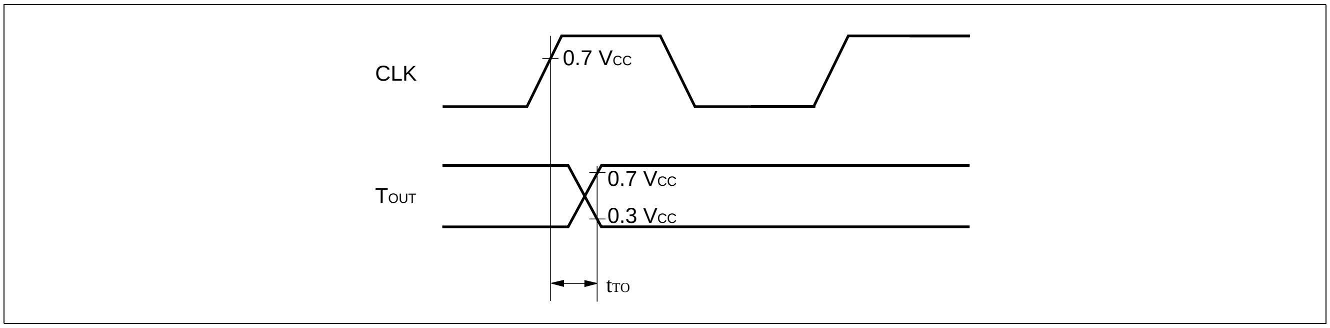
Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Input pulse width	t_{TIWH} t_{TIWL}	TIN1 to TIN5	Load condition: 80 pF	4 t_{CYC}	—	—	ns	External event count input mode
				2 t_{CYC}	—	—	ns	Trigger input/gate input mode
		PWC0 to PWC3		2 t_{CYC}	—	—	ns	
		ASR0 to ASR3		2 t_{CYC}	—	—	ns	
		INT0 to INT7		3 t_{CYC}	—	—	ns	
		TRG0		2 t_{CYC}	—	—	ns	
		$\overline{\text{ATG}}$		2 t_{CYC}	—	—	ns	
	t_{WIWL}	$\overline{\text{WI}}$		4 t_{CYC}	—	—	ns	



(11) Resourse Output Timing

Single-chip mode MB90223/224/P224B/W224B: (V_{CC} = +4.5 V to +5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +105°C)
MB90P224A/W224A : (V_{CC} = +4.5 V to +5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)
External bus mode : (V_{CC} = +4.5 V to +5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +70°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
CLK ↑ → T_{OUT} transition time	t_{TO}	TOT0 to TOT5 PPG0 to PPG1 POT0 to POT3 DOT0 to DOT7	Load condition: 80 pF	—	—	30	ns	



5. A/D Converter Electrical Characteristics

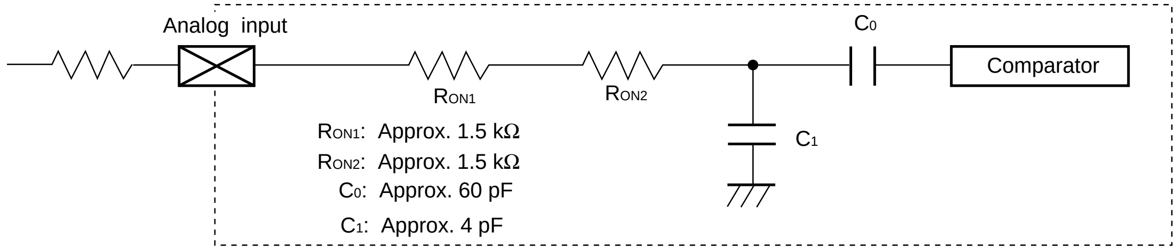
Single-chip mode MB90223/224/P224B/W224B
: (AV_{CC} = V_{CC} = +4.5 V to +5.5 V, AV_{SS} =V_{SS} = 0.0 V, T_A = –40°C to +105°C, +4.5 V ≤ AVRH – AVRL)
MB90P224A/W224A
: (AV_{CC} = V_{CC} = +4.5 V to +5.5 V, AV_{SS} = V_{SS} =0.0 V, T_A = –40°C to +85°C, +4.5 V ≤ AVRH – AVRL)
External bus mode : (AV_{CC} = V_{CC} = +4.5 V to +5.5 V, AV_{SS} = V_{SS} =0.0 V, T_A = –40°C to +70°C, +4.5 V ≤ AVRH – AVRL)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Resolution	n	—	—	—	—	10	bit	
Total error	—	—	—	—	—	±3.0	LSB	
Linearity error	—	—	—	—	—	±2.0	LSB	
Differential linearity error	—	—	—	—	—	±1.5	LSB	
Zero transition voltage	V_{0T}	AN00 to AN15	—	AVRL – 1.5	AVRL + 0.5	AVRL + 2.5	LSB	
Full-scale transition voltage	V_{FST}		—	AVRH – 3.5	AVRH – 1.5	AVRH + 0.5	LSB	
Conversion time*1	T_{CONV}	—	t_{CYC} = 62.5 ns	6.125	—	—	µs	98 machine cycles
Sampling period	T_{SAMP}	—		3.75	—	—	µs	60 machine cycles
Analog port input current	I_{AIN}	AN00 to AN15	—	—	—	±0.1	µA	
Analog input voltage	V_{AIN}		—	AVRL	—	AVRH	V	
Analog reference voltage	—	AVRH	—	AVRL	—	AV_{CC}	V	
		AVRL	—	AV_{SS}	—	AVRH	V	
Reference voltage supply current	I_R	AVRH	—	—	200	500	µA	
	I_{RH}		—	—	—	5*2	µA	
Variation between channels	—	AN00 to AN15	—	—	—	4	LSB	

*1: These standards in this table are for MB90224/P224A/P224B/W224A/W224B.
MB90223: Minimum conversion time is 8.17 µs and minimum sampling time is 5 µs at t_{CYC} = 83.4 ns.
*2: The current value applies to the CPU stop mode with the A/D converter inactive (V_{CC} = AV_{CC} = AVRH = +5.5 V).

Notes:
(1) The error becomes larger as | AVRH – AVRL | becomes smaller.
(2) Use the output impedance of the external circuit for analog input under the following conditions:
External circuit output impedance < approx. 10 kΩ (Sampling time approx. 3.75 µs, t_{CYC} = 62.5 ns)
(3) Precision values are standard values applicable to sleep mode.
(4) If V_{CC}/AV_{CC} or V_{SS}/AV_{SS} is caused by a noise to drop to below the analog input volgtage, the analog input current is likely to increase. In such cases, a bypass capacitor or the like should be provided in the external circuit to suppress the noise.

- **Analog Input Circuit Mode**



Note: The values shown here are reference values.

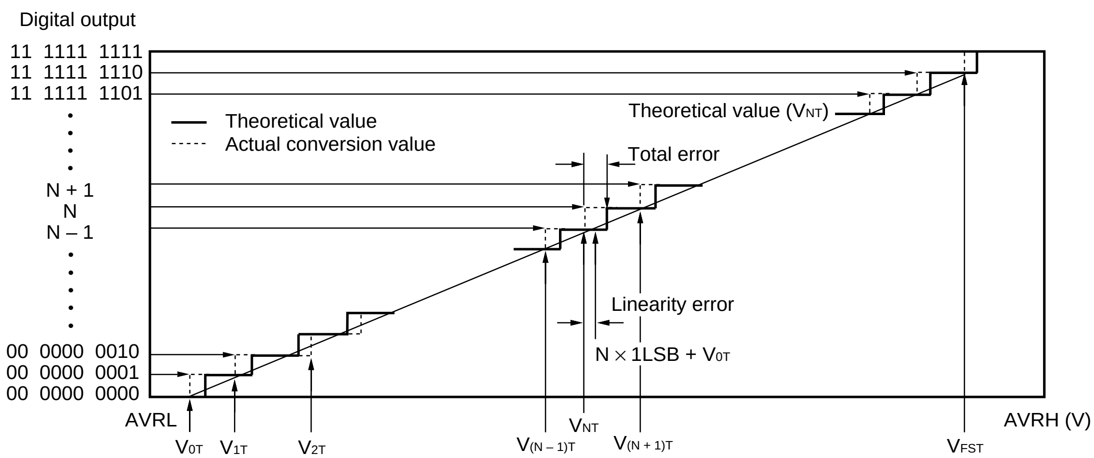
6. A/D Converter Glossary

Resolution: Analog changes that are identifiable with the A/D converter
When the number of bits is 10, analog voltage can be divided into $2^{10} = 1024$.

Total error: Difference between actual and logical values. This error is caused by a zero transition error, full-scale transition error, linearity error, differential linearity error, or by noise.

Linearity error: The deviation of the straight line connecting the zero transition point ("00 0000 0000" ↔ "00 0000 0001") with the full-scale transition point ("11 1111 1111" ↔ "11 1111 1110") from actual conversion characteristics

Differential linearity error: The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value



$1\text{ LSB} = \dfrac{V_{FST} - V_{0T}}{1022}$, $\quad 1\text{ LSB theoretical value} = \dfrac{AVRH - AVRL}{1022}$

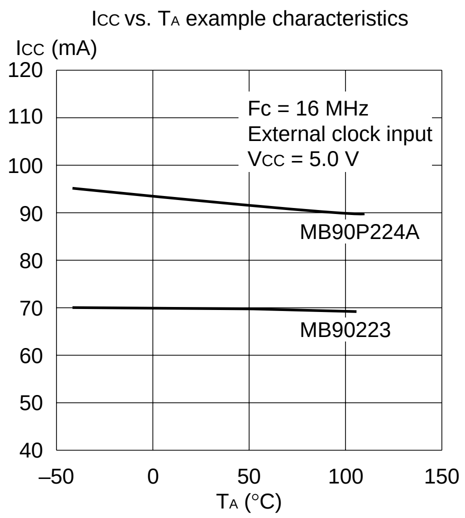
Linearity error $= \dfrac{V_{NT} - (N \times 1\text{ LSB} + V_{0T})}{1\text{ LSB}}$ $\quad$ N = 0 to 1022, $V_{NT\,(N=0)} = V_{0T}$, $V_{NT\,(N=1022)} = V_{FST}$

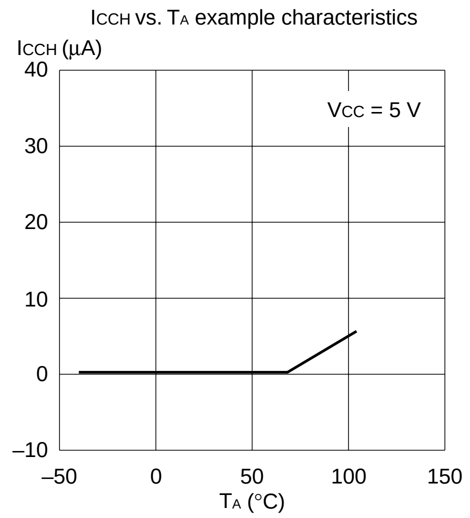
Differential linearity error $= \dfrac{V_{NT} - V_{(N-1)T}}{1\text{ LSB}} - 1$ $\quad$ N = 1 to 1022

Total error $= \dfrac{V_{NT} - \{(N + 0.5) \times 1\text{ LSB theoretical value}\}}{1\text{ LSB theoretical value}}$ $\quad$ N = 0 to 1022

■ EXAMPLE CHARACTERISTICS

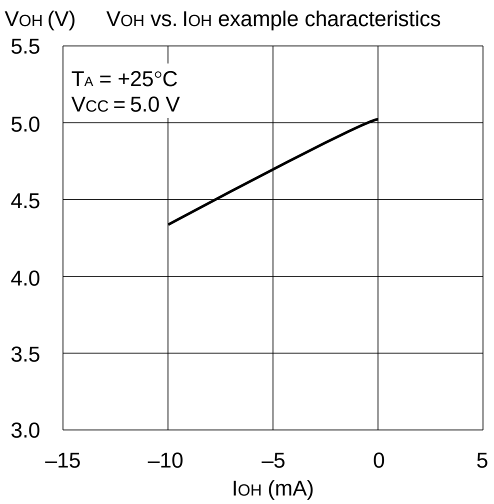
(1) Power Supply Current

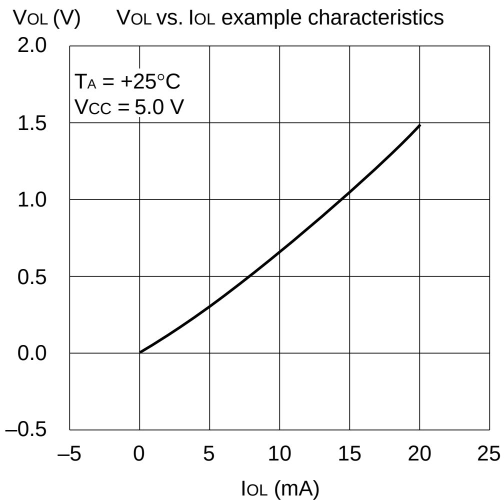




Note: These are not assured value of characteristics but example characteristics.

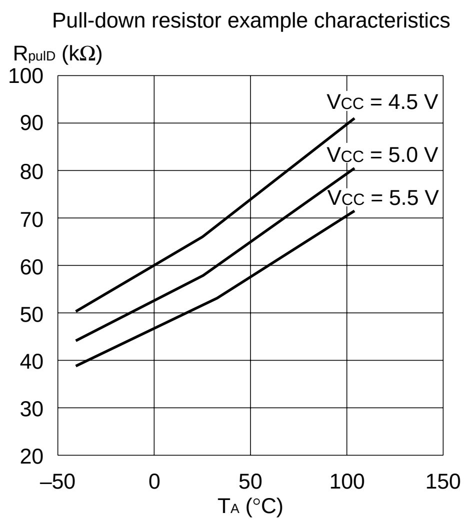
(2) Output Voltage

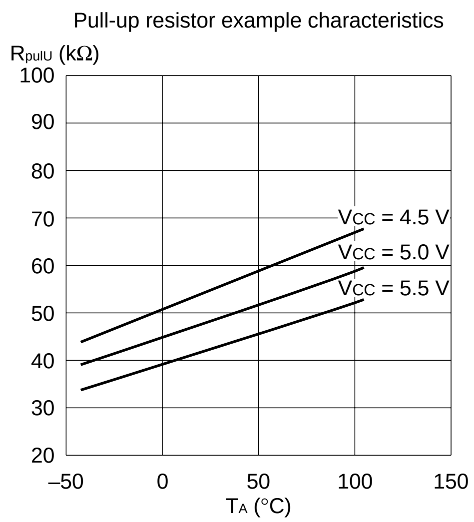




Note: These are not assured value of characteristics but example characteristics.

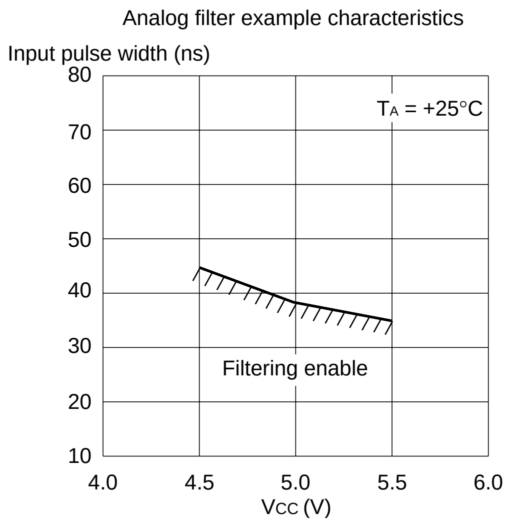
(3) Pull-up/Pull-down Resistor





Note: These are not assured value of characteristics but example characteristics.

(4) Analog Filter



Note: These are not assured value of characteristics but example characteristics.

■ INSTRUCTION SET (412 INSTRUCTIONS)

Table 1 Explanation of Items in Table of Instructions

Item	Explanation
Mnemonic	Upper-case letters and symbols: Represented as they appear in assembler Lower-case letters: Replaced when described in assembler. Numbers after lower-case letters: Indicate the bit width within the instruction.
#	Indicates the number of bytes.
~	Indicates the number of cycles. See Table 4 for details about meanings of letters in items.
B	Indicates the correction value for calculating the number of actual cycles during execution of instruction. The number of actual cycles during execution of instruction is summed with the value in the “cycles” column.
Operation	Indicates operation of instruction.
LH	Indicates special operations involving the bits 15 through 08 of the accumulator. Z: Transfers “0”. X: Extends before transferring. —: Transfers nothing.
AH	Indicates special operations involving the high-order 16 bits in the accumulator. *: Transfers from AL to AH. —: No transfer. Z: Transfers 00_H to AH. X: Transfers 00_H or FF_H to AH by extending AL.
I	Indicates the status of each of the following flags: I (interrupt enable), S (stack), T (sticky bit), N (negative), Z (zero), V (overflow), and C (carry). *: Changes due to execution of instruction. —: No change. S: Set by execution of instruction. R: Reset by execution of instruction.
S	
T	
N	
Z	
V	
C	
RMW	Indicates whether the instruction is a read-modify-write instruction (a single instruction that reads data from memory, etc., processes the data, and then writes the result to memory.). *: Instruction is a read-modify-write instruction —: Instruction is not a read-modify-write instruction Note: Cannot be used for addresses that have different meanings depending on whether they are read or written.

Table 2 Explanation of Symbols in Table of Instructions

Symbol	Explanation
A	32-bit accumulator The number of bits used varies according to the instruction. Byte: Low order 8 bits of AL Word: 16 bits of AL Long: 32 bits of AL, AH
AH	High-order 16 bits of A
AL	Low-order 16 bits of A
SP	Stack pointer (USP or SSP)
PC	Program counter
SPCU	Stack pointer upper limit register
SPCL	Stack pointer lower limit register
PCB	Program bank register
DTB	Data bank register
ADB	Additional data bank register
SSB	System stack bank register
USB	User stack bank register
SPB	Current stack bank register (SSB or USB)
DPR	Direct page register
brg1	DTB, ADB, SSB, USB, DPR, PCB, SPB
brg2	DTB, ADB, SSB, USB, DPR, SPB
Ri	R0, R1, R2, R3, R4, R5, R6, R7
RWi	RW0, RW1, RW2, RW3, RW4, RW5, RW6, RW7
RWj	RW0, RW1, RW2, RW3
RLi	RL0, RL1, RL2, RL3
dir addr16 addr24 addr24 0 to 15 addr24 16 to 23	Compact direct addressing Direct addressing Physical direct addressing Bits 0 to 15 of addr24 Bits 16 to 23 of addr24
io	I/O area (000000_H to $0000FF_H$)

(Continued)

(Continued)

Symbol	Explanation
#imm4 #imm8 #imm16 #imm32 ext (imm8)	4-bit immediate data 8-bit immediate data 16-bit immediate data 32-bit immediate data 16-bit data signed and extended from 8-bit immediate data
disp8 disp16	8-bit displacement 16-bit displacement
bp	Bit offset value
vct4 vct8	Vector number (0 to 15) Vector number (0 to 255)
( )b	Bit address
rel ear eam	Branch specification relative to PC Effective addressing (codes 00 to 07) Effective addressing (codes 08 to 1F)
rlst	Register list

Table 3 Effective Address Fields

Code	Notation			Address format	Number of bytes in address extemsion*
00 01 02 03 04 05 06 07	R0 R1 R2 R3 R4 R5 R6 R7	RW0 RW1 RW2 RW3 RW4 RW5 RW6 RW7	RL0 (RL0) RL1 (RL1) RL2 (RL2) RL3 (RL3)	Register direct "ea" corresponds to byte, word, and long-word types, starting from the left	—
08 09 0A 0B	@RW0 @RW1 @RW2 @RW3			Register indirect	0
0C 0D 0E 0F	@RW0 + @RW1 + @RW2 + @RW3 +			Register indirect with post-increment	0
10 11 12 13 14 15 16 17	@RW0 + disp8 @RW1 + disp8 @RW2 + disp8 @RW3 + disp8 @RW4 + disp8 @RW5 + disp8 @RW6 + disp8 @RW7 + disp8			Register indirect with 8-bit displacement	1
18 19 1A 1B	@RW0 + disp16 @RW1 + disp16 @RW2 + disp16 @RW3 + disp16			Register indirect with 16-bit displacemen	2
1C 1D 1E 1F	@RW0 + RW7 @RW1 + RW7 @PC + dip16 addr16			Register indirect with index Register indirect with index PC indirect with 16-bit displacement Direct address	0 0 2 2

* : The number of bytes for address extension is indicated by the "+" symbol in the "#" (number of bytes) column in the Table of Instructions.

Table 4 Number of Execution Cycles for Each Form of Addressing

Code	Operand	(a)* Number of execution cycles for each from of addressing
00 to 07	Ri RWi RLi	Listed in Table of Instructions
08 to 0B	@RWj	1
0C to 0F	@RWj +	4
10 to 17	@RWi + disp8	1
18 to 1B	@RWj + disp16	1
1C 1D 1E 1F	@RW0 + RW7 @RW1 + RW7 @PC + dip16 @addr16	2 2 2 1

* : "(a)" is used in the "cycles" (number of cycles) column and column B (correction value) in the Table of Instructions.

Table 5 Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles

Operand	(b)* byte	(c)* word	(d)* long
Internal register	+ 0	+ 0	+ 0
Internal RAM even address	+ 0	+ 0	+ 0
Internal RAM odd address	+ 0	+ 1	+ 2
Even address not in internal RAM	+ 1	+ 1	+ 2
Odd address not in internal RAM	+ 1	+ 3	+ 6
External data bus (8 bits)	+ 1	+ 3	+ 6

* : "(b)", "(c)", and "(d)" are used in the "cycles" (number of cycles) column and column B (correction value) in the Table of Instructions.

Table 6 Transfer Instructions (Byte) [50 Instructions]

Mnemonic	#	cycles	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
MOV A, dir	2	2	(b)	byte (A) ← (dir)	Z	*	–	–	–	*	*	–	–	–
MOV A, addr16	3	2	(b)	byte (A) ← (addr16)	Z	*	–	–	–	*	*	–	–	–
MOV A, Ri	1	1	0	byte (A) ← (Ri)	Z	*	–	–	–	*	*	–	–	–
MOV A, ear	2	1	0	byte (A) ← (ear)	Z	*	–	–	–	*	*	–	–	–
MOV A, eam	2+	2+ (a)	(b)	byte (A) ← (eam)	Z	*	–	–	–	*	*	–	–	–
MOV A, io	2	2	(b)	byte (A) ← (io)	Z	*	–	–	–	*	*	–	–	–
MOV A, #imm8	2	2	0	byte (A) ← imm8	Z	*	–	–	–	*	*	–	–	–
MOV A, @A	2	2	(b)	byte (A) ← ((A))	Z	–	–	–	–	*	*	–	–	–
MOV A, @RLi+disp8	3	6	(b)	byte (A) ← ((RLi))+disp8)	Z	*	–	–	–	*	*	–	–	–
MOV A, @SP+disp8	3	3	(b)	byte (A) ← ((SP)+disp8)	Z	*	–	–	–	*	*	–	–	–
MOVP A, addr24	5	3	(b)	byte (A) ←(addr24)	Z	*	–	–	–	*	*	–	–	–
MOVP A, @A	2	2	(b)	byte (A) ← ((A))	Z	–	–	–	–	*	*	–	–	–
MOVN A, #imm4	1	1	0	byte (A) ← imm4	Z	*	–	–	–	R	*	–	–	–
MOVX A, dir	2	2	(b)	byte (A) ← (dir)	X	*	–	–	–	*	*	–	–	–
MOVX A, addr16	3	2	(b)	byte (A) ← (addr16)	X	*	–	–	–	*	*	–	–	–
MOVX A, Ri	2	1	0	byte (A) ← (Ri)	X	*	–	–	–	*	*	–	–	–
MOVX A, ear	2	1	0	byte (A) ← (ear)	X	*	–	–	–	*	*	–	–	–
MOVX A, eam	2+	2+ (a)	(b)	byte (A) ← (eam)	X	*	–	–	–	*	*	–	–	–
MOVX A, io	2	2	(b)	byte (A) ← (io)	X	*	–	–	–	*	*	–	–	–
MOVX A, #imm8	2	2	0	byte (A) ← imm8	X	*	–	–	–	*	*	–	–	–
MOVX A, @A	2	2	(b)	byte (A) ← ((A))	X	–	–	–	–	*	*	–	–	–
MOVX A,@RWi+disp8	2	3	(b)	byte (A) ← ((RWi))+disp8)	X	*	–	–	–	*	*	–	–	–
MOVX A, @RLi+disp8	3	6	(b)	byte (A) ← ((RLi))+disp8)	X	*	–	–	–	*	*	–	–	–
MOVX A, @SP+disp8	3	3	(b)	byte (A) ← ((SP)+disp8)	X	*	–	–	–	*	*	–	–	–
MOVPX A, addr24	5	3	(b)	byte (A) ←(addr24)	X	*	–	–	–	*	*	–	–	–
MOVPX A, @A	2	2	(b)	byte (A) ← ((A))	X	–	–	–	–	*	*	–	–	–
MOV dir, A	2	2	(b)	byte (dir) ← (A)	–	–	–	–	–	*	*	–	–	–
MOV addr16, A	3	2	(b)	byte (addr16) ← (A)	–	–	–	–	–	*	*	–	–	–
MOV Ri, A	1	1	0	byte (Ri) ← (A)	–	–	–	–	–	*	*	–	–	–
MOV ear, A	2	2	0	byte (ear) ← (A)	–	–	–	–	–	*	*	–	–	–
MOV eam, A	2+	2+ (a)	(b)	byte (eam) ← (A)	–	–	–	–	–	*	*	–	–	–
MOV io, A	2	2	(b)	byte (io) ← (A)	–	–	–	–	–	*	*	–	–	–
MOV @RLi+disp8, A	3	6	(b)	byte ((RLi)) +disp8) ← (A)	–	–	–	–	–	*	*	–	–	–
MOV @SP+disp8, A	3	3	(b)	byte ((SP)+disp8) ← (A)	–	–	–	–	–	*	*	–	–	–
MOVP addr24, A	5	3	(b)	byte (addr24) ← (A)	–	–	–	–	–	*	*	–	–	–
MOV Ri, ear	2	2	0	byte (Ri) ← (ear)	–	–	–	–	–	*	*	–	–	–
MOV Ri, eam	2+	3+ (a)	(b)	byte (Ri) ← (eam)	–	–	–	–	–	*	*	–	–	–
MOVP @A, Ri	2	3	(b)	byte ((A)) ← (Ri)	–	–	–	–	–	*	*	–	–	–
MOV ear, Ri	2	3	0	byte (ear) ← (Ri)	–	–	–	–	–	*	*	–	–	–
MOV eam, Ri	2+	3+ (a)	(b)	byte (eam) ← (Ri)	–	–	–	–	–	*	*	–	–	–
MOV Ri, #imm8	2	2	0	byte (Ri) ← imm8	–	–	–	–	–	*	*	–	–	–
MOV io, #imm8	3	3	(b)	byte (io) ← imm8	–	–	–	–	–	–	–	–	–	–
MOV dir, #imm8	3	3	(b)	byte (dir) ← imm8	–	–	–	–	–	–	–	–	–	–
MOV ear, #imm8	3	2	0	byte (ear) ← imm8	–	–	–	–	–	*	*	–	–	–
MOV eam, #imm8	3+	2+ (a)	(b)	byte (eam) ← imm8	–	–	–	–	–	–	–	–	–	–
MOV @AL, AH	2	2	(b)	byte ((A)) ← (AH)	–	–	–	–	–	*	*	–	–	–

(Continued)

(Continued)

Mnemonic	#	cycles	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
XCH A, ear	2	3	0	byte (A) ↔ (ear)	Z	–	–	–	–	–	–	–	–	–
XCH A, eam	2+	3+ (a)	2× (b)	byte (A) ↔ (eam)	Z	–	–	–	–	–	–	–	–	–
XCH Ri, ear	2	4	0	byte (Ri) ↔ (ear)	–	–	–	–	–	–	–	–	–	–
XCH Ri, eam	2+	5+ (a)	2× (b)	byte (Ri) ↔ (eam)	–	–	–	–	–	–	–	–	–	–

For an explanation of “(a)” and “(b)”, refer to Table 4, “Number of Execution Cycles for Each Form of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

Table 7 Transfer Instructions (Word) [40 Instructions]

Mnemonic	#	cycles	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
MOVW A, dir	2	2	(c)	word (A) ← (dir)	–	*	–	–	–	*	*	–	–	–
MOVW A, addr16	3	2	(c)	word (A) ← (addr16)	–	*	–	–	–	*	*	–	–	–
MOVW A, SP	1	2	0	word (A) ← (SP)	–	*	–	–	–	*	*	–	–	–
MOVW A, RWi	1	1	0	word (A) ← (RWi)	–	*	–	–	–	*	*	–	–	–
MOVW A, ear	2	1	0	word (A) ← (ear)	–	*	–	–	–	*	*	–	–	–
MOVW A, eam	2+	2+ (a)	(c)	word (A) ← (eam)	–	*	–	–	–	*	*	–	–	–
MOVW A, io	2	2	(c)	word (A) ← (io)	–	*	–	–	–	*	*	–	–	–
MOVW A, @A	2	2	(c)	word (A) ← ((A))	–	–	–	–	–	*	*	–	–	–
MOVW A, #imm16	3	2	0	word (A) ← imm16	–	*	–	–	–	*	*	–	–	–
MOVW A, @RWi+disp8	2	3	(c)	word (A) ← ((RWi) +disp8)	–	*	–	–	–	*	*	–	–	–
MOVW A, @RLi+disp8	3	6	(c)	word (A) ← ((RLi) +disp8)	–	*	–	–	–	*	*	–	–	–
MOVW A, @SP+disp8	3	3	(c)	word (A) ← ((SP) +disp8)	–	*	–	–	–	*	*	–	–	–
MOVPW A, addr24	5	3	(c)	word (A) ← (addr24)	–	*	–	–	–	*	*	–	–	–
MOVPW A, @A	2	2	(c)	word (A) ← ((A))	–	–	–	–	–	*	*	–	–	–
MOVW dir, A	2	2	(c)	word (dir) ← (A)	–	–	–	–	–	*	*	–	–	–
MOVW addr16, A	3	2	(c)	word (addr16) ← (A)	–	–	–	–	–	*	*	–	–	–
MOVW SP, # imm16	4	2	0	word (SP) ← imm16	–	–	–	–	–	*	*	–	–	–
MOVW SP, A	1	2	0	word (SP) ← (A)	–	–	–	–	–	*	*	–	–	–
MOVW RWi, A	1	1	0	word (RWi) ← (A)	–	–	–	–	–	*	*	–	–	–
MOVW ear, A	2	2	0	word (ear) ← (A)	–	–	–	–	–	*	*	–	–	–
MOVW eam, A	2+	2+ (a)	(c)	word (eam) ← (A)	–	–	–	–	–	*	*	–	–	–
MOVW io, A	2	2	(c)	word (io) ← (A)	–	–	–	–	–	*	*	–	–	–
MOVW @RWi+disp8, A	2	3	(c)	word ((RWi) +disp8) ← (A)	–	–	–	–	–	*	*	–	–	–
MOVW @RLi+disp8, A	3	6	(c)	word ((RLi) +disp8) ← (A)	–	–	–	–	–	*	*	–	–	–
MOVW @SP+disp8, A	3	3	(c)	word ((SP) +disp8) ← (A)	–	–	–	–	–	*	*	–	–	–
MOVPW addr24, A	5	3	(c)	word (addr24) ← (A)	–	–	–	–	–	*	*	–	–	–
MOVPW @A, RWi	2	3	(c)	word ((A)) ← (RWi)	–	–	–	–	–	*	*	–	–	–
MOVW RWi, ear	2	2	0	word (RWi) ← (ear)	–	–	–	–	–	*	*	–	–	–
MOVW RWi, eam	2+	3+ (a)	(c)	word (RWi) ← (eam)	–	–	–	–	–	*	*	–	–	–
MOVW ear, RWi	2	3	0	word (ear) ← (RWi)	–	–	–	–	–	*	*	–	–	–
MOVW eam, RWi	2+	3+ (a)	(c)	word (eam) ← (RWi)	–	–	–	–	–	*	*	–	–	–
MOVW RWi, #imm16	3	2	0	word (RWi) ← imm16	–	–	–	–	–	*	*	–	–	–
MOVW io, #imm16	4	3	(c)	word (io) ← imm16	–	–	–	–	–	–	–	–	–	–
MOVW ear, #imm16	4	2	0	word (ear) ← imm16	–	–	–	–	–	*	*	–	–	–
MOVW eam, #imm16	4+	2+ (a)	(c)	word (eam) ← imm16	–	–	–	–	–	–	–	–	–	–
MOVW @AL, AH	2	2	(c)	word ((A)) ← (AH)	–	–	–	–	–	*	*	–	–	–
XCHW A, ear	2	3	0	word (A) ↔ (ear)	–	–	–	–	–	–	–	–	–	–
XCHW A, eam	2+	3+ (a)	2× (c)	word (A) ↔ (eam)	–	–	–	–	–	–	–	–	–	–
XCHW RWi, ear	2	4	0	word (RWi) ↔ (ear)	–	–	–	–	–	–	–	–	–	–
XCHW RWi, eam	2+	5+ (a)	2× (c)	word (RWi) ↔ (eam)	–	–	–	–	–	–	–	–	–	–

Note: For an explanation of “(a)” and “(c)”, refer to Table 4, “Number of Execution Cycles for Each Form of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

Table 8 Transfer Instructions (Long Word) [11 Instructions]

Mnemonic	#	cycles	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
MOVL A, ear	2	1	0	long (A) ← (ear)	–	–	–	–	–	*	*	–	–	–
MOVL A, eam	2+	3+ (a)	(d)	long (A) ← (eam)	–	–	–	–	–	*	*	–	–	–
MOVL A, # imm32	5	3	0	long (A) ← imm32	–	–	–	–	–	*	*	–	–	–
MOVL A, @SP + disp8	3	4	(d)	long (A) ← ((SP) +disp8)	–	–	–	–	–	*	*	–	–	–
MOVPL A, addr24	5	4	(d)	long (A) ← (addr24)	–	–	–	–	–	*	*	–	–	–
MOVPL A, @A	2	3	(d)	long (A) ← ((A))	–	–	–	–	–	*	*	–	–	–
MOVPL @A, RLi	2	5	(d)	long ((A)) ← (RLi)	–	–	–	–	–	*	*	–	–	–
MOVL @SP + disp8, A	3	4	(d)	long ((SP) + disp8) ← (A)	–	–	–	–	–	*	*	–	–	–
MOVPL addr24, A	5	4	(d)	long (addr24) ← (A)	–	–	–	–	–	*	*	–	–	–
MOVL ear, A	2	2	0	long (ear) ← (A)	–	–	–	–	–	*	*	–	–	–
MOVL eam, A	2+	3+ (a)	(d)	long (eam) ← (A)	–	–	–	–	–	*	*	–	–	–

For an explanation of “(a)” and “(d)”, refer to Table 4, “Number of Execution Cycles for Each Form of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

Table 9 Addition and Subtraction Instructions (Byte/Word/Long Word) [42 Instructions]

Mnemonic	#	cycles	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
ADD A, #imm8	2	2	0	byte (A) ← (A) +imm8	Z	–	–	–	–	*	*	*	*	–
ADD A, dir	2	3	(b)	byte (A) ← (A) +(dir)	Z	–	–	–	–	*	*	*	*	–
ADD A, ear	2	2	0	byte (A) ← (A) +(ear)	Z	–	–	–	–	*	*	*	*	–
ADD A, eam	2+	3+ (a)	(b)	byte (A) ← (A) +(eam)	Z	–	–	–	–	*	*	*	*	–
ADD ear, A	2	2	0	byte (ear) ← (ear) + (A)	–	–	–	–	–	*	*	*	*	*
ADD eam, A	2+	3+ (a)	2× (b)	byte (eam) ← (eam) + (A)	Z	–	–	–	–	*	*	*	*	*
ADDC A	1	2	0	byte (A) ← (AH) + (AL) + (C)	Z	–	–	–	–	*	*	*	*	–
ADDC A, ear	2	2	0	byte (A) ← (A) + (ear) + (C)	Z	–	–	–	–	*	*	*	*	–
ADDC A, eam	2+	3+ (a)	(b)	byte (A) ← (A) + (eam) + (C)	Z	–	–	–	–	*	*	*	*	–
ADDDC A	1	3	0	byte (A) ← (AH) + (AL) + (C) (Decimal)	Z	–	–	–	–	*	*	*	*	–
SUB A, #imm8	2	2	0	byte (A) ← (A) –imm8	Z	–	–	–	–	*	*	*	*	–
SUB A, dir	2	3	(b)	byte (A) ← (A) – (dir)	Z	–	–	–	–	*	*	*	*	–
SUB A, ear	2	2	0	byte (A) ← (A) – (ear)	Z	–	–	–	–	*	*	*	*	–
SUB A, eam	2+	3+ (a)	(b)	byte (A) ← (A) – (eam)	Z	–	–	–	–	*	*	*	*	–
SUB ear, A	2	2	0	byte (ear) ← (ear) – (A)	–	–	–	–	–	*	*	*	*	*
SUB eam, A	2+	3+ (a)	2× (b)	byte (eam) ← (eam) – (A)	–	–	–	–	–	*	*	*	*	*
SUBC A	1	2	0	byte (A) ← (AH) – (AL) – (C)	Z	–	–	–	–	*	*	*	*	–
SUBC A, ear	2	2	0	byte (A) ← (A) – (ear) – (C)	Z	–	–	–	–	*	*	*	*	–
SUBC A, eam	2+	3+ (a)	(b)	byte (A) ← (A) – (eam) – (C)	Z	–	–	–	–	*	*	*	*	–
SUBDC A	1	3	0	byte (A) ← (AH) – (AL) – (C) (Decimal)	Z	–	–	–	–	*	*	*	*	–
ADDW A	1	2	0	word (A) ← (AH) + (AL)	–	–	–	–	–	*	*	*	*	–
ADDW A, ear	2	2	0	word (A) ← (A) +(ear)	–	–	–	–	–	*	*	*	*	–
ADDW A, eam	2+	3+ (a)	(c)	word (A) ← (A) +(eam)	–	–	–	–	–	*	*	*	*	–
ADDW A, #imm16	3	2	0	word (A) ← (A) +imm16	–	–	–	–	–	*	*	*	*	–
ADDW ear, A	2	2	0	word (ear) ← (ear) + (A)	–	–	–	–	–	*	*	*	*	*
ADDW eam, A	2+	3+ (a)	2× (c)	word (eam) ← (eam) + (A)	–	–	–	–	–	*	*	*	*	*
ADDCW A, ear	2	2	0	word (A) ← (A) + (ear) + (C)	–	–	–	–	–	*	*	*	*	–
ADDCW A, eam	2+	3+ (a)	(c)	word (A) ← (A) + (eam) + (C)	–	–	–	–	–	*	*	*	*	–
SUBW A	1	2	0	word (A) ← (AH) – (AL)	–	–	–	–	–	*	*	*	*	–
SUBW A, ear	2	2	0	word (A) ← (A) – (ear)	–	–	–	–	–	*	*	*	*	–
SUBW A, eam	2+	3+ (a)	(c)	word (A) ← (A) – (eam)	–	–	–	–	–	*	*	*	*	–
SUBW A, #imm16	3	2	0	word (A) ← (A) –imm16	–	–	–	–	–	*	*	*	*	–
SUBW ear, A	2	2	0	word (ear) ← (ear) – (A)	–	–	–	–	–	*	*	*	*	*
SUBW eam, A	2+	3+ (a)	2× (c)	word (eam) ← (eam) – (A)	–	–	–	–	–	*	*	*	*	*
SUBCW A, ear	2	2	0	word (A) ← (A) – (ear) – (C)	–	–	–	–	–	*	*	*	*	–
SUBCW A, eam	2+	3+ (a)	(c)	word (A) ← (A) – (eam) – (C)	–	–	–	–	–	*	*	*	*	–
ADDL A, ear	2	5	0	long (A) ← (A) + (ear)	–	–	–	–	–	*	*	*	*	–
ADDL A, eam	2+	6+ (a)	(d)	long (A) ← (A) + (eam)	–	–	–	–	–	*	*	*	*	–
ADDL A, #imm32	5	4	0	long (A) ← (A) +imm32	–	–	–	–	–	*	*	*	*	–
SUBL A, ear	2	5	0	long (A) ← (A) – (ear)	–	–	–	–	–	*	*	*	*	–
SUBL A, eam	2+	6+ (a)	(d)	long (A) ← (A) – (eam)	–	–	–	–	–	*	*	*	*	–
SUBL A, #imm32	5	4	0	long (A) ← (A) –imm32	–	–	–	–	–	*	*	*	*	–

For an explanation of “(a)”, “(b)”, “(c)” and “(d)”, refer to Table 4, “Number of Execution Cycles for Each Form of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

Table 10 Increment and Decrement Instructions (Byte/Word/Long Word) [12 Instructions]

Mnemonic	#	cycles	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
INC ear	2	2	0	byte (ear) ← (ear) +1	–	–	–	–	–	*	*	*	–	*
INC eam	2+	3+ (a)	2× (b)	byte (eam) ← (eam) +1	–	–	–	–	–	*	*	*	–	*
DEC ear	2	2	0	byte (ear) ← (ear) –1	–	–	–	–	–	*	*	*	–	*
DEC eam	2+	3+ (a)	2× (b)	byte (eam) ← (eam) –1	–	–	–	–	–	*	*	*	–	*
INCW ear	2	2	0	word (ear) ← (ear) +1	–	–	–	–	–	*	*	*	–	*
INCW eam	2+	3+ (a)	2× (c)	word (eam) ← (eam) +1	–	–	–	–	–	*	*	*	–	*
DECW ear	2	2	0	word (ear) ← (ear) –1	–	–	–	–	–	*	*	*	–	*
DECW eam	2+	3+ (a)	2× (c)	word (eam) ← (eam) –1	–	–	–	–	–	*	*	*	–	*
INCL ear	2	4	0	long (ear) ← (ear) +1	–	–	–	–	–	*	*	*	–	*
INCL eam	2+	5+ (a)	2× (d)	long (eam) ← (eam) +1	–	–	–	–	–	*	*	*	–	*
DECL ear	2	4	0	long (ear) ← (ear) –1	–	–	–	–	–	*	*	*	–	*
DECL eam	2+	5+ (a)	2× (d)	long (eam) ← (eam) –1	–	–	–	–	–	*	*	*	–	*

For an explanation of “(a)”, “(b)”, “(c)” and “(d)”, refer to Table 4, “Number of Execution Cycles for Each Form of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

Table 11 Compare Instructions (Byte/Word/Long Word) [11 Instructions]

Mnemonic	#	cycles	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
CMP A	1	2	0	byte (AH) – (AL)	–	–	–	–	–	*	*	*	*	–
CMP A, ear	2	2	0	byte (A) – (ear)	–	–	–	–	–	*	*	*	*	–
CMP A, eam	2+	2+ (a)	(b)	byte (A) – (eam)	–	–	–	–	–	*	*	*	*	–
CMP A, #imm8	2	2	0	byte (A) – imm8	–	–	–	–	–	*	*	*	*	–
CMPW A	1	2	0	word (AH) – (AL)	–	–	–	–	–	*	*	*	*	–
CMPW A, ear	2	2	0	word (A) – (ear)	–	–	–	–	–	*	*	*	*	–
CMPW A, eam	2+	2+ (a)	(c)	word (A) – (eam)	–	–	–	–	–	*	*	*	*	–
CMPW A, #imm16	3	2	0	word (A) – imm16	–	–	–	–	–	*	*	*	*	–
CMPL A, ear	2	3	0	long (A) – (ear)	–	–	–	–	–	*	*	*	*	–
CMPL A, eam	2+	4+ (a)	(d)	long (A) – (eam)	–	–	–	–	–	*	*	*	*	–
CMPL A, #imm32	5	3	0	long (A) – imm32	–	–	–	–	–	*	*	*	*	–

For an explanation of “(a)”, “(b)”, “(c)” and “(d)”, refer to Table 4, “Number of Execution Cycles for Each Form of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

Table 12 Unsigned Multiplication and Division Instructions (Word/Long Word) [11 Instructions]

Mnemonic	#	cycles	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
DIVU A	1	*1	0	word (AH) /byte (AL) Quotient → byte (AL) Remainder → byte (AH)	–	–	–	–	–	–	–	*	*	–
DIVU A, ear	2	*2	0	word (A)/byte (ear) Quotient → byte (A) Remainder → byte (ear)	–	–	–	–	–	–	–	*	*	–
DIVU A, eam	2+	*3	*6	word (A)/byte (eam) Quotient → byte (A) Remainder → byte (eam)	–	–	–	–	–	–	–	*	*	–
DIVUW A, ear	2	*4	0	long (A)/word (ear) Quotient → word (A) Remainder → word (ear)	–	–	–	–	–	–	–	*	*	–
DIVUW A, eam	2+	*5	*7	long (A)/word (eam) Quotient → word (A) Remainder → word (eam)	–	–	–	–	–	–	–	*	*	–
MULU A	1	*8	0	byte (AH) × byte (AL) → word (A)	–	–	–	–	–	–	–	–	–	–
MULU A, ear	2	*9	0	byte (A) × byte (ear) → word (A)	–	–	–	–	–	–	–	–	–	–
MULU A, eam	2+	*10	(b)	byte (A) × byte (eam) → word (A)	–	–	–	–	–	–	–	–	–	–
MULUW A	1	*11	0	word (AH) × word (AL) → long (A)	–	–	–	–	–	–	–	–	–	–
MULUW A, ear	2	*12	0	word (A) × word (ear) → long (A)	–	–	–	–	–	–	–	–	–	–
MULUW A, eam	2+	*13	(c)	word (A) × word (eam) → long (A)	–	–	–	–	–	–	–	–	–	–

For an explanation of "(b)" and "(c), refer to Table 5, "Correction Values for Number of Cycle Used to Calculate Number of Actual Cycles."

*1: 3 when dividing into zero, 6 when an overflow occurs, and 14 normally.
*2: 3 when dividing into zero, 5 when an overflow occurs, and 13 normally.
*3: 5 + (a) when dividing into zero, 7 + (a) when an overflow occurs, and 17 + (a) normally.
*4: 3 when dividing into zero, 5 when an overflow occurs, and 21 normally.
*5: 4 + (a) when dividing into zero, 7 + (a) when an overflow occurs, and 25 + (a) normally.
*6: (b) when dividing into zero or when an overflow occurs, and 2 × (b) normally.
*7: (c) when dividing into zero or when an overflow occurs, and 2 × (c) normally.
*8: 3 when byte (AH) is zero, and 7 when byte (AH) is not 0.
*9: 3 when byte (ear) is zero, and 7 when byte (ear) is not 0.
*10: 4 + (a) when byte (eam) is zero, and 8 + (a) when byte (eam) is not 0.
*11: 3 when word (AH) is zero, and 11 when word (AH) is not 0.
*12: 3 when word (ear) is zero, and 11 when word (ear) is not 0.
*13: 4 + (a) when word (eam) is zero, and 12 + (a) when word (eam) is not 0.

Table 13 Signed Multiplication and Division Instructions (Word/Long Word) [11 Insturctions]

Mnemonic	#	cycles	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
DIV A	2	*1	0	word (AH) /byte (AL) Quotient → byte (AL) Remainder → byte (AH)	Z	–	–	–	–	–	–	*	*	–
DIV A, ear	2	*2	0	word (A)/byte (ear) Quotient → byte (A) Remainder → byte (ear)	Z	–	–	–	–	–	–	*	*	–
DIV A, eam	2+	*3	*6	word (A)/byte (eam) Quotient → byte (A) Remainder → byte (eam)	Z	–	–	–	–	–	–	*	*	–
DIVW A, ear	2	*4	0	long (A)/word (ear) Quotient → word (A) Remainder → word (ear)	–	–	–	–	–	–	–	*	*	–
DIVW A, eam	2+	*5	*7	long (A)/word (eam) Quotient → word (A) Remainder → word (eam)	–	–	–	–	–	–	–	*	*	–
MUL A	2	*8	0	byte (AH) × byte (AL) → word (A)	–	–	–	–	–	–	–	–	–	–
MUL A, ear	2	*9	0	byte (A) × byte (ear) → word (A)	–	–	–	–	–	–	–	–	–	–
MUL A, eam	2+	*10	(b)	byte (A) × byte (eam) → word (A)	–	–	–	–	–	–	–	–	–	–
MULW A	2	*11	0	word (AH) × word (AL) → long (A)	–	–	–	–	–	–	–	–	–	–
MULW A, ear	2	*12	0	word (A) × word (ear) → long (A)	–	–	–	–	–	–	–	–	–	–
MULW A, eam	2+	*13	(b)	word (A) × word (eam) → long (A)	–	–	–	–	–	–	–	–	–	–

For an explanation of "(b)" and "(c)", refer to Table 5, "Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles."

*1: 3 when dividing into zero, 8 or 18 when an overflow occurs, and 18 normally.
*2: 3 when dividing into zero, 10 or 21 when an overflow occurs, and 22 normally.
*3: 4 + (a) when dividing into zero, 11 + (a) or 22 + (a) when an overflow occurs, and 23 + (a) normally.
*4: When the dividend is positive: 4 when dividing into zero, 10 or 29 when an overflow occurs, and 30 normally.
When the dividend is negative: 4 when dividing into zero, 11 or 30 when an overflow occurs, and 31 normally.
*5: When the dividend is positive: 4 + (a) when dividing into zero, 11 + (a) or 30 + (a) when an overflow occurs, and 31 + (a) normally.
When the dividend is negative: 4 + (a) when dividing into zero, 12 + (a) or 31 + (a) when an overflow occurs, and 32 + (a) normally.
*6: (b) when dividing into zero or when an overflow occurs, and 2 × (b) normally.
*7: (c) when dividing into zero or when an overflow occurs, and 2 × (c) normally.
*8: 3 when byte (AH) is zero, 12 when the result is positive, and 13 when the result is negative.
*9: 3 when byte (ear) is zero, 12 when the result is positive, and 13 when the result is negative.
*10: 4 + (a) when byte (eam) is zero, 13 + (a) when the result is positive, and 14 + (a) when the result is negative.
*11: 3 when word (AH) is zero, 12 when the result is positive, and 13 when the result is negative.
*12: 3 when word (ear) is zero, 16 when the result is positive, and 19 when the result is negative.
*13: 4 + (a) when word (eam) is zero, 17 + (a) when the result is positive, and 20 + (a) when the result is negative.

Note: Which of the two values given for the number of execution cycles applies when an overflow error occurs in a DIV or DIVW instruction depends on whether the overflow was detected before or after the operation.

Table 14 Logical 1 Instructions (Byte, Word) [39 Instructions]

Mnemonic		#	cycles	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
AND	A, #imm8	2	2	0	byte (A) ← (A) and imm8	–	–	–	–	–	*	*	R	–	–
AND	A, ear	2	2	0	byte (A) ← (A) and (ear)	–	–	–	–	–	*	*	R	–	–
AND	A, eam	2+	3+ (a)	(b)	byte (A) ← (A) and (eam)	–	–	–	–	–	*	*	R	–	–
AND	ear, A	2	3	0	byte (ear) ← (ear) and (A)	–	–	–	–	–	*	*	R	–	*
AND	eam, A	2+	3+ (a)	2× (b)	byte (eam) ← (eam) and (A)	–	–	–	–	–	*	*	R	–	*
OR	A, #imm8	2	2	0	byte (A) ← (A) or imm8	–	–	–	–	–	*	*	R	–	–
OR	A, ear	2	2	0	byte (A) ← (A) or (ear)	–	–	–	–	–	*	*	R	–	–
OR	A, eam	2+	3+ (a)	(b)	byte (A) ← (A) or (eam)	–	–	–	–	–	*	*	R	–	–
OR	ear, A	2	3	0	byte (ear) ← (ear) or (A)	–	–	–	–	–	*	*	R	–	*
OR	eam, A	2+	3+ (a)	2× (b)	byte (eam) ← (eam) or (A)	–	–	–	–	–	*	*	R	–	*
XOR	A, #imm8	2	2	0	byte (A) ← (A) xor imm8	–	–	–	–	–	*	*	R	–	–
XOR	A, ear	2	2	0	byte (A) ← (A) xor (ear)	–	–	–	–	–	*	*	R	–	–
XOR	A, eam	2+	3+ (a)	(b)	byte (A) ← (A) xor (eam)	–	–	–	–	–	*	*	R	–	–
XOR	ear, A	2	3	0	byte (ear) ← (ear) xor (A)	–	–	–	–	–	*	*	R	–	*
XOR	eam, A	2+	3+ (a)	2× (b)	byte (eam) ← (eam) xor (A)	–	–	–	–	–	*	*	R	–	*
NOT	A	1	2	0	byte (A) ← not (A)	–	–	–	–	–	*	*	R	–	–
NOT	ear	2	2	0	byte (ear) ← not (ear)	–	–	–	–	–	*	*	R	–	*
NOT	eam	2+	3+ (a)	2× (b)	byte (eam) ← not (eam)	–	–	–	–	–	*	*	R	–	*
ANDW	A	1	2	0	word (A) ← (AH) and (A)	–	–	–	–	–	*	*	R	–	–
ANDW	A, #imm16	3	2	0	word (A) ← (A) and imm16	–	–	–	–	–	*	*	R	–	–
ANDW	A, ear	2	2	0	word (A) ← (A) and (ear)	–	–	–	–	–	*	*	R	–	–
ANDW	A, eam	2+	3+ (a)	(c)	word (A) ← (A) and (eam)	–	–	–	–	–	*	*	R	–	–
ANDW	ear, A	2	3	0	word (ear) ← (ear) and (A)	–	–	–	–	–	*	*	R	–	*
ANDW	eam, A	2+	3+ (a)	2× (c)	word (eam) ← (eam) and (A)	–	–	–	–	–	*	*	R	–	*
ORW	A	1	2	0	word (A) ← (AH) or (A)	–	–	–	–	–	*	*	R	–	–
ORW	A, #imm16	3	2	0	word (A) ← (A) or imm16	–	–	–	–	–	*	*	R	–	–
ORW	A, ear	2	2	0	word (A) ← (A) or (ear)	–	–	–	–	–	*	*	R	–	–
ORW	A, eam	2+	3+ (a)	(c)	word (A) ← (A) or (eam)	–	–	–	–	–	*	*	R	–	–
ORW	ear, A	2	3	0	word (ear) ← (ear) or (A)	–	–	–	–	–	*	*	R	–	*
ORW	eam, A	2+	3+ (a)	2× (c)	word (eam) ← (eam) or (A)	–	–	–	–	–	*	*	R	–	*
XORW	A	1	2	0	word (A) ← (AH) xor (A)	–	–	–	–	–	*	*	R	–	–
XORW	A, #imm16	3	2	0	word (A) ← (A) xor imm16	–	–	–	–	–	*	*	R	–	–
XORW	A, ear	2	2	0	word (A) ← (A) xor (ear)	–	–	–	–	–	*	*	R	–	–
XORW	A, eam	2+	3+ (a)	(c)	word (A) ← (A) xor (eam)	–	–	–	–	–	*	*	R	–	–
XORW	ear, A	2	3	0	word (ear) ← (ear) xor (A)	–	–	–	–	–	*	*	R	–	*
XORW	eam, A	2+	3+ (a)	2× (c)	word (eam) ← (eam) xor (A)	–	–	–	–	–	*	*	R	–	*
NOTW	A	1	2	0	word (A) ← not (A)	–	–	–	–	–	*	*	R	–	–
NOTW	ear	2	2	0	word (ear) ← not (ear)	–	–	–	–	–	*	*	R	–	*
NOTW	eam	2+	3+ (a)	2× (c)	word (eam) ← not (eam)	–	–	–	–	–	*	*	R	–	*

For an explanation of “(a)”, “(b)”, “(c)” and “(d)”, refer to Table 4, “Number of Execution Cycles for Each Form of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

Table 15 Logical 2 Instructions (Long Word) [6 Instructions]

Mnemonic	#	cycles	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
ANDL A, ear	2	5	0	long (A) ← (A) and (ear)	–	–	–	–	–	*	*	R	–	–
ANDL A, eam	2+	6+ (a)	(d)	long (A) ← (A) and (eam)	–	–	–	–	–	*	*	R	–	–
ORL A, ear	2	5	0	long (A) ← (A) or (ear)	–	–	–	–	–	*	*	R	–	–
ORL A, eam	2+	6+ (a)	(d)	long (A) ← (A) or (eam)	–	–	–	–	–	*	*	R	–	–
XORL A, ear	2	5	0	long (A) ← (A) xor (ear)	–	–	–	–	–	*	*	R	–	–
XORL A, eam	2+	6+ (a)	(d)	long (A) ← (A) xor (eam)	–	–	–	–	–	*	*	R	–	–

For an explanation of “(a)” and “(d)”, refer to Table 4, “Number of Execution Cycles for Each Form of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

Table 16 Sign Inversion Instructions (Byte/Word) [6 Instructions]

Mnemonic	#	cycles	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
NEG A	1	2	0	byte (A) ← 0 – (A)	X	–	–	–	–	*	*	*	*	–
NEG ear	2	2	0	byte (ear) ← 0 – (ear)	–	–	–	–	–	*	*	*	*	*
NEG eam	2+	3+ (a)	2× (b)	byte (eam) ← 0 – (eam)	–	–	–	–	–	*	*	*	*	*
NEGW A	1	2	0	word (A) ← 0 – (A)	–	–	–	–	–	*	*	*	*	–
NEGW ear	2	2	0	word (ear) ← 0 – (ear)	–	–	–	–	–	*	*	*	*	*
NEGW eam	2+	3+ (a)	2× (c)	word (eam) ← 0 – (eam)	–	–	–	–	–	*	*	*	*	*

For an explanation of “(a)”, “(b)” and “(c)” and refer to Table 4, “Number of Execution Cycles for Each Form of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

Table 17 Absolute Value Instructions (Byte/Word/Long Word) [3 Insturctions]

Mnemonic	#	cycles	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
ABS A	2	2	0	byte (A) ← absolute value (A)	Z	–	–	–	–	*	*	*	–	–
ABSW A	2	2	0	word (A) ← absolute value (A)	–	–	–	–	–	*	*	*	–	–
ABSL A	2	4	0	long (A) ← absolute value (A)	–	–	–	–	–	*	*	*	–	–

Table 18 Normalize Instructions (Long Word) [1 Instruction]

Mnemonic	#	cycles	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
NRML A, R0	2	*	0	long (A) ← Shifts to the position at which “1” was set first byte (R0) ← current shift count	–	–	–	–	*	–	–	–	–	–

* : 5 when the contents of the accumulator are all zeroes, 5 + (R0) in all other cases.

Table 19 Shift Instructions (Byte/Word/Long Word) [27 Instructions]

Mnemonic	#	cycles	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
RORC A	2	2	0	byte (A) ← Right rotation with carry	–	–	–	–	–	*	*	–	*	–
ROLC A	2	2	0	byte (A) ← Left rotation with carry	–	–	–	–	–	*	*	–	*	–
RORC ear	2	2	0	byte (ear) ← Right rotation with carry	–	–	–	–	–	*	*	–	*	*
RORC eam	2+	3+ (a)	2× (b)	byte (eam) ← Right rotation with carry	–	–	–	–	–	*	*	–	*	*
ROLC ear	2	2	0	byte (ear) ← Left rotation with carry	–	–	–	–	–	*	*	–	*	*
ROLC eam	2+	3+ (a)	2× (b)	byte (eam) ← Left rotation with carry	–	–	–	–	–	*	*	–	*	*
ASR A, R0	2	*1	0	byte (A) ← Arithmetic right barrel shift (A, R0)	–	–	–	–	*	*	*	–	*	–
LSR A, R0	2	*1	0	byte (A) ← Logical right barrel shift (A, R0)	–	–	–	–	*	*	*	–	*	–
LSL A, R0	2	*1	0	byte (A) ← Logical left barrel shift (A, R0)	–	–	–	–	–	*	*	–	*	–
ASR A, #imm8	3	*3	0	byte (A) ← Arithmetic right barrel shift (A, imm8)	–	–	–	–	*	*	*	–	*	–
LSR A, #imm8	3	*3	0	byte (A) ← Logical right barrel shift (A, imm8)	–	–	–	–	*	*	*	–	*	–
LSL A, #imm8	3	*3	0	byte (A) ← Logical left barrel shift (A, imm8)	–	–	–	–	–	*	*	–	*	–
ASRW A	1	2	0	word (A) ← Arithmetic right shift (A, 1 bit)	–	–	–	–	*	*	*	–	*	–
LSRW A/SHRW A	1	2	0	word (A) ← Logical right shift (A, 1 bit)	–	–	–	–	*	R	*	–	*	–
LSLW A/SHLW A	1	2	0	word (A) ← Logical left shift (A, 1 bit)	–	–	–	–	–	*	*	–	*	–
ASRW A, R0	2	*1	0	word (A) ← Arithmetic right barrel shift (A, R0)	–	–	–	–	*	*	*	–	*	–
LSRW A, R0	2	*1	0	word (A) ← Logical right barrel shift (A, R0)	–	–	–	–	*	*	*	–	*	–
LSLW A, R0	2	*1	0	word (A) ← Logical left barrel shift (A, R0)	–	–	–	–	–	*	*	–	*	–
ASRW A, #imm8	3	*3	0	word (A) ← Arithmetic right barrel shift (A, imm8)	–	–	–	–	*	*	*	–	*	–
LSRW A, #imm8	3	*3	0	word (A) ← Logical right barrel shift (A, imm8)	–	–	–	–	*	*	*	–	*	–
LSLW A, #imm8	3	*3	0	word (A) ← Logical left barrel shift (A, imm8)	–	–	–	–	–	*	*	–	*	–
ASRL A, R0	2	*2	0	long (A) ← Arithmetic right shift (A, R0)	–	–	–	–	*	*	*	–	*	–
LSRL A, R0	2	*2	0	long (A) ← Logical right barrel shift (A, R0)	–	–	–	–	*	*	*	–	*	–
LSLL A, R0	2	*2	0	long (A) ← Logical left barrel shift (A, R0)	–	–	–	–	–	*	*	–	*	–
ASRL A, #imm8	3	*4	0	long (A) ← Arithmetic right shift (A, imm8)	–	–	–	–	*	*	*	–	*	–
LSRL A, #imm8	3	*4	0	long (A) ← Logical right barrel shift (A, imm8)	–	–	–	–	*	*	*	–	*	–
LSLL A, #imm8	3	*4	0	long (A) ← Logical left barrel shift (A, imm8)	–	–	–	–	–	*	*	–	*	–

For an explanation of “(a)” and “(b)”, refer to Table 4, “Number of Execution Cycles for Each Form of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

*1: 3 when R0 is 0, 3 + (R0) in all other cases.
*2: 3 when R0 is 0, 4 + (R0) in all other cases.
*3: 3 when imm8 is 0, 3 + (imm8) in all other cases.
*4: 3 when imm8 is 0, 4 + (imm8) in all other cases.

Table 20 Branch 1 Instructions [31 Instructions]

Mnemonic	#	cycles	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
BZ/BEQ rel	2	*1	0	Branch when (Z) = 1	–	–	–	–	–	–	–	–	–	–
BNZ/BNE rel	2	*1	0	Branch when (Z) = 0	–	–	–	–	–	–	–	–	–	–
BC/BLO rel	2	*1	0	Branch when (C) = 1	–	–	–	–	–	–	–	–	–	–
BNC/BHS rel	2	*1	0	Branch when (C) = 0	–	–	–	–	–	–	–	–	–	–
BN rel	2	*1	0	Branch when (N) = 1	–	–	–	–	–	–	–	–	–	–
BP rel	2	*1	0	Branch when (N) = 0	–	–	–	–	–	–	–	–	–	–
BV rel	2	*1	0	Branch when (V) = 1	–	–	–	–	–	–	–	–	–	–
BNV rel	2	*1	0	Branch when (V) = 0	–	–	–	–	–	–	–	–	–	–
BT rel	2	*1	0	Branch when (T) = 1	–	–	–	–	–	–	–	–	–	–
BNT rel	2	*1	0	Branch when (T) = 0	–	–	–	–	–	–	–	–	–	–
BLT rel	2	*1	0	Branch when (V) xor (N) = 1	–	–	–	–	–	–	–	–	–	–
BGE rel	2	*1	0	Branch when (V) xor (N) = 0	–	–	–	–	–	–	–	–	–	–
BLE rel	2	*1	0	((V) xor (N)) or (Z) = 1	–	–	–	–	–	–	–	–	–	–
BGT rel	2	*1	0	((V) xor (N)) or (Z) = 0	–	–	–	–	–	–	–	–	–	–
BLS rel	2	*1	0	Branch when (C) or (Z) = 1	–	–	–	–	–	–	–	–	–	–
BHI rel	2	*1	0	Branch when (C) or (Z) = 0	–	–	–	–	–	–	–	–	–	–
BRA rel	2	*1	0	Branch unconditionally	–	–	–	–	–	–	–	–	–	–
JMP @A	1	2	0	word (PC) ← (A)	–	–	–	–	–	–	–	–	–	–
JMP addr16	3	2	0	word (PC) ← addr16	–	–	–	–	–	–	–	–	–	–
JMP @ear	2	3	0	word (PC) ← (ear)	–	–	–	–	–	–	–	–	–	–
JMP @eam	2+	4+ (a)	(c)	word (PC) ← (eam)	–	–	–	–	–	–	–	–	–	–
JMPP @ear *3	2	3	0	word (PC) ← (ear), (PCB) ← (ear +2)	–	–	–	–	–	–	–	–	–	–
JMPP @eam *3	2+	4+ (a)	(d)	word (PC) ← (eam), (PCB) ← (eam +2)	–	–	–	–	–	–	–	–	–	–
JMPP addr24	4	3	0	word (PC) ← ad24 0 to 15 (PCB) ← ad24 16 to 23	–	–	–	–	–	–	–	–	–	–
CALL @ear *4	2	4	(c)	word (PC) ← (ear)	–	–	–	–	–	–	–	–	–	–
CALL @eam *4	2+	5+ (a)	2× (c)	word (PC) ← (eam)	–	–	–	–	–	–	–	–	–	–
CALL addr16 *5	3	5	(c)	word (PC) ← addr16	–	–	–	–	–	–	–	–	–	–
CALLV #vct4 *5	1	5	2× (c)	Vector call linstruction	–	–	–	–	–	–	–	–	–	–
CALLP @ear *6	2	7	2× (c)	word (PC) ← (ear) 0 to 15, (PCB) ← (ear) 16 to 23	–	–	–	–	–	–	–	–	–	–
CALLP @eam *6	2+	8+ (a)	*2	word (PC) ← (eam) 0 to 15, (PCB) ← (eam) 16 to 23	–	–	–	–	–	–	–	–	–	–
CALLP addr24 *7	4	7	2× (c)	word (PC) ← addr 0 to 15, (PCB) ← addr 16 to 23	–	–	–	–	–	–	–	–	–	–

For an explanation of “(a)”, “(c)” and “(d)”, refer to Table 4, “Number of Execution Cycles for Each Form of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

*1: 3 when branching, 2 when not branching.
*2: 3 × (c) + (b)
*3: Read (word) branch address.
*4: W: Save (word) to stack; R: Read (word) branch address.
*5: Save (word) to stack.
*6: W: Save (long word) to W stack; R: Read (long word) branch address.
*7: Save (long word) to stack.

Table 21 Branch 2 Instructions [20 Instructions]

Mnemonic	#	cycles	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
CBNE A, #imm8, rel	3	*1	0	Branch when byte (A) ≠ imm8	–	–	–	–	–	*	*	*	*	–
CWBNE A, #imm16, rel	4	*1	0	Branch when byte (A) ≠ imm16	–	–	–	–	–	*	*	*	*	–
CBNE ear, #imm8, rel	4	*1	0	Branch when byte (ear) ≠ imm8	–	–	–	–	–	*	*	*	*	–
CBNE eam, #imm8, rel	4+	*3	(b)	Branch when byte (eam) ≠ imm8	–	–	–	–	–	*	*	*	*	–
CWBNE ear, #imm16, rel	5	*1	0	Branch when word (ear) ≠ imm16	–	–	–	–	–	*	*	*	*	–
CWBNE eam, #imm16, rel	5+	*3	(c)	Branch when word (eam) ≠ imm16	–	–	–	–	–	*	*	*	*	–
DBNZ ear, rel	3	*2	0	Branch when byte (ear) = (ear) – 1, and (ear) ≠ 0	–	–	–	–	–	*	*	*	–	–
DBNZ eam, rel	3+	*4	2× (b)	Branch when byte (ear) = (eam) – 1, and (eam) ≠ 0	–	–	–	–	–	*	*	*	–	*
DWBNZ ear, rel	3	*2	0	Branch when word (ear) = (ear) – 1, and (ear) ≠ 0	–	–	–	–	–	*	*	*	–	–
DWBNZ eam, rel	3+	*4	2× (c)	Branch when word (eam) = (eam) – 1, and (eam) ≠ 0	–	–	–	–	–	*	*	*	–	*
INT #vct8	2	14	8× (c)	Software interrupt	–	–	R	S	–	–	–	–	–	–
INT addr16	3	12	6× (c)	Software interrupt	–	–	R	S	–	–	–	–	–	–
INTP addr24	4	13	6× (c)	Software interrupt	–	–	R	S	–	–	–	–	–	–
INT9	1	14	8× (c)	Software interrupt	–	–	R	S	–	–	–	–	–	–
RETI	1	9	6× (c)	Return from interrupt	–	–	*	*	*	*	*	*	*	–
RETIQ *6	2	11	*5	Return from interrupt	–	–	*	*	*	*	*	*	*	–
LINK #imm8	2	6	(c)	At constant entry, save old frame pointer to stack, set new frame pointer, and allocate local pointer area	–	–	–	–	–	–	–	–	–	–
UNLINK	1	5	(c)	At constant entry, retrieve old frame pointer from stack.	–	–	–	–	–	–	–	–	–	–
RET *7	1	4	(c)	Return from subroutine	–	–	–	–	–	–	–	–	–	–
RETP *8	1	5	(d)	Return from subroutine	–	–	–	–	–	–	–	–	–	–

For an explanation of "(b)", "(c)" and "(d)", refer to Table 5, "Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles."

*1: 4 when branching, 3 when not branching
*2: 5 when branching, 4 when not branching
*3: 5 + (a) when branching, 4 + (a) when not branching
*4: 6 + (a) when branching, 5 + (a) when not branching
*5: 3 × (b) + 2 × (c) when an interrupt request is generated, 6 × (c) when returning from the interrupt.
*6: High-speed interrupt return instruction. When an interrupt request is detected during this instruction, the instruction branches to the interrupt vector without performing stack operations when the interrupt is generated.
*7: Return from stack (word)
*8: Return from stack (long word)

Table 22 Other Control Instructions (Byte/Word/Long Word) [36 Instructions]

Mnemonic	#	cycles	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
PUSHW A	1	3	(c)	word (SP) ← (SP) –2, ((SP)) ← (A)	–	–	–	–	–	–	–	–	–	–
PUSHW AH	1	3	(c)	word (SP) ← (SP) –2, ((SP)) ← (AH)	–	–	–	–	–	–	–	–	–	–
PUSHW PS	1	3	(c)	word (SP) ← (SP) –2, ((SP)) ← (PS)	–	–	–	–	–	–	–	–	–	–
PUSHW rlst	2	*3	*4	(SP) ← (SP) –2n, ((SP)) ← (rlst)	–	–	–	–	–	–	–	–	–	–
POPW A	1	3	(c)	word (A) ← ((SP)), (SP) ← (SP) +2	–	*	–	–	–	–	–	–	–	–
POPW AH	1	3	(c)	word (AH) ← ((SP)), (SP) ← (SP) +2	–	–	–	–	–	–	–	–	–	–
POPW PS	1	3	(c)	word (PS) ← ((SP)), (SP) ← (SP) +2	–	–	*	*	*	*	*	*	*	–
POPW rlst	2	*2	*4	(rlst) ← ((SP)) , (SP) ← (SP)	–	–	–	–	–	–	–	–	–	–
JCTX @A	1	9	6× (c)	Context switch instruction	–	–	*	*	*	*	*	*	*	–
AND CCR, #imm8	2	3	0	byte (CCR) ← (CCR) and imm8	–	–	*	*	*	*	*	*	*	–
OR CCR, #imm8	2	3	0	byte (CCR) ← (CCR) or imm8	–	–	*	*	*	*	*	*	*	–
MOV RP, #imm8	2	2	0	byte (RP) ←imm8	–	–	–	–	–	–	–	–	–	–
MOV ILM, #imm8	2	2	0	byte (ILM) ←imm8	–	–	–	–	–	–	–	–	–	–
MOVEA RWi, ear	2	3	0	word (RWi) ←ear	–	–	–	–	–	–	–	–	–	–
MOVEA RWi, eam	2+	2+ (a)	0	word (RWi) ←eam	–	–	–	–	–	–	–	–	–	–
MOVEA A, ear	2	2	0	word(A) ←ear	–	*	–	–	–	–	–	–	–	–
MOVEA A, eam	2+	1+ (a)	0	word (A) ←eam	–	*	–	–	–	–	–	–	–	–
ADDSP #imm8	2	3	0	word (SP) ← ext (imm8)	–	–	–	–	–	–	–	–	–	–
ADDSP #imm16	3	3	0	word (SP) ← imm16	–	–	–	–	–	–	–	–	–	–
MOV A, brgl	2	*1	0	byte (A) ← (brgl)	Z	*	–	–	–	*	*	–	–	–
MOV brg2, A	2	1	0	byte (brg2) ← (A)	–	–	–	–	–	*	*	–	–	–
MOV brg2, #imm8	3	2	0	byte (brg2) ← imm8	–	–	–	–	–	*	*	–	–	–
NOP	1	1	0	No operation	–	–	–	–	–	–	–	–		–
ADB	1	1	0	Prefix code for AD space access	–	–	–	–	–	–	–	–	–	–
DTB	1	1	0	Prefix code for DT space access	–	–	–	–	–	–	–	–	–	–
PCB	1	1	0	Prefix code for PC space access	–	–	–	–	–	–	–	–	–	–
SPB	1	1	0	Prefix code for SP space access	–	–	–	–	–	–	–	–	–	–
NCC	1	1	0	Prefix code for no flag change	–	–	–	–	–	–	–	–	–	–
CMR	1	1	0	Prefix code for the common register bank	–	–	–	–	–	–	–	–	–	–
MOVW SPCU, #imm16	4	2	0	word (SPCU) ← (imm16)	–	–	–	–	–	–	–	–	–	–
MOVW SPCL, #imm16	4	2	0	word (SPCL) ← (imm16)	–	–	–	–	–	–	–	–	–	–
SETSPC	2	2	0	Stack check ooperation enable	–	–	–	–	–	–	–	–	–	–
CLRSPC	2	2	0	Stack check ooperation disable	–	–	–	–	–	–	–	–	–	–
BTSCN A	2	*5	0	byte (A)← position of "1" bit in word (A)	Z	–	–	–	–	–	*	–	–	–
BTSCNS A	2	*6	0	byte (A)← position of "1" bit in word (A) ×2	Z	–	–	–	–	–	*	–	–	–
BTSCND A	2	*7	0	byte (A)← position of "1" bit in word (A) ×4	Z	–	–	–	–	–	*	–	–	–

For an explanation of "(a)" and "(c)", refer to Tables 4 and 5.

*1: PCB, ADB, SSB, USB, and SPB: 1 cycle
DTB: 2 cycles
DPR: 3 cycles

*2: 3 + 4 × (pop count)

*3: 3 + 4 × (push count)

*4: Pop count × (c), or push count × (c)

*5: 3 when AL is 0, 5 when AL is not 0.

*6: 4 when AL is 0, 6 when AL is not 0.

*7: 5 when AL is 0, 7 when AL is not 0.

Table 23 Bit Manipulation Instructions [21 Instructions]

Mnemonic		#	cycles	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
MOVB	A, dir:bp	3	3	(b)	byte (A) ← (dir:bp) b	Z	*	–	–	–	*	*	–	–	–
MOVB	A, addr16:bp	4	3	(b)	byte (A) ← (addr16:bp) b	Z	*	–	–	–	*	*	–	–	–
MOVB	A, io:bp	3	3	(b)	byte (A) ← (io:bp) b	Z	*	–	–	–	*	*	–	–	–
MOVB	dir:bp, A	3	4	2× (b)	bit (dir:bp) b ← (A)	–	–	–	–	–	*	*	–	–	*
MOVB	addr16:bp, A	4	4	2× (b)	bit (addr16:bp) b ← (A)	–	–	–	–	–	*	*	–	–	*
MOVB	io:bp, A	3	4	2× (b)	bit (io:bp) b ← (A)	–	–	–	–	–	*	*	–	–	*
SETB	dir:bp	3	4	2× (b)	bit (dir:bp) b ← 1	–	–	–	–	–	–	–	–	–	*
SETB	addr16:bp	4	4	2× (b)	bit (addr16:bp) b ← 1	–	–	–	–	–	–	–	–	–	*
SETB	io:bp	3	4	2× (b)	bit (io:bp) b ← 1	–	–	–	–	–	–	–	–	–	*
CLRB	dir:bp	3	4	2× (b)	bit (dir:bp) b ← 0	–	–	–	–	–	–	–	–	–	*
CLRB	addr16:bp	4	4	2× (b)	bit (addr16:bp) b ← 0	–	–	–	–	–	–	–	–	–	*
CLRB	io:bp	3	4	2× (b)	bit (io:bp) b ← 0	–	–	–	–	–	–	–	–	–	*
BBC	dir:bp, rel	4	*1	(b)	Branch when (dir:bp) b = 0	–	–	–	–	–	–	*	–	–	–
BBC	addr16:bp, rel	5	*1	(b)	Branch when (addr16:bp) b = 0	–	–	–	–	–	–	*	–	–	–
BBC	io:bp, rel	4	*1	(b)	Branch when (io:bp) b = 0	–	–	–	–	–	–	*	–	–	–
BBS	dir:bp, rel	4	*1	(b)	Branch when (dir:bp) b = 1	–	–	–	–	–	–	*	–	–	–
BBS	addr16:bp, rel	5	*1	(b)	Branch when (addr16:bp) b = 1	–	–	–	–	–	–	*	–	–	–
BBS	io:bp, rel	4	*1	(b)	Branch when (io:bp) b = 1	–	–	–	–	–	–	*	–	–	–
SBBS	addr16:bp, rel	5	*2	2× (b)	Branch when (addr16:bp) b = 1, bit = 1	–	–	–	–	–	–	*	–	–	*
WBTS	io:bp	3	*3	*4	Wait until (io:bp) b = 1	–	–	–	–	–	–	–	–	–	–
WBTC	io:bp	3	*3	*4	Wait until (io:bp) b = 0	–	–	–	–	–	–	–	–	–	–

For an explanation of “(b)”, refer to Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

*1: 5 when branching, 4 when not branching
*2: 7 when condition is satisfied, 6 when not satisfied
*3: Undefined count
*4: Until condition is satisfied

Table 24 Accumulator Manipulation Instructions (Byte/Word) [6 Instructions]

Mnemonic	#	cycles	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
SWAP	1	3	0	byte (A) 0 to 7 ←→ (A) 8 to 15	–	–	–	–	–	–	–	–	–	–
SWAPW	1	2	0	word (AH) ←→ (AL)	–	*	–	–	–	–	–	–	–	–
EXT	1	1	0	Byte code extension	X	–	–	–	–	*	*	–	–	–
EXTW	1	2	0	Word code extension	–	X	–	–	–	*	*	–	–	–
ZEXT	1	1	0	Byte zero extension	Z	–	–	–	–	R	*	–	–	–
ZEXTW	1	2	0	Word zero extension	–	Z	–	–	–	R	*	–	–	–

Table 25 String Instructions [10 Instructions]

Mnemonic	#	cycles	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
MOVS/MOVSI	2	*2	*3	Byte transfer @AH+ ← @AL+, counter = RW0	–	–	–	–	–	–	–	–	–	–
MOVSD	2	*2	*3	Byte transfer @AH– ← @AL–, counter = RW0	–	–	–	–	–	–	–	–	–	–
SCEQ/SCEQI	2	*1	*4	Byte retrieval @AH+ – AL, counter = RW0	–	–	–	–	–	*	*	*	*	–
SCEQD	2	*1	*4	Byte retrieval @AH– – AL, counter = RW0	–	–	–	–	–	*	*	*	*	–
FILS/FILSI	2	5m +3	*5	Byte filling @AH+ ← AL, counter = RW0	–	–	–	–	–	*	*	–	–	–
MOVSW/MOVSWI	2	*2	*6	Word transfer @AH+ ← @AL+, counter = RW0	–	–	–	–	–	–	–	–	–	–
MOVSWD	2	*2	*6	Word transfer @AH– ← @AL–, counter = RW0	–	–	–	–	–	–	–	–	–	–
SCWEQ/SCWEQI	2	*1	*7	Word retrieval @AH+ – AL, counter = RW0	–	–	–	–	–	*	*	*	*	–
SCWEQD	2	*1	*7	Word retrieval @AH– – AL, counter = RW0	–	–	–	–	–	*	*	*	*	–
FILSW/FILSWI	2	5m +3	*8	Word filling @AH+ ← AL, counter = RW0	–	–	–	–	–	*	*	–	–	–

m: RW0 value (counter value)

*1: 3 when RW0 is 0, 2 + 6 × (RW0) for count out, and 6n + 4 when match occurs
*2: 4 when RW0 is 0, 2 + 6 × (RW0) in any other case
*3: (b) × (RW0)
*4: (b) × n
*5: (b) × (RW0)
*6: (c) × (RW0)
*7: (c) × n
*8: (c) × (RW0)

Table 26 Multiple Data Transfer Instructions [18 Instructions]

Mnemonic	#	cycles	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
MOVM @A, @RLi, #imm8	3	*1	*3	Multiple data trasfer byte ((A)) ← ((RLi))	–	–	–	–	–	–	–	–	–	–
MOVM @A, eam, #imm8	3+	*2	*3	Multiple data trasfer byte ((A)) ← (eam)	–	–	–	–	–	–	–	–	–	–
MOVM addr16, @RLi, #imm8	5	*1	*3	Multiple data trasfer byte (addr16) ← ((RLi))	–	–	–	–	–	–	–	–	–	–
MOVM addr16, eam, #imm8	5+	*2	*3	Multiple data trasfer byte (addr16) ← (eam)	–	–	–	–	–	–	–	–	–	–
MOVMW @A, @RLi, #imm8	3	*1	*4	Multiple data trasfer word ((A)) ← ((RLi))	–	–	–	–	–	–	–	–	–	–
MOVMW @A, eam, #imm8	3+	*2	*4	Multiple data trasfer word ((A)) ← (eam)	–	–	–	–	–	–	–	–	–	–
MOVMW addr16, @RLi, #imm8	5	*1	*4	Multiple data trasfer word (addr16) ← ((RLi))	–	–	–	–	–	–	–	–	–	–
MOVMW addr16, eam, #imm8	5+	*2	*4	Multiple data trasfer word (addr16) ← (eam)	–	–	–	–	–	–	–	–	–	–
MOVM @RLi, @A, #imm8	3	*1	*3	Multiple data trasfer byte ((RLi)) ← ((A))	–	–	–	–	–	–	–	–	–	–
MOVM eam, @A, #imm8	3+	*2	*3	Multiple data trasfer byte (eam) ← ((A))	–	–	–	–	–	–	–	–	–	–
MOVM @RLi, addr16, #imm8	5	*1	*3	Multiple data transfer byte ((RLi)) ← (addr16)	–	–	–	–	–	–	–	–	–	–
MOVM eam, addr16, #imm8	5+	*2	*3	Multiple data transfer byte (eam) ← (addr16)	–	–	–	–	–	–	–	–	–	–
MOVMW @RLi, @A, #imm8	3	*1	*4	Multiple data trasfer word ((RLi)) ← ((A))	–	–	–	–	–	–	–	–	–	–
MOVMW eam, @A, #imm8	3+	*2	*4	Multiple data trasfer word (eam) ← ((A))	–	–	–	–	–	–	–	–	–	–
MOVMW @RLi, addr16, #imm8	5	*1	*4	Multiple data transfer word ((RLi)) ← (addr16)	–	–	–	–	–	–	–	–	–	–
MOVMW eam, addr16, #imm8	5+	*2	*4	Multiple data transfer word (eam) ← (addr16)	–	–	–	–	–	–	–	–	–	–
MOVM bnk : addr16, *5 bnk : addr16, #imm8	7	*1	*3	Multiple data transfer byte (bnk:addr16) ← (bnk:addr16)	–	–	–	–	–	–	–	–	–	–
MOVMW bnk : addr16, *5 bnk : addr16, #imm8	7	*1	*4	Multiple data transfer word (bnk:addr16) ← (bnk:addr16)	–	–	–	–	–	–	–	–	–	–

*1: 5 + imm8 × 5, 256 times when imm8 is zero.
*2: 5 + imm8 × 5 + (a), 256 times when imm8 is zero.
*3: Number of transfers × (b) × 2
*4: Number of transfers × (c) × 2
*5: The bank register specified by “bnk” is the same as for the MOVS instruction.

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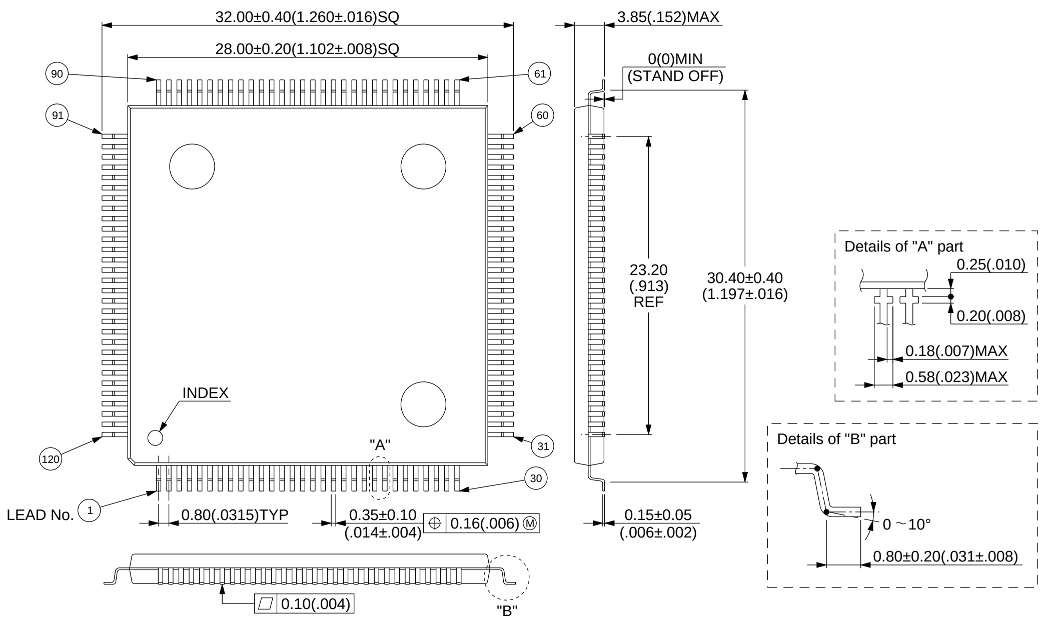
Part number	Type	Package	Remarks
MB90224 MB90223 MB90P224A MB90P224B	MB90224PF MB90223PF MB90P224PF MB90P224BPF	120-pin Plastic QFP (FPT-120P-M03)	
MB90W224A MB90W224B	MB90W224ZF MB90W224BZF	120-pin Ceramic QFP (FPT-120C-C02)	ES level only
MB90V220	MB90V220CR	256-pin Ceramic PGA (PGA-256C-A02)	For evaluation

■ PACKAGE DIMENSIONS

120-pin Plastic QFP
(FPT-120P-M03)



Dimensions in mm (inches)

120-pin Ceramic QFP
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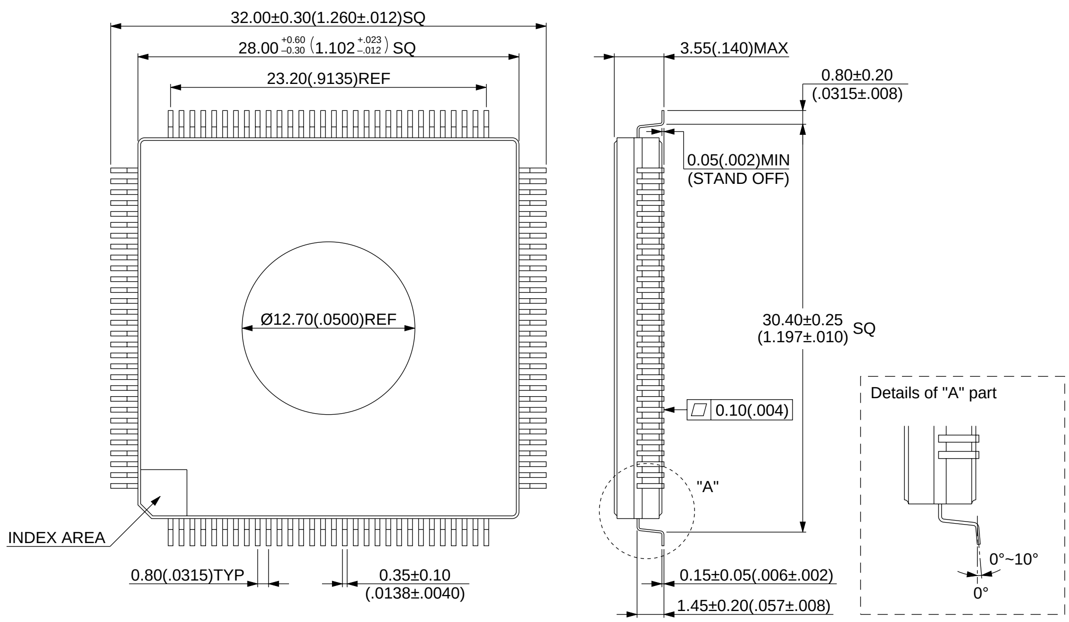

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