FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-13728-3E

*16-bit Proprietary Microcontroller*

**CMOS**

# F²MC-16LX MB90455 Series

## MB90F455 (S) /F456 (S) /F457 (S)
## MB90455 (S) /456 (S) /457 (S) /V495G

## ■ DESCRIPTION

MB90455 series devices are general-purpose high-performance 16-bit micro controllers designed for process control of consumer products, which require high-speed real-time processing.

The system, inheriting the architecture of F²MC* family, employs additional instruction ready for high-level languages, expanded addressing mode, enhanced multiply-divide instructions, and enriched bit-processing instructions. Furthermore, employment of 32-bit accumulator achieves processing of long-word data (32 bits).

The peripheral resources of MB90455 series include the following:

8/10-bit A/D converter, UART 1, 8/16-bit PPG timer, 16-bit input-output timer (16-bit free-run timer, input capture 0, 1, 2, 3 (ICU)).

*: "F²MC", an abbreviation for FUJITSU Flexible Microcontroller, is a registered trademark of FUJITSU Ltd.

## ■ FEATURES

- **Clock**
  - Built-in PLL clock frequency multiplication circuit
  - Selection of machine clocks (PLL clocks) is allowed among frequency division by two on oscillation clock, and multiplication of 1 to 4 times of oscillation clock (for 4-MHz oscillation clock, 4 MHz to 16 MHz).
  - Operation by sub-clock (8.192 kHz) is allowed.
  - Minimum execution time of instruction: 62.5 ns (when operating with 4-MHz oscillation clock, and 4-time multiplied PLL clock).

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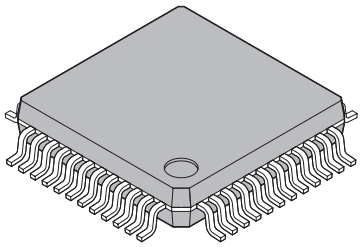
## ■ PACKAGE

48-pin plastic-LQFP



(FPT-48P-M26)

FUJITSU

- **16 Mbyte CPU memory space**
  - 24-bit internal addressing
- **Instruction system best suited to controller**
  - Wide choice of data types (bit, byte, word, and long word)
  - Wide choice of addressing modes (23 types)
  - Enhanced multiply-divide instructions and RETI instructions
  - Enhanced high-precision computing with 32-bit accumulator
- **Instruction system compatible with high-level language (C language) and multitask**
  - Employing system stack pointer
  - Enhanced various pointer indirect instructions
  - Barrel shift instructions
- **Increased processing speed**
  - 4-byte instruction queue
- **Powerful interrupt function with 8 levels and 34 factors**
- **Automatic data transfer function independent of CPU**
  - Expanded intelligent I/O service function ($EI^2$ OS): Maximum of 16 channels
- **Low power consumption (standby) mode**
  - Sleep mode (a mode that halts CPU operating clock)
  - Time-base timer mode (a mode that operates oscillation clock, sub clock, time-base timer and clock timer only)
  - Clock mode (a mode that operates sub clock and clock timer only)
  - Stop mode (a mode that stops oscillation clock and sub clock)
  - CPU blocking operation mode
- **Process**
  - CMOS technology
- **I/O port**
  - General-purpose input/output port (CMOS output): 34 ports(MB90F455/F456/F457, MB90455/456/457) (including 4 high-current output ports) (When sub clock is not used, 36 ports(MB90F455S/F456S/F457S, MB90455S/456S/457S))
- **Timer**
  - Time-base timer, clock timer, watchdog timer: 1 channel
  - 8/16-bit PPG timer: 8-bit x 4 channels, or 16-bit x 2 channels
  - 16-bit reload timer: 2 channels
  - 16-bit input/output timer
    - 16-bit free run timer: 1 channel
    - 16-bit input capture: (ICU): 4 channels

    Interrupt request is issued upon latching a count value of 16-bit free run timer by detection of an edge on pin input.
- **UART 1: 1 channel**
  - Equipped with full-duplex double buffer
  - Clock-asynchronous or clock-synchronous serial transmission is available

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- **DTP/External interrupt: 4 channels**
  - Module for activation of expanded intelligent I/O service ($EI^2OS$), and generation of external interrupt.
- **Delay interrupt generator module**
  - Generates interrupt request for task switching.
- **8/10-bit A/D converter: 8 channels**
  - Resolution is selectable between 8-bit and 10-bit.
  - Activation by external trigger input is allowed.
  - Conversion time: 6.125 µs (at 16-MHz machine clock, including sampling time)
- **Program patch function**
  - Address matching detection for 2 address pointers.

## ■ PRODUCT LINEUP

| Parameter \ Part Number | | MB90F455 (S) / F456 (S) /F457 (S) | MB90455 (S) / 456 (S) /457 (S) | MB90V495G |
|---|---|---|---|---|
| Classification | | Flash ROM | Mask ROM | Evaluation product |
| ROM capacity | | MB90F455 (S) : 24 Kbytes<br>MB90F456 (S) : 32 Kbytes<br>MB90F457 (S) : 64 Kbytes | MB90455 (S) : 24 Kbytes<br>MB90456 (S) : 32 Kbytes<br>MB90457 (S) : 64 Kbytes | — |
| RAM capacity | | 2 Kbytes | | 6 Kbytes |
| Clock | | MB90F455/F456/F457 : 2 systems<br>MB90F455S/F456S/F457S : 1 system | MB90455/456/457 : 2 systems<br>MB90455S/456S/457S : 1 system | 2 systems |
| Process | | CMOS | | |
| Package | | LQFP-48 (0.50 mm width) | | PGA256 |
| Operating power supply voltage | | 3.5 V to 5.5 V | | 4.5 V to 5.5 V |
| Special power supply for emulator*1 | | — | | None |
| CPU functions | | Number of basic instructions : 351 instructions<br>Instruction bit length : 8 bits and 16 bits<br>Instruction length : 1 byte to 7 bytes<br>Data bit length : 1 bit, 8 bits, 16 bits | | |
| | | Minimum instruction execution time : 62.5 ns (at 16-MHz machine clock) | | |
| | | Interrupt processing time : 1.5 µs at minimum (at 16-MHz machine clock) | | |
| Low power consumption (standby) mode | | Sleep mode/Clock mode/Time-base timer mode/<br>Stop mode/CPU intermittent | | |
| I/O port | | General-purpose input/output ports (CMOS output) : 34 ports (36 ports*2)<br>including 4 high-current output ports (P14 to P17) | | |
| Time-base timer | | 18-bit free-run counter<br>Interrupt cycle : 1.024 ms, 4.096 ms, 16.834 ms, 131.072 ms<br>(with oscillation clock frequency at 4 MHz) | | |
| Watchdog timer | | Reset generation cycle: 3.58 ms, 14.33 ms, 57.23 ms, 458.75 ms<br>(with oscillation clock frequency at 4 MHz) | | |
| 16-bit input/ output timer | 16-bit free-run timer | Number of channels: 1<br>Interrupt upon occurrence of overflow | | |
| | Input capture | Number of channels: 4<br>Retaining free-run timer value set by pin input (rising edge, falling edge, and both edges) | | |
| 16-bit reload timer | | Number of channels: 2<br>16-bit reload timer operation<br>Count clock cycle: 0.25 µs, 0.5 µs, 2.0 µs<br>(at 16-MHz machine clock frequency)<br>External event count is allowed. | | |
| Clock timer | | 15-bit free-run counter<br>Interrupt cycle: 31.25 ms, 62.5 ms, 12 ms, 250 ms, 500 ms, 1.0 s, 2.0 s<br>(with 8.192 kHz sub clock) | | |

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| Parameter \ Part Number | MB90F455 (S) / F456 (S) /F457 (S) | MB90455 (S) / 456 (S) /457 (S) | MB90V495G |
|---|---|---|---|
| 8/16-bit PPG timer | Number of channels: 2 (four 8-bit channels are available also)<br>PPG operation is allowed with four 8-bit channels or one 16-bit channel.<br>Outputting pulse wave of arbitrary cycle or arbitrary duty is allowed.<br>Count clock: 62.5 ns to 1 µs<br>(with 16 MHz machine clock) | | |
| Delay interrupt generator module | Interrupt generator module for task switching. Used for Real-time OS. | | |
| DTP/External interrupt | Number of inputs: 4<br>Activated by rising edge, falling edge, “H” level or “L” level input.<br>External interrupt or expanded intelligent I/O service (EI²OS) is available. | | |
| 8/10-bit A/D converter | Number of channels: 8<br>Resolution: Selectable 10-bit or 8-bit.<br>Conversion time: 6.125 µs (at 16-MHz machine clock, including sampling time)<br>Sequential conversion of two or more successive channels is allowed. (Setting a maximum of 8 channels is allowed.)<br>Single conversion mode : Selected channel is converted only once.<br>Sequential conversion mode: Selected channel is converted repetitively.<br>Halt conversion mode : Conversion of selected channel is stopped and activated alternately. | | |
| UART 1 | Number of channels: 1<br>Clock-synchronous transfer: 62.5 Kbps to 2 Mbps<br>Clock-asynchronous transfer: 9,615 bps to 500 Kbps<br>Communication is allowed by bi-directional serial communication function and master/slave type connection. | | |

*1 : Settings of DIP switch S2 for using emulation pod MB2145-507. For details, See MB2145-507 Hardware Manual (2.7 Power Pin solely for Emulator).

*2 : MB90F455S/F456S/F457S, MB90455S/456S/457S

## ■ PACKAGES AND PRODUCT MODELS

| Package | MB90F455 (S) /F456 (S) /F457 (S) | MB90455 (S) /456 (S) /457 (S) |
|---|---|---|
| FPT-48P-M26 | ◯ | ◯ |

◯ : Yes × : No

Note : Refer to “■ PACKAGE DIMENSION” for details of the package.

## ■ PRODUCT COMPARISON

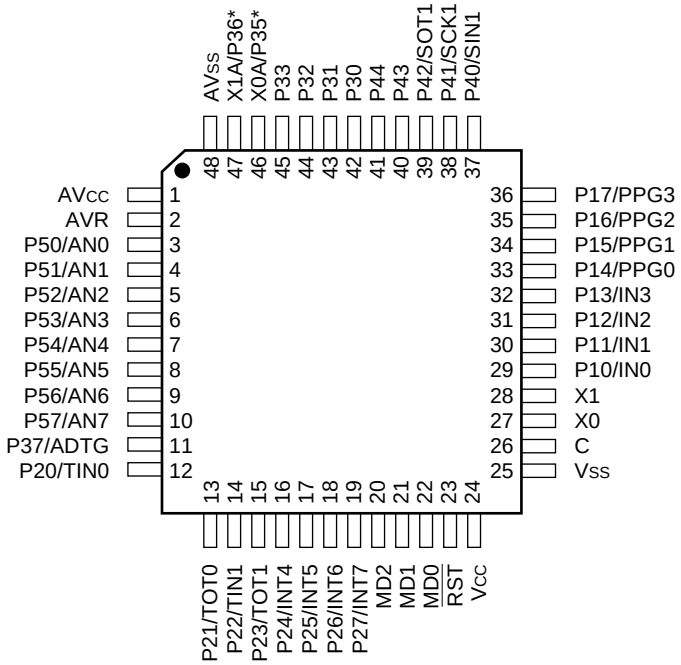
**Memory space**

When testing with test product for evaluation, check the differences between the product and a product to be used actually. Pay attention to the following points:

- The MB90V495G has no built-in ROM. However, a special-purpose development tool allows the operations as those of one with built-in ROM. ROM capacity depends on settings on a development tool.
- On MB90V495G, an image from $FF4000_H$ to $FFFFFF_H$ is viewed on 00 bank and an image of $FE0000_H$ to $FF3FFF_H$ is viewed only on FE bank and FF bank. (Modified on settings of a development tool.)
- On MB90F455 (S) /F456 (S) /F457 (S) , MB90455 (S) /456 (S) /457 (S) , an image from $FF4000_H$ to $FFFFFF_H$ is viewed on 00 bank and an image of $FE0000_H$ to $FF3FFF_H$ is viewed only on FF bank.

## ■ PIN ASIGNMENT

(TOP VIEW)




(FPT-48P-M26)

* : MB90F455/F456/F457, MB90455/456/457 : X1A, X0A
MB90F455S/F456S/F457S, MB90455S/456S/457S : P36, P35

## ■ PIN DESCRIPTION

| Pin No. | Pin name | Circuit format | Description |
|---|---|---|---|
| 1 | AVcc | — | Vcc power input pin for A/D converter |
| 2 | AVR | — | Power (Vref+) input pin for A/D converter. Use as input for Vcc or lower. |
| 3 to 10 | P50 to P57 | E | General-purpose input/output ports. |
| | AN0 to AN7 | | Functions as an analog input pin for A/D converter. Valid when analog input setting is “enabled.” |
| 11 | P37 | D | General-purpose input/output port. |
| | ADTG | | Function as an external trigger input pin for A/D converter. Use the pin by setting as input port. |
| 12 | P20 | D | General-purpose input/output port. |
| | TIN0 | | Function as an event input pin for reload timer 0. Use the pin by setting as input port. |
| 13 | P21 | D | General-purpose input/output port. |
| | TOT0 | | Function as an event output pin for reload timer 0. Valid only when output setting is “enabled.” |
| 14 | P22 | D | General-purpose input/output port. |
| | TIN1 | | Function as an event input pin for reload timer 1. Use the pin by setting as input port. |
| 15 | P23 | D | General-purpose input/output port. |
| | TOT1 | | Function as an event output pin for reload timer 1. Valid only when output setting is “enabled.” |
| 16 to 19 | P24 to P27 | D | General-purpose input/output ports. |
| | INT4 to INT7 | | Functions as an external interrupt input pin. Use the pin by setting as input port. |
| 20 | MD2 | F | Input pin for specifying operation mode. Connect directly to Vss. |
| 21 | MD1 | C | Input pin for specifying operation mode. Connect directly to Vcc. |
| 22 | MD0 | C | Input pin for specifying operation mode. Connect directly to Vcc. |
| 23 | RST | B | External reset input pin. |
| 24 | Vcc | — | Power source (5 V) input pin. |
| 25 | Vss | — | Power source (0 V) input pin. |
| 26 | C | — | Capacitor pin for stabilizing power source. Connect a ceramic capacitor of approximately 0.1 μF. |
| 27 | X0 | A | Pin for high-rate oscillation. |
| 28 | X1 | A | Pin for high-rate oscillation. |
| 29 to 32 | P10 to P13 | D | General-purpose input/output ports. |
| | IN0 to IN3 | | Functions as trigger input pins of input capture channels 0 to 3. Use the pins by setting as input ports. |

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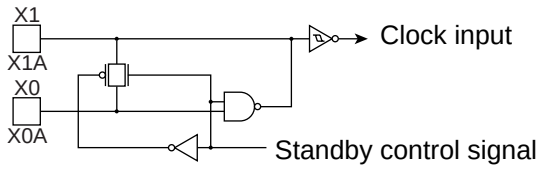
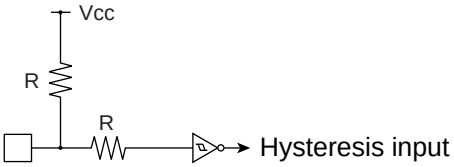
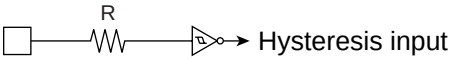
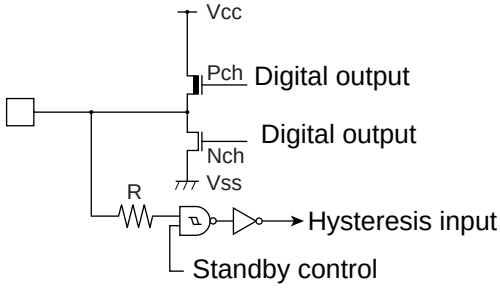
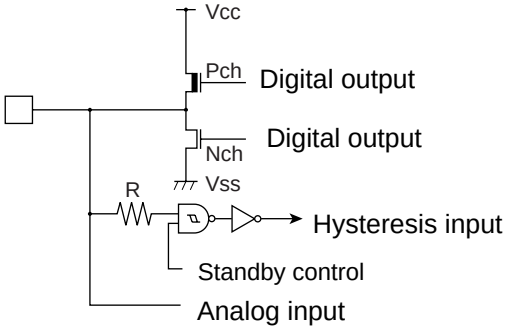
| Pin No. | Pin name | Circuit format | Description |
|---|---|---|---|
| 33 to 36 | P14 to P17 | G | General-purpose input/output ports. High-current output ports. |
| | PPG0 to PPG3 | | Functions as output pins of PPG timers 01 and 23. Valid when output setting is “enabled.” |
| 37 | P40 | D | General-purpose input/output port. |
| | SIN1 | | Serial data input pin for UART. Use the pin by setting as input port. |
| 38 | P41 | D | General-purpose input/output port. |
| | SCK1 | | Serial clock input pin for UART. Valid only when serial clock input/output setting on UART is “enabled.” |
| 39 | P42 | D | General-purpose input/output port. |
| | SOT1 | | Serial data input pin for UART. Valid only when serial data input/output setting on UART is “enabled.” |
| 40 | P43 | D | General-purpose input/output port. |
| 41 | P44 | D | General-purpose input/output port. |
| 42 to 45 | P30 to P33 | D | General-purpose input/output ports. |
| 46 | X0A* | A | Pin for low-rate oscillation. |
| | P35* | | General-purpose input/output port. |
| 47 | X1A* | A | Pin for low-rate oscillation. |
| | P36* | | General-purpose input/output port. |
| 48 | AVss | — | Vss power source input pin for A/D converter. |

* : MB90F455/F456/F457, MB90455/456/457 : X1A, X0A
MB90F455S/F456S/F457S, MB90455S/456S/457S : P36, P35

## ■ I/O CIRCUIT TYPE

| Type | Circuit | Remarks |
|---|---|---|
| A |  | • High-rate oscillation feedback resistor, approx.1 MΩ<br>• Low-rate oscillation feedback resistor, approx.10 MΩ |
| B |  | • Hysteresis input with pull-up resistor.<br>• Pull-up resistor, approx.50 kΩ |
| C |  | • Hysteresis input |
| D |  | • CMOS hysteresis input<br>• CMOS level output<br>• Standby control provided |
| E |  | • CMOS hysteresis input<br>• CMOS level output<br>• Shared for analog input pin<br>• Standby control provided |

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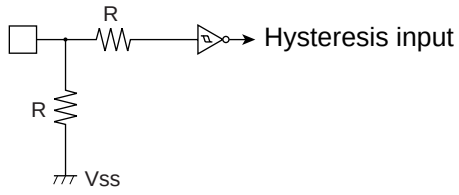
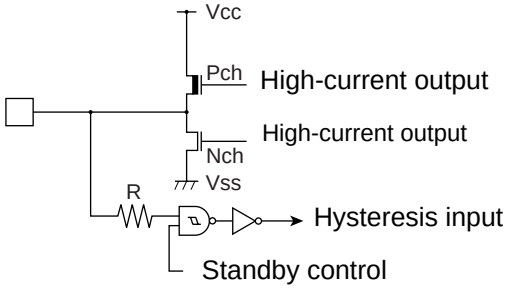
| Type | Circuit | Remarks |
|---|---|---|
| F |  | • Hysteresis input with pull-down resistor<br>• Pull-down resistor, approx. 50 kΩ<br>• FLASH product is not provided with pull-down resistor. |
| G |  | • CMOS hysteresis input<br>• CMOS level output (high-current output)<br>• Standby control provided |

## ■ HANDLING DEVICES

**• Do not exceed maximum rating (preventing “latch up”)**

- On a CMOS IC, latch-up may occur when applying a voltage higher than Vcc or a voltage lower than Vss to input or output pin, which has no middle or high withstand voltage. Latch-up may also occur when a voltage exceeding maximum rating is applied across Vcc and Vss.
- Latch-up causes drastic increase of power current, which may lead to destruction of elements by heat. Extreme caution must be taken not to exceed maximum rating.
- When turning on and off analog power source, take extra care not to apply an analog power voltages (AVcc and AVR) and analog input voltage that are higher than digital power voltage (Vcc).

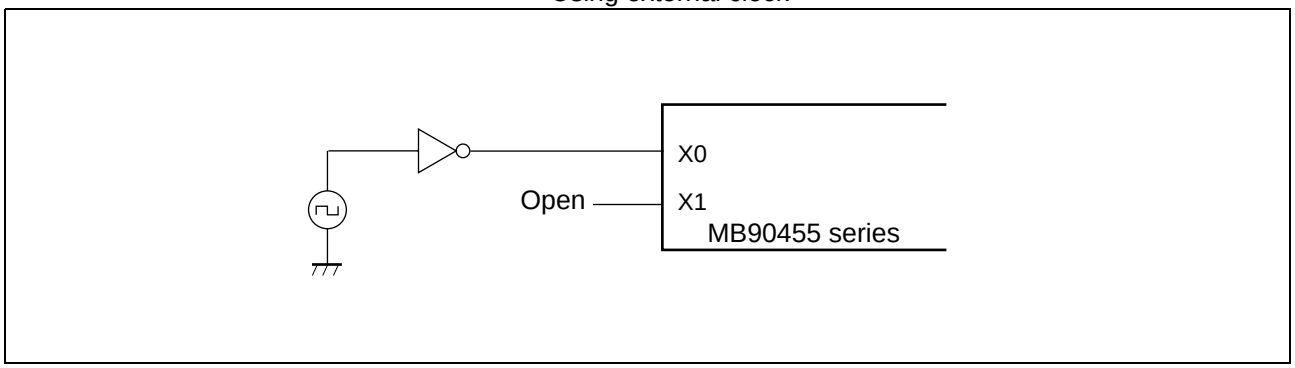
**• Handling unused pins**

- Leaving unused input pins open may cause permanent destruction by malfunction or latch-up. Apply pull-up or pull-down process to the unused pins using resistors of 2 kΩ or higher. Leave unused input pins open under output status, or process as input pins if they are under input status.

**• Using external clock**

- When using an external clock, drive only X0 pin and leave X1 pin open. An example of using an external clock is shown below.

Using external clock




**• Notes when using no sub clock**

- If an oscillator is not connected to X0A and X1A pin, apply pull-down resistor to X0A pin and leave X1A pin open.

**• About power supply pins**

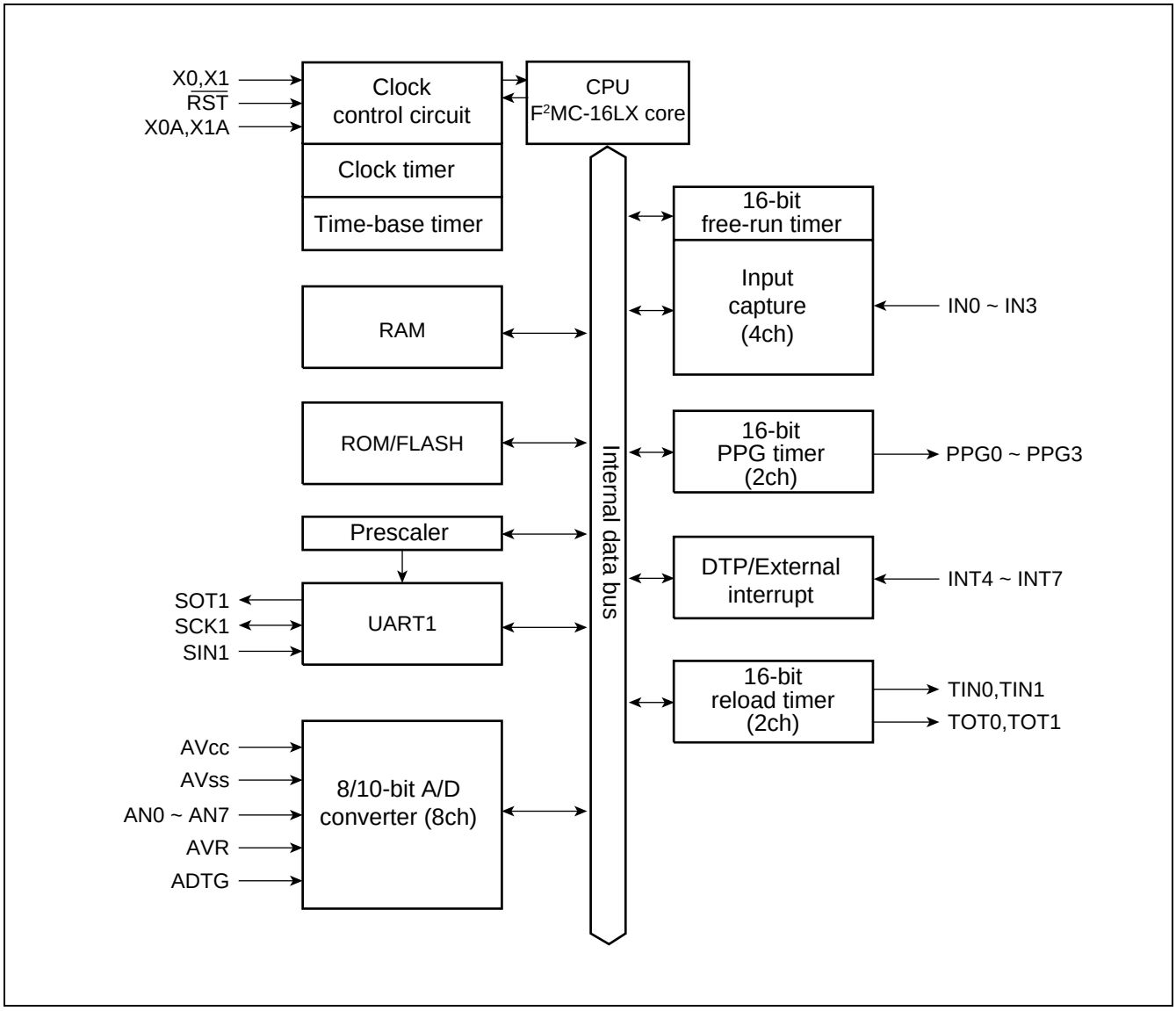
- If two ore more Vcc and Vss exist, the pins that should be at the same potential are connected to each other inside the device. For reducing unwanted emissions and preventing malfunction of strobe signals caused by increase of ground level, however, be sure to connect the Vcc and Vss pins to the power source and the ground externally.
- Pay attention to connect a power supply to Vcc and Vss of MB90455 series device in a lowest-possible impedance.
- Near pins of MB90455 series device, connecting a bypass capacitor is recommended at 0.1 μF across Vcc and Vss.

**• Crystal oscillator circuit**

- Noises around X0 and X1 pins cause malfunctions on a MB90455 series device. Design a print circuit so that X0 and X1 pins, an crystal oscillator (or a ceramic oscillator), and bypass capacitor to the ground become as close as possible to each other. Furthermore, avoid wires to X0 and X1 pins crossing each other as much as possible.
- Print circuit designing that surrounds X0 and X1 pins with grounding wires, which ensures stable operation, is strongly recommended.

- **Caution on Operations during PLL Clock Mode**
  - If the PLL clock mode is selected, the microcontroller attempt to be working with the self-oscillating circuit even when there is no external oscillator or external clock input is stopped. Performance of this operation, however, cannot be guaranteed.
- **Sequence of turning on power of A/D converter and applying analog input**
  - Be sure to turn on digital power (Vcc) before applying signals to the A/D converter and applying analog input signals (AN0 to AN7 pins).
  - Be sure to turn off the power of A/D converter and analog input before turning off the digital power source.
  - Be sure not to apply AVR exceeding AVcc when turning on and off. (No problems occur if analog and digital power is turned on and off simultaneously.)
- **Handling pins when A/D converter is not used**
  - If the A/D converter is not used, connect the pins under the following conditions: “AVcc=AVR=Vcc,” and “Avss=Vss”
- **Note on turning on power**
  - For preventing malfunctions on built-in step-down circuit, maintain a minimum of 50 μs of voltage rising time (between 0.2 V and 2.7 V) when turning on the power.
- **Stabilization of supply voltage**
  - A sudden change in the supply voltage may cause the device to malfunction even within the specified Vcc supply voltage operating range. Therefore, the Vcc supply voltage should be stabilized.
    For reference, the supply voltage should be controlled so that Vcc ripple variations (peak-to-peak values) at commercial frequencies (50 Hz to 60 Hz) fall below 10% of the standard $V_{CC}$ supply voltage and the coefficient of fluctuation does not exceed 0.1 V/ms at instantaneous power switching.

## ■ BLOCK DIAGRAM



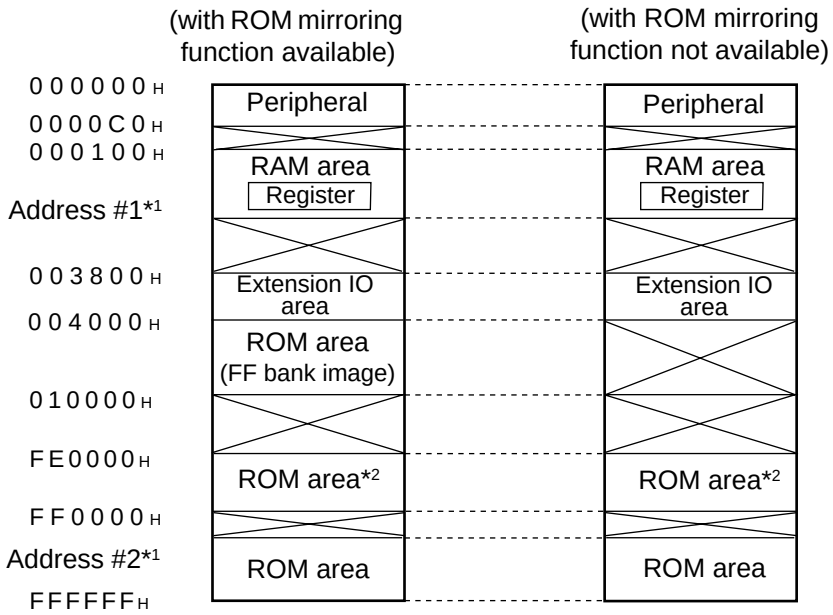
## ■ MEMORY MAP

MB90455 series allows specifying a memory access mode “single chip mode.”

### 1. Memory allocation of MB90455

MB90455 series model has 24-bit wide internal address bus and up to 24-bit bus of external address bus. A maximum of 16 Mbyte memory space of external access memory is accessible.

### 2. Memory map




| Product | Address #1*1 | Address #2*1 |
|---|---|---|
| MB90F455 (S) /455 (S) | 000900H | FFA000H |
| MB90F456 (S) /456 (S) | 000900H | FF8000H |
| MB90F457 (S) /457 (S) | 000900H | FF0000H |
| MB90V495G | 001900H | — |

: Internal access memory

: Access disallowed

*1 : Addresses #1 and #3 are product-specific.

*2 : On MB90F455 (S) /F456 (S) /F457 (S) , 455 (S) /456 (S) /457 (S) , to read “FE0000H” to “FEFFFFH” is to read out “FF0000H” to “FFFFFFH”.

Note : When internal ROM is operating, F2MC-16LX allows viewing ROM data image on FF bank at upper-level of 00 bank. This function is called “mirroring ROM,” which allows effective use of C compiler small model. F2MC-16LX assigns the same low order 16-bit address to FF bank and 00 bank, which allows referencing table in ROM without specifying “far” using pointer.
For example, when accessing to “00C000H”, ROM data at “FFC000H” is accessed actually. However, because ROM area of FF bank exceeds 48 Kbytes, viewing all areas is not possible on 00 bank image. Because ROM data of “FF4000H” to “FFFFFFH” is viewed on “004000H” to “00FFFFH” image, store a ROM data table in area “FF4000H” to “FFFFFFH.”

## ■ I/O MAP

| Address | Register abbreviation | Register name | Reset value | Peripheral function name | Read/ Write |
|---|---|---|---|---|---|
| 000000H | (Reserved area) * | | | | |
| 000001H | PDR1 | Port 1 data register | XXXXXXXXB | Port 1 | R/W |
| 000002H | PDR2 | Port 2 data register | XXXXXXXXB | Port 2 | R/W |
| 000003H | PDR3 | Port 3 data register | XXXXXXXXB | Port 3 | R/W |
| 000004H | PDR4 | Port 4 data register | XXXXXXXXB | Port 4 | R/W |
| 000005H | PDR5 | Port 5 data register | XXXXXXXXB | Port 5 | R/W |
| 000006H to 000010H | (Reserved area) * | | | | |
| 000011H | DDR1 | Port 1 direction data register | 00000000B | Port 1 | R/W |
| 000012H | DDR2 | Port 2 direction data register | 00000000B | Port 2 | R/W |
| 000013H | DDR3 | Port 3 direction data register | 000X0000B | Port 3 | R/W |
| 000014H | DDR4 | Port 4 direction data register | XXX00000B | Port 4 | R/W |
| 000015H | DDR5 | Port 5 direction data register | 00000000B | Port 5 | R/W |
| 000016H to 00001AH | (Reserved area) * | | | | |
| 00001BH | ADER | Analog input permission register | 11111111B | 8/10-bit A/D converter | R/W |
| 00001CH to 000025H | (Reserved area) * | | | | |
| 000026H | SMR1 | Serial mode register 1 | 00000000B | UART1 | R/W |
| 000027H | SCR1 | Serial control register 1 | 00000100B | | R/W, W |
| 000028H | SIDR1/ SODR1 | Serial input data register 1/ Serial output data register 1 | XXXXXXXXB | | R, W |
| 000029H | SSR1 | Serial status data register 1 | 00001000B | | R, R/W |
| 00002AH | (Reserved area) * | | | | |
| 00002BH | CDCR1 | Communication prescaler control register 1 | 0XXX0000B | UART1 | R/W |
| 00002CH to 00002FH | (Reserved area) * | | | | |
| 000030H | ENIR | DTP/External interrupt permission register | 00000000B | DTP/External interrupt | R/W |
| 000031H | EIRR | DTP/External interrupt permission register | XXXXXXXXB | | R/W |
| 000032H | (Reserved area) * | | | | |
| 000033H | ELVR | Detection level setting register | 00000000B | DTP/External interrupt | R/W |

*(Continued)*

| Address | Register abbreviation | Register name | Reset value | Peripheral function name | Read/ Write |
|---|---|---|---|---|---|
| 000034H | ADCS | A/D control status register | 00000000B | 8/10-bit A/D converter | R/W |
| 000035H | | | 00000000B | | R/W, W |
| 000036H | ADCR | A/D data register | XXXXXXXXB | | W, R |
| 000037H | | | 00101XXXB | | R |
| 000038H to 00003FH | (Reserved area) * | | | | |
| 000040H | PPGC0 | PPG0 operation mode control register | 0X000XX1B | 8/16-bit PPG timer 0/1 | R/W, W |
| 000041H | PPGC1 | PPG1 operation mode control register | 0X000001B | | R/W, W |
| 000042H | PPG01 | PPG0/1 count clock selection register | 000000XXB | | R/W |
| 000043H | (Reserved area) * | | | | |
| 000044H | PPGC2 | PPG2 operation mode control register | 0X000XX1B | 8/16-bit PPG timer 2/3 | R/W, W |
| 000045H | PPGC3 | PPG3 operation mode control register | 0X000001B | | R/W, W |
| 000046H | PPG23 | PPG2/3 count clock selection register | 000000XXB | | R/W |
| 000047H to 00004FH | (Reserved area) * | | | | |
| 000050H | IPCP0 | Input capture data register 0 | XXXXXXXXB | 16-bit input/output timer | R |
| 000051H | | | XXXXXXXXB | | |
| 000052H | IPCP1 | Input capture data register 1 | XXXXXXXXB | | R |
| 000053H | | | XXXXXXXXB | | |
| 000054H | ICS01 | Input capture control status register | 00000000B | | R/W |
| 000055H | ICS23 | | 00000000B | | |
| 000056H | TCDT | Timer counter data register | 00000000B | | R/W |
| 000057H | | | 00000000B | | |
| 000058H | TCCS | Timer counter control status register | 00000000B | | R/W |
| 000059H | (Reserved area) * | | | | |
| 00005AH | IPCP2 | Input capture data register 2 | XXXXXXXXB | 16-bit input/output timer | R |
| 00005BH | | | XXXXXXXXB | | |
| 00005CH | IPCP3 | Input capture data register 3 | XXXXXXXXB | | R |
| 00005DH | | | XXXXXXXXB | | |

*(Continued)*

| Address | Register abbreviation | Register name | Reset value | Peripheral function name | Read/ Write |
|---|---|---|---|---|---|
| 00005E$_H$ to 000065$_H$ | (Reserved area) * | | | | |
| 000066$_H$ | TMCSR0 | Timer control status register | 00000000$_B$ | 16-bit reload timer 0 | R/W |
| 000067$_H$ | | | XXXX0000$_B$ | | R/W |
| 000068$_H$ | TMCSR1 | | 00000000$_B$ | 16-bit reload timer 1 | R/W |
| 000069$_H$ | | | XXXX0000$_B$ | | R/W |
| 00006A$_H$ to 00006E$_H$ | (Reserved area) * | | | | |
| 00006F$_H$ | ROMM | ROM mirroring function selection register | XXXXXXX1$_B$ | ROM mirroring function selection module | W |
| 000070$_H$ to 00007F$_H$ | (Reserved area) * | | | | |
| 000080$_H$ to 00008F$_H$ | (Reserved area) * | | | | |
| 000090$_H$ to 00009D$_H$ | (Reserved area) * | | | | |
| 00009E$_H$ | PACSR | Address detection control register | 00000000$_B$ | Address matching detection function | R/W |
| 00009F$_H$ | DIRR | Delay interrupt request generation/ release register | XXXXXXX0$_B$ | Delay interrupt generation module | R/W |
| 0000A0$_H$ | LPMCR | Lowe power consumption mode control register | 00011000$_B$ | Lowe power consumption mode | W,R/W |
| 0000A1$_H$ | CKSCR | Clock selection register | 11111100$_B$ | Clock | R,R/W |
| 0000A2$_H$ to 0000A7$_H$ | (Reserved area) * | | | | |
| 0000A8$_H$ | WDTC | Watchdog timer control register | XXXXX111$_B$ | Watchdog timer | R,W |
| 0000A9$_H$ | TBTC | Time-base timer control register | 1XX00100$_B$ | Time-base timer | R/W,W |
| 0000AA$_H$ | WTC | Clock timer control register | 1X001000$_B$ | Clock timer | R,R/W |
| 0000AB$_H$ to 0000AD$_H$ | (Reserved area) * | | | | |

*(Continued)*

| Address | Register abbreviation | Register name | Reset value | Peripheral function name | Read/ Write |
|---|---|---|---|---|---|
| 0000AE$_H$ | FMCS | Flash memory control status register | 000X0000$_B$ | 512 k-bit flash memory | R,W,R/W |
| 0000AF$_H$ | (Reserved area) * | | | | |
| 0000B0$_H$ | ICR00 | Interrupt control register 00 | 00000111$_B$ | Interrupt controller | R/W |
| 0000B1$_H$ | ICR01 | Interrupt control register 01 | 00000111$_B$ | | |
| 0000B2$_H$ | ICR02 | Interrupt control register 02 | 00000111$_B$ | | |
| 0000B3$_H$ | ICR03 | Interrupt control register 03 | 00000111$_B$ | | |
| 0000B4$_H$ | ICR04 | Interrupt control register 04 | 00000111$_B$ | | |
| 0000B5$_H$ | ICR05 | Interrupt control register 05 | 00000111$_B$ | | |
| 0000B6$_H$ | ICR06 | Interrupt control register 06 | 00000111$_B$ | | |
| 0000B7$_H$ | ICR07 | Interrupt control register 07 | 00000111$_B$ | | |
| 0000B8$_H$ | ICR08 | Interrupt control register 08 | 00000111$_B$ | | |
| 0000B9$_H$ | ICR09 | Interrupt control register 09 | 00000111$_B$ | | |
| 0000BA$_H$ | ICR10 | Interrupt control register 10 | 00000111$_B$ | | |
| 0000BB$_H$ | ICR11 | Interrupt control register 11 | 00000111$_B$ | | |
| 0000BC$_H$ | ICR12 | Interrupt control register 12 | 00000111$_B$ | | |
| 0000BD$_H$ | ICR13 | Interrupt control register 13 | 00000111$_B$ | | |
| 0000BE$_H$ | ICR14 | Interrupt control register 14 | 00000111$_B$ | | |
| 0000BF$_H$ | ICR15 | Interrupt control register 15 | 00000111$_B$ | | |
| 0000C0$_H$ to 0000FF$_H$ | (Reserved area) * | | | | |
| 001FF0$_H$ | PADR0 | Detection address setting register 0 (low-order) | XXXXXXXX$_B$ | Address matching detection function | R/W |
| 001FF1$_H$ | | Detection address setting register 0 (middle-order) | XXXXXXXX$_B$ | | |
| 001FF2$_H$ | | Detection address setting register 0 (high-order) | XXXXXXXX$_B$ | | |
| 001FF3$_H$ | PADR1 | Detection address setting register 1 (low-order) | XXXXXXXX$_B$ | | R/W |
| 001FF4$_H$ | | Detection address setting register 1 (middle-order) | XXXXXXXX$_B$ | | |
| 001FF5$_H$ | | Detection address setting register 1 (high-order) | XXXXXXXX$_B$ | | |
| 003900$_H$ | TMR0/ TMRLR0 | 16-bit timer register 0/16-bit reload register | XXXXXXXX$_B$ | 16-bit reload timer 0 | R,W |
| 003901$_H$ | | | XXXXXXXX$_B$ | | |

*(Continued)*

*(Continued)*

| Address | Register abbreviation | Register name | Reset value | Peripheral function name | Read/ Write |
|---|---|---|---|---|---|
| 003902H | TMR1/ TMRLR1 | 16-bit timer register 1/16-bit reload register | XXXXXXXXB | 16-bit reload timer 1 | R,W |
| 003903H | | | XXXXXXXXB | | |
| 003904H to 00390FH | (Reserved area) * | | | | |
| 003910H | PRLL0 | PPG0 reload register L | XXXXXXXXB | 8/16-bit PPG timer | R/W |
| 003911H | PRLH0 | PPG0 reload register H | XXXXXXXXB | | R/W |
| 003912H | PRLL1 | PPG1 reload register L | XXXXXXXXB | | R/W |
| 003913H | PRLH1 | PPG1 reload register H | XXXXXXXXB | | R/W |
| 003914H | PRLL2 | PPG2 reload register L | XXXXXXXXB | | R/W |
| 003915H | PRLH2 | PPG2 reload register H | XXXXXXXXB | | R/W |
| 003916H | PRLL3 | PPG3 reload register L | XXXXXXXXB | | R/W |
| 003917H | PRLH3 | PPG3 reload register H | XXXXXXXXB | | R/W |
| 003918H to 003BFFH | (Reserved area) * | | | | |
| 003C00H to 003C0FH | RAM (General purpose RAM) | | | | |
| 003C10H to 003FFFH | (Reserved area) * | | | | |

Reset values :

0 : Reset value of this bit is “0.”

1 : Reset value of this bit is “1.”

X : Reset value of this bit is undefined.

* : “Reserved area” should not be written anything. Result of reading from “Reserved area” is undefined.

## ■ INTERRUPT SOURCES, INTERRUPT VECTORS, AND INTERRUPT CONTROL REGISTERS

| Interrupt source | EI²OS readiness | Interrupt vector | | | Interrupt control register | | Priority*3 |
|---|---|---|---|---|---|---|---|
| | | Number | | Address | ICR | Address | |
| Reset | × | #08 | 08H | FFFFDCH | — | — | High |
| INT 9 instruction | × | #09 | 09H | FFFFD8H | — | — | ↑ |
| Exceptional treatment | × | #10 | 0AH | FFFFD4H | — | — | |
| Reserved | × | #11 | 0BH | FFFFD0H | ICR00 | 0000B0H | |
| Reserved | × | #12 | 0CH | FFFFCCH | | | |
| Reserved | × | #13 | 0DH | FFFFC8H | ICR01 | 0000B1H | |
| Reserved | × | #14 | 0EH | FFFFC4H | | | |
| Reserved | × | #15 | 0FH | FFFFC0H | ICR02 | 0000B2H | |
| Time-base timer | × | #16 | 10H | FFFFBCH | | | |
| 16-bit reload timer 0 | Δ | #17 | 11H | FFFFB8H | ICR03 | 0000B3H*1 | |
| 8/10-bit A/D converter | Δ | #18 | 12H | FFFFB4H | | | |
| 16-bit free-run timer overflow | Δ | #19 | 13H | FFFFB0H | ICR04 | 0000B4H | |
| Reserved | × | #20 | 14H | FFFFACH | | | |
| Reserved | × | #21 | 15H | FFFFA8H | ICR05 | 0000B5H | |
| PPG timer ch0, ch1 underflow | × | #22 | 16H | FFFFA4H | | | |
| Input capture 0-input | Δ | #23 | 17H | FFFFA0H | ICR06 | 0000B6H*1 | |
| External interrupt (INT4/INT5) | Δ | #24 | 18H | FFFF9CH | | | |
| Input capture 1-input | Δ | #25 | 19H | FFFF98H | ICR07 | 0000B7H*2 | |
| PPG timer ch2, ch3 underflow | × | #26 | 1AH | FFFF94H | | | |
| External interrupt (INT6/INT7) | Δ | #27 | 1BH | FFFF90H | ICR08 | 0000B8H*1 | |
| Clock timer | Δ | #28 | 1CH | FFFF8CH | | | |
| Reserved | × | #29 | 1DH | FFFF88H | ICR09 | 0000B9H | |
| Input capture 2-input<br>Input capture 3-input | × | #30 | 1EH | FFFF84H | | | |
| Reserved | × | #31 | 1FH | FFFF80H | ICR10 | 0000BAH | |
| Reserved | × | #32 | 20H | FFFF7CH | | | |
| Reserved | × | #33 | 21H | FFFF78H | ICR11 | 0000BBH | |
| Reserved | × | #34 | 22H | FFFF74H | | | |
| Reserved | × | #35 | 23H | FFFF70H | ICR12 | 0000BCH | ↓ |
| 16-bit reload timer 1 | ○ | #36 | 24H | FFFF6CH | | | Low |

*(Continued)*

*(Continued)*

| Cause of interrupt | EI²OS readiness | Interrupt vector | | | Interrupt control register | | Priority*3 |
|---|---|---|---|---|---|---|---|
| | | Number | | Address | ICR | Address | |
| UART1 reception completed | ◎ | #37 | 25H | FFFF68H | ICR13 | 0000BDH*1 | High ↑ |
| UART1 transmission completed | Δ | #38 | 26H | FFFF64H | | | |
| Reserved | × | #39 | 27H | FFFF60H | ICR14 | 0000BEH | |
| Reserved | × | #40 | 28H | FFFF5CH | | | |
| Flash memory | × | #41 | 29H | FFFF58H | ICR15 | 0000BFH | |
| Delay interrupt generation module | × | #42 | 2AH | FFFF54H | | | ↓ Low |

○ : Available

× : Unavailable

◎ : Available EI²OS function is provided.

Δ : Available when a cause of interrupt sharing a same ICR is not used.

*1: • Peripheral functions sharing an ICR register have the same interrupt level.
• If peripheral functions share an ICR register, only one function is available when using expanded intelligent I/O service (EI²OS) .
• If peripheral functions share an ICR register, a function using expanded intelligent I/O service (EI²OS) does not allow interrupt by another function.

*2: Input capture 1 is ready only for EI²OS, and PPG is not ready for EI²OS. Disable PPG interrupt when using EI²OS with Input capture 1.

*3: Priority when two or more interrupts of a same level occur simultaneously.

## ■ PERIPHERAL RESOURCES

### 1. I/O Ports

The I/O ports are used as general-purpose input/output ports (parallel I/O ports). The MB90455 series model is provided with 5 ports (34 inputs). The ports function as input/output pins for peripheral functions also.

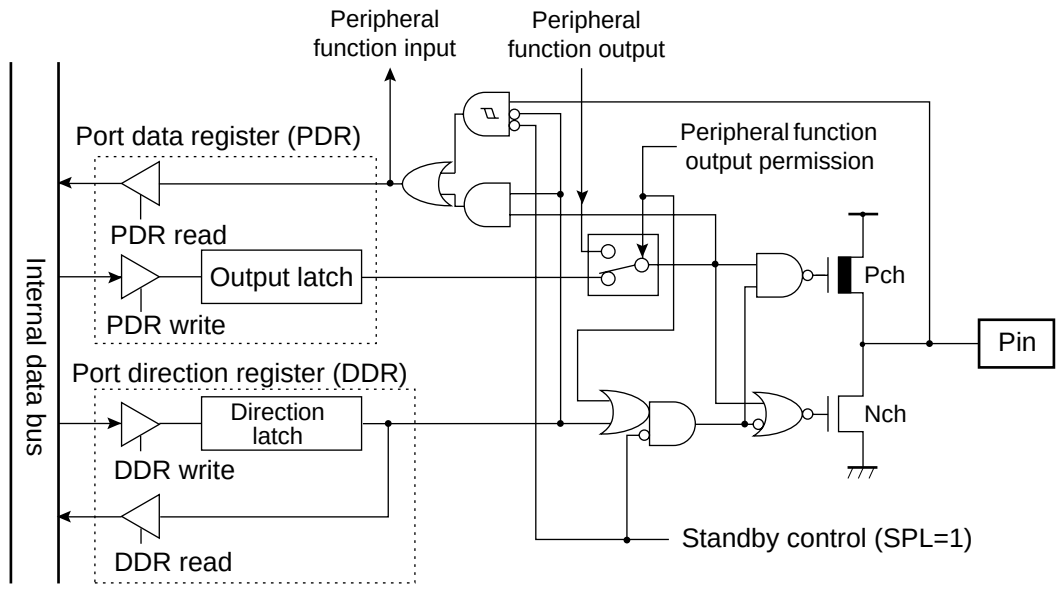
**• I/O port functions**

An I/O port, using port data resister (PDR), outputs the output data to I/O pin and input a signal input to I/O port. The port direction register (DDR) specifies direction of input/output of I/O pins on a bit-by-bit basis.

The following summarizes functions of the ports and sharing peripheral functions :

- Port 1 : General-purpose input/output port, used also for PPG timer output and input capture inputs.
- Port 2 : General-purpose input/output port, used also for reload timer input/output and external interrupt input.
- Port 3 : General-purpose input/output port, used also for A/D converter activation trigger pin.
- Port 4 : General-purpose input/output port, used also for UART input/output.
- Port 5 : General-purpose input/output port, used also analog input pin.

**• Port 1 pins block diagram (single-chip mode)**




Standby control : Control among Stop mode (SPL=1), Time-base timer mode (SPL=1), and clock mode (SPL=1).

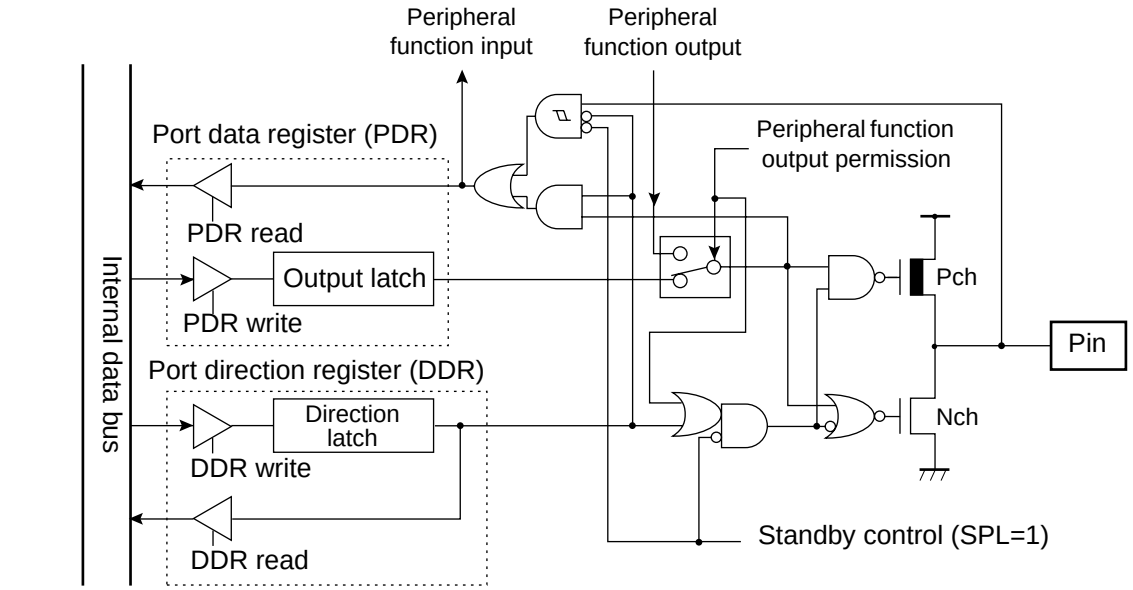
**• Port 1 registers (single-chip mode)**

- Port 1 registers include port 1 data register (PDR1) and port 1 direction register (DDR1).
- The bits configuring the register correspond to port 1 pins on a one-to-one basis.

**Relation between port 1 registers and pins**

| Port name | Bits of register and corresponding pins | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Port 1 | PDR1, DDR1 | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
| | Corresponding pins | P17 | P16 | P15 | P14 | P13 | P12 | P11 | P10 |

• **Port 2 pins block diagram (general-purpose input/output port)**




Standby control : Control among Stop mode (SPL=1), Time-base timer mode (SPL=1), and clock mode (SPL=1).

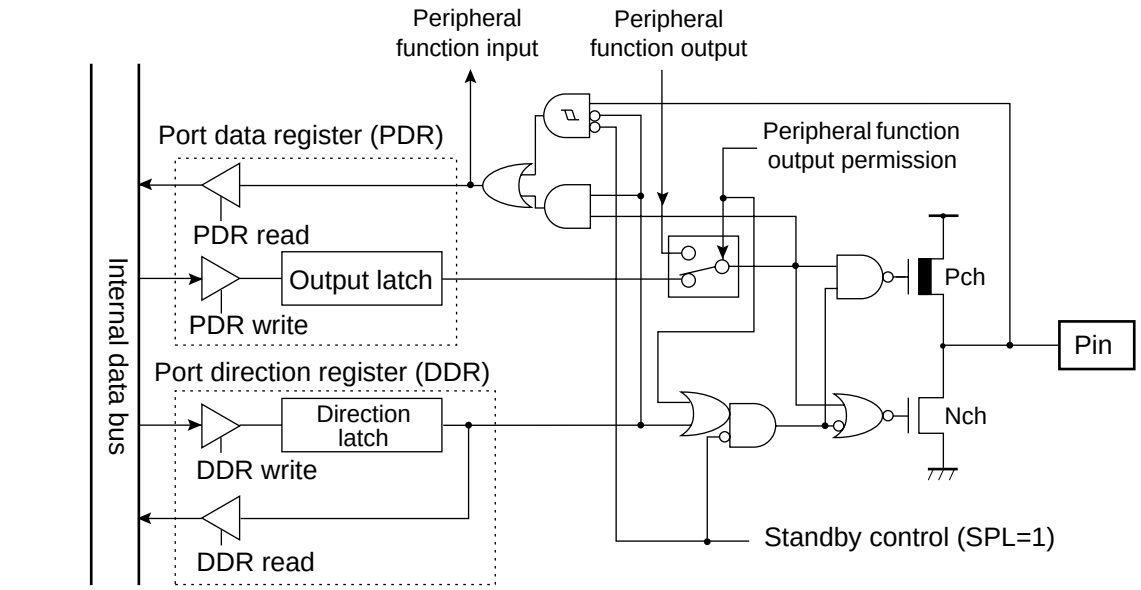
• **Port 2 registers**

- Port 2 registers include port 2 data register (PDR2) and port 2 direction register (DDR2).
- The bits configuring the register correspond to port 2 pins on a one-to-one basis.

**Relation between port 2 registers and pins**

| Port name | Bits of register and corresponding pins | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Port 2 | PDR2,DDR2 | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
| | Corresponding pins | P27 | P26 | P25 | P24 | P23 | P22 | P21 | P20 |

● **Port 3 pins block diagram (general-purpose input/output port)**




Standby control : Control among Stop mode (SPL=1), Time-base timer mode (SPL=1), and clock mode (SPL=1).

● **Port 3 registers**

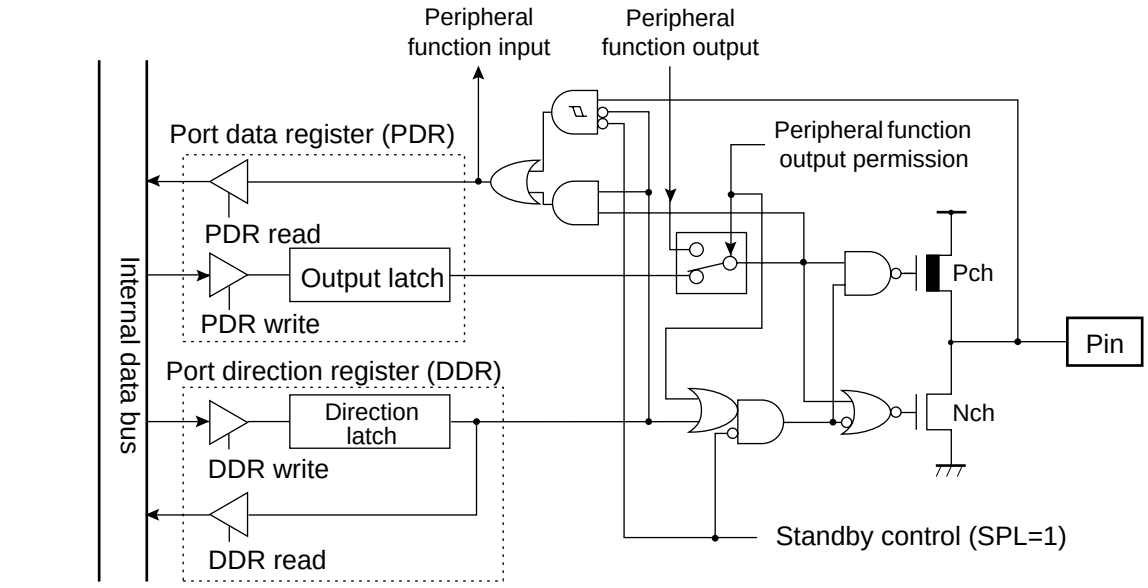
- Port 3 registers include port 3 data register (PDR3) and port 3 direction register (DDR3).
- The bits configuring the register correspond to port 3 pins on a one-to-one basis.

**Relation between port 3 registers and pins**

| Port name | Bits of register and corresponding pins | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Port 3 | PDR3, DDR3 | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
| | Corresponding pins | P37 | P36* | P35* | — | P33 | P32 | P31 | P30 |

* : P35 and P36 do not exist on MB90F455/F456/F457, and MB90455/456/457.

• **Port 4 pins block diagram**




Standby control : Control among Stop mode (SPL=1), Time-base timer mode (SPL=1), and clock mode (SPL=1).

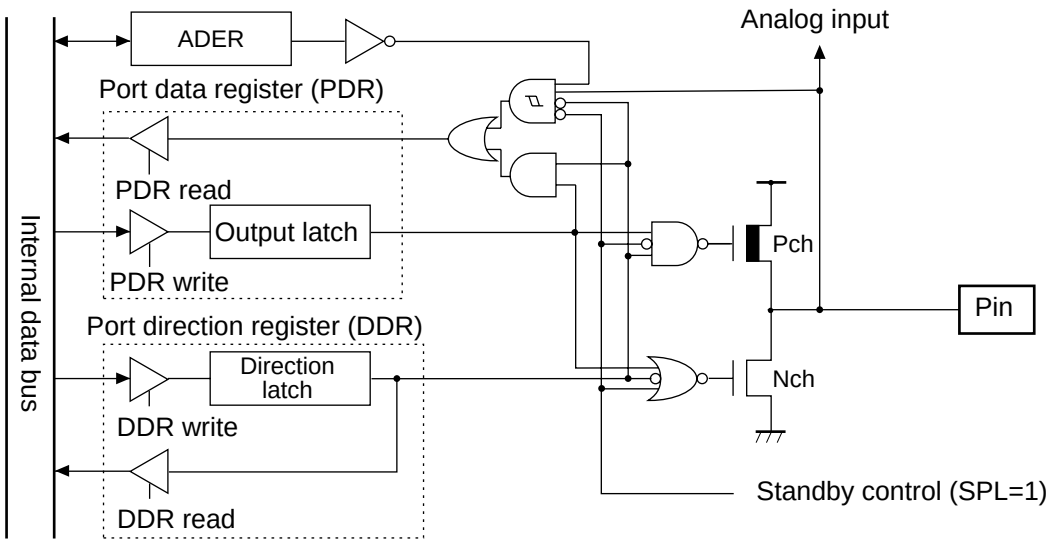
• **Port 4 registers**

- Port 4 registers include port 4 data register (PDR4) and port 4 direction register (DDR4).
- The bits configuring the register correspond to port 4 pins on a one-to-one basis.

**Relation between port 4 registers and pins**

| Port name | Bits of register and corresponding pins | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Port 4 | PDR4, DDR4 | — | — | — | bit4 | bit3 | bit2 | bit1 | bit0 |
| | Corresponding pins | — | — | — | P44 | P43 | P42 | P41 | P40 |

• **Port 5 pins block diagram**




Standby control: Control among Stop mode (SPL=1), Time-base timer mode (SPL=1), and clock mode (SPL=1).

• **Port 5 registers**

- Port 5 registers include port 5 data register (PDR5), port 5 direction register (DDR5), and analog input permission register (ADER).
- Analog input permission register (ADER) allows or disallows input of analog signal to the analog input pin.
- The bits configuring the register correspond to port 5 pins on a one-to-one basis.

**Relation between port 5 registers and pins**

| Port name | Bits of register and corresponding pins | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Port 5 | PDR5, DDR5 | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
| | ADER | ADE7 | ADE6 | ADE5 | ADE4 | ADE3 | ADE2 | ADE1 | ADE0 |
| | Corresponding pins | P57 | P56 | P55 | P54 | P53 | P52 | P51 | P50 |

## 2. Time-Base Timer

The time-base time is a 18-bit free-run counter (time-base timer counter) that counts up in synchronization with the main clock (dividing main oscillation clock by 2).

- Four choices of interval time are selectable, and generation of interrupt request is allowed for each interval time.
- Provides operation clock signal to oscillation stabilizing wait timer and peripheral functions.

**• Interval timer function**

- When the counter of time-base timer reaches an interval time specified by interval time selection bit (TBTC:TBC1, TBC0), an overflow (carrying-over) occurs (TBTC: TBOF=1) and interrupt request is generated.
- If an interrupt by overflow is permitted (TBTC: TBIE=1), an interrupt is generated when overflow occurs (TBTC: TBOF=1).
- The following four interval time settings are selectable :

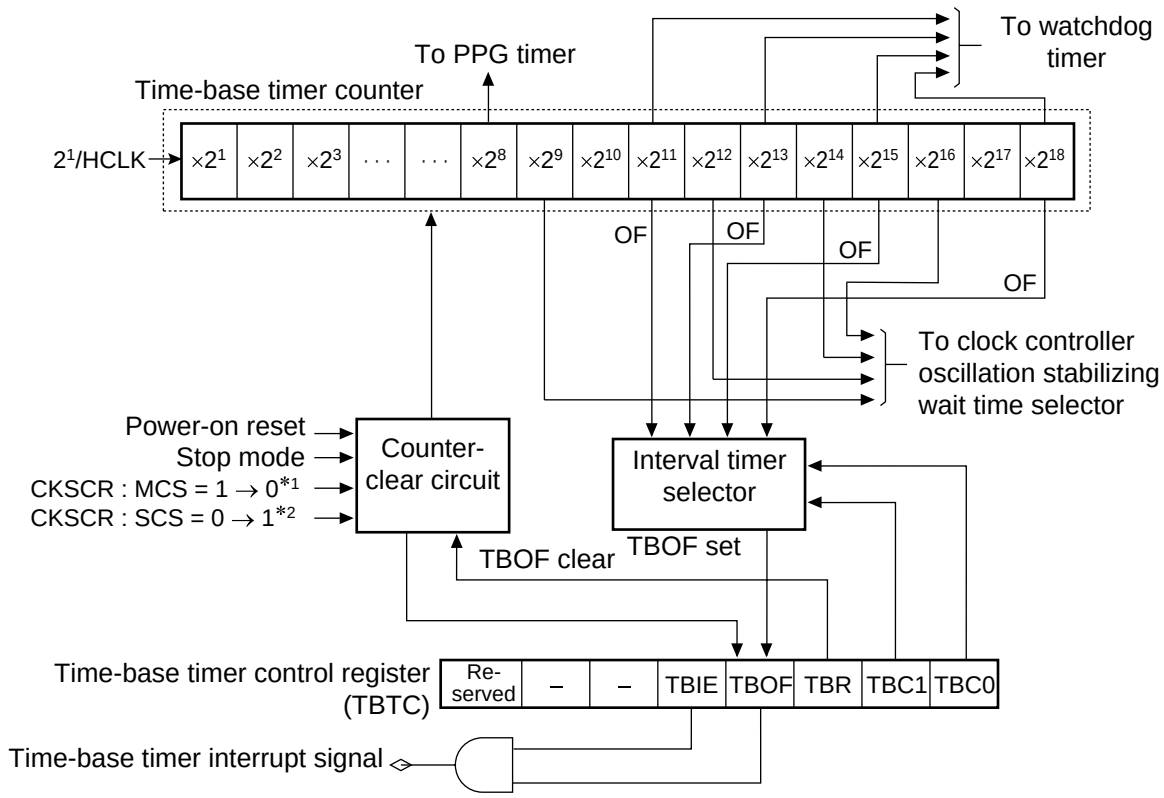
**Interval time of time-base timer**

| Count clock | Interval time |
|---|---|
| 2/HCLK (0.5 μs) | $2^{12}$/HCLK (Approx. 1.0 ms) |
| | $2^{14}$/HCLK (Approx. 4.1 ms) |
| | $2^{16}$/HCLK (Approx. 16.4 ms) |
| | $2^{19}$/HCLK (Approx. 131.1 ms) |

HCLK: Oscillation clock

Values in parentheses “( )” are those under operation of 4-MHz oscillation clock.

• **Time-base timer block diagram**




OF : Overflow
HCLK : Oscillation clock

*1 : Switch machine clock from main clock to PLL clock.

*2 : Switch machine clock from sub clock to main clock.

Actual interrupt request number of time-base timer is as follows:

Interrupt request number: #16 ($10_H$)

## 3. Watchdog Timer

The watchdog timer is a 2-bit counter that uses time-base timer or clock timer as count clock. If the counter is not cleared within an interval time, CPU is reset.

**• Watchdog timer functions**

- The watchdog timer is a timer counter that prevents runaway of a program. Once a watchdog timer is activated, the counter of watchdog timer must always be cleared within a specified time of interval. If specified interval time elapses without clearing the counter of a watchdog timer, CPU resetting occurs. This is the function of a watchdog timer.
- The interval time of a watchdog timer is determined by a clock cycle, which is input as a count clock. Watchdog resetting occurs between a minimum time and a maximum time specified.
- The output target of a clock source is specified by the watchdog clock selection bit (WTC: WDCS) in the clock timer control register.
- Interval time of a watchdog timer is specified by the time-base timer output selection bit/clock timer output selection bit (WDTC: WT1, WT0) in the watchdog timer control register.

**Interval timer of watchdog timer**

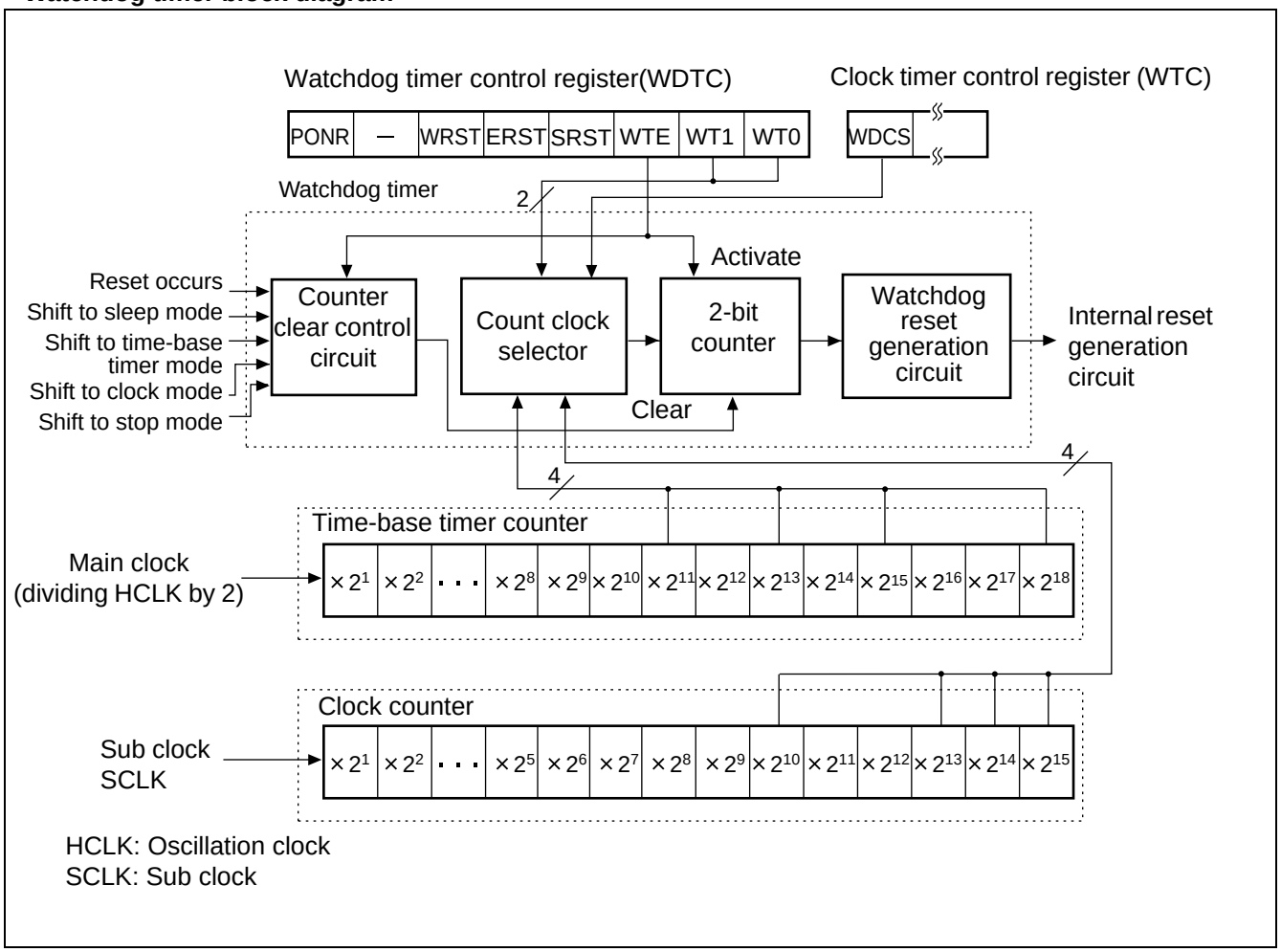
| Min | Max | Clock cycle | Min | Max | Clock cycle |
|---|---|---|---|---|---|
| Approx. 3.58 ms | Approx. 4.61 ms | $2^{14} \pm 2^{11}$ /HCLK | Approx. 0.457 s | Approx. 0.576 s | $2^{12} \pm 2^{9}$ /SCLK |
| Approx. 14.33 ms | Approx. 18.3 ms | $2^{16} \pm 2^{13}$ /HCLK | Approx. 3.584 s | Approx. 4.608 s | $2^{15} \pm 2^{12}$ /SCLK |
| Approx. 57.23 ms | Approx. 73.73 ms | $2^{18} \pm 2^{15}$ /HCLK | Approx. 7.168 s | Approx. 9.216 s | $2^{16} \pm 2^{13}$ /SCLK |
| Approx. 458.75 ms | Approx. 589.82 ms | $2^{21} \pm 2^{18}$ /HCLK | Approx. 14.336 s | Approx. 18.432 s | $2^{17} \pm 2^{14}$ /SCLK |

HCLK: Oscillation clock ( 4 MHz) , CSCLK: Sub clock (8.192 kHz)

Notes: • If the time-base timer is cleared when watchdog timer count clock is used as time base timer output (carry-over signal), watchdog reset time may become longer.

• When using the sub clock as machine clock, be sure to specify watchdog timer clock source selection bit (WDCS) in clock timer control register (WTC) at “0,” selecting output of clock timer.

• **Watchdog timer block diagram**



## 4. 16-bit Input/Output Timer

The 16-bit input/output timer is a compound module composed of 16-bit free-run timer, (1 unit) and input capture (2 units, 4 input pins). The timer, using the 16-bit free-run timer as a basis, enables measurement of clock cycle of an input signal and its pulse width.

### • Configuration of 16-bit input/output timer

The 16-bit input/output timer is composed of the following modules:

- 16-bit free-run timer (1 unit)
- Input capture (2 units, 2 input pins per unit)

### • Functions of 16-bit input/output timer

#### (1) Functions of 16-bit free-run timer

The 16-bit free-run timer is composed of 16-bit up counter, timer counter control status register, and prescaler. The 16-bit up counter increments in synchronization with dividing ratio of machine clock.

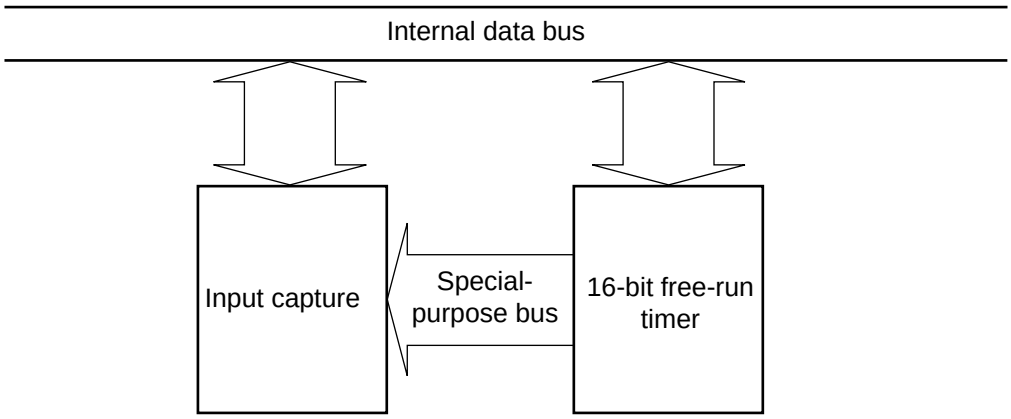
- Count clock is set among four types of machine clock dividing rates.
- Generation of interrupt is allowed by counter value overflow.
- Activation of expanded intelligent I/O service (EI$^2$OS) is allowed by interrupt generation.
- Counter value of 16-bit free-run timer is cleared to "0000$_H$" by either resetting or software-clearing with timer count clear bit (TCCS: CLR).
- Counter value of 16-bit free-run timer is output to input capture, which is available as base time for capture operation.

#### (2) Functions of input capture

The input capture, upon detecting an edge of a signal input to the input pin from external device, stores a counter value of 16-bit free-run timer at the time of detection into the input capture data register. The function includes the input capture data registers corresponding to four input pins, input capture control status register, and edge detection circuit.

- Rising edge, falling edge, and both edge are selectable for detection.
- Generating interrupt on CPU is allowed by detecting an edge of input signal.
- Expanded intelligent I/O service (EI$^2$OS) is activated by interrupt generation.
- The four input capture input pins and input capture data registers allows monitoring of a maximum of four events.

• **16-bit input/output timer block diagram**



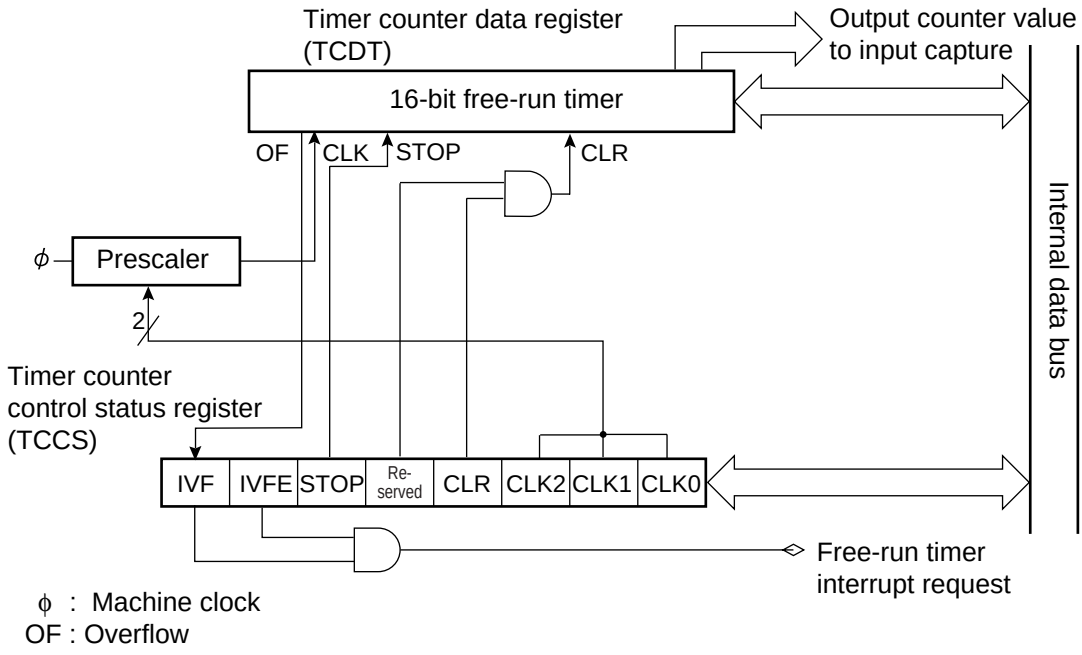

• **16-bit free-run timer**

Counter value of 16-bit free-run timer is used as reference time (base time) of input capture.

• **Input capture**

Input capture detects rising edge, falling edge or both edges and retains a counter value of 16-bit free-run timer. Detection of edge on input signal is allowed to generate interrupt.

• **16-bit free-run timer block diagram**



● **Detailed pin assignment on block diagram**

The 16-bit input/output timer includes a 16-bit free-run timer. Interrupt request number of the 16-bit free-run timer is as follows:
Interrupt request number: 19 ($13_H$)

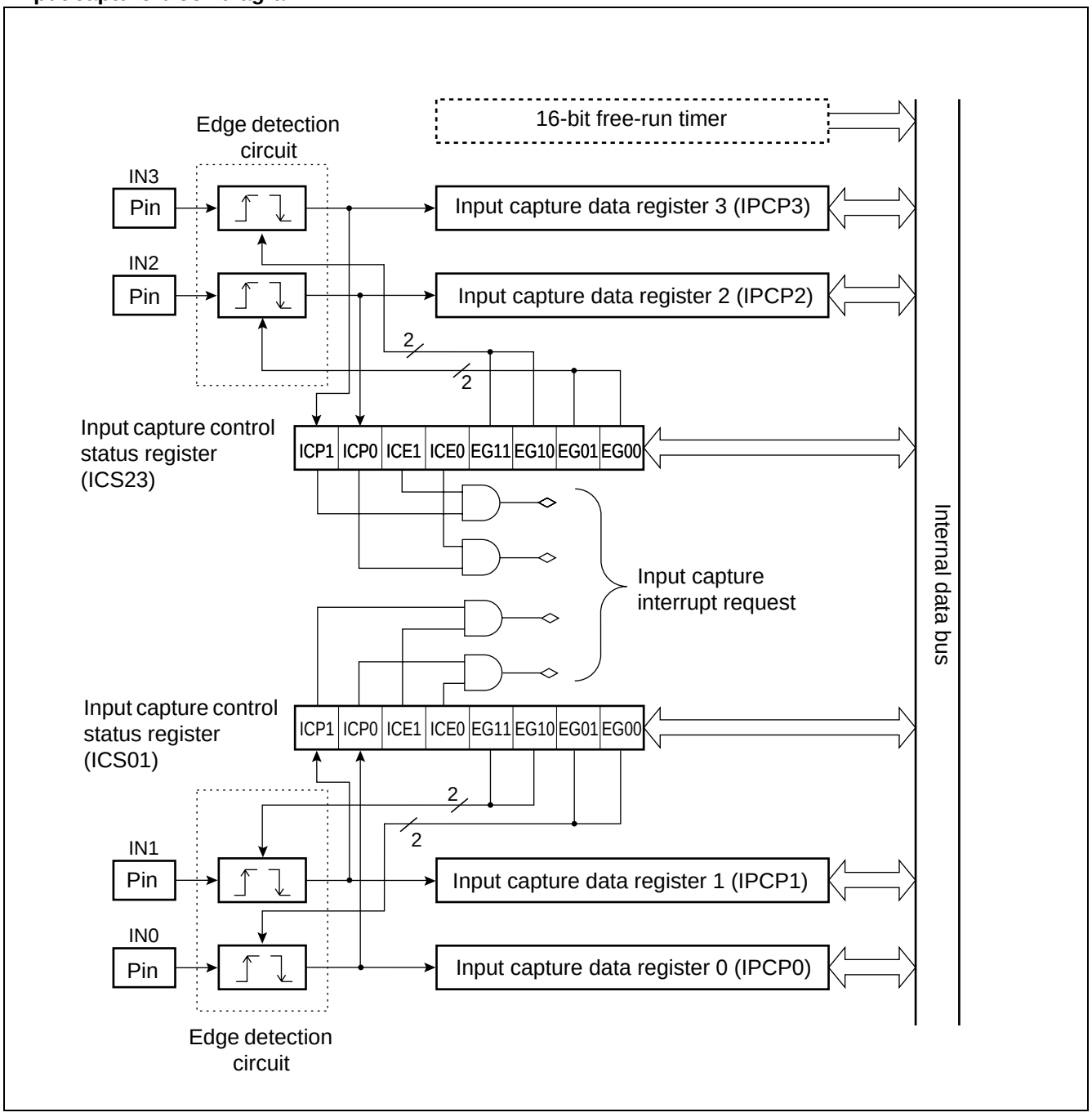
● **Prescaler**

The prescaler divides a machine clock and provides a counter clock to the 16-bit up counter. Dividing ratio of the machine clock is specified by timer counter control status register (TCCS) among four values.

● **Timer counter data register (TCDT)**

The timer counter data register is a 16-bit up counter. A current counter value of the 16-bit free-run timer is read. Writing a value during halt of the counter allows setting an arbitrary counter value.

**•Input capture block diagram**



## 5. 16-bit Reload Timer

The 16-bit reload timer has the following functions:

- Count clock is selectable among 3 internal clocks and external event clock.
- Activation trigger is selectable between software trigger and external trigger.
- Generation of CPU interrupt is allowed upon occurrence of underflow on 16-bit timer register. Available as an interval timer using the interrupt function.
- When underflow of 16-bit timer register (TMR) occurs, one of two reload modes is selectable between one-shot mode that halts counting operation of TMR, and reload mode that reloads 16-bit reload register value to TMR, continuing TMR counting operation.
- The 16-bit reload timer is ready for expanded intelligent I/O service (EI$^2$OS).
- MB90455 series device has 2 channels of built-in 16-bit reload timer.

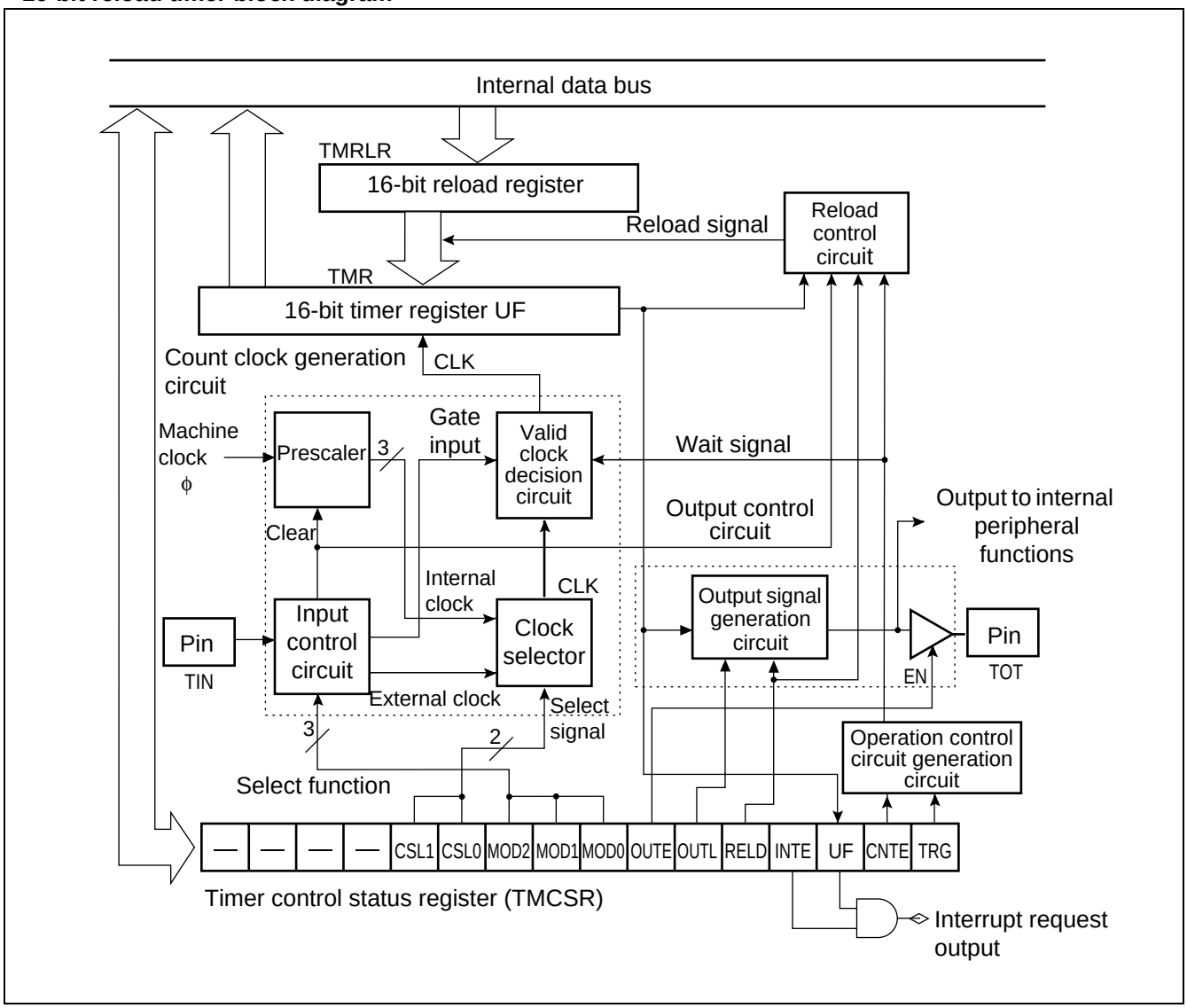
**• Operation mode of 16-bit reload timer**

| Count clock | Activation trigger | Operation upon underflow |
|---|---|---|
| Internal clock mode | Software trigger, external trigger | One-shot mode, reload mode |
| Event count mode | Software trigger | One-shot mode, reload mode |

**• Internal clock mode**

- The 16-bit reload timer is set to internal clock mode, by setting count clock selection bit (TMCSR: CSL1, CSL0) to “$00_B$”, “$01_B$”, “$10_B$”.
- In the internal clock mode, the counter decrements in synchronization with the internal clock.
- Three types of count clock cycles are selectable by count clock selection bit (TMCSR: CSL1, CSL0) in timer control status register.
- Edge detection of software trigger or external trigger is specified as an activation trigger.

• **16-bit reload timer block diagram**



## 6. Clock Timer Outline

The clock timer is a 15-bit free-run counter that increments in synchronization with sub clock.

- Interval time is selectable among 7 choices, and generation of interrupt request is allowed for each interval.
- Provides operation clock to the subclock oscillation stabilizing wait timer and watchdog timer.
- Always uses subclock as a count clock regardless of settings of clock selection register (CKSCR).

**• Interval timer function**

- In the clock timer, a bit corresponding to the interval time overflows (carry-over) when an interval time, which is specified by interval time selection bit, is reached. Then overflow flag bit is set (WTC: WTOF=1).
- If an interrupt by overflow is permitted (WTC: WTIE=1), an interrupt request is generated upon setting an overflow flag bit.
- Interval time of clock timer is selectable among the following seven choices :

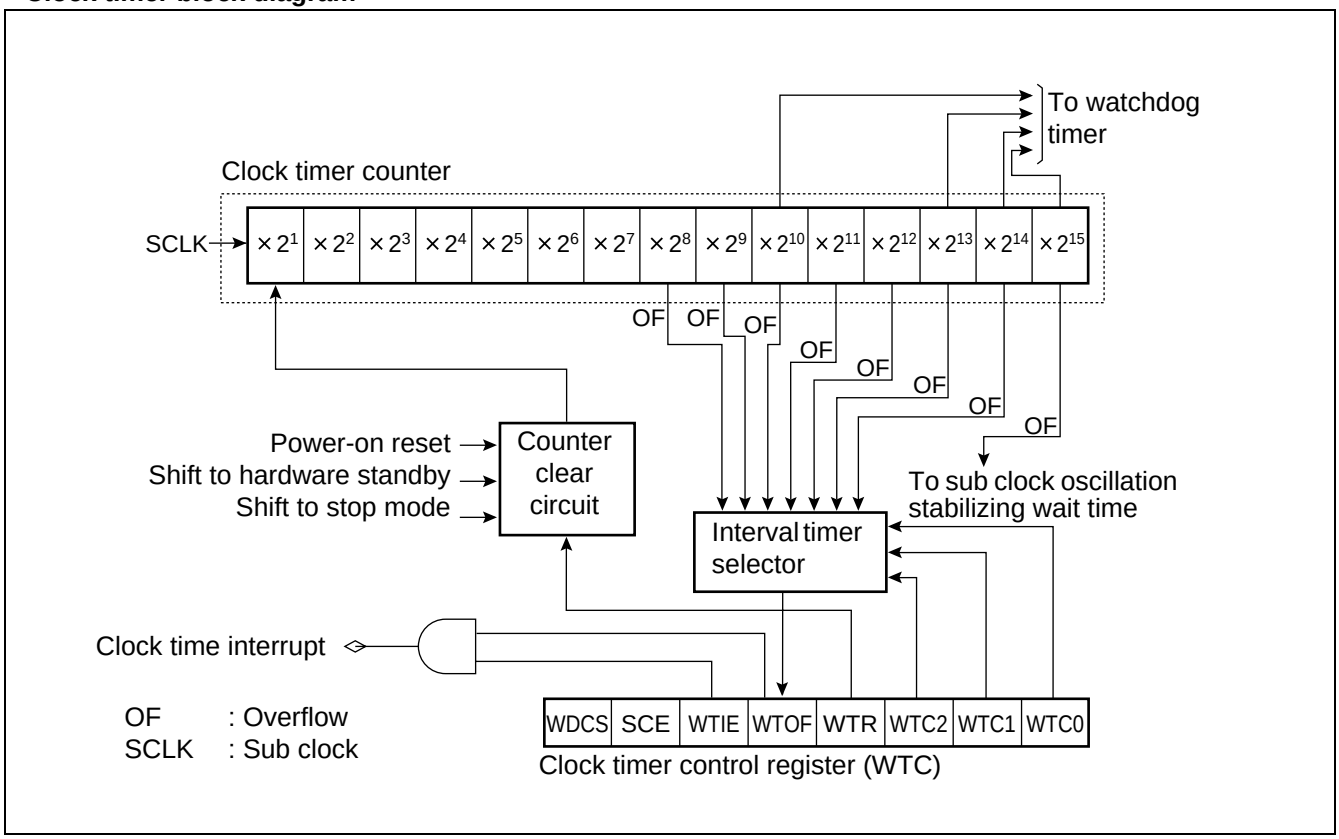
**• Interval time of clock timer**

| Sub clock cycle | Interval time |
|---|---|
| SCLK (122 μs) | $2^8$/SCLK (31.25 ms) |
| | $2^9$/SCLK (62.5 ms) |
| | $2^{10}$/SCLK (125 ms) |
| | $2^{11}$/SCLK (250 ms) |
| | $2^{12}$/SCLK (500 ms) |
| | $2^{13}$/SCLK (1.0 s) |
| | $2^{14}$/SCLK (2.0 s) |

SCLK: Sub clock frequency

Values in parentheses “( )” are calculation when operating with 8.192 kHz clock.

• **Clock timer block diagram**




Actual interrupt request number of clock timer is as follows :

Interrupt request number : #28 ($1C_H$)

• **Clock timer counter**

A 15-bit up counter that uses sub clock (SCLK) as a count clock.

• **Counter clear circuit**

A circuit that clears the clock timer counter.

## 7. 8/16-bit PPG Timer Outline

The 8/16-bit PPG timer is a 2-channel reload timer module (PPG0 and PPG1) that allows outputting pulses of arbitrary cycle and duty cycle. Combination of the two channels allows selection among the following operations:

- 8-bit PPG output 2-channel independent operation mode
- 16-bit PPG output operation mode
- 8-bit and 8-bit PPG output operation mode

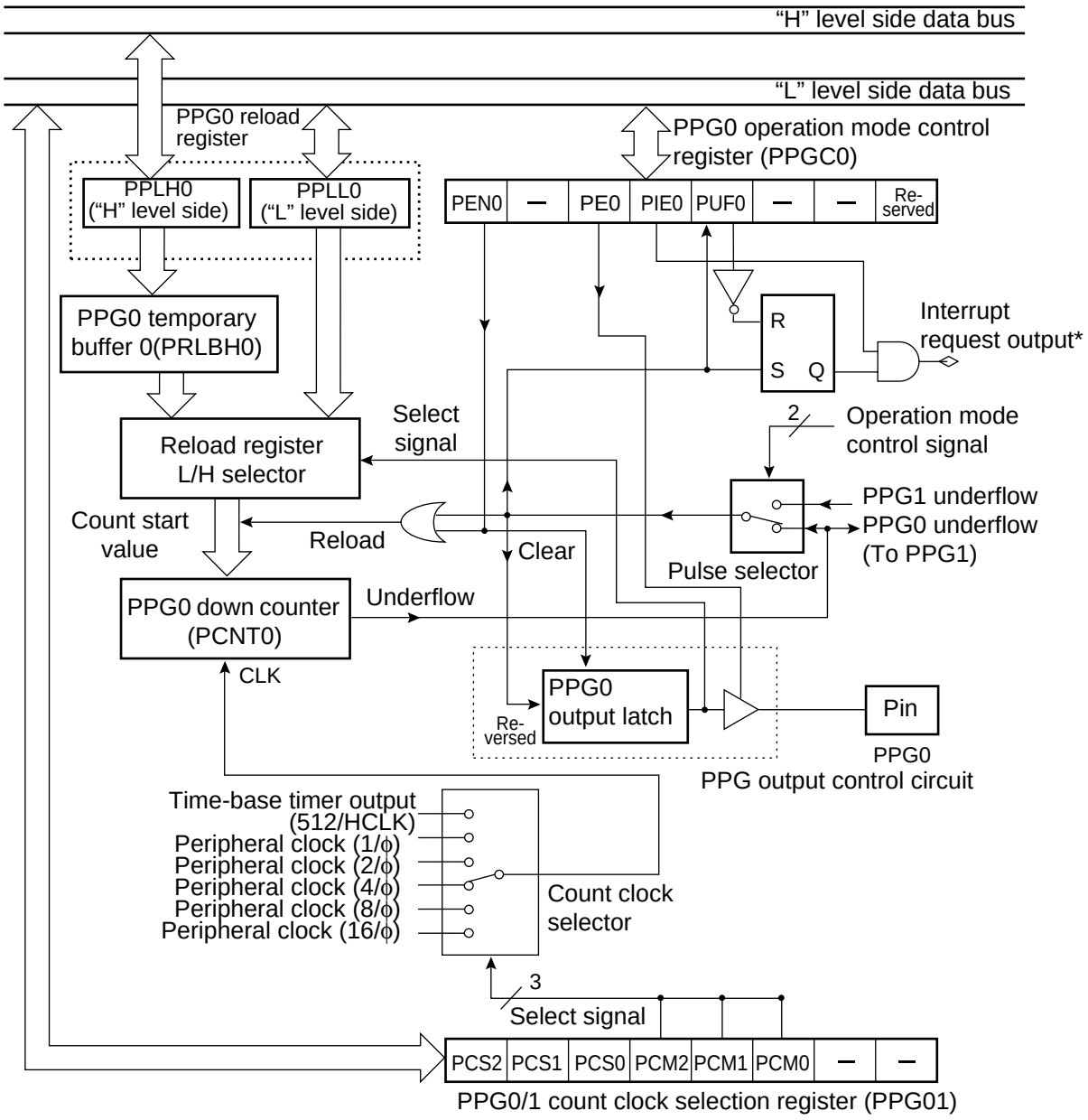
MB90455 series device has two 8/16-bit built-in PPG timers. This section describes functions of PPG0/1. PPG2/3 have the same functions as those of PPG0/1.

**• Functions of 8/-16-bit PPG timer**

The 8/-16-bit PPG timer is composed of four 8-bit reload register (PRLH0/PRLL0, PRLH1/PRLL1) and two PPG down counters (PCNT0, PCNT1).

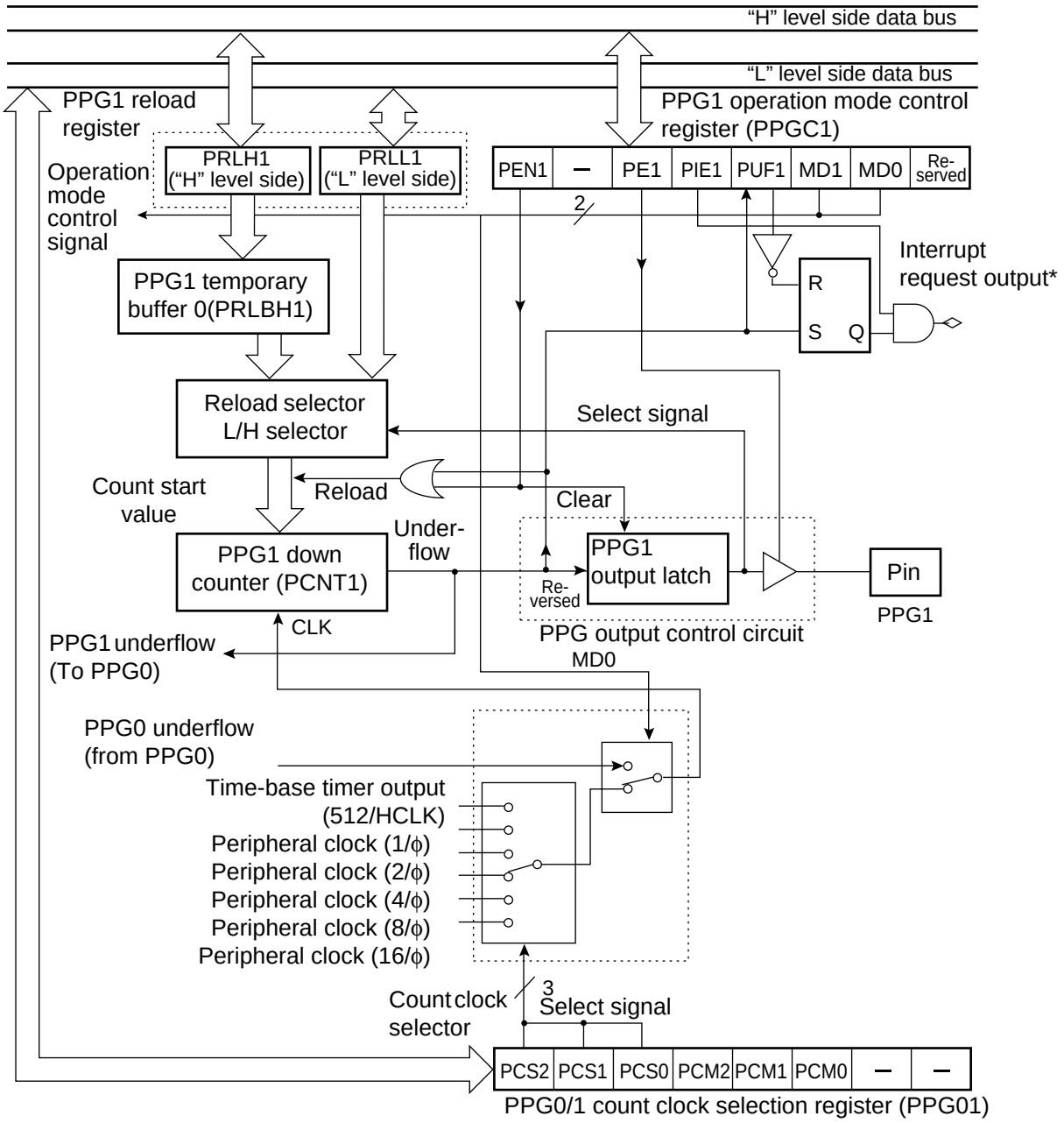
- Widths of “H” and “L” in output pulse are specifiable independently. Cycle and duty factor of output pulse is specifiable arbitrarily.
- Count clock is selectable among 6 internal clocks.
- The timer is usable as an interval timer, by generating interrupt requests for each interval.
- The time is usable as a D/A converter, with an external circuit.

• **8/16-bit PPG timer0 block diagram**




– : Undefined
Reserved : Reserved bit
HCLK : Oscillation clock frequency
ϕ : Machine clock frequency
* : Interrupt output of 8/16-bit PPG timer 0 is incorporated into one by the OR circuit against interrupt output of 8/16-bit PPG timer 1.

• **8/16-bit PPG timer 1 block diagram**




– : Undefined
Reserved : Reserved bit
HCLK : Oscillation clock frequency
ϕ : Machine clock frequency
* : Interrupt output of 8/16-bit PPG timer 1 is incorporated into one by the OR circuit against interrupt output of 8/16-bit PPG timer 0.

## 8. Delay Interrupt Generation Module Outline

The delay interrupt generation module is a module that generates interrupts for switching tasks. Generation of a hardware interrupt request is performed by software.

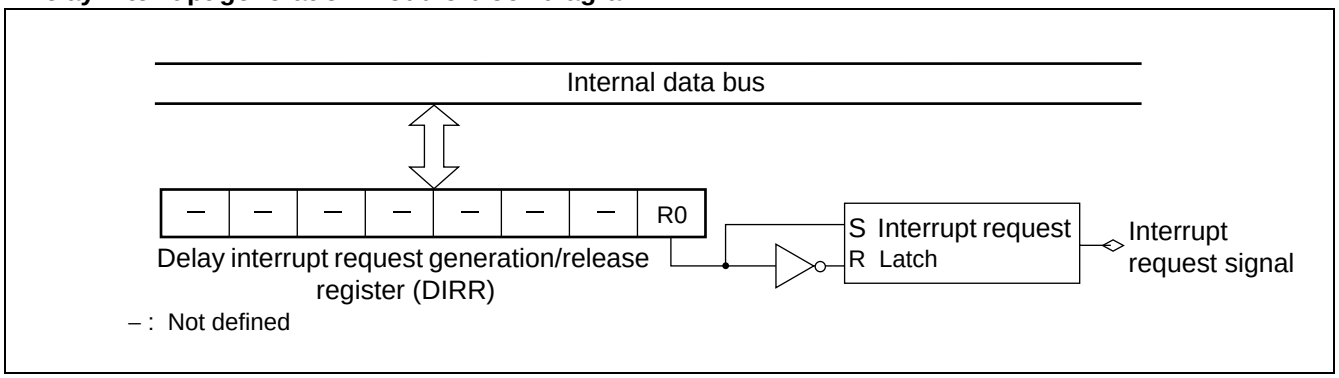
**• Delay interrupt generation module outline**

Using the delay interrupt generation module, hardware interrupt request is generated and released by software.

**Delay interrupt generation module outline**

| | Function and control |
|---|---|
| Cause of interrupt | Set “1” in R0 bit of delay interrupt request generation/release register (DIRR: R0=1), generating an interrupt request.<br>Set “0” in R0 bit of delay interrupt request generation/release register (DIRR: R0=0), releasing an interrupt request. |
| Interrupt number | #42 ($2A_H$) |
| Interrupt control | No setting of permission register is provided. |
| Interrupt flag | Retained in DIRR: R0 bit |
| $EI^2OS$ | Not ready for expanded intelligent I/O service. |

**• Delay interrupt generation module block diagram**




**• Interrupt request latch**

A latch that retains settings on delay interrupt request generation/release register (generation or release of delay interrupt request).

**• Delay interrupt request generation/release register (DIRR)**

Generates or releases delay interrupt request.

**• Interrupt number.**

An interrupt number used in delay interrupt generation module is as follows:

Interrupt number: #42 ($2A_H$)

## 9. DTP/External Interrupt Outline

DTP/external interrupt transfers an interrupt request generated by an external peripheral device or a data transmission request to CPU, generating external interrupt request and activating expanded intelligent I/O service.

**• DTP/external interrupt function**

An interrupt request input from external peripheral device to external input pins (INT7 to INT4), just as interrupt request of peripheral device, generates an interrupt request. The interrupt request generates an external interrupt and activates expanded intelligent I/O service (EI$^2$OS).

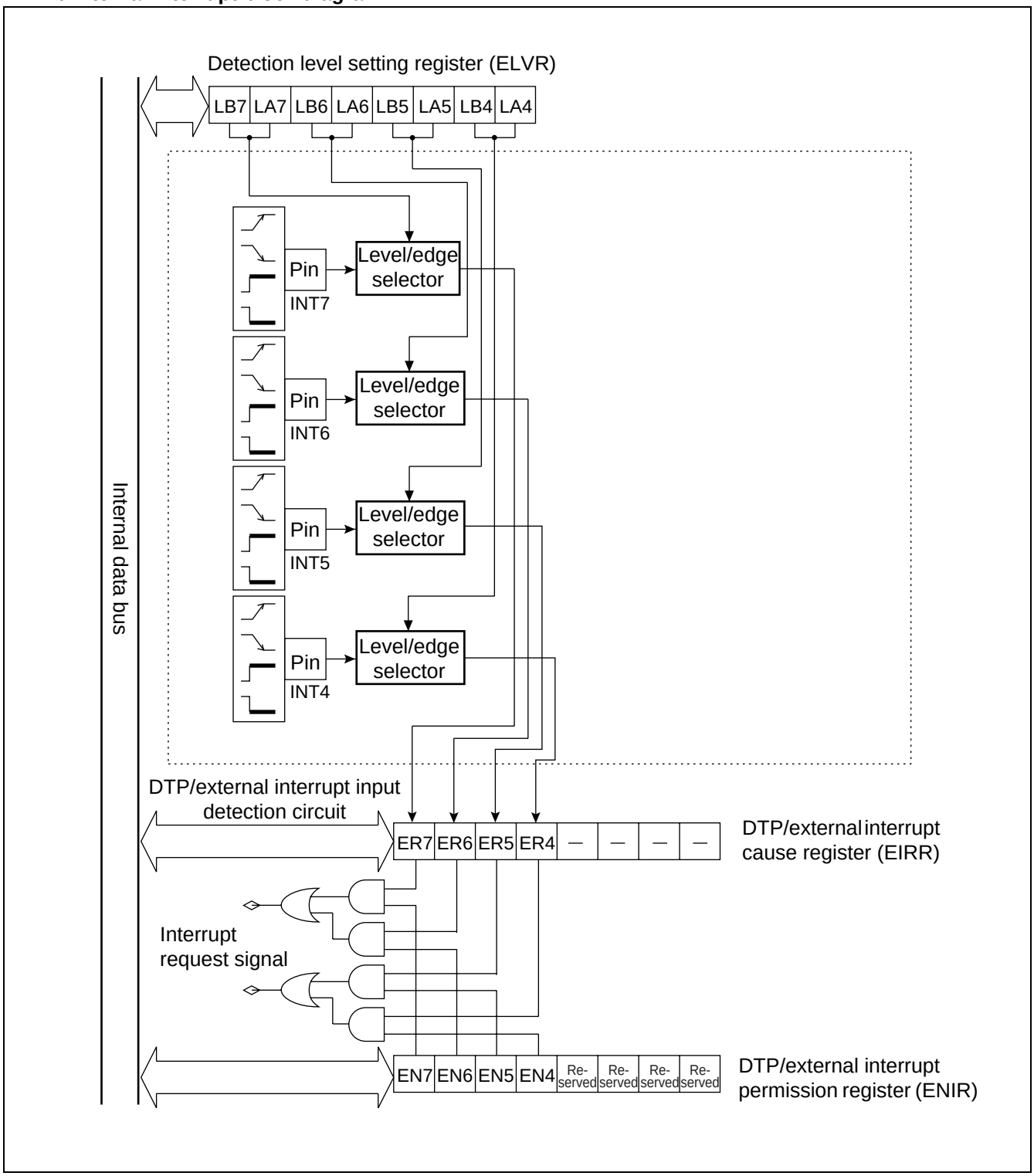
If the expanded intelligent I/O service (EI$^2$OS) has been disabled by interrupt control register (ICR: ISE=0), external interrupt function is enabled and branches to interrupt processing.

If the EI$^2$OS has been enabled, (ICR: ISE=1), DTP function is enabled and automatic data transmission is performed by EI$^2$OS. After performing specified number of data transmission processes, the process branches to interrupt processing.

**DTP/external interrupt**

| | External interrupt | DTP function |
|---|---|---|
| Input pin | 4 pins (INT4 to INT7) | |
| Interrupt cause | Specify for each pin with detection level setting register (ELVR). | |
| | Input of “H” level/“L” level/rising edge/falling edge. | Input of “H” level/ “L” level |
| Interrupt number | #24 ($18_H$) , #27 ($1B_H$) | |
| Interrupt control | Enabling or disabling output of interrupt request, using DTP/external interrupt permission register (ENIR). | |
| Interrupt flag | Retaining interrupt cause with DTP/external interrupt cause register (EIRR). | |
| Process selection | Disable EI$^2$OS (ICR: ISE=0) | Enable EI$^2$OS (ICR: ISE=1) |
| Process | Branch to external interrupt process | After automatic data transmission by EI$^2$OS for specified number of times, branch to interrupt process. |

• **DTP/External interrupt block diagram**



## 10. 8/10-bit A/D Converter

The 8/10-bit A/D converter converts an analog input voltage into 8-bit or 10/bit digital value, using the RC-type successive approximation conversion method.

- Input signal is selected among 8 channels of analog input pins.
- Activation trigger is selected among software trigger, internal timer output, and external trigger.

### • Functions of 8/10-bit A/D converter

The 8/10-bit A/D converter converts an analog voltage (input voltage) input to analog input pin into an 8-bit or 10-bit digital value (A/D conversion).

The 8/10-bit A/D converter has the following functions:

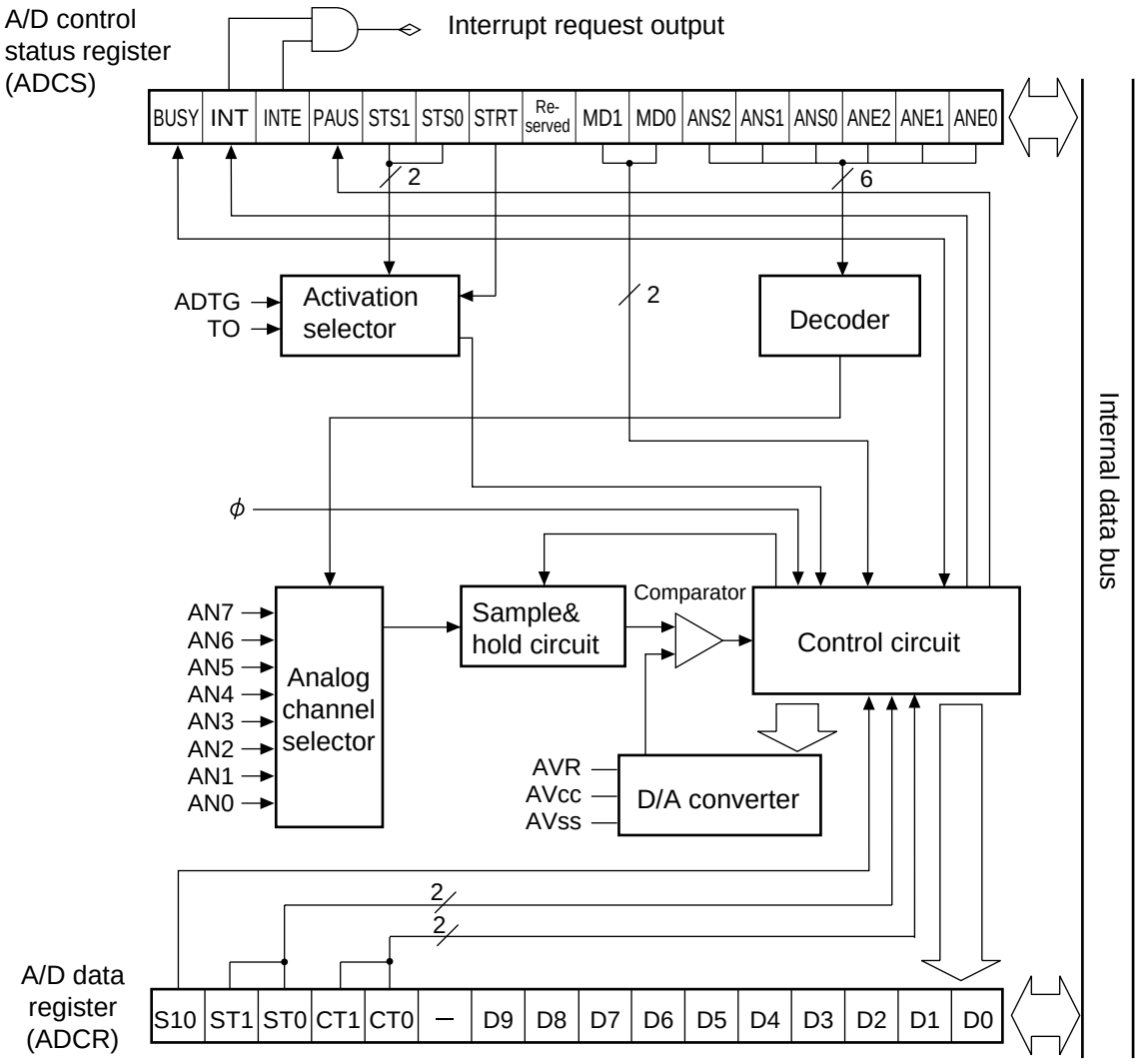
- A/D conversion takes a minimum of 6.12 µs*1 for one channel, including sampling time. (A/D conversion)
- Sampling of one channel takes a minimum of 2.0 µs*.
- RC-type successive approximation conversion method, with sample & hold circuit is used for conversion.
- Resolution of either 8 bits or 10 bits is specifiable.
- A maximum of 8 channels of analog input pins are allowed for use.
- Generation of interrupt request is allowed, by storing A/D conversion result in A/D data register.
- Activation of EI$^2$OS is allowed upon occurrence of an interrupt request. With use of EI$^2$OS, data loss is avoided even if A/D conversion is performed successively.
- An activation trigger is selectable among software trigger, internal timer output, and external trigger (fall edge).

*: When operating with 16-MHz machine clock

### • 8/10-bit A/D converter conversion mode

| Conversion mode | Description |
|---|---|
| Singular conversion mode | The A/D conversion is performed form a start channel to an end channel sequentially. Upon completion of A/D conversion on an end channel, A/D conversion function stops. |
| Sequential conversion mode | The A/D conversion is performed form a start channel to an end channel sequentially. Upon completion of A/D conversion on an end channel, A/D conversion function resumes from the start channel. |
| Pausing conversion mode | The A/D conversion is performed by pausing at each channel. Upon completion of A/D conversion on an end channel, A/D conversion and pause functions resume from the start channel. |

• **8/10-bit A/D converter block diagram**




TO : Internal timer output
– : Not defined
Reserved : Be sure to set to “0”
ϕ : Machine clock

## 11. UART Outline

UART is a general-purpose serial data communication interface for synchronous and asynchronous communication using external devices.

- Provided with bi-directional communication function for both clock-synchronous and clock-asynchronous modes.
- Provided with master/slave communication function (multi-processor mode). (Only master side is available.)
- Interrupt request is generated upon completion of reception, completion of transmission and detection of reception error.
- Ready for expanded intelligent service, EI$^2$OS.

**UART functions**

| | Description |
|---|---|
| Data buffer | Full-duplex double buffer |
| Transmission mode | Clock synchronous (No start/stop bit, no parity bit)<br>Clock asynchronous (start-stop synchronous) |
| Baud rate | Built-in special-purpose baud-rate generator. Setting is selectable among 8 values.<br>Input of external values is allowed.<br>Use of clock from external timer (16-bit reload timer 0) is allowed. |
| Data length | 7 bits (only asynchronous normal mode)<br>8 bits |
| Signaling system | Non Return to Zero (NRZ) system |
| Reception error detection | Framing error<br>Overrun error<br>Parity error (not detectable in operation mode 1 (multi-processor mode)) |
| Interrupt request | Receive interrupt (reception completed, reception error detected)<br>Transmission interrupt (transmission completed)<br>Ready for expanded intelligent I/O service (EI$^2$OS) in both transmission and reception |
| Master/slave communication function (asynchronous, multi-processor mode) | Communication between 1 (master) and n (slaves) are available (usable as master only). |

Note : Start/stop bit is not added upon clock-synchronous transmission. Data only is transmitted.

**UART operation modes**

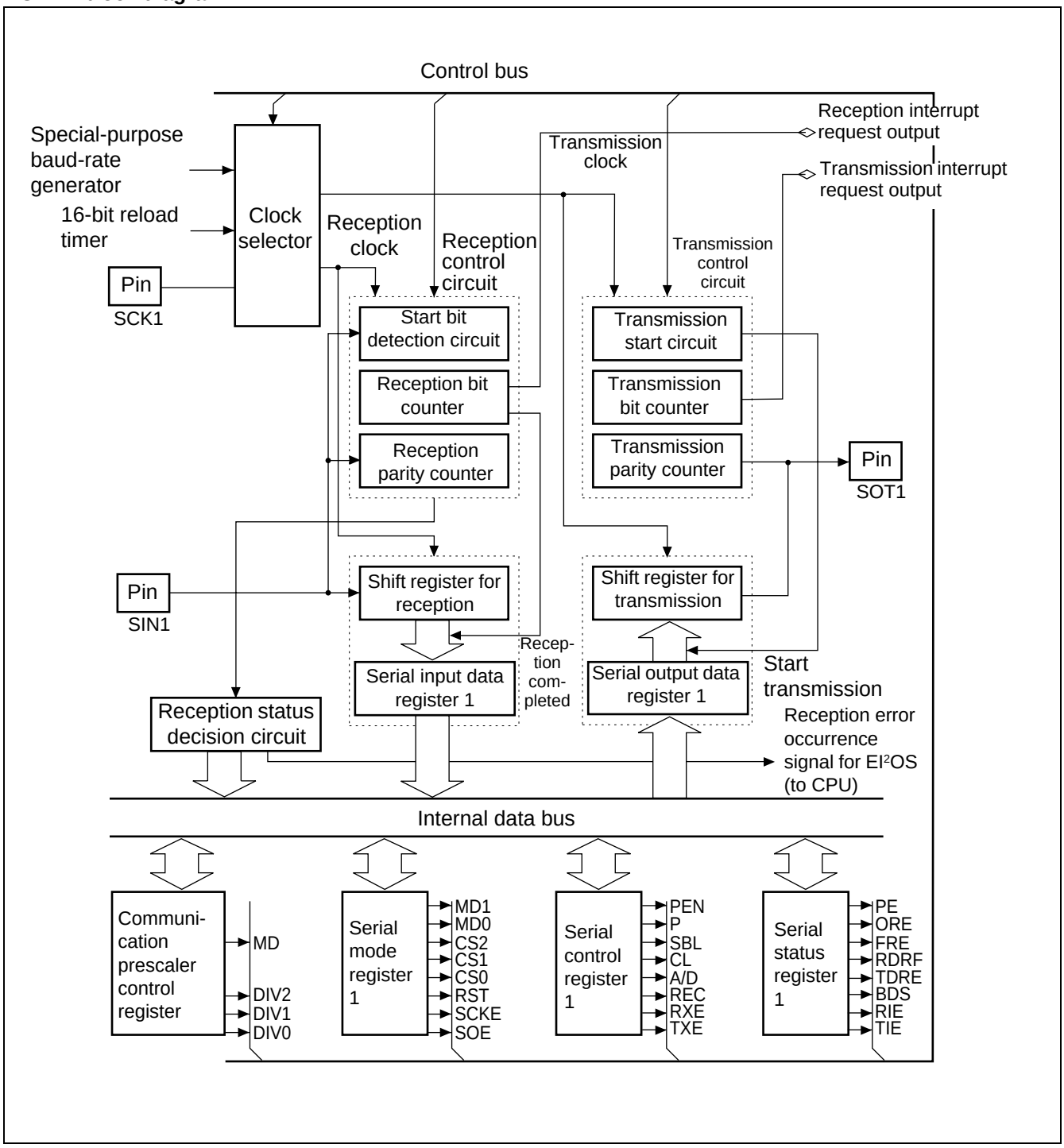
| Operation mode | | Data length | | Synchronization | Stop bit length |
|---|---|---|---|---|---|
| | | With parity | Without parity | | |
| 0 | Asynchronous mode (normal mode) | 7-bit or 8-bit | | Asynchronous | 1- bit or 2-bit *2 |
| 1 | Multi processor mode | 8+1*1 | — | Asynchronous | |
| 2 | Synchronous mode | 8 | — | Synchronous | No |

— : Disallowed

*1 : “+1” is an address/data selection bit used for communication control (bit 11 of SCR1 register: A/D)

*2 : Only 1 bit is detected as a stop bit on data reception.

• **UART block diagram**



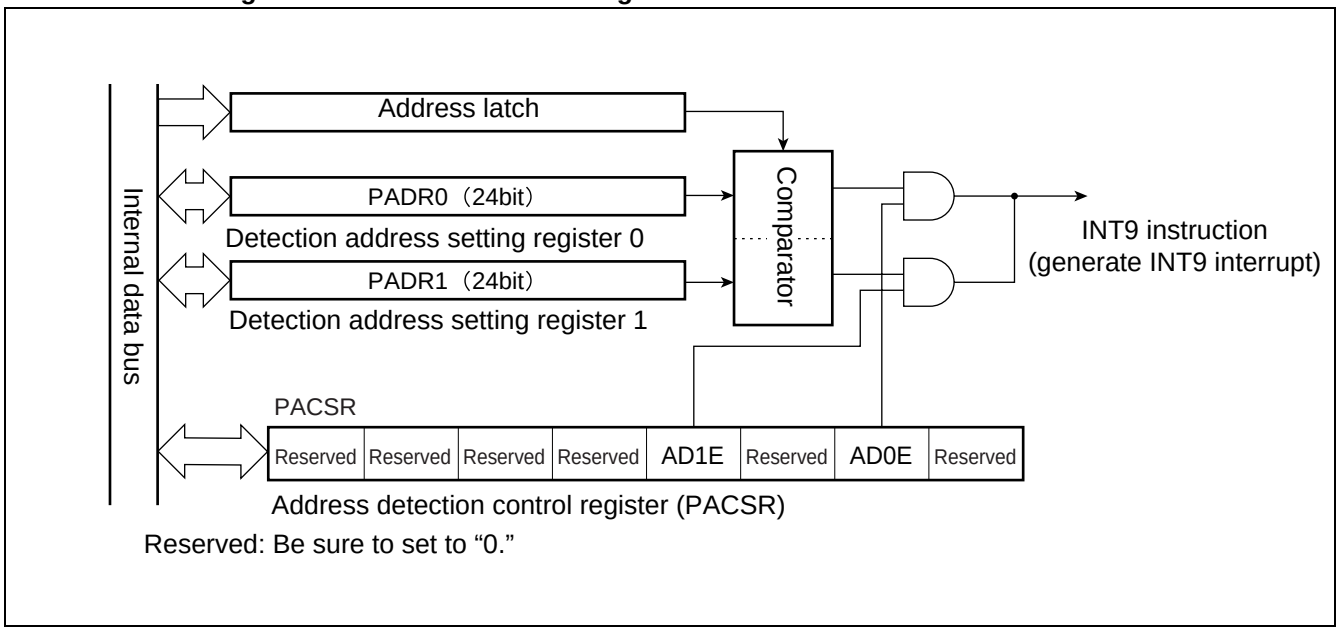
## 12. Address Matching Detection Function Outline

The address matching detection function checks if an address of an instruction to be processed next to a currently-processed instruction is identical with an address specified in the detection address register. If the addresses match with each other, an instruction to be processed next in program is forcibly replaced with INT9 instruction, and process branches to the interrupt process program. Using INT9 interrupt, this function is available for correcting program by batch processing.

**• Address matching detection function outline**

- An address of an instruction to be processed next to a currently-processed instruction of the program is always retained in an address latch via internal data bus. By the address matching detection function, the address value retained in the address latch is always compared with an address specified in detection address setting register. If the compared address values match with each other, an instruction to be processed next by CPU is forcibly replaced with INT9 instruction, and an interrupt process program is executed.
- Two detection address setting registers are provided (PADR0 and PADR1), and each register is provided with interrupt permission bit. Generation of interrupt, which is caused by address matching between the address retained in address latch and the address specified in address setting register, is permitted and prohibited on a register-by-register basis.

**• Address matching detection function block diagram**

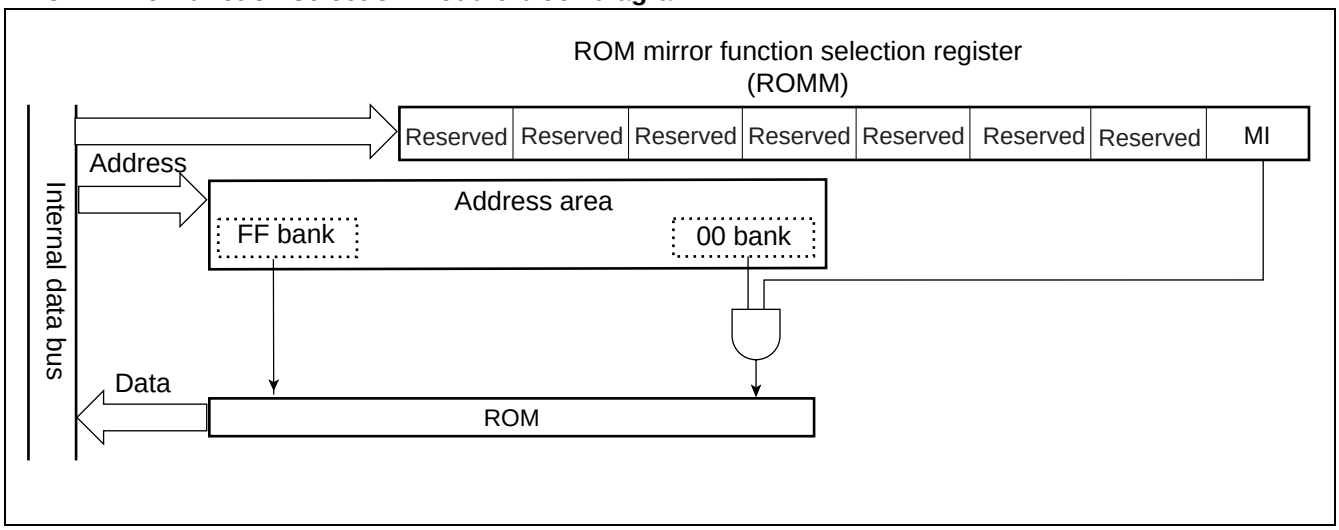



- Address latch
  Retains address value output to internal data bus.
- Address detection control register (PACSR)
  Specifies if interrupt is permitted or prohibited when addresses match with each other.
- Detection address setting (PADR0, PADR1)
  Specifies addresses to be compared with values in address latch.

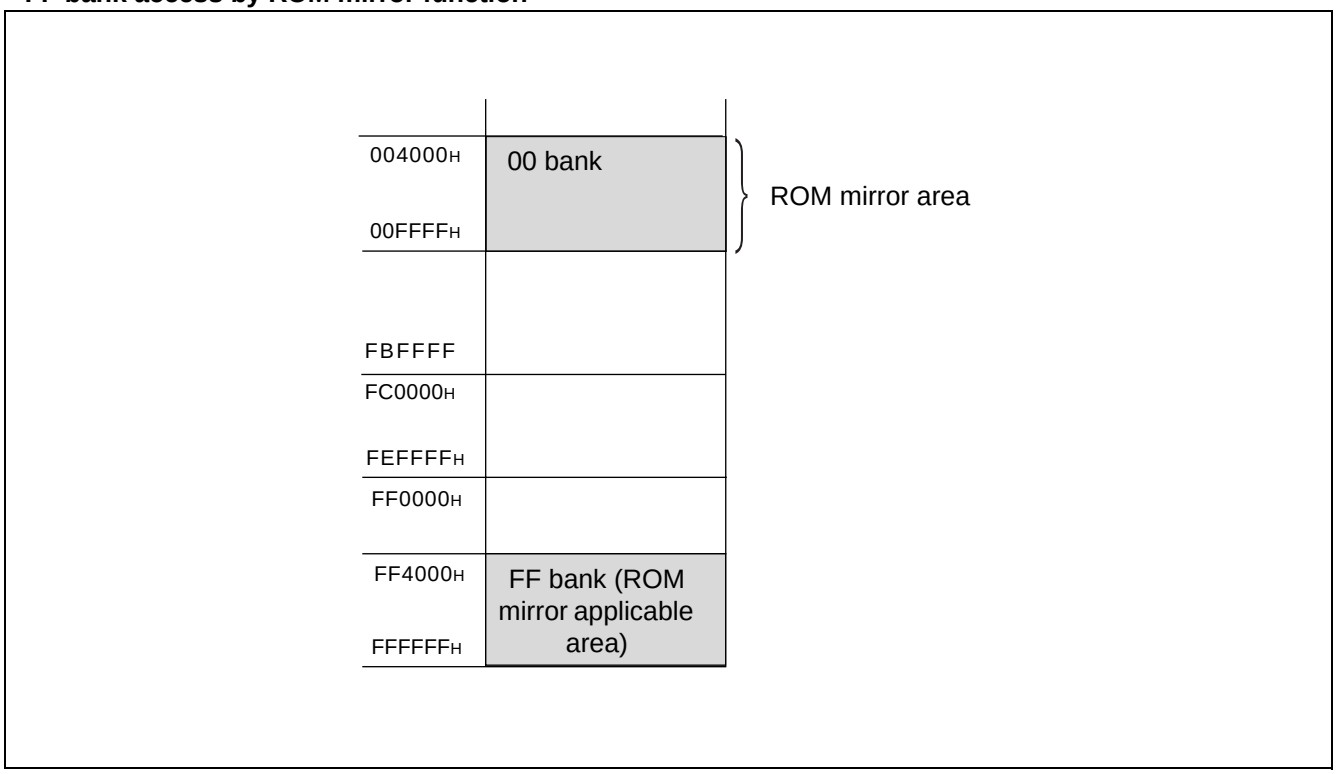
## 13. ROM Mirror Function Selection Module Outline

The ROM mirror function selection module sets the data in ROM assigned to FF bank so that the data is read by access to 00 bank.

**• ROM mirror function selection module block diagram**




**• FF bank access by ROM mirror function**



## 14. 192 K/256 K/512 Kbit Flash Memory Outline

The following three methods are provided for data writing and deleting on flash memory:

1. Parallel writer
2. Serial special-purpose writer
3. Writing/deleting by program execution

**• 192 K/256 K/512 Kbit flash memory outline**

The 192 K/256 K/512K-bit flash memory is allocated on $FF_H$ bank of CPU memory map. Using the function of flash memory interface circuit, the memory allows read access and program access from CPU.

Writing/deleting on flash memory is performed by instruction from CPU via flash memory interface. Because rewriting is allowed on mounted memory, modifying program and data is performed efficiently.

**• Features of 192 K/256 K/512 Kbit flash memory**

- Dividing into many sectors
- Automatic program algorithm (Embedded Algorithm™: Similar to MBM29LV200.)
- Built-in deletion pause/deletion resume function
- Detection of completed writing/deleting by data polling and toggle bits.
- Detection of completed writing/deleting by CPU interrupt.
- Deletion is allowed on a sector-by-sector basis (sectors are combined freely).
- Number of writing/deleting operations (minimum): 10,000 times
- Sector protection
- Extended sector protection
- Temporary sector unprotection

Embedded Algorithm™ is a registered trademark of Advanced Micro Device.

Note : A function of reading manufacture code and device code is not provided. These codes are not accessible by command either.

**• Flash memory writing/deleting**

- Writing and reading data is not allowed simultaneously on the flash memory.
- Data writing and deleting on the flash memory is performed by the processes as follows: Make a copy of program on flash memory onto RAM. Then, execute the program copied on the RAM.

**• List of registers and reset values in flash memory**

Flash memory control status register (FMCS)

| bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | 0 | 0 | 0 | X | 0 | 0 | 0 | 0 |

× : Undefined

**• Sector configuration of 192 K/256 K/512 Kbit flash memory**

• Sector configuration of 192 Kbit to flash memory (MB90F455 (S) )

| Flash memory | CPU address | Writer address* |
|---|---|---|
| SA0 (8 Kbytes) | FFA000H<br>FFBFFFH | 7A000H<br>7BFFFH |
| SA1 (16 Kbytes) | FFC000H<br>FFFFFFH | 7C000H<br>7FFFFH |

• Sector configuration of 256 Kbit to flash memory (MB90F456 (S) )

| Flash memory | CPU address | Writer address* |
|---|---|---|
| SA0 (8 Kbytes) | FF8000H<br>FF9FFFH | 78000H<br>79FFFH |
| SA1 (8 Kbytes) | FFA000H<br>FFBFFFH | 7A000H<br>7BFFFH |
| SA2 (16 Kbytes) | FFC000H<br>FFFFFFH | 7C000H<br>7FFFFH |

• Sector configuration of 512 Kbit to flash memory (MB90F457 (S) )

| Flash memory | CPU address | Writer address* |
|---|---|---|
| SA0 (32 Kbytes) | FF0000H<br>FF7FFFH | 70000H<br>77FFFH |
| SA1 (8 Kbytes) | FF8000H<br>FF9FFFH | 78000H<br>79FFFH |
| SA2 (8 Kbytes) | FFA000H<br>FFBFFFH | 7A000H<br>7BFFFH |
| SA3 (16 Kbytes) | FFC000H<br>FFFFFFH | 7C000H<br>7FFFFH |

* : “Writer address” is an address equivalent to CPU address, which is used when data is written on flash memory, using parallel writer. When writing/deleting data with general-purpose writer, the writer address is used for writing and deleting.

## ■ ELECTRIC CHARACTERISTICS

### 1. Absolute Maximum Rating

($V_{SS}$ = $AV_{SS}$ = 0.0 V)

| Parameter | Symbol | Rating | | Unit | Remarks |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Power supply voltage | $V_{CC}$ | $V_{SS}$ – 0.3 | $V_{SS}$ + 6.0 | V | |
| | $AV_{CC}$ | $V_{SS}$ – 0.3 | $V_{SS}$ + 6.0 | V | $V_{CC}$ = $AV_{CC}$*1 |
| | AVR | $V_{SS}$ – 0.3 | $V_{SS}$ + 6.0 | V | $AV_{CC}$ ≥ AVR*1 |
| Input voltage | $V_I$ | $V_{SS}$ – 0.3 | $V_{SS}$ + 6.0 | V | *2 |
| Output voltage | $V_O$ | $V_{SS}$ – 0.3 | $V_{SS}$ + 6.0 | V | *2 |
| Maximum clamp current | $I_{CLAMP}$ | – 2.0 | + 2.0 | mA | *6 |
| Total maximum clamp current | $\sum \lvert I_{CLAMP} \rvert$ | — | 20 | mA | *6 |
| “L” level maximum output current | $I_{OL1}$ | — | 15 | mA | Normal output*3 |
| | $I_{OL2}$ | — | 40 | mA | High-current output*3 |
| “L” level average output current | $I_{OLAV1}$ | — | 4 | mA | Normal output*4 |
| | $I_{OLAV2}$ | — | 30 | mA | High-current output*4 |
| “L” level maximum total output current | $\sum I_{OL1}$ | — | 125 | mA | Normal output |
| | $\sum I_{OL2}$ | — | 160 | mA | High-current output |
| “L” level average total output current | $\sum I_{OLAV1}$ | — | 40 | mA | Normal output*5 |
| | $\sum I_{OLAV2}$ | — | 40 | mA | High-current output*5 |
| “H” level maximum output current | $I_{OH1}$ | — | –15 | mA | Normal output*3 |
| | $I_{OH2}$ | — | –40 | mA | High-current output*3 |
| “H” level average output current | $I_{OHAV1}$ | — | –4 | mA | Normal output*4 |
| | $I_{OHAV2}$ | — | –30 | mA | High-current output*4 |
| “H” level maximum total output current | $\sum I_{OH1}$ | — | –125 | mA | Normal output |
| | $\sum I_{OH2}$ | — | –160 | mA | High-current output |
| “H” level average total output current | $\sum I_{OHAV1}$ | — | –40 | mA | Normal output*5 |
| | $\sum I_{OHAV2}$ | — | –40 | mA | High-current output*5 |
| Power consumption | $P_D$ | — | 245 | mW | |
| Operating temperature | $T_A$ | –40 | +105 | °C | |
| Storage temperature | Tstg | –55 | +150 | °C | |

*1 : AVcc and AVR should not exceed Vcc. Also AVR should not exceed AVcc.

*2 : $V_I$, $V_O$, should not exceed Vcc + 0.3V.

*3 : A peak value of an applicable one pin is specified as a maximum output current.

*4 : An average current value of an applicable one pin within 100 ms is specified as an average output current. (Average value is found by multiplying operating current by operating rate.)

*5 : An average current value of all pins within 100 ms is specified as an average total output current. (Average value is found by multiplying operating current by operating rate.)

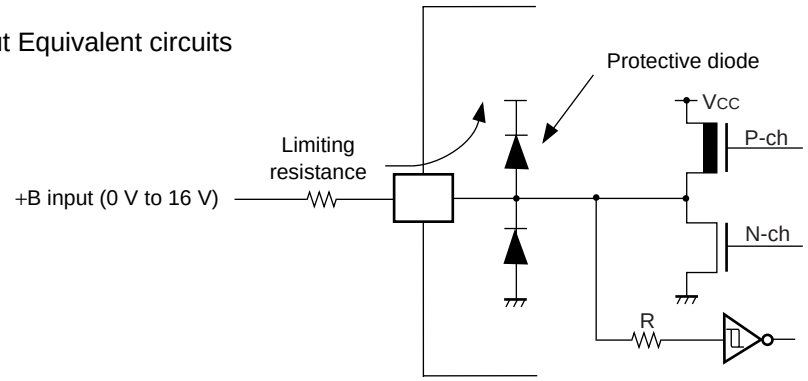
*(Continued)*

*(Continued)*

*6 : • Applicable to pins: P10 to P17, P20 to P27, P30 to P33, P35*, P36*, P37, P40 to P44, P50 to P57
Note : P35 and P36 are applicable only for products of MB90F455S/F456S/F457S, MB90455S/456S/457S.

- Use within recommended operating conditions.
- Use at DC voltage (current) .
- The +B signal should always be applied a limiting resistance placed between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the $V_{CC}$ pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V) , the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on reset.
- Care must be taken not to leave the +B input pin open.
- Note that analog system input/output pins other than the A/D input pins (LCD drive pins, comparator input pins, etc.) cannot accept +B signal input.
- Sample recommended circuits:

• Input/Output Equivalent circuits




WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

## 2. Recommended Operating Conditions

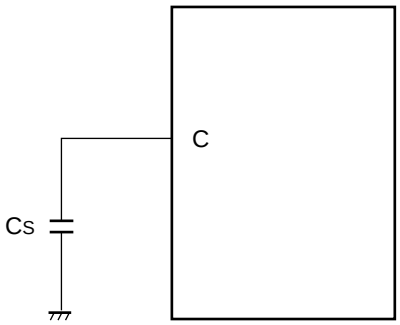
($V_{SS}$ = $AV_{SS}$ = 0.0V)

| Parameter | Symbol | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| Power supply voltage | $V_{CC}$ | 3.5 | 5.0 | 5.5 | V | Under normal operation |
| | | 3.0 | — | 5.5 | V | Retain status of stop operation |
| | $AV_{CC}$ | 4.0 | — | 5.5 | V | *2 |
| Smoothing capacitor | $C_S$ | 0.1 | — | 1.0 | µF | *1 |
| Operating temperature | $T_A$ | −40 | — | +105 | °C | |

*1 : Use a ceramic capacitor, or a capacitor of similar frequency characteristics. On the Vcc pin, use a bypass capacitor that has a larger capacity than that of Cs.
Refer to the following figure for connection of smoothing capacitor Cs.

*2 : AVcc is a voltage at which accuracy is guaranteed. AVcc should not exceed Vcc.

• C pin connection diagram




WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

### 3. DC Characteristics

($V_{CC}$ = 5.0 V±10%, $V_{SS}$ = $AV_{SS}$ = 0.0 V, $T_A$ = –40 °C to +105 °C)

| Parameter | Symbol | Pin name | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| "H" level input voltage | $V_{IHS}$ | CMOS hysteresis input pin | — | 0.8 $V_{CC}$ | — | $V_{CC}$ + 0.3 | V | |
| | $V_{IHM}$ | MD input pin | — | $V_{CC}$ – 0.3 | — | $V_{CC}$ + 0.3 | V | |
| "L" level input voltage | $V_{ILS}$ | CMOS hysteresis input pin | — | $V_{SS}$ – 0.3 | — | 0.2 $V_{CC}$ | V | |
| | $V_{ILM}$ | MD input pin | — | $V_{SS}$ – 0.3 | — | $V_{SS}$ + 0.3 | V | |
| "H" level output voltage | $V_{OH1}$ | Pins other than P14 to P17 | $V_{CC}$ = 4.5 V, $I_{OH}$ = –4.0 mA | $V_{CC}$ – 0.5 | — | — | V | |
| | $V_{OH2}$ | P14 to P17 | $V_{CC}$ = 4.5 V, $I_{OH}$ = –14.0 mA | $V_{CC}$ – 0.5 | — | — | V | |
| "L" level output voltage | $V_{OL1}$ | Pins other than P14 to P17 | $V_{CC}$ = 4.5 V, $I_{OL}$ = 4.0 mA | — | — | 0.4 | V | |
| | $V_{OL2}$ | P14 to P17 | $V_{CC}$ = 4.5 V, $I_{OL}$ = 20.0 mA | — | — | 0.4 | V | |
| Input leak current | $I_{IL}$ | All input pins | $V_{CC}$ = 5.5 V, $V_{SS}$ < $V_I$ < $V_{CC}$ | –5 | — | +5 | µA | |
| Power supply current* | $I_{CC}$ | $V_{CC}$ | $V_{CC}$ = 5.0 V, Internally operating at 16 MHz, normal operation. | — | 25 | 30 | mA | |
| | | | $V_{CC}$ = 5.0 V, Internally operating at 16 MHz, writing on flash memory. | — | 45 | 50 | mA | Flash ROM product |
| | | | $V_{CC}$ = 5.0 V, Internally operating at 16 MHz, deleting on flash memory. | — | 45 | 50 | mA | Flash ROM product |
| | $I_{CCS}$ | | $V_{CC}$ = 5.0 V, Internally operating at 16 MHz, sleeping. | — | 8 | 12 | mA | |
| | $I_{CTS}$ | | $V_{CC}$ = 5.0 V, Internally operating at 2 MHz, transition from main clock mode, in time-base timer mode. | — | 0.75 | 1.0 | mA | Flash ROM product |
| | | | | | 0.2 | 0.35 | mA | Mask ROM product |

*(Continued)*

*(Continued)*

($V_{CC}$ = 5.0 V±10%, $V_{SS}$ = $AV_{SS}$ = 0.0 V, $T_A$ = –40 °C to +105 °C)

| Parameter | Symbol | Pin name | Conditions | Rating | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Power supply current* | $I_{CCL}$ | $V_{CC}$ | $V_{CC}$ = 5.0 V, Internally operating at 8 kHz, subclock operation, $T_A$ = + 25°C | — | 0.3 | 1.2 | mA | Flash ROM product |
| | | | | — | 40 | 100 | µA | Mask ROM product |
| | $I_{CCLS}$ | | $V_{CC}$ = 5.0 V, Internally operating at 8 kHz, subclock, sleep mode, $T_A$ = + 25°C | — | 10 | 30 | µA | |
| | $I_{CCT}$ | | $V_{CC}$ = 5.0 V, Internally operating at 8 kHz, clock mode, $T_A$ = + 25°C | — | 8 | 25 | µA | |
| | $I_{CCH}$ | | Stopping, $T_A$ = + 25°C | — | 5 | 20 | µA | |
| Input capacity | $C_{IN}$ | Other than $AV_{CC}$, $AV_{SS}$, AVR, C, $V_{CC}$, $V_{SS}$ | — | — | 5 | 15 | pF | |
| Pull-up resistor | $R_{UP}$ | $\overline{RST}$ | — | 25 | 50 | 100 | kΩ | |
| Pull-down resistor | $R_{DOWN}$ | MD2 | — | 25 | 50 | 100 | kΩ | Flash ROM product is not provided with pull-down resistor. |

* : Test conditions of power supply current are based on a device using external clock.

## 4. AC Characteristics

### (1) Clock timing

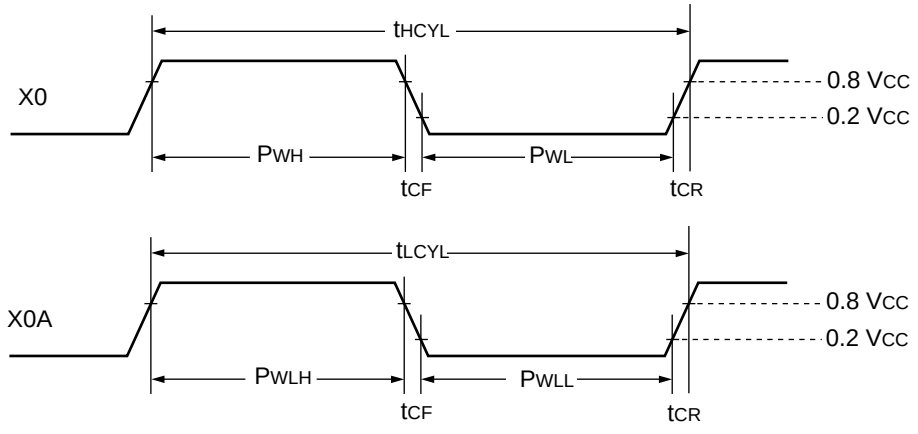
($V_{CC}$ = 5.0 V±10%, $V_{SS}$ = $AV_{SS}$ = 0.0 V, $T_A$ = –40 °C to +105 °C)

| Parameter | Symbol | Pin name | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Clock frequency | $f_C$ | X0, X1 | 3 | — | 8 | MHz | When crystal or ceramic resonator is used*2 |
| | | | 3 | — | 16 | MHz | External clock *1, *2 |
| | $f_{CL}$ | X0A, X1A | — | 32.768 | — | kHz | |
| Clock cycle time | $t_{HCYL}$ | X0, X1 | 125 | — | 333 | ns | |
| | $t_{LCYL}$ | X0A, X1A | — | 30.5 | — | µs | |
| Input clock pulse width | $P_{WH}$, $P_{WL}$ | X0 | 10 | — | — | ns | Set duty factor at 30% to 70% as a guideline. |
| | $P_{WLH}$,$P_{WLL}$ | X0A | — | 15.2 | — | µs | |
| Input clock rise time and fall time | $t_{CR}$, $t_{CF}$ | X0 | — | — | 5 | ns | When external clock is used |
| Internal operation clock frequency | $f_{CP}$ | — | 1.5 | — | 16 | MHz | When main clock is used |
| | $f_{LCP}$ | — | — | 8.192 | — | kHz | When sub clock is used |
| Internal operation clock cycle time | $t_{CP}$ | — | 62.5 | — | 666 | ns | When main clock is used |
| | $t_{LCP}$ | — | — | 122.1 | — | µs | When sub clock is used |

*1 : Internal operation clock frequency should not exceed 16 MHz.

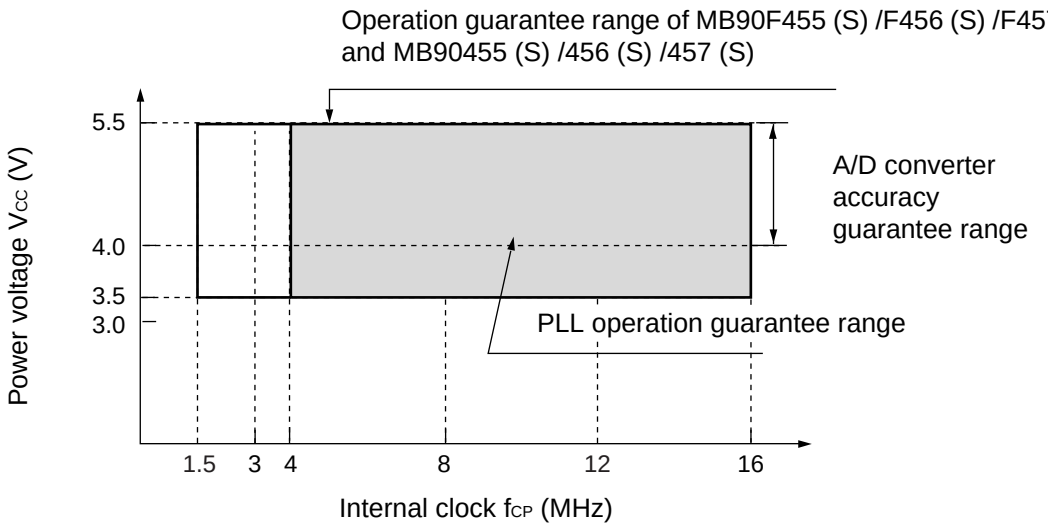
*2 : When selecting the PLL clock, the range of clock frequency is limitted. Use this product within range as mentioned in “Relation among external clock frequency and internal clock frequency”.

• Clock timing

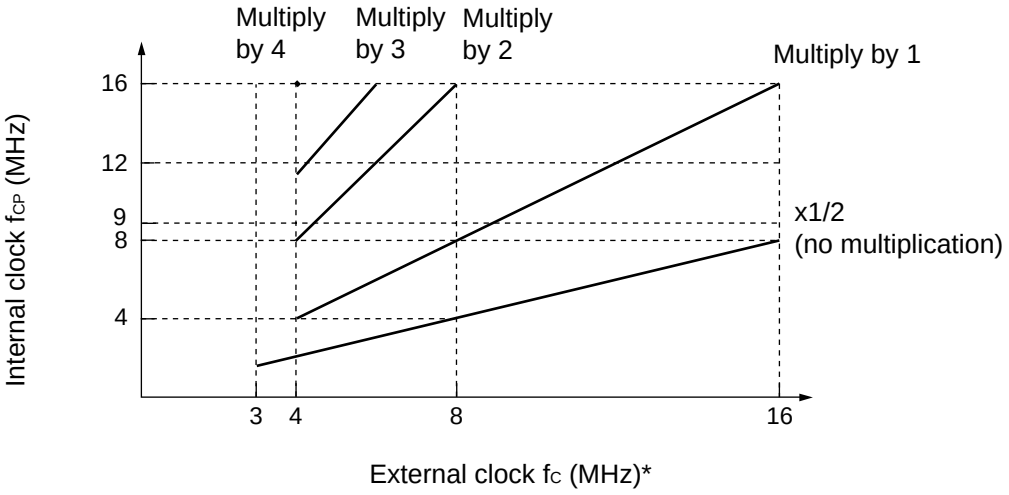


• PLL operation guarantee range

Relation between internal operation clock frequency and power supply voltage




Relation among external clock frequency and internal clock frequency

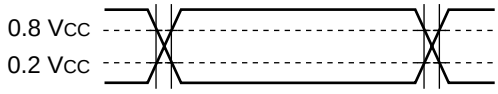



* : fc is 8 MHz at maximum when crystal or ceramic resonator is used.

Rating values of alternating current is defined by the measurement reference voltage values shown below:

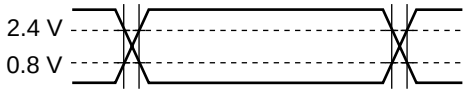
• Input signal waveform

Hysteresis input pin




• Output signal waveform

Output pin



**(2) Reset input timing**

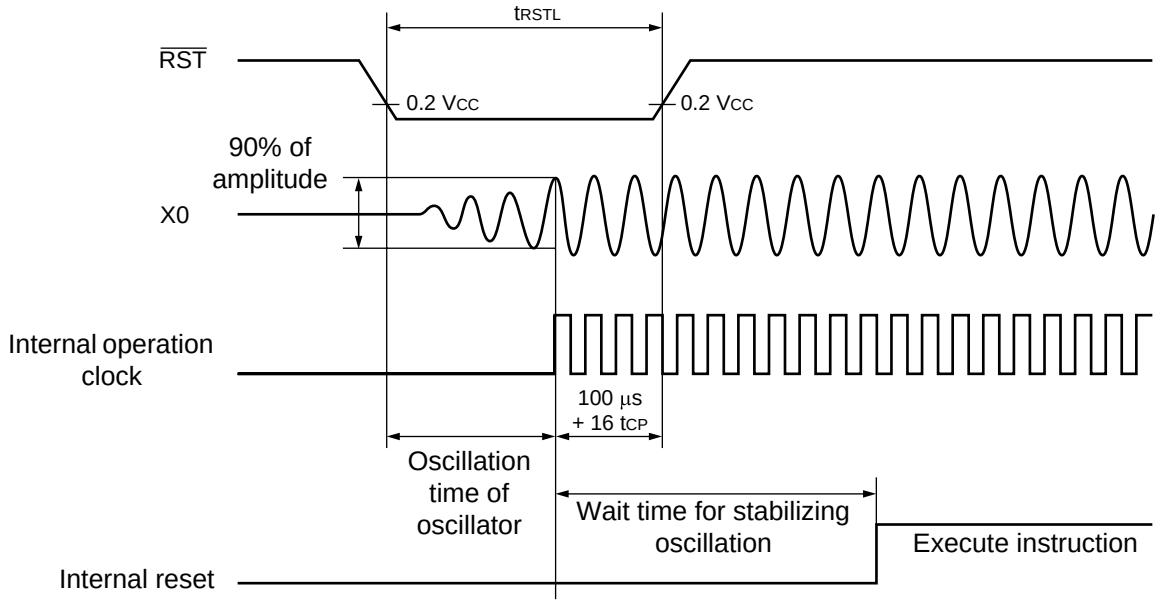
| Parameter | Symbol | Pin name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Reset input time | $t_{RSTL}$ | $\overline{RST}$ | — | 16 $t_{CP}$*3 | — | ns | Normal operation |
| | | | | Oscillation time of oscillator*1 + 100 µs + 16 $t_{CP}$*3 | — | — | In sub clock*2, sub sleep*2, watch*2 and stop mode |
| | | | | 100 | — | µs | In time base timer mode |

*1 : Oscillation time of oscillator is time until oscillation reaches 90% of amplitude. It takes several milliseconds to several dozens of milliseconds on a crystal oscillator, several hundreds of microseconds to several milliseconds on a FAR/ceramic oscillator, and 0 milliseconds on an external clock.

*2 : Except for MB90F455S/F456S/F457S, MB90455S/456S/457S.

*3 : Refer to "(1) Clock timing" ratings for $t_{CP}$ (internal operation clock cycle time).

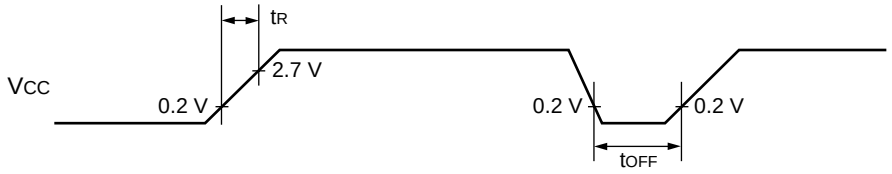
- In sub clock, sub sleep, watch and stop mode



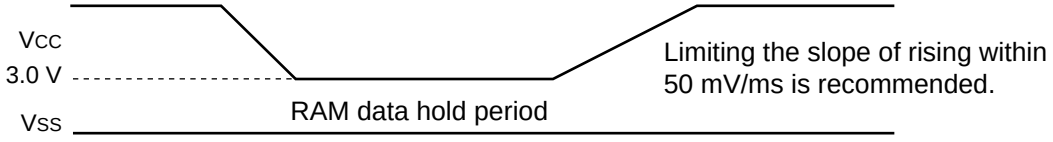
**(3) Power-on reset**

($V_{CC}$ = 5.0 V ± 10%, $V_{SS}$ = $AV_{SS}$ = 0.0 V, $T_A$ = –40 °C to +105 °C)

| Parameter | Symbol | Pin name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Power supply rise time | $t_R$ | $V_{CC}$ | — | 0.05 | 30 | ms | |
| Power supply shutdown time | $t_{OFF}$ | $V_{CC}$ | | 1 | — | ms | Repeated operation |




Sudden change of power supply voltage may activate the power-on reset function. When changing power supply voltages during operation, raise the power smoothly by suppressing variation of voltages as shown below. When raising the power, do not use PLL clock. However, if voltage drop is 1V/s or less, use of PLL clock is allowed during operation.



**(4) UART timing**

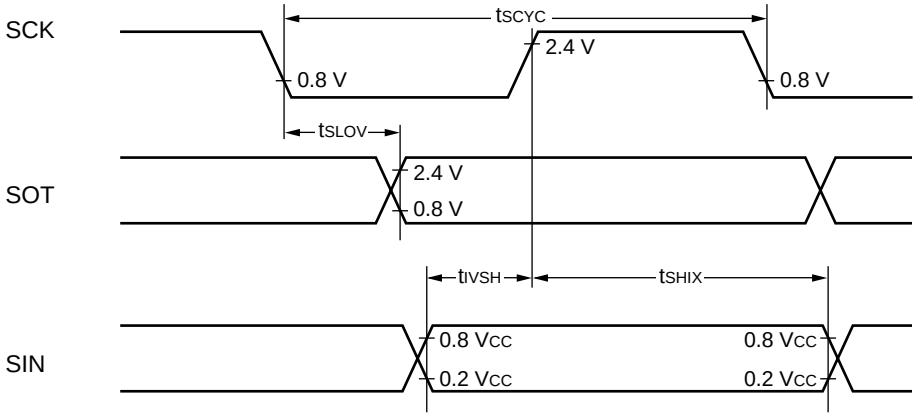
($V_{CC}$ = 4.5 V to 5.5 V, $V_{SS}$ = 0.0 V, $T_A$ = –40 °C to +105 °C)

| Parameter | Symbol | Pin name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Serial clock cycle time | $t_{SCYC}$ | SCK1 | Internal shift clock mode output pin is : CL = 80 pF+1TTL. | 8 $t_{CP}$ * | — | ns | |
| SCK ↓ → SOT delay time | $t_{SLOV}$ | SCK1, SOT1 | | –80 | +80 | ns | |
| Valid SIN → SCK ↑ | $t_{IVSH}$ | SCK1, SIN1 | | 100 | — | ns | |
| SCK ↑ → valid SIN hold time | $t_{SHIX}$ | SCK1, SIN1 | | 60 | — | ns | |
| Serial clock “H” pulse width | $t_{SHSL}$ | SCK1 | External shift clock mode output pin is : CL = 80 pF+1TTL. | 4 $t_{CP}$ * | — | ns | |
| Serial clock “L” pulse width | $t_{SLSH}$ | SCK1 | | 4 $t_{CP}$ * | — | ns | |
| SCK ↓ → SOT delay time | $t_{SLOV}$ | SCK1, SOT1 | | — | 150 | ns | |
| Valid SIN → SCK ↑ | $t_{IVSH}$ | SCK1, SIN1 | | 60 | — | ns | |
| SCK ↑ →valid SIN hold time | $t_{SHIX}$ | SCK1, SIN1 | | 60 | — | ns | |

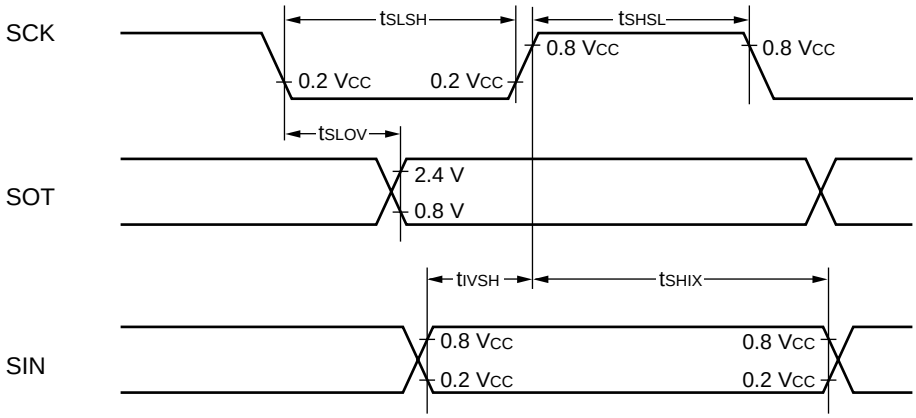
* : Refer to "(1) Clock timing" ratings for $t_{CP}$ (internal operation clock cycle time).

Notes: • AC rating in CLK synchronous mode.
• $C_L$ is a load capacitance value on pins for testing.

• Internal shift clock mode




• External shift clock mode



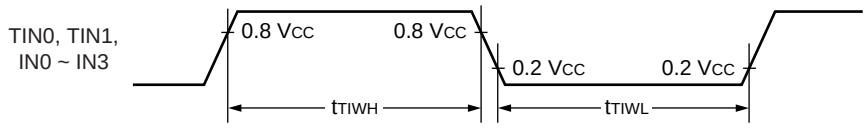
### (5) Timer input timing

($V_{CC}$ = 4.5 V to 5.5 V, $V_{SS}$ = 0.0 V, $T_A$ = –40 °C to +105 °C)

| Parameter | Symbol | Pin name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Input pulse width | $t_{TIWH}$ | TIN0, TIN1 | — | 4 $t_{CP}$ * | — | ns | |
| | $t_{TIWL}$ | IN0 to IN3 | | | | | |

* : Refer to "(1) Clock timing" ratings for $t_{CP}$ (internal operation clock cycle time).

• Timer input timing



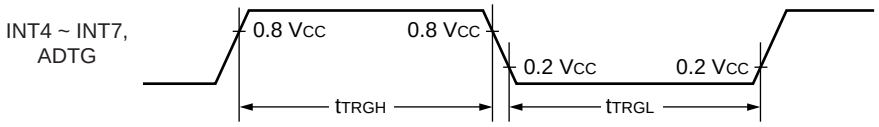

### (6) Trigger input timing

($V_{CC}$ = 4.5 V to 5.5 V, $V_{SS}$ = 0.0 V, $T_A$ = –40 °C to +105 °C)

| Parameter | Symbol | Pin name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Input pulse width | $t_{TRGH}$<br>$t_{TRGL}$ | INT4 to INT7, ADTG | — | 5 $t_{CP}$ * | — | ns | |

* : Refer to "(1) Clock timing" ratings for $t_{CP}$ (internal operation clock cycle time).

• Trigger input timing



## 5. A/D converter

($V_{CC}$ = $AV_{CC}$ = 5.0 V ± 10%, $V_{SS}$ = $AV_{SS}$ = 0.0 V, 3.0 V ≤ AVR − $AV_{SS}$, $T_A$ = −40 °C to +105 °C)

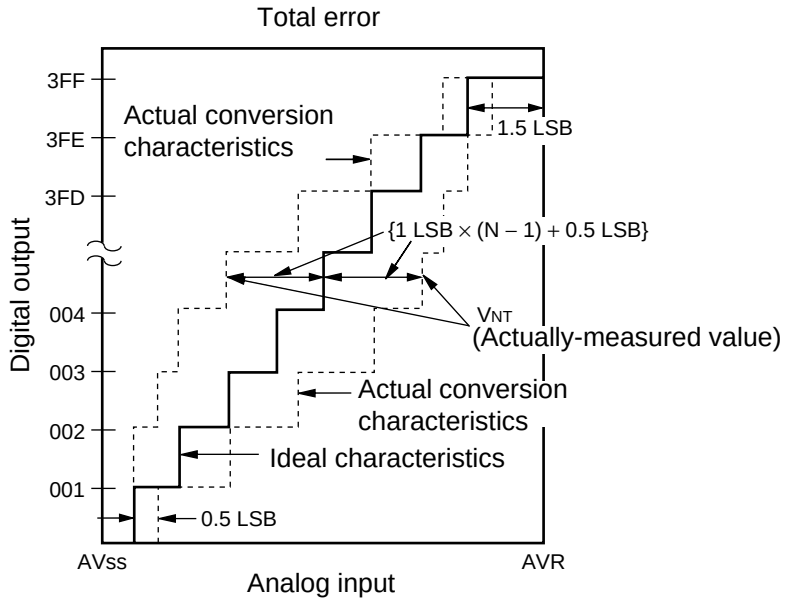
| Parameter | Symbol | Pin name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Resolution | — | — | — | — | 10 | bit | |
| Total error | — | — | — | — | ± 3.0 | LSB | |
| Nonlinear error | — | — | — | — | ± 2.5 | LSB | |
| Differential linear error | — | — | — | — | ± 1.9 | LSB | |
| Zero transition voltage | $V_{OT}$ | AN0 to AN7 | $AV_{SS}$ − 1.5 LSB | $AV_{SS}$ + 0.5 LSB | $AV_{SS}$ + 2.5 LSB | V | 1 LSB = AVR/1024 |
| Full-scale transition voltage | $V_{FST}$ | AN0 to AN7 | AVR − 3.5 LSB | AVR − 1.5 LSB | AVR + 0.5 LSB | V | |
| Compare time | — | — | 66 $t_{CP}$ *1 | — | — | ns | With 16 MHz machine clock 5.5 V ≥ $AV_{CC}$ ≥ 4.5 V |
| | | | 88 $t_{CP}$ *1 | — | — | ns | With 16 MHz machine clock 4.5 V > $AV_{CC}$ ≥ 4.0 V |
| Sampling time | — | — | 32 $t_{CP}$ *1 | — | — | ns | With 16 MHz machine clock 5.5 V ≥ $AV_{CC}$ ≥ 4.5 V |
| | | | 128 $t_{CP}$ *1 | — | — | ns | With 16 MHz machine clock 4.5 V > $AV_{CC}$ ≥ 4.0 V |
| Analog port input current | $I_{AIN}$ | AN0 to AN7 | — | — | 10 | µA | |
| Analog input voltage | $V_{AIN}$ | AN0 to AN7 | $AV_{SS}$ | — | AVR | V | |
| Reference voltage | — | AVR | $AV_{SS}$ + 2.7 | — | $AV_{CC}$ | V | |
| Power supply current | $I_A$ | $AV_{CC}$ | — | 3.5 | 7.5 | mA | |
| | $I_{AH}$ | $AV_{CC}$ | — | — | 5 | µA | *2 |
| Reference voltage supplying current | $I_R$ | AVR | — | 165 | 250 | µA | |
| | $I_{RH}$ | AVR | — | — | 5 | µA | *2 |
| Variation among channels | — | AN0 to AN7 | — | — | 4 | LSB | |

*1 : Refer to "(1) Clock timing" ratings for $t_{CP}$ (internal operation clock cycle time).

*2 : If A/D converter is not operating, a current when CPU is stopped is applicable (Vcc=AVcc=AVR=5.0 V).

## 6. Definition of A/D Converter Terms

| | |
|---|---|
| Resolution | : Analog variation that is recognized by an A/D converter. |
| Linear error | : Deviation between a line across zero-transition line (“00 0000 00 0 0” ←→“00 0000 0001”) and full-scale transition line (“11 1111 11 1 0” ←→ “11 1111 1111”) and actual conversion characteristics. |
| Differential linear error | : Deviation of input voltage, that is required for changing output code by 1 LSB, from an ideal value. |
| Total error | : Difference between an actual value and an ideal value. A total error includes zero transition error, full-scale transition error, and linear error. |




$$\text{Total error of digital output “N”} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$1\ \text{LSB} = (\text{Ideal value})\ \frac{AVR - AV_{SS}}{1024}\ [\text{V}]$$

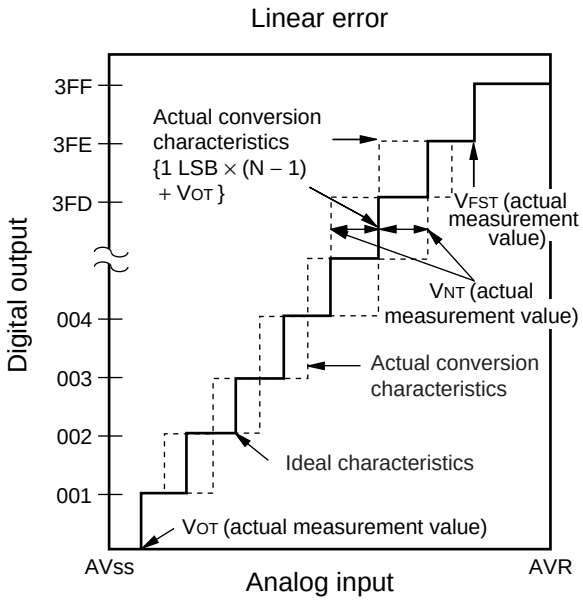
$V_{OT}$ (Ideal value) $= AV_{SS} + 0.5$ LSB [V]

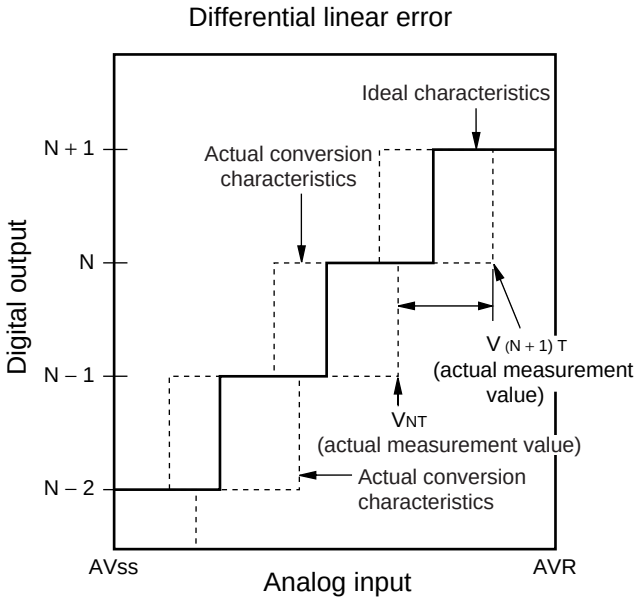
$V_{FST}$ (Ideal value) $= AVR - 1.5$ LSB [V]

$V_{NT}$ : A voltage at which digital output transits from (N-1) to N.

*(Continued)*

*(Continued)*




$$\text{Linear error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + V_{OT}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$\text{Differential linear error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\text{LSB}\ [\text{LSB}]$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ [\text{V}]$$

$V_{OT}$ : Voltage at which digital output transits from "$000_H$" to "$001_H$."
$V_{FST}$ : Voltage at which digital output transits from "$3FE_H$" to "$3FF_H$."

## 7. Notes on A/D Converter Section

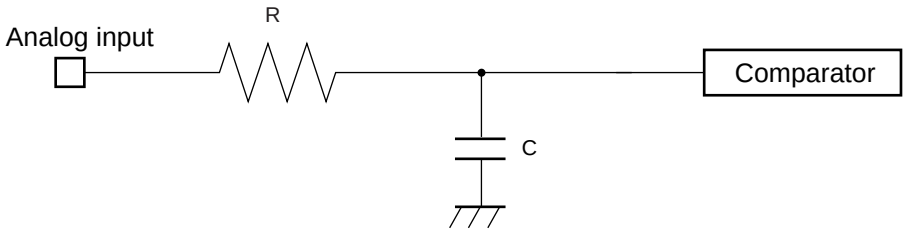
Use the device with external circuits of the following output impedance for analog inputs:

Recommended output impedance of external circuits are: Approx. 3.9 kΩ or lower (4.5 V ≤ AVcc ≤ 5.5 V) (sampling period=2.00 µs at 16-MHz machine clock), Approx. 11 kΩ or lower (4.0 V ≤ AVcc < 4.5 V) (sampling period=8.0 µs at 16-MHz machine clock).

If an external capacitor is used, in consideration of the effect by tap capacitance caused by external capacitors and on-chip capacitors, capacitance of the external one is recommended to be several thousand times as high as internal capacitor.

If output impedance of an external circuit is too high, a sampling period for an analog voltage may be insufficient.

• Analog input circuit model




MB90F455 (S) /F456 (S) /F457 (S) and MB90455 (S) /456 (S) /457 (S)

4.5 V ≤ $AV_{CC}$ ≤ 5.5 V R≒ 2.35 kΩ, C≒ 36.4 pF

4.0 V ≤ $AV_{CC}$ < 4.5 V R≒ 16.4 kΩ, C≒ 36.4 pF

Note : Use the values in the figure only as a guideline.

**• About errors**

As [AVR-AVss] become smaller, values of relative errors grow larger.

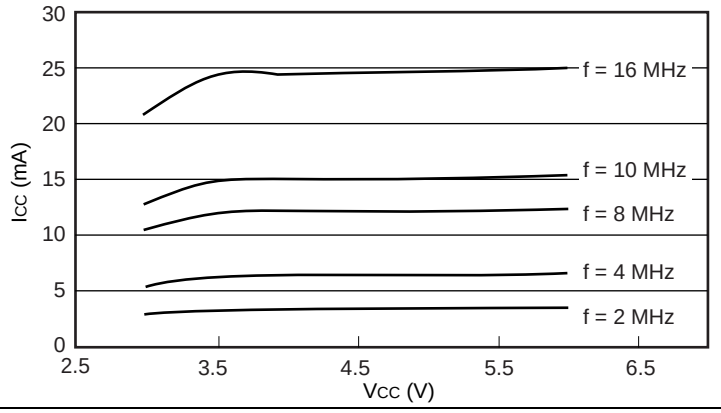
## 8. Flash Memory Program/Erase Characteristics

| Parameter | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| Sector eraset time | $T_A$ = + 25 °C<br>$V_{CC}$ = 5.0 V | — | 1 | 15 | s | Excludes $00_H$ programming prior to erasure |
| Chip erase time | | — | 4 | — | s | Excludes $00_H$ programming prior to erasure |
| Word (16 bit width) programming time | | — | 16 | 3,600 | µs | Except for the over head time of the system |
| Program/Erase cycle | — | 10,000 | — | — | cycle | |

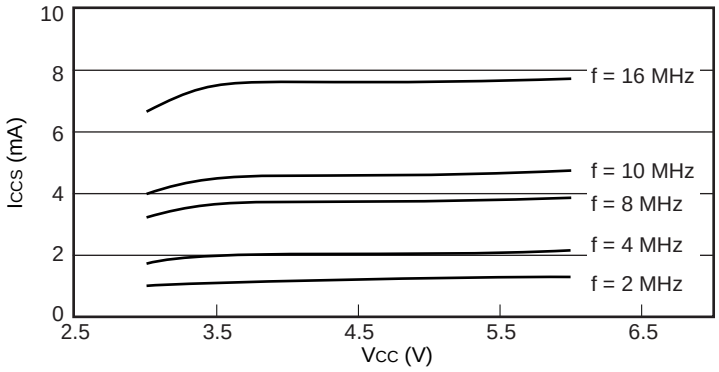
## ■ EXAMPLE CHARACTERISTICS

- MB90F457

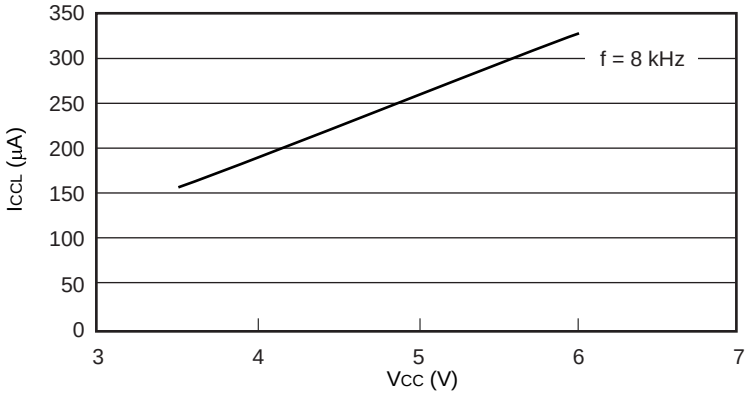
$I_{CC} - V_{CC}$
$T_A$ = +25 °C, external clock operation
f = Internal operation frequency




$I_{CCS} - V_{CC}$
$T_A$ = +25 °C, external clock operation
f = Internal operation frequency




$I_{CCL} - V_{CC}$
$T_A$ = +25 °C, external clock operation
f = Internal operation frequency

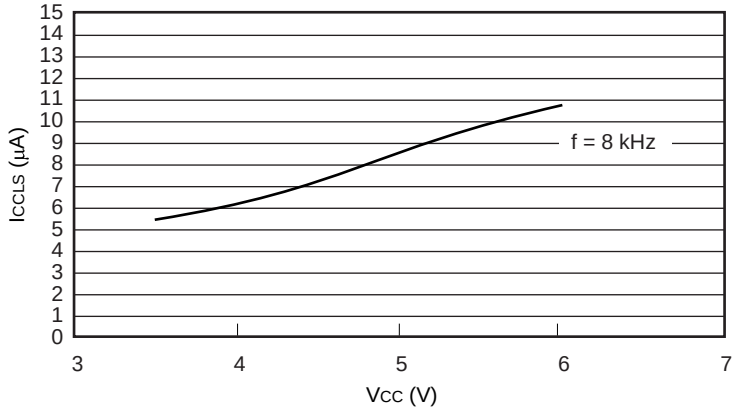



*(Continued)*

$I_{CCLS}$ – $V_{CC}$

$T_A$ = +25 °C, external clock operation

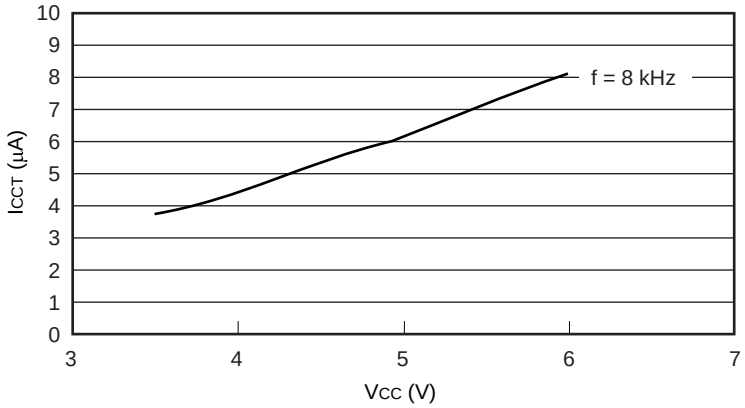
f = Internal operation frequency




$I_{CCT}$ – $V_{CC}$

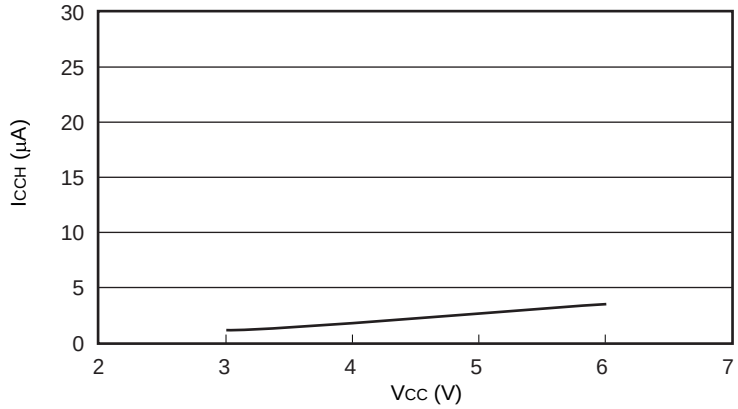
$T_A$ = +25 °C, external clock operation

f = Internal operation frequency




$I_{CCH}$ – $V_{CC}$

Stopping, $T_A$ = +25 °C

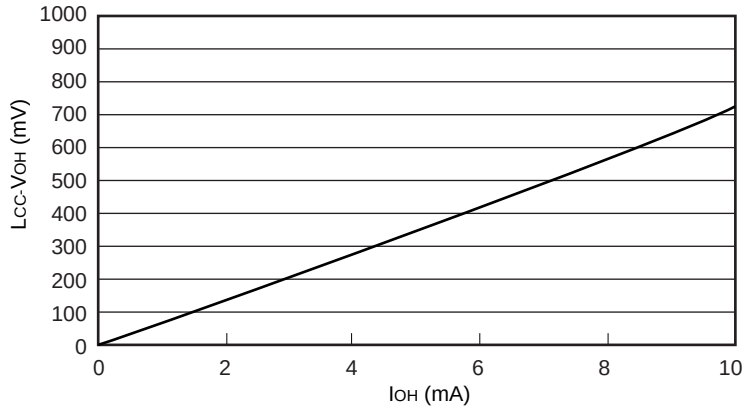



*(Continued)*

*(Continued)*

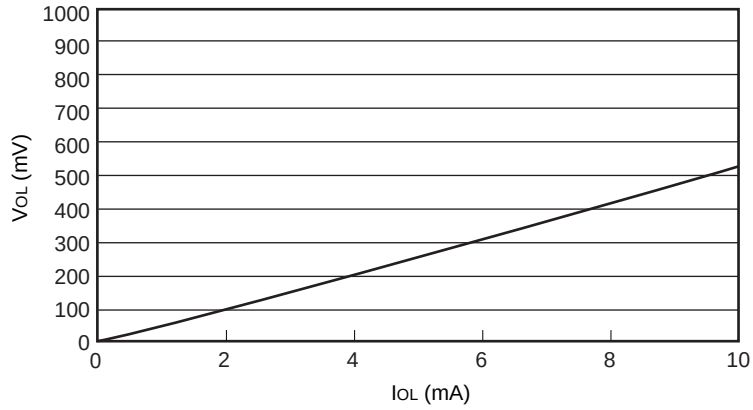
$(V_{CC} - V_{OH}) - I_{OH}$

$T_A$ = +25 °C, $V_{CC}$ = 4.5 V




$V_{OL} - I_{OL}$

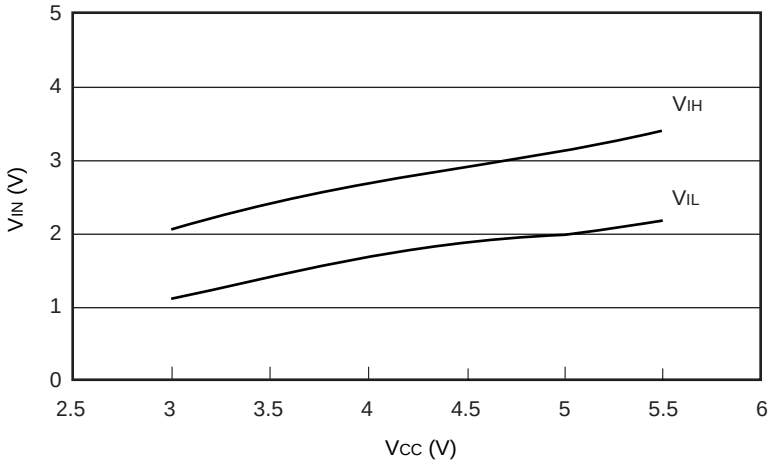
$T_A$ = +25 °C, $V_{CC}$ = 4.5 V




"H" level input voltage/ "L" level input voltage

$V_{IN} - V_{CC}$

$T_A$ = +25 °C

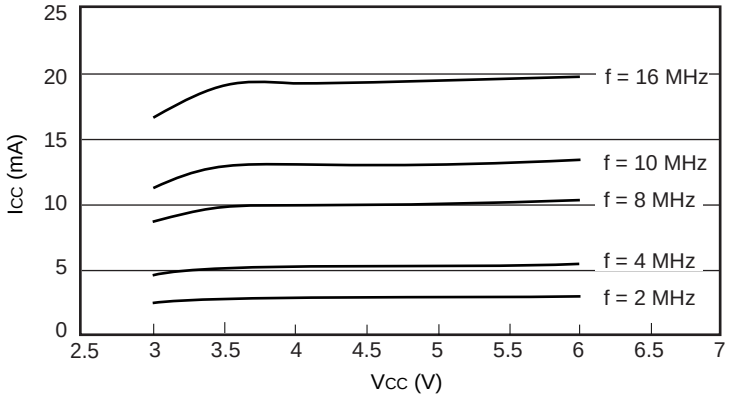


- MB90457

$I_{CC} - V_{CC}$

$T_A$ = +25 °C, external clock operation

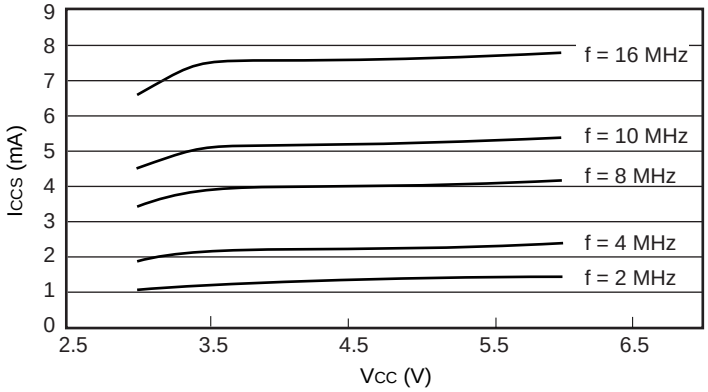
f = Internal operation frequency




$I_{CCS} - V_{CC}$

$T_A$ = +25 °C, external clock operation

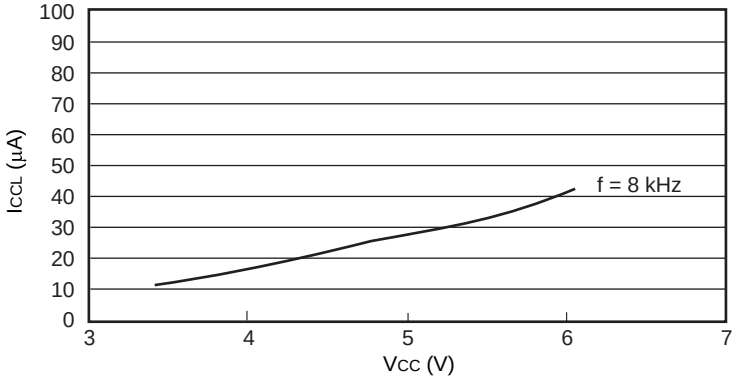
f = Internal operation frequency




$I_{CCL} - V_{CC}$

$T_A$ = +25 °C, external clock operation

f = Internal operation frequency

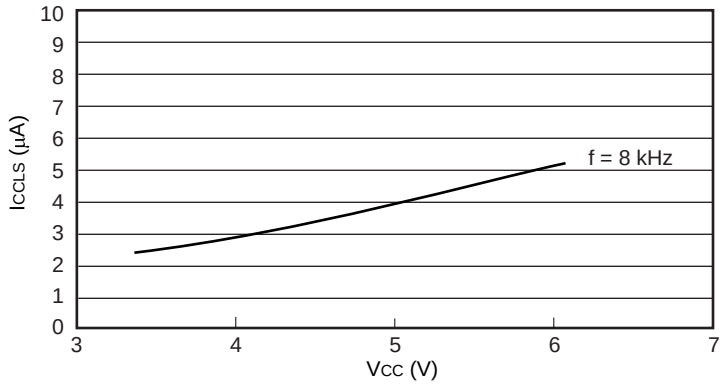



*(Continued)*

$I_{CCLS}$ – $V_{CC}$

$T_A$ = +25 °C, external clock operation

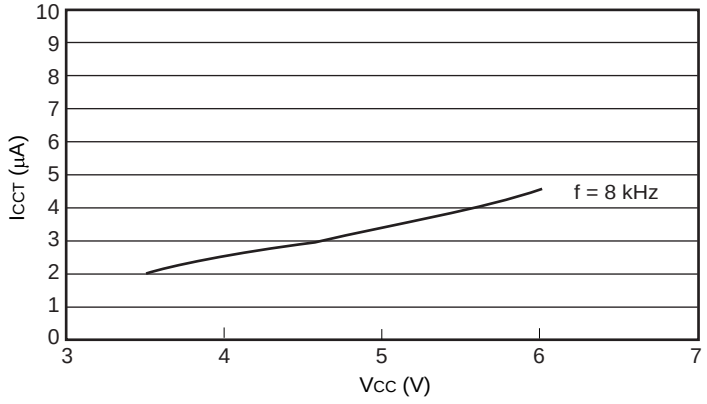
f = Internal operation frequency




$I_{CCT}$ – $V_{CC}$

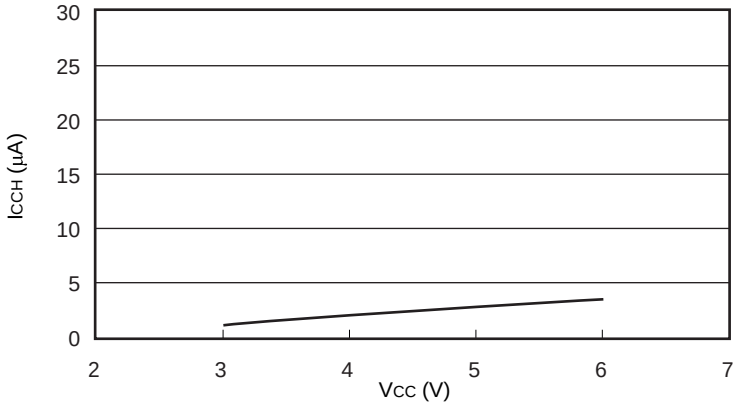
$T_A$ = +25 °C, external clock operation

f = Internal operation frequency




$I_{CCH}$ – $V_{CC}$

Stopping, $T_A$ = +25 °C




*(Continued)*

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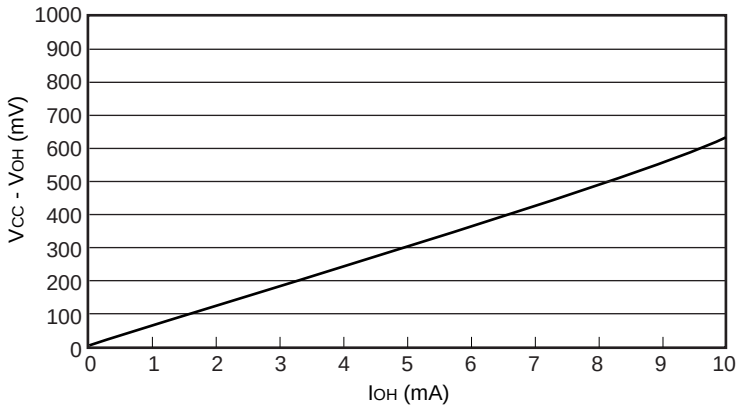
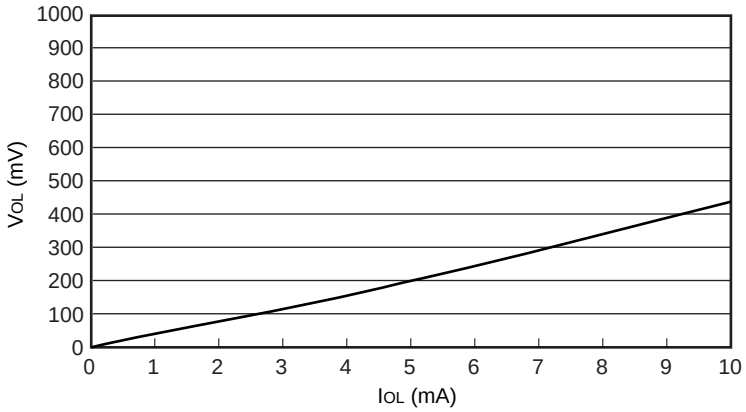
$(V_{CC} - V_{OH}) - I_{OH}$

$T_A$ = +25 °C, $V_{CC}$ = 4.5 V




$V_{OL} - I_{OL}$

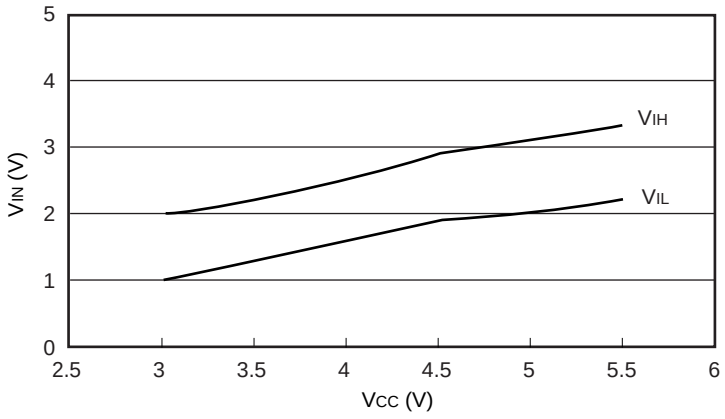
$T_A$ = +25 °C, $V_{CC}$ = 4.5 V




“H” level input voltage/ “L” level input voltage

$V_{IN} - V_{CC}$

$T_A$ = +25 °C



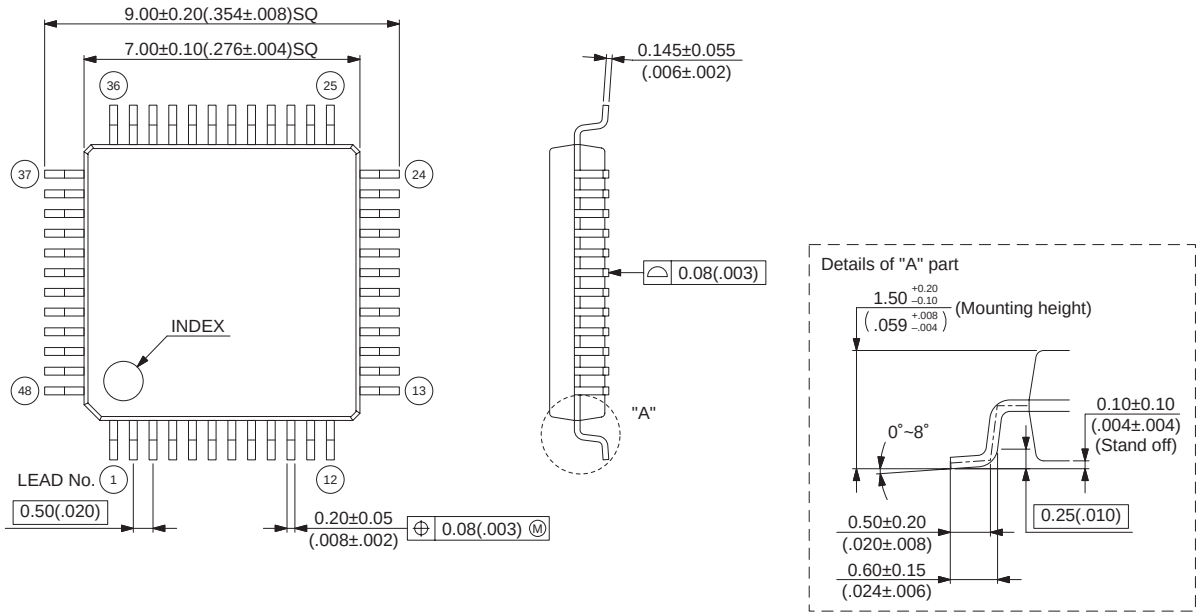
## ■ ORDERING INFORMATION

| Part number | Package | Remarks |
|---|---|---|
| MB90F455PMT<br>MB90F456PMT<br>MB90F457PMT<br>MB90455PMT<br>MB90456PMT<br>MB90457PMT<br>MB90F455SPMT<br>MB90F456SPMT<br>MB90F457SPMT<br>MB90455SPMT<br>MB90456SPMT<br>MB90457SPMT | 48-pin plastic LQFP<br>(FPT-48P-M26) | |

## ■ PACKAGE DIMENTION

48-pin plastic LQFP
(FPT-48P-M26)

Note : Pins width and pins thickness include plating tackiness.

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Dimensions in mm (inches)

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