FUJITSU SEMICONDUCTOR
DATA SHEET

Preliminary
2004.07.22

16-bit Proprietary Microcontroller

CMOS

F²MC®-16LX MB90800 Series

MB90803/F804/V800

■ DESCRIPTION

The MB90800 series is a general-purpose 16-bit microcontroller that has been developed for high-speed real-time processing required for industrial and office automation equipment and process control, etc. The LCD controller of 48 segment four common is built into.

Instruction set has taken over the same AT architecture as in the F²MC*-8L and F²MC 16L, and is further enhanced to support high level languages, extend addressing mode, enhanced divide/multiply instructions with sign and enrichment of bit processing. In addition, long word processing is now available by introducing a 32-bit accumulator.

* : F²MC, an abbreviation for FUJITSU Flexible Microcontroller, is a registered trademark of FUJITSU Ltd.

■ FEATURES

- **Clock**
  - Built-in PLL clock frequency multiplication circuit
  - Operating clock (PLL clock) can be selected from divided-by-2 of oscillation or 1 to 4 times the oscillation (at oscillation of 6.25 MHz, 6.25 MHz to 25 MHz).
  - Minimum instruction execution time of 40.0 ns (at oscillation of 6.25 MHz, four times the PLL clock, operation at Vcc = 3.3 V)
- **The maximum memory space:16 MB**
  - 24-bit internal addressing
  - Bank addressing

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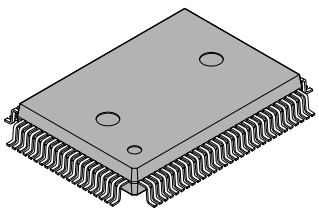
■ PACKAGE

100-pin plastic QFP



(FPT-100P-M06)

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- **Optimized instruction set for controller applications**
  - Wide choice of data types (bit, byte, word, and long word)
  - Wide choice of addressing modes (23 types)
  - High code efficiency
  - Enhanced high-precision computing with 32-bit accumulator
  - Enhanced Multiply/Divide instructions with sign and the RETI instruction
- **Instruction system compatible with high-level language (C language) and multitask**
  - Employing system stack pointer
  - Instruction set has symmetry and barrel shift instructions
- **Program Patch Function (2 address pointer)**
- **4-byte instruction queue**
- **Interrupt function**
  - The priority level can be set to programmable.
  - Interrupt function with 32 factors
- **Data transfer function**
  - Expanded intelligent I/O service function (EI 2 OS): Maximum of 16 channels]
- **Low Power Consumption Mode**
  - Sleep mode (a mode that helts CPU operating clock)
  - Time-base timer mode (a mode that operates oscillation clock and time-base timer)
  - Watch timer mode (mode in which only the subclock and watch timers operate)
  - Stop mode (a mode that stops oscillation clock and sub clock)
  - CPU blocking operation mode (operating CPU at each set cycle)
- **Package**
  - LQFP-120P (FPT-100P-M06:0.65 mm pin pitch)
- **Process : CMOS technology**

■ BUILT-IN PERIPHERAL FUNCTION (RESOURCE)

- **I/O port : 68 or less (sub-clocking 70 unused)**
- **Time-base timer : 1channel**
- **Watchdog timer : 1 channel**
- **Watch timer : 1channel**
- **LCD Controller**
  - 48SEG 4COM
- **8/10-bit A/D converter : 12 channels**
  - 8-bit resolution or 10-bit resolution can be set.
- **16-bit reload timer : 3 channels**
- **Multi-functional timer**
  - 16-bit free run timer : 1 channel
  - 16-bit Output Compare : 2 channels
    An interrupt request can be output when the count value of the 16-bit free-run timer and the setting value in the compare register match.
  - Input capture : 2 channels
    Upon detecting a valid edge of the signal input from the external input pin, the count value of the 16-bit free-run timer is loaded into the input capture data register and an interrupt request can be output.
  - 16-bit PPG timer : 2 channels
  - 16-bit reload timer : 3 channels
- **UART : 2 channels**
- **Extended I/O serial interface : 2 channels**
- **DTP/External interrupt circuit : 4 channels**
  - Activate the extended intelligent I/O service by external interrupt input
  - Interrupt output by external interrupt input
- **Timer clock output circuit**
- **Delay interrupt output module**
  - Output an interrupt request for task switching
- **I^2C Interface : 1 channel**

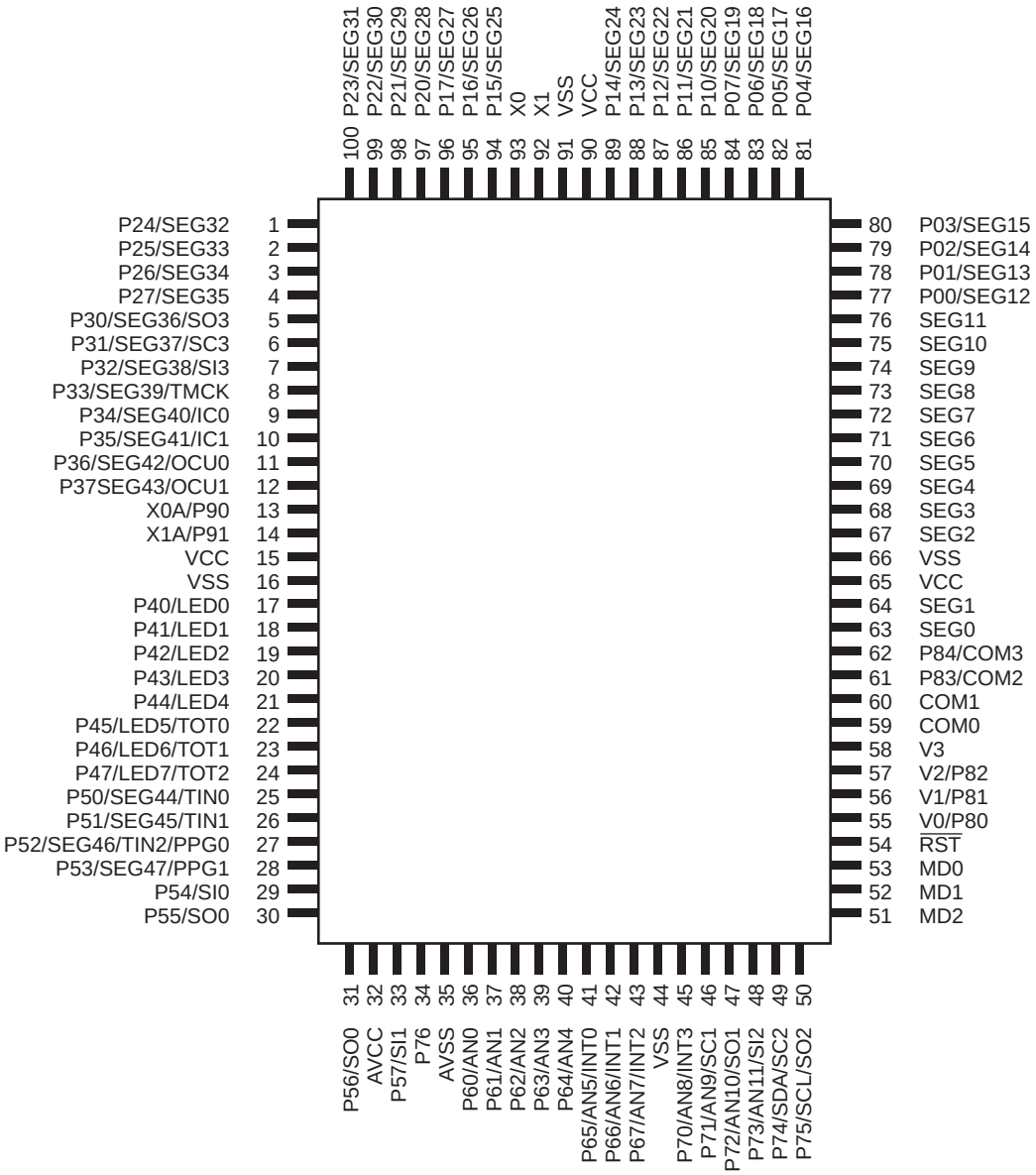
■ PRODUCT LINEUP

1. MB90800 Series

Part number		MB90V800	MB90F804-101/201	MB90803/S
Type		For evaluation	FLASH MEMORY built-in type	Mask ROM built-in type
System clock		On-chip PLL clock multiplication method(× 1, × 2, × 3, × 4, 1/2 when PLL stops) Minimum instruction execution time of 40.0 ns (at oscillation of 6.25 MHz, four times the PLL clock)		
ROM capacity		No	256 Kbytes	128 Kbytes
RAM capacity		28 Kbytes	16 Kbytes	4 Kbytes
CPU functions		Number of basic instructions : 351 Minimum instruction execution time : 40.0 ns/6.25 MHz oscillator (When four times is used : machine clock 25 MHz, Power supply voltage : 3.3 V ± 0.3 V) Addressing type : 23 types Program Patch Function : 2 address pointers The maximum memory space : 16MB		
Ports		I/O port (CMOS) 68 ports (shared with resources), (70 ports when the subclock is not used)		
LCD controller/driver		Segment driver that can drive the LCD panel (liquid crystal display) directly, and common driver 48 SEG × 4 COM		
16-bit input/ output timer	16-bit free-run timer	1 channel Overflow interrupt		
	Output compare (OCU)	2 channels Pin input factor: matching of the compare register		
	Input capture (ICU)	2 channels Rewriting a register value upon a pin input (rising edge, falling edge, or both edges)		
16-Bit Reload Timer		16-bit reload timer operation (toggle output, single shot output selectable) The event count function is optional. The event count function is optional. Three channels are built in.		
16-bit PPG timer		Output pin × 2 ports Operating clock frequency : fcp, fcp/22, fcp/24, fcp/26 Two channels are built in.		
Timer clock output circuit		Clock with a frequency of external input clock divided by 16/32/64/128 can be output externally.		
I^2C bus		I^2C Interface. 1 channel is built-in.		
8/10-bit A/D converter		12 channels (input multiplex) The 8-bit resolution or 10-bit resolution can be set. Conversion time : 5.9 μs (When machine clock 16.8 MHz works).		
UART		Full-duplex double buffer Asynchronous/synchronous transmit (with start/stop bits) are supported. Two channels are built in.		
Extended I/O serial interface		Two channels are built in.		
Interrupt delay interrupt		Four channel independence (A/D input and using combinedly) Interrupt causes : “L”→“H” edge/“H”→“L” edge/“L” level/“H” level selectable		
DTP/External interrupt		8 channels (The 8 channels include with the shared A/D input) Interrupt causes : “L”→“H” edge/“H”→“L” edge/“L” level/“H” level selectable		
Low Power Consumption Mode		Sleep mode/Timebase timer mode/Watch mode/Stop mode/CPU intermittent mode		
Process		CMOS		
Operating voltage		2.7 V to 3.6 V		

■ PIN ASSIGNMENT

(TOP VIEW)



(FPT-100P-M06)

■ PIN DESCRIPTION

Pin No. QFP	Pin Name	Circuit Type*	Status/function at reset	Description
92, 93	X0, X1	A	Oscillation status	It is a terminal which connects the oscillator. When connecting an external clock, leave the x1 pin side unconnected.
13, 14	X0A, X1A	B	Oscillation status	It is 32 kHz oscillation pin. (Dual-line model)
	P90, P91	G	Port input (High-Z)	General purpose input/output port. (Single-line model)
51	MD2	M	Mode Pins	Input pin for selecting operation mode. Connect directly to Vss.
52, 53	MD1, MD0	L	Mode Pins	Input pin for selecting operation mode. Connect directly to Vcc.
54	$\overline{RST}$	K	Reset input	External reset input pin.
63, 64, 67 to 72, 73 to 76	SEG0 to SEG11	D	LCD SEG output	A segment output terminal of the LCD controller/ driver.
77 to 84	SEG12 to SEG19	E	Port input (High-Z)	A segment output terminal of the LCD controller/ driver.
	P00 to P07			General purpose input/output port.
85 to 89, 94 to 96	SEG20 to SEG27	E		A segment output terminal of the LCD controller/ driver.
	P10 to P17			General purpose input/output port.
97 to 100, 1 to 4	SEG28 to SEG35	E		A segment output terminal of the LCD controller/ driver.
	P20 to P27			General purpose input/output port.
5	SEG36	E		A segment output terminal of the LCD controller/ driver.
	P30			General purpose input/output port.
	SO3			Serial data output pin of serial I/O channel 3. Valid when serial data output of serial I/O channel 3 is enabled.
6	SEG37	E		A segment output terminal of the LCD controller/ driver.
	P31			General purpose input/output port.
	SC3			Serial clock I/O pin of serial I/O channel 3. Valid when serial clock output of serial I/O channel 3 is enabled.

* : For the circuit type, see section "■ I/O CIRCUIT TYPE".

(Continued)

Pin No. QFP	Pin Name	Circuit Type*	Status/function at reset	Description
7	SEG38	E	Port input (High-Z)	A segment output terminal of the LCD controller/ driver.
	P32			General purpose input/output port.
	SI3			Serial data input pin of serial I/O channel 3. This pin may be used at any time during serial I/O channel 3 in input mode, so do not use it as other pin function.
8	SEG39	E		A segment output terminal of the LCD controller/ driver.
	P33			General purpose input/output port.
	TMCK			Timer clock output pin. It is effective when permitting the power output.
9, 10	SEG40, SEG41	E		A segment output terminal of the LCD controller/ driver.
	P34, P35			General purpose input/output port.
	IC0, IC1			External trigger input pin of input capture channel 0/ channel 1.
11, 12	SEG42, SEG43	E		A segment output terminal of the LCD controller/ driver.
	P36, P37			General purpose input/output port.
	OCU0, OCU1			Output terminal for the Output Compares.
17 to 21	LED0 to LED4	F		It is a output terminal for LED (I_{OL} = 15 mA).
	P40 to P44			General purpose input/output port.
22 to 24	LED5 to LED7	F		It is a output terminal for LED (I_{OL} = 15 mA).
	P45 to P47			General purpose input/output port.
	TOT0 to TOT2			External event output pin of reload timer channel 0 to chanel 2. It is effective when permitting the external event output.
25, 26	SEG44 to SEG45	E		A segment output terminal of the LCD controller/ driver.
	P50, P51			General purpose input/output port.
	TIN0, TIN1			External clock input pin of reload timer channel 0, channel 1. It is effective when permitting the external clock input.

* : For the circuit type, see section "■ I/O CIRCUIT TYPE".

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Pin No. QFP	Pin Name	Circuit Type*	Status/function at reset	Description
27	SEG46	E	Port input (High-Z)	A segment output terminal of the LCD controller/ driver.
	P52			General purpose input/output port.
	TIN2			External clock input pin of reload timer channel 2. It is effective when permitting the external clock input.
	PPG0			PPG timer (ch0) output pin.
28	SEG47	E		A segment output terminal of the LCD controller/ driver.
	P53			General purpose input/output port.
	PPG1			PPG (ch1) timer output pin.
29	SIO	G		Serial data input pin of UART channel 0. This pin may be used at any time during UART channel 0 in receiving mode, so do not use it as other pin function.
	P54			General purpose input/output port.
30	SC0	G		Serial clock input/output pin of UART channel 0. It is effective when permitting the serial clock output of UART channel 0.
	P55			General purpose input/output port.
31	SO0	G		Serial data output pin of UART channel 0. It is effective when permitting the serial clock output of UART channel 0.
	P56			General purpose input/output port.
33	SI1	G		Serial data input pin of UART channel 1. This pin may be used at any time during UART channel 1 in receiving mode, so do not use it as other pin function.
	P57			General purpose input/output port.
34	P76	G		General purpose input/output port.
36 to 40	AN0 to AN4	I		Analog input pin channel 0 to channel 4 of A/D converter. Enabled when analog input setting is " enabled "(set by ADER).
	P60 to P64			General purpose input/output port.

* : For the circuit type, see section “■ I/O CIRCUIT TYPE”.

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Pin No. QFP	Pin Name	Circuit Type*	Status/function at reset	Description
41 to 43	AN5 to AN7	I	Analog input (High-Z)	Analog input pin channel 5 to channel 7 of A/D converter. Enabled when analog input setting is " enabled "(set by ADER).
	P65 to P67			General purpose input/output port.
	INT0 to INT2			Functions as an external interrupt ch0 to ch2 input pin.
45	AN8	I		Analog input pin channel 8 of A/D converter. Enabled when analog input setting is " enabled "(set by ADER).
	P70			General purpose input/output port.
	INT3			Functions as an external interrupt ch3 input pin.
46	AN9	I	Port input (High-Z)	Analog input pin channel 9 of A/D converter. Enabled when analog input setting is " enabled "(set by ADER).
	P71			General purpose input/output port.
	SC1			Serial clock input/output pin of UART channel 1. It is effective when permitting the serial clock output of UART channel 1.
47	AN10	I		Analog input pin channel 10 of A/D converter. Enabled when analog input setting is " enabled "(set by ADER).
	P72			General purpose input/output port.
	SO1			Serial data output pin of serial I/O channel 1. Valid when serial data output of serial I/O channel 1 is enabled.
48	AN11	I		Analog input pin channel 11 of A/D converter. Enabled when analog input setting is " enabled "(set by ADER).
	P73			General purpose input/output port.
	SI2			Serial data input pin of serial I/O channel 2. This pin may be used at any time during serial I/O channel 2 in input mode, so do not use it as other pin function.

* : For the circuit type, see section “■ I/O CIRCUIT TYPE”.

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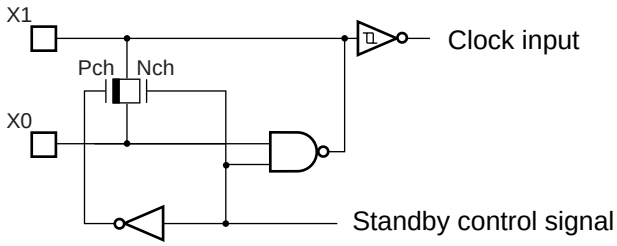
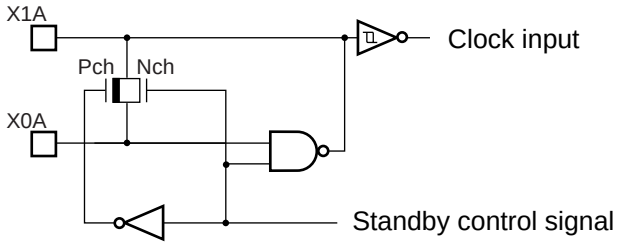
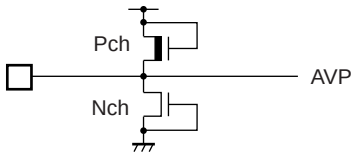
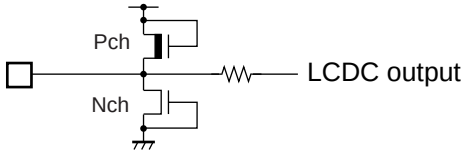
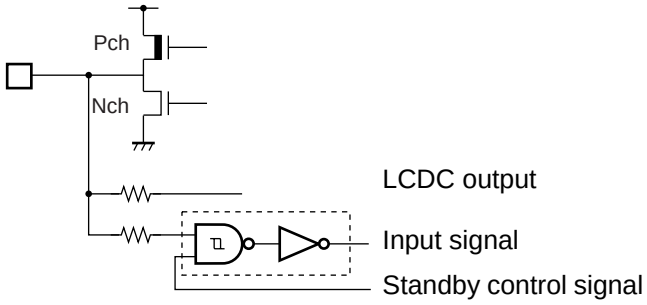
Pin No. QFP	Pin Name	Circuit Type*	Status/function at reset	Description
49	SDA	H	Port input (High-Z)	Data input/output pin of I²C Interface. This function is enabled when the operation of the I²C interface is permitted. While the I²C interface is running, the port must be set for input use.
	P74			General purpose input/output port. (N-ch open drain)
	SC2			Serial clock input pin of serial I/O channel 2. Valid when serial clock output of serial I/O channel 2 is enabled.
50	SCL	H		Clock input/output pin of I²C Interface. This function is enabled when the operation of the I²C interface is permitted. While the I²C interface is running, the port must be set for input use.
	P75			General purpose input/output port. (N-ch open drain)
	SO2			Serial data output pin of serial I/O channel 2. Valid when serial data output of serial I/O channel 2 is enabled.
55 to 57	V0 to V2	J	LCD drive power supply input	LCD controller/driver. Reference power terminals of LCD controller/driver.
	P80 to P82			General purpose input/output port.
59, 60	COM0, COM1	D	LCD COM output	A common output terminal of the LCD controller/ driver.
61, 62	P83, P84	E	Port input (Hi-Z)	General purpose input/output port.
	COM2, COM3			A common output terminal of the LCD controller/ driver.
32	AVCC	C	Power supply	A/D converter exclusive power supply input pin.
35	AVSS	C		A/D converter-exclusive GND power supply pin.
58	V3	J		LCD controller/driver Reference power terminals of LCD controller/driver.
15, 65, 90	VCC	—		These are power supply input pins.
16, 44, 66, 91	VSS	—		GND power supply pin.

* : For the circuit type, see section “■ I/O CIRCUIT TYPE”.

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		• Oscillation feedback resistance : 1 MΩ approx.
B		• Low-rate oscillation feedback resistor, approx.10 MΩ
C		• Analog power supply input protection circuit
D		• LCDC output
E		• CMOS output • LCDC output • Hysteresis input (With input interception function at standby)

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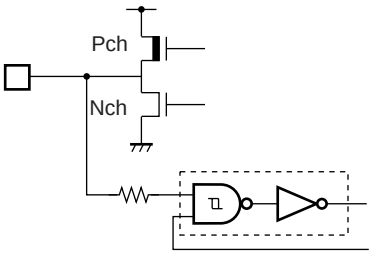
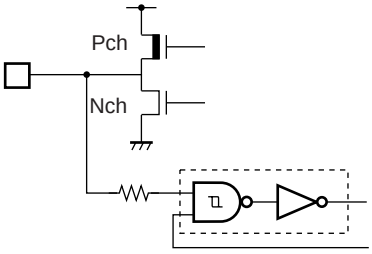
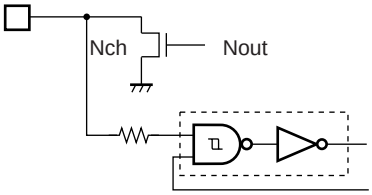
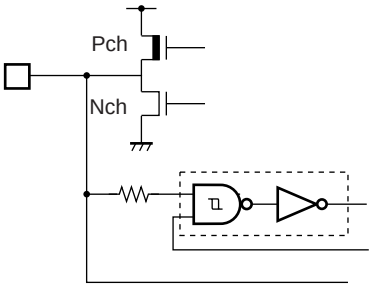
Type	Circuit	Remarks
F		• CMOS output (Heavy-current I_{OL} =15 mA for LED drive) • Hysteresis input (With input interception function at standby)
G		• CMOS output • CMOS hysteresis input (With input interception function at standby) <Note> Output of input/output port and built-in resource share one output buffer. Input of input/output port and built-in resource share one input buffer.
H		• Hysteresis input (With input interception function at standby) • N-ch open drain output
I		• CMOS output • CMOS hysteresis input (With input interception function at standby) • Analog input (If the bit of analog input enable register = 1, the analog input of A/D converter is enabled.) <Note> Outp put of input/output port and built-in resource share one output buffer. Input of input/output port and built-in resource share one input buffer.

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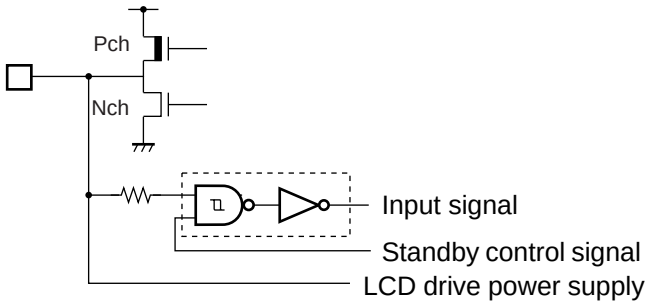
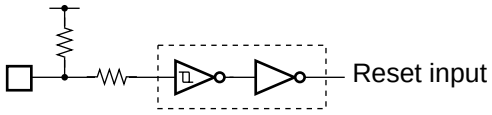
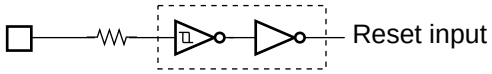
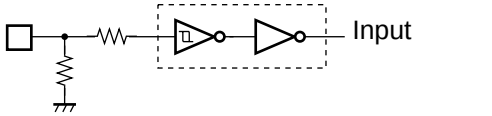
Type	Circuit	Remarks
J		• CMOS output • CMOS hysteresis input (With input interception function at standby) • LCD drive power supply input
K		• CMOS hysteresis input with pull-up resistor.
L		• CMOS hysteresis input
M		• CMOS hysteresis input with pull-down resistor

■ HANDLING DEVICES

1. Preventing Latchup, Turning on Power Supply

Latchup may occur on CMOSICs under the following conditions:

- If a voltage higher than V_{CC} or lower than V_{SS} is applied to input and output pins,
- A voltage higher than the rated voltage is applied between V_{CC} and V_{SS}.
- If the AV_{CC} power supply is turned on before the V_{CC} voltage.

Ensure that you apply a voltage to the analog power supply at the same time as V_{CC} or after you turn on the digital power supply (when you perform power-off, turn off the analog power supply first or at the same time as V_{CC} and the digital power supply).

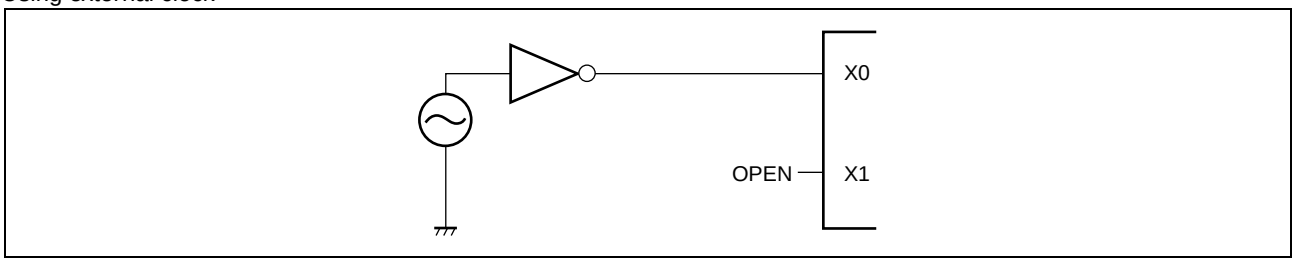
When latchup occurs, power supply current increases rapidly and might thermally damage elements. When using CMOSICs, take great care to prevent the occurrence of latchup.

2. Treatment of unused pins

Leaving unused input pins open could cause malfunctions. They should be connected to pull-up or pull-down registor. If the A/D converter is not used, connect the pins under the following conditions: AVcc = Vcc and AVss = Vss.

3. About the attention when the external clock is used

• Using external clock



4. Treatment of power supply pins (V_{CC}/V_{SS})

To prevent malfunctions of strobe signals due to the rise in the ground level, lower the level of unnecessary electro-magnetic emission, and prevent latchup, and conform to the total current rating in designing devices if multiple V_{CC} or V_{SS} pins exist. Pay attention to connect a power supply to V_{CC} and V_{SS} of MB90800 series device in a lowest-possible impedance. In addition, near pins of MB90800 series device, connecting a bypass capacitor is recommended at 0.1 μF across V_{CC} and V_{SS}.

5. Crystal oscillators circuit

Noise near the X0/X1 and X0A/X1A pin may cause the device to malfunction. Design a print circuit so that X0/X1 and X0A/X1A, a crystal oscillator (or a ceramic oscillator) , and bypass capacitor to the ground become as close as possible to each other. Furthermore, avoid wires to crossing each other as much as possible. It is highly recommended that you should use a printed circuit board artwork because you can expect stable operations from it.

6. Caution on Operations during PLL Clock Mode

If the PLL clock mode is selected, the microcontroller attempt to be working with the self-oscillating circuit even when there is no external oscillator or external clock input is stopped. Performance of this operation, however, cannot be guaranteed. Performance of this operation, however, cannot be guaranteed.

7. Stabilization of Supply Power Supply

A sudden change in the supply voltage may cause the device to malfunction even within the V_{CC} supply voltage operating range.Therefore, the V_{CC} supply voltage should be stabilized. For reference, the supply voltage should be controlled so that V_{CC} ripple variations (peak- to-peak values) at commercial frequencies (50 MHz/60 Mhz) fall below 10% of the standard V_{CC} supply voltage and the coefficient of fluctuation does not exceed 0.1 V/ms at instantaneous power switching.

8. Note on Using the two-subsystem product as one-subsystem product

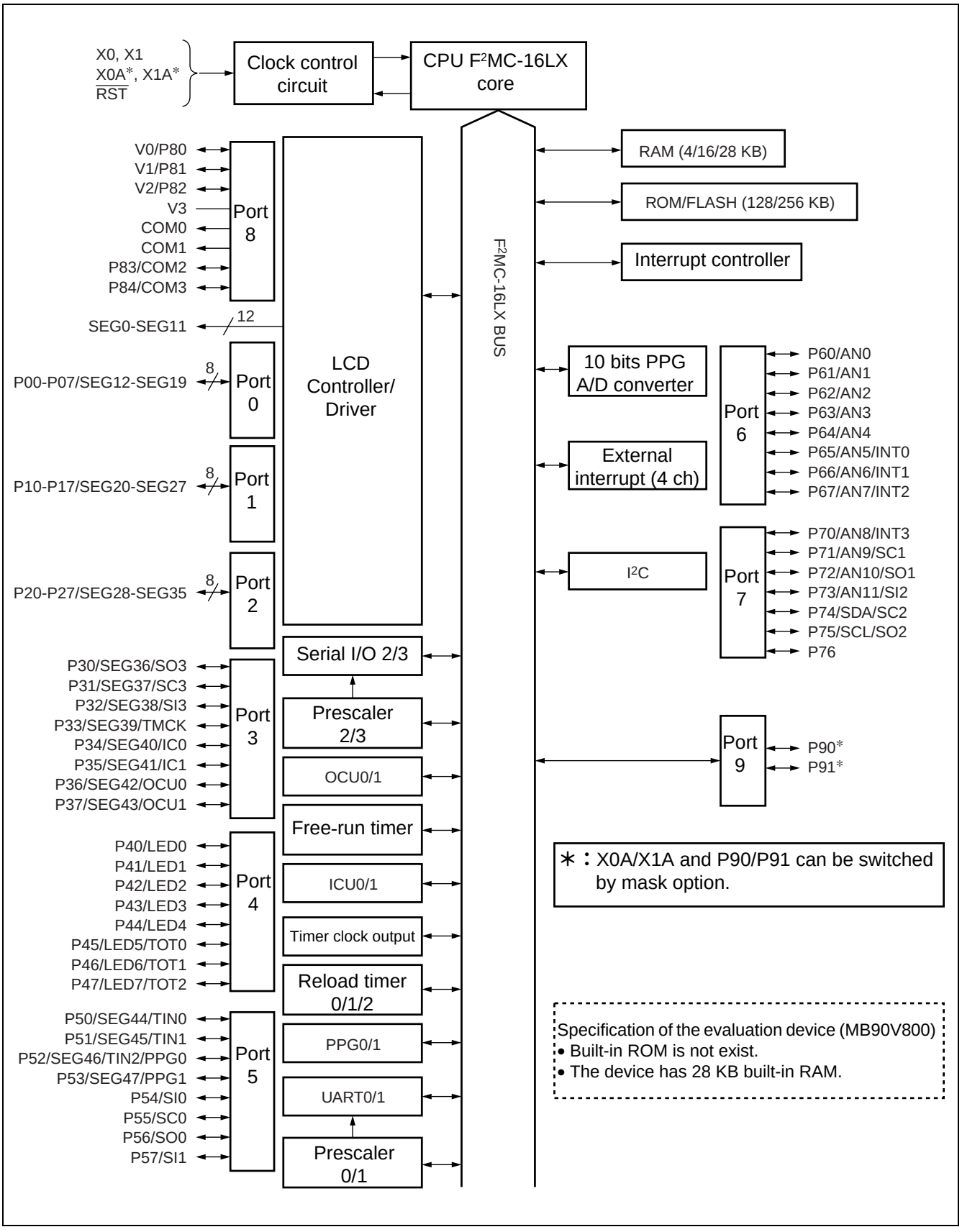
If you are using only one subsystem of the MB90800 series that come in one two-subsystem product, use it with X0A = VSS and X1A = OPEN.

9. Write to FLASH

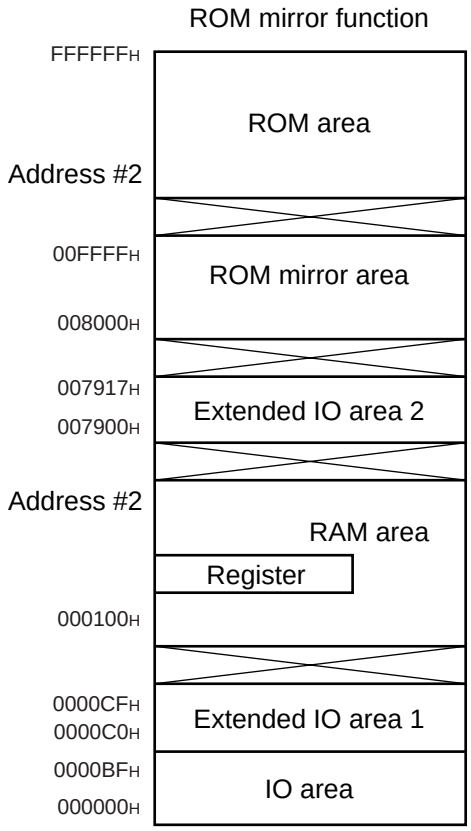
Ensure that you must write to FLASH at the operating voltage V_{CC} = 3.13 V to 3.6 V.

Ensure that you must normal write to FLASH at the operating voltage V_{CC} = 3.0 V to 3.6 V.

■ BLOCK DIAGRAM



■ MEMORY MAP



Part number	Address #1	Address #2
MB90803	0010FFH	FE0000H
MB90F804	0040FFH	FC0000H
MB90V800	0070FFH	F80000H*

* : ROM is not built into V products.
I must think ROM decipherment region on the tool side.

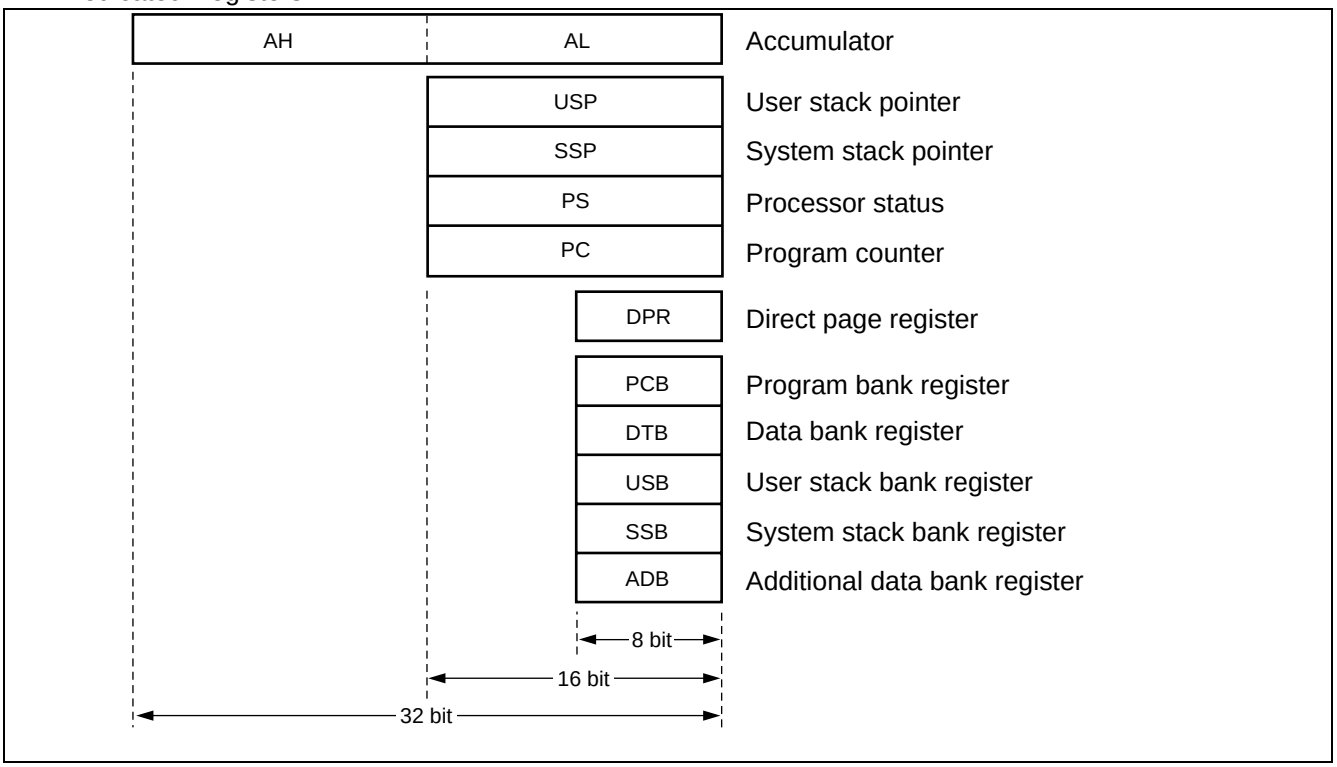
Memory Map of MB90800 Series

Notes :
- When the ROM mirror function register has been set, the mirror image data at higher addresses ("FF4000H to FFFFFFH") of bank FF is visible from the higher addresses (" 008000H to 00FFFFH ") of bank 00.
- For setting of the ROM mirror function, see “■ PERIPHERAL RESOURCE 17. ROM Mirror Function Selection Module”.

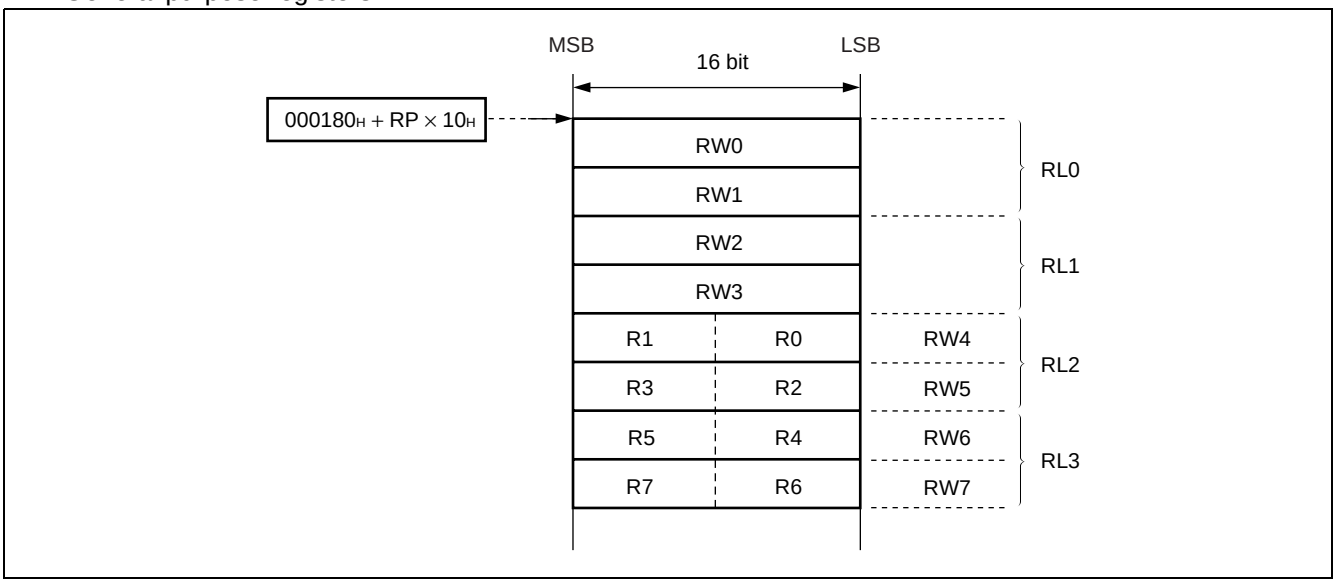
Reference:
- The ROM mirror function is for using the C compiler small model.
- The lower 16-bit addresses of bank FF are equivalent to those of bank 00. Note that because the ROM area of bank FF exceeds
  32 K bytes, all data in the ROM area cannot be shown in mirror image in bank 00.
- When the C compiler small model is used, the data table mirror image can be shown at " 008000H to 00FFFFH " by storing the data table at " FF8000H to FFFFFFH. Therefore, data tables in the ROM area can be referenced without declaring the far addressing with the pointer.

■ F²MC-16L CPUProgramming model

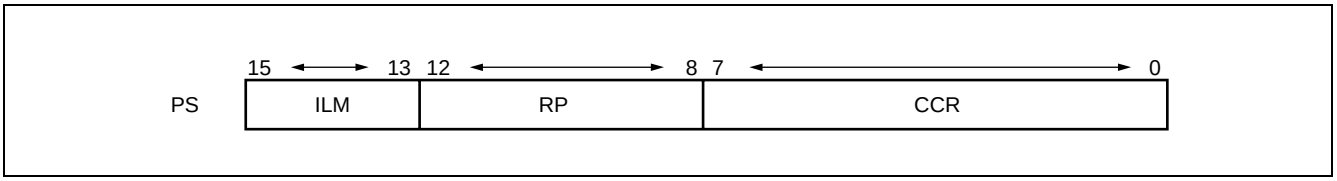
- Dedicated Registers



- General purpose registers



- Processor status



■ I/O MAP

Address	Register abbreviation	Register	Read/ Write	Resource name	Initial Value
000000H	PDR0	Port 0 data register	R/W	Port 0	XXXXXXXXB
000001H	PDR1	Port 1 data register	R/W	Port 1	XXXXXXXXB
000002H	PDR2	Port 2 data register	R/W	Port 2	XXXXXXXXB
000003H	PDR3	Port 3 data register	R/W	Port 3	XXXXXXXXB
000004H	PDR4	Port 4 data register	R/W	Port 4	XXXXXXXXB
000005H	PDR5	Port 5 data register	R/W	Port 5	XXXXXXXXB
000006H	PDR6	Port 6 data register	R/W	Port 6	XXXXXXXXB
000007H	PDR7	Port 7 data register	R/W	Port 7	- XXXXXXXB
000008H	PDR8	Port 8 data register	R/W	Port 8	- - - XXXXXB
000009H	PDR9	Port 9 data register	R/W	Port 9	- - - - - - XXB
00000AH to 00000FH	Prohibited				
000010H	DDR0	Port 0 direction register	R/W	Port 0	0 0 0 0 0 0 0 0B
000011H	DDR1	Port 1 direction register	R/W	Port 1	0 0 0 0 0 0 0 0B
000012H	DDR2	Port 2 direction register	R/W	Port 2	0 0 0 0 0 0 0 0B
000013H	DDR3	Port 3 direction register	R/W	Port 3	0 0 0 0 0 0 0 0B
000014H	DDR4	Port 4 direction register	R/W	Port 4	0 0 0 0 0 0 0 0B
000015H	DDR5	Port 5 direction register	R/W	Port 5	0 0 0 0 0 0 0 0B
000016H	DDR6	Port 6 direction register	R/W	Port 6	0 0 0 0 0 0 0 0B
000017H	DDR7	Port 7 direction register	R/W	Port 7	- 0 0 0 0 0 0 0B
000018H	DDR8	Port 8 direction register	R/W	Port 8	- - - 0 0 0 0 0B
000019H	DDR9	Port 9 direction register	R/W	Port 9	- - - - - - 0 0B
00001AH to 00001DH	Prohibited				
00001EH	ADER0	Analog input enable 0	R/W	Port 6, A/D	1 1 1 1 1 1 1 1B
00001FH	ADER1	Analog input enable 1	R/W	Port 7, A/D	- - - - 1 1 1 1B
000020H	SMR0	Mode Register ch0	R/W	UART0	0 0 0 0 0 - 0 0B
000021H	SCR0	Control register ch0	R/W		0 0 0 0 0 1 0 0B
000022H	S1DR0/ SODR0	Input/output data register ch0	R/W		XXXXXXXXB
000023H	SSR0	Status register ch0	R/W		0 0 0 0 1 0 0 0B
000024H	Prohibited.				
000025H	CDCR0	Communication prescaler control register ch0	R/W	Prescaler 0	0 0 - - 0 0 0 0B
000026H to 000027H	Prohibited				

(Continued)

Address	Register abbreviation	Register	Read/ Write	Resource name	Initial Value
000028H	SMR1	Mode Register ch1	R/W	UART1	0 0 0 0 0 - 0 0B
000029H	SCR1	Control register ch1	R/W		0 0 0 0 0 1 0 0B
00002AH	SIDR1/ SODR1	Input/output data register ch1	R/W		XXXXXXXXB
00002BH	SSR1	Status register ch1	R/W		0 0 0 0 1 0 0 0B
00002CH	Prohibited				
00002DH	CDCR1	Communication prescaler control register ch1	R/W	Prescaler 1	0 0 - - 0 0 0 0B
00002EH	Prohibited				
00002FH					
000030H	ENIR	External interrupt enable	R/W	External interrupt	- - - - 0 0 0 0B
000031H	EIRR	External interrupt request	R/W		XXXXXXXXB
000032H	ELVR	External interrupt level (lower)	R/W		0 0 0 0 0 0 0 0B
000033H	Prohibited				
000034H	ADCS0	A/D control status register (lower)	R/W	A/D converter	0 0 - - - - - - B
000035H	ADCS1	A/D control status register (upper)	R/W		0 0 0 0 0 0 0 0B
000036H	ADCR0	A/D data register (lower)	R		XXXXXXXXB
000037H	ADCR1	A/D data register (upper)	R/W		0 0 1 0 1 XXXB
000038H	Prohibited				
000039H	ADMR	A/D conversion channel set register	R/W	A/D converter	0 0 0 0 0 0 0 0B
00003AH	CPCLR	Compare clear register	R/W	16-bit free-run timer	XXXXXXXXB
00003BH					XXXXXXXXB
00003CH	TCDT	Timer Data register	R/W		0 0 0 0 0 0 0 0B
00003DH					0 0 0 0 0 0 0 0B
00003EH	TCCSL	Timer control status register (lower)	R/W		0 0 0 0 0 0 0 0B
00003FH	TCCSH	Timer control status register (upper)	R/W		0 - - 0 0 0 0 0B
000040H to 000043H	Prohibited				
000044H	IPCP0	Input Capture register 0	R	Input Capture 0/1	XXXXXXXXB
000045H					XXXXXXXXB
000046H	IPCP1	Input Capture register 1			XXXXXXXXB
000047H					XXXXXXXXB
000048H	ICS01	Input capture control status 0/1	R/W		0 0 0 0 0 0 0 0B
000049H	Prohibited				
00004AH	OCCP0	Output Compare register 0	R/W	Output compare 0	XXXXXXXXB
00004BH					XXXXXXXXB
00004CH	OCCP1	Output Compare register 1	R/W	Output compare 1	XXXXXXXXB
00004DH					XXXXXXXXB

(Continued)

Address	Register abbreviation	Register	Read/ Write	Resource name	Initial Value
00004E$_H$	OCSL	Output compare control status (lower)	R/W	Output Compare 0/1	0 0 0 0 - - 0 0$_B$
00004F$_H$	OCSH	Output compare control status (upper)	R/W		- - - 0 0 0 0 0$_B$
000050$_H$	TMCSR0L	Timer control status register 0 (lower)	R/W	16-bit reload timer 0	0 0 0 0 0 0 0 0$_B$
000051$_H$	TMCSR0H	Timer Control Status register 0 (upper)	R/W		- - - - 0 0 0 0$_B$
000052$_H$	TMR0/ TMRLR0	Timer register 0/Reload register 0	R/W		XXXXXXXX$_B$
000053$_H$					XXXXXXXX$_B$
000054$_H$	TMCSR1L	Timer control status register 1 (lower)	R/W	Reload timer 1	0 0 0 0 0 0 0 0$_B$
000055$_H$	TMCSR1H	Timer control status register 1 (upper)	R/W		- - - - 0 0 0 0$_B$
000056$_H$	TMR1/ TMRLR1	Timer register 1/Reload register 1	R/W		XXXXXXXX$_B$
000057$_H$					XXXXXXXX$_B$
000058$_H$	TMCSR2L	Timer control status register 2 (lower)	R/W	Reload timer 2	0 0 0 0 0 0 0 0$_B$
000059$_H$	TMCSR2H	Timer control status register 2 (upper)	R/W		- - - - 0 0 0 0$_B$
00005A$_H$	TMR2/ TMRLR2	Timer register 2/Reload register 2	R/W		XXXXXXXX$_B$
00005B$_H$					XXXXXXXX$_B$
00005C$_H$	LCRL	LCDC control register (lower)	R/W	LCD controller/ driver	0 0 0 1 0 0 0 0$_B$
00005D$_H$	LCRH	LCDC control register (upper)	R/W		0 0 0 0 0 0 0 0$_B$
00005E$_H$	LCRR	LCDC range register	R/W		0 0 0 0 0 0 0 0$_B$
00005F$_H$	Prohibited				
000060$_H$	SMCS0	Serial mode control status register (ch2)	R/W	SIO (Extended Serial I/O)	- - - - 0 0 0 0$_B$
000061$_H$					0 0 0 0 0 0 1 0$_B$
000062$_H$	SDR0	Serial Data Register (ch2)	R/W		XXXXXXXX$_B$
000063$_H$	SDCR0	Control register of clock dividing frequency (ch2)	R/W	Communication prescaler (SIO)	0 - - - 0 0 0 0$_B$
000064$_H$	SMCS1	Serial mode control status register (ch3)	R/W	SIO (Extended Serial I/O)	- - - - 0 0 0 0$_B$
000065$_H$					0 0 0 0 0 0 1 0$_B$
000066$_H$	SDR1	Serial Data Register (ch3)	R/W		XXXXXXXX$_B$
000067$_H$	SDCR1	Control register of clock dividing frequency (ch3)	R/W	Communication prescaler (SIO)	0 - - - 0 0 0 0$_B$
000068$_H$	Prohibited				
000069$_H$					
00006A$_H$	IBSR	I^{2}C bus status register	R	I^{2}C	0 0 0 0 0 0 0 0$_B$
00006B$_H$	IBCR	I^{2}C bus control register	R/W		0 0 0 0 0 0 0 0$_B$
00006C$_H$	ICCR	I^{2}C bus clock selection register	R/W		- - 0XXXXX$_B$
00006D$_H$	IADR	I^{2}C bus address register	R/W		- XXXXXXX$_B$
00006E$_H$	IDAR	I^{2}C bus data register	R/W		XXXXXXXX$_B$
00006F$_H$	ROMM	ROM mirror	W	ROM mirror	XXXXXXX1$_B$

(Continued)

Address	Register abbreviation	Register	Read/ Write	Resource name	Initial Value
000070H	PDCRL0	PPG0 down counter register	R	16 bit PPG0	1 1 1 1 1 1 1 1B
000071H	PDCRH0				1 1 1 1 1 1 1 1B
000072H	PCSRL0	PPG0 cycle set register	W		XXXXXXXXB
000073H	PCSRH0				XXXXXXXXB
000074H	PDUTL0	PPG0 duty setting register	W		XXXXXXXXB
000075H	PDUTH0				XXXXXXXXB
000076H	PCNTL0	PPG0 control status register	R/W		- - 0 0 0 0 0 0B
000077H	PCNTH0				0 0 0 0 0 0 0 -B
000078H	PDCRL1	PPG1 down counter register	R	16 bit PPG1	1 1 1 1 1 1 1 1B
000079H	PDCRH1				1 1 1 1 1 1 1 1B
00007AH	PCSRL1	PPG1 cycle set register	W		XXXXXXXXB
00007BH	PCSRH1				XXXXXXXXB
00007CH	PDUTL1	PPG1 duty setting register	W		XXXXXXXXB
00007DH	PDUTH1				XXXXXXXXB
00007EH	PCNTL1	PPG1 control status register	R/W		- - 0 0 0 0 0 0B
00007FH	PCNTH1				0 0 0 0 0 0 0 -B
000080H to 000095H	(Reserved)				
000096H	Prohibited				
000097H	(Reserved)				
000098H to 00009DH	Prohibited				
00009EH	PACSR	ROM correction control register	R/W	ROM Correction	0 0 0 0 0 0 0 0B
00009FH	DIRR	Delayed interrupt/release	R/W	Delayed interrupt	- - - - - - - 0B
0000A0H	LPMCR	Low power consumption mode	R/W	Low power consumption control circuit	0 0 0 1 1 0 0 0B
0000A1H	CKSCR	Clock selector	R/W		1 1 1 1 1 1 0 0B
0000A2H to 0000A7H	Prohibited				
0000A8H	WDTC	Watchdog control	R/W	Watchdog timer	XXXXX 1 1 1B
0000A9H	TBTC	Time-base timer control register	R/W	Time-base timer	1 - - 0 0 1 0 0B
0000AAH	WTC	Watch timer control register	R/W	Watch timer (Sub clock)	1 X0 1 1 0 0 0B
0000ABH to 0000ADH	Prohibited				

(Continued)

(Continued)

Address	Register abbreviation	Register	Read/ Write	Resource name	Initial Value
0000AE$_H$	FMCS	Flash control register	R/W	Flash I/F	0 0 0 X 0 0 0 0$_B$
0000AF$_H$	TMCS	Timer clock output control register	R/W	Timer clock devide	XXXXX 0 0 0$_B$
0000B0$_H$	ICR00	Interrupt control register 00	R/W	Interrupt controller	0 0 0 0 0 1 1 1$_B$
0000B1$_H$	ICR01	Interrupt control register 01	R/W		0 0 0 0 0 1 1 1$_B$
0000B2$_H$	ICR02	Interrupt control register 02	R/W		0 0 0 0 0 1 1 1$_B$
0000B3$_H$	ICR03	Interrupt control register 03	R/W		0 0 0 0 0 1 1 1$_B$
0000B4$_H$	ICR04	Interrupt control register 04	R/W		0 0 0 0 0 1 1 1$_B$
0000B5$_H$	ICR05	Interrupt control register 05	R/W		0 0 0 0 0 1 1 1$_B$
0000B6$_H$	ICR06	Interrupt control register 06	R/W		0 0 0 0 0 1 1 1$_B$
0000B7$_H$	ICR07	Interrupt control register 07	R/W		0 0 0 0 0 1 1 1$_B$
0000B8$_H$	ICR08	Interrupt control register 08	R/W		0 0 0 0 0 1 1 1$_B$
0000B9$_H$	ICR09	Interrupt control register 09	R/W		0 0 0 0 0 1 1 1$_B$
0000BA$_H$	ICR10	Interrupt control register 10	R/W		0 0 0 0 0 1 1 1$_B$
0000BB$_H$	ICR11	Interrupt control register 11	R/W		0 0 0 0 0 1 1 1$_B$
0000BC$_H$	ICR12	Interrupt control register 12	R/W		0 0 0 0 0 1 1 1$_B$
0000BD$_H$	ICR13	Interrupt control register 13	R/W		0 0 0 0 0 1 1 1$_B$
0000BE$_H$	ICR14	Interrupt control register 14	R/W		0 0 0 0 0 1 1 1$_B$
0000BF$_H$	ICR15	Interrupt control register 15	R/W		0 0 0 0 0 1 1 1$_B$
001FF0$_H$	PADR0	Program address detection register 0	R/W	Address matching detection function	XXXXXXXX$_B$
001FF1$_H$			R/W		XXXXXXXX$_B$
001FF2$_H$			R/W		XXXXXXXX$_B$
001FF3$_H$	PADR1	Program address detection register 1	R/W		XXXXXXXX$_B$
001FF4$_H$			R/W		XXXXXXXX$_B$
001FF5$_H$			R/W		XXXXXXXX$_B$
007900$_H$ to 007917$_H$	VRAM	LCD display RAM	R/W	LCD controller/ driver	XXXXXXXX$_B$

- Read/Write
  - R/W Readable and Writable
  - R Read only
  - W Write only

- Initial values
  - 0 Initial Value is “0”.
  - 1 Initial Value is “1”.
  - X Initial Value is Indeterminate.

■ INTERRUPT SOURCES, INTERRUPT VECTORS AND INTERRUPT CONTROL REGISTERS

Interrupt source	EI²OS readiness	Interrupt vector			Interrupt control register		Priority
		Number*		Address	ICR	Address	
Reset	×	#08	08H	FFFFDCH	—	—	High
INT 9 instruction	×	#09	09H	FFFFD8H	—	—	
Exceptional treatment	×	#10	0AH	FFFFD4H	—	—	
DTP/External interrupt ch0	○	#11	0BH	FFFFD0H	ICR00	0000B0H	
DTP/External interrupt ch1	○	#13	0DH	FFFFC8H	ICR01	0000B1H	
Serial I/O ch2	×	#15	0FH	FFFFC0H	ICR02	0000B2H	
DTP/External interrupt ch2/3	○	#16	10H	FFFFBCH			
Serial I/O ch3	×	#17	11H	FFFFB8H	ICR03	0000B3H	
16-bit free-run timer	○	#18	12H	FFFFB4H			
Watch timer	×	#19	13H	FFFFB0H	ICR04	0000B4H	
16-Bit Reload Timer ch2	○	#21	15H	FFFFA8H	ICR05	0000B5H	
16-Bit Reload Timer ch0	△	#23	17H	FFFFA0H	ICR06	0000B6H	
16-Bit Reload Timer ch1	△	#24	18H	FFFF9CH			
Input capture ch0	△	#25	19H	FFFF98H	ICR07	0000B7H	
Input capture ch1	△	#26	1AH	FFFF94H			
PPG timer ch0 counter-borrow	○	#27	1BH	FFFF90H	ICR08	0000B8H	
Output compare match	○	#29	1DH	FFFF88H	ICR09	0000B9H	
PPG timer ch1 counter-borrow	○	#31	1FH	FFFF80H	ICR10	0000BAH	
Time-base timer	×	#33	21H	FFFF78H	ICR11	0000BBH	
UART0 reception end	◎	#35	23H	FFFF70H	ICR12	0000BCH	
UART0 transmission end	△	#36	24H	FFFF6CH			
A/D converter conversion termination	○	#37	25H	FFFF68H	ICR13	0000BDH	
I²C Interface	×	#38	26H	FFFF64H			
UART1 : Reception	◎	#39	27H	FFFF60H	ICR14	0000BEH	
UART1 : Transmission	△	#40	28H	FFFF5CH			
Flash memory status	×	#41	29H	FFFF58H	ICR15	0000BFH	
Delayed interrupt output module	×	#42	2AH	FFFF54H			Low

○ : Available
× : Unavailable
◎ : Available EI²OS function is provided.
△ : Available when a cause of interrupt sharing a same ICR is not used.

* : When interrupts of the same level are output at the same time, the interrupt with the smallest interrupt vector number has the priority.
- When there are two interrupt causes in the same interrupt control register (ICR) and use of IIOS is enabled, IIOS is started upon detection of one of the interrupt causes. As interrupts other than the start cause are masked during IIOS start, masking one of the interrupt requests is recommended when using IIOS.
- For a resource that has two interrupt causes in the same interrupt control register (ICR), the interrupt flag is cleared by an IIOS interrupt clear signal.

■ PERIPHERAL RESOURCES

1. I/O port

The I/O ports function to output data from the CPU to I/O pins via their port data register (PDR) and send signals input to I/O pins to the CPU. In addition, the port can randomly set the direction of the input/output of the I/O pin in bit by the port direction register (DDR).

The MB90800 series has 68 (70 ports when the subclock is not used) input/output pins. Port0 to port8 (port0 to port9 when the subclock is not used) are input/output port.

(1) Port data register

	7	6	5	4	3	2	1	0	Initial Value	Access
PDR0 Address : 000000H	P07	P06	P05	P04	P03	P02	P01	P00	Indeterminate	R/W*

	15	14	13	12	11	10	9	8	Initial Value	Access
PDR1 Address : 000001H	P17	P16	P15	P14	P13	P12	P11	P10	Indeterminate	R/W*

	7	6	5	4	3	2	1	0	Initial Value	Access
PDR2 Address : 000002H	P27	P26	P25	P24	P23	P22	P21	P20	Indeterminate	R/W*

	15	14	13	12	11	10	9	8	Initial Value	Access
PDR3 Address : 000003H	P37	P36	P35	P34	P33	P32	P31	P30	Indeterminate	R/W*

	7	6	5	4	3	2	1	0	Initial Value	Access
PDR4 Address : 000004H	P47	P46	P45	P44	P43	P42	P41	P40	Indeterminate	R/W*

	15	14	13	12	11	10	9	8	Initial Value	Access
PDR5 Address : 000005H	P57	P56	P55	P54	P53	P52	P51	P50	Indeterminate	R/W*

	7	6	5	4	3	2	1	0	Initial Value	Access
PDR6 Address : 000006H	P67	P66	P65	P64	P63	P62	P61	P60	Indeterminate	R/W*

	15	14	13	12	11	10	9	8	Initial Value	Access
PDR7 Address : 000007H	—	P76	P75	P74	P73	P72	P71	P70	Indeterminate	R/W*

	7	6	5	4	3	2	1	0	Initial Value	Access
PDR8 Address : 000008H	—	—	—	P84	P83	P82	P81	P80	Indeterminate	R/W*

	15	14	13	12	11	10	9	8	Initial Value	Access
PDR9 Address : 000009H	—	—	—	—	—	—	P91	P90	Indeterminate	R/W*

When reading : Read the corresponding pin level.
When writing : Write into the latch for the input/output.

- Output mode

When reading : Read the value of the data register latch.
When writing : Write into the corresponding pin.

(2) Port direction register

	7	6	5	4	3	2	1	0	Initial Value	Access
DDR0 Address : 000010H	D07	D06	D05	D04	D03	D02	D01	D 00	00000000B	R/W
DDR1 Address : 000011H	15	14	13	12	11	10	9	8	00000000B	R/W
	D17	D16	D15	D14	D13	D12	D11	D10		
DDR2 Address : 000012H	7	6	5	4	3	2	1	0	00000000B	R/W
	D27	D26	D25	D24	D23	D22	D21	D20		
DDR3 Address : 000013H	15	14	13	12	11	10	9	8	00000000B	R/W
	D37	D36	D35	D34	D33	D32	D31	D30		
DDR4 Address : 000014H	7	6	5	4	3	2	1	0	00000000B	R/W
	D47	D46	D45	D44	D43	D42	D41	D40		
DDR5 Address : 000015H	15	14	13	12	11	10	9	8	00000000B	R/W
	D57	D56	D55	D54	D53	D52	D51	D50		
DDR6 Address : 000016H	7	6	5	4	3	2	1	0	00000000B	R/W
	D67	D66	D65	D64	D63	D62	D61	D60		
DDR7 Address : 000017H	15	14	13	12	11	10	9	8	- 0000000B	R/W
	—	D76	D75	D74	D73	D72	D71	D70		
DDR8 Address : 000018H	7	6	5	4	3	2	1	0	- - - 00000B	R/W
	—	—	—	D84	D83	D82	D81	D80		
DDR9 Address : 000019H	15	14	13	12	11	10	9	8	- - - - - - 00B	R/W
	—	—	—	—	—	—	D91	D90		

- When each terminal functions as a port, each correspondent pin are controlled to following;
  0 : Input mode
  1 : Output mode This bit becomes “0” after a reset.

Note : When accessing this register by using the instruction of the read modify write system (instructions such as bit set) is mode, the bit targeted by an instruction becomes the defined value, while the content of the output register set with the other. Therefore, be sure to write an expected value into PDR firstly, and then set DDR and finally change to the output when changing the input pin to the output pin is made.

(3) Analog Input Enable register

	7	6	5	4	3	2	1	0	Initial Value	Access
ADER0 Address : 00001E$_H$	ADE7	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0	11111111$_B$	R/W
	15	14	13	12	11	10	9	8		
ADER1 Address : 00001F$_H$	—	—	—	—	ADE11	ADE10	ADE9	ADE8	- - - -1111$_B$	R/W

Control each pin of Port 6 as follows.

0 : Port input/output mode.

1 : Analog input mode.This bit becomes “1” after a reset.

2. UART

UART is a serial I/O port for asynchronous (start-stop synchronization) communication or CLK synchronous communications.

- With full-duplex double buffer
- Clock asynchronous (start-stop synchronization) , CLK synchronous communications (no start-bit/stop-bit) can be used.
- Supports multi-processor mode
- Built-in dedicated baud rate generator

  Asynchronous : 120192/60096/30048/15024/781.25 K/390.625 Kbps
  CLK synchronous : 25 M/12.5 M/6.25 M/3.125 M/1.5627 M/781.25 Kbps
- Variable baud rate can be set by an external clock.
- 7-bits data length (only asynchronous normal mode) /8-bits length
- Master/slave type communication function (at multiprocessor mode) : The communication between one (master) to n (slave) can be operating.
- Error detection functions(parity, framing, overrun)
- Transmission signal format is NRZ

(1) Register list

15	8	7	0
CDCR		—	
SCR		SMR	
SSR		SIDR (R)/SODR (W)	
← 8 bit →		← 8 bit →	

Serial mode register (SMR)

Address : 000020H / 000028H

7	6	5	4	3	2	1	0	
MD1	MD0	CS2	CS1	CS0	—	SCKE	SOE	
(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(—)	(R/W)	(R/W)	
(0)	(0)	(0)	(0)	(0)	(—)	(0)	(0)	Initial Value

Serial control register(SCR)

Address : 000021H / 000029H

15	14	13	12	11	10	9	8	
PEN	P	SBL	CL	A/D	REC	RXE	TXE	
(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(W)	(R/W)	(R/W)	
(0)	(0)	(0)	(0)	(0)	(1)	(0)	(0)	Initial Value

Serial input/output register (SIDR/SODR)

Address : 000022H / 00002AH

7	6	5	4	3	2	1	0	
D7	D6	D5	D4	D3	D2	D1	D0	
(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)	Initial Value

Serial Data Register (SSR)

Address : 000023H / 00002BH

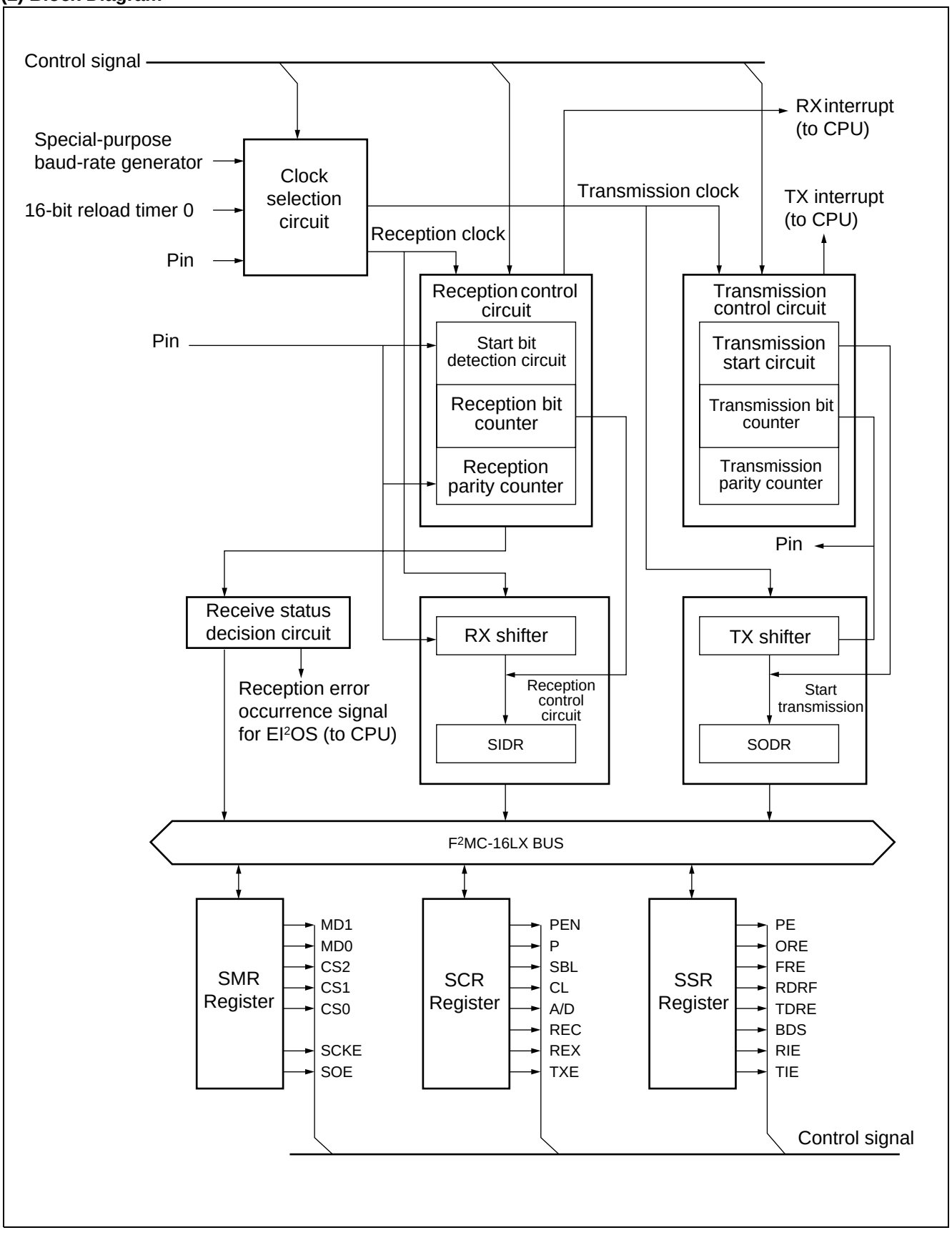
15	14	13	12	11	10	9	8	
PE	ORE	FRE	RDRF	TDRE	BDS	RIE	TIE	
(R)	(R)	(R)	(R)	(R)	(R/W)	(R/W)	(R/W)	
(0)	(0)	(0)	(0)	(1)	(0)	(0)	(0)	Initial Value

Communication prescaler control register (CDCR)

Address : 000025H / 00002DH

15	14	13	12	11	10	9	8	
MD	URST	—	—	Reserved	DIV2	DIV1	DIV0	
(R/W)	(R/W)	(—)	(—)	(R/W)	(R/W)	(R/W)	(R/W)	
(0)	(0)	(—)	(—)	(0)	(0)	(0)	(0)	Initial Value

(2) Block Diagram



3. I²C Interface

I²C interface is the serial input/output port that support Inter IC BUS and functions as the master/slave device on the I²C bus. MB90800 series have 1 channel of the built-in I²C interface.

It has the features of I²C interface below.

- Master/slave sending and receiving
- Arbitration function
- Clock synchronization function
- Slave address and general call address detection function
- Detecting transmitting direction function
- Repeat generating and detecting function of the start conditions
- Bus error detection function
- The forwarding rate can be supported to 100 Kbps.

(1) Register list

I²C status register (IBSR)

Address :00006A$_H$

7	6	5	4	3	2	1	0	Initial Value
BB	RSC	AL	LRB	TRX	AAS	GCA	FBT	00000000$_B$
R	R	R	R	R	R	R	R	

I²C control register (IBCR)

Address :00006B$_H$

15	14	13	12	11	10	9	8	
BER	BEIE	SCC	MSS	ACK	GCAA	INTE	INT	00000000$_B$
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

I²C clock control register (ICCR)

Address :00006C$_H$

7	6	5	4	3	2	1	0	
—	—	EN	CS4	CS3	CS2	CS1	CS0	XX0XXXXX$_B$
—	—	R/W	R/W	R/W	R/W	R/W	R/W	

I²C data register(IDAR)

Address :00006E$_H$

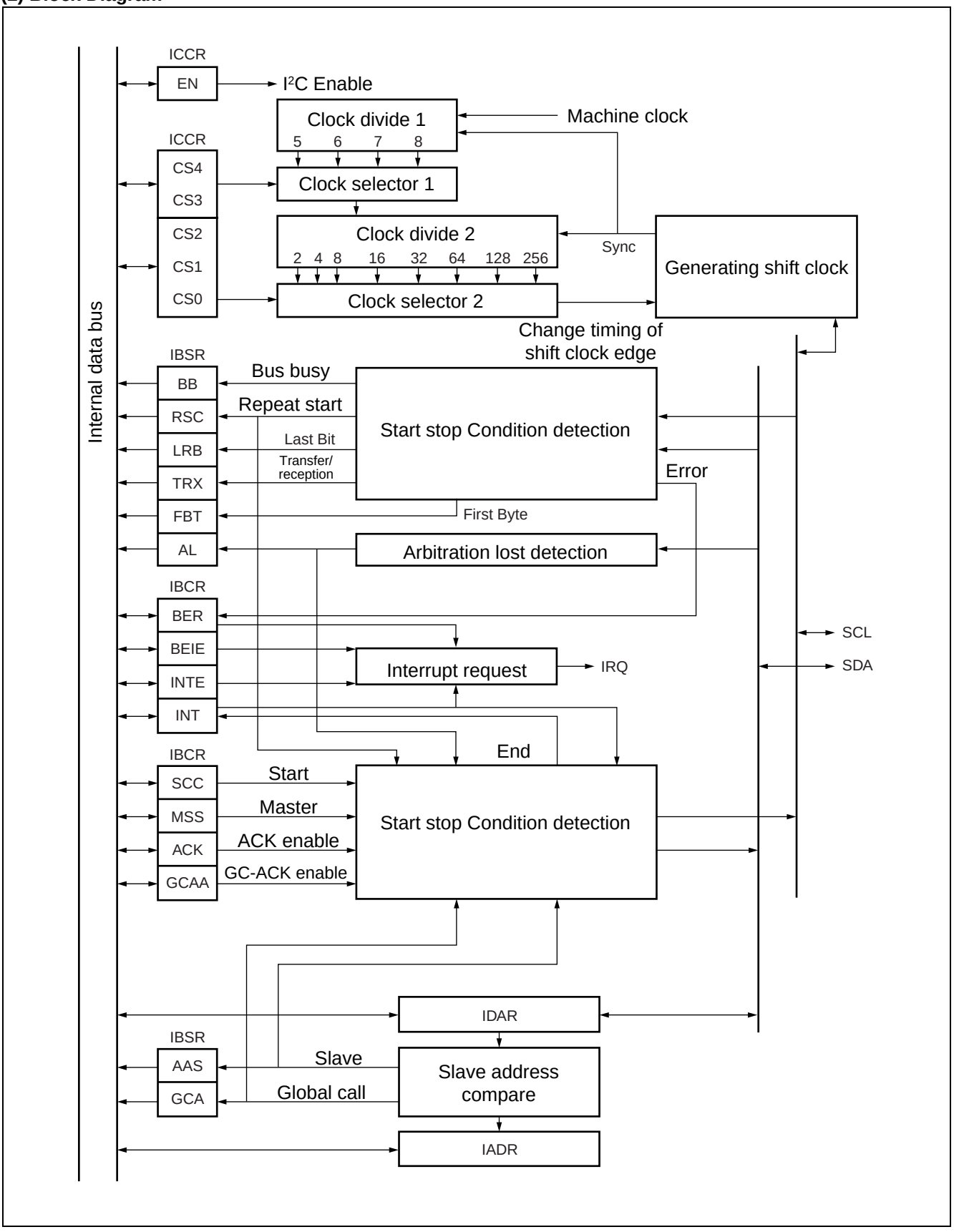
15	14	13	12	11	10	9	8	
D7	D6	D5	D4	D3	D2	D1	D0	XXXXXXXX$_B$
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

I²C address register (IADR)

Address :00006D$_H$

7	6	5	4	3	2	1	0	
—	A6	A5	A4	A3	A2	A1	A0	XXXXXXXX$_B$
—	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

(2) Block Diagram



4. Extended I/O serial interface

The extended I/O serial interface is a serial I/O interface that can transfer data through the adoption of 8 bit × 2 channel configured clock synchronization scheme. The extended I/O serial interface also has two alternatives in data transfer called LSB first and MSB sirst.

The serial I/O interface operates in two modes:

- Internal shift clock mode : Transfer data in sync with the internal clock.
- External shift clock mode : Transfers data in sync with the clock input through an external pin (SCK) . In this mode, transfer operation performed by the CPU instruction is also available by operating the general-use port sharing an external pin (SCK) .

(1) Register list

Serial mode control status register(SMCS)

Address :	15	14	13	12	11	10	9	8	Initial Value
000060H 000064H	SMD2	SMD1	SMD0	SIE	SIR	BUSY	STOP	STRT	00000010B
	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	

Address :	7	6	5	4	3	2	1	0	Initial Value
000061H 000065H	—	—	—	—	MODE	BDS	SOE	SCOE	----0000B
	—	—	—	—	R/W	R/W	R/W	R/W	

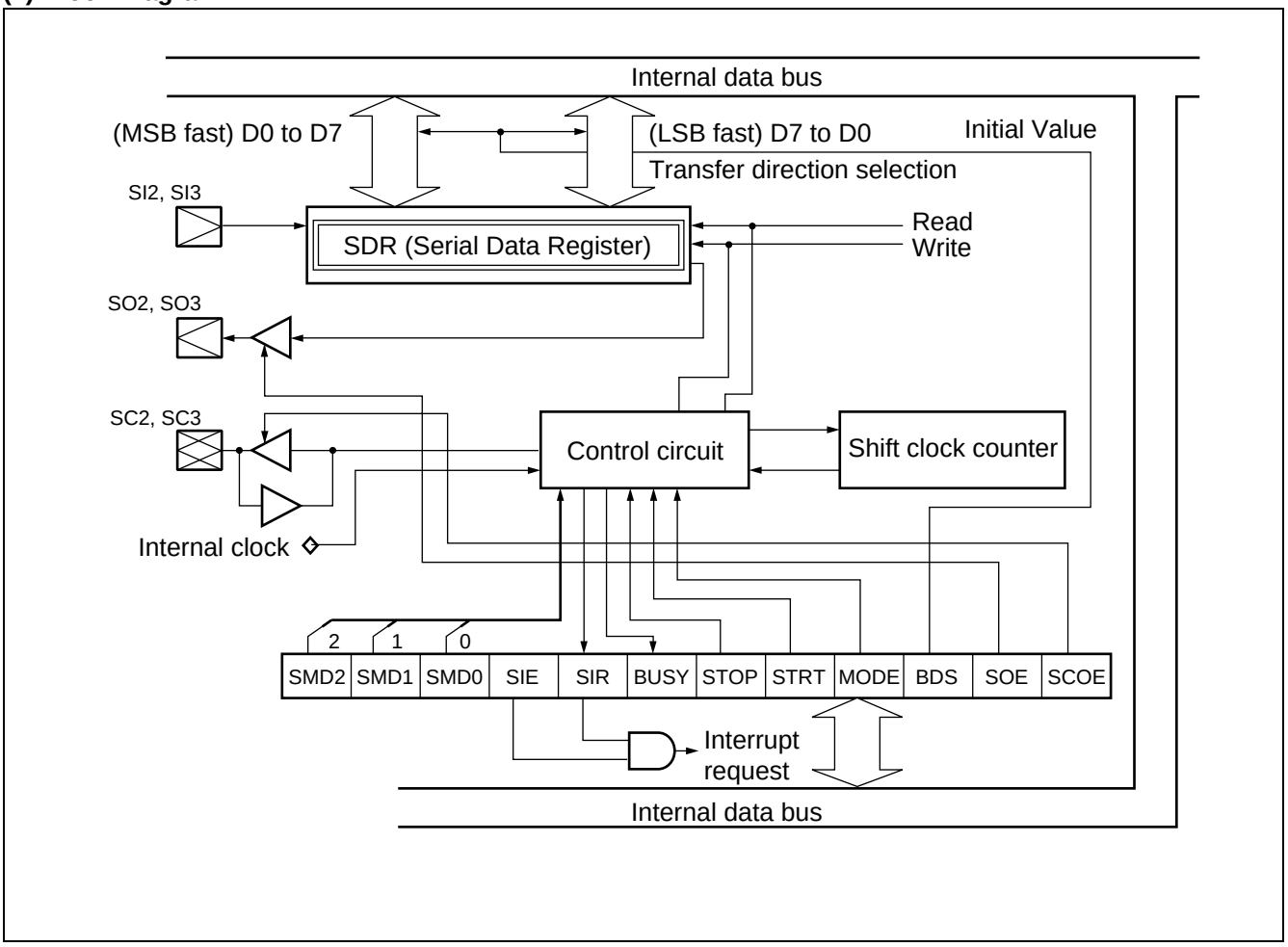
Serial Data Register (SDR)

Address :	7	6	5	4	3	2	1	0	Initial Value
000062H 000066H	D7	D6	D5	D4	D3	D2	D1	D0	XXXXXXXX
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Communication Prescaler control register (SDCR0, SDCR1)

Address :	15	14	13	12	11	10	9	8	Initial Value
000063H 000067H	MD	—	—	—	Reserved	DIV2	DIV1	DIV0	0---0000
	R/W	—	—	—	R/W	R/W	R/W	R/W	

(2) Block Diagram



5. 8/10-bit A/D converter

A/D converter converts an analog input voltage into digital value. The feature of A/D converter is shown as follows.

- conversion time : 3.1 μs minimum per 1 channel

(78 machine cycle/at machine clock 25 MHz/including the sampling time)

- Sampling time : 2.0 μs minimum per 1channel

(50 machine cycle/at machine clock 25 MHz)

- Uses RC-type successive approximation conversion method with a sample & hold circuit
- 8-bit resolution or 10-bit resolution can be select.
- 12 channel program-selectable analog inputs.
  Single conversion mode : Convert 1 specified channel
  Scan conversion mode : Continuous plural channels (maximum 12 channels can be programmed) are converted.
  Continuous conversion mode : Selected channel converted continuously.
  Stop conversion time : Perform conversion for one channel, then wait for the next activation trigger (synchronizes the conversion start timing)
- EI^{2}OS can be activated by outputting the interrupt request when the A/D conversion completes.
- If the A/D conversion is performed under the condition of the interrupt enable, the converting data will be protected.
- Selectable conversion activation trigger : Software, or reload timer (rising edge)

(1) Register list

ADCS1, ADCS0 (Control status register)

ADCS0

Address : 000034$_H$

bit	7	6	5	4	3	2	1	0	
	MD1	MD0	—	—	—	—	—	—	
	0	0	—	—	—	—	—	—	←Initial Value
	R/W	R/W	—	—	—	—	—	—	←bit

ADCS1 bit

Address : 000035$_H$

bit	15	14	13	12	11	10	9	8	
	BUSY	INT	INTE	PAUS	STS1	STS0	STRT	Reserved	
	0	0	0	0	0	0	0	0	←Initial Value
	R/W	R/W	R/W	R/W	R/W	R/W	W	R/W	←bit

ADCR1, ADCR0 (data register)

ADCR0 bit

Address : 000036$_H$

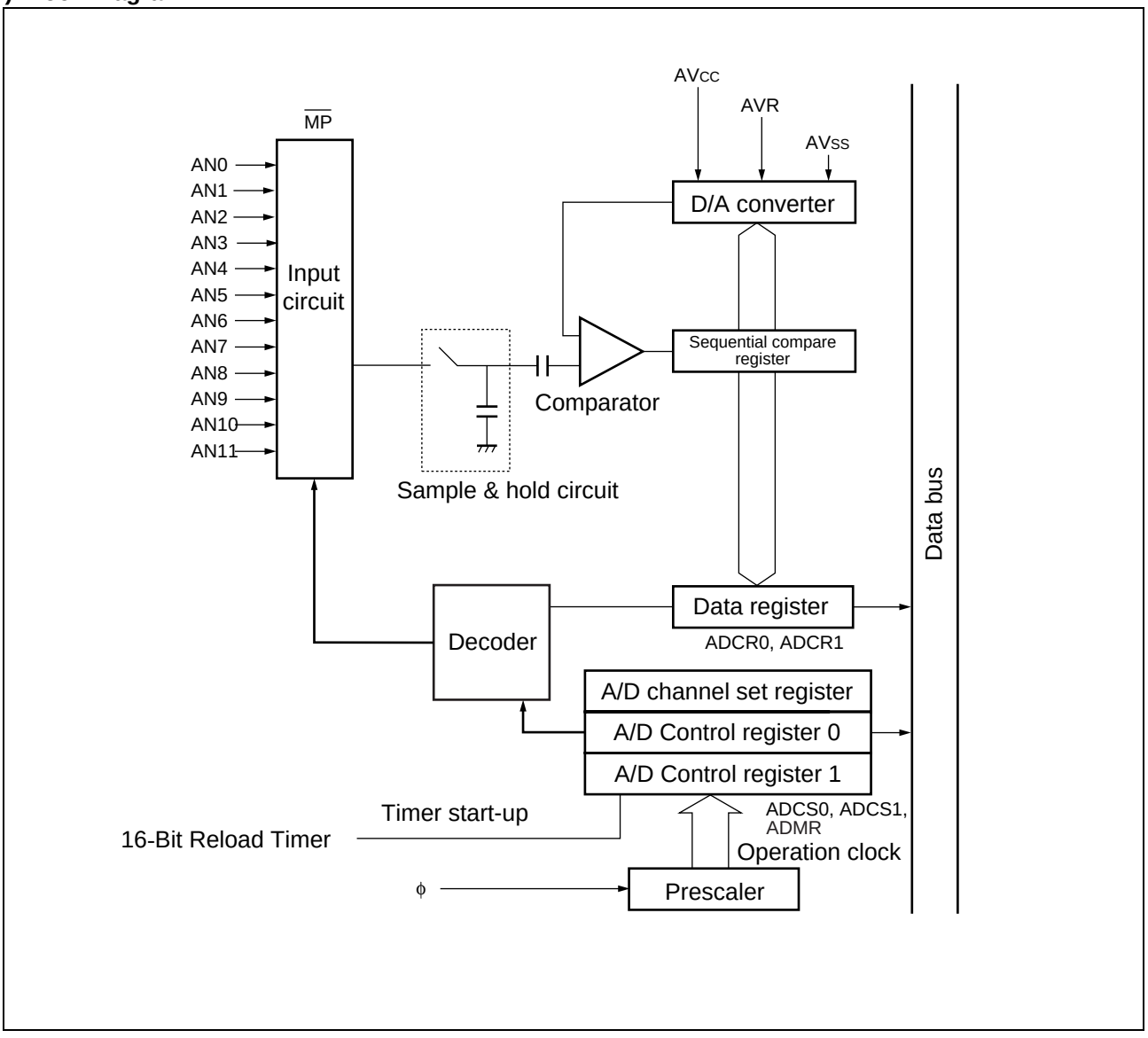
bit	7	6	5	4	3	2	1	0	
	D7	D6	D5	D4	D3	D2	D1	D0	
	X	X	X	X	X	X	X	X	←Initial Value
	R	R	R	R	R	R	R	R	←bit

ADCR1 bit

Address : 000037$_H$

bit	15	14	13	12	11	10	9	8	
	S10	ST1	ST0	CT1	CT0	—	D9	D8	
	0	0	1	0	1	—	X	X	←Initial Value
	W	W	W	W	W	—	R	R	←bit

(2) Block Diagram



6. 16 bits PPG

The PPG timer consists of the prescaler, one 16-bit down-counter, one 16-bit data register with a cycle setting buffer, a 16-bit compare register with a duty setting buffer, and the pin control unit.

The PPG timer can output pulses synchronized to the software trigger.

The period and duty of the output pulse can be changed freely by updating two 16-bit register values.

- PWM function

The PPG timer can output pulses programmably by updating the values of the registers described above in synchronization to the trigger.

Can also be used as a D/A converter by an external circuit.

- Single shot function

By detecting an edge of the trigger input, a single pulse can be output.

- 16-bit down counter

The counter operation clock comes from eight kinds optional. There are eight kinds of internal clocks.

(ϕ, ϕ2, ϕ4, ϕ8, ϕ16, ϕ32, ϕ64, ϕ128) ϕ : machine clock

The counter is initialized to " $FFFF_H$ " at a reset or counter borrow.

- Interrupt request

The PPG timer generates an interrupt request when :

Timer start-up/counter borrow occurs (cycle match) /duty match occurs/counter borrow occurs (cycle match) , or duty match occurs.

(1) Register list

PCNTH (PCNTH0/1 Control Status register)

	15	14	13	12	11	10	9	8	
000077H 00007FH	CNTE	STGR	MDSE	RTRG	CSK2	CSK1	CSK0	PGMS	
	(R/W) (0)	(R/W) (0)	(R/W) (0)	(R/W) (0)	(R/W) (0)	(R/W) (0)	(R/W) (0)	(R/W) (X)	Read/Write Initial Value

PCNTL (PCNTL0/1 Control Status register)

	7	6	5	4	3	2	1	0	
000076H 00007EH	—	—	IREN	IRQF	IRS1	IRS0	POEN	OSEL	
	(—) (—)	(—) (—)	(R/W) (0)	(R/W) (0)	(R/W) (0)	(R/W) (0)	(R/W) (0)	(R/W) (0)	Read/Write Initial Value

PDCRH (PDCRH0/1 PPG Down Counter Register)

	15	14	13	12	11	10	9	8	
000071H 000079H	DC15	DC14	DC13	DC12	DC11	DC10	DC09	DC08	
	(R) (1)	(R) (1)	(R) (1)	(R) (1)	(R) (1)	(R) (1)	(R) (1)	(R) (1)	Read/Write Initial Value

PDCRL (PDCRL0/1 PPG Down Counter Register)

	7	6	5	4	3	2	1	0	
000070H 000078H	DC07	DC06	DC05	DC04	DC03	DC02	DC01	DC00	
	(R) (1)	(R) (1)	(R) (1)	(R) (1)	(R) (1)	(R) (1)	(R) (1)	(R) (1)	Read/Write Initial Value

PCSRH (PCSRH0/1 PPG cycle set register)

	15	14	13	12	11	10	9	8	
000073H 00007BH	CS15	CS14	CS13	CS12	CS11	CS10	CS09	CS08	Read/Write Initial Value
	(W) (X)	(W) (X)	(W) (X)	(W) (X)	(W) (X)	(W) (X)	(W) (X)	(W) (X)	

PCSRL (PCSRH0/1 PPG cycle set register)

	7	6	5	4	3	2	1	0	
000072H 00007AH	CS07	CS06	CS05	CS04	CS03	CS02	CS01	CS00	
	(W) (X)	(W) (X)	(W) (X)	(W) (X)	(W) (X)	(W) (X)	(W) (X)	(W) (X)	Read/Write Initial Value

PDUTH (PDUTH0/1 PPG duty set register)

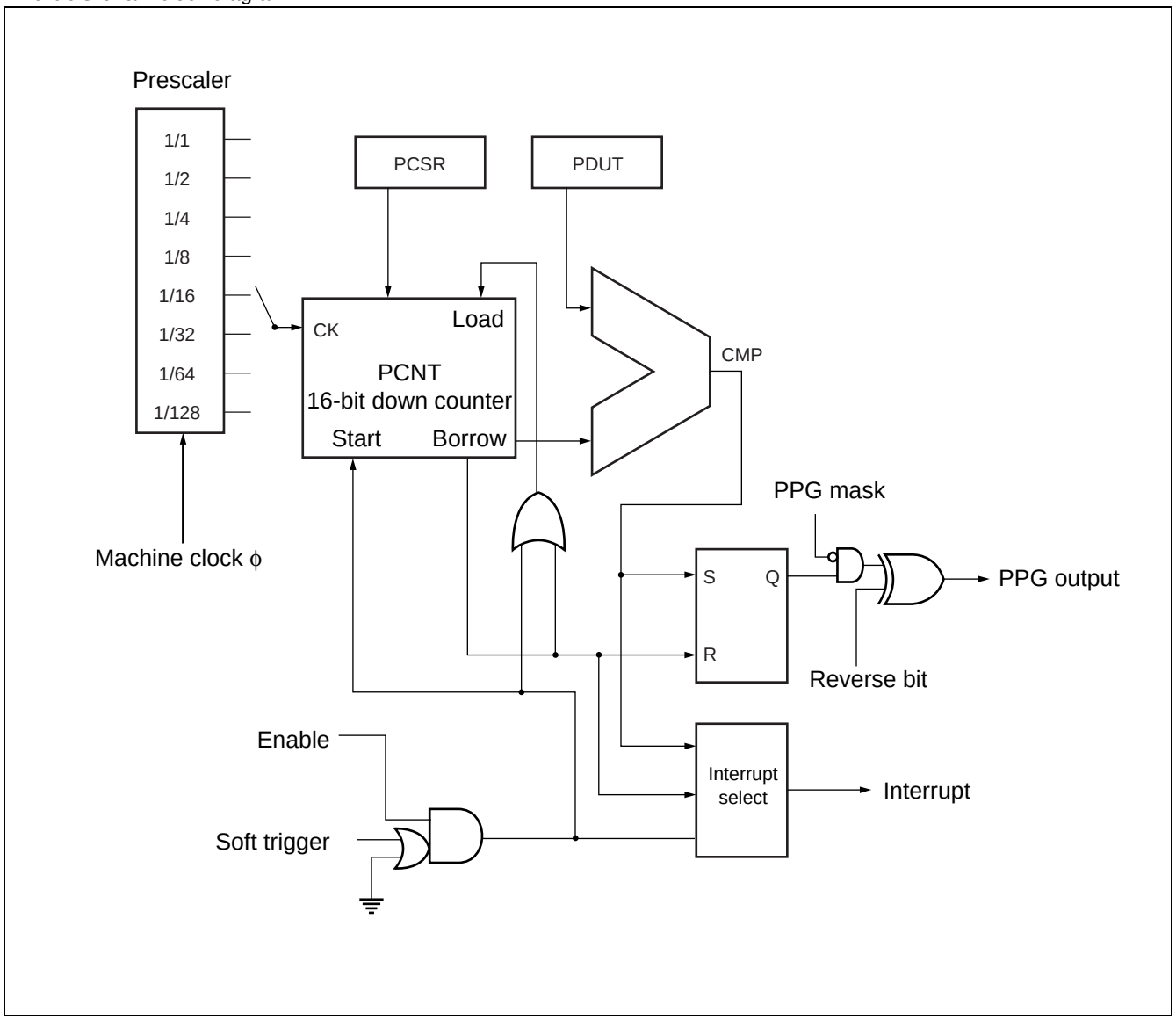
	15	14	13	12	11	10	9	8	
000075H 00007DH	DU15	DU14	DU13	DU12	DU11	DU10	DU09	DU08	
	(W) (X)	(W) (X)	(W) (X)	(W) (X)	(W) (X)	(W) (X)	(W) (X)	(W) (X)	Read/Write Initial Value

PDUTL (PDUTL0/1 PPG duty set register)

	7	6	5	4	3	2	1	0	
000074H 00007CH	DU07	DU06	DU05	DU04	DU03	DU02	DU01	DU00	
	(W) (X)	(W) (X)	(W) (X)	(W) (X)	(W) (X)	(W) (X)	(W) (X)	(W) (X)	Read/Write Initial Value

(2) Block Diagram

• 16-bit G ch0/1 block diagram



7. Delay interrupt generator module

The delayed interrupt generation module outputs an interrupt request for task swiching. When the delayed interrupt generation module is used, software is allowed to output and clear task switching interrupts for the MB90800 Series CPU.

(1) Register list

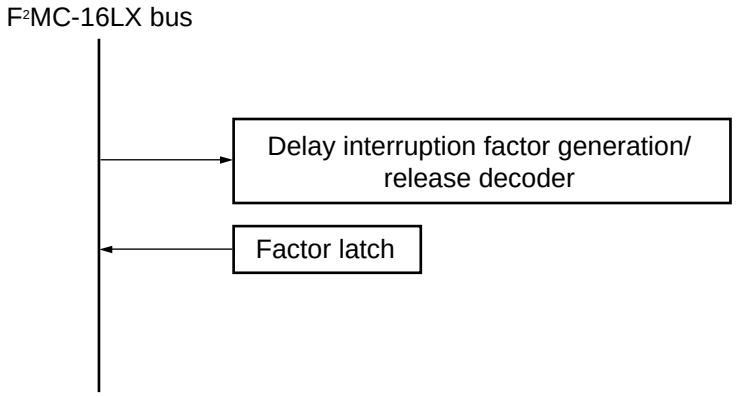
Delayed Interrupt/release register(DIRR)

DIRR

Address : 00009F$_H$

15	14	13	12	11	10	9	8	Initial Value
—	—	—	—	—	—	—	R0	- - - - - - - 0$_B$
—	—	—	—	—	—	—	R/W	

(2) Block diagram



8. DTP/External interrupt

DTP (Data Transfer Peripheral)/External interrupt circuit detects the interrupt request input from the external interrupt input terminal, and outputs the interrupt request.

(1) Register list

Interrupt/DTP enable register (ENIR : Enable Interrupt Request Register)

ENIR
Address : 000030H

7	6	5	4	3	2	1	0
—	—	—	—	EN3	EN2	EN1	EN0
—	—	—	—	R/W	R/W	R/W	R/W

Initial Value
- - - - 0000B

Interrupt/DTP source register (EIRR : External Interrupt Request Register)

EIRR
Address : 000031H

15	14	13	12	11	10	9	8
—	—	—	—	ER3	ER2	ER1	ER0
—	—	—	—	R/W	R/W	R/W	R/W

Initial Value
- - - - XXXXB

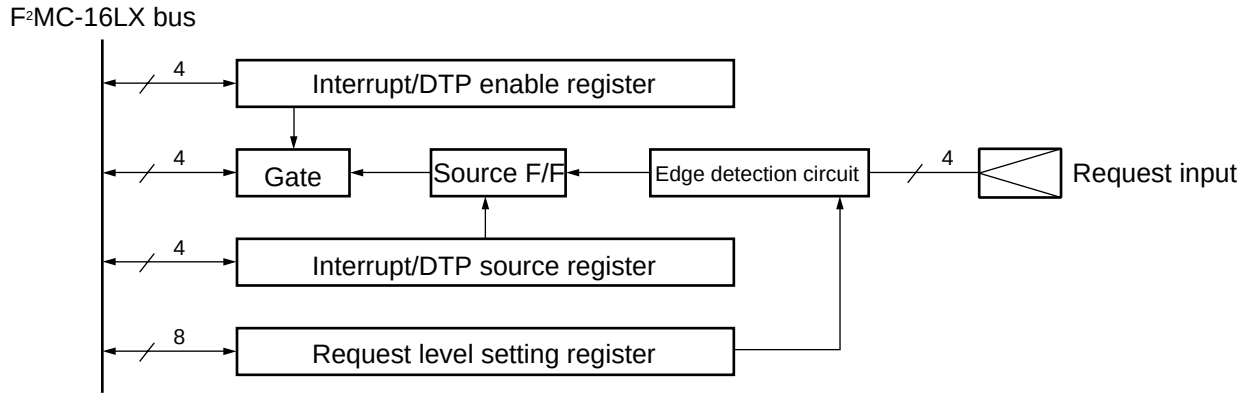
Request level setting register (ELVR : External Level Register)

Address : 000032H

7	6	5	4	3	2	1	0
LB3	LA3	LB2	LA2	LB1	LA1	LB0	LA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial Value
00000000B

(2) Block diagram

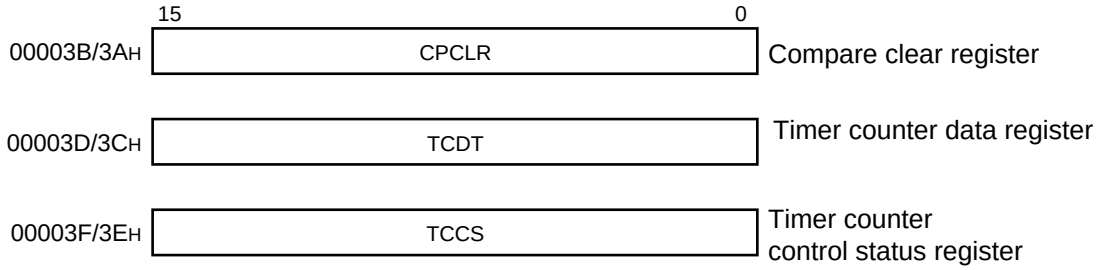


9. 16-bit input/output timer

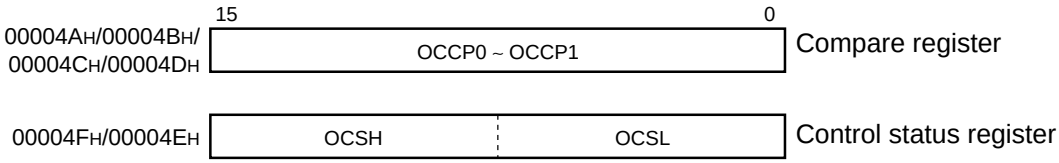
The 16-bit I/O timer consists of one 16-bit free-run timer, two output compare and two input capture modules. This function enables six independent waveforms to be output based on the 16-bit free-run timer, and input pulse widths and external clock frequencies to be measured.

• Register list

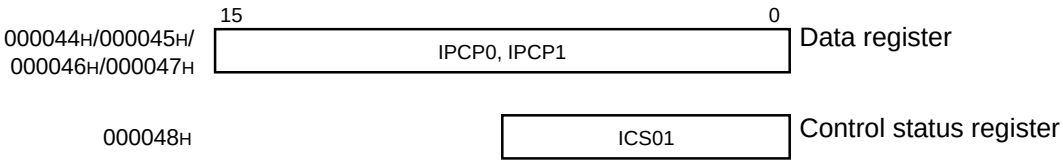
• 16-bit free-run timer



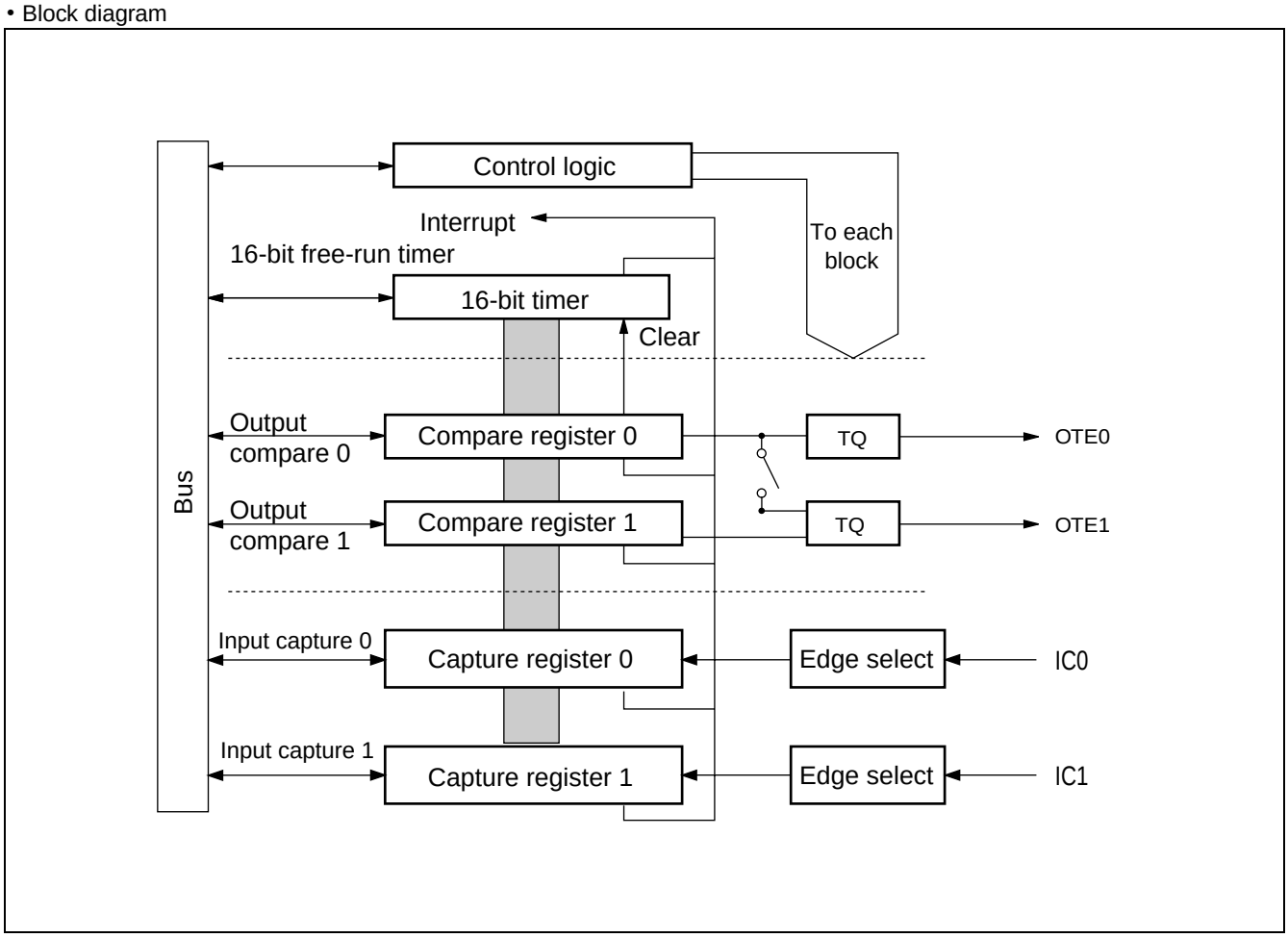
• 16-bit Output Compare



• 16-bit Input Capture



• Block diagram



(1) 16-bit free-run timer

The 16-bit free-run timer consists of a 16-bit up-down counter and control status register.

Counter value of 16-bit free-run timer is available as base timer for input capture and output compare.

- Clock for the counter operation can be selected from eight types.
- The counter overflow interruption can be generated.
- Setting the mode enables initialization of the counter through compare-match operation with the value of the compare clear register in the output compare.

• Register list

Compare clear register (CPCLR)

00003B$_H$

15	14	13	12	11	10	9	8
CL15	CL14	CL13	CL12	CL11	CL10	CL09	CL08
(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)

Initial Value XXXXXXXX$_B$

00003A$_H$

7	6	5	4	3	2	1	0
CL07	CL06	CL05	CL04	CL03	CL02	CL01	CL00
(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)

Initial Value XXXXXXXX$_B$

Timer counter data register (TCDT)

00003D$_H$

15	14	13	12	11	10	9	8
T15	T14	T13	T12	T11	T10	T09	T08
(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)

Initial Value 00000000$_B$

00003C$_H$

7	6	5	4	3	2	1	0
T07	T06	T05	T04	T03	T02	T01	T00
(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)

Initial Value 00000000$_B$

Timer counter control/status register (TCCS)

00003F$_H$

15	14	13	12	11	10	9	8
ECKE	—	—	MSI2	MSI1	MSI0	ICLR	ICRE
(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)

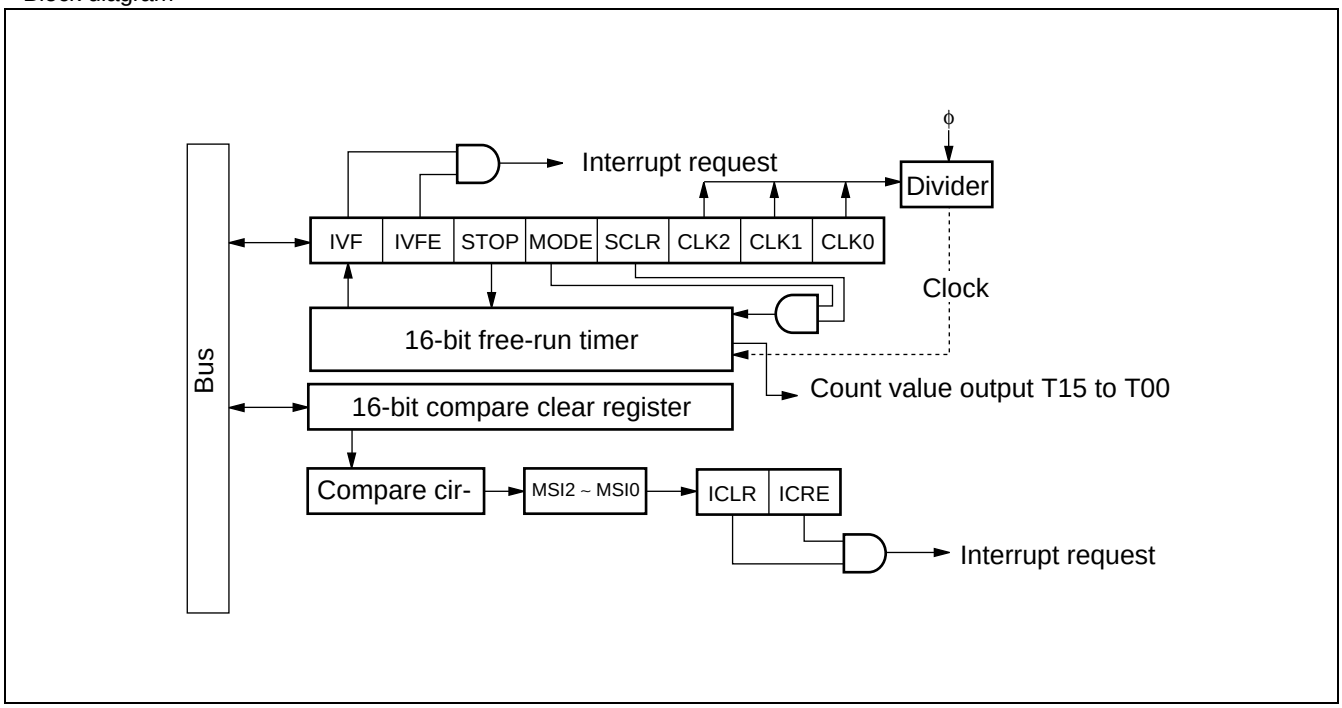
Initial Value 0--00000$_B$

00003E$_H$

7	6	5	4	3	2	1	0
IVF	IVFE	STOP	MODE	SCLR	CLK2	CLK1	CLK0
(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)

Initial Value 00000000$_B$

• Block diagram



(2) Output compare

The output compare consists of 16-bit compare registers, compare output pin part and a control register. It can reverse the output level for the pin and at the same time, generate an interrupt when the 16-bit free-run timer value matches a value set in one of the 16-bit compare registers of this module.

- It has a total of six compare registers that can operate independently. In addition, the output can be set to be controlled by using two compare registers.
- An interrupt can be set by a comparing match.

• Register list

Compare register (OCCP0, OCCP1)

	15	14	13	12	11	10	9	8	Initial Value
00004B$_H$ 00004D$_H$	OP15	OP14	OP13	OP12	OP11	OP10	OP09	OP08	00000000$_B$
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

	7	6	5	4	3	2	1	0	Initial Value
00004A$_H$ 00004C$_H$	OP07	OP06	OP05	OP04	OP03	OP02	OP01	C00	00000000$_B$
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

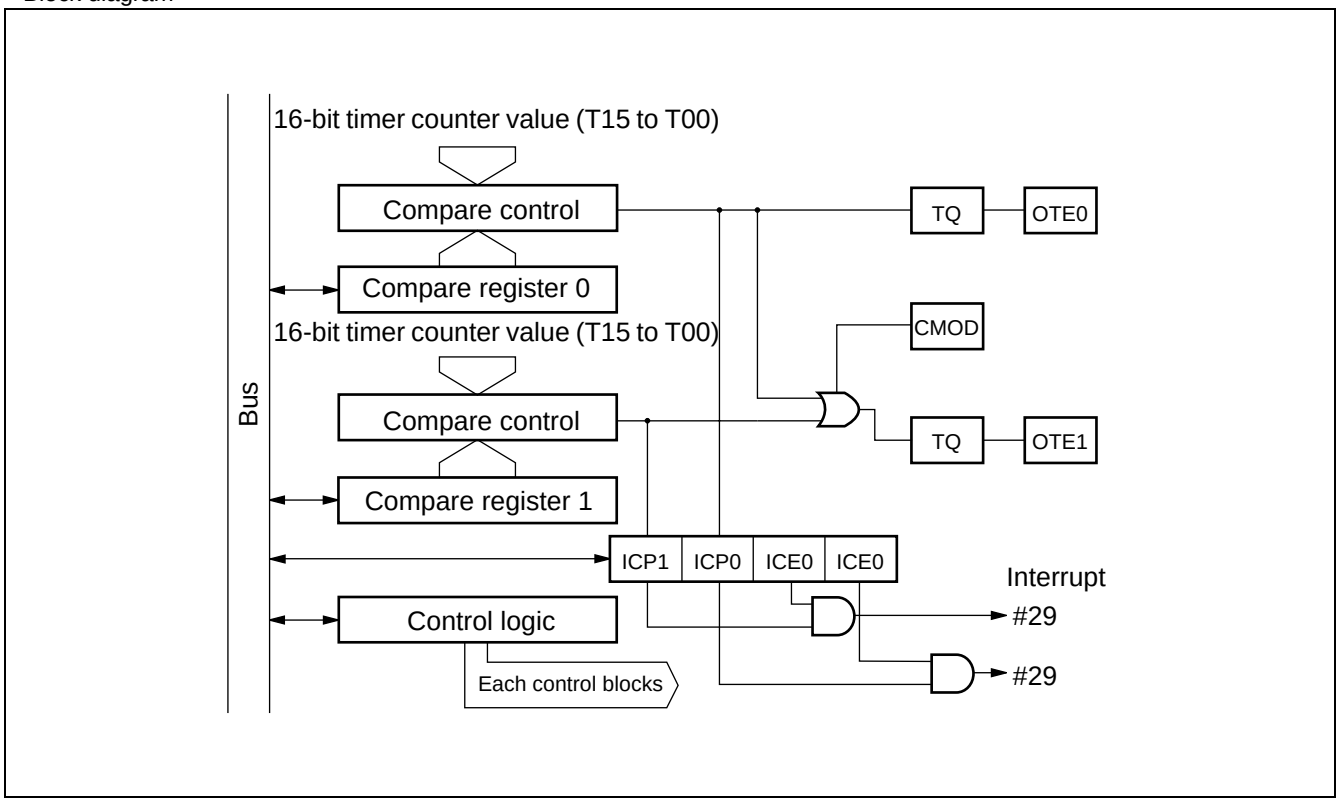
Control register (OCSH)

	15	14	13	12	11	10	9	8	Initial Value
00004F$_H$	—	—	—	CMOD	OTE1	OTE0	OTD1	OTD0	---00000$_B$
	(—)	(—)	(—)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

Control register (OCSL)

	7	6	5	4	3	2	1	0	Initial Value
00004E$_H$	IOP1	IOP0	IOE1	IOE0	—	—	CST1	CST0	0000--00$_B$
	(R/W)	(R/W)	(R/W)	(R/W)	(—)	(—)	(R/W)	(R/W)	

• Block diagram



(3) Input capture

This module has a function that detects a rising edge, falling edge or both edges and holds a value of the 16-bit free-run timer in a register at the time of detection. It can also generate an interrupt when detecting an edge.

The input capture consists of input capture and control registers. Each input capture has its corresponding external input pin.

- The detection edge of an external input can be selected from among three types. Rising edge/falling edge/ both edges.
- It can generate an interrupt when it detects the valid edge of the external input.

• Register list

Input capture data register (IPCP0, IPCP1)

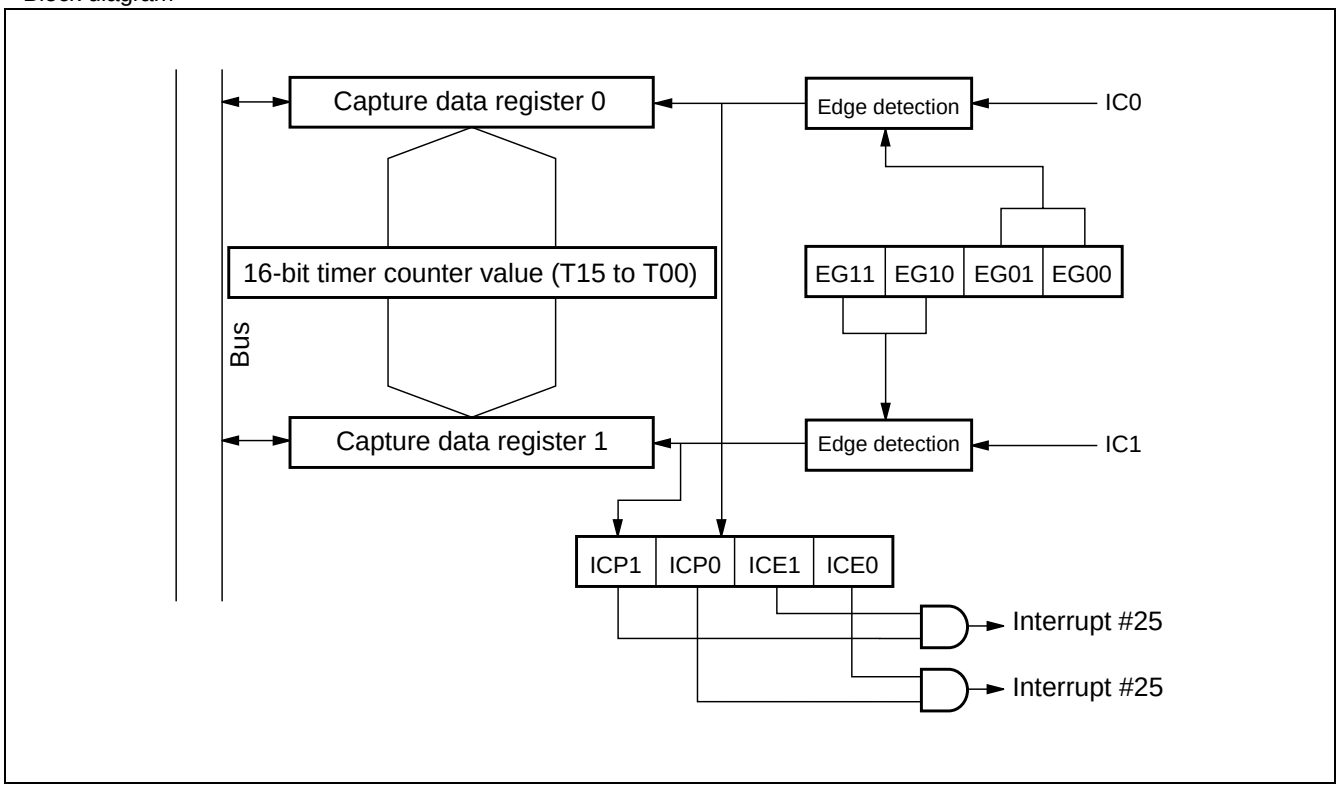
	15	14	13	12	11	10	9	8	Initial Value
000045H 000047H	CP15	CP14	CP13	CP12	CP11	CP10	CP09	CP08	XXXXXXXXB
	(R)	(R)	(R)	(R)	(R)	(R)	(R)	(R)	

	7	6	5	4	3	2	1	0	Initial Value
000044H 000046H	CP07	CP06	CP05	CP04	CP03	CP02	CP01	CP00	XXXXXXXXB
	(R)	(R)	(R)	(R)	(R)	(R)	(R)	(R)	

Control status register (ICS01)

	7	6	5	4	3	2	1	0	Initial Value
000048H	ICP1	ICP0	ICE1	ICE0	EG11	EG10	EG01	EG00	00000000B
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

• Block diagram



10. 16-bit reload timer

The 16-bit reload timer provides two functions either one which can be selected, the internal clock the performs the count down by synchronizing with 3-type internal clocks and the event count mode that performs the count down by detecting the arbitration. This timer defines an underflow as a transition of the count value from 0000_H to $FFFF_H$. Therefore, when the equation (counted value = reload register setting value+1) holds, an underflow occurs. Either mode can be selected for the count operation from the reload mode which repeats the count by reloading the count setting value at the underflow occurrence or the one-shot mode which stops the count at the underflow occurrence. The interrupt can be generated at the counter underflow occurrence so as to correspond to the DTC.

(1) Register list

• TMCSRTimer control status register

Timer control status register (upper) (TMCSR)

	15	14	13	12	11	10	9	8	
000051_H	—	—	—	—	CSL1	CSL0	MOD2	MOD1	
000055_H	(—)	(—)	(—)	(—)	(R/W)	(R/W)	(R/W)	(R/W)	Read/Write
000059_H	(—)	(—)	(—)	(—)	(0)	(0)	(0)	(0)	Initial Value

Timer control status register (lower) (TMCSR)

	7	6	5	4	3	2	1	0	
000050_H	MOD0	OUTE	OUTL	RELD	INTE	UF	CNTE	TRG	
000054_H	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	Read/Write
000058_H	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	Initial Value

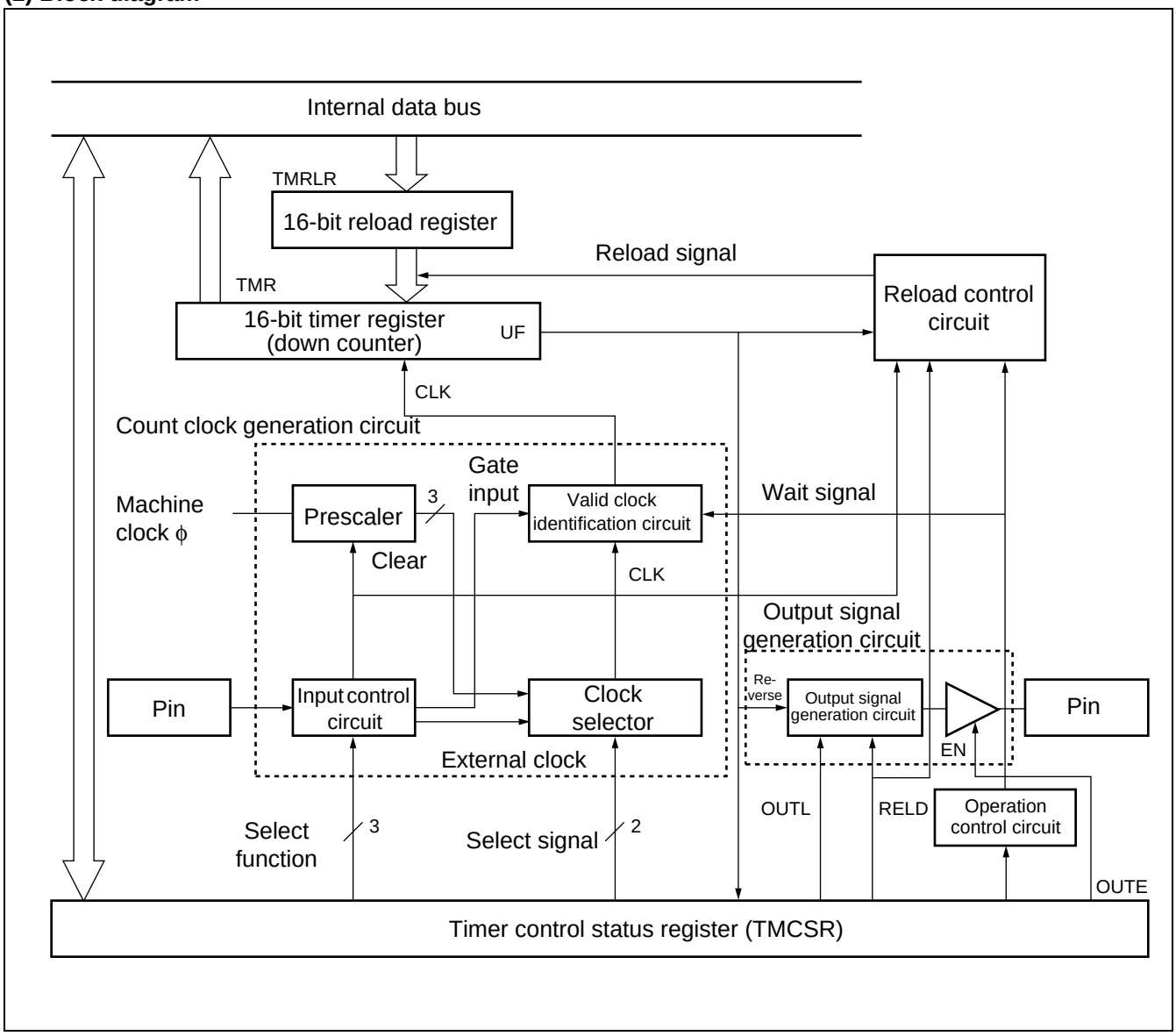
• 16-bit timer register/16-bit reload register TMR/TMRLR (upper)

	15	14	13	12	11	10	9	8	
000053_H	D15	D14	D13	D12	D11	D10	D9	D8	
000057_H	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	Read/Write
$00005B_H$	(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)	Initial Value

TMR/TMRLR (low)

	7	6	5	4	3	2	1	0	
000052_H	D7	D6	D5	D4	D3	D2	D1	D0	
000056_H	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	Read/Write
$00005A_H$	(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)	Initial Value

(2) Block diagram



11. Watch timer

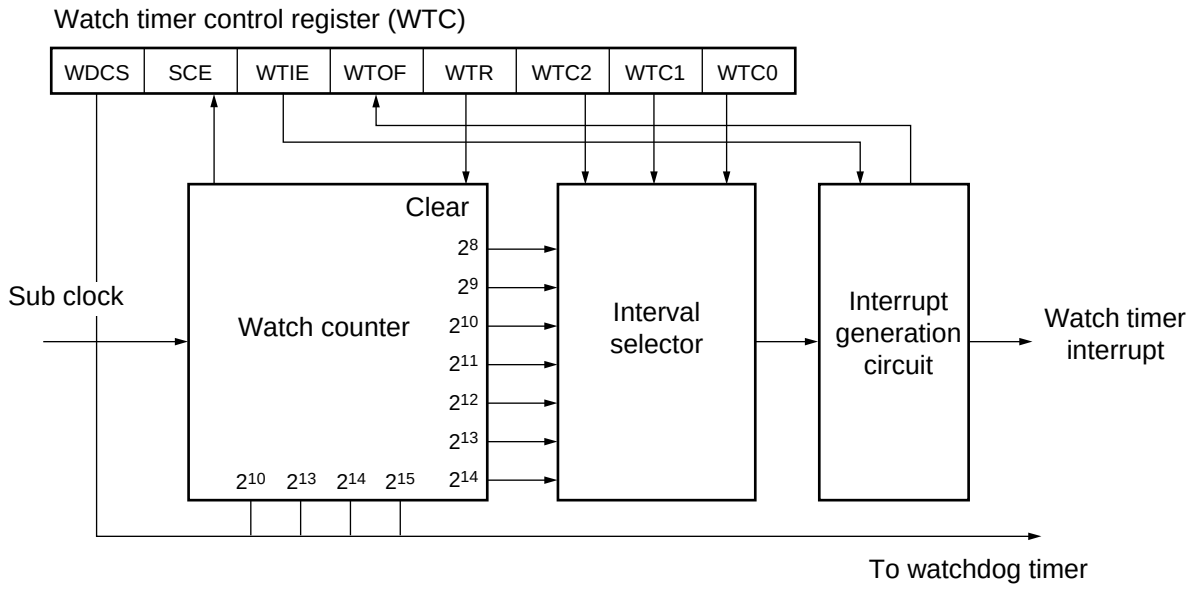
The watch timer is a 15-bit timer using the subclock. It can generate interval interrupts. The watch timer can also be used as the clock source of the watchdog timer by setting so.

(1) Register list

Watch timer control register (WTC)

	7	6	5	4	3	2	1	0	
0000AA$_H$	WDCS	SCE	WTIE	WTOF	WTR	WTC2	WTC1	WTC0	
	(R/W)	(R)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
	(1)	(X)	(0)	(1)	(1)	(0)	(0)	(0)	Initial Value

(2) Block diagram



12. Watchdog timer

The watchdog timer is a 2-bit counter operating with an output of the timebase timer or watch timer and resets the CPU when the counter is not cleared for a preset period of time.

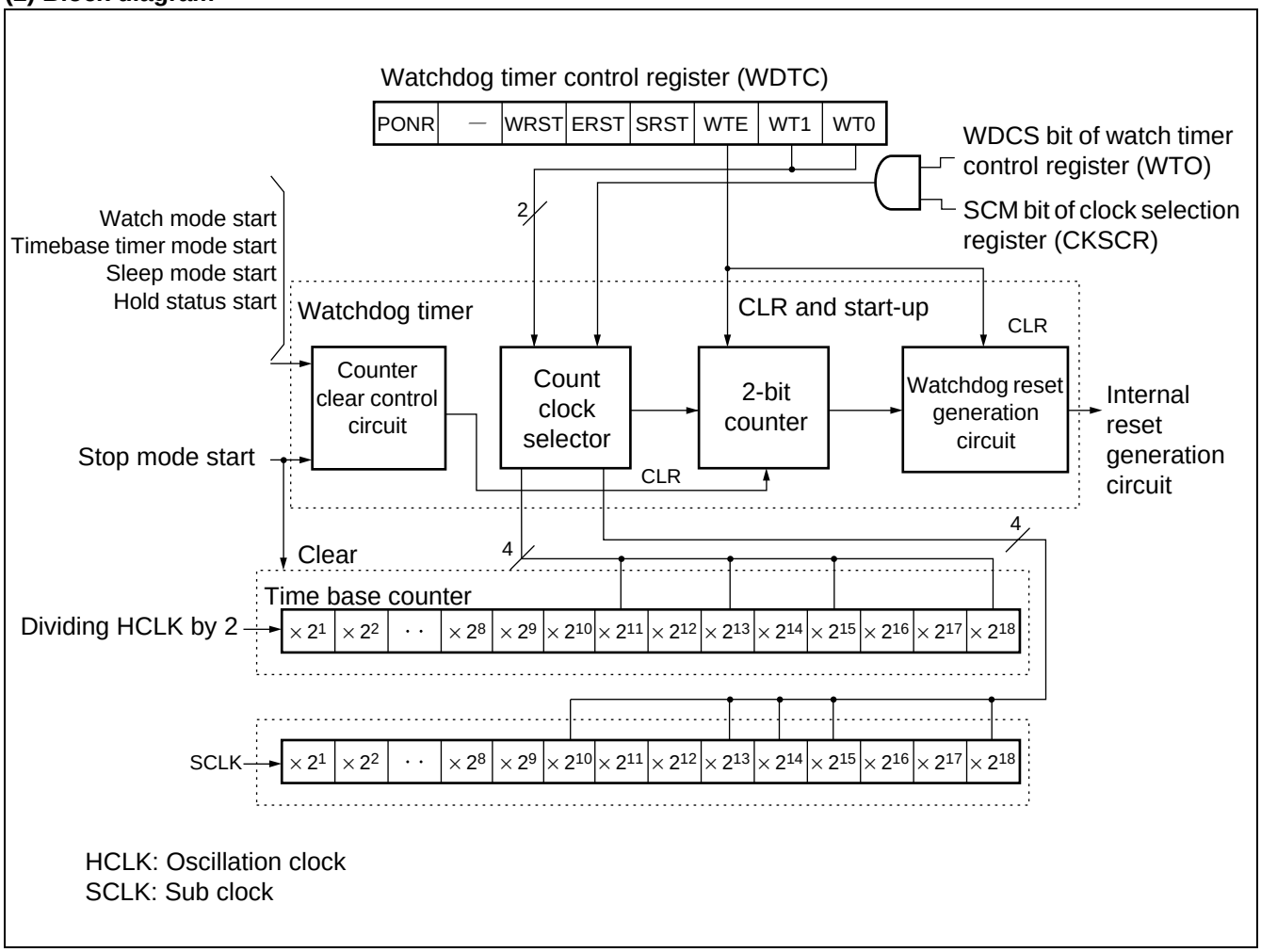
(1) Register list

Watchdog timer control register (WDTC)

	7	6	5	4	3	2	1	0
0000A8H	PONR	—	WRST	ERST	SRST	WTE	WT1	WT0
	(R) (X)	(—) (X)	(R) (X)	(R) (X)	(R) (X)	(W) (1)	(W) (1)	(W) (1)

Initial Value

(2) Block diagram



HCLK: Oscillation clock
SCLK: Sub clock

13. Time-base timer

The time-base timer has a function that enables a selection of four interval times using 18-bit free-run counter (time-base counter) with synchronizing to the internal count clock (two division of original oscillation). Furthermore, the function of timer output of oscillation stabilization wait or function supplying operation clocks for watchdog timer are provided.

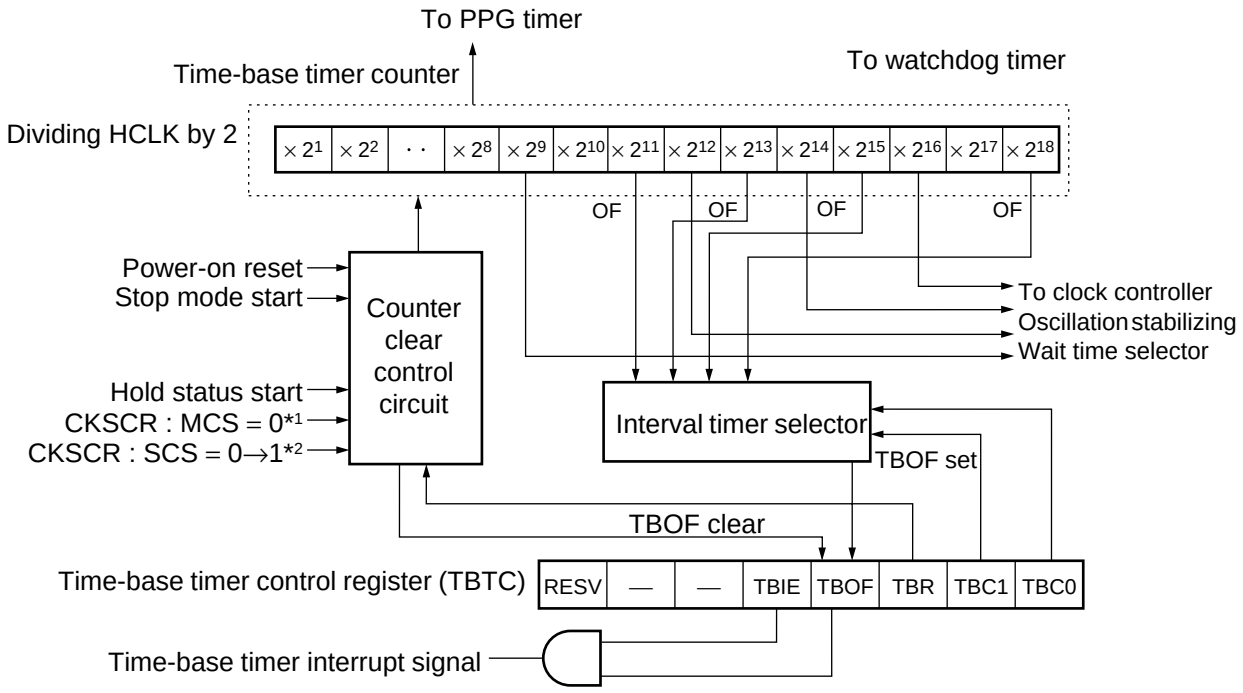
(1) Register list

Timer base timer control register (TBTC)

0000A9H

15	14	13	12	11	10	9	8
Reserved	—	—	TBIE	TBOF	TBR	TBC1	TBC0
(R/W)	(—)	(—)	(R/W)	(R/W)	(W)	(R/W)	(R/W)
(1)	(—)	(—)	(0)	(0)	(1)	(0)	(0)

(2) Block diagram



— : Unused
OF : Overflow
HCLK : Oscillation clock
*1 : The machine clock is switched from main/sub clock to PLL clock.
*2 : The machine clock is switched from sub clock to main clock.

14. Clock

The clock generator controls operation of the internal clock which is the operation clock for the CPU and peripheral devices. This internal clock is referred to as machine clock and its one cycle as machine cycle. In addition, the clock generated by original oscillation is referred to as oscillation clock and that by internal PLL oscillation as PLL clock.

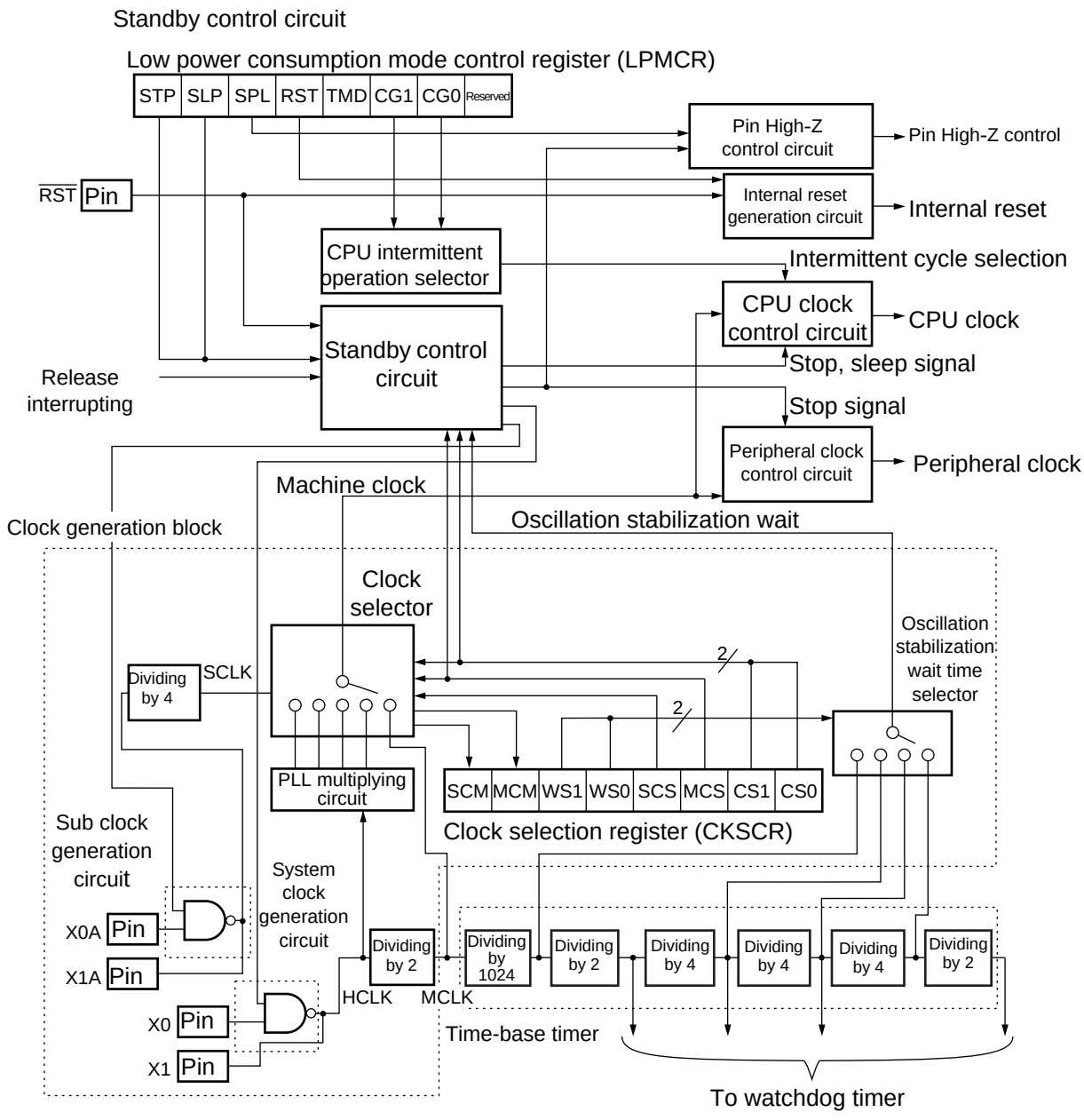
(1) Register list

Clock selection register (CKSCR)

0000A1H

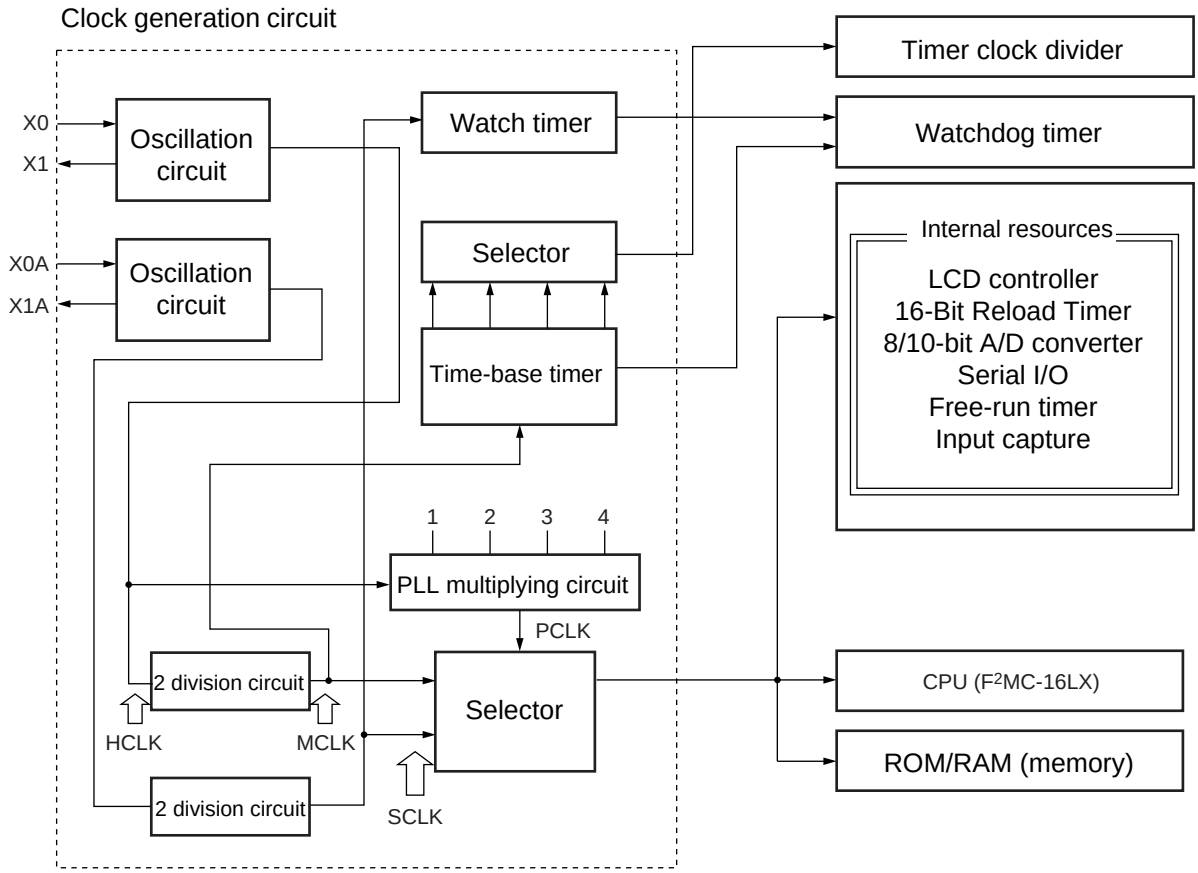
15	14	13	12	11	10	9	8	
SCM	MCM	WS1	WS0	SCS	MCS	CS1	CS0	
(R)	(R)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
(1)	(1)	(1)	(1)	(1)	(1)	(0)	(0)	Initial Value

(2) Block diagram



HCLK : Oscillation clock
MCLK : Main clock
SCLK : Sub clock

(3) Clock supply map



HCLK : Oscillation clock frequency
MCLK : Main clock frequency
PCLK : PLL clock frequency
SCLK : Sub clock frequency

15. Low power consumption mode

The MB90800 Series have the following CPU operation modes by selecting the operation clock and operating the control of the clock.

- Clock mode
  (PLL clock mode, main clock mode and sub clock mode)
- CPU intermittent operation mode
  (PLL clock intermittent operation mode, main clock intermittent operation mode and subclock intermittent operation mode)
- Standby mode
  (Sleep mode, time base timer mode, stop mode and watch mode)

(1) Register list

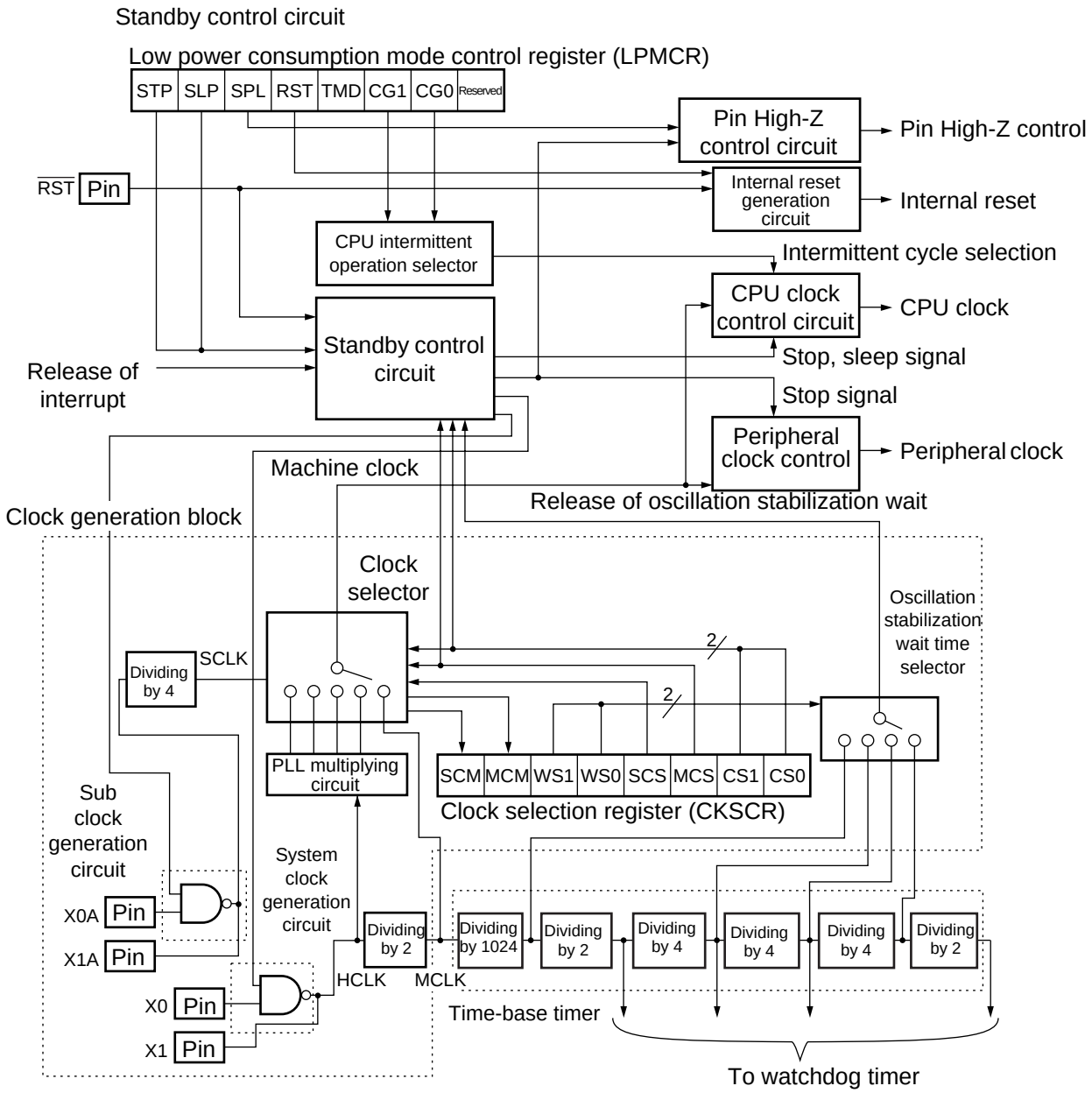
Low power consumption mode control register (LPMCR)

0000A0$_H$

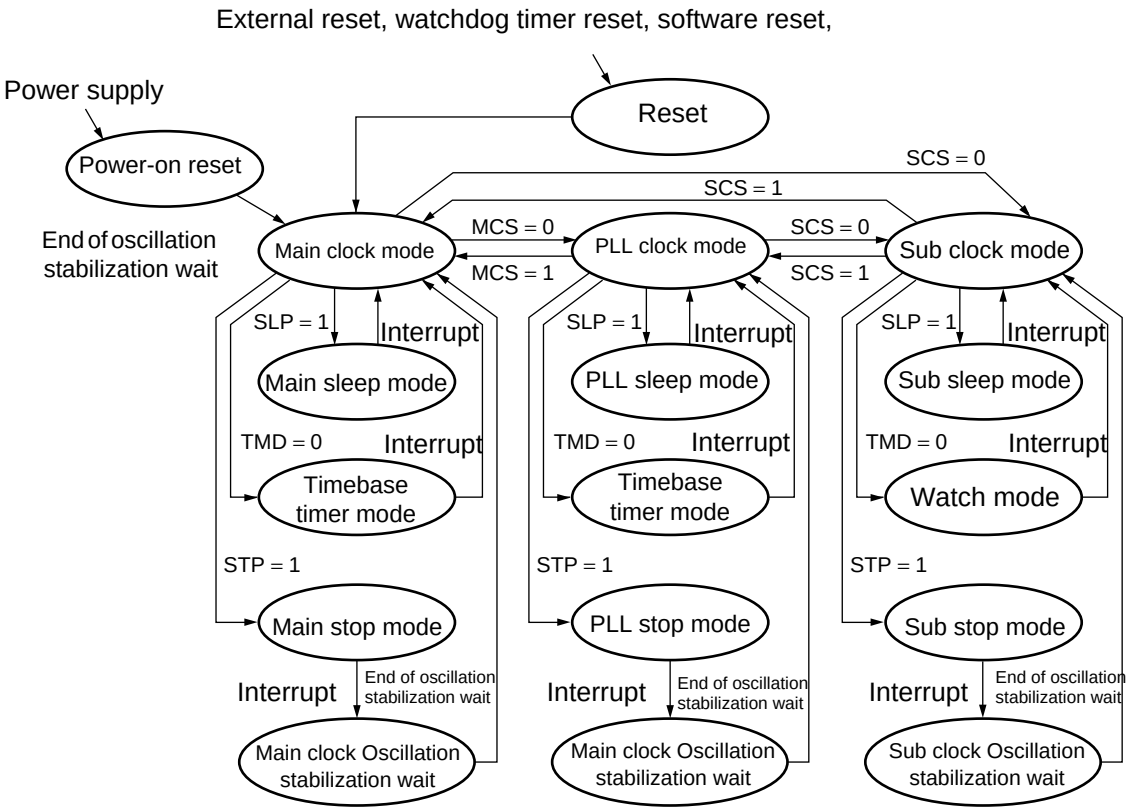
7	6	5	4	3	2	1	0
STP	SLP	SPL	RST	TMD	CG1	CG0	Reserved
(W)	(W)	(R/W)	(W)	(R/W)	(R/W)	(R/W)	(R/W)
(0)	(0)	(0)	(1)	(1)	(0)	(0)	(0)

Initial Value

(2) Block diagram



(3) Figure of status transition



16. Timer clock output

The timer clock output circuit divides the oscillation clock by the time-base timer and generates and outputs the set division clock. Selectable from 32/64/128/256 division of the oscillation clock.

The timer clock output circuit is inactive in reset or stop mode. Normally, it is active in run, sleep, or pseudo-timer mode.

	PLL_Run	Main_Run	Sleep	Pseudo clock	STOP	Reset
Operation status	○	○	○	○	×	×

Note : When the time-base timer is cleared while using the timer clock output circuit, the clock is not correctly output. For detail of the timebase timer's clear condition, see the section of timebase timer in Hardware Manual.

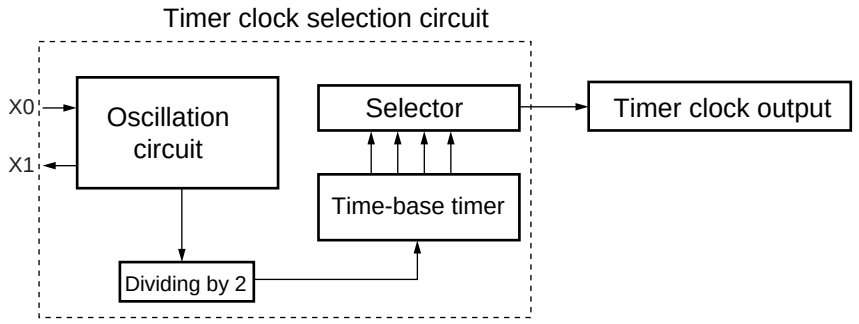
(1) Register list

Address : 0000AF$_H$

bit	15	14	13	12	11	10	9	8	Initial Value
	—	—	—	—	—	TEN	TS1	TS0	XXXXX000$_B$
						R/W	R/W	R/W	

\- : Unused

(2) Block diagram



17. ROM mirrorring function selection module

ROM mirrorring function selection module can select that FF bank where ROM is located look into 00 bank among the settings of the register.

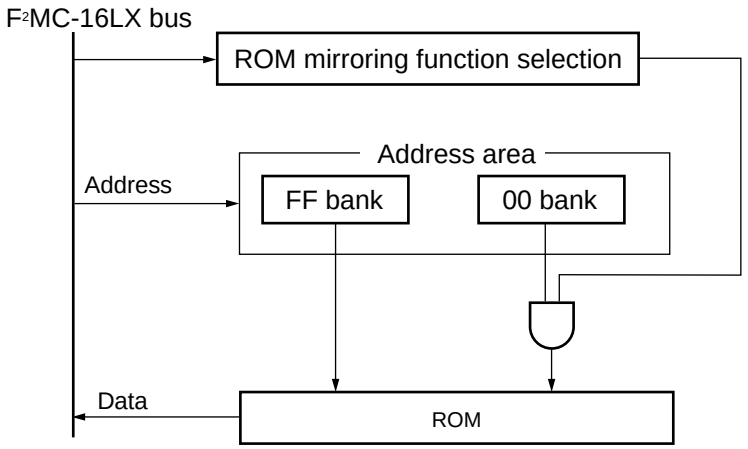
(1) Register list

Address : 00006F$_H$

bit	15	14	13	12	11	10	9	8	Initial Value
	—	—	—	—	—	—	—	MI	XXXXXXX1$_B$
								R/W	

- : Unused

(2) Block diagram



Note : Do not access to this register in the middle of the operation of the address 008000$_H$ to 00FFFF$_H$.

18. Interrupt controller

Interrupt control register is in the interrupt controller. The register corresponds to all I/O of interrupt function. The register has following functions;

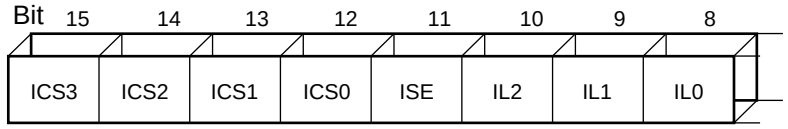
- Setting of Interrupt level at correspondent peripheral circuit.

(1) Register list (at writing)

Interrupt control register

Address :

ICR01 0000B1H
ICR03 0000B3H
ICR05 0000B5H
ICR07 0000B7H
ICR09 0000B9H
ICR11 0000BBH
ICR13 0000BDH
ICR15 0000BFH



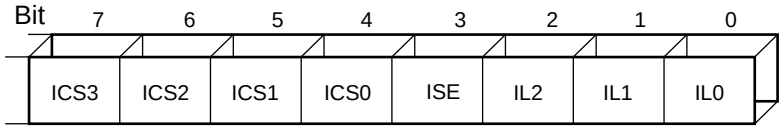
ICR01, 03, 05, 07, 09, 11, 13, 15

Read/Write →	W	W	W	W	R/W	R/W	R/W	R/W
Initial Value →	(0)	(0)	(0)	(0)	(0)	(1)	(1)	(1)

Interrupt control register

Address :

ICR00 0000B0H
ICR02 0000B2H
ICR04 0000B4H
ICR06 0000B6H
ICR08 0000B8H
ICR10 0000BAH
ICR12 0000BCH
ICR14 0000BEH



ICR00, 02, 04, 06, 08, 10, 12, 14

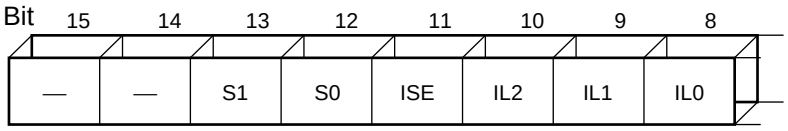
Read/Write →	W	W	W	W	R/W	R/W	R/W	R/W
Initial Value →	(0)	(0)	(0)	(0)	(0)	(1)	(1)	(1)

(2)Register list (at reading)

Interrupt control register

Address :

ICR01	0000B1H
ICR03	0000B3H
ICR05	0000B5H
ICR07	0000B7H
ICR09	0000B9H
ICR11	0000BBH
ICR13	0000BDH
ICR15	0000BFH



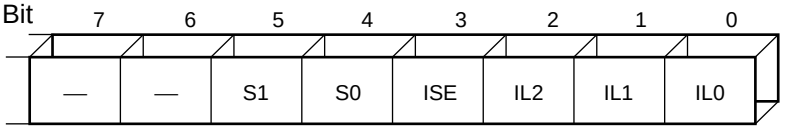
ICR01, 03, 05, 07, 09, 11, 13, 15

Read/Write →	—	—	R	R	R/W	R/W	R/W	R/W
Initial Value →	(—)	(—)	(0)	(0)	(0)	(1)	(1)	(1)

Interrupt control register

Address :

ICR00	0000B0H
ICR02	0000B2H
ICR04	0000B4H
ICR06	0000B6H
ICR08	0000B8H
ICR10	0000BAH
ICR12	0000BCH
ICR14	0000BEH

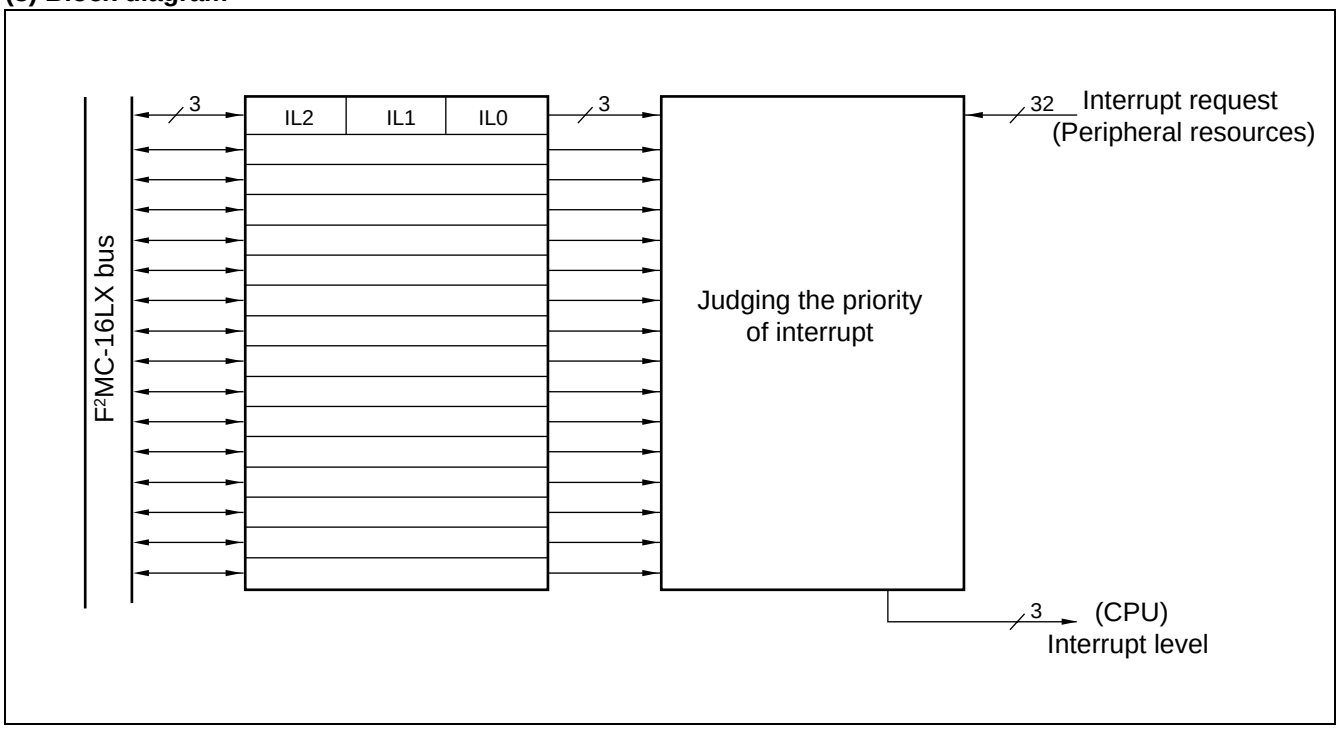


ICR00, 02, 04, 06, 08, 10, 12, 14

Read/Write →	—	—	R	R	R/W	R/W	R/W	R/W
Initial Value →	(—)	(—)	(0)	(0)	(0)	(1)	(1)	(1)

Note : Do not access using the read modify write instruction because it causes a malfunction.

(3) Block diagram



19. LCD controller/driver

The LCD controller/driver contains 24 × 8-bit display data memory and controls the LCD display with four common output lines and 48 segment output lines. Three duty outputs can be selected to directly drive the LCD panel (liquid crystal display).

- Contains an LCD driving voltage split resistor. Moreover, the external division resistance can be connected.
- A maximum of four common output lines (COM0 to COM3) and 48 segment output lines (SEG0 to SEG47) are available.
- Contains 24-byte display data memory (display RAM).
- For the duty, 1/2, 1/3, or 1/4 can be selected (restricted by bias setting).
- The LCD can directly be driven.

Bias	1/2 duty	1/3 duty	1/4 duty
1/2 bias	○	×	×
1/3 bias	×	○	○

○ : Recommended mode

× : Disable

(1) Register list

• LCR (LCD control register)

LCD control register (higher) (LCRH)

00005D$_H$

15	14	13	12	11	10	9	8	
SS4	VS0	CS1	CS0	SS3	SS2	SS1	SS0	
(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	Read/Write
(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	Initial Value

LCD control register (lower) (LCRL)

00005C$_H$

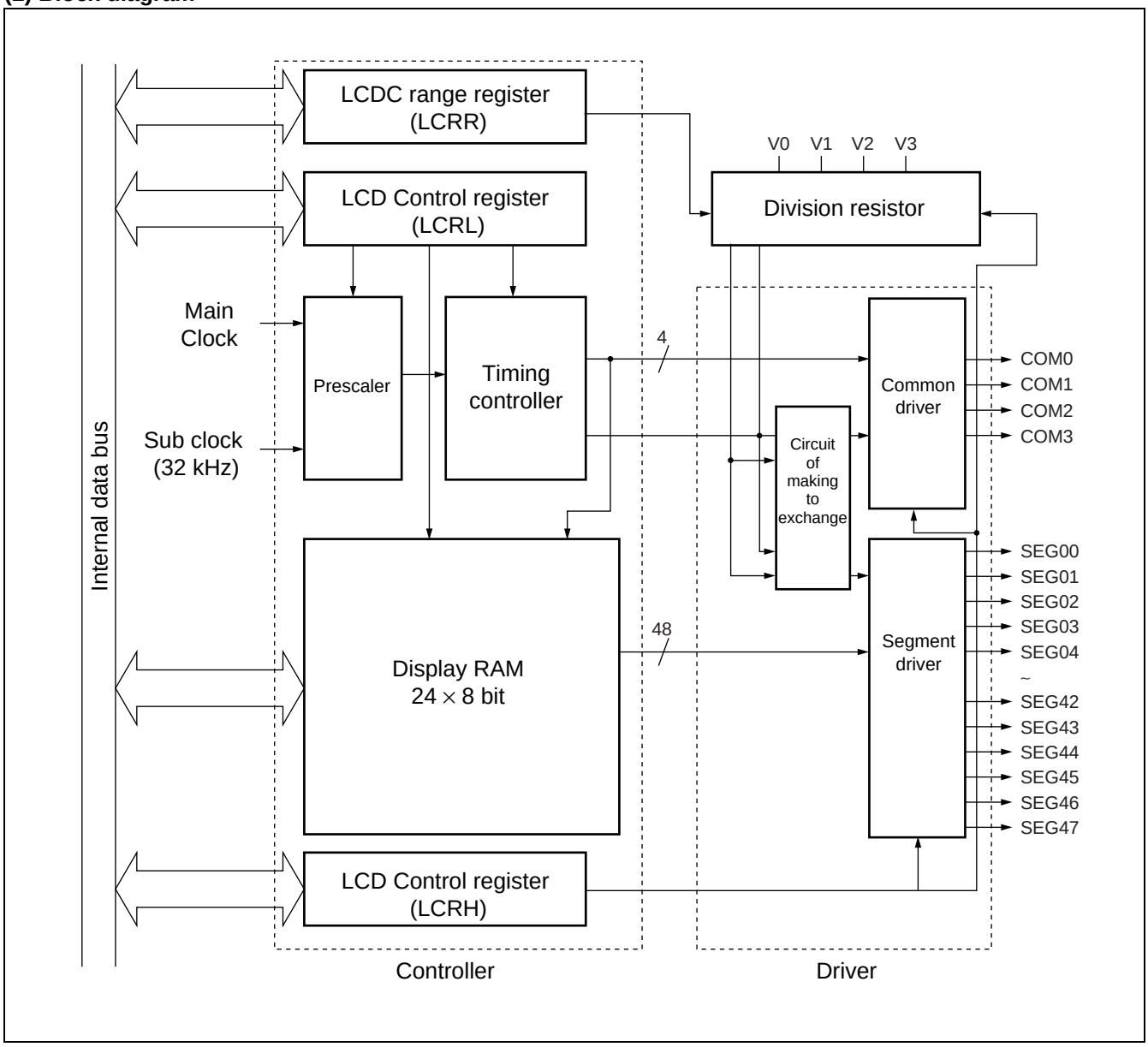
7	6	5	4	3	2	1	0	
CSS	LCEN	VSEL	BK	MS1	MS0	FP1	FP0	
(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	Read/Write
(0)	(0)	(0)	(1)	(0)	(0)	(0)	(0)	Initial Value

• LCDC range register (LCRR)

00005E$_H$

7	6	5	4	3	2	1	0	
Reserved	Reserved	SE4	SE3	SE2	SE1	SE0	LCR	
(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	Read/Write
(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	Initial Value

(2) Block diagram



■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC}	V_{SS} – 0.3	V_{SS} + 4.0	V	
	AV_{CC}	V_{SS} – 0.3	V_{SS} + 4.0	V	$V_{CC} \geq AV_{CC}$*1
Input voltage	V_I	V_{SS} – 0.3	V_{SS} + 4.0	V	*2
		V_{SS} – 0.3	V_{SS} + 6.0	V	N-ch O.D (5 V withstand voltageI/O)
Output voltage	V_O	V_{SS} – 0.3	V_{SS} + 4.0	V	*2
“L” level maximum output current	I_{OL11}	—	10	mA	Other than P74, P75, P40 to P47*3
	I_{OL12}	—	30	mA	P74, P75, P40 to P47 (Heavy-current output port) *3
“L” level average output current	I_{OLAV1}	—	3	mA	Other than P74, P75, P40 to P47*4
	I_{OLAV2}	—	15	mA	P74, P75, P40 to P47 (Heavy-current output port) *4
“L” level maximum total output current	ΣI_{OL}	—	120	mA	
“L” level average total output current	ΣI_{OLAV}	—	60	mA	*5
“H” level maximum output current	I_{OH11}	—	– 10	mA	Other than P74, P75, P40 to P47*3
	I_{OH12}	—	– 12	mA	P40 to P47 (Heavy-current output port) *3
“H” level average output current	I_{OHAV}	—	– 3	mA	*4
“H” level maximum total output current	ΣI_{OH}	—	– 120	mA	
“H” level average total output current	ΣI_{OHAV}	—	– 60	mA	*5
Power consumption	Pd	—	351	mW	
Operating temperature	T_A	– 40	+ 85	°C	
Storage temperature	Tstg	– 55	+ 150	°C	

The Absolute Maximum Ratings is based on $V_{SS} = AV_{SS} = 0.0$ V.

*1 : AV_{CC} should not be exceeding V_{CC} at power-on etc.

*2 : V_I, V_O, should not exceed Vcc + 0.3 V.

*3 : A peak value of an applicable one pin is specified as a maximum output current.

*4 : An average current value of an applicable one pin within 100 ms is specified as an average output current. (Average value is found by multiplying operating current by operating rate.)

*5 : An average current value of all pins within 100 ms is specified as an average total output current. (Average value is found by multiplying operating current by operating rate.)

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC}	2.7	3.6	V	At normal operating
		1.8	3.6	V	Stop operation state maintenance
"H" level input voltage	V_{IH}	0.7 V_{CC}	V_{CC} + 0.3	V	CMOS input pin
	V_{IHS}	0.8 V_{CC}	V_{CC} + 0.3	V	CMOS hysteresis input pin (Resisting pressure of 5 V is V_{CC} = 5.0 V)
	V_{IHM}	V_{CC} – 0.3	V_{CC} + 0.3	V	MD pin input
"L" level input voltage	V_{IL}	V_{SS} – 0.3	0.3 V_{CC}	V	CMOS input pin
	V_{ILS}	V_{SS} – 0.3	0.2 V_{CC}	V	CMOS hysteresis input pin
	V_{ILM}	V_{SS} – 0.3	V_{SS} + 0.3	V	MD pin input
Operating temperature	T_A	– 40	+ 85	°C	

The Recommended Operating Conditions is based on V_{SS} = AV_{SS} = 0.0 V.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

3. DC Characteristics

(V_{CC} = AV_{CC} = 3.3 V ± 0.3 V, T_A = – 40 to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level output voltage	V_{OH}	Output pins other than P40 to P47, P74, P75	I_{OH} = – 4.0 mA	V_{CC} – 0.5	—	Vcc	V	
	V_{OH1}	P40 to P47	I_{OH} = – 8.0 mA	V_{CC} – 0.5	—	Vcc	V	Heavy-current output port
"L" level output voltage	V_{OL}	Output pins other than P40 to P47, P74, P75	I_{OL} = 4.0 mA	Vss	—	Vss + 0.4	V	
	V_{OL1}	P40 to P47	I_{OL} = 15.0 mA	Vss	—	Vss + 0.6	V	Heavy-current output port
	V_{OL2}	P74, P75	I_{OL} = 15.0 mA	—	0.5	Vss + 0.8	V	Open-drain pin
Open-drain output application voltage	V_{D1}	P74, P75	—	Vss – 0.3	—	Vss + 5.5	V	
Input leak current	I_{IL}	All output pin	V_{CC} = 3.3 V, V_{SS} < V_I < V_{CC}	– 10	—	10	µA	
Pull-up resistor	R_{UP}	$\overline{RST}$	Vcc = 3.3 V, T_A = + 25 °C	25	50	100	kΩ	
Pull-down resistor	R_{DOWN}	MD2	Vcc = 3.3 V, T_A = + 25 °C	25	50	100	kΩ	Except FLASH products
Open drain output current	I_{leak}	P74, P75	—	—	0.1	10	µA	

The DC Characteristics is based on V_{SS} = AV_{SS} = 0.0 V.

(Continued)

(V_{CC} = AV_{CC} = 3.3 V ± 0.3 V, T_A = – 40 to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current	I_{CC}	V_{CC}	V_{CC} = 3.3 V, Internal frequency 25 MHz At normal operating	—	48	60	mA	
			V_{CC} = 3.3 V, Internal frequency 25 MHz At Flash writing	—	60	75	mA	FLASH products
			V_{CC} = 3.3 V, Internal frequency 25 MHz At Flash erasing	—	60	75	mA	FLASH products
	I_{CCS}		V_{CC} = 3.3 V, Internal frequency 25 MHz at sleep mode	—	22.5	30	mA	
	I_{CCTS}		V_{CC} = 3.3 V, Internal frequency 3 MHz at timer mode	—	0.75	7	mA	
	I_{CCL}		V_{CC} = 3.3 V, Internal frequency 8 kHz at subclock operation, (T_A = + 25 °C)	—	15	140	µA	MASK products
				—	0.5	0.9	mA	FLASH products
	I_{CCLS}		V_{CC} = 3.3 V, Internal frequency 8 kHz at subclock sleep operation, (T_A = + 25 °C)	—	23	40	µA	
	I_{CCT}		V_{CC} = 3.3 V, Internal frequency 8 kHz at watch mode (T_A = + 25 °C)	—	1.8	40	µA	
	I_{CCH}		At Stop mode, (T_A = + 25 °C)	—	0.8	40	µA	
LCD division resistance	R_{LCD}	V_{CC} – V3	At LCR = 0 setting	100	200	400	kΩ	*
		V_{CC} – V3	At LCR = 1 setting	12.5	25	50		
		V0 – V1, V1 – V2, V2 – V3	At LCR = 0 setting	50	100	200		
		V0 – V1, V1 – V2, V2 – V3	At LCR = 1 setting	6.25	12.5	25		
COM0 to COM3 output impedance	R_{VCOM}	COM0 to COM3	V1 to V3 = 3.3 V	—	—	2.5	kΩ	
SEG00 to SEG47 output impedance	R_{VSEG}	SEG00 to SEG47		—	—	15	kΩ	

The DC Characteristics is based on V_{SS} = AV_{SS} = 0.0 V.

(Continued)

(Continued)

(V_{CC} = AV_{CC} = 3.3 V ± 0.3 V, T_A = – 40 to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
LCD leak current	I_{LCDC}	V0 to V3, COM0 to COM3, SEG00 to SEG47	—	– 5	—	5	µA	

The DC Characteristics is based on V_{SS} = AV_{SS} = 0.0 V.

* : LCD internal diveded resistor can be select two type resistor by LCR (internal diveded resistor selecting bit) of LCRR (LCDC range register) .

4. AC Characteristics

(1) Clock timing

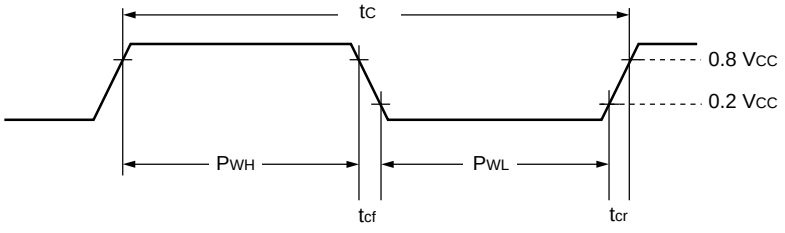
(V_{CC} = AV_{CC} = 3.3 V ± 0.3 V, Ta = – 40 to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Clock frequency	f_{CH}	X0, X1	—	3	—	16	MHz	External crystal oscillation
	f_{CH}	X0, X1		3	—	25	MHz	At external clock*
				4.5	—	25		Multiply by 1
				4	—	12.5		Multiply by 2
				4	—	8.33		Multiply by 3
				4	—	6.25		Multiply by 4
	f_{CL}	X0A, X1A		—	32.768	—	kHz	
Clock cycle time	t_{HCYL}	X0, X1		40	—	333	ns	
	t_{LCYL}	X0A, X1A		—	30.5	—	µs	
Input clock pulse width	P_{WH} P_{WL}	X0		5	—	—	ns	Set Duty ratio 50% ± 3%
	P_{WLH} P_{WLL}	X0A		—	15.2	—	µs	Set duty ratio at 30% to 70% as a guideline.
Input clock rise time and fall time	tcr tcf	X0		—	—	5	ns	At external clock
Internal operating clock frequency	f_{CP}	—		1.5	—	25	MHz	When main clock is used
	f_{CP1}	—		—	8.192	—	kHz	When sub clock is used
Internal operating clock cycle time	t_{CP}	—		40	—	666	ns	When main clock is used
	t_{CP1}	—		—	122.1	—	µs	When sub clock is used

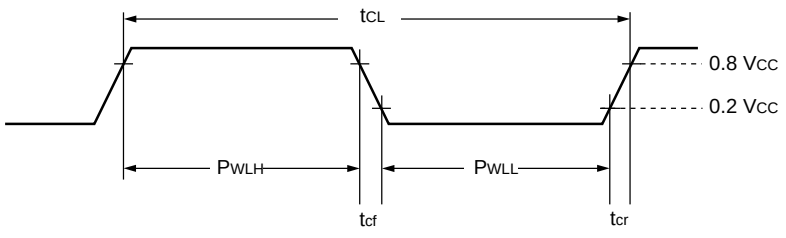
The Clock timing is based on V_{SS} = AV_{SS} = 0.0 V.

* : When selecting the PLL clock, the range of clock frequency is limited. Use this product within range as mentioned in “Base oscillator frequency vs. Internal operating clock frequency”.

• X0, X1 clock timing

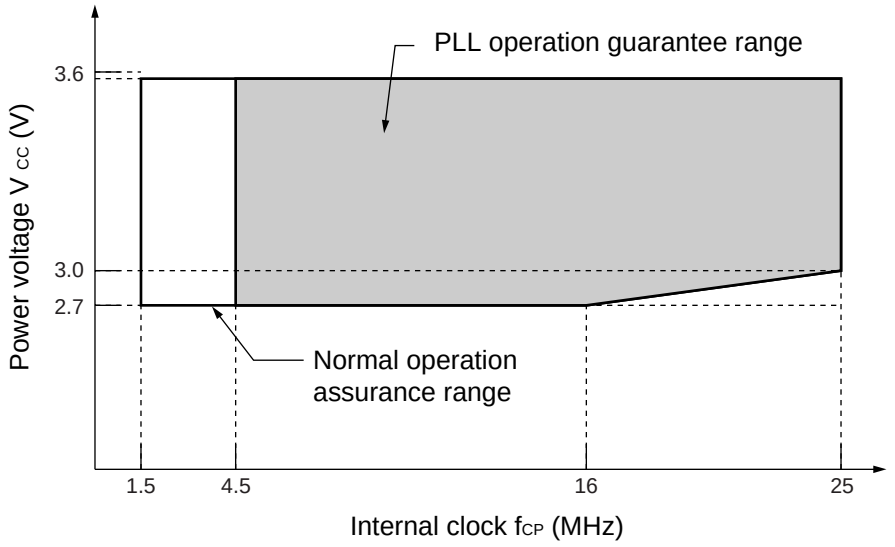


• X0A, X1A clock timing

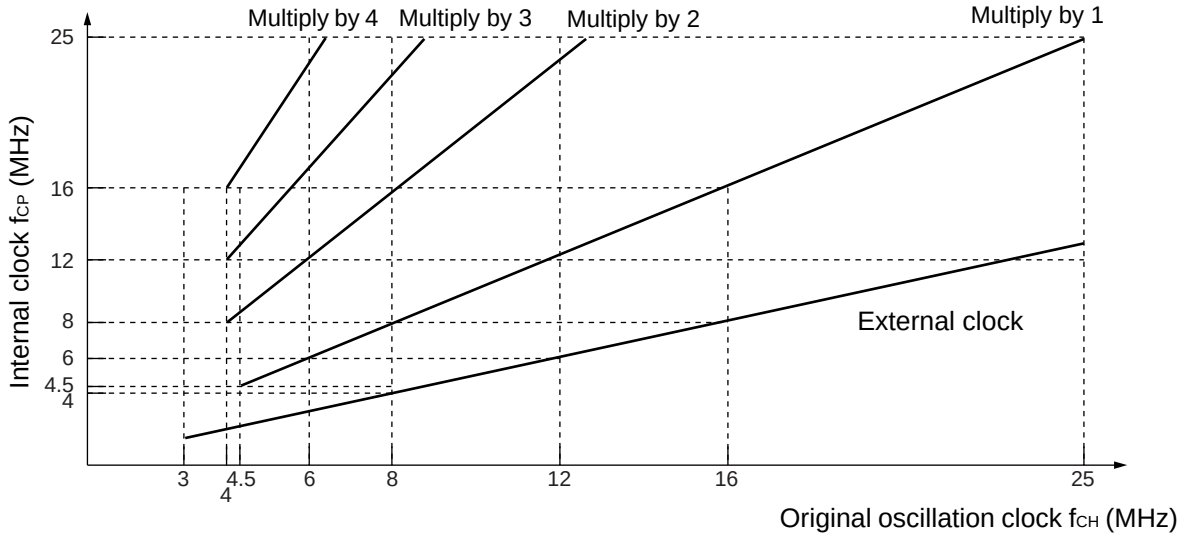


—PLL operation guarantee range

Relation between internal operation clock frequency and power supply voltage



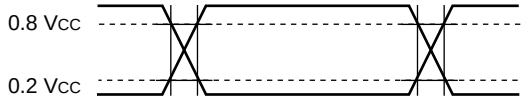
Relation between oscillation frequency and internal operating clock frequency



Rating values of alternating current is defined by the measurement reference voltage values shown below :

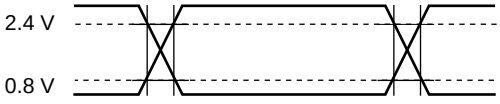
- Input signal waveform

Hysteresis input pin



- Output signal waveform

Output pin



(2) Reset input timing

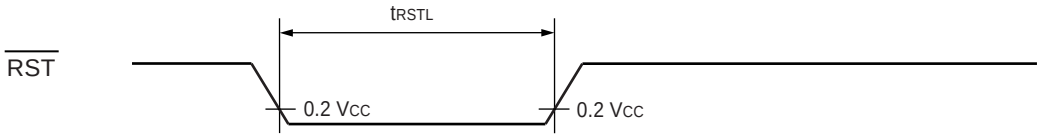
(V_{CC} = AV_{CC} = 3.3 V ± 0.3 V, Ta = – 40 to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Reset input time	t_{RSTL}	$\overline{RST}$	—	500	—	ns	At normal operating, at time base timer mode, at main leep mode, at PLL sleep mode
				Oscillation time of oscillator*+ 500 ns	—	µs	At stop mode, at sub clock mode, at sub sleep mode, at watch mode

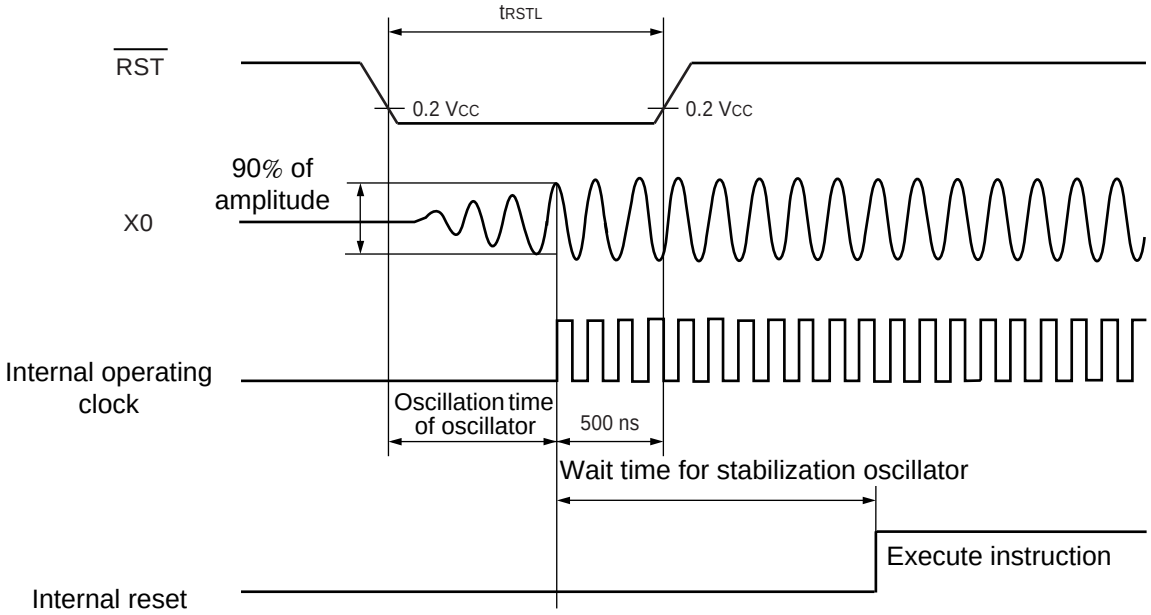
The Reset input timing is based on V_{SS} = AV_{SS} = 0.0 V.

* : Oscillation time of oscillator is time until oscillation reaches 90% of amplitude. It takes several milliseconds to several dozens of milliseconds on a crystal oscillator, several hundreds of microseconds to several milliseconds on a FAR/ceramic oscillator, and 0 milliseconds on an external clock.

- In normal operating, time base timer mode, main sleep mode and PLL sleep mode



- In stop mode, sub clock mode, sub sleep mode and watch mode



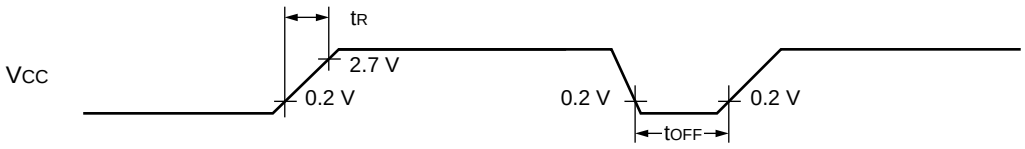
(3) Power-on reset

(V_{CC} = AV_{CC} = 3.3 V ± 0.3 V, Ta = – 40 to + 85 °C)

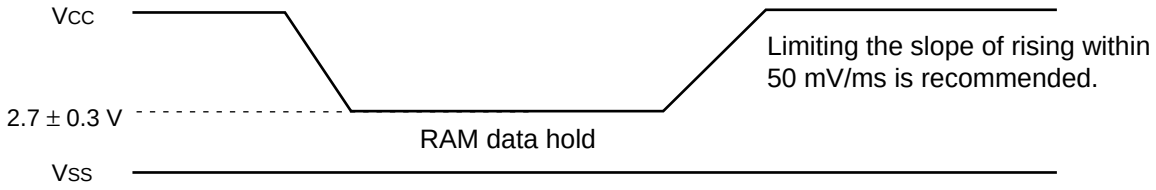
Parameter	Symbol	Pin name	Condi-tions	Value		Unit	Remarks
				Min	Max		
Power supply rising time	t_R	V_{CC}	—	—	30	ms	At normal operating
Power supply shutdown time	t_{OFF}	V_{CC}		1	—	ms	For repeated operation

The Power-on reset is based on V_{SS} = AV_{SS} = 0.0 V.

Notes :
- V_{CC} should be set under 0.2 V before power-on rising up.
- These value are for power-on reset.
- In the device, there are internal registers which is initialized only by a power-on reset. If these initialization is executing, power-on prosedure must be obeyed by these value.



Sudden change of power supply voltage may activate the power-on reset function. When changing power supply voltages during operation, raise the power smoothly by suppressing variation of voltages as shown below. When raising the power, do not use PLL clock. However, if voltage drop is 1mV/s or less, use of PLL clock is allowed during operation.



(4) Serial I/O

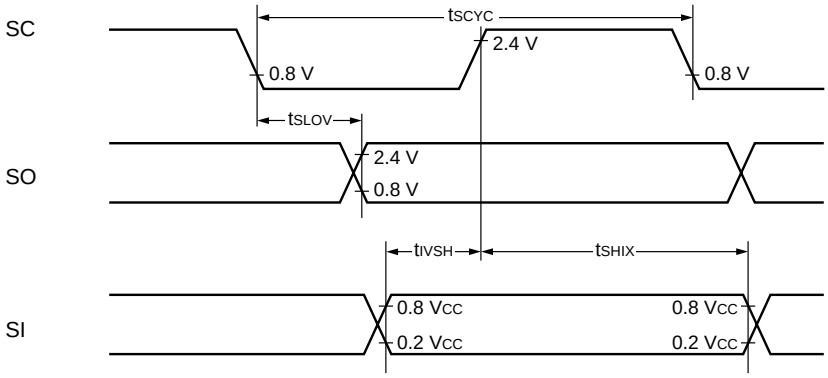
(V_{CC} = AV_{CC} = 3.3 V ± 0.3 V, Ta = – 40 to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SC0 to SC3	Internal shift clock mode output pin : C_L = 80 pF + 1TTL	8 t_{CP}	—	ns	
SCK ↓ → SOT delay time	t_{SLOV}	SC0 to SC3 SO0 to SO3		–80	80	ns	
Valid SIN → SCK ↑	t_{IVSH}	SC0 to SC3 SI0 to SI3		100	—	ns	
SCK ↑ → Valid SIN hold time	t_{SHIX}			60	—	ns	
Serial clock H pulse width	t_{SHSL}	SC0 to SC3	External shift clock mode output pin : C_L = 80 pF + 1TTL	4 t_{CP}	—	ns	
Serial clock L pulse width	t_{SLSH}			4 t_{CP}	—	ns	
SCK ↓ → SOT delay time	t_{SLOV}	SC0 to SC3 SO0 to SO3		—	150	ns	
Valid SIN → SCK ↑	t_{IVSH}	SC0 to SC3 SI0 to SI3		60	—	ns	
SCK ↑ → valid SIN hold time	t_{SHIX}			60	—	ns	

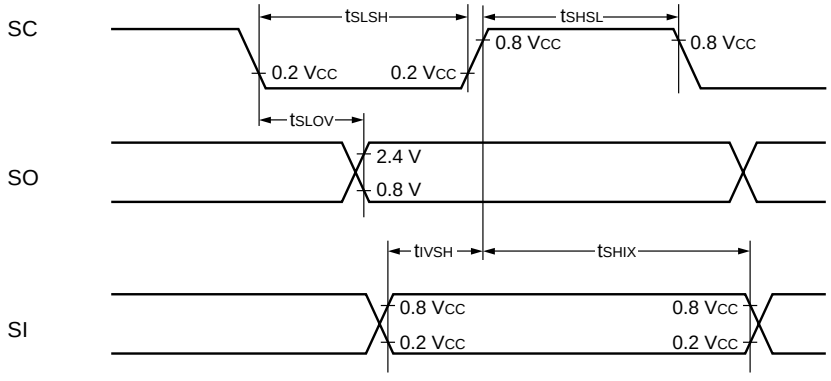
The Serial I/O is based on V_{SS} = AV_{SS} = 0.0 V.

Notes :
- AC rating in CLK synchronous mode.
- C_L is a load capacitance value on pins for testing.
- t_{CP} is machine cycle frequency (ns) .

• Internal shift clock mode



• External shift clock mode



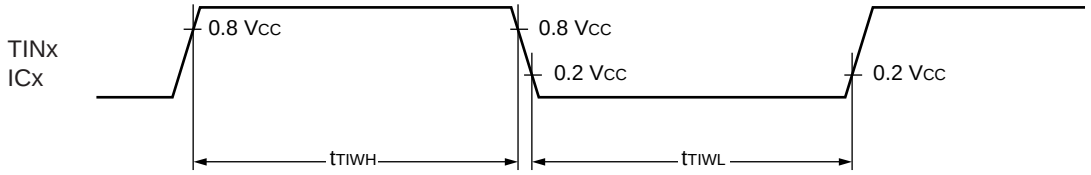
(5) Timer input timing

(V_{CC} = AV_{CC} = 3.3 V ± 0.3 V, Ta = – 40 to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH} t_{TIWL}	TIN0 to TIN2 IC0 to IC1	—	4 t_{CP}	—	ns	

The Timer input timing is based on V_{SS} = AV_{SS} = 0.0 V.

• Timer Input Timing



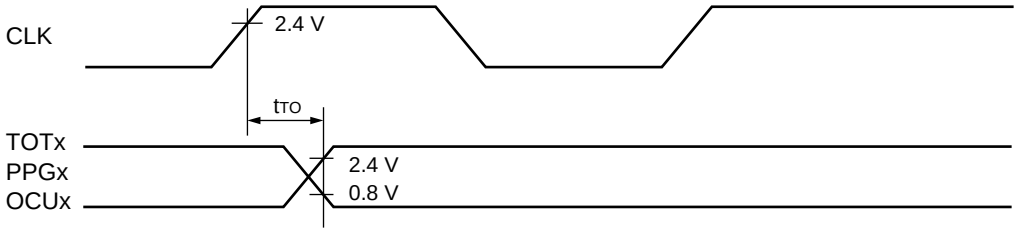
(6) Timer output timing

(V_{CC} = AV_{CC} = 3.3 V ± 0.3 V, Ta = – 40 to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
CLK ↑ → T_{OUT} change time	t_{TO}	TOT0 to TOT2, PPG0 to PPG1, OCU0 to OCU1	—	30	—	ns	

The Timer output timing is based on V_{SS} = AV_{SS} = 0.0 V.

• Timer Output Timing



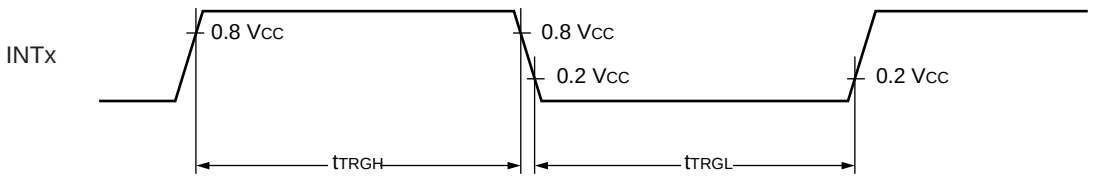
(7) Trigger Input Timing

(V_{CC} = AV_{CC} = 3.3 V ± 0.3 V, Ta = – 40 to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH} t_{TRGL}	INT0 to INT3	—	5 t_{CP}	—	ns	At normal operating
				1	—	µs	In Stop mode

The Trigger Input Timing is based on V_{SS} = AV_{SS} = 0.0 V.

• Trigger Input Timing



(8) I²C Timing

($AV_{CC} = V_{CC} = 3.3\ V \pm 0.3\ V$, $Ta = -40$ to $+85\ °C$)

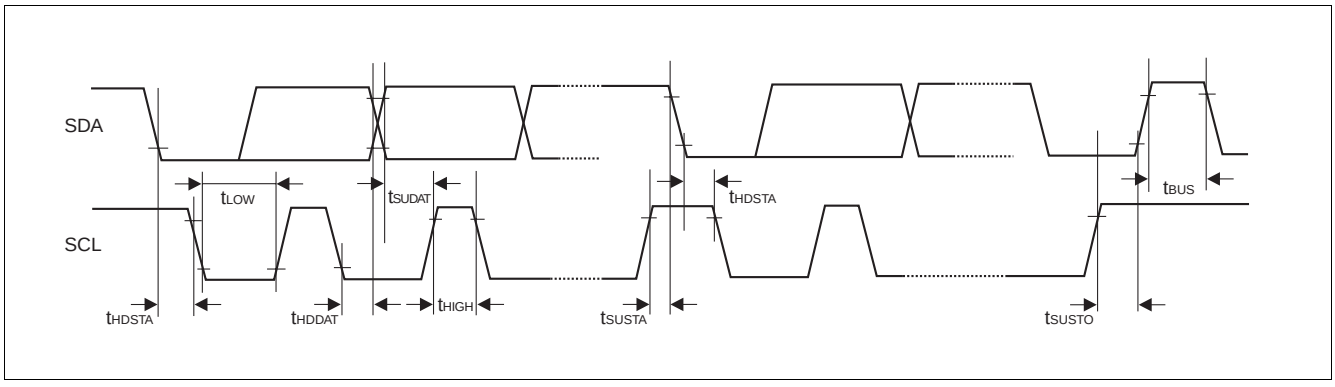
Parameter	Symbol	Conditions	Standard-mode		Unit
			Min	Max	
SCL clock frequency	f_{SCL}	When power supply voltage of external pull-up resistor is 5.0 V R = 1.0 kΩ, C = 50 pF*2 When power supply voltage of external pull-up resistor is 3.6 V R = 1.0 kΩ, C = 50 pF*2	0	100	kHz
Hold time (repeated) START condition SDA ↓ → SCL ↓	t_{HDSTA}		4.0	—	µs
"L" width of the SCL clock	t_{LOW}		4.7	—	µs
"H" width of the SCL clock	t_{HIGH}		4.0	—	µs
Set-up time for a repeated START condition SCL ↑ → SDA ↓	t_{SUSTA}		4.7	—	µs
Data hold time SCL ↓ → SDA ↓ ↑	t_{HDDAT}		0	3.45 *3	µs
Data set-up time SDA ↓ ↑ → SCL ↑	t_{SUDAT}	When power supply voltage of external pull-up resistor is 5.0 V f_{CP}*1 ≤ 20 MHz, R = 1.0 kΩ, C = 50 pF*2 When power supply voltage of external pull-up resistor is 3.6 V f_{CP}*1 ≤ 20 MHz, R = 1.0 kΩ, C = 50 pF*2	250	—	ns
		When power supply voltage of external pull-up resistor is 5.0 V f_{CP}*1 ≤ 20 MHz, R = 1.0 kΩ, C = 50 pF*2 When power supply voltage of external pull-up resistor is 3.6 V f_{CP}*1 ≤ 20 MHz, R = 1.0 kΩ, C = 50 pF*2	200	—	ns
Set-up time for STOP condition SCL ↑ → SDA ↑	t_{SUSTO}	When power supply voltage of external pull-up resistor is 5.0 V R = 1.0 kΩ, C = 50 pF*2 When power supply voltage of external pull-up resistor is 3.6 V R = 1.0 kΩ, C = 50 pF*2	4.0	—	µs
Bus free time between a STOP and START condition	t_{BUS}		4.7	—	µs

The I²C trriger is based on $AV_{SS} = V_{SS} = 0.0\ V$.

*1 : f_{CP} is internal operation clock frequency. Refer to " (1) Clock timing".

*2 : R, C : Pull-up resistor and load capacitor of the SCL and SDA lines.

*3 : The maximum t_{HDDAT} only has to be met if the device does not stretch the "L" width (t_{LOW}) of the SCL signal.



5. Electrical Characteristics for the A/D Converter

(V_{CC} = AV_{CC} = 3.3 V ± 0.3 V, Ta = – 40 to + 85 °C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	10	bit	
Total error	—	—	—	—	± 3.0	LSB	
Nonlinear error	—	—	—	—	± 2.5	LSB	
Differential linear error	—	—	—	—	± 1.9	LSB	
Zero transition voltage	V_{OT}	AN0 to AN11	AV_{SS} – 1.5 LSB	AVss + 0.5 LSB	AV_{SS} + 2.5 LSB	mV	1 LSB = AVcc/1024
Full-scale transition voltage	V_{FST}	AN0 to AN11	AVcc – 3.5 LSB	AVcc – 1.5 LSB	AVcc + 0.5 LSB	mV	
Conversion time	—	—	8.64*1	—	—	µs	
Sampling time	—	—	2	—	—	µs	
Analog port input current	I_{AIN}	AN0 to AN11	—	—	10	µA	
Analog input voltage	V_{AIN}	AN0 to AN11	0	—	AVcc	V	
Reference voltage	—	AVcc	3.0	—	AVcc	V	
Power supply current	I_A	AVcc	—	1.4	3.5	mA	
	I_{AH}	AVcc	—	—	5*2	µA	
Reference voltage supplying current	I_R	AVcc	—	94	150	µA	
	I_{RH}	AVcc	—	—	5*2	µA	
Interchannel disparity	—	AN0 to AN11	—	—	4	LSB	

The Electrical characteristics for the A/D converter is based on V_{SS} = AV_{SS} = 0.0 V.

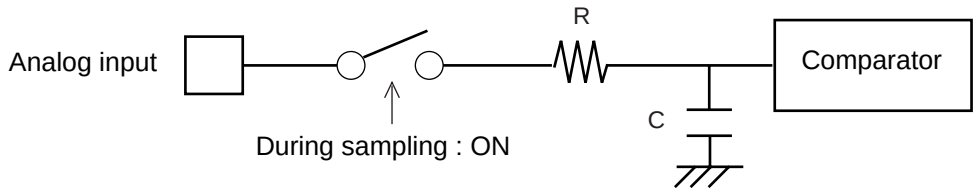
*1 : At operating, main clock 25 MHz.

*2 : If A/D converter is not operating, a current when CPU is stopped is applicable (at Vcc – CPU = AVcc = 3.3 V)

<About the external impedance of analog input and its sampling time>

- A/D converter with sample and hold circuit. If the extrernal impedance is too high to keep sufficient sampling time, the analog voltage changed to the internal sample and hold capacitor is insufficient, adversely affecting A/D conversion precision.

Analog input circuit model

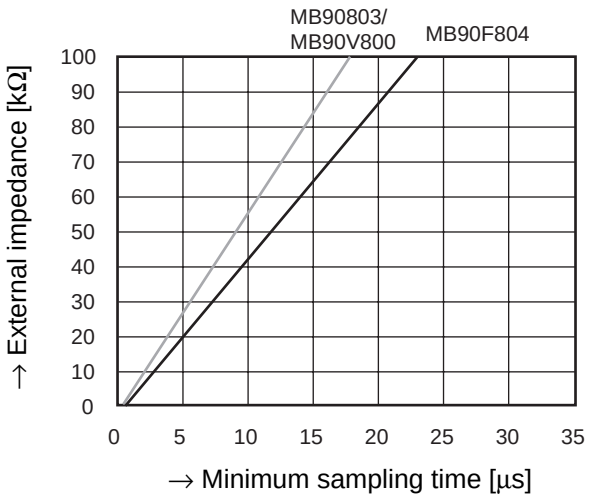


	R	C
MB90803	1.9 kΩ (Max)	32.3 pF (Max)
MB90F804	1.9 kΩ (Max)	25.0 pF (Max)
MB90V800	1.9 kΩ (Max)	32.3 pF (Max)

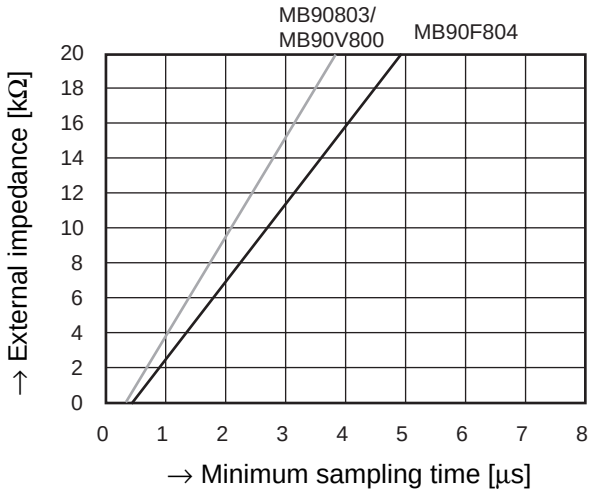
Note : The values are reference values.

- To satisfy the A/D conversion precision standard, consider the relationship between the external impedance and minimum sampling time and either adjust the resistor value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value.

[External impedance = 0 kΩ to 100 kΩ]



[External impedance = 0 kΩ to 20 kΩ]



The relationship between external impedance and minimum sampling time

- If the sampling time cannot be sufficient, connect a capacitor of about 0.1 µF to the analog input pin.

<About errors>

- As | AV_{CC} | becomes smaller, values of relative errors grow larger.

6. Definition of A/D Converter Terms

Resolution

Analog variation that is recognized by an A/D converter.

The 10-bit can resolve analog voltage into $2^{10} = 1024$.

Total error

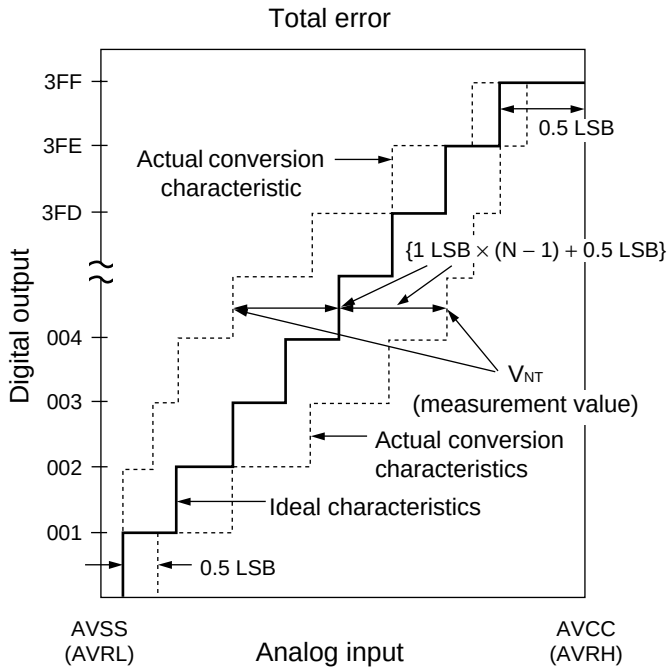
This shows the difference between the actual voltage and the ideal value and means a total of error because of offset error, gain error, non-linearity error and noise.

Linearity error

Deviation between a line across zero-transition line (00 0000 0000↔00 0000 0001) and full-scale transition line (11 1111 1110↔11 1111 1111) and actual conversion characteristics.

Differential linear error

Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value.



$$\text{Total error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$1\text{LSB(Ideal value)} = \frac{AVCC - AVSS}{1024}\ [V]$$

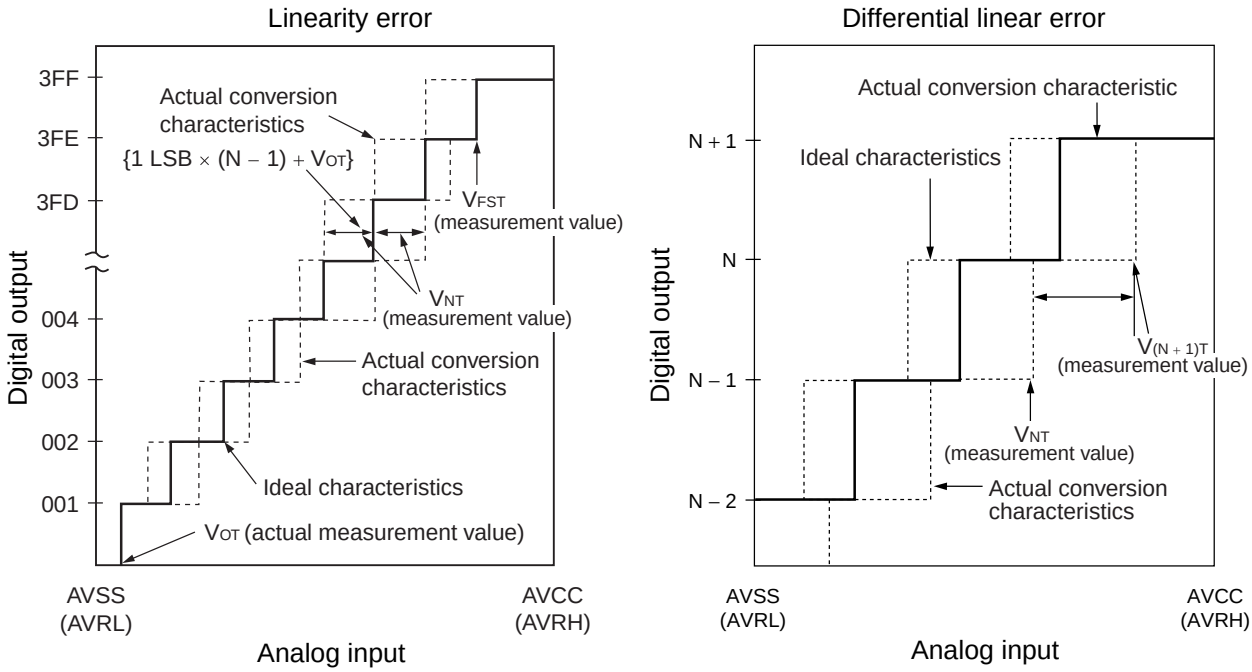
V_{OT}(Ideal value) = AVSS + 0.5 LSB [V]

V_{FST}(Ideal value) = AVCC – 1.5 LSB [V]

V_{NT}: A voltage at which digital output transitions from (N-1) to N.

(Continued)

(Continued)



$$\text{Linear error in digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + V_{OT}\}}{1\ \text{LSB}}\ \text{[LSB]}$$

$$\text{Differential linear error in digital output N} = \frac{V_{(N+1)T} - V_{NT}\}}{1\ \text{LSB}} - 1\text{LSB}\ \text{[LSB]}$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ \text{[V]}$$

V_{OT} : Voltage at which digital output transits from 000_H to 001_H.

V_{FST} : Voltage at which digital output transits from $3FE_H$ to $3FF_H$.

7. FLASH MEMORY

Parameter	Conditions	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	T_A = + 25 °C Vcc = 3.0 V	—	1	15	s	Excludes 00 H programming prior to erasure.
Chip erase time		—	9	—	µs	Excludes 00 H programming prior to erasure.
Word (16 bit width) programming time		—	16	3,600	s	Except for the over head time of the system.
Program/erase cycle	—	10,000	—	—	cycle	
Flash data retension time	Average T_A = + 85 °C	20	—	—	Yearss	*

* : This value comes from the technology qualification (using Arrhenius equation to translate high temperature measuremunts into normalized value at + 85 °C).

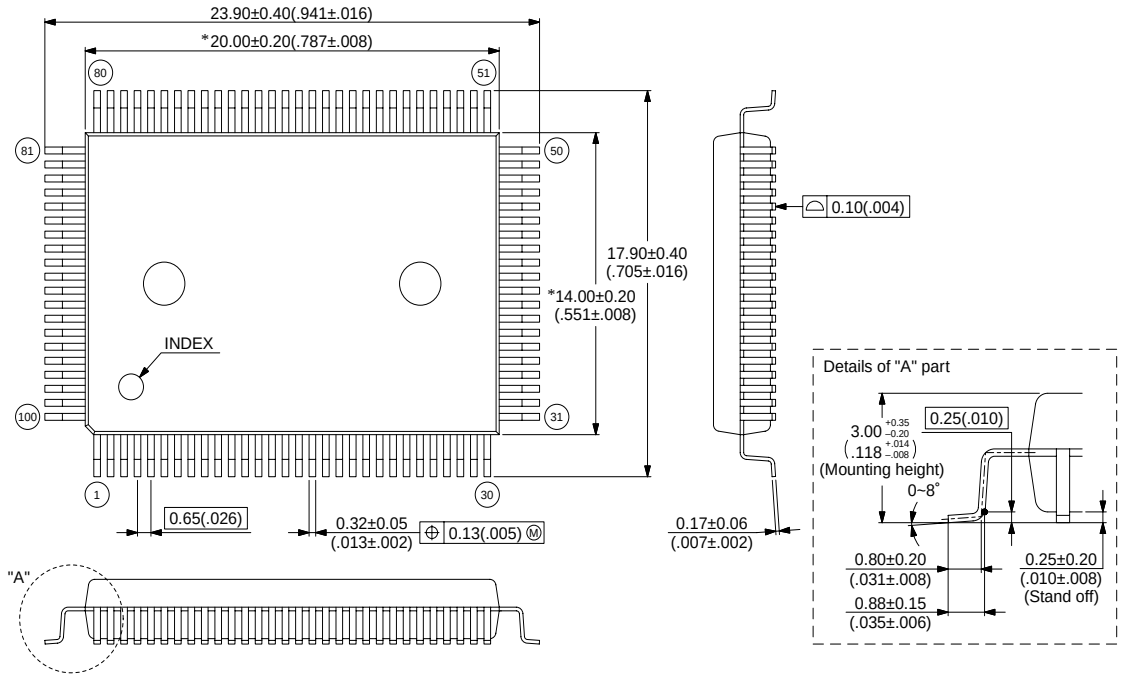
■ ORDERING INFORMATION

Part number	Package	Remarks
MB90F804-101PF-G MB90F804-201PF-G	100-pin plastic QFP (FPT-100P-M06)	
MB90803PF MB90803SPF		

■ PACKAGE DIMENSION

100-pin plastic QFP
(FPT-100P-M06)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches) .
Note : The values in parentheses are reference values.

MEMO

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