FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-13742-1E

16-bit Proprietary Microcontroller

CMOS

F²MC-16LX MB90980 Series

MB90982/MB90F983/MB90V485B

■ DESCRIPTION

The MB90980 series is a 16-bit general-purpose FUJITSU microcontroller designed for process control in consumer devices and other applications requiring high-speed real-time processing.

The F²MC-16LX CPU core instruction set retains the AT architecture of the F²MC*1 family, with additional instructions for high-level languages, expanded addressing mode, enhanced multiply-drive instructions, and complete bit processing. In addition, a 32-bit accumulator is provided to enable long-word processing.

The MB90980 series features embedded peripheral resources including 8/16-bit PPG, expanded I/O serial interface, UART, 10-bit A/D converter, 16-bit I/O timer, 8/16-bit up/down-counter, PWC timer, I²C*2 interface, DTP/external interrupt, chip select, and 16-bit reload timer.

*1 : F²MC is the abbreviation of FUJITSU Flexible Microcontroller.

*2 : Purchase of Fujitsu I²C components conveys a license under the Philips I²C Patent Rights to use, these components in an I²C system provided that the system conforms to the I²C standard Specification as defined by Philips.

■ FEATURES

- Clock
  - Minimum instruction execution time:
    40.0 ns/6.25 MHz base frequency multiplied × 4 (25 MHz internal operating frequency/3.3 V ± 0.3 V)
    62.5 ns/4 MHz base frequency multiplied × 4 (16 MHz internal operating frequency/3.0 V ± 0.3 V)
    PLL clock multiplier

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Be sure to refer to the “Check Sheet” for the latest cautions on development.

“Check Sheet” is seen at the following support page
URL : http://jp.fujitsu.com/microelectronics/products/micom/support/index.html

“Check Sheet” lists the minimal requirement items to be checked to prevent problems beforehand in system development.

(Continued)

- Maximum memory space
  - 16 Mbytes
- Instruction set optimized for controller applications
  - Supported data types (bit, byte, word, or long word)
  - Typical addressing modes (23 types)
  - Enhanced signed multiplication/division instruction and RETI instruction functions
  - 32-bit accumulator for enhanced high-precision calculation
- Instruction set designed for high-level language (C) and multi-task operations
  - System stack pointer adopted
  - Instruction set compatibility and barrel shift instructions
- Enhanced execution speed
  - 4 byte instruction queue
- Enhanced interrupt functions
  - 8 levels setting with programmable priority, 8 external interrupt pins
- Data transmission function (μDMAC)
  - Up to 16 channels
- Embedded ROM
  - Flash versions : 192 Kbytes, Mask versions : 128 Kbytes
- Embedded RAM
  - Flash versions : 12 Kbytes, Mask versions : 10 Kbytes
- General purpose ports
  - Up to 48 ports
    (10 ports with output open-drain settings)
- 8/10-bit A/D converter
  - 8-channel RC sequential comparison type (10-bit resolution, 3.68 μs conversion time (at 25 MHz))
- I^2C interface
  - 1 channel, P76/P77 N-ch open drain pin (without P-ch)
- UART
  - 1 channel
- Extended I/O serial interface (SIO)
  - 2 channels
- 8/16-bit PPG
  - 2 channels (with 8-bit × 4 channels/16-bit × 2 channels mode switching function)
- 8/16-bit up/down timer
  - 1 channel (with 8-bit × 2 channels/16-bit × 1-channel mode switching function)
- 16-bit PWC
  - 2 channels (Capable of compare the inputs)
- 16-bit reload timer
  - 1 channel
- 16-bit I/O timer
  - 2 channels input capture, 4 channels output compare, 1 channel free run timer
- On chip dual clock generator system
- Low-power consumption (standby) mode
  - With stop mode, sleep mode, CPU intermittent operation mode, watch timer mode, timebase timer mode

- Packages
  - LQFP 64
- Process
  - CMOS technology
- Power supply voltage
  3 V, single source (some ports can be operated by 5 V power supply.)

■ PRODUCT LINEUP

Item \ Part number		MB90982	MB90F983	MB90V485B
Classification		Mask ROM product	Flash memory product	Evaluation product
ROM size		128 Kbytes	192 Kbytes	—
RAM size		10 Kbytes	12 Kbytes	16 Kbytes
CPU function		Number of instructions : 351 Instruction bit length : 8-bit, 16-bit Instruction length : 1 byte to 7 bytes Data bit length : 1-bit, 8-bits, 16-bits Minimum execution time : 40 ns (25 MHz machine clock)		
Ports		General-purpose I/O ports: up to 48 General-purpose I/O ports (CMOS output) General-purpose I/O ports (with pull-up resistance Input) General-purpose I/O ports (N-ch open drain output)		
UART		1 channel, start-stop synchronized		
8/16-bit PPG		8-bit × 4 channels/16-bit × 2 channels		8-bit × 6 channels/ 16-bit × 3 channels
8/16-bit up/down counter/timer		6 event input pins, 8-bit up/down counters : 2 8-bit reload/compare registers : 2		
16-bit I/O timers	16-bit free run timer	Number of channels : 1 Overflow interrupt		
	Output compare (OCU)	Number of channels : 4 Pin input factor : A match signal of compare register		Number of channels : 6 Pin input factor : A match signal of compare register
	Input capture (ICU)	Number of channels : 2 Rewriting a register value upon a pin input (rising, falling, or both edges)		
DTP/external interrupt circuit		Number of external interrupt channels : 8 (edge or level detection)		
Extended I/O serial interface		2 channels, embedded		
I^2C interface*2		1 channel		
PWC		2 channels		3 channels
Timebase timer		18-bit counter Interrupt cycles: 1.0 ms, 4.1 ms, 16.4 ms, 131.1 ms (at 4 MHz base oscillator)		
A/D converter		Conversion resolution : 8/10-bit, switchable One-shot conversion mode (converts selected channel 1 time only) Scan conversion mode (conversion of multiple consecutive channels, programmable up to 8 channels) Continuous conversion mode (repeated conversion of selected channels) Stop conversion mode (conversion of selected channels with repeated pause)		
Watchdog timer		Reset generation interval : 3.58 ms, 14.33 ms, 57.23 ms, 458.75 ms (minimum value, at 4 MHz base oscillator)		
Low-power consumption (standby) modes		Sleep mode, stop mode, CPU intermittent mode, watch timer mode, timebase timer mode		
Process		CMOS		
Type		Flash model 3V/5V power supply*1	Mask model 3V/5V power supply*1	3V/5V power supply*1
Emulator power supply*3		—	—	Yes

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*1 : 3V/5V I/F pin : All pins should be for 3 V power supply without P24 to P27, P30 to P37, P40 to P42, P70 to P74, P76, and P77.

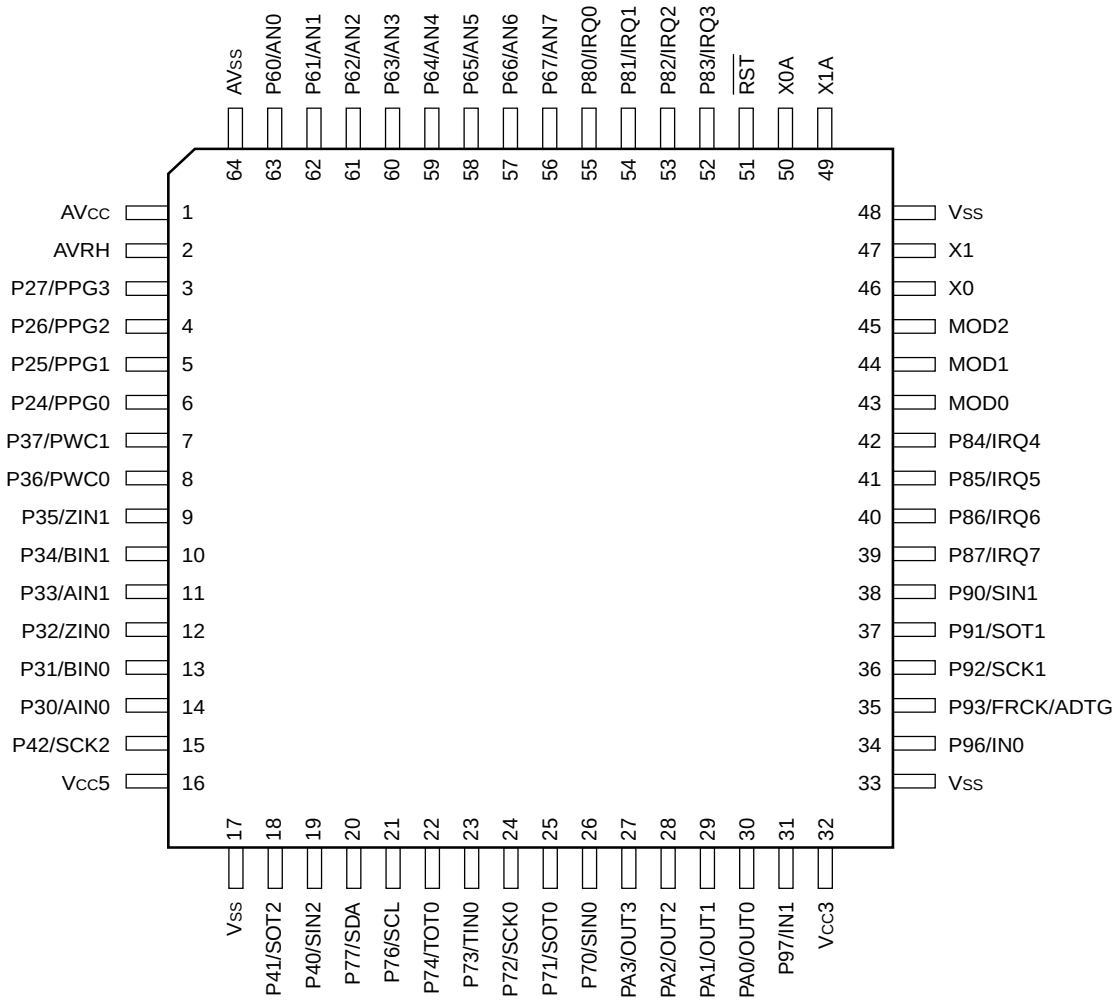
*2 : P76/P77 pins are N-ch open drain pins (without P-ch) at built-in I^2C.

*3 : It is setting of Jumper switch (TOOL VCC) when Emulator (MB2147-01) is used.
Please refer to the hardware manual of MB2147-01 or MB2147-20 (“3.3 Emulator-dedicated Power Supply Switching”) about details.

Note : Ensure that you must write to Flash at V_{CC} = 3.13 V to 3.60 V (3.3 V + 10%, −5%) .

■ PIN ASSIGNMENT

(TOP VIEW)



(FPT-64P-M03)

Notes : • I²C pin P76 and P77 are N-ch open drain pin (without P-ch) .
• P24 to P27, P30 to P37, P40 to P42, P70 to P74, P76 and P77 also used as 3 V/5 V I/F pin.

■ PIN DESCRIPTIONS

Pin No.	Pin name	I/O Circuit type*	Function
46	X0	A	Oscillator pin
47	X1	A	Oscillator pin
50	X0A	A	32 kHz oscillator pin
49	X1A	A	32 kHz oscillator pin
51	$\overline{RST}$	B	Reset input pin
3 to 6	P27 to P24	E (CMOS/H)	General purpose I/O port
	PPG3 to PPG0		PPG timer output pin
14	P30	E (CMOS/H)	General purpose I/O port
	AIN0		8/16-bit up/down timer counter input pin (ch.0)
13	P31	E (CMOS/H)	General purpose I/O port
	BIN0		8/16-bit up/down timer counter input pin (ch.0)
12	P32	E (CMOS/H)	General purpose I/O port
	ZIN0		8/16-bit up/down timer counter input pin (ch.0)
11	P33	E (CMOS/H)	General purpose I/O port
	AIN1		8/16-bit up/down timer counter input pin (ch.1)
10	P34	E (CMOS/H)	General purpose I/O port
	BIN1		8/16-bit up/down timer counter input pin (ch.1)
9	P35	E (CMOS/H)	General purpose I/O port
	ZIN1		8/16-bit up/down timer counter input pin (ch.1)
7, 8	P37, P36	E (CMOS/H)	General purpose I/O port
	PWC1, PWC0		PWC input pin
19	P40	G (CMOS/H)	General purpose I/O port
	SIN2		Simple serial I/O 2-input pin
18	P41	F (CMOS)	General purpose I/O port
	SOT2		Simple serial I/O 2-output pin
15	P42	G (CMOS/H)	General purpose I/O port
	SCK2		Simple serial I/O 2-clock I/O pin
60 to 63	P63 to P60	H (CMOS)	General purpose I/O port
	AN3 to AN0		Analog input pin
56 to 59	P67 to P64	F (CMOS)	General purpose I/O port
	AN7 to AN4		Analog input pin
26	P70	G (CMOS/H)	General purpose I/O port
	SIN0		UART data input pin
25	P71	F (CMOS)	General purpose I/O port
	SOT0		UART data output pin

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Pin No.	Pin name	I/O Circuit type*	Function
24	P72	G (CMOS/H)	General purpose I/O port
	SCK0		UART clock I/O pin
23	P73	G (CMOS/H)	General purpose I/O port
	TIN0		16-bit reload timer event input pin
22	P74	F (CMOS)	General purpose I/O port
	TOT0		16-bit reload timer output pin
21	P76	I (NMOS/H)	General purpose I/O port
	SCL		This pin functions as the I^2C interface clock I/O pin. Set port output to Hi-Z during the I^2C interface operation.
20	P77	I (NMOS/H)	General purpose I/O port
	SDA		This pin functions as the I^2C interface data I/O pin. Set port output to Hi-Z during the I^2C interface operation.
52 to 55	P83 to P80	E (CMOS/H)	General purpose I/O port
	IRQ3 to IRQ0		External interrupt input pin
39 to 42	P87 to P84	E (CMOS/H)	General purpose I/O port
	IRQ7 to IRQ4		External interrupt input pin
38	P90	E (CMOS/H)	General purpose I/O port
	SIN1		Simple serial I/O1-data input pin
37	P91	D (CMOS)	General purpose I/O port
	SOT1		Simple serial I/O-1 data output pin
36	P92	E (CMOS/H)	General purpose I/O port
	SCK1		Simple serial I/O-1 data I/O pin
35	P93	E (CMOS/H)	General purpose I/O port
	FRCK		When using free-run timer, this pin functions as the external clock input pin.
	ADTG		When using A/D converter, this pin fuctions as the external trigger input pin.
34	P96	E (CMOS/H)	General purpose I/O port
	IN0		Input capture ch.0 trigger input pin
31	P97	E (CMOS/H)	General purpose I/O port
	IN1		Input capture ch.1 trigger input pin
27 to 30	PA3 to PA0	D (CMOS)	General purpose I/O port
	OUT3 to OUT0		Output compare event output pin
1	AV_{CC}	—	A/D converter power supply pin
2	AVRH	—	A/D converter external reference power supply pin
64	AV_{SS}	—	A/D converter power supply pin
43 to 45	MD0 to MD2	J (CMOS/H)	Operating mode selection input pins
32	$V_{CC}3$	—	3.3 V ± 0.3 V power supply pins ($V_{CC}3$)

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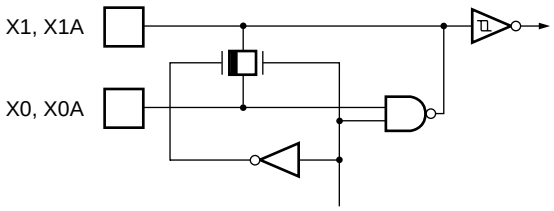
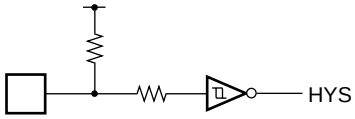
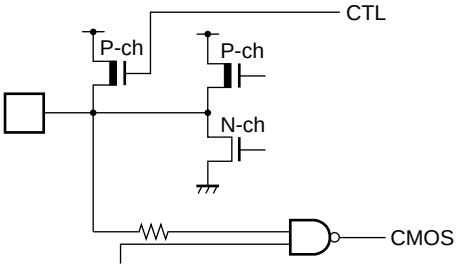
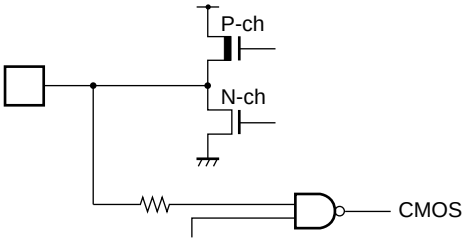
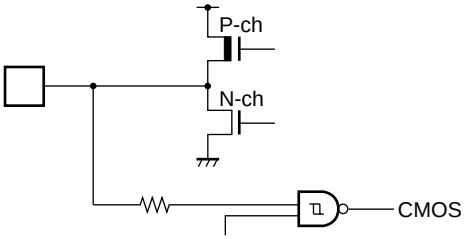
Pin No.	Pin name	I/O Circuit type*	Function
16	$V_{CC}5$	—	3 V/5 V power supply pin. 5 V power supply pin when P24 to P27, P30 to P37, P40 to P42, P70 to P74, P76 and P77 are used as 5 V I/F pins. Usually, use $V_{CC} = V_{CC}3 = V_{CC}5$ as a 3 V power supply (when the 3 V power supply is used alone) .
17, 33, 48	V_{SS}	—	Power supply input pins (GND)

*: Refer to "■ I/O CIRCUIT TYPES" for I/O circuit types.

■ I/O CIRCUIT TYPES

Type	Circuit	Remarks
A	 Hard/soft standby control signal	• Oscillator feedback resistance X1, X0 : approx. 1 MΩ X1A, X0A : approx. 10 MΩ • With standby control
B		Hysteresis input with pull-up resistance
C	 Standby control signal	• With input pull-up resistance control • CMOS level input/output
D	 Standby control signal	CMOS level input/output
E	 Standby control signal	• Hysteresis input • CMOS level output

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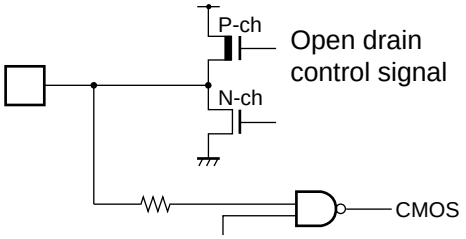
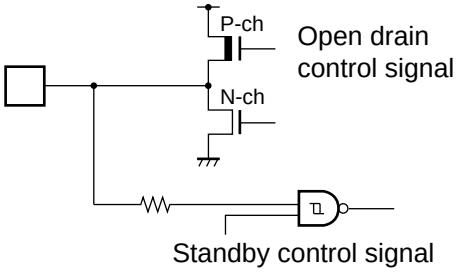
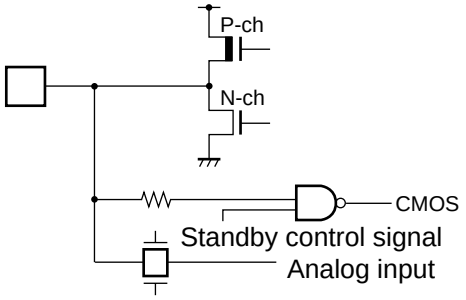
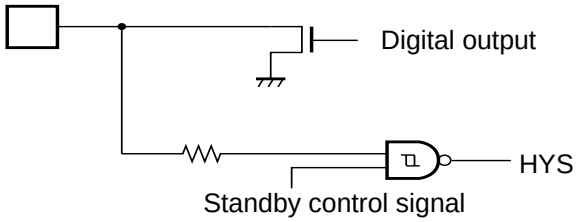
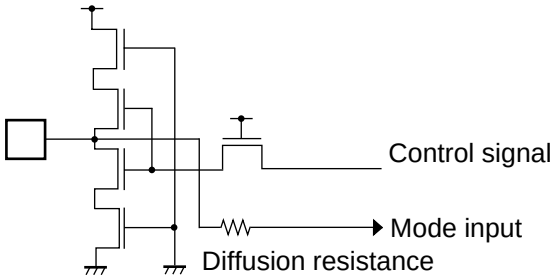
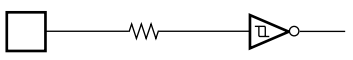
Type	Circuit	Remarks
F		• CMOS level input/output • With open drain control
G		• CMOS level output • Hysteresis input • With open drain control
H		• CMOS level input/output • Analog input
I		• Hysteresis input • N-ch open drain output
J	Flash memory model 	• CMOS level input • With high voltage control for flash testing
	Mask ROM model 	Hysteresis input

■ CAUTION OF USING DEVICES

1. Maximum rated voltages (preventing latchup)

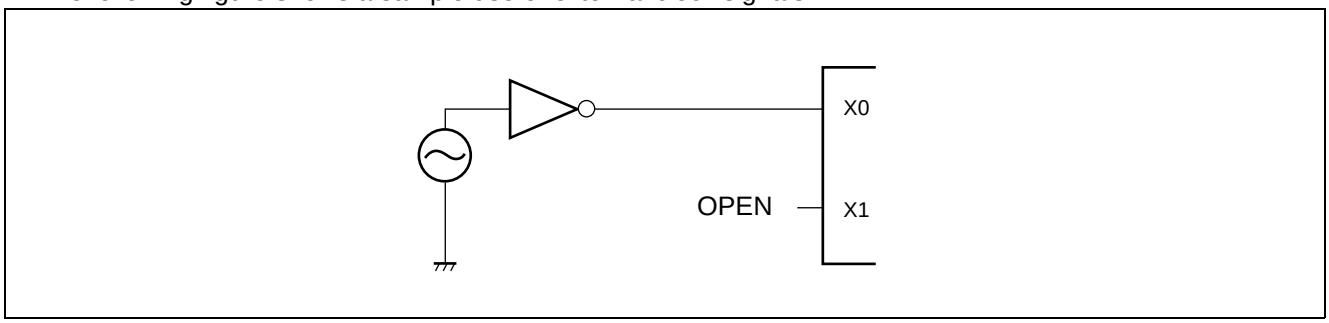
In CMOS IC devices, a condition known as latchup may occur if voltages higher than V_{CC} or lower than V_{SS} are applied to input or output pins other than medium-or high-voltage pins, or if the voltage applied between V_{CC} and V_{SS} exceeds the rated voltage level.
When latchup occurs, the power supply current increases rapidly causing the possibility of thermal damage to circuit elements. Therefore it is necessary to ensure that maximum ratings are not exceeded in circuit operation.
Similarly, when turning the analog power supply on or off, it is necessary to ensure that the analog power supply voltages (AV_{CC} and AVRH) and analog input voltages do not exceed the digital power supply (V_{CC}) .

2. Treatment of unused pins

Leaving unused input pins unconnected can cause abnormal operation or latchup, leading to permanent damage. Unused input pins should always be pulled up or down through resistance of at least 2 kΩ. Any unused input/output pins may be set to output mode and left open, or set to input mode and treated the same as unused input pins.

3. Notes on Using External Clock

Even when using an external clock signal, an oscilltion stabilization delay is applied after a power-on reset or when recovering from sub-clock or stop mode. When using an external clock, 25 MHz should be the upper frequency limit.
The following figure shows a sample use of external clock signals.



4. Treatment of Power Supply Pins (V_{CC}/V_{SS})

When multiple V_{CC} pins or V_{SS} pins are present, device design considerations for prevention of latch-up and unwanted electromagnetic interference, abnormal storobe signal operation due to ground level rise, and conformity with total output current ratings require that all power supply pins must be externally connected to power supply or ground.
Consideration should be given to connecting power supply sources to the V_{CC} pin or V_{SS} pin of this device with as low impedane as possible. It is also recommended that a bypass capacitor of approximately 0.1 µF be placed between the V_{CC} and V_{SS} lines as close to this device as possible.

5. Crystal Oscillator Circuits

Noise around the high-speed oscillation pins (X0 and X1) and low-speed oscillation pins (X0A and X1A) may cause this device to operate abnormally. Design the printed circuit board so that the crystal oscillator (or ceramic oscillator) and bypass capacitor to the ground are located as close to the high-speed oscillation pins and low-speed oscillation pins as possible. Also, design the printed circuit board to prevent the wiring from crossing another writing.
It is highly recommended to provide a printed circuit board artwork surrounding the high-speed oscillation pins and low-speed oscillation pins with a ground area for stabilizing the operation.

6. Notes on during operation of PLL clock mode

If the PLL clock mode is selected, the microcontroller attempt to be working with the self-oscillating circuit even when there is no external oscillator or external clock input is stopped. Performance of this operation, however, cannot be guaranteed.

7. Proper power-on/off sequence

The A/D converter power (AV_{CC}, AVRH) and analog input (AN0 to AN7) must be turned on after the digital power supply (V_{CC}) is turned on. The A/D converter power (AV_{CC}, AVRH) and analog input (AN0 to AN7) must be shut off before the digital power supply (V_{CC}) is shut off. Care should be taken that AVRH does not exceed AV_{CC}. Even when pins used as analog input pins are doubled as input ports, be sure that the input voltage does not exceed AV_{CC}.

8. Treatment of power supply pins on models with A/D converters

Even when the A/D converters are not in use, be sure to make the necessary connections AV_{CC} = AVRH = V_{CC}, and AV_{SS} = V_{SS}.

9. Precautions when turning the power supply on

In order to prevent abnormal operation in the chip's internal step-down circuits, a voltage rise time during power-on of 50 µs (0.2 V to 2.7 V) or greater should be assured.

10. Supply Voltage Stabilization

Even within the operating range of V_{CC} supply voltage, rapid voltage fluctuations may cause abnormal operation. As a standard for power supply voltage stability, it is recommended that the peak-to-peak V_{CC} ripple voltage at commercial supply frequency (50 Hz/60 Hz) be 10 % or less of V_{CC}, and that the transient voltage fluctuation be no more than 0.1 V/ms or less when the power supply is turned on or off.

11. Notes on Using Power Supply

Only the MB90980 series usually uses a 3 V power supply. By setting $V_{CC}3$ = 3 V power supply and $V_{CC}5$ = 5 V power supply, P24 to P27, P30 to P37, P40 to P42 and P70 to P74, P76, P77 can be intefaced as 5 V power supplies separately from the main 3 V power supply. Note that the analog power supplies (such as AV_{CC} and AV_{SS}) for the A/D converter can be used only as 3 V power supplies.

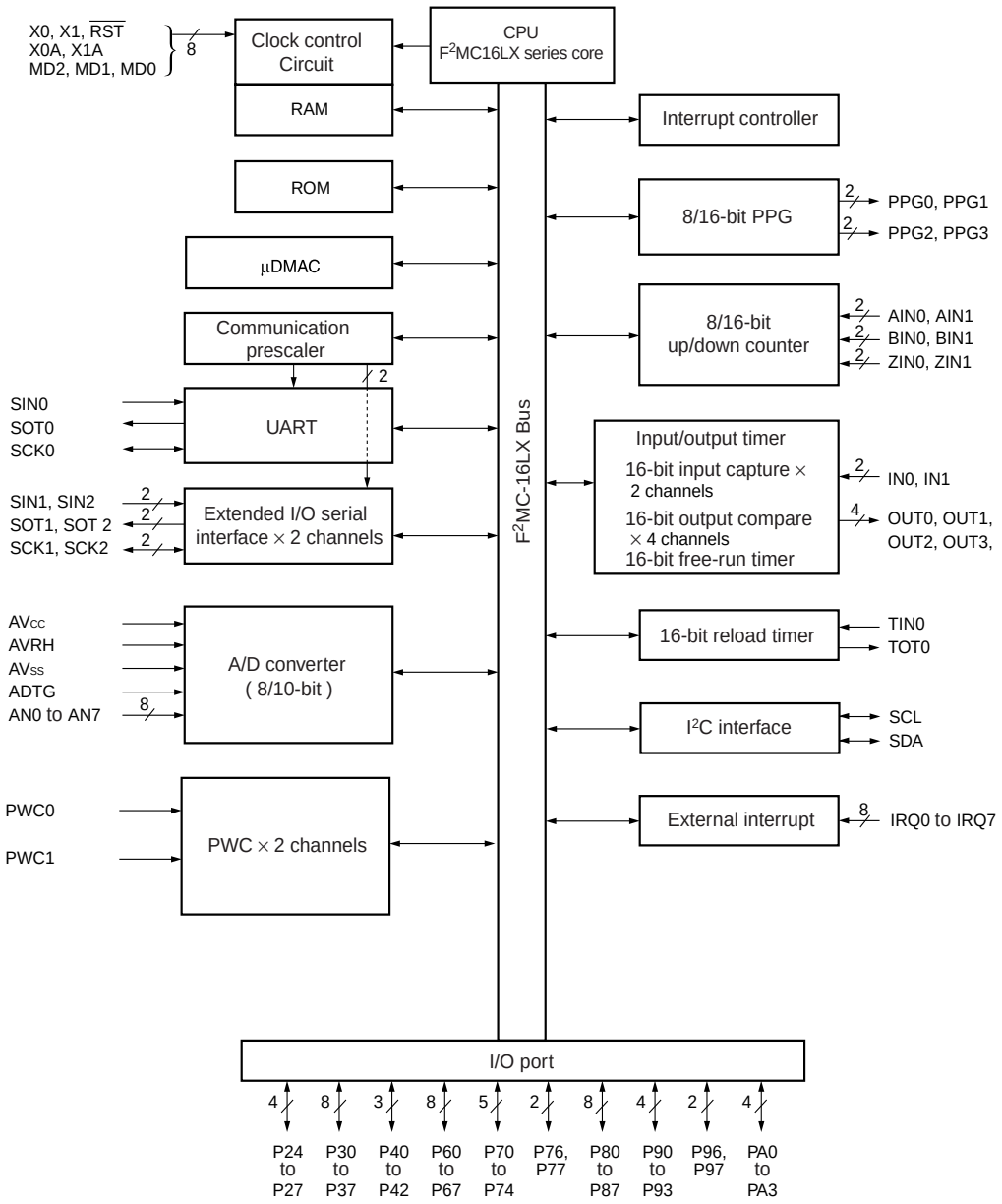
12. Treatment of NC pins

NC (internally connected) pins should always be left open.

13. Writing to Flash memory

For serial writing to Flash memory, always ensure that the operating voltage V_{CC} is between 3.13 V and 3.6 V. For normal writing to Flash memory, always ensure that the operating voltage V_{CC} is between 3.0 V and 3.6 V.

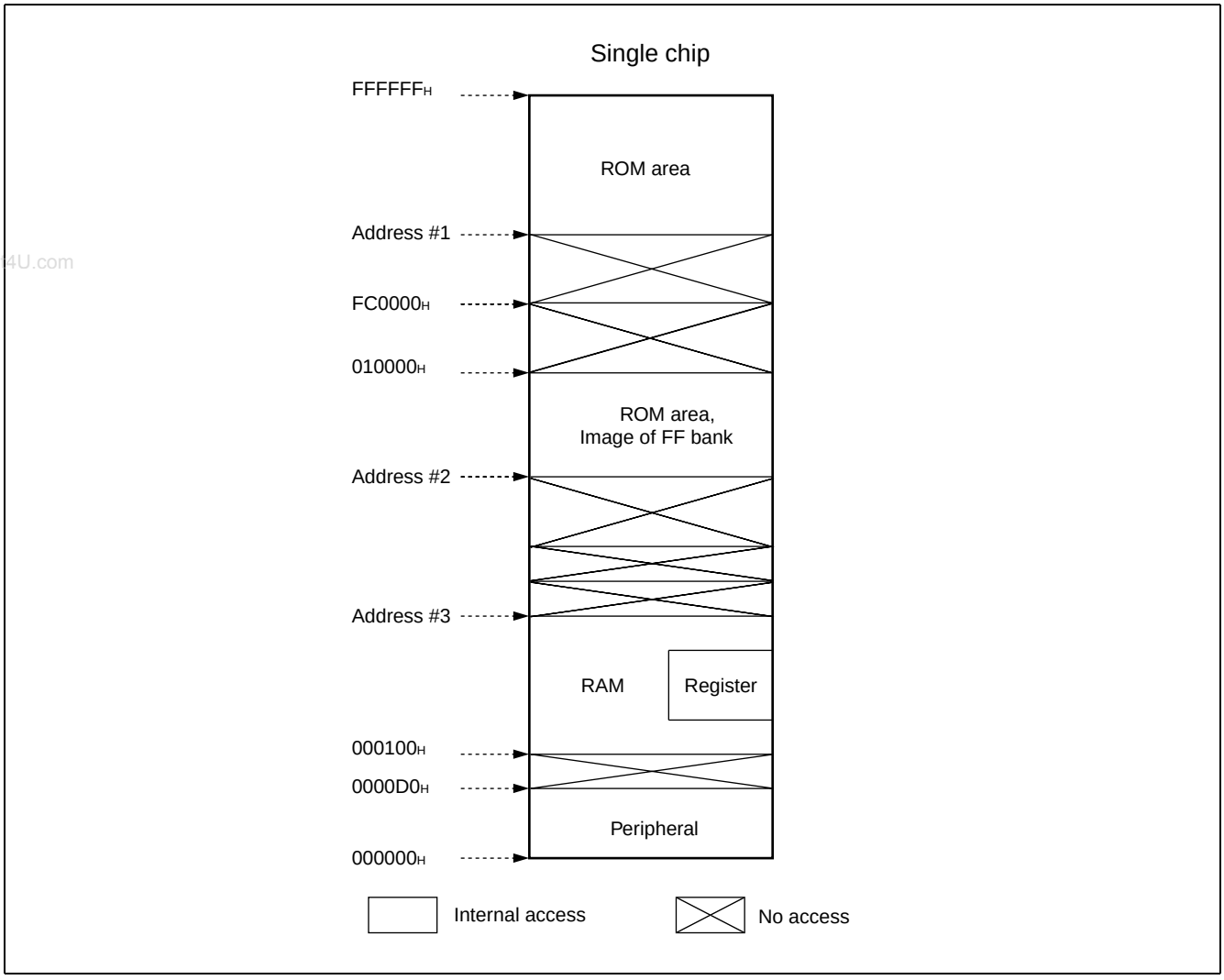
■ BLOCK DIAGRAM



P40 to P42 (× 3) : with an open drain setting register
I²C pin P77 and P76 are N-ch open drain pin (without P-ch) .

Note : In the above diagram, I/O ports share internal function blocks and pins. However, when a set of pins is used with an internal module, it cannot also be used as an I/O port.

■ MEMORY MAP



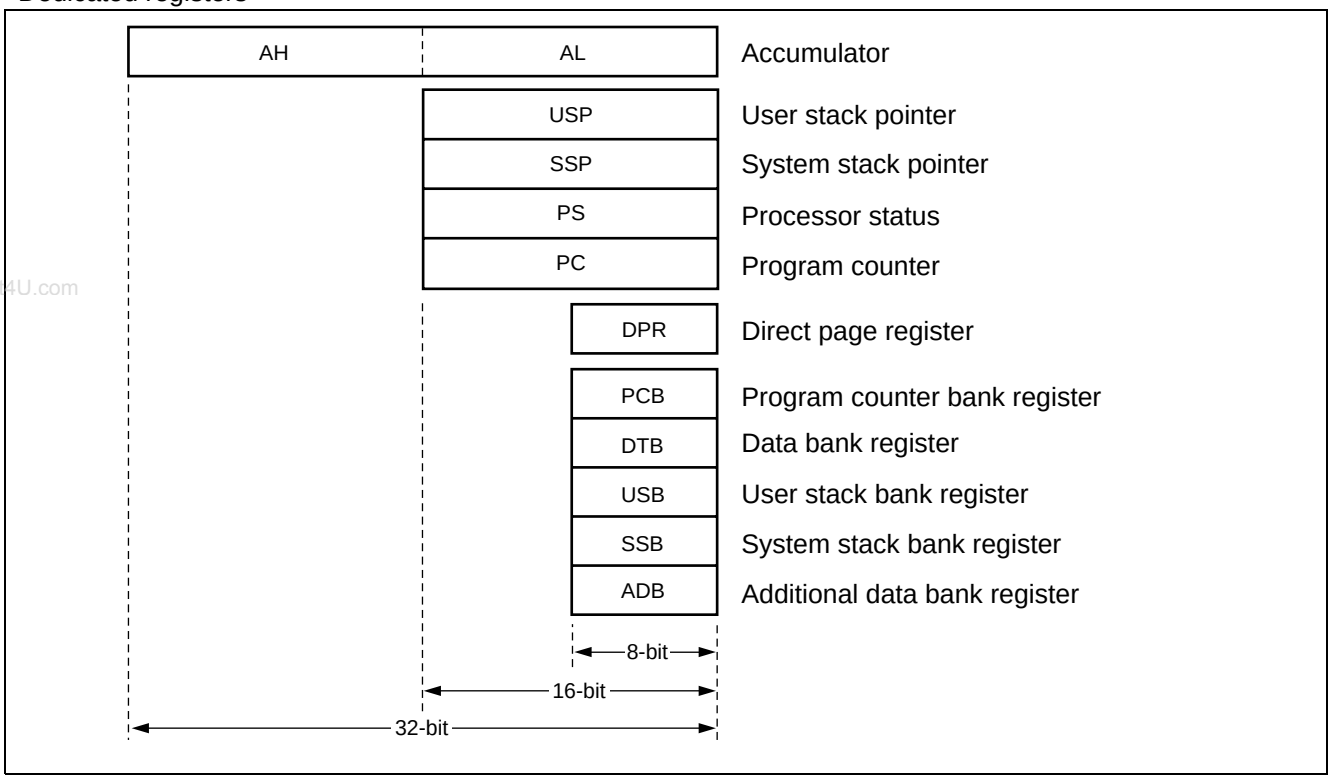
Model	Address #1	Address #2	Address #3
MB90F983	FC0000H *1	004000H or 008000H, selected by the MS bit in the ROMM register	003100H
MB90982	FD0000H*2		002900H

*1 : No memory cells from FC0000H to FC7FFFH and FE0000H to FE7FFFH.

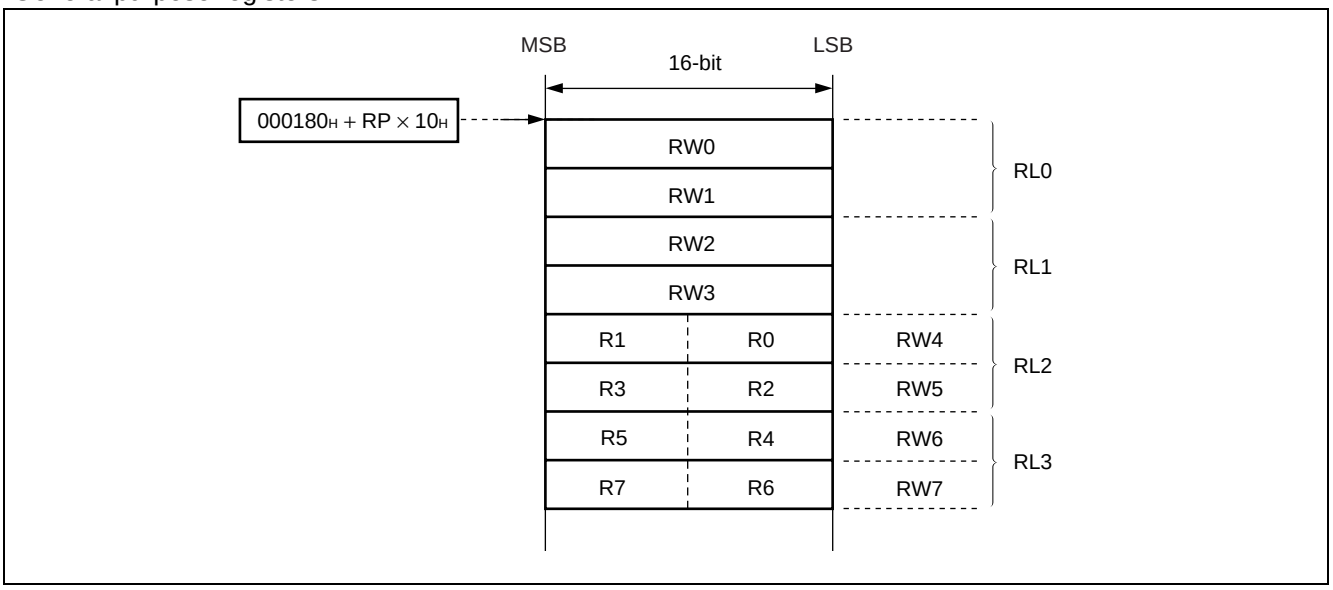
*2 : No memory cells from FE0000H to FEFFFFH. The upper part of the 00 bank is set up to mirror the image of FF bank ROM, to enable efficient use of small model C compilers. Because the lower 16-bit address of the FF bank and the lower 16-bit address of the 00 bank is the same, enabling reference to tables in ROM without the “far” pointer declaration.
For example, in accessing address 00C000H it is actually the contents of ROM at FFC000H that are accessed. If the MS bit in the ROMM register is set to “0”, the ROM area in the FF bank will exceed 48 Kbytes and it is not possible to reflect the entire area in the image in the 00 bank. Therefore the image from FF4000H to FFFFFFH is reflected in the 00 bank and the area from FF0000H to FF3FFFH can be seen in the FF bank only.

■ F²MC-16LX CPU PROGRAMMING MODEL

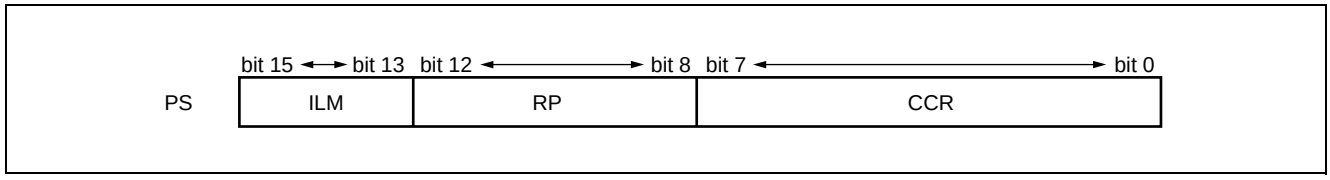
•Dedicated registers



•General purpose registers



•Processor status



■ I/O MAP

Address	Abbreviated register name	Register name	R/W	Resource name	Initial value
000000H, 000001H	Reserved area				
000002H	PDR2	Port 2 data register	R/W	Port 2	XXXXXXXXB
000003H	PDR3	Port 3 data register	R/W	Port 3	XXXXXXXXB
000004H	PDR4	Port 4 data register	R/W	Port 4	XXXXXXXXB
000005H	Reserved area				
000006H	PDR6	Port 6 data register	R/W	Port 6	XXXXXXXXB
000007H	PDR7	Port 7 data register	R/W	Port 7	11XXXXXXB
000008H	PDR8	Port 8 data register	R/W	Port 8	XXXXXXXXB
000009H	PDR9	Port 9 data register	R/W	Port 9	XXXXXXXXB
00000AH	PDRA	Port A data register	R/W	Port A	- - - - XXXXB
00000BH	UDER	Up/down timer input enable register	R/W	Up/down timer input control	XX 0 0 0 0 0 0B
00000CH	ENIR	Interrupt/DTP enable register	R/W	DTP/external interrupts	0 0 0 0 0 0 0 0B
00000DH	EIRR	Interrupt/DTP source register	R/W		XXXXXXXXB
00000EH	ELVR	Request level setting register	R/W		0 0 0 0 0 0 0 0B
00000FH		Request level setting register	R/W		0 0 0 0 0 0 0 0B
000010H, 000011H	Reserved area				
000012H	DDR2	Port 2 direction register	R/W	Port 2	0 0 0 0 XXXXB
000013H	DDR3	Port 3 direction register	R/W	Port 3	0 0 0 0 0 0 0 0B
000014H	DDR4	Port 4 direction register	R/W	Port 4	0 0 0 0 0 0 0 0B
000015H	Reserved area				
000016H	DDR6	Port 6 direction register	R/W	Port 6	0 0 0 0 0 0 0 0B
000017H	DDR7	Port 7 direction register	R/W	Port 7	XX 0 0 0 0 0 0B
000018H	DDR8	Port 8 direction register	R/W	Port 8	0 0 0 0 0 0 0 0B
000019H	DDR9	Port 9 direction register	R/W	Port 9	0 0 XX 0 0 0 0B
00001AH	DDRA	Port A direction register	R/W	Port A	- - - - 0 0 0 0B
00001BH	ODR4	Port 4 output pin register	R/W	Port 4 (Open-drain control)	XXXXX 0 0 0B
00001CH, 00001DH	Reserved area				
00001EH	ODR7	Port 7 output pin register	R/W	Port 7 (Open-drain control)	XXX 0 0 0 0 0 0B
00001FH	ADER	Analog input enable register	R/W	Port 6, A/D	1 1 1 1 1 1 1 1B
000020H	SMR	Serial mode register	R/W	UART	0 0 0 0 0 X 0 0B
000021H	SCR	Serial control register	W, R/W		0 0 0 0 0 1 0 0B
000022H	SIDR/SODR	Serial input/output register	R/W		XXXXXXXXB
000023H	SSR	Serial status register	R, R/W		0 0 0 0 1 0 0 0B
000024H	Reserved area				
000025H	CDCR	Communication prescaler control register	R/W	Communication prescaler (UART)	0 0 - - 0 0 0 0B

(Continued)

Address	Abbreviated register name	Register name	R/W	Resource name	Initial value
000026H	SMCS0	Serial mode control status register 0	R, R/W	SIO1 (ch.0)	- - - - 0 0 0 0B
000027H	SMCS0	Serial mode control status register 0	R, R/W		0 0 0 0 0 0 1 0B
000028H	SDR0	Serial data register 0	R/W		XXXXXXXXB
000029H	SDCR0	Communication prescaler control register 0	R/W	Communication prescaler SIO1 (ch.0)	0 - - - 0 0 0 0B
00002AH	SMCS1	Serial mode control status register 1	R, R/W	SIO2 (ch.1)	- - - - 0 0 0 0B
00002BH	SMCS1	Serial mode control status register 1	R, R/W		0 0 0 0 0 0 1 0B
00002CH	SDR1	Serial data register 1	R/W		XXXXXXXXB
00002DH	SDCR1	Communication prescaler control register 1	R/W	Communication prescaler SIO2 (ch.1)	0 - - - 0 0 0 0B
00002EH	PRLL0	Reload register L (ch.0)	R/W	8/16-bit PPG (ch.0 to ch.3)	XXXXXXXXB
00002FH	PRLH0	Reload register H (ch.0)	R/W		XXXXXXXXB
000030H	PRLL1	Reload register L (ch.1)	R/W		XXXXXXXXB
000031H	PRLH1	Reload register H (ch.1)	R/W		XXXXXXXXB
000032H	PRLL2	Reload register L (ch.2)	R/W		XXXXXXXXB
000033H	PRLH2	Reload register H (ch.2)	R/W		XXXXXXXXB
000034H	PRLL3	Reload register L (ch.3)	R/W		XXXXXXXXB
000035H	PRLH3	Reload register H (ch.3)	R/W		XXXXXXXXB
000036H to 000039H	Reserved area				
00003AH	PPGC0	PPG0 operating mode control register	R/W	8/16-bit PPG (ch.0 to ch.3)	0 X 0 0 0XX 1B
00003BH	PPGC1	PPG1 operating mode control register	R/W		0 X 0 0 0 0 0 1B
00003CH	PPGC2	PPG2 operating mode control register	R/W		0 X 0 0 0XX 1B
00003DH	PPGC3	PPG3 operating mode control register	R/W		0 X 0 0 0 0 0 1B
00003EH, 00003FH	Reserved area				
000040H	PPG01	PPG0, PPG1 output control register	R/W	8/16-bit PPG	0 0 0 0 0 0 0 0B
000041H	Reserved area				
000042H	PPG23	PPG2, PPG3 output control register	R/W	8/16-bit PPG	0 0 0 0 0 0 0 0B
000043H to 000045H	Reserved area				
000046H	ADCS1	Control status register	R/W	8/10-bit A/D converter	0 0 0 0 0 0 0 0B
000047H	ADCS2		W, R/W		0 0 0 0 0 0 0 0B
000048H	ADCR1	Data register	R		XXXXXXXXB
000049H	ADCR2		W, R		0 0 0 0 0 XXXB

(Continued)

Address	Abbreviated register name	Register name	R/W	Resource name	Initial value
00004A$_H$	OCCP0	Output compare register (ch.0) lower digits	R/W	16-bit I/O timer output compare (ch.0 to ch.3)	0 0 0 0 0 0 0 0$_B$
00004B$_H$		Output compare register (ch.0) upper digits			0 0 0 0 0 0 0 0$_B$
00004C$_H$	OCCP1	Output compare register (ch.1) lower digits	R/W		0 0 0 0 0 0 0 0$_B$
00004D$_H$		Output compare register (ch.1) upper digits			0 0 0 0 0 0 0 0$_B$
00004E$_H$	OCCP2	Output compare register (ch.2) lower digits	R/W		0 0 0 0 0 0 0 0$_B$
00004F$_H$		Output compare register (ch.2) upper digits			0 0 0 0 0 0 0 0$_B$
000050$_H$	OCCP3	Output compare register (ch.3) lower digits	R/W		0 0 0 0 0 0 0 0$_B$
000051$_H$		Output compare register (ch.3) upper digits			0 0 0 0 0 0 0 0$_B$
000052$_H$ to 000055$_H$	Reserved area				
000056$_H$	OCS01	Output compare control register (ch.0, ch.1) lower digits	R/W	16-bit I/O timer output compare (ch.0 to ch.3)	0 0 0 0 - - 0 0$_B$
000057$_H$		Output compare control register (ch.0, ch.1) upper digits	R/W		- - - 0 0 0 0 0$_B$
000058$_H$	OCS23	Output compare control register (ch.2, ch.3) lower digits	R/W		0 0 0 0 - - 0 0$_B$
000059$_H$		Output compare control register (ch.2, ch.3) upper digits	R/W		- - - 0 0 0 0 0$_B$
00005A$_H$, 00005B$_H$	Reserved area				
00005C$_H$	IPCP0	Input capture data register (ch.0) lower digits	R	16-bit I/O timer input capture (ch.0, ch.1)	XXXXXXXX$_B$
00005D$_H$		Input capture data register (ch.0) upper digits	R		XXXXXXXX$_B$
00005E$_H$	IPCP1	Input capture data register (ch.1) lower digits	R		XXXXXXXX$_B$
00005F$_H$		Input capture data register (ch.1) upper digits	R		XXXXXXXX$_B$
000060$_H$	ICS01	Input capture control status register	R/W		0 0 0 0 0 0 0 0$_B$
000061$_H$	Reserved area				
000062$_H$	TCDT	Timer counter data register lower digits	R/W	16-bit I/O timer free-run timer	0 0 0 0 0 0 0 0$_B$
000063$_H$	TCDT	Timer counter data register upper digits	R/W		0 0 0 0 0 0 0 0$_B$
000064$_H$	TCCS	Timer counter control status register	R/W		0 0 0 0 0 0 0 0$_B$
000065$_H$	TCCS	Timer counter control status register	R/W		0 - - 0 0 0 0 0$_B$
000066$_H$	CPCLR	Compare clear register lower digits	R/W		XXXXXXXX$_B$
000067$_H$		Compare clear register upper digits			XXXXXXXX$_B$
000068$_H$	UDCR0	Up/down count register (ch.0)	R	8/16-bit up/ down counter/ timer	0 0 0 0 0 0 0 0$_B$
000069$_H$	UDCR1	Up/down count register (ch.1)	R		0 0 0 0 0 0 0 0$_B$
00006A$_H$	RCR0	Reload/compare register (ch.0)	W		0 0 0 0 0 0 0 0$_B$
00006B$_H$	RCR1	Reload/compare register (ch.1)	W		0 0 0 0 0 0 0 0$_B$
00006C$_H$	CCRL0	Counter control register (ch.0) lower digits	W, R/W		0 X 0 0 X 0 0 0$_B$
00006D$_H$	CCRH0	Counter control register (ch.0) upper digits	R/W		0 0 0 0 0 0 0 0$_B$

(Continued)

Address	Abbreviated register name	Register name	R/W	Resource name	Initial value
00006E$_H$	Reserved area				
00006F$_H$	ROMM	ROM mirror function select register	R/W	ROM mirroring function	- - - - - - 0 1$_B$
000070$_H$	CCRL1	Counter control register (ch.1) lower digits	R/W	8/16-bit up/down counter/timer	0 X 0 0 X 0 0 0$_B$
000071$_H$	CCRH1	Counter control register (ch.1) upper digits	R/W		- 0 0 0 0 0 0 0$_B$
000072$_H$	CSR0	Counter status register (ch.0)	R/W		0 0 0 0 0 0 0 0$_B$
000073$_H$	Reserved area				
000074$_H$	CSR1	Counter status register (ch.1)	R, R/W	8/16-bit UDC	0 0 0 0 0 0 0 0$_B$
000075$_H$	Reserved area				
000076$_H$	PWCSR0	PWC control/status register	R, R/W	PWC timer (ch.0)	0 0 0 0 0 0 0 0$_B$
000077$_H$					0 0 0 0 0 0 0 X$_B$
000078$_H$	PWCR0	PWC data buffer register	R/W		0 0 0 0 0 0 0 0$_B$
000079$_H$					0 0 0 0 0 0 0 0$_B$
00007A$_H$	PWCSR1	PWC control/status register	R, R/W	PWC timer (ch. 1)	0 0 0 0 0 0 0 0$_B$
00007B$_H$					0 0 0 0 0 0 0 X$_B$
00007C$_H$	PWCR1	PWC data buffer register	R/W		0 0 0 0 0 0 0 0$_B$
00007D$_H$					0 0 0 0 0 0 0 0$_B$
00007E$_H$ to 000081$_H$	Reserved area				
000082$_H$	DIVR0	Dividing ratio control register	R/W	PWC (ch.0)	- - - - - - 0 0$_B$
000083$_H$	Reserved area				
000084$_H$	DIVR1	Dividing ratio control register	R/W	PWC (ch.1)	- - - - - - 0 0$_B$
000085$_H$ to 000087$_H$	Reserved area				
000088$_H$	IBSR	Bus status register	R	I^2C	0 0 0 0 0 0 0 0$_B$
000089$_H$	IBCR	Bus control register	R/W		0 0 0 0 0 0 0 0$_B$
00008A$_H$	ICCR	Clock control register	R/W		- - 0 X X X X X$_B$
00008B$_H$	IADR	Address register	R/W		- X X X X X X X$_B$
00008C$_H$	IDAR	Data register	R/W		XXXXXXXX$_B$
00008D$_H$, 00008E$_H$	Reserved area				
00008F$_H$ to 00009B$_H$	Disabled				
00009C$_H$	DSRL	µDMAC status register	R/W	µDMAC	0 0 0 0 0 0 0 0$_B$
00009D$_H$	DSRH	µDMAC status register	R/W	µDMAC	0 0 0 0 0 0 0 0$_B$
00009E$_H$	PACSR	Program address detection control status resister	R/W	Address match detection function	0 0 0 0 0 0 0 0$_B$
00009F$_H$	DIRR	Dilayed interrupt source generator/ cancel register	R/W	Delayed interruput generator module	- - - - - - - 0$_B$

(Continued)

Address	Abbreviated register name	Register name	R/W	Resource name	Initial value
0000A0H	LPMCR	Low-power consumption mode control register	W, R/W	Low-power operation	0 0 0 1 1 0 0 0B
0000A1H	CKSCR	Clock select register	R, R/W	Low-power operation	1 1 1 1 1 1 0 0B
0000A2H to 0000A7H	Reserved area				
0000A8H	WDTC	Watchdog timer control register	R, W	Watchdog timer	XXXXX 1 1 1B
0000A9H	TBTC	Timebase timer control register	W, R/W	Timebase timer	1 X X 0 0 1 0 0B
0000AAH	WTC	Watch timer control register	R, R/W	Watch timer	1 0 0 0 1 0 0 0B
0000ABH	Reserved area				
0000ACH	DERL	µDMAC enable register	R/W	µDMAC	0 0 0 0 0 0 0 0B
0000ADH	DERH	µDMAC enable register	R/W	µDMAC	0 0 0 0 0 0 0 0B
0000AEH	FMCS	Flash memory control status register	W, R/W	Flash memory I/F	0 0 0 X 0 0 0 0B
0000AFH	Disabled				
0000B0H	ICR00	Interrupt control register 00	W, R/W	Interrupt controller	0 0 0 0 0 1 1 1B
0000B1H	ICR01	Interrupt control register 01	W, R/W		0 0 0 0 0 1 1 1B
0000B2H	ICR02	Interrupt control register 02	W, R/W		0 0 0 0 0 1 1 1B
0000B3H	ICR03	Interrupt control register 03	W, R/W		0 0 0 0 0 1 1 1B
0000B4H	ICR04	Interrupt control register 04	W, R/W		0 0 0 0 0 1 1 1B
0000B5H	ICR05	Interrupt control register 05	W, R/W		0 0 0 0 0 1 1 1B
0000B6H	ICR06	Interrupt control register 06	W, R/W		0 0 0 0 0 1 1 1B
0000B7H	ICR07	interrupt control register 07	W, R/W		0 0 0 0 0 1 1 1B
0000B8H	ICR08	Interrupt control register 08	W, R/W		0 0 0 0 0 1 1 1B
0000B9H	ICR09	Interrupt control register 09	W, R/W		0 0 0 0 0 1 1 1B
0000BAH	ICR10	Interrupt control register 10	W, R/W		0 0 0 0 0 1 1 1B
0000BBH	ICR11	Interrupt control register 11	W, R/W		0 0 0 0 0 1 1 1B
0000BCH	ICR12	Interrupt control register 12	W, R/W		0 0 0 0 0 1 1 1B
0000BDH	ICR13	Interrupt control register 13	W, R/W		0 0 0 0 0 1 1 1B
0000BEH	ICR14	Interrupt control register 14	W, R/W		0 0 0 0 0 1 1 1B
0000BFH	ICR15	Interrupt control register 15	W, R/W		0 0 0 0 0 1 1 1B
0000C0H to 0000C9H	Reserved area				
0000CAH	TMCSR	Timer control status register	R/W	16-bit reload timer	0 0 0 0 0 0 0 0B
0000CBH					- - - - 0 0 0 0B
0000CCH	TMR/TMRLR	16-bit timer register/ 16-bit reload register	R/W		XXXXXXXXB
0000CDH					
0000CEH	Reserved area				

(Continued)

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Address	Abbreviated register name	Register name	R/W	Resource name	Initial value
0000CF$_H$	PLLOS	PLL output select register	W	Low-power operation	- - - - - - 0 0$_B$
0000D0$_H$ to 0000FF$_H$	External area				
000100$_H$ to 00000#$_H$	RAM area				
001FF0$_H$	PADR0	Program address detection resister 0 (Low order address)	R/W	Address match detection function	XXXXXXXX$_B$
001FF1$_H$		Program address detection resister 0 (Middle order address)			
001FF2$_H$		Program address detection resister 0 (High order address)			
001FF3$_H$	PADR1	Program address detection resister 1 (Low order address)	R/W	Address match detection function	XXXXXXXX$_B$
001FF4$_H$		Program address detection resister 1 (Middle order address)			
001FF5$_H$		Program address detection resister 1 (High order address)			

Notes : • Descriptions for R/W
R/W : Enabled to read and write
R : Read only
W : Write only

• Descriptions for initial value
0 : The initila value of this bit is “0”.
1 : The initial value of this bit is “1”.
X : The initial value of this bit is undefined.
- : This bit is not used.

■ INTERRUPT SOURCES, INTERRUPT VECTORS, AND INTERRUPT CONTROL REGISTERS

Interrupt source	Clear of EI²OS	μDMAC cnannel number	Interrupt vector		Interrupt control register	
			Number	Address	Number	Address
Reset	×	—	#08	FFFFDC$_H$	—	—
INT9 instruction	×	—	#09	FFFFD8$_H$	—	—
Exception	×	—	#10	FFFFD4$_H$	—	—
INT0 (IRQ0)	○	0	#11	FFFFD0$_H$	ICR00	0000B0$_H$
INT1 (IRQ1)	○	×	#12	FFFFCC$_H$		
INT2 (IRQ2)	○	×	#13	FFFFC8$_H$	ICR01	0000B1$_H$
INT3 (IRQ3)	○	×	#14	FFFFC4$_H$		
INT4 (IRQ4)	○	×	#15	FFFFC0$_H$	ICR02	0000B2$_H$
INT5 (IRQ5)	○	×	#16	FFFFBC$_H$		
INT6 (IRQ6)	○	×	#17	FFFFB8$_H$	ICR03	0000B3$_H$
INT7 (IRQ7)	○	×	#18	FFFFB4$_H$		
PWC1	○	×	#19	FFFFB0$_H$	ICR04	0000B4$_H$
—	—	—	#20	FFFFAC$_H$		
PWC0	○	1	#21	FFFFA8$_H$	ICR05	0000B5$_H$
PPG0/PPG1 counter borrow	×	2	#22	FFFFA4$_H$		
PPG2/PPG3 counter borrow	×	3	#23	FFFFA0$_H$	ICR06	0000B6$_H$
—	—	—	#24	FFFF9C$_H$		
8/16-bit up/down counter/ timer (ch.0, ch.1) compare/ underflow/overflow/inversion	○	×	#25	FFFF98$_H$	ICR07	0000B7$_H$
Input capture (ch.0) load	○	5	#26	FFFF94$_H$		
Input capture (ch.1) load	○	6	#27	FFFF90$_H$	ICR08	0000B8$_H$
Output compare (ch.0) match	○	8	#28	FFFF8C$_H$		
Output compare (ch.1) match	○	9	#29	FFFF88$_H$	ICR09	0000B9$_H$
Output compare (ch.2) match	○	10	#30	FFFF84$_H$		
Output compare (ch.3) match	○	×	#31	FFFF80$_H$	ICR10	0000BA$_H$
—	—	—	#32	FFFF7C$_H$		
—	—	—	#33	FFFF78$_H$	ICR11	0000BB$_H$
UART sending completed	○	11	#34	FFFF74$_H$		
16-bit free run timer overflow, 16-bit reload timer underflow*2	○	12	#35	FFFF70$_H$	ICR12	0000BC$_H$
UART receiving compleated	◎	7	#36	FFFF6C$_H$		
SIO1 (ch.0)	○	13	#37	FFFF68$_H$	ICR13	0000BD$_H$
SIO2 (ch.1)	○	14	#38	FFFF64$_H$		

(Continued)

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Interrupt source	Clear of EI²OS	µDMAC channel number	Interrupt vector		Interrupt control register	
			Number	Address	Number	Address
I²C interface	×	×	#39	FFFF60H	ICR14	0000BEH
8/10-bit A/D converter	○	15	#40	FFFF5CH		
Flash write/erase, timebase timer,watch timer *1	×	×	#41	FFFF58H	ICR15	0000BFH
Delay interrupt generator module	×	×	#42	FFFF54H		

× : Interrupt request flag is not cleared by the interrupt clear signal.
○ : Interrupt request flag is cleared by the interrupt clear signal.
◎ : Interrupt request flag is cleared by the interrupt clear signal (stop request present) .

*1 : Caution : The Flash write/erase, timebase timer, and watch timer cannot be used at the same time.

*2 : When the 16-bit reload timer underflow interrupt is changed from enable (TMCSR : INTE = 1) to disable (TMCSR : INTE = 0) , disable the interrupt in the interrupt control register (ICR12 : IL2 to IL0 : 111B) , then set the INTE bit to 0.

Note : If there are two interrupt sources for the same interrupt number, the interrupt request flags of both resources are cleared by the EI²OS/µDMAC. Therefore if either of the two sources uses the EI²OS/µDMAC function, the other interrupt function cannot be used. The interrupt request enable bit for the resource that does not use the EI²OS/µDMAC function should be set to “0” and the interrupt function should be handled by software polling.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	$V_{CC}3$	V_{SS} – 0.3	V_{SS} + 4.0	V	
	$V_{CC}5$	V_{SS} – 0.3	V_{SS} + 7.0	V	
	AV_{CC}	V_{SS} – 0.3	V_{SS} + 4.0	V	*2
	AVRH	V_{SS} – 0.3	V_{SS} + 4.0	V	
Input voltage*1	V_I	V_{SS} – 0.3	V_{SS} + 4.0	V	*3
		V_{SS} – 0.3	V_{SS} + 7.0	V	*3, *8, *9
Output volatage*1	V_O	V_{SS} – 0.3	V_{SS} + 4.0	V	*3
		V_{SS} – 0.3	V_{SS} + 7.0	V	*3, *8, *9
Maximum clamp current	I_{CLAMP}	–2.0	+2.0	mA	*7
Total maximum clamp current	$\Sigma \lvert I_{CLAMP} \rvert$	—	20	mA	*7
“L” level maximum output current	I_{OL}	—	10	mA	*4
“L” level average output current	I_{OLAV}	—	3	mA	*5
“L” level maximum total output current	ΣI_{OL}	—	60	mA	
“L” level total average output current	ΣI_{OLAV}	—	30	mA	*6
“H” level maximum output current	I_{OH}	—	–10	mA	*4
“H” level average output current	I_{OHAV}	—	–3	mA	*5
“H” level maximum total output current	ΣI_{OH}	—	–60	mA	
“H” level total average output current	ΣI_{OHAV}	—	–30	mA	*6
Power consumption	P_D	—	320	mW	
Operating temperature	T_A	–40	+85	°C	
Storage temperature	Tstg	–55	+150	°C	

*1 : This parameter is based on $V_{SS} = AV_{SS} = 0.0$ V.

*2 : AV_{CC} and AVRH must not exceed V_{CC}. Also, AVRH must not exceed AV_{CC}.

*3 : V_I and V_O must not exceed V_{CC} + 0.3 V. However, if the maximum current to/from input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating.

*4 : Maximum output current is defined as the peak value for one of the corresponding pins.

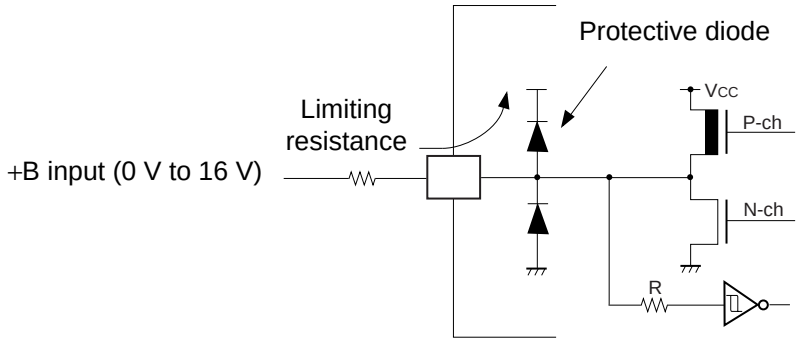
*5 : Average output current is defined as the average current flow in a 100 ms interval at one of the corresponding pins.

*6 : Average total output current is defined as the average current flow in a 100 ms interval at all corresponding pins.

*7 : • Applicable to pins : P24 to P27, P30 to P37, P40 to P42, P60 to P67, P70 to P74, P76, P77, P80 to P87, P90 to P93, P96, P97, PA0 to PA3
- Use within recommended operating conditions.
- Use at DC voltage (current) .
- The +B signal should always be applied with a limiting resistance placed between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.

- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller current is off (not fixed at 0 V) , the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on reset.
- Care must be taken not to leave the +B input pin open.
- Note that analog system input/output pins other than the A/D input pins (LCD drive pins, comparator input pins, etc.) cannot accept +B signal input.
- Sample recommended circuits:

- Input/Output Equivalent circuits



*8 : P24 to P27, P30 to P37, P40 to P42, P70 to P74, P76, P77 pins can be used as 5 V I/F pin on applied 5 V to $V_{CC}5$ pin.
P76 and P77 is N-ch open drain pin.

*9 : As for P76 and P77 (N-ch open drain pin) , even if using at 3 V simplicity ($V_{CC}3 = V_{CC}5$) , the ratings are applied.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

(V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Supply voltage	$V_{CC}3$	2.7	3.6	V	During normal operation
		1.8	3.6	V	To maintain RAM state in stop mode
	$V_{CC}5$	2.7	5.5	V	During normal operation*
		1.8	5.5	V	To maintain RAM state in stop mode*
"H" level input voltage	V_{IH}	0.7 V_{CC}	V_{CC} + 0.3	V	All pins other than V_{IH2}, V_{IHS}, V_{IHM} and V_{IHX}
	V_{IH2}	0.7 V_{CC}	V_{SS} + 5.8	V	P76, P77 pins (N-ch open drain pins)
	V_{IHS}	0.8 V_{CC}	V_{CC} + 0.3	V	Hysteresis input pins
	V_{IHM}	V_{CC} – 0.3	V_{CC} + 0.3	V	MD pin input
	V_{IHX}	0.8 V_{CC}	V_{CC} + 0.3	V	X0A pin, X1A pin
"L" level input voltage	V_{IL}	V_{SS} – 0.3	0.3 V_{CC}	V	All pins other than V_{ILS}, V_{ILM} and V_{IHX}
	V_{ILS}	V_{SS} – 0.3	0.2 V_{CC}	V	Hysteresis input pins
	V_{ILM}	V_{SS} – 0.3	V_{SS} + 0.3	V	MD pin input
	V_{ILX}	V_{SS} – 0.3	0.1	V	X0A pin, X1A pin
Operating temperature	T_A	–40	+85	°C	

* : P24 to P27, P30 to P37, P40 to P42, P70 to P74, P76, P77 pins can be used as 5 V I/F pin on applied 5 V to $V_{CC}5$ pin.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

3. DC Characteristics

(V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
"H" level output voltage	V_{OH}	All output pins	V_{CC} = 2.7 V, I_{OH} = –1.6 mA	$V_{CC}3$ – 0.3	—	—	V	
			V_{CC} = 4.5 V, I_{OH} = –4.0 mA	$V_{CC}5$ – 0.5	—	—	V	At using 5 V power supply
"L" level output voltage	V_{OL}	All output pins	V_{CC} = 2.7 V, I_{OL} = 2.0 mA	—	—	0.4	V	
			V_{CC} = 4.5 V, I_{OH} = 4.0 mA	—	—	0.4	V	At using 5 V power supply
Input leakage current	I_{IL}	All input pins	V_{CC} = 3.3 V, $V_{SS} < V_I < V_{CC}$	–10	—	+10	µA	
Pull-up resistance	R_{PULL}	—	V_{CC} = 3.0 V, at T_A = +25 °C	20	53	200	kΩ	
Open drain output current	I_{leak}	P40 to P42, P70 to P74, P76, P77	—	—	0.1	10	µA	
Power supply current	I_{CC}	—	At V_{CC} = 3.3 V, internal 25 MHz operation, normal operation	—	45	60	mA	
			At V_{CC} = 3.3 V, internal 25 MHz operation, Flash programming	—	55	70	mA	
	I_{CCS}	—	At V_{CC} = 3.3 V, internal 25 MHz operation, sleep mode	—	17	35	mA	
	I_{CCL}	—	At V_{CC} = 3.3 V, external 32 kHz, internal 8 kHz operation, sub clock operation (T_A = +25 °C)	—	15	140	µA	
	I_{CCT}	—	At V_{CC} = 3.3 V, external 32 kHz, internal 8 kHz operation, watch mode (T_A = +25 °C)	—	1.8	40	µA	
	I_{CCH}	—	T_A = +25 °C, stop mode, at V_{CC} = 3.3 V	—	0.8	40	µA	
Input capacitance	C_{IN}	Other than AV_{CC}, AV_{SS}, V_{CC}, V_{SS}	—	—	5	15	pF	

Notes :
- Pins P40 to P42, P70 to P74, P76, and P77 are N-ch open drain pins with control, which are usually used as CMOS.
- P76 and P77 are open drain pins without P-ch.
- For use as a single 3 V power supply products, set $V_{CC} = V_{CC}3 = V_{CC}5$.
- When the device is used with dual power supplies, P24 to P27, P30 to P37, P40 to P42, P70 to P74, P76 and P77 serve as 5 V pins while the other pins serve as 3 V I/O pins.

4. AC Characteristics

(1) Clock Timing

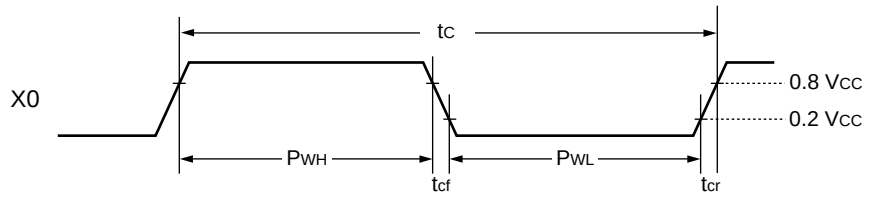
(V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Clock frequency	F_{CH}	X0, X1	—	3	—	25	MHz	External crystal oscillator
			—	3	—	50		External clock input
			—	4	—	25		1 multiplied PLL
			—	3	—	12.5		2 multiplied PLL
			—	3	—	6.66		3 multiplied PLL
			—	3	—	6.25		4 multiplied PLL
			—	3	—	4.16		6 multiplied PLL
			—	3	—	3.12		8 multiplied PLL
	F_{CL}	X0A, X1A	—	—	32.768	—	kHz	
Clock cycle time	t_C	X0, X1	—	20	—	333	ns	*1
	t_{CL}	X0A, X1A	—	—	30.5	—	µs	
Input clock pulse width	P_{WH} P_{WL}	X0	—	5	—	—	ns	
	P_{WLH} P_{WLL}	X0A	—	—	15.2	—	µs	*2
Input clock rise, fall time	t_{cr} t_{cf}	X0	—	—	—	5	ns	With external clock
Internal operating clock frequency	f_{CP}	—	—	1.5	—	25	MHz	*1
	f_{CPL}	—	—	—	8.192	—	kHz	
Internal operating clock cycle time	t_{CP}	—	—	40.0	—	666	ns	*1
	t_{CPL}	—	—	—	122.1	—	µs	

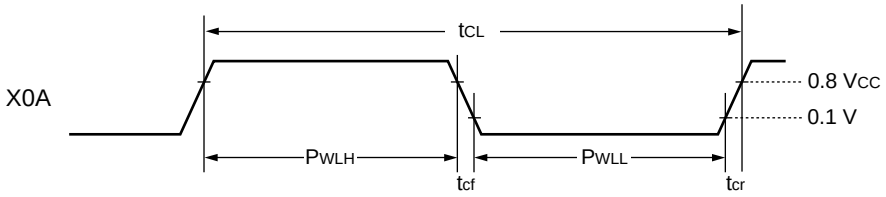
*1 : Be careful of the operating voltage.

*2 : Duty raito should be 50 % ± 3 %.

- X0, X1 clock timing

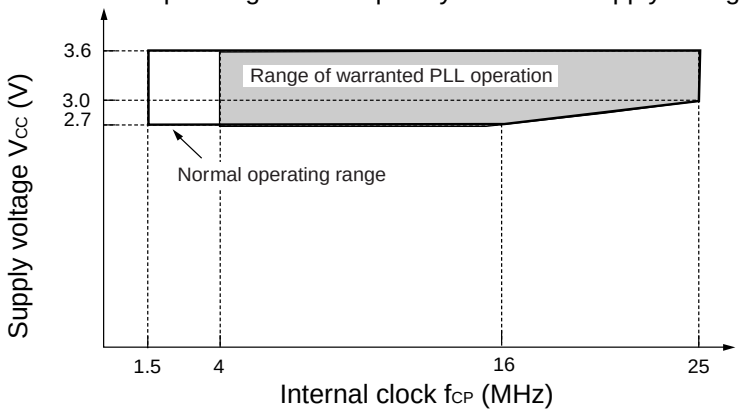


- X0A, X1A clock timing



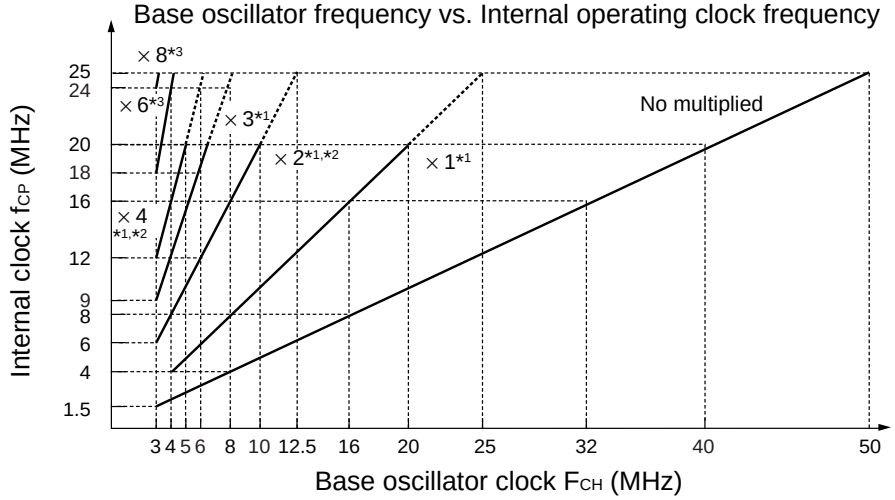
• Range of warranted PLL operation

Internal operating clock frequency vs. Power supply voltage



Notes: • Only at 1 multiplied PLL, use with more than f_{CP} = 4 MHz.
• For A/D operating frequency, refer to “5. A/D Converter Electrical Characteristics”.

Base oscillator frequency vs. Internal operating clock frequency



*1 : In setting as 1, 2, 3 and 4 multiplied PLL, when the internal clock is used at 20 MHz < f_{CP} ≤ 25 MHz, set the PLLOS register to “DIV2 bit = 1” and “PLL2 bit = 1”.
[Example] When using the base oscillator frequency of 24 MHz at 1 multiplied PLL :
CKSCR register : CS1 bit = “0”, CS0 bit = “0” PLLOS register : DIV2 bit = “1”, PLL2 bit = “1”
[Example] When using the base oscillator frequency of 6 MHz at 3 multiplied PLL :
CKSCR register : CS1 bit = “1”, CS0 bit = “0” PLLOS register : DIV2 bit = “1”, PLL2 bit = “1”

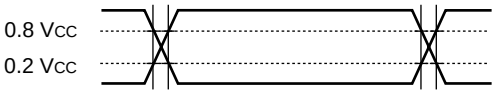
*2 : In setting as 2 and 4 multiplied PLL, when the internal clock is used at 20 MHz < f_{CP} ≤ 25 MHz, the following setting is also enabled.
2 multiplied PLL : CKSCR register : CS1 bit = “0”, CS0 bit = “0”
PLLOS register : DIV2 bit = “0”, PLL2 bit = “1”
4 multiplied PLL : CKSCR register : CS1 bit = “0”, CS0 bit = “1”
PLLOS register : DIV2 bit = “0”, PLL2 bit = “1”

*3 : When using in setting as 6 and 8 multiplied PLL, set the PLLOS register to “DIV2 bit = 0” and “PLL2 bit = 1”.
[Example] When using the base oscillator frequency of 4 MHz at 6 multiplied PLL :
CKSCR register : CS1 bit = “1”, CS0 bit = “0” PLLOS register : DIV2 bit = “0”, PLL2 bit = “1”
[Example] When using the base oscillator frequency of 3 MHz at 8 multiplied PLL :
CKSCR register : CS1 bit = “1”, CS0 bit = “1” PLLOS register : DIV2 bit = “0”, PLL2 bit = “1”

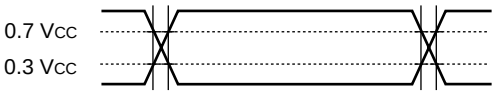
AC standards are set at the following measurement voltage values.

- Input signal waveform

Hysteresis input pins

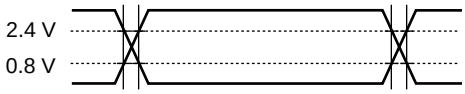


- Pins other than hysteresis input/MD input



- Output signal waveform

Output pins



(2) Reset Input Standards

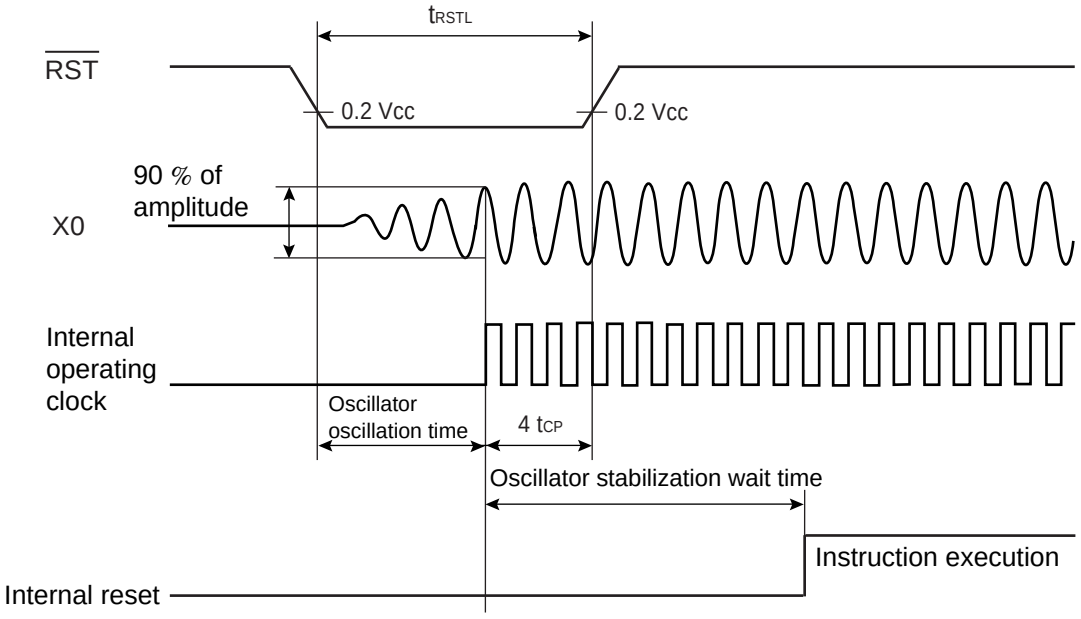
(V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condi-tions	Value		Unit	Remarks
				Min	Max		
Reset input time	t_{RSTL}	$\overline{RST}$	—	16 t_{CP}*1	—	ns	Normal operation
				Oscillator oscillation time*2 + 4 t_{CP}*1	—	ms	Stop mode

*1 : t_{CP} is internal operating clock cycle time. Refer to “ (1) Clock Timing”.

*2 : Oscillator oscillation time is the time to 90 % of amplitude. For a crystal oscillator this is on the order of several milliseconds to tens of milliseconds. For a FAR/ceramic oscillator, this is several hundred microseconds to several milliseconds. For an external clock signal the value is 0 ms.

• In stop mode



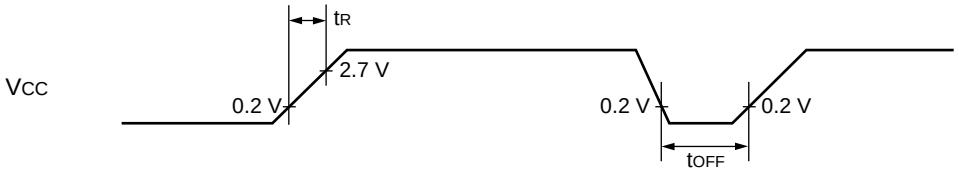
(3) Power-on Reset Standards

(V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

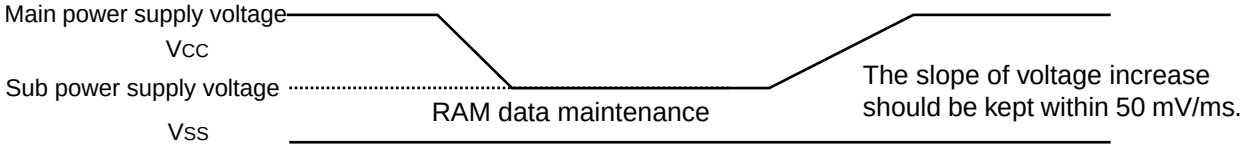
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Power rise time	t_R	V_{CC}	—	—	30	ms	*
Power down time	t_{OFF}	V_{CC}		1	—	ms	In repeated operation

* : Power rise time requires V_{CC} < 0.2 V.

Notes:
- The above standards are for the application of a power-on reset.
- Within the device, the power-on reset should be applied by switching the power supply off and on again.



Rapid fluctuations in power supply voltage may trigger a power-on reset in some cases. As shown below, when changing supply voltage during operation, it is recommended that voltage changes be suppressed and a smooth restart be applied.



(4) UART Timing

(V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

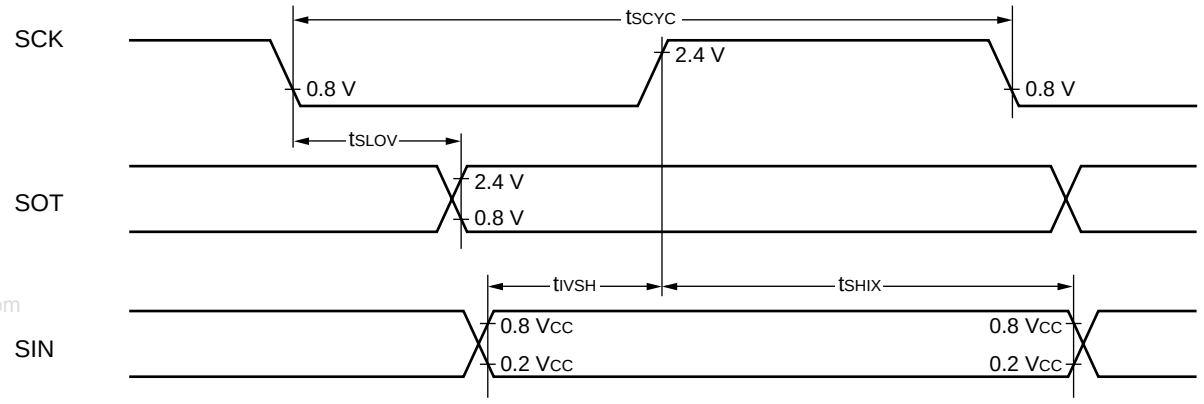
Parameter	Symbol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	—	Internal shift clock mode output pins : C_L*1 = 80 pF + 1 TTL	8 t_{CP}*2	—	ns	
SCK↓→SOT delay time	t_{SLOV}	—		–80	+80	ns	
				–120	+120	ns	f_{CP} = 8 MHz
Valid SIN→SCK↑	t_{IVSH}	—		100	—	ns	
				200	—	ns	f_{CP} = 8 MHz
SCK↑→valid SIN hold time	t_{SHIX}	—		t_{CP}*2	—	ns	
Serial clock “H” pulse width	t_{SHSL}	—	External shift clock mode output pins : C_L*1 = 80 pF + 1 TTL	4 t_{CP}*2	—	ns	
Serial clock “L” pulse width	t_{SLSH}	—		4 t_{CP}*2	—	ns	
SCK↓→SOT delay time	t_{SLOV}	—		—	150	ns	
				—	200	ns	f_{CP} = 8 MHz
Valid SIN→SCK↑	t_{IVSH}	—		60	—	ns	
				120	—	ns	f_{CP} = 8 MHz
SCK↑→valid SIN hold time	t_{SHIX}	—		60	—	ns	
				120	—	ns	f_{CP} = 8 MHz

*1 : C_L is the load capacitance applied to pins for testing.

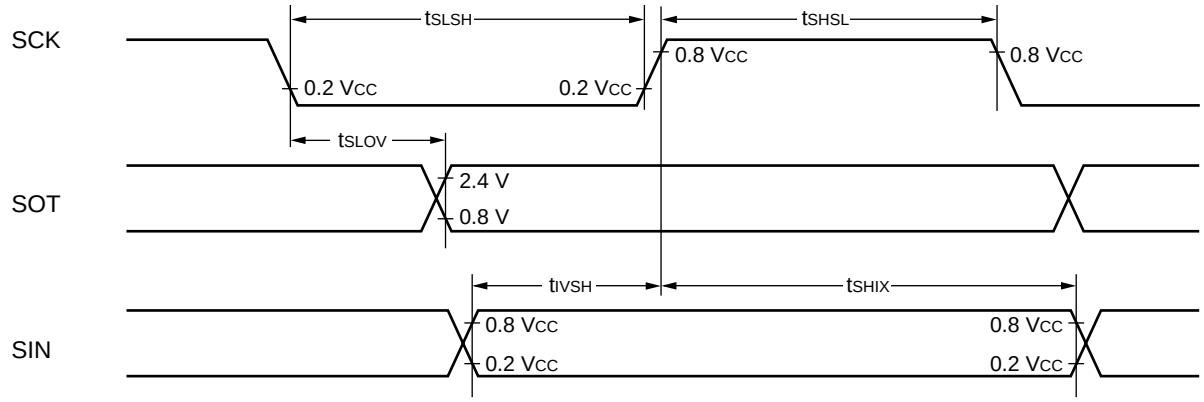
*2 : t_{CP} is internal operating clock cycle time. Refer to “ (1) Clock Timing”.

Note : AC ratings are for CLK synchronized mode.

• Internal shift clock mode



• External shift clock mode



(5) Extended I/O Serial Interface Timing

(V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

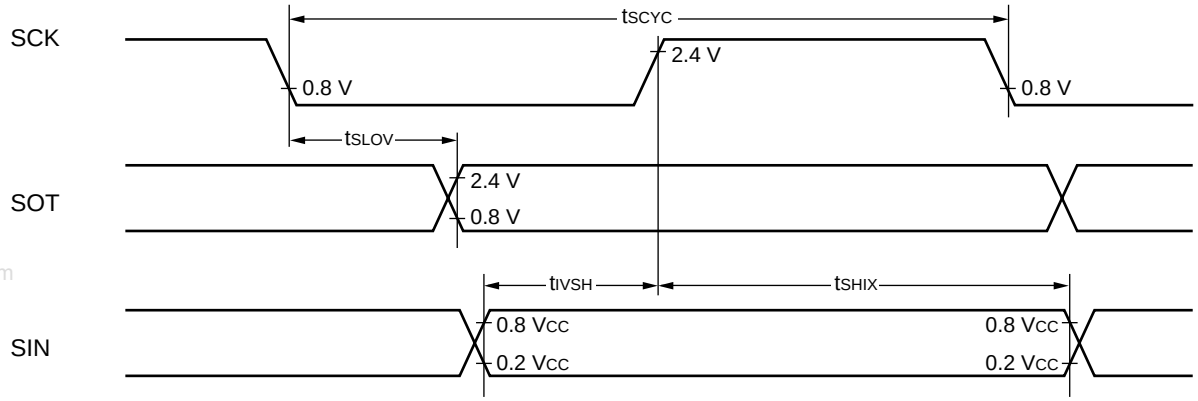
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	—	Internal shift clock mode output pins : C_L*1 = 80 pF + 1 TTL	8 t_{CP}*2	—	ns	
SCK↓→SOT delay time	t_{SLOV}	—		–80	+ 80	ns	
				–120	+ 120	ns	f_{CP} = 8 MHz
Valid SIN→SCK↑	t_{IVSH}	—		100	—	ns	
				200	—	ns	f_{CP} = 8 MHz
SCK↑→valid SIN hold time	t_{SHIX}	—		t_{CP}*2	—	ns	
Serial clock “H” pulse width	t_{SHSL}	—	External shift clock mode output pins : C_L*1 = 80 pF + 1 TTL	4 t_{CP}*2	—	ns	
Serial clock “L” pulse width	t_{SLSH}	—		4 t_{CP}*2	—	ns	
SCK↓→SOT delay time	t_{SLOV}	—		—	150	ns	
				—	200	ns	f_{CP} = 8 MHz
Valid SIN→SCK↑	t_{IVSH}	—		60	—	ns	
				120	—	ns	f_{CP} = 8 MHz
SCK↑→valid SIN hold time	t_{SHIX}	—		60	—	ns	
				120	—	ns	f_{CP} = 8 MHz

*1 : C_L is the load capacitance applied to pins for testing.

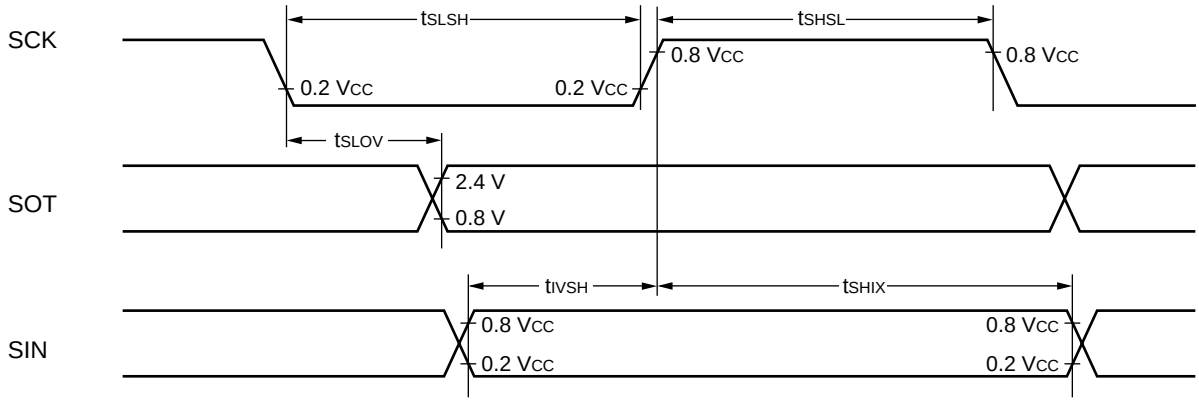
*2 : t_{CP} is internal operating clock cycle time. Refer to “ (1) Clock Timing”.

Notes : • AC ratings are for CLK synchronized mode.
• Values on this table are target values.

• Internal shift clock mode



• External shift clock mode

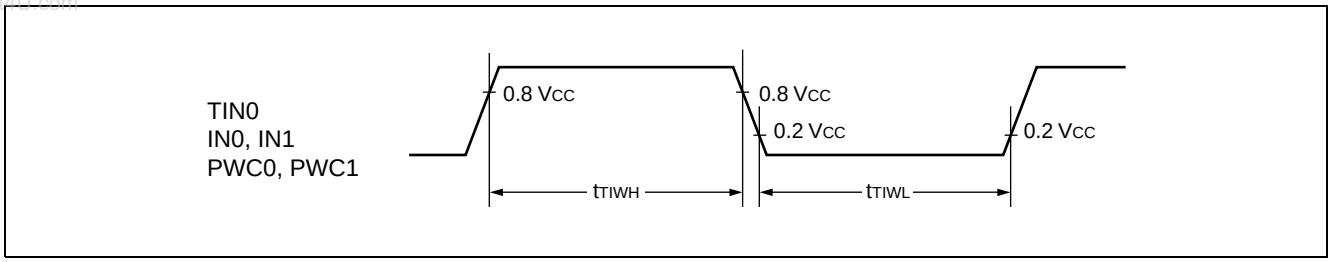


(6) Timer Input Timing

(V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH} t_{TIWL}	TIN0, IN0, IN1, PWC0, PWC1	—	4 t_{CP}*	—	ns	

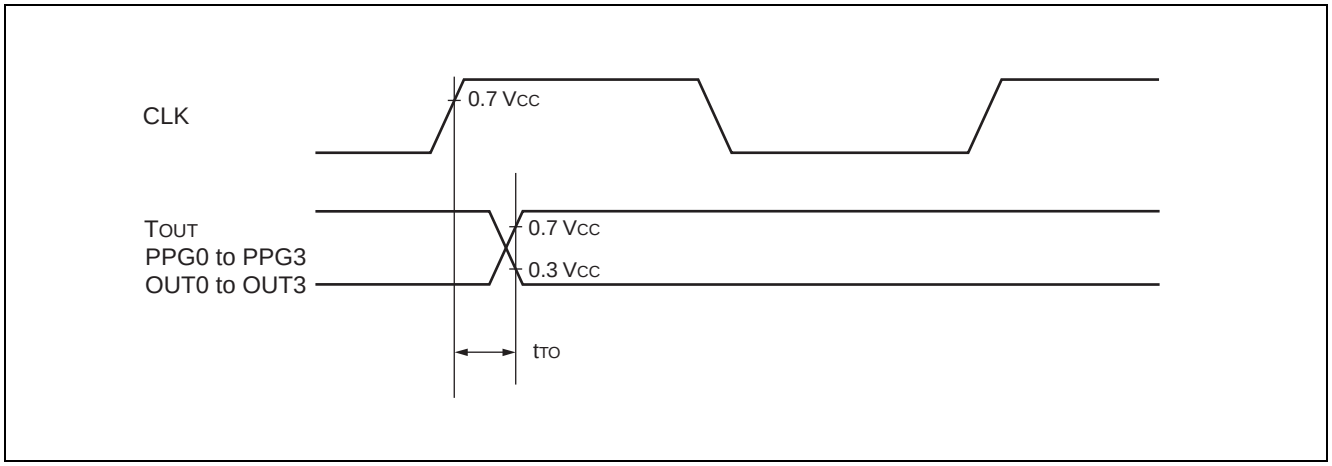
* : t_{CP} is internal operating clock cycle time. Refer to “ (1) Clock Timing”.



(7) Timer Output Timing

(V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Sym-bol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
CLK↑→Tout change time PPG0 to PPG3 change time OUT0 to OUT3 change time	t_{TO}	TOT0, PPG0 to PPG3, OUT0 to OUT3	Load conditions 80 pF	30	—	ns	



(8) I²C Timing

(V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

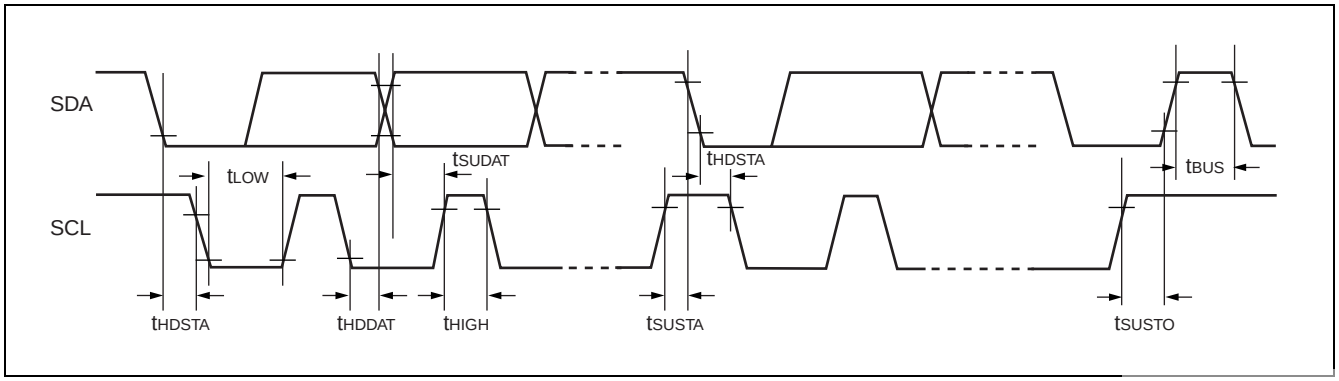
Parameter	Symbol	Condition	Standard-mode		Unit
			Min	Max	
SCL clock frequency	f_{SCL}	When power supply voltage of external pull-up resistance is 5.5 V R = 1.3 kΩ, C = 50 pF*2 When power supply voltage of external pull-up resistance is 3.6 V R = 1.6 kΩ, C = 50 pF*2	0	100	kHz
Hold time (repeated) START condition SDA↓→SCL↓	t_{HDSTA}		4.0	—	µs
"L" width of the SCL clock	t_{LOW}		4.7	—	µs
"H" width of the SCL clock	t_{HIGH}		4.0	—	µs
Set-up time (repeated) START condition SCL↑→SDA↓	t_{SUSTA}		4.7	—	µs
Data hold time SCL↓→SDA↓↑	t_{HDDAT}		0	3.45*3	µs
Data set-up time SDA↓↑→SCL↑	t_{SUDAT}	When power supply voltage of external pull-up resistance is 5.5 V f_{CP}*1 ≤ 20 MHz, R = 1.3 kΩ, C = 50 pF*2 When power supply voltage of external pull-up resistance is 3.6 V f_{CP}*1 ≤ 20 MHz, R = 1.6 kΩ, C = 50 pF*2	250	—	ns
		When power supply voltage of external pull-up resistance is 5.5 V f_{CP}*1 > 20 MHz, R = 1.3 kΩ, C = 50 pF*2 When power supply voltage of external pull-up resistance is 3.6 V f_{CP}*1 > 20 MHz, R = 1.6 kΩ, C = 50 pF*2	200	—	ns
Set-up time for STOP condition SCL↑→SDA↑	t_{SUSTO}	When power supply voltage of external pull-up resistance is 5.5 V R = 1.3 kΩ, C = 50 pF*2 When power supply voltage of external pull-up resistance is 3.6 V R = 1.6 kΩ, C = 50 pF*2	4.0	—	µs
Bus free time between a STOP and START condition	t_{BUS}		4.7	—	µs

*1 : f_{CP} is internal operation clock frequency. Refer to " (1) Clock Timing".

*2 : R,C : Pull-up resistor and load capacitor of the SCL and SDA lines.

*3 : The maximum t_{HDDAT} only has to be met if the device does not stretch the "L" width (t_{LOW}) of the SCL signal.

Note : V_{CC} = $V_{CC}3$ = $V_{CC}5$

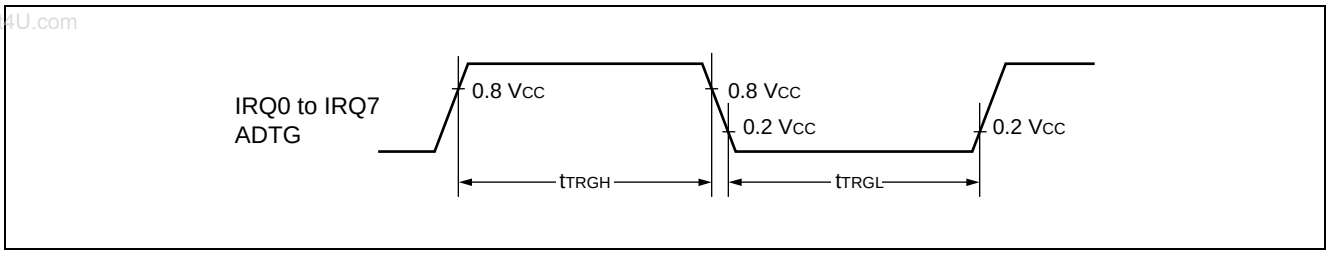


(9) Trigger Input Timing

(V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condi-tions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH}, t_{TRGL}	ADTG, IRQ0 to IRQ7	—	5 t_{CP}*	—	ns	Normal operation
				1	—	µs	Stop mode

* : t_{CP} is internal operating clock cycle time. Refer to “ (1) Clock Timing”.

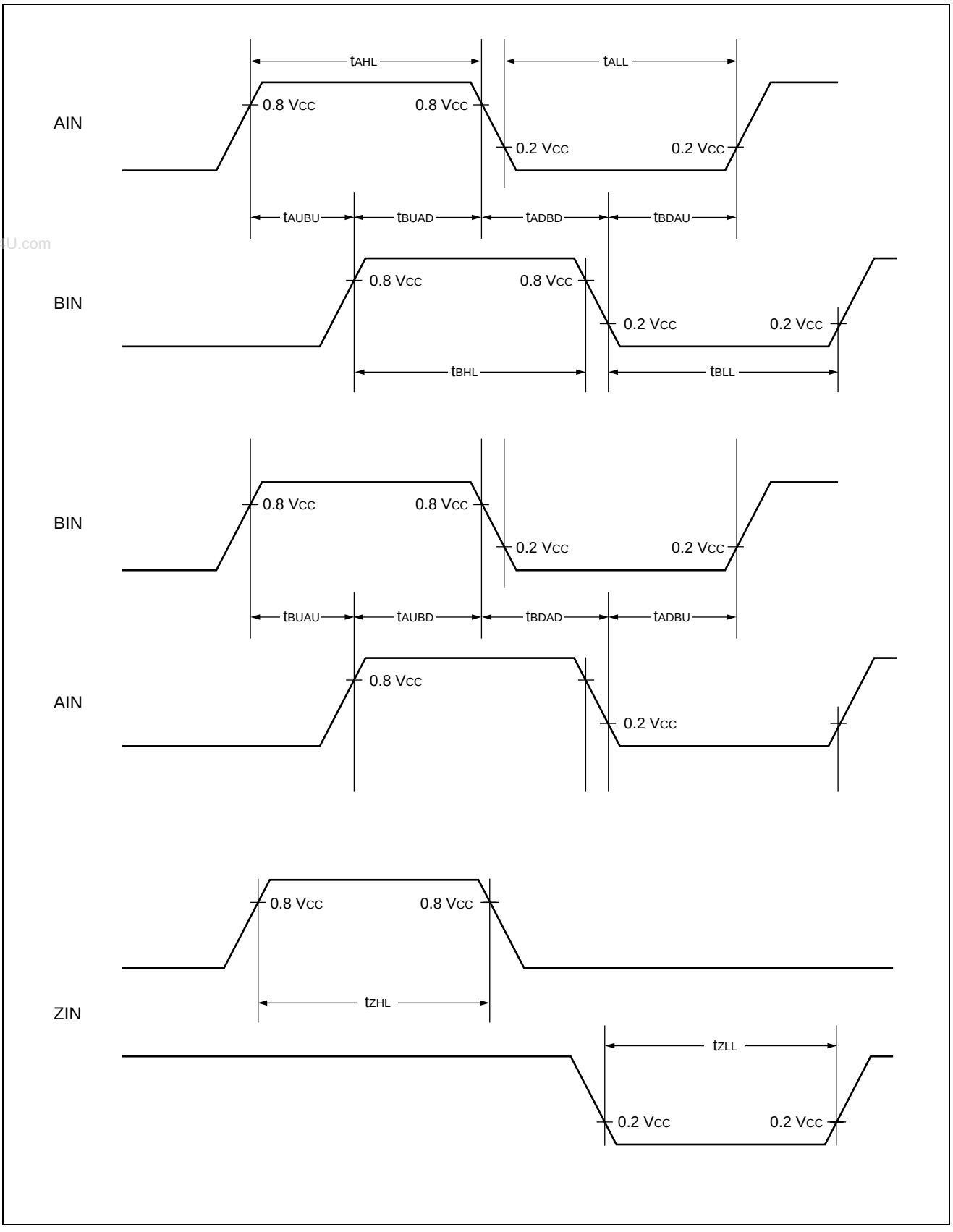


(10) Up-down Counter Timing

(V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
AIN input “H” pulse width	t_{AHL}	AIN0, AIN1, BIN0, BIN1	Load conditions 80 pF	8 t_{CP}*	—	ns	
AIN input “L” pulse width	t_{ALL}			8 t_{CP}*	—	ns	
BIN input “H” pulse width	t_{BHL}			8 t_{CP}*	—	ns	
BIN input “L” pulse width	t_{BLL}			8 t_{CP}*	—	ns	
AIN↑→BIN↑ rise time	t_{AUBU}			4 t_{CP}*	—	ns	
BIN↑→AIN↓ fall time	t_{BUAD}			4 t_{CP}*	—	ns	
AIN↓→BIN↑ rise time	t_{ADBD}			4 t_{CP}*	—	ns	
BIN↓→AIN↑ rise time	t_{BDAU}			4 t_{CP}*	—	ns	
BIN↑→AIN↑ rise time	t_{BUAU}			4 t_{CP}*	—	ns	
AIN↑→BIN↓ fall time	t_{AUBD}			4 t_{CP}*	—	ns	
BIN↓→AIN↑ rise time	t_{BDAD}			4 t_{CP}*	—	ns	
AIN↓→BIN↑ rise time	t_{ADBU}			4 t_{CP}*	—	ns	
ZIN input “H” pulse width	t_{ZHL}	ZIN0, ZIN1		4 t_{CP}*	—	ns	
ZIN input “L” pulse width	t_{ZLL}			4 t_{CP}*	—	ns	

* : t_{CP} is internal operating clock cycle time. Refer to “ (1) Clock Timing”.



5. A/D Converter Electrical Characteristics

(V_{CC} = AV_{CC} = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V, 2.7 V ≤ AVRH, T_A = –40 °C to +85 °C)

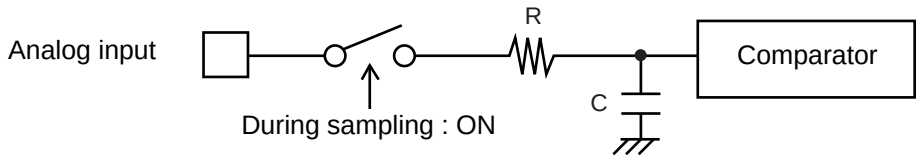
Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	10	bit	
Total error	—	—	—	—	±3.0	LSB	
Non-linear error	—	—	—	—	±2.5	LSB	
Differential linearity error	—	—	—	—	±1.9	LSB	
Zero transition voltage	V_{OT}	AN0 to AN7	AV_{SS} – 1.5 LSB	AV_{SS} + 0.5 LSB	AV_{SS} + 2.5 LSB	mV	
Full scale transition voltage	V_{FST}	AN0 to AN7	AVRH – 3.5 LSB	AVRH – 1.5 LSB	AVRH + 0.5 LSB	mV	
Conversion time	—	—	3.68 *1	—	—	µs	
Analog port input current	I_{AIN}	AN0 to AN7	—	0.1	10	µA	
Analog input voltage	V_{AIN}	AN0 to AN7	AV_{SS}	—	AVRH	V	
Reference voltage	—	AVRH	AV_{SS} + 2.2	—	AV_{CC}	V	
Power supply current	I_A	AV_{CC}	—	1.4	3.5	mA	
	I_{AH}	AV_{CC}	—	—	5 *2	µA	
Reference voltage supply current	I_R	AVRH	—	94	150	µA	
	I_{RH}	AVRH	—	—	5 *2	µA	
Offset between channels	—	AN0 to AN7	—	—	4	LSB	

*1 : At machine clock frequency of 25 MHz.

*2 : CPU stop mode current when A/D converter is not operating (at V_{CC} = AV_{CC} = AVRH = 3.0 V) .

- **About the external impedance of the analog input and its sampling time**
  - A/D converter with sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting A/D conversion precision.

- Analog input circuit model



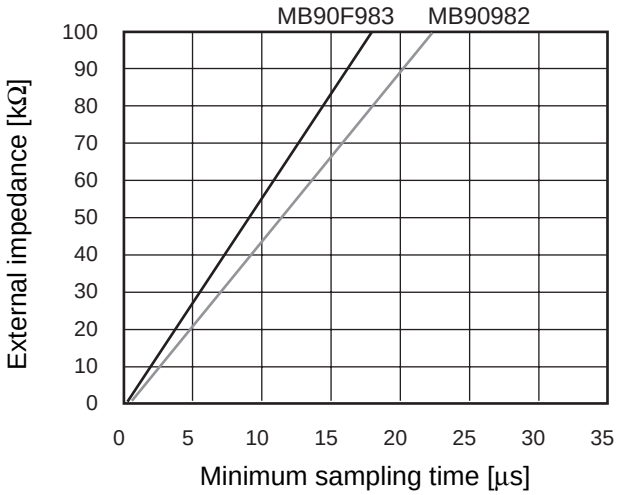
	R	C
MB90982	2.5 kΩ (Max)	31.0 pF (Max)
MB90F983	1.9 kΩ (Max)	25.0 pF (Max)

Note: The values are reference values.

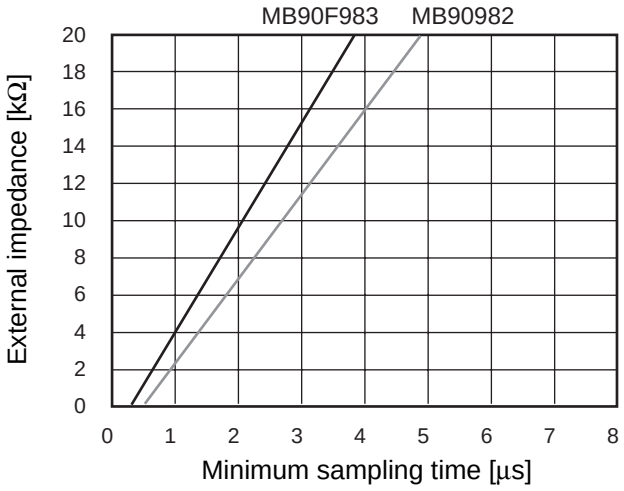
- To satisfy the A/D conversion precision standard, consider the relationship between the external impedance and minimum sampling time and either adjust the resistor value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value.

- The relationship between external impedance and minimum sampling time

(External impedance = 0 kΩ to 100 kΩ)



(External impedance = 0 kΩ to 100 kΩ)



- If the sampling time cannot be sufficient, connect a capacitor of about 0.1 µF to the analog input pin.

- **About errors**

As |AVRH – AV_{SS}| becomes smaller, values of relative errors grow larger.

Note : Concerning sampling time, and compare time
When 3.6 V ≥ AV_{CC} ≥ 2.7 V, then
Sampling time : 1.92 µs, compare time : 1.1 µs
Settings should ensure that actual values do not go below these values due to operating frequency changes.

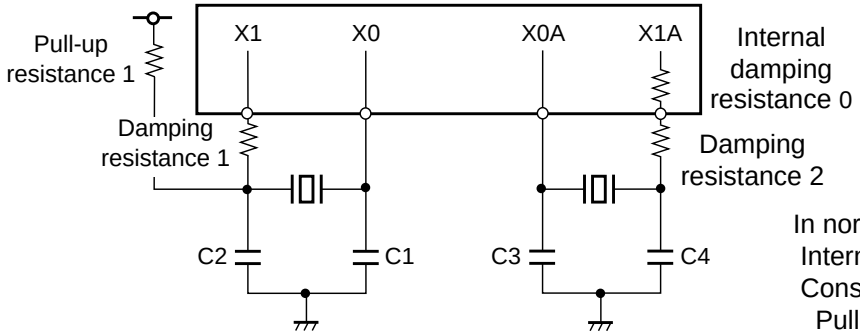
• Flash Memory Program/Erase Characteristics

Parameter	Conditions	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	T_A = + 25 °C, V_{CC} = 3.0 V	—	1	15	s	Excludes 00_H programming prior erasure
Chip erase time		—	7	—	s	Excludes 00_H programming prior erasure
Word (16-bit) programming time		—	16	3600	µs	Excludes system-level overhead
Program/Erase cycle	—	10000	—	—	cycle	
Flash Memory Data hold time	Average T_A = + 85 °C	10	—	—	year	*

* : The value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at +85 °C) .

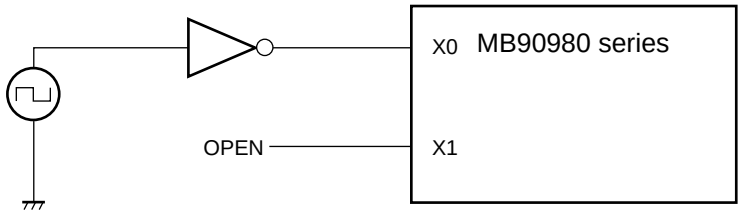
• Use of the X0/X1, X0A/X1A pins

When used with a crystal oscillator



In normal use :
Internal damping resistance 1 : Typ 600 kΩ
Consult with the oscillator manufacturer.
Pull-up resistance 1,
Damping resistance 1, 2,
C1 to C4

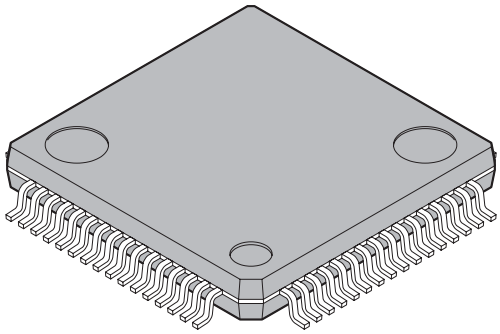
• Sample use with external clock input



■ ORDERING INFORMATION

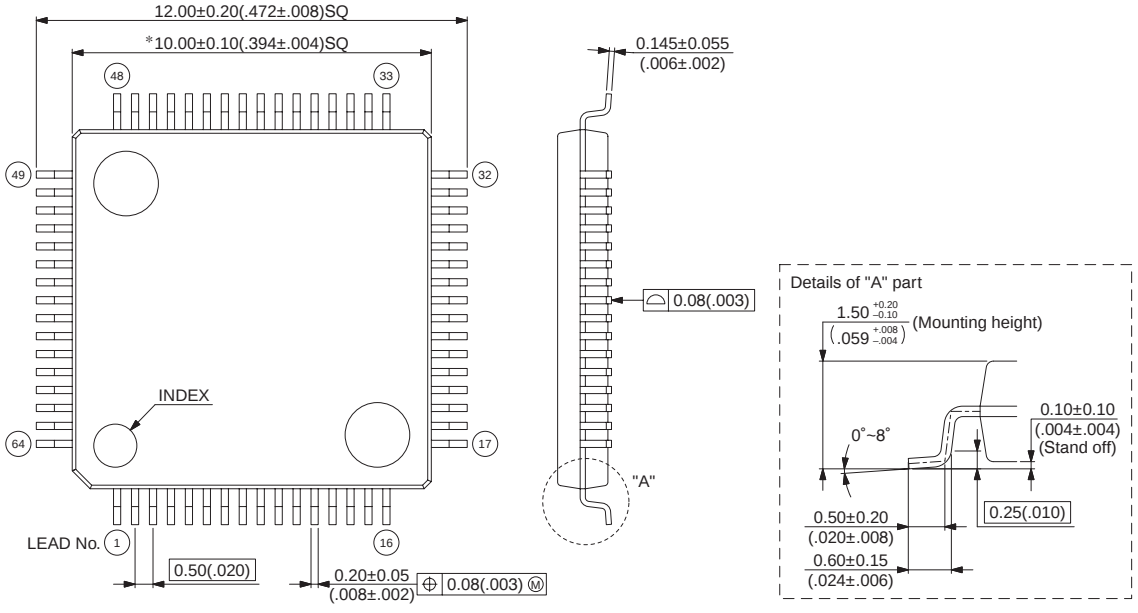
Model	Package	Remarks
MB90F983 MB90982	64-pin plastic LQFP (FPT-64P-M03)	

■ PACKAGE DIMENSIONS

64-pin plastic LQFP		
	Lead pitch	0.50 mm
	Package width × package length	10.0 × 10.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.32g
(FPT-64P-M03)	Code (Reference)	P-LFQFP64-10×10-0.50

64-pin plastic LQFP
(FPT-64P-M03)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values

The information for microcontroller supports is shown in the following homepage.
http://www.fujitsu.com/global/services/microelectronics/product/micom/support/index.html

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