FUJITSU MICROELECTRONICS
DATA SHEET

DS07-13734-6E

16-bit Microcontroller

CMOS

F²MC-16LX MB90330A Series

MB90333A/F334A/F335A/V330A

■ DESCRIPTION

The MB90330A series are 16-bit microcontrollers designed for applications, such as personal computer peripheral devices, that require USB communications. The USB feature supports not only 12-Mbps Function operation but also Mini-HOST operation. It is equipped with functions that are suitable for personal computer peripheral devices such as displays and audio devices, and control of mobile devices that support USB communications. While inheriting the AT architecture of the F²MC family, the instruction set supports the C language and extended addressing modes and contains enhanced signed multiplication and division instructions as well as a substantial collection of improved bit manipulation instructions. In addition, long word processing is now available by introducing a 32-bit accumulator.

Note : F²MC is the abbreviation of FUJITSU Flexible Microcontroller.

■ FEATURES

- **Clock**
  - Built-in oscillation circuit and PLL clock frequency multiplication circuit
  - Oscillation clock
  - The main clock is the oscillation clock divided into 2 (for oscillation 6 MHz : 3 MHz)
  - Clock for USB is 48 MHz
  - Machine clock frequency of 6 MHz, 12 MHz, or 24 MHz selectable
  - Minimum execution time of instruction : 41.6 ns (6 MHz oscillation clock, 4-time multiplied : machine clock 24 MHz and at operating V_{CC} = 3.3 V.
- **The maximum memory space : 16 Mbytes**
- **24-bit addressing**

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For the information for microcontroller supports, see the following web site.

http://edevice.fujitsu.com/micom/en-support/

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- **Bank addressing**
- **Instruction system**
  - Data types : Bit, Byte, Word and Long word
  - Addressing mode (23 types)
  - Enhanced high-precision computing with 32-bit accumulator
  - Enhanced Multiply/Divide instructions with sign and the RETI instruction
- **Instruction system compatible with high-level language (C language) and multi-task**
  - Employing system stack pointer
  - Instruction set symmetry and barrel shift instructions
- **Program Patch Function (2 address pointer)**
- **4-byte instruction queue**
- **Interrupt function**
  - Priority levels are programmable
  - 32 interrupts function
- **Data transfer function**
  - Extended intelligent I/O service function (EI²OS) : Maximum of 16 channels
  - μDMAC : Maximum 16 channels
- **Low Power Consumption Mode**
  - Sleep mode (with the CPU operating clock stopped)
  - Time-base timer mode (with the oscillator clock and time-base timer operating)
  - Stop mode (with the oscillator clock stopped)
  - CPU intermittent operation mode (with the CPU operating at fixed intervals of set cycles)
  - Watch mode (with 32 kHz oscillator clock and watch timer operating)
- **Package**
  - LQFP-120P (FPT-120P-M24 : 0.40 mm pin pitch)
  - LQFP-120P (FPT-120P-M21 : 0.50 mm pin pitch)

- **Process : CMOS technology**
- **Operation guaranteed temperature : − 40 °C to + 85 °C (0 °C to + 70 °C when USB is in use)**

■ INTERNAL PERIPHERAL FUNCTION (RESOURCE)

- **I/O port : Max 94 ports**
- **Time-base timer : 1 channel**
- **Watchdog timer : 1 channel**
- **Watch timer : 1 channel**
- **16-bit reload timer : 3 channels**
- **Multi-functional timer**
  - 16-bit free run timer : 1 channel
  - Output compare : 4 channels
    An interrupt request can be output when the 16-bit free-run timer value matches the compare register value.
  - Input capture : 4 channels
    Upon detection of the effective edge of the signal input to the external input pin, the input capture unit sets the input capture data register to the 16-bit free-run timer value to output an interrupt request.
  - 8/16-bit PPG timer (8-bit × 6 channels or 16-bit × 3 channels) the period and duty of the output pulse can be set by the program.
  - 16-bit PWC timer : 1 channel
    Timer function and pulse width measurement function
- **UART : 4 channels**
  - Full-duplex double buffer (8-bit length)
  - Asynchronous transfer or clock-synchronous serial (Extended I/O serial) transfer can be set.
- **Extended I/O serial interface : 1 channel**
- **DTP/External interrupt circuit (8 channels)**
  - Activate the extended intelligent I/O service by external interrupt input
  - Interrupt output by external interrupt input
- **Delay interrupt output module**
  - Output an interrupt request for task switching

- **8/10-bit A/D converter : 16 channels**
  - 8-bit resolution or 10-bit resolution can be set.
- **USB : 1 channel**
  - USB function (correspond to USB Full Speed)
  - Full Speed is supported/Endpoint are specifiable up to six.
  - Dual port RAM (The FIFO mode is supported).
  - Transfer type : Control, Interrupt, Bulk, or Isochronous transfer possible
  - USB Mini-HOST function
- **I^2C Interface : 3 channels**
  - Supports Intel SM bus standard and Phillips I^2C bus standards
  - Two-wire data transfer protocol specification
  - Master and slave transmission/reception

■ PRODUCT LINEUP

Part number	MB90V330A	MB90F334A	MB90F335A	MB90333A
Type	For evaluation	Built-in Flash memory	Built-in Flash memory	Built-in MASK ROM
ROM capacity	No	384 Kbytes	512 Kbytes	256 Kbytes
RAM capacity	28 Kbytes	24 Kbytes	30 Kbytes	16 Kbytes
Emulator-specific power supply *	Yes	—		
CPU functions	Number of basic instructions : 351 instructions Minimum instruction execution time : 41.6 ns/at oscillation of 6 MHz (When 4 times are used : Machine clock of 24 MHz) Addressing type : 23 types Program Patch Function : For 2 address pointers Maximum memory space : 16 Mbytes			
Ports	I/O Ports (CMOS) 94 ports			
UART	Equipped with full-duplex double buffer Clock synchronous or asynchronous operation selectable It can also be used for I/O serial Built-in special baud-rate generator Built-in 4 channels			
16-bit reload timer	16-bit reload timer operation Built-in 3 channels			
Multi-functional timer	16-bit free run timer × 1 channel Output compare × 4 channels Input capture × 4 channels 8/16-bit PPG timer (8-bit mode × 6 channels, 16-bit mode × 3 channels) 16-bit PWC timer × 1 channel			
8/10-bit A/D converter	16 channels (input multiplex) 8-bit resolution or 10-bit resolution can be set. Conversion time : 7.16 μs at minimum (24 MHz machine clock at maximum)			
DTP/External interrupt	8 channels Interrupt factor : “L”→“H” edge/“H”→“L” edge/“L” level/“H” level selectable			
I²C	3 channels			
Extended I/O serial interface	1 channel			
USB	1 channel USB function (correspond to USB Full Speed) USB Mini-HOST function			
External bus interface	For multi-bus/non-multi-bus			
Withstand voltage of 5 V	16 ports (excluding UTEST and I/O for I²C)			
Low Power Consumption Mode	Sleep mode/Time-base timer mode/Stop mode/CPU intermittent mode/ Watch mode			
Process	CMOS			
Operating voltage	3.3 V ± 0.3 V (at maximum machine clock 24 MHz)			

* : It is setting of Jumper switch (TOOL VCC) when Emulator (MB2147-01) is used. Please refer to the MB2147-01 or MB2147-20 hardware manual (3.3 Emulator-dedicated Power Supply Switching) about details.

■ PACKAGES AND PRODUCT MODELS

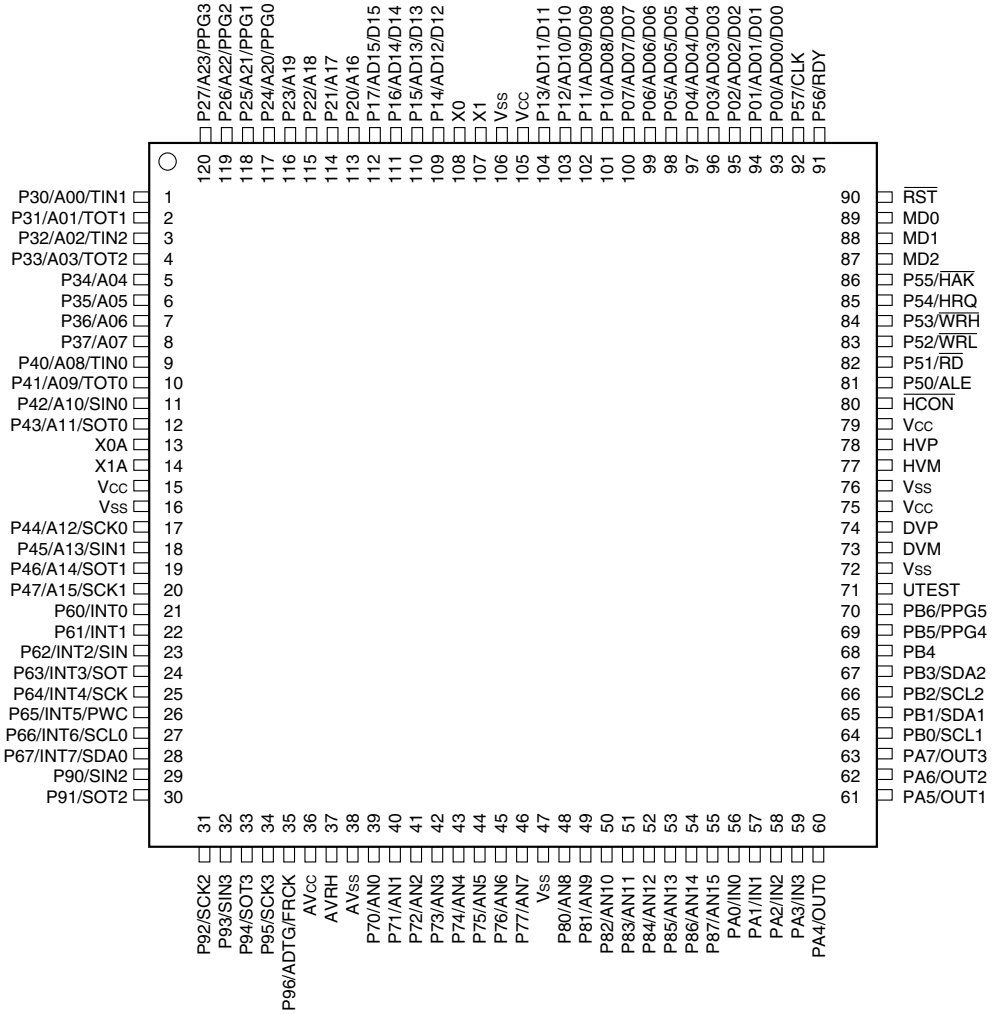
Package	MB90333A	MB90F334A	MB90F335A	MB90V330A
FPT-120P-M24 (LQFP-0.40 mm)	○	○	○	×
FPT-120P-M21 (LQFP-0.50 mm)	○	○	○	×
PGA-299C-A01 (PGA)	×	×	×	○

○ : Yes × : No

Note : For detailed information on each package, refer to "■ PACKAGE DIMENSIONS".

■ PIN ASSIGNMENT

(TOP VIEW)



(FPT-120P-M24 / FPT-120P-M21)

■ PIN DESCRIPTION

Pin no.	Pin name	I/O Circuit type*	Function
108, 107	X0, X1	A	Terminals to connect the oscillator. When connecting an external clock, leave the X1 pin side unconnected.
13, 14	X0A, X1A	A	32 kHz oscillation terminals.
90	$\overline{\text{RST}}$	F	External reset input pin.
93 to 100	P00 to P07	H	General purpose input/output port. The ports can be set to be added with a pull-up resistor (RD00 to RD07 = 1) by the pull-up resistor setting register (RDR0). (When the power output is set, it is invalid.)
	AD00 to AD07		Function as an I/O pin for the low-order external address and data bus in multiplex mode.
	D00 to D07		Function as an output pin for the low-order external data bus in non-multiplex mode.
101 to 104	P10 to P13	H	General purpose input/output port. The ports can be set to be added with a pull-up resistor (RD10 to RD13 = 1) by the pull-up resistor setting register (RDR1). (When the power output is set, it is invalid.)
	AD08 to AD11		Function as an I/O pin for the high-order external address and data bus in multiplex mode.
	D08 to D11		Function as an output pin for the high-order external data bus in non-multiplex mode.
109 to 112	P14 to P17	H	General purpose input/output port. The ports can be set to be added with a pull-up resistor (RD14 to RD17 = 1) by the pull-up resistor setting register (RDR1). (When the power output is set, it is invalid.)
	AD12 to D15		Function as an I/O pin for the high-order external address and data bus in multiplex mode.
	D12 to D15		Function as an output pin for the high-order external data bus in non-multiplex mode.
113 to 116	P20 to P23	D	This is a general purpose I/O port. When the bits of external address output control register (HACR) are set to “1” in external bus mode, these pins function as general purpose I/O ports.
	A16 to A19		When the bits of external address output control register (HACR) are set to “0” in multiplex mode, these pins function as address high output pins.
	A16 to A19		When the bits of external address output control register (HACR) are set to “0” in non-multiplex mode, these pins function as address high output pins.

(Continued)

Pin no.	Pin name	I/O Circuit type*	Function
117 to 120	P24 to P27	D	This is a general purpose I/O port. When the bits of external address output control register (HACR) are set to “1” in external bus mode, these pins function as general purpose I/O ports.
	A20 to A23		When the bits of external address output control register (HACR) are set to “0” in multiplex mode, these pins function as address high output pins.
	A20 to A23		When the bits of external address output control register (HACR) are set to “0” in non-multiplex mode, these pins function as address high output pins.
	PPG0 to PPG3		Function as ch.0 to ch.3 output pins for the 8-bit PPG timer.
1	P30	D	General purpose input/output port.
	A00		Function as the external address pin in non-multi-bus mode.
	TIN1		Function as an event input pin for 16-bit reload timer ch.1.
2	P31	D	General purpose input/output port.
	A01		Function as the external address pin in non-multi-bus mode.
	TOT1		Function as the output pin for 16-bit reload timer ch.1.
3	P32	D	General purpose input/output port.
	A02		Function as the external address pin in non-multi-bus mode.
	TIN2		Function as an event input pin for 16-bit reload timer ch.2.
4	P33	D	General purpose input/output port.
	A03		Function as the external address pin in non-multi-bus mode.
	TOT2		Function as the output pin for 16-bit reload timer ch.2.
5 to 8	P34 to P37	D	General purpose input/output port.
	A04 to A07		Function as the external address pin in non-multi-bus mode.
9	P40	G	General purpose input/output port.
	A08		Function as the external address pin in non-multi-bus mode.
	TIN0		Function as an event input pin for 16-bit reload timer ch.0.
10	P41	G	General purpose input/output port.
	A09		Function as the external address pin in non-multi-bus mode.
	TOT0		Function as the output pin for 16-bit reload timer ch.0.
11	P42	G	General purpose input/output port.
	A10		Function as the external address pin in non-multi-bus mode.
	SIN0		Function as a data input pin for UART ch.0.
12	P43	G	General purpose input/output port.
	A11		Function as the external address pin in non-multi-bus mode.
	SOT0		Function as a data output pin for UART ch.0.
17	P44	G	General purpose input/output port.
	A12		Function as the external address pin in non-multi-bus mode.
	SCK0		Function as a clock I/O pin for UART ch.0.

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Pin no.	Pin name	I/O Circuit type*	Function
18	P45	G	General purpose input/output port.
	A13		Function as the external address pin in non-multi-bus mode.
	SIN1		Function as a data input pin for UART ch.1.
19	P46	G	General purpose input/output port.
	A14		Function as the external address pin in non-multi-bus mode.
	SOT1		Function as a data output pin for UART ch.1.
20	P47	G	General purpose input/output port.
	A15		Function as the external address pin in non-multi-bus mode.
	SCK1		Function as a clock I/O pin for UART ch.1.
81	P50	L	General purpose input/output port.
	ALE		Function as the address latch enable signal pin in external bus mode.
82	P51	L	General purpose input/output port.
	$\overline{RD}$		Function as the read strobe output pin in external bus mode.
83	P52	L	General purpose input/output port.
	$\overline{WRL}$		Function as the data write strobe output pin on the lower side in external bus mode. This pin functions as a general-purpose I/O port when the WRE bit in the EPCR register is “0”.
84	P53	L	General purpose input/output port.
	$\overline{WRH}$		Function as the data write strobe output pin on the higher side in bus width 16-bit external bus mode. This pin functions as a general-purpose I/O port when the WRE bit in the EPCR register is “0”.
85	P54	L	General purpose input/output port.
	HRQ		Function as the hold request input pin in external bus mode. This pin functions as a general-purpose I/O port when the HDE bit in the EPCR register is “0”.
86	P55	L	General purpose input/output port.
	$\overline{HAK}$		Function as the hold acknowledge output pin in external bus mode. This pin functions as a general-purpose I/O port when the HDE bit in the EPCR register is “0”.
91	P56	L	General purpose input/output port.
	RDY		Function as the external ready input pin in external bus mode. This pin functions as a general-purpose I/O port when the RYE bit in the EPCR register is “0”.
92	P57	L	General purpose input/output port.
	CLK		Function as the machine cycle clock output pin in external bus mode. This pin functions as a general-purpose I/O port when the CKE bit in the EPCR register is “0”.
21, 22	P60, P61	C	General purpose input/output port. (With stand voltage of 5 V)
	INT0, INT1		Function as external interrupt ch.0 and ch.1 input pins.

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Pin no.	Pin name	I/O Circuit type*	Function
23	P62	C	General purpose input/output ports. (Withstand voltage of 5 V)
	INT2		Function as an external interrupt ch.2 input pin.
	SIN		Extended I/O serial interface data input pin.
24	P63	C	General purpose input/output port. (Withstand voltage of 5 V)
	INT3		Function as an external interrupt ch.3 input pin.
	SOT		Extended I/O serial interface data output pin.
25	P64	C	General purpose input/output port. (Withstand voltage of 5 V)
	INT4		Function as an external interrupt ch.4 input pin.
	SCK		Extended I/O serial interface clock input/output pin.
26	P65	C	General purpose input/output port. (Withstand voltage of 5 V)
	INT5		Function as an external interrupt ch.5 input pin.
	PWC		Function as the PWC input pin.
27	P66	C	General purpose input/output port. (Withstand voltage of 5 V)
	INT6		Function as an external interrupt ch.6 input pin.
	SCL0		Function as the ch.0 clock I/O pin for the I^2C interface. Set port output to High-Z during I^2C interface operations.
28	P67	C	General purpose input/output port. (Withstand voltage of 5 V)
	INT7		Function as an external interrupt ch.7 input pin.
	SDA0		Function as the ch.0 data I/O pin for the I^2C interface. Set port output to High-Z during I^2C interface operations.
39 to 46	P70 to P77	I	General purpose input/output port.
	AN0 to AN7		Function as input pins for analog ch.0 to ch.7.
48 to 55	P80 to P87	I	General purpose input/output port.
	AN8 to AN15		Function as input pins for analog ch.8 to ch.15.
29	P90	D	General purpose input/output port.
	SIN2		Function as a data input pin for UART ch.2.
30	P91	D	General purpose input/output port.
	SOT2		Function as a data output pin for UART ch.2.
31	P92	D	General purpose input/output port.
	SCK2		Function as a clock I/O pin for UART ch.2.
32	P93	D	General purpose input/output port.
	SIN3		Function as a data input pin for UART ch.3.
33	P94	D	General purpose input/output port.
	SOT3		Function as a data output pin for UART ch.3.
34	P95	D	General purpose input/output port.
	SCK3		Function as a clock I/O pin for UART ch.3.
35	P96	C	General purpose input/output port. (Withstand voltage of 5 V)
	ADTG		Function as the external trigger input pin when the A/D converter is being used.
	FRCK		Function as the external clock input pin when the free-run timer is being used.

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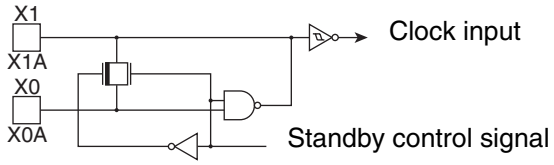
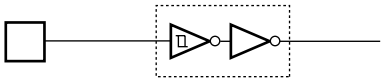
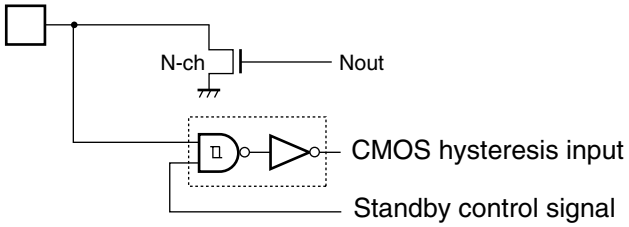
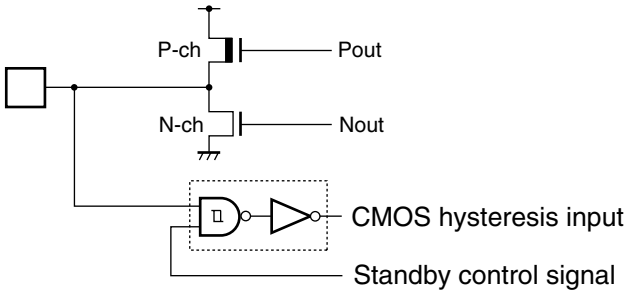
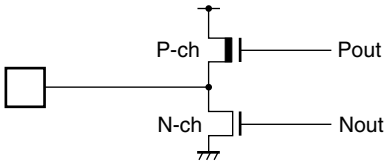
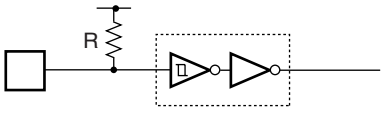
Pin no.	Pin name	I/O Circuit type*	Function
56 to 59	PA0 to PA3	C	General purpose input/output port. (Withstand voltage of 5 V)
	IN0 to IN3		Function as the input capture ch.0 to ch.3 trigger inputs.
60 to 63	PA4 to PA7	C	General purpose input/output port. (Withstand voltage of 5 V)
	OUT0 to OUT3		Function as the output compare ch.0 to ch.3 event output pins.
64	PB0	C	General purpose input/output port. (Withstand voltage of 5 V)
	SCL1		Function as the ch.1 clock I/O pin for the I²C interface. Set port output to High-Z during I²C interface operations.
65	PB1	C	General purpose input/output port. (Withstand voltage of 5 V)
	SDA1		Function as the ch.1 data I/O pin for the I²C interface. Set port output to High-Z during I²C interface operations.
66	PB2	C	General purpose input/output port. (Withstand voltage of 5 V)
	SCL2		Function as the ch.2 clock I/O pin for the I²C interface. Set port output to High-Z during I²C interface operations.
67	PB3	C	General purpose input/output port. (Withstand voltage of 5 V)
	SDA2		Function as the ch.2 data I/O pin for the I²C interface. Set port output to High-Z during I²C interface operations.
68	PB4	C	General purpose input/output port. (Withstand voltage of 5 V)
69, 70	PB5, PB6	D	General purpose input/output port.
	PPG4, PPG5		Function as ch.4 and ch.5 output pins for the 8-bit PPG timer.
71	UTEST	C	USB test pin. Connect this to a pull-down resistor during normal usage.
73	DVM	K	USB function D– pin.
74	DVP	K	USB function D+ pin.
77	HVM	K	USB Mini-HOST D– pin.
78	HVP	K	USB Mini-HOST D+ pin.
80	$\overline{\text{HCON}}$	E	External pull-up resistor connect pin.
36	AVcc	—	A/D converter power supply pin.
37	AVRH	J	A/D converter external reference power supply pin.
38	AVss	—	A/D converter power supply pin.
87 to 89	MD2 to MD0	B	Operation mode select input pin.
15	Vcc	—	Power supply pin.
75	Vcc	—	Power supply pin.
79	Vcc	—	Power supply pin.
105	Vcc	—	Power supply pin.
16	Vss	—	Power supply pin (GND).
47	Vss	—	Power supply pin (GND).
72	Vss	—	Power supply pin (GND).
76	Vss	—	Power supply pin (GND).
106	Vss	—	Power supply pin (GND).

* : For circuit information, refer to “■ I/O CIRCUIT TYPE”.

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		• High-rate oscillation feedback resistor, approx.1 MΩ • Low-rate oscillation feedback resistor, approx.10 MΩ • With standby control
B		CMOS hysteresis input
C		• CMOS hysteresis input • N-ch open drain output
D		• CMOS output • CMOS hysteresis input (With input interception function at standby) Notes : • Share one output buffer because both output of I/O port and internal resource are used. • Share one input buffer because both input of I/O port and internal resource are used.
E		CMOS output
F		CMOS hysteresis input with pull-up resistor

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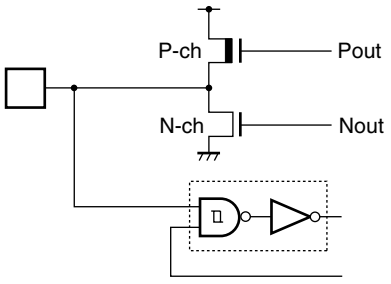
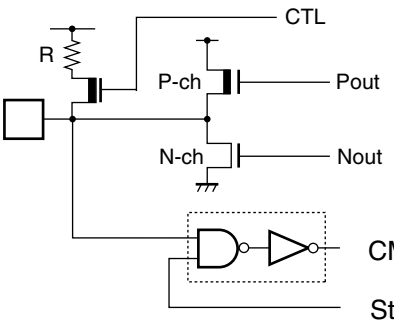
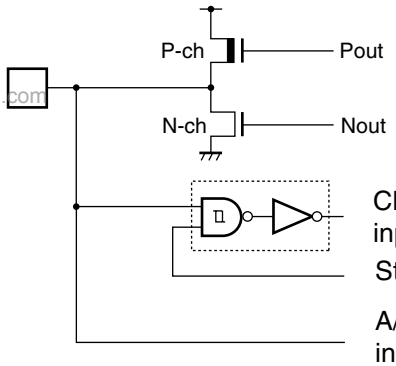
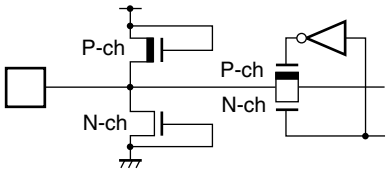
Type	Circuit	Remarks
G		• CMOS output • CMOS hysteresis input (With input interception function at standby) With open drain control signal
H		• CMOS output • CMOS input (With input interception function at standby) • With input pull-up register control
I		• CMOS output • CMOS hysteresis input (With input interception function at standby) • Analog input (The A/D converter analog input is enabled when the corresponding bit in the analog input enable register (ADER) is 1.) Notes: • Because the output of the I/O port and the output of internal resources are used combinedly, one output buffer is shared. • Because the input of the I/O port and the input of internal resources are used combinedly, one input buffer is shared.
J		A/D converter (AVRH) voltage input pin

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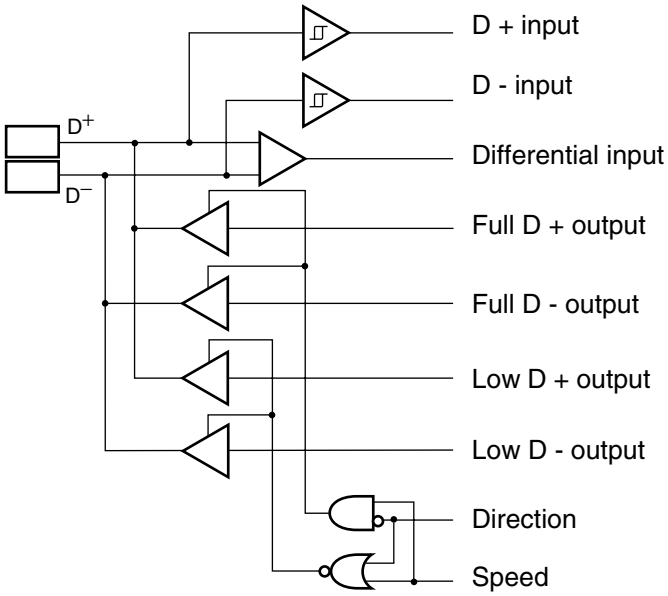
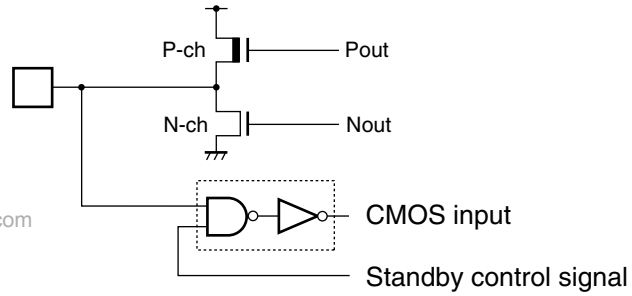
Type	Circuit	Remarks
K		USB I/O pin
L		• CMOS output • CMOS input • With standby control

■ HANDLING DEVICES

1. Preventing latch-up and turning on power supply

Latch-up may occur on CMOS IC under the following conditions:

- If a voltage higher than V_{CC} or lower than V_{SS} is applied to input and output pins.
- A voltage higher than the rated voltage is applied between V_{CC} pin and V_{SS} pin.
- If the AV_{CC} power supply is turned on before the V_{CC} voltage.

Ensure that you apply a voltage to the analog power supply at the same time as V_{CC} or after you turn on the digital power supply (when you perform power-off, turn off the analog power supply first or at the same time as V_{CC} and the digital power supply).

If latch-up occurs, the supply current increases rapidly, sometimes resulting in thermal breakdown of the device. Use meticulous care not to let any voltage exceed the maximum rating.

2. Treatment of unused pins

Leaving unused input pins unconnected can cause abnormal operation or latch-up, leading to permanent damage.
Unused input pins should always be pulled up or down through resistance of at least 2 kΩ. Any unused input/output pins may be set to output mode and left open, or set to input mode and treated the same as unused input pins. If there is unused output pin, make it to open.

3. Treatment of power supply pins on models with A/D converters

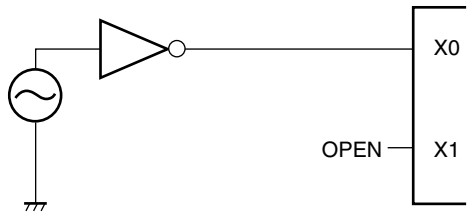
Even when the A/D converters are not in use, be sure to make the necessary connections AV_{CC} = AVRH = V_{CC}, and AV_{SS} = V_{SS}.

4. About the attention when the external clock is used

Even when using an external clock signal, an oscillation stabilization delay is applied after a power-on reset or when recovering from sub clock or stop mode. When suing an external clock, 25 MHz should be the upper frequency limit.

The following figure shows a sample use of external clock signals.

- Using external clock



5. Treatment of power supply pins (V_{CC}/V_{SS})

In products with multiple V_{CC} or V_{SS} pins, the pins of the same potential are internally connected in the device to avoid abnormal operations including latch-up. However, you must connect the pins to external power supply and a ground line to lower the electro-magnetic emission level, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating. Moreover, connect the current supply source with the V_{CC} and V_{SS} pins of this device at the low impedance.

It is also advisable to connect a ceramic bypass capacitor of approximately 0.1 μF between V_{CC} pin and V_{SS} pin near this device.

6. About Crystal oscillator circuit

Noise near the X0/X1 pins and X0A/X1A pins may cause the device to malfunction. Design the printed circuit board so that X0/X1 pins and X0A/X1A pins, the crystal oscillator (or the ceramic oscillator) and the bypass capacitor to ground are located as close to the device as possible.

It is strongly recommended to design the PC board artwork with the X0/X1 pins and X0A/X1A pins surrounded by ground plane because stable operation can be expected with such a layout.

Please ask the crystal maker to evaluate the oscillational characteristics of the crystal and this device.

7. Caution on Operations during PLL Clock Mode

On this microcontroller, if in case the crystal oscillator breaks off or an external reference clock input stops while the PLL clock mode is selected, a self-oscillator circuit contained in the PLL may continue its operation at its self-running frequency. However, Fujitsu will not guarantee results of operations if such failure occurs.

8. Stabilization of supply voltage

A sudden change in the supply voltage may cause the device to malfunction even within the V_{CC} supply voltage operating range. For stabilization reference, the supply voltage should be stabilized so that V_{CC} ripple variations (peak-to-peak value) at commercial frequencies (50 Hz/60 Hz) fall below 10% of the standard V_{CC} supply voltage and the transient regulation does not exceed 0.1 V/ms at temporary changes such as power supply switching.

9. When the dual-supply is used as a single-supply device

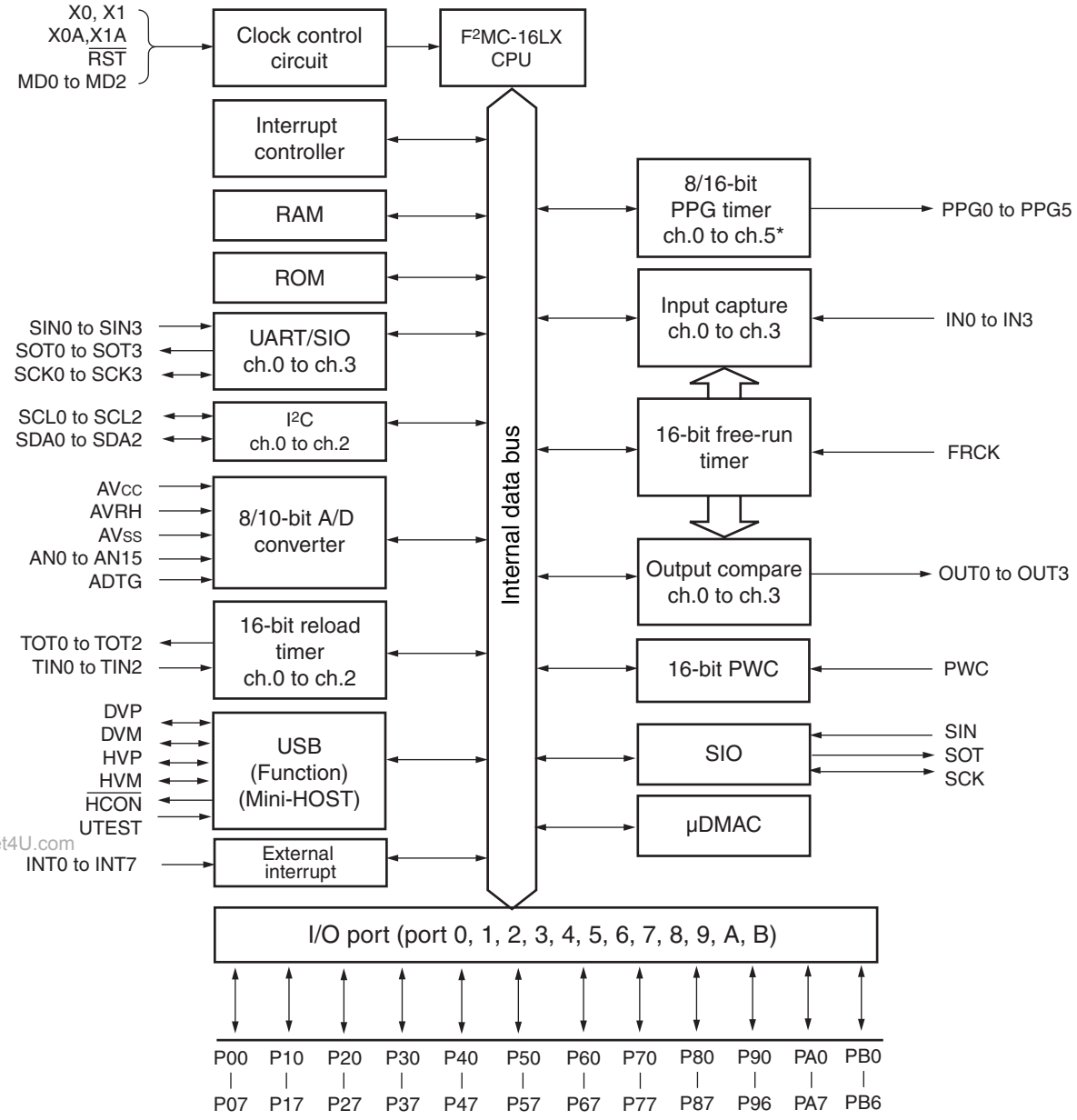
If you are using only a single-system of the MB90330A series that come in the dual-system product, use it with X0A = V_{SS} : X1A = OPEN.

10. Writing to flash memory

For serial writing to flash memory, always make sure that the operating voltage V_{CC} is between 3.13 V and 3.6 V.

For normal writing to flash memory, always make sure that the operating voltage V_{CC} is between 3.0 V and 3.6 V.

■ BLOCK DIAGRAM

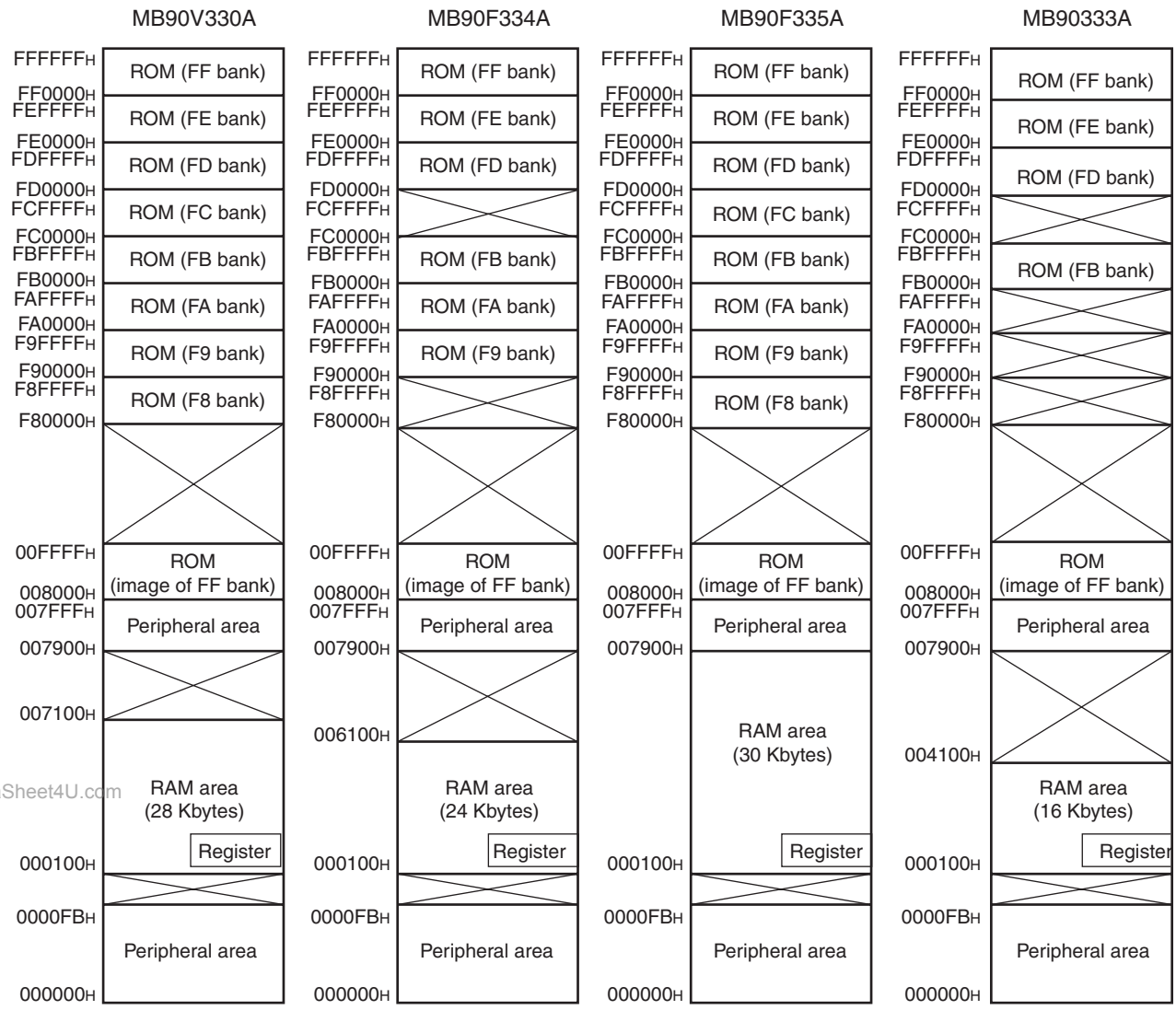


* : Channel for use in 8-bit mode. 3 channels (ch.1, ch.3, ch.5) are used in 16-bit mode.

Note : I/O ports share pins with peripheral function (resources) .
For details, refer to "■ PIN ASSIGNMENT" and "■ PIN DESCRIPTION".
Note also that pins used for peripheral function (resources) cannot serve as I/O ports.

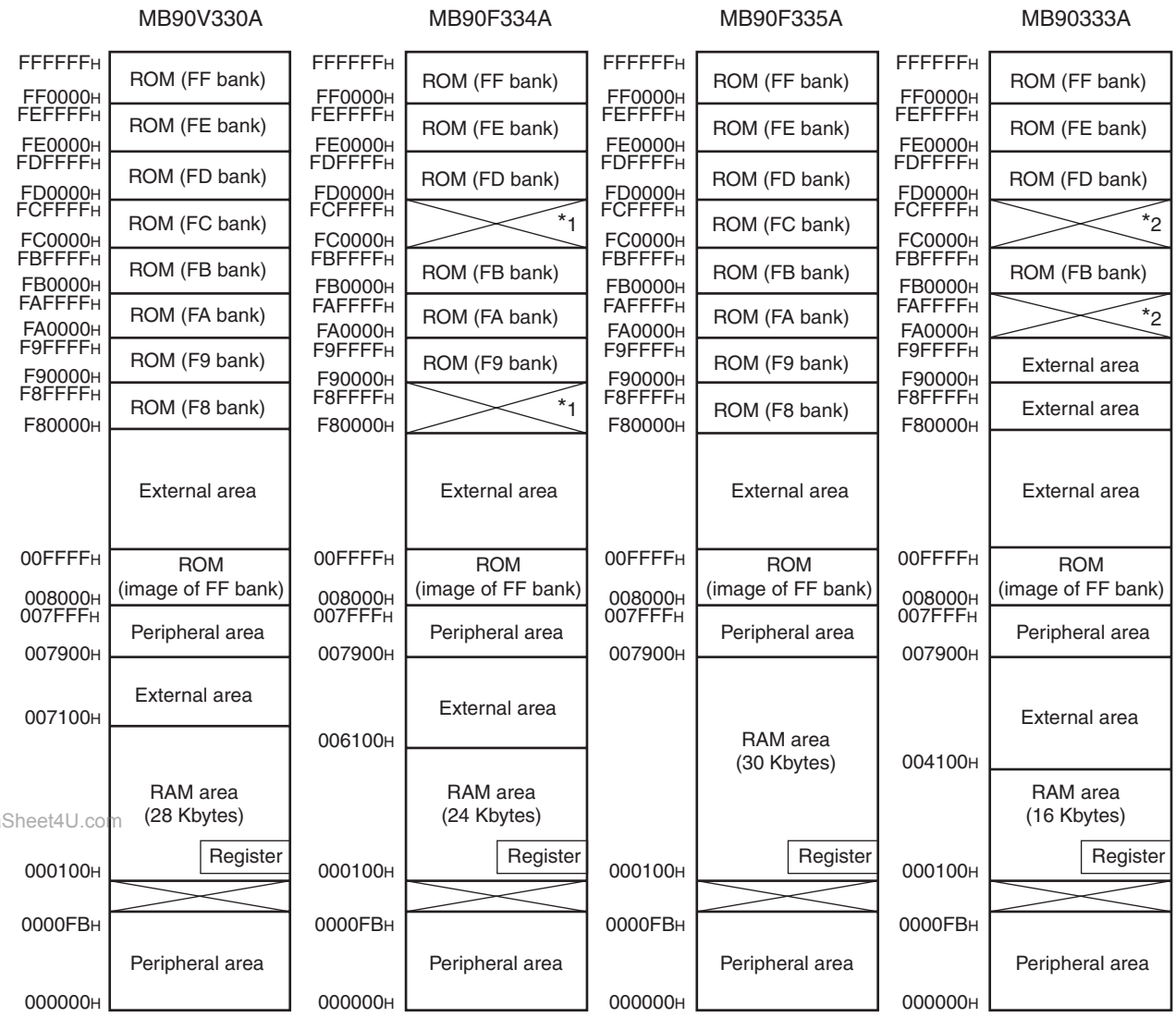
■ MEMORY MAP

Single chip mode (with ROM mirror function)



Memory map of MB90330A series (1/3)

Internal ROM external bus mode (with ROM mirror function)

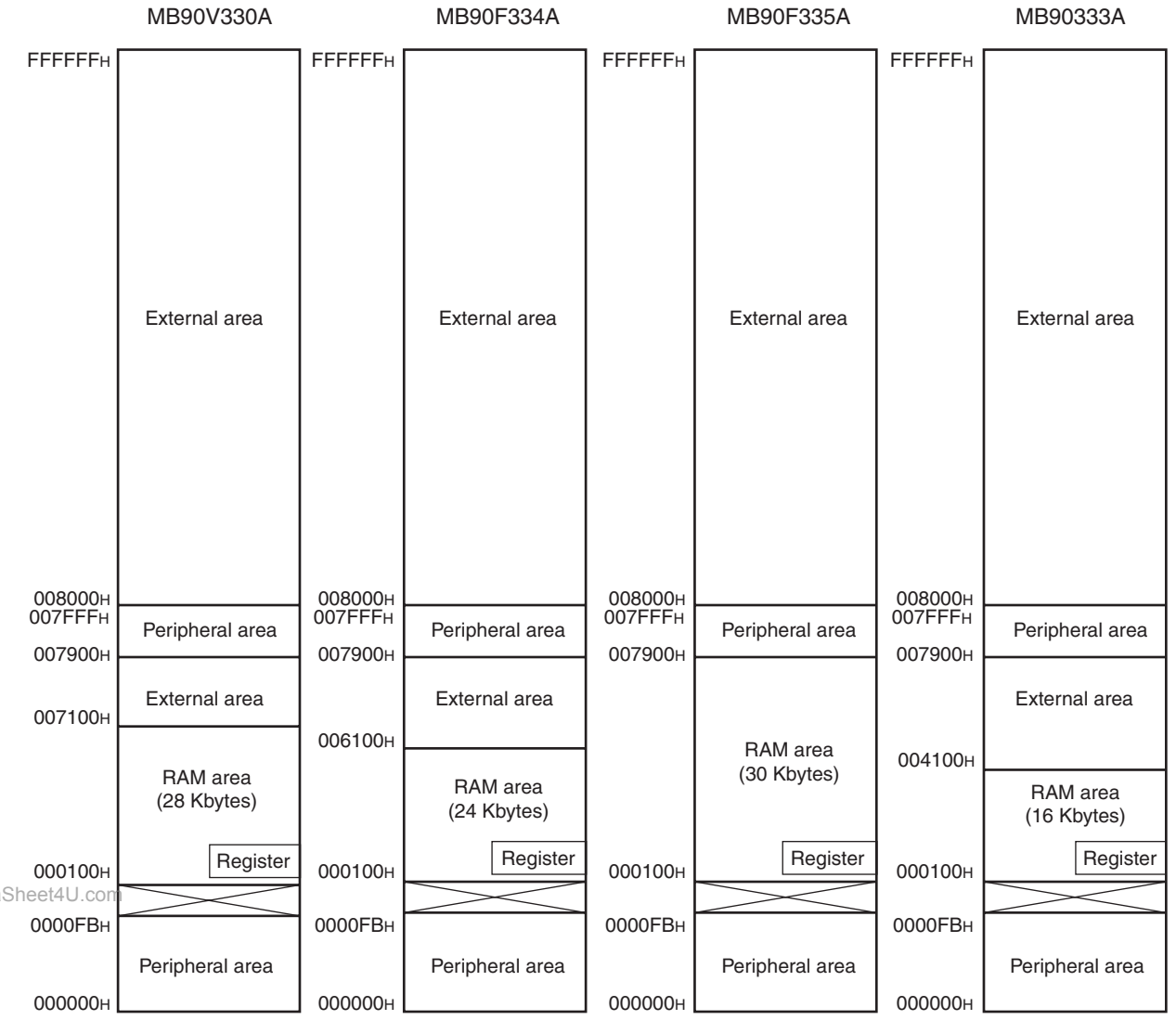


*1 : In the area of F80000H to F8FFFFH and FC0000H to FCFFFFH at MB90F334A, a value of “1” is read at read operating.

*2 : In the area of FA0000H to FAFFFFH and FC0000H to FCFFFFH at MB90333A, a value of “1” is read at read operating.

Memory map of MB90330A series (2/3)

External ROM external bus mode

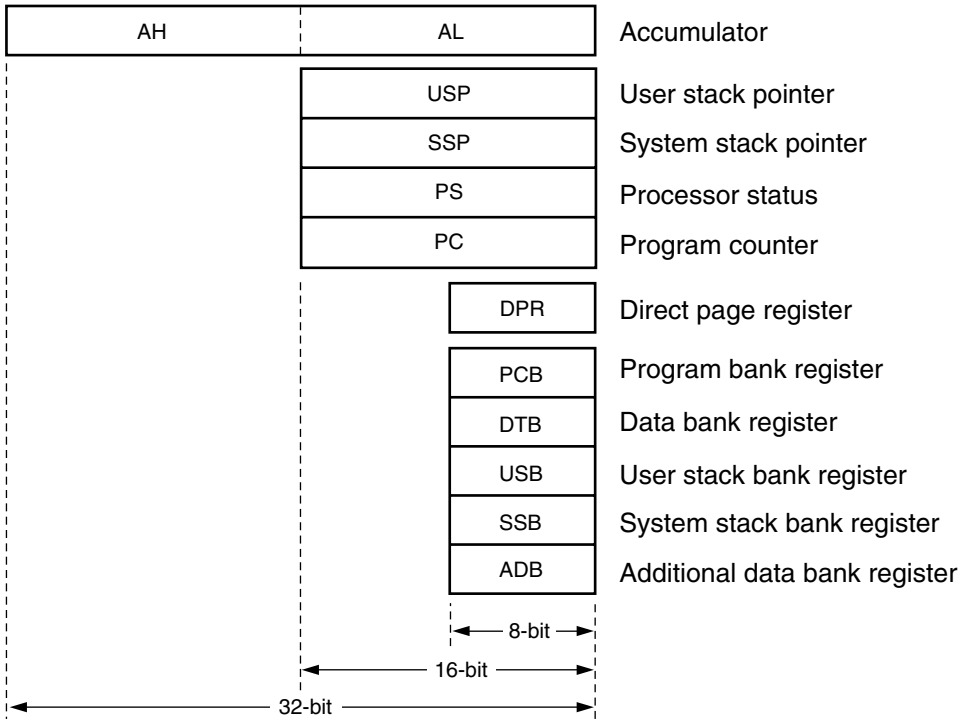


Memory map of MB90330A series (3/3)

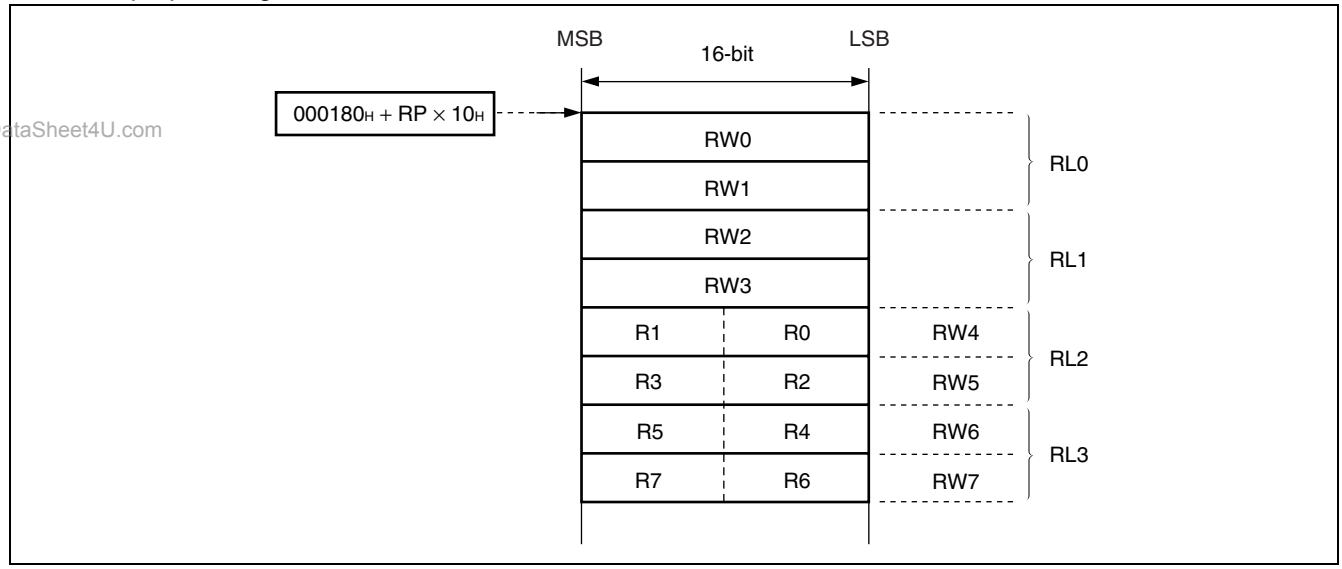
Notes:
- When the ROM mirror function register has been set, the mirror image data at higher addresses ("FF8000H to FFFFFFH") of bank FF is visible from the higher addresses ("008000H to 00FFFFH") of bank 00.
- The ROM mirror function is effective for using the C compiler small model.
- The lower 16-bit addresses of bank FF are equivalent to those of bank 00. Since the ROM area in bank FF exceeds 48 Kbytes, however, the mirror image of all the data in the ROM area cannot be reproduced in bank 00.
- When the C compiler small model is used, the data table mirror image can be shown at "008000H to 00FFFFH" by storing the data table at "FF8000H to FFFFFFH". Therefore, data tables in the ROM area can be referred without declaring the far addressing with the pointer.
- MB90F335A has the larger size of RAM area than MB90V330A, so that the emulation memory area needs to be set in the tools for a larger size of emulation area than 007100H.
  For details of setting, please refer to "Notes on Debug Environment Setting for MB90330A Series" by clicking "Application note" at the following URL.
  http://edevice.fujitsu.com/micom/en-support/
- 3 cycles are required to access to the emulation memory area (007100H to 0078FFH), which is 1 cycle more than to the mounted RAM area.

■ F²MC-16L CPU PROGRAMMING MODEL

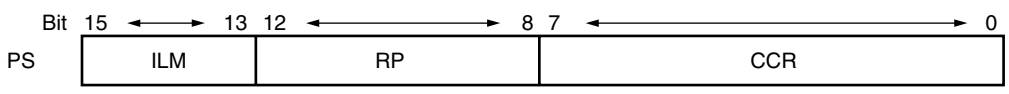
• Dedicated register



• General purpose register



• Processor status



■ I/O MAP

Address	Register abbreviation	Register	Read/ Write	Resource name	Initial Value
000000H	PDR0	Port 0 Data Register	R/W	Port 0	XXXXXXXXB
000001H	PDR1	Port 1 Data Register	R/W	Port 1	XXXXXXXXB
000002H	PDR2	Port 2 Data Register	R/W	Port 2	XXXXXXXXB
000003H	PDR3	Port 3 Data Register	R/W	Port 3	XXXXXXXXB
000004H	PDR4	Port 4 Data Register	R/W	Port 4	XXXXXXXXB
000005H	PDR5	Port 5 Data Register	R/W	Port 5	XXXXXXXXB
000006H	PDR6	Port 6 Data Register	R/W	Port 6	XXXXXXXXB
000007H	PDR7	Port 7 Data Register	R/W	Port 7	XXXXXXXXB
000008H	PDR8	Port 8 Data Register	R/W	Port 8	XXXXXXXXB
000009H	PDR9	Port 9 Data Register	R/W	Port 9	- XXXXXXXB
00000AH	PDRA	Port A Data Register	R/W	Port A	XXXXXXXXB
00000BH	Prohibited				
00000CH	PDRB	Port B Data Register	R/W	Port B	- XXXXXXXB
00000DH	DDRB	Port B Direction Register	R/W	Port B	- 0 0 0 0 0 0 0B
00000EH	Prohibited				
00000FH					
000010H	DDR0	Port 0 Direction Register	R/W	Port 0	0 0 0 0 0 0 0 0B
000011H	DDR1	Port 1 Direction Register	R/W	Port 1	0 0 0 0 0 0 0 0B
000012H	DDR2	Port 2 Direction Register	R/W	Port 2	0 0 0 0 0 0 0 0B
000013H	DDR3	Port 3 Direction Register	R/W	Port 3	0 0 0 0 0 0 0 0B
000014H	DDR4	Port 4 Direction Register	R/W	Port 4	0 0 0 0 0 0 0 0B
000015H	DDR5	Port 5 Direction Register	R/W	Port 5	0 0 0 0 0 0 0 0B
000016H	DDR6	Port 6 Direction Register	R/W	Port 6	0 0 0 0 0 0 0 0B
000017H	DDR7	Port 7 Direction Register	R/W	Port 7	0 0 0 0 0 0 0 0B
000018H	DDR8	Port 8 Direction Register	R/W	Port 8	0 0 0 0 0 0 0 0B
000019H	DDR9	Port 9 Direction Register	R/W	Port 9	- 0 0 0 0 0 0 0B
00001AH	DDRA	Port A Direction Register	R/W	Port A	0 0 0 0 0 0 0 0B
00001BH	ODR4	Port 4 Output Pin Register	R/W	Port 4 (open drain control)	0 0 0 0 0 0 0 0B
00001CH	RDR0	Port 0 Pull-up Resistance Register	R/W	Port 0 (PULL-UP)	0 0 0 0 0 0 0 0B
00001DH	RDR1	Port 1 Pull-up Resistance Register	R/W	Port 1 (PULL-UP)	0 0 0 0 0 0 0 0B
00001EH	ADER0	Analog Input Enable Register 0	R/W	Port 7, 8, A/D	1 1 1 1 1 1 1 1B
00001FH	ADER1	Analog Input Enable Register 1	R/W	Port 7, 8, A/D	1 1 1 1 1 1 1 1B
000020H	SMR0	Serial Mode Register 0	R/W	UART0	0 0 1 0 0 0 0 0B
000021H	SCR0	Serial Control Register 0	R/W		0 0 0 0 0 1 0 0B
000022H	SIDR0	Serial Input Data Register 0	R		XXXXXXXXB
	SODR0	Serial Output Data Register 0	W		
000023H	SSR0	Serial Status Register 0	R/W		0 0 0 0 1 0 0 0B
000024H	UTRLR0	UART Prescaler Reload Register 0	R/W	Communication Prescaler (UART0)	0 0 0 0 0 0 0 0B
000025H	UTCR0	UART Prescaler Control Register 0	R/W		0 0 0 0 - 0 0 0B

(Continued)

Address	Register abbreviation	Register	Read/ Write	Resource name	Initial Value
000026H	SMR1	Serial Mode Register 1	R/W	UART1	0 0 1 0 0 0 0 0B
000027H	SCR1	Serial Control Register 1	R/W		0 0 0 0 0 1 0 0B
000028H	SIDR1	Serial Input Data Register 1	R		XXXXXXXXB
	SODR1	Serial Output Data Register 1	W		
000029H	SSR1	Serial Status Register 1	R/W		0 0 0 0 1 0 0 0B
00002AH	UTRLR1	UART Prescaler Reload Register 1	R/W	Communication Prescaler (UART1)	0 0 0 0 0 0 0 0B
00002BH	UTCR1	UART Prescaler Control Register 1	R/W		0 0 0 0 - 0 0 0B
00002CH	SMR2	Serial Mode Register 2	R/W	UART2	0 0 1 0 0 0 0 0B
00002DH	SCR2	Serial Control Register 2	R/W		0 0 0 0 0 1 0 0B
00002EH	SIDR2	Serial Input Data Register 2	R		XXXXXXXXB
	SODR2	Serial Output Data Register 2	W		
00002FH	SSR2	Serial Status Register 2	R/W		0 0 0 0 1 0 0 0B
000030H	UTRLR2	UART Prescaler Reload Register 2	R/W	Communication Prescaler (UART2)	0 0 0 0 0 0 0 0B
000031H	UTCR2	UART Prescaler Control Register 2	R/W		0 0 0 0 - 0 0 0B
000032H	SMR3	Serial Mode Register 3	R/W	UART3	0 0 1 0 0 0 0 0B
000033H	SCR3	Serial Control Register 3	R/W		0 0 0 0 0 1 0 0B
000034H	SIDR3	Serial Input Data Register 3	R		XXXXXXXXB
	SODR3	Serial Output Data Register 3	W		
000035H	SSR3	Serial Status Register 3	R/W		0 0 0 0 1 0 0 0B
000036H	UTRLR3	UART Prescaler Reload Register 3	R/W	Communication Prescaler (UART3)	0 0 0 0 0 0 0 0B
000037H	UTCR3	UART Prescaler Control Register 3	R/W		0 0 0 0 - 0 0 0B
000038H to 00003BH	Prohibited				
00003CH	ENIR	DTP/Interrupt Enable Register	R/W	DTP/External Interrupt	0 0 0 0 0 0 0 0B
00003DH	EIRR	DTP/Interrupt Source Register	R/W		0 0 0 0 0 0 0 0B
00003EH	ELVR	Request Level Setting Register Lower	R/W		0 0 0 0 0 0 0 0B
00003FH		Request Level Setting Register Upper	R/W		0 0 0 0 0 0 0 0B
000040H	ADCS0	A/D Control Status Register Lower	R/W	8/10-bit A/D Converter	0 0 - - - - - 0B
000041H	ADCS1	A/D Control Status Register Upper	R/W		0 0 0 0 0 0 0 0B
000042H	ADCR0	A/D Data Register Lower	R/W		XXXXXXXXB
000043H	ADCR1	A/D Data Register Upper	R/W		0 0 1 0 1 XXXB
000044H	Prohibited				
000045H	ADMR	A/D Conversion Channel Selection Register	R/W	8/10-bit A/D Converter	0 0 0 0 0 0 0 0B
000046H	PPGC0	PPG0 Operation Mode Control Register	R/W	PPG ch.0	0X0 0 0XX1B
000047H	PPGC1	PPG1 Operation Mode Control Register	R/W	PPG ch.1	0X0 0 0 0 0 1B
000048H	PPGC2	PPG2 Operation Mode Control Register	R/W	PPG ch.2	0X0 0 0XX1B

(Continued)

Address	Register abbreviation	Register	Read/ Write	Resource name	Initial Value
000049H	PPGC3	PPG3 Operation Mode Control Register	R/W	PPG ch.3	0X0 0 0 0 0 1B
00004AH	PPGC4	PPG4 Operation Mode Control Register	R/W	PPG ch.4	0X0 0 0XX1B
00004BH	PPGC5	PPG5 Operation Mode Control Register	R/W	PPG ch.5	0X0 0 0 0 0 1B
00004CH	PPG01	PPG0 and PPG1 Output Control Register	R/W	PPG ch.0/ch.1	0 0 0 0 0 0XXB
00004DH	Prohibited				
00004EH	PPG23	PPG2 and PPG3 Output Control Register	R/W	PPG ch.2/ch.3	0 0 0 0 0 0 XXB
00004FH	Prohibited				
000050H	PPG45	PPG4 and PPG5 Output Control Register	R/W	PPG ch.4/ch.5	0 0 0 0 0 0 XXB
000051H	Prohibited				
000052H	ICS01	Input Capture Control Status Register 01	R/W	Input Capture ch.0/ch.1	0 0 0 0 0 0 0 0B
000053H	ICS23	Input Capture Control Status Register 23	R/W	Input Capture ch.2/ch.3	0 0 0 0 0 0 0 0B
000054H	OCS0	Output Compare Control Register ch.0 Lower	R/W	Output Compare ch.0/ch.1	0 0 0 0 - - 0 0B
000055H	OCS1	Output Compare Control Register ch.1 Upper	R/W		- - - 0 0 0 0 0B
000056H	OCS2	Output Compare Control Register ch.2 Lower	R/W	Output Compare ch.2/ch.3	0 0 0 0 - - 0 0B
000057H	OCS3	Output Compare Control Register ch.3 Upper	R/W		- - - 0 0 0 0 0B
000058H	SMCS	Serial Mode Control Status Register	R/W	Extended Serial I/O	XXXX0 0 0 0B
000059H					0 0 0 0 0 0 1 0B
00005AH	SDR	Serial Data Register	R/W		XXXXXXXXB
00005BH	SDCR	Communication Prescaler Control Register	R/W	Communication Prescaler	0XXX0 0 0 0B
00005CH	PWCSR	PWC Control Status Register	R/W	16-bit PWC Timer	0 0 0 0 0 0 0 0B
00005DH					0 0 0 0 0 0 0 XB
00005EH	PWCR	PWC Data Buffer Register	R/W		0 0 0 0 0 0 0 0B
00005FH					0 0 0 0 0 0 0 0B
000060H	DIVR	PWC Dividing Ratio Control Register	R/W		- - - - - - 0 0B
000061H	Prohibited				
000062H	TMCSR0	Timer Control Status Register 0	R/W	16-bit Reload Timer ch.0	0 0 0 0 0 0 0 0B
000063H					XXXX 0 0 0 0B
000064H	TMR0	16-bit Timer Register 0 Lower	R		XXXXXXXXB
	TMRLR0	16-bit Reload Register 0 Lower	W		XXXXXXXXB
000065H	TMR0	16-bit Timer Register 0 Upper	R		XXXXXXXXB
	TMRLR0	16-bit Reload Register 0 Upper	W		XXXXXXXXB

(Continued)

Address	Register abbreviation	Register	Read/ Write	Resource name	Initial Value
000066H	TMCSR1	Timer Control Status Register 1	R/W	16-bit Reload Timer ch.1	0 0 0 0 0 0 0 0B
000067H					XXXX 0 0 0 0B
000068H	TMR1	16-bit Timer Register 1 Lower	R		XXXXXXXXB
	TMRLR1	16-bit Reload Register 1 Lower	W		XXXXXXXXB
000069H	TMR1	16-bit Timer Register 1 Upper	R		XXXXXXXXB
	TMRLR1	16-bit Reload Register 1 Upper	W		XXXXXXXXB
00006AH	TMCSR2	Timer Control Status Register 2	R/W	16-bit Reload Timer ch.2	0 0 0 0 0 0 0 0B
00006BH					XXXX 0 0 0 0B
00006CH	TMR2	16-bit Timer Register 2 Lower	R		XXXXXXXXB
	TMRLR2	16-bit Reload Register 2 Lower	W		XXXXXXXXB
00006DH	TMR2	16-bit Timer Register 2 Upper	R		XXXXXXXXB
	TMRLR2	16-bit Reload Register 2 Upper	W		XXXXXXXXB
00006EH	Prohibited				
00006FH	ROMM	ROM Mirror Function Selection Register	W	ROM Mirror Function Selection Module	- - - - - - 1 1B
000070H	IBSR0	I²C Bus Status Register 0	R	I²C Bus Interface ch.0	0 0 0 0 0 0 0 0B
000071H	IBCR0	I²C Bus Control Register 0	R/W		0 0 0 0 0 0 0 0B
000072H	ICCR0	I²C Bus Clock Control Register 0	R/W		XX 0 XXXXXB
000073H	IADR0	I²C Bus Address Register 0	R/W		XXXXXXXXB
000074H	IDAR0	I²C Bus Data Register 0	R/W		XXXXXXXXB
000075H	Prohibited				
000076H	IBSR1	I²C Bus Status Register 1	R	I²C Bus Interface ch.1	0 0 0 0 0 0 0 0B
000077H	IBCR1	I²C Bus Control Register 1	R/W		0 0 0 0 0 0 0 0B
000078H	ICCR1	I²C Bus Clock Control Register 1	R/W		XX 0 XXXXXB
000079H	IADR1	I²C Bus Address Register 1	R/W		XXXXXXXXB
00007AH	IDAR1	I²C Bus Data Register 1	R/W		XXXXXXXXB
00007BH	Prohibited				
00007CH	IBSR2	I²C Bus Status Register 2	R	I²C Bus Interface ch.2	0 0 0 0 0 0 0 0B
00007DH	IBCR2	I²C Bus Control Register 2	R/W		0 0 0 0 0 0 0 0B
00007EH	ICCR2	I²C Bus Clock Control Register 2	R/W		XX 0 XXXXXB
00007FH	IADR2	I²C Bus Address Register 2	R/W		XXXXXXXXB
000080H	IDAR2	I²C Bus Data Register 2	R/W		XXXXXXXXB
000081H to 000085H	Prohibited				

(Continued)

Address	Register abbreviation	Register	Read/ Write	Resource name	Initial Value
000086H	TCDT	Timer Data Register Lower	R/W	16-bit Free-Run Timer	0 0 0 0 0 0 0 0B
000087H		Timer Data Register Upper	R/W		0 0 0 0 0 0 0 0B
000088H	TCCS	Timer Control Status Register Lower	R/W		0 0 0 0 0 0 0 0B
000089H		Timer Control Status Register Upper	R/W		0 - - 0 0 0 0 0B
00008AH	CPCLR	Compare Clear Register Lower	R/W		XXXXXXXXB
00008BH		Compare Clear Register Upper	R/W		XXXXXXXXB
00008CH to 00009AH	Prohibited				
00009BH	DCSR	DMA Descriptor Channel Specification Register	R/W	µDMAC	0 0 0 0 0 0 0 0B
00009CH	DSRL	DMA Status Register Lower	R/W		0 0 0 0 0 0 0 0B
00009DH	DSRH	DMA Status Register Upper	R/W		0 0 0 0 0 0 0 0B
00009EH	PACSR	Program Address Detection Control Status Register	R/W	Address Match Detection	0 0 0 0 0 0 0 0B
00009FH	DIRR	Delay Interruption Factor Generation/ Release Register	R/W	Delay Interrupt	- - - - - - - 0B
0000A0H	LPMCR	Low Power Consumption Mode Control Register	R/W	Low Power Consumption Control Circuit	0 0 0 1 1 0 0 0B
0000A1H	CKSCR	Clock Selection Register	R/W	Clock	1 1 1 1 1 1 0 0B
0000A2H	Prohibited				
0000A3H					
0000A4H	DSSR	DMA Stop Status Register	R/W	µDMAC	0 0 0 0 0 0 0 0B
0000A5H	ARSR	Automatic Ready Function Selection Register	W	External Pin	0 0 1 1- - 0 0B
0000A6H	HACR	External Address Output Control Register	W		* * * * * * * * B
0000A7H	EPCR	Bus Control Signal Selection Register	W		1 0 0 0 * 1 0 -B
0000A8H	WDTC	Watchdog Timer Control Register	R/W	Watchdog Timer	X - XXX 1 1 1B
0000A9H	TBTC	Time-base Timer Control Register	R/W	Time-base Timer	1 - - 0 0 1 0 0B
0000AAH	WTC	Watch Timer Control Register	R/W	Watch Timer	1 0 0 0 1 0 0 0B
0000ABH	Prohibited				
0000ACH	DERL	DMA Enable Register Lower	R/W	µDMAC	0 0 0 0 0 0 0 0B
0000ADH	DERH	DMA Enable Register Upper	R/W		0 0 0 0 0 0 0 0B
0000AEH	FMCS	Flash Memory Control Status Register	R/W	Flash Memory I/F	0 0 0 X 0 0 0 0B
0000AFH	Prohibited				

(Continued)

Address	Register abbreviation	Register	Read/ Write	Resource name	Initial Value
0000B0H	ICR00	Interrupt Control Register 00	R/W	Interrupt Controller	0 0 0 0 0 1 1 1B
0000B1H	ICR01	Interrupt Control Register 01	R/W		0 0 0 0 0 1 1 1B
0000B2H	ICR02	Interrupt Control Register 02	R/W		0 0 0 0 0 1 1 1B
0000B3H	ICR03	Interrupt Control Register 03	R/W		0 0 0 0 0 1 1 1B
0000B4H	ICR04	Interrupt Control Register 04	R/W		0 0 0 0 0 1 1 1B
0000B5H	ICR05	Interrupt Control Register 05	R/W		0 0 0 0 0 1 1 1B
0000B6H	ICR06	Interrupt Control Register 06	R/W		0 0 0 0 0 1 1 1B
0000B7H	ICR07	Interrupt Control Register 07	R/W		0 0 0 0 0 1 1 1B
0000B8H	ICR08	Interrupt Control Register 08	R/W		0 0 0 0 0 1 1 1B
0000B9H	ICR09	Interrupt Control Register 09	R/W		0 0 0 0 0 1 1 1B
0000BAH	ICR10	Interrupt Control Register 10	R/W		0 0 0 0 0 1 1 1B
0000BBH	ICR11	Interrupt Control Register 11	R/W		0 0 0 0 0 1 1 1B
0000BCH	ICR12	Interrupt Control Register 12	R/W		0 0 0 0 0 1 1 1B
0000BDH	ICR13	Interrupt Control Register 13	R/W		0 0 0 0 0 1 1 1B
0000BEH	ICR14	Interrupt Control Register 14	R/W		0 0 0 0 0 1 1 1B
0000BFH	ICR15	Interrupt Control Register 15	R/W		0 0 0 0 0 1 1 1B
0000C0H	HCNT0	Host Control Register 0	R/W	USB Mini-HOST	0 0 0 0 0 0 0 0B
0000C1H	HCNT1	Host Control Register 1	R/W		0 0 0 0 0 0 0 1B
0000C2H	HIRQ	Host Interruption Register	R/W		0 0 0 0 0 0 0 0B
0000C3H	HERR	Host Error Status Register	R/W		0 0 0 0 0 0 1 1B
0000C4H	HSTATE	Host State Status Register	R/W		XX 0 1 0 0 1 0B
0000C5H	HFCOMP	SOF Interrupt FRAME Compare Register	R/W		0 0 0 0 0 0 0 0B
0000C6H	HRTIMER	Retry Timer Setting Register	R/W		0 0 0 0 0 0 0 0B
0000C7H			R/W		0 0 0 0 0 0 0 0B
0000C8H			R/W		XXXXXX 0 0B
0000C9H	HADR	Host Address Register	R/W		X 0 0 0 0 0 0 0B
0000CAH	HEOF	EOF Setting Register	R/W		0 0 0 0 0 0 0 0B
0000CBH			R/W		XX 0 0 0 0 0 0B
0000CCH	HFRAME	FRAME Setting Register	R/W		0 0 0 0 0 0 0 0B
0000CDH			R/W		XXXXX 0 0 0B
0000CEH	HTOKEN	Host Token End Point Register	R/W		0 0 0 0 0 0 0 0B
0000CFH	Prohibited				
0000D0H	UDCC	UDC Control Register	R/W	USB Function	1 0 1 0 0 0 0 0B
0000D1H			R/W		0 0 0 0 0 0 0 0B

(Continued)

Address	Register abbreviation	Register	Read/ Write	Resource name	Initial Value
0000D2H	EP0C	EP0 Control Register	R/W	USB Function	0 1 0 0 0 0 0 0B
0000D3H			R/W		XXXX 0 0 0 0B
0000D4H	EP1C	EP1 Control Register	R/W		0 0 0 0 0 0 0 0B
0000D5H			R/W		0 1 1 0 0 0 0 1B
0000D6H	EP2C	EP2 Control Register	R/W		0 1 0 0 0 0 0 0B
0000D7H			R/W		0 1 1 0 0 0 0 0B
0000D8H	EP3C	EP3 Control Register	R/W		0 1 0 0 0 0 0 0B
0000D9H			R/W		0 1 1 0 0 0 0 0B
0000DAH	EP4C	EP4 Control Register	R/W		0 1 0 0 0 0 0 0B
0000DBH			R/W		0 1 1 0 0 0 0 0B
0000DCH	EP5C	EP5 Control Register	R/W		0 1 0 0 0 0 0 0B
0000DDH			R/W		0 1 1 0 0 0 0 0B
0000DEH	TMSP	Time Stamp Register	R		0 0 0 0 0 0 0 0B
0000DFH			R		XXXXX0 0 0B
0000E0H	UDCS	UDC Status Register	R/W		XX0 0 0 0 0 0B
0000E1H	UDCIE	UDC Interrupt Enable Register	R/W, R		0 0 0 0 0 0 0 0B
0000E2H	EP0IS	EP0I Status Register	R/W		XXXXXXXXB
0000E3H			R/W		1 0 XXX 1 XXB
0000E4H	EP0OS	EP0O Status Register	R/W, R		0 XXXXXXXB
0000E5H			R/W		1 0 0 XX 0 0 0B
0000E6H	EP1S	EP1 Status Register	R		XXXXXXXXB
0000E7H			R/W, R		1 0 0 0 0 0 0 XB
0000E8H	EP2S	EP2 Status Register	R		XXXXXXXXB
0000E9H			R/W, R		1 0 0 0 0 0 0 0B
0000EAH	EP3S	EP3 Status Register	R		XXXXXXXXB
0000EBH			R/W, R		1 0 0 0 0 0 0 0B
0000ECH	EP4S	EP4 Status Register	R		XXXXXXXXB
0000EDH			R/W, R		1 0 0 0 0 0 0 0B
0000EEH	EP5S	EP5 Status Register	R		XXXXXXXXB
0000EFH			R/W, R		1 0 0 0 0 0 0 0B
0000F0H	EP0DT	EP0 Data Register	R/W		XXXXXXXXB
0000F1H			R/W		XXXXXXXXB
0000F2H	EP1DT	EP1 Data Register	R/W		XXXXXXXXB
0000F3H			R/W		XXXXXXXXB
0000F4H	EP2DT	EP2 Data Register	R/W		XXXXXXXXB
0000F5H			R/W		XXXXXXXXB
0000F6H	EP3DT	EP3 Data Register	R/W		XXXXXXXXB
0000F7H			R/W		XXXXXXXXB

(Continued)

Address	Register abbreviation	Register	Read/ Write	Resource name	Initial Value
0000F8H	EP4DT	EP4 Data Register	R/W	USB Function	XXXXXXXXB
0000F9H			R/W		XXXXXXXXB
0000FAH	EP5DT	EP5 Data Register	R/W		XXXXXXXXB
0000FBH			R/W		XXXXXXXXB
0000FCH to 0000FFH	Prohibited				
000100H to #H	RAM Area				
001FF0H	PADR0	Program Address Detection Register ch.0 Lower	R/W	Address Match Detection	XXXXXXXXB
001FF1H		Program Address Detection Register ch.0 Middle	R/W		XXXXXXXXB
001FF2H		Program Address Detection Register ch.0 Upper	R/W		XXXXXXXXB
001FF3H	PADR1	Program Address Detection Register ch.1 Lower	R/W		XXXXXXXXB
001FF4H		Program Address Detection Register ch.1 Middle	R/W		XXXXXXXXB
001FF5H		Program Address Detection Register ch.1 Upper	R/W		XXXXXXXXB
#H to 0078FFH	Unused Area				
007900H	PRLL0	PPG Reload Register Lower ch.0	R/W	PPG ch.0	XXXXXXXXB
007901H	PRLH0	PPG Reload Register Upper ch.0	R/W		XXXXXXXXB
007902H	PRLL1	PPG Reload Register Lower ch.1	R/W	PPG ch.1	XXXXXXXXB
007903H	PRLH1	PPG Reload Register Upper ch.1	R/W		XXXXXXXXB
007904H	PRLL2	PPG Reload Register Lower ch.2	R/W	PPG ch.2	XXXXXXXXB
007905H	PRLH2	PPG Reload Register Upper ch.2	R/W		XXXXXXXXB
007906H	PRLL3	PPG Reload Register Lower ch.3	R/W	PPG ch.3	XXXXXXXXB
007907H	PRLH3	PPG Reload Register Upper ch.3	R/W		XXXXXXXXB
007908H	PRLL4	PPG Reload Register Lower ch.4	R/W	PPG ch.4	XXXXXXXXB
007909H	PRLH4	PPG Reload Register Upper ch.4	R/W		XXXXXXXXB
00790AH	PRLL5	PPG Reload Register Lower ch.5	R/W	PPG ch.5	XXXXXXXXB
00790BH	PRLH5	PPG Reload Register Upper ch.5	R/W		XXXXXXXXB
00790CH to 00790FH	Prohibited				

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Address	Register abbreviation	Register	Read/ Write	Resource name	Initial Value
007910H	IPCP0	Input Capture Data Register Lower ch.0	R	Input Capture ch.0/ch.1	XXXXXXXXB
007911H		Input Capture Data Register Upper ch.0	R		XXXXXXXXB
007912H	IPCP1	Input Capture Data Register Lower ch.1	R		XXXXXXXXB
007913H		Input Capture Data Register Upper ch.1	R		XXXXXXXXB
007914H	IPCP2	Input Capture Data Register Lower ch.2	R	Input Capture ch.2/ch.3	XXXXXXXXB
007915H		Input Capture Data Register Upper ch.2	R		XXXXXXXXB
007916H	IPCP3	Input Capture Data Register Lower ch.3	R		XXXXXXXXB
007917H		Input Capture Data Register Upper ch.3	R		XXXXXXXXB
007918H	OCCP0	Output Compare Register Lower ch.0	R/W	Output Compare ch.0/ch.1	XXXXXXXXB
007919H		Output Compare Register Upper ch.0	R/W		XXXXXXXXB
00791AH	OCCP1	Output Compare Register Lower ch.1	R/W		XXXXXXXXB
00791BH		Output Compare Register Upper ch.1	R/W		XXXXXXXXB
00791CH	OCCP2	Output Compare Register Lower ch.2	R/W	Output Compare ch.2/ch.3	XXXXXXXXB
00791DH		Output Compare Register Upper ch.2	R/W		XXXXXXXXB
00791EH	OCCP3	Output Compare Register Lower ch.3	R/W		XXXXXXXXB
00791FH		Output Compare Register Upper ch.3	R/W		XXXXXXXXB
007920H	DBAPL	DMA Buffer Address Pointer Lower 8-bit	R/W	μDMAC	XXXXXXXXB
007921H	DBAPM	DMA Buffer Address Pointer Middle 8-bit	R/W		XXXXXXXXB
007922H	DBAPH	DMA Buffer Address Pointer Upper 8-bit	R/W		XXXXXXXXB
007923H	DMACS	DMA Control Register	R/W		XXXXXXXXB
007924H	DIOAL	DMA I/O Register Address Pointer Lower 8-bit	R/W		XXXXXXXXB
007925H	DIOAH	DMA I/O Register Address Pointer Upper 8-bit	R/W		XXXXXXXXB
007926H	DDCTL	DMA Data Counter Lower 8-bit	R/W		XXXXXXXXB
007927H	DDCTH	DMA Data Counter Upper 8-bit	R/W		XXXXXXXXB
007928H to 007FFFH	Prohibited				

- Explanation on read/write
  - R/W : Readable / Writable
  - R : Read only
  - W : Write only

- Explanation on initial values
  - 0 : Initial value is “0”.
  - 1 : Initial value is “1”.
  - X : Initial value is undefined.
  - - : Initial value is undefined (None) .
  - * : Initial value of this bit is “1” or “0”.

Note : No I/O instruction can be used for registers located between 007900H and 007FFFH.

■ INTERRUPT SOURCES, INTERRUPT VECTORS, AND INTERRUPT CONTROL REGISTERS

Interrupt source	EI²OS support	μDMAC	Interrupt vector			Interrupt control register		Priority
			Number*1		Address	ICR	Address	
Reset	×	×	#08	08H	FFFFDCH	—	—	High
INT 9 instruction	×	×	#09	09H	FFFFD8H	—	—	
Exceptional treatment	×	×	#10	0AH	FFFFD4H	—	—	
USB Function1	×	0, 1	#11	0BH	FFFFD0H	ICR00	0000B0H	
USB Function2	×	2 to 6*2	#12	0CH	FFFFCCH			
USB Function3	×	×	#13	0DH	FFFFC8H	ICR01	0000B1H	
USB Function4	×	×	#14	0EH	FFFFC4H			
USB Mini-HOST1	×	×	#15	0FH	FFFFC0H	ICR02	0000B2H	
USB Mini-HOST2	×	×	#16	10H	FFFFBCH			
I²C ch.0	×	×	#17	11H	FFFFB8H	ICR03	0000B3H	
DTP/External interrupt ch.0/ch.1	○	×	#18	12H	FFFFB4H			
I²C ch.1	×	×	#19	13H	FFFFB0H	ICR04	0000B4H	
DTP/External interrupt ch.2/ch.3	○	×	#20	14H	FFFFACH			
I²C ch.2	×	×	#21	15H	FFFFA8H	ICR05	0000B5H	
DTP/External interrupt ch.4/ch.5	○	×	#22	16H	FFFFA4H			
PWC/Reload timer ch.0	△	14	#23	17H	FFFFA0H	ICR06	0000B6H	
DTP/External interrupt ch.6/ch.7	△	×	#24	18H	FFFF9CH			
Input capture ch.0/ch.1	△	7	#25	19H	FFFF98H	ICR07	0000B7H	
Reload timer ch.1	△	×	#26	1AH	FFFF94H			
Input capture ch.2/ch.3	△	8	#27	1BH	FFFF90H	ICR08	0000B8H	
Reload timer ch.2	△	×	#28	1CH	FFFF8CH			
Output compare ch.0/ch.1	○	×	#29	1DH	FFFF88H	ICR09	0000B9H	
PPG ch.0/ch.1	×	×	#30	1EH	FFFF84H			
Output compare ch.2/ch.3	○	×	#31	1FH	FFFF80H	ICR10	0000BAH	
PPG ch.2/ch.3	×	×	#32	20H	FFFF7CH			
UART (Send completed) ch.2/ch.3	○	11	#33	21H	FFFF78H	ICR11	0000BBH	
PPG ch.4/ch.5	×	×	#34	22H	FFFF74H			
UART (Reception completed) ch.2/ch.3	◎	10	#35	23H	FFFF70H	ICR12	0000BCH	
A/D converter/Free-run timer	△	15	#36	24H	FFFF6CH			
UART (Send completed) ch.0/ch.1	○	13	#37	25H	FFFF68H	ICR13	0000BDH	
Extended serial I/O	×	9	#38	26H	FFFF64H			
UART (Reception completed) ch.0/ch.1	◎	12	#39	27H	FFFF60H	ICR14	0000BEH	
Time-base timer/Watch timer	×	×	#40	28H	FFFF5CH			
Flash memory status	×	×	#41	29H	FFFF58H	ICR15	0000BFH	
Delay interrupt output module	×	×	#42	2AH	FFFF54H			Low

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◎ : Available, EI²OS stop function provided (The interrupt request flag is cleared by the interrupt clear signal. With a stop request).

○ : Available (The interrupt request flag is cleared by the interrupt clear signal.)

△ : Available when any interrupt source sharing ICR is not used.

× : Unavailable

*1 : If the same level interrupt is output simultaneously, the lower interrupt factor of interrupt vector number has priority.

*2 : ch.2 and 3 can also be used during Mini-HOST operation.

Notes :
- If the same interrupt control register (ICR) has two interrupt factors and the use of the EI²OS is permitted, the EI²OS is activated when either of the factors is detected. As any interrupt other than the activation factor is masked while the EI²OS is running, it is recommended that you should mask either of the interrupt requests when using the EI²OS.
- The interrupt flag is cleared by the EI²OS interrupt clear signal for the resource that has two interrupt factors in the same interrupt control register (ICR).
- If a resource has two interrupt sources for the same interrupt number, both of the interrupt request flags are cleared by the μDMAC interrupt clear signal. Therefore, when you use either of two interrupt factors for the DMAC function, another interrupt function is disabled. Set the interrupt request permission bit to “0” in the appropriate resource, and take measures by software polling.

• Content of USB interruption factor

USB interrupt factor	Details
USB function 1	End Point0-IN End Point0-OUT
USB function 2	End Point1-5 *
USB function 3	SUSP SOF BRST WKUP CONF
USB function 4	SPK
USB Mini-HOST1	DIRQ CNNIRQ URIRQ RWKIRQ
USB Mini-HOST2	SOFIRQ CMPIRQ

* : Endpoints 1 and 2 can also be used during Mini-HOST operation.

■ PERIPHERAL RESOURCES

1. I/O port

The I/O ports are used as general-purpose input/output ports (parallel I/O ports). MB90330A series model is provided with 12 ports (94 inputs) . The ports function as input/output pins for peripheral functions also.

The port data register (PDR) can be used to send output data to the I/O pin and to receive the signal input to the I/O port. The port direction register (DDR) can be used to set the I/O direction of the I/O pin in bit units.

The following table lists the I/O ports and the peripheral functions with which they share pins.

	Port Pin Name	Pin Name (Peripheral)	Peripheral Function that Shares Pin
Port 0	P00 to P07	—	(External bus)
Port 1	P10 to P17	—	(External bus)
Port 2	P20 to P23	—	(External bus)
	P24 to P27	PPG0 to PPG3	8/16-bit PPG timer 0, 1 (External bus)
Port 3	P30 to P33	TIN1, TOT1, TIN2, TOT2	16-bit Reload timer 1, 2 (External bus)
	P34 to P37	—	(External bus)
Port 4	P40, P41	TIN0, TOT0	16-bit Reload timer 0 (External bus)
	P42 to P47	SIN0, SOT0, SCK0, SIN1, SOT1, SCK1	UART0, UART1 (External bus)
Port 5	P50 to P57	—	(External bus)
Port 6	P60, P61	INT0, INT1	External interrupt
	P62 to P64	INT2 to INT4, SIN, SOT, SCK	External interrupt, Serial I/O
	P65	INT5, PWC	External interrupt, PWC
	P66, P67	INT6, INT7, SCL0, SDA0	External interrupt, I²C 0
Port 7	P70 to P77	AN0 to AN7	8/10-bit A/D converter
Port 8	P80 to P87	AN8 to AN15	8/10-bit A/D converter
Port 9	P90 to P95	SIN2, SOT2, SCK2, SIN3, SOT3, SCK3	UART2, 3
	P96	ADTG, FRCK	8/10-bit A/D converter, Free-run timer
Port A	PA0 to PA3	IN0 to IN3	Input capture 0, 1, 2, 3
	PA4 to PA7	OUT0 to OUT3	Output compare 0, 1, 2, 3
Port B	PB0 to PB3	SCL1, SDA1, SCL2, SDA2	I²C 1, 2
	PB4	—	—
	PB5, PB6	PPG4, PPG5	PPG timer 2

Note : These pins also serve as the analog input pins for ports 7 and 8. To use them as general-purpose ports, be sure to set the corresponding bits in the analog input enable register (ADER) to 0_B. The ADER is initialized to FF_H at a reset.

• Register list (port data register)

		7	6	5	4	3	2	1	0	Initial Value	Access
PDR0	bit										
Address : 000000H		P07	P06	P05	P04	P03	P02	P01	P00	XXXXXXXXB	R/W*
PDR1	bit	15	14	13	12	11	10	9	8		
Address : 000001H		P17	P16	P15	P14	P13	P12	P11	P10	XXXXXXXXB	R/W*
PDR2	bit	7	6	5	4	3	2	1	0		
Address : 000002H		P27	P26	P25	P24	P23	P22	P21	P20	XXXXXXXXB	R/W*
PDR3	bit	15	14	13	12	11	10	9	8		
Address : 000003H		P37	P36	P35	P34	P33	P32	P31	P30	XXXXXXXXB	R/W*
PDR4	bit	7	6	5	4	3	2	1	0		
Address : 000004H		P47	P46	P45	P44	P43	P42	P41	P40	XXXXXXXXB	R/W*
PDR5	bit	15	14	13	12	11	10	9	8		
Address : 000005H		P57	P56	P55	P54	P53	P52	P51	P50	XXXXXXXXB	R/W*
PDR6	bit	7	6	5	4	3	2	1	0		
Address : 000006H		P67	P66	P65	P64	P63	P62	P61	P60	XXXXXXXXB	R/W*
PDR7	bit	15	14	13	12	11	10	9	8		
Address : 000007H		P77	P76	P75	P74	P73	P72	P71	P70	XXXXXXXXB	R/W*
PDR8	bit	7	6	5	4	3	2	1	0		
Address : 000008H		P87	P86	P85	P84	P83	P82	P81	P80	XXXXXXXXB	R/W*
PDR9	bit	15	14	13	12	11	10	9	8		
Address : 000009H		—	P96	P95	P94	P93	P92	P91	P90	- XXXXXXXB	R/W*
PDRA	bit	7	6	5	4	3	2	1	0		
Address : 00000AH		PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	XXXXXXXXB	R/W*
PDRB	bit	7	6	5	4	3	2	1	0		
Address : 00000CH		—	PB6	PB5	PB4	PB3	PB2	PB1	PB0	- XXXXXXXB	R/W*

* : R/W access to I/O ports is a bit different in behavior from R/W access to memory as follows :

- Input mode

  Read : The level at the relevant pin is read.
  Write : Data is written to the output latch.

- Output mode

  Read : The data register latch value is read.
  Write : Data is output to the relevant pin.

• Register list (port direction register)

	bit	7	6	5	4	3	2	1	0	Initial Value	Access
DDR0 Address : 000010H		D07	D06	D05	D04	D03	D02	D01	D00	00000000B	R/W
DDR1 Address : 000011H	bit	15	14	13	12	11	10	9	8		
		D17	D16	D15	D14	D13	D12	D11	D10	00000000B	R/W
DDR2 Address : 000012H	bit	7	6	5	4	3	2	1	0		
		D27	D26	D25	D24	D23	D22	D21	D20	00000000B	R/W
DDR3 Address : 000013H	bit	15	14	13	12	11	10	9	8		
		D37	D36	D35	D34	D33	D32	D31	D30	00000000B	R/W
DDR4 Address : 000014H	bit	7	6	5	4	3	2	1	0		
		D47	D46	D45	D44	D43	D42	D41	D40	00000000B	R/W
DDR5 Address : 000015H	bit	15	14	13	12	11	10	9	8		
		D57	D56	D55	D54	D53	D52	D51	D50	00000000B	R/W
DDR6 Address : 000016H	bit	7	6	5	4	3	2	1	0		
		D67	D66	D65	D64	D63	D62	D61	D60	00000000B	R/W
DDR7 Address : 000017H	bit	15	14	13	12	11	10	9	8		
		D77	D76	D75	D74	D73	D72	D71	D70	00000000B	R/W
DDR8 Address : 000018H	bit	7	6	5	4	3	2	1	0		
		D87	D86	D85	D84	D83	D82	D81	D80	00000000B	R/W
DDR9 Address : 000019H	bit	15	14	13	12	11	10	9	8		
		—	D96	D95	D94	D93	D92	D91	D90	-0000000B	R/W
DDRA Address : 00001AH	bit	7	6	5	4	3	2	1	0		
		DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0	00000000B	R/W
DDRB Address : 00000DH	bit	15	14	13	12	11	10	9	8		
		—	DB6	DB5	DB4	DB3	DB2	DB1	DB0	-0000000B	R/W

- When each pin is serving as a port, the corresponding pin is controlled as follows :

  0 : Input mode

  1 : Output mode

  This bit becomes 0 after a reset.

Note : If these registers are accessed by a read modify write instruction (such as a bit set instruction) , the bits manipulated by the instruction are set to prescribed values but those other bits in output registers which have been set for input are rewritten to current input values of the pins. When switching a pin from input port to output port, therefore, write a desired value in the PDR first, then set the DDR to switch the pin for output.

• Register list (Analog input enable register)

	bit	7	6	5	4	3	2	1	0	Initial Value	Access
ADER0 Address : 00001E$_H$		ADE7	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0	11111111$_B$	R/W
ADER1 Address : 00001F$_H$	bit	15	14	13	12	11	10	9	8		
		ADE15	ADE14	ADE13	ADE12	ADE11	ADE10	ADE9	ADE8	11111111$_B$	R/W

This register controls the port 7, 8 pins as follows.

0 : Port input/output mode.
1 : Analog input mode.
This bit becomes 1 after a reset.

• Register list (Port pull-up resistance register)

	bit	7	6	5	4	3	2	1	0	Initial Value	Access
RDR0 Address : 00001C$_H$		RD07	RD06	RD05	RD04	RD03	RD02	RD01	RD00	00000000$_B$	R/W
RDR1 Address : 00001D$_H$	bit	15	14	13	12	11	10	9	8		
		RD17	RD16	RD15	RD14	RD13	RD12	RD11	RD10	00000000$_B$	R/W

Controls the pull-up resistor in input mode.

0 : Without pull-up resistor in input mode.

1 : With pull-up resistor in input mode.

Meaningless in output mode. (Without pull-up resistor)/The input/output mode is decided by the setting of the port direction register (DDR).

Without pull-up resistor is used in stop mode (SPL = 1). (High-Z) This function is disabled when the external bus is used. Do not attempt to write to this register.

• Register list (Output pin register)

	bit	7	6	5	4	3	2	1	0	Initial Value	Access
ODR4 Address : 00001B$_H$		OD47	OD46	OD45	OD44	OD43	OD42	OD41	OD40	00000000$_B$	R/W

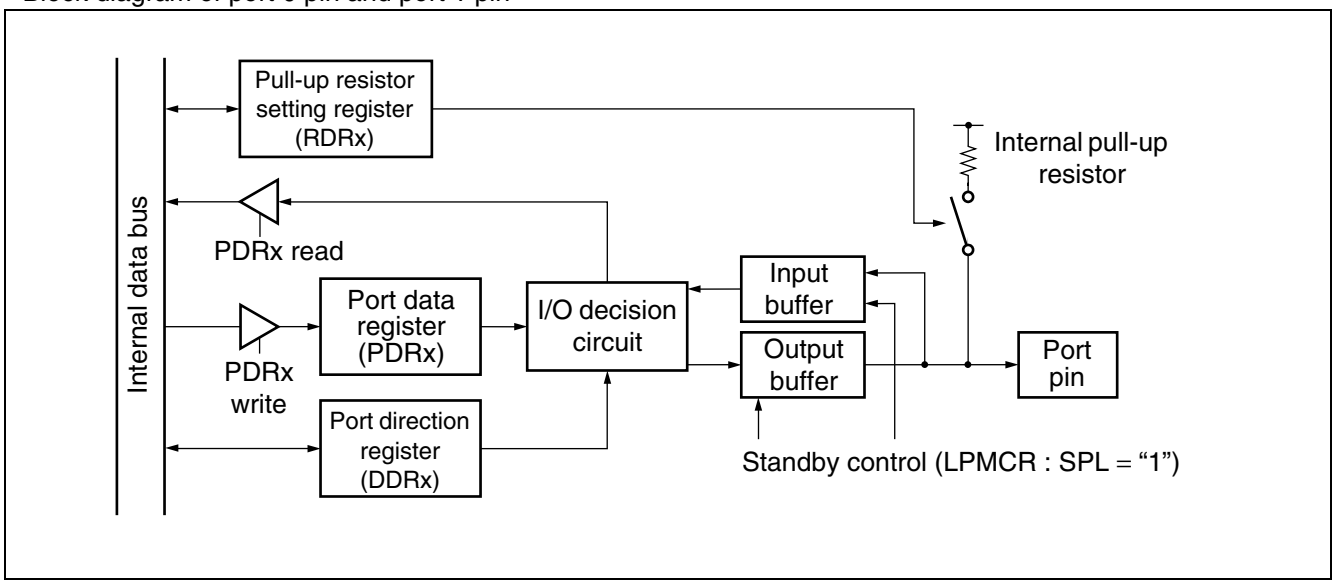
Controls open-drain in output mode.

0 : Serves as a standard output port in output mode.

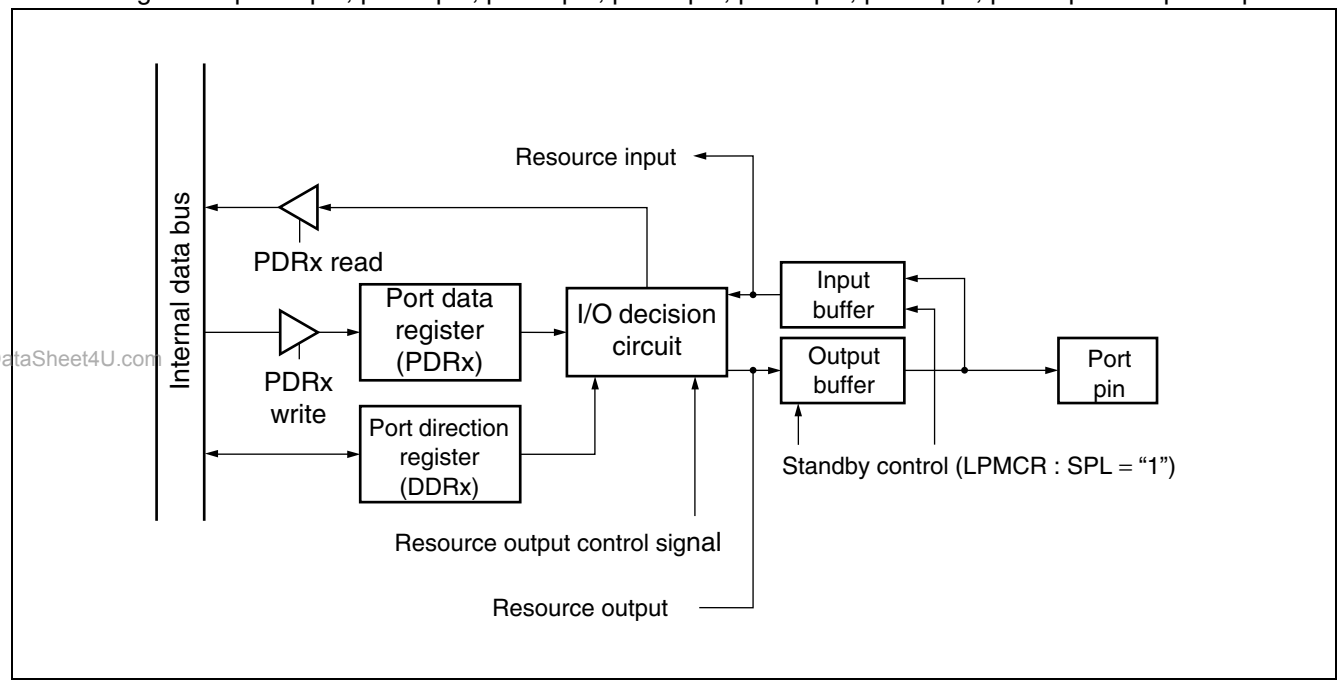
1 : Serves as an open-drain output port in output mode.

Meaningless in input mode (output High-Z)./The input/output mode is decided by the setting of the port direction register (DDR). This function is disabled when the external bus is used. Do not attempt to write to this register.

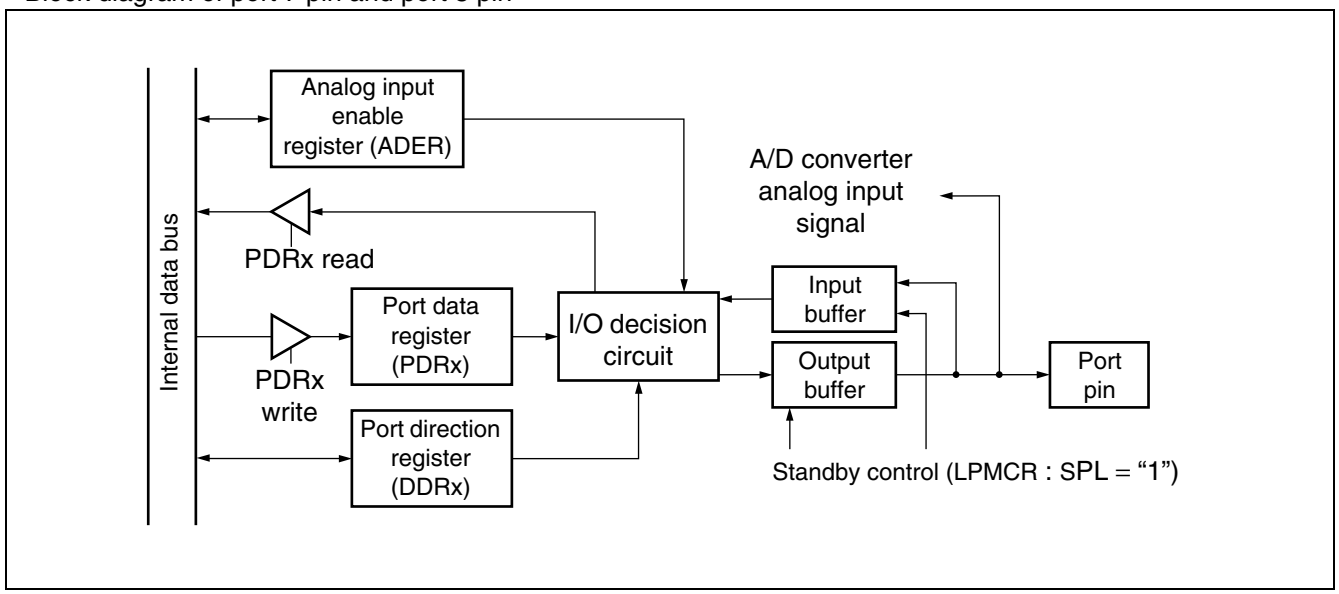
• Block diagram of port 0 pin and port 1 pin



• Block diagram of port 2 pin, port 3 pin, port 4 pin, port 5 pin, port 6 pin, port 9 pin, port A pin and port B pin



• Block diagram of port 7 pin and port 8 pin



Notes :
- When using as an input port, set "0" in the corresponding bit of the port-7 and port-8 direction register (DDR7 and DDR8) and "0" in the related bit of the analog input enable register (ADER).
- When using as an analog input pin, set "0" in the corresponding bit of the port-7 and port-8 direction register (DDR7 and DDR8) and "1" in the related bit of the analog input enable register (ADER).

2. Time-base timer

The time-base timer is an 18-bit free-run counter (time-base timer counter) that counts in synchronization with the main clock (2 cycles of the oscillation clock HCLK). Four different time intervals can be selected, for each of which an interrupt request can be generated. Operating clock signals are supplied to peripheral resources such as the oscillation stabilization wait timer and watchdog timer.

• Interval time of time-base timer

Internal count clock cycle	Interval time
2/HCLK (0.33 μs)	2^{12}/HCLK (Approx. 0.68 ms)
	2^{14}/HCLK (Approx. 2.7 ms)
	2^{16}/HCLK (Approx. 10.9 ms)
	2^{19}/HCLK (Approx. 87.4 ms)

Notes : • HCLK : Oscillation clock frequency
• The parenthesized values assume an oscillator clock frequency of 6 MHz.

• Clock cycles supplied from time-base timer

Where to supply clock	Clock cycle
Main clock oscillation stabilization wait	2^{13}/HCLK (Approx. 1.36 ms)
	2^{15}/HCLK (Approx. 5.46 ms)
	2^{17}/HCLK (Approx. 21.84 ms)
Watchdog timer	2^{12}/HCLK (Approx. 0.68 ms)
	2^{14}/HCLK (Approx. 2.7 ms)
	2^{16}/HCLK (Approx. 10.9 ms)
	2^{19}/HCLK (Approx. 87.4 ms)

Notes : • HCLK : Oscillation clock frequency
• The parenthesized values assume an oscillator clock frequency of 6 MHz.

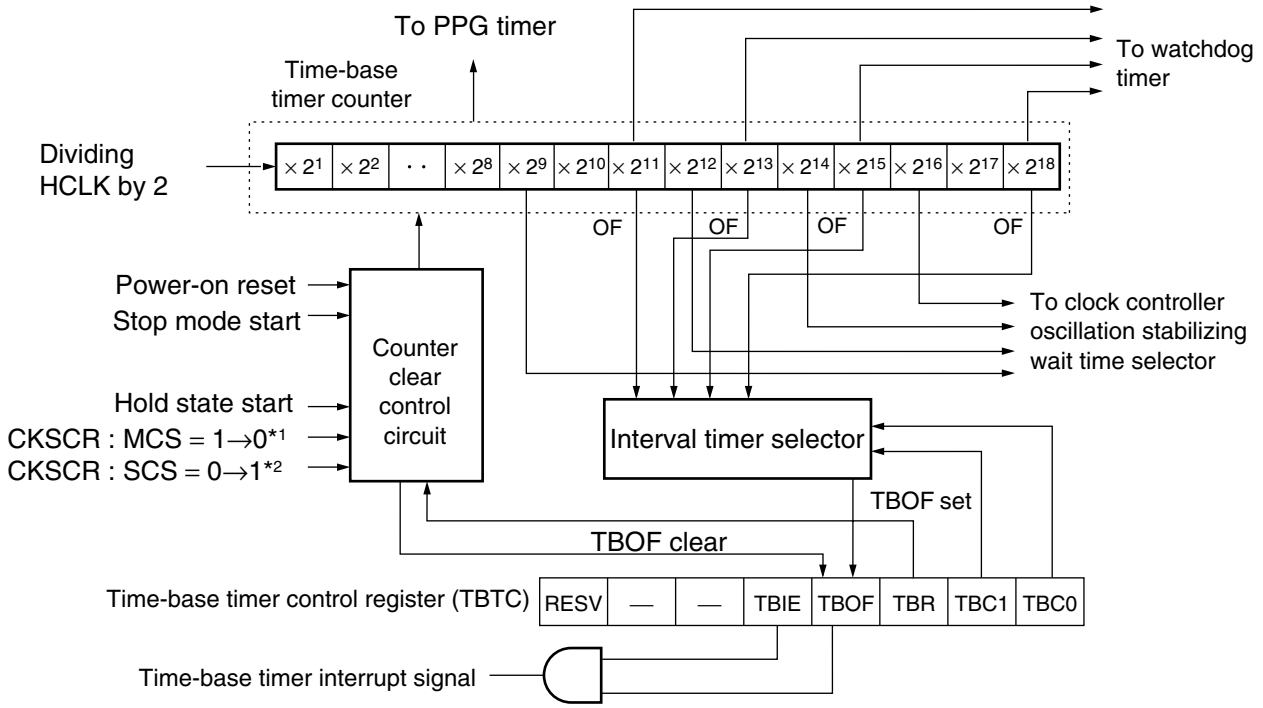
• Register list

Time-base timer control register (TBTC)

Address : 0000A9H

bit	15	14	13	12	11	10	9	8
	RESV	—	—	TBIE	TBOF	TBR	TBC1	TBC0
	(R/W)	(—)	(—)	(R/W)	(R/W)	(W)	(R/W)	(R/W)
Initial Value	1	-	-	0	0	1	0	0

• Block Diagram



– : Unused
OF : Overflow
HCLK : Oscillation clock
*1 : Switching the machine clock from main clock or sub clock to PLL clock
*2 : Switching the machine clock from sub clock to main clock

Actual interrupt request number of time-base timer is as follows :
Interrupt request number : #40 (28_H)

3. Watchdog timer

The watchdog timer is timer counter provided for measure of program runaway. It is a 2-bit counter operating with an output of the timebase timer or watch timer as the count clock and resets the CPU when the counter is not cleared for a preset period of time after start.

• Interval time of watchdog timer

HCLK : Oscillation clock(6 MHz) SCLK : Sub clock(8 kHz)		
Min	**Max**	**Clock cycle**
Approx. 2.39 ms	Approx. 3.07 ms	$(2^{14} \pm 2^{11})$ /HCLK
Approx. 9.56 ms	Approx. 12.29 ms	$(2^{16} \pm 2^{13})$ /HCLK
Approx. 38.23 ms	Approx. 49.15 ms	$(2^{18} \pm 2^{15})$ /HCLK
Approx. 305.83 ms	Approx. 393.22 ms	$(2^{21} \pm 2^{18})$ /HCLK
Approx. 0.448 s	Approx. 0.576 s	$(2^{12} \pm 2^{9})$ /SCLK
Approx. 3.584 s	Approx. 4.608 s	$(2^{15} \pm 2^{12})$ /SCLK
Approx. 7.168 s	Approx. 9.216 s	$(2^{16} \pm 2^{13})$ /SCLK
Approx. 14.336 s	Approx. 18.432 s	$(2^{17} \pm 2^{14})$ /SCLK

Notes :
- The maximum and minimum time intervals for the watchdog timer depend on the counter clear timing.
- The watchdog timer contains a 2-bit counter that counts the carry-up signal from the time-base timer or watch timer.
- Interval time of watchdog timer is longer than the set time during the following conditions.
  - When clearing the timebase timer during operation on oscillation (HCLK)
  - When clearing the watch timer during operation on sub clock (SCLK)

• Events that stop the watchdog timer
- Stop due to a power-on reset
- Watchdog reset

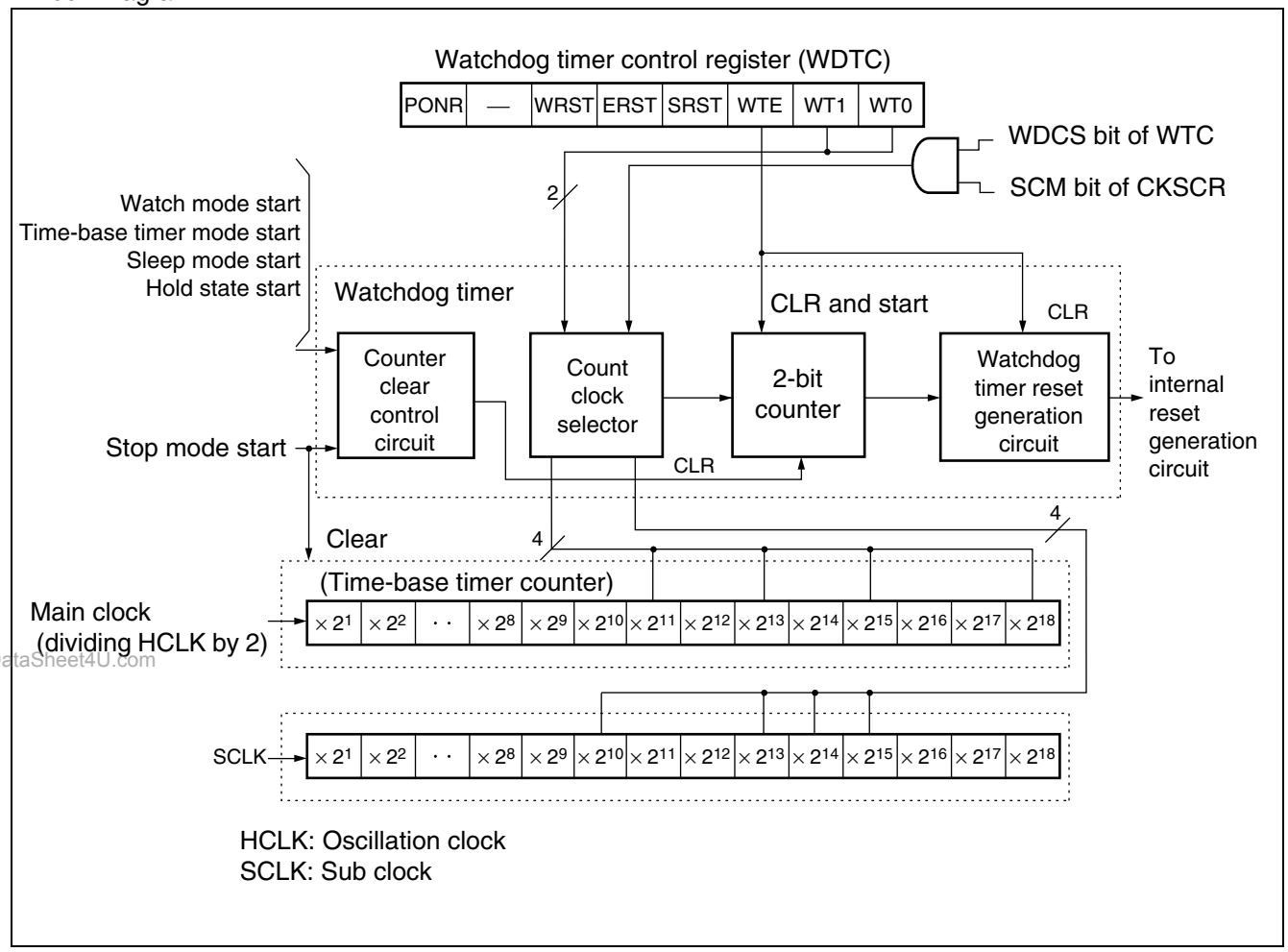
• Clear factor of watchdog timer
- External reset input by $\overline{\text{RST}}$ pin
- Writing “0” to the software reset bit
- Writing “0” to the watchdog timer control bit (second and subsequent times)
- Transition to sleep mode (clearing the watchdog timer to suspend counting)
- Transition to time-base timer mode (clearing the watchdog timer to suspend counting)
- Transition to stop mode (clearing the watchdog timer to suspend counting)

• Register list

Watchdog timer control register (WDTC)

bit	7	6	5	4	3	2	1	0	Initial Value
Address : 0000A8H	PONR	—	WRST	ERST	SRST	WTE	WT1	WT0	X-XXX111B
	(R)	(—)	(R)	(R)	(R)	(W)	(W)	(W)	

• Block Diagram



4. Watch timer

The watch timer is a 15-bit timer using the sub clock. It can generate interval interrupts. It can also be used as a clock source for the watchdog timer.

• Register list

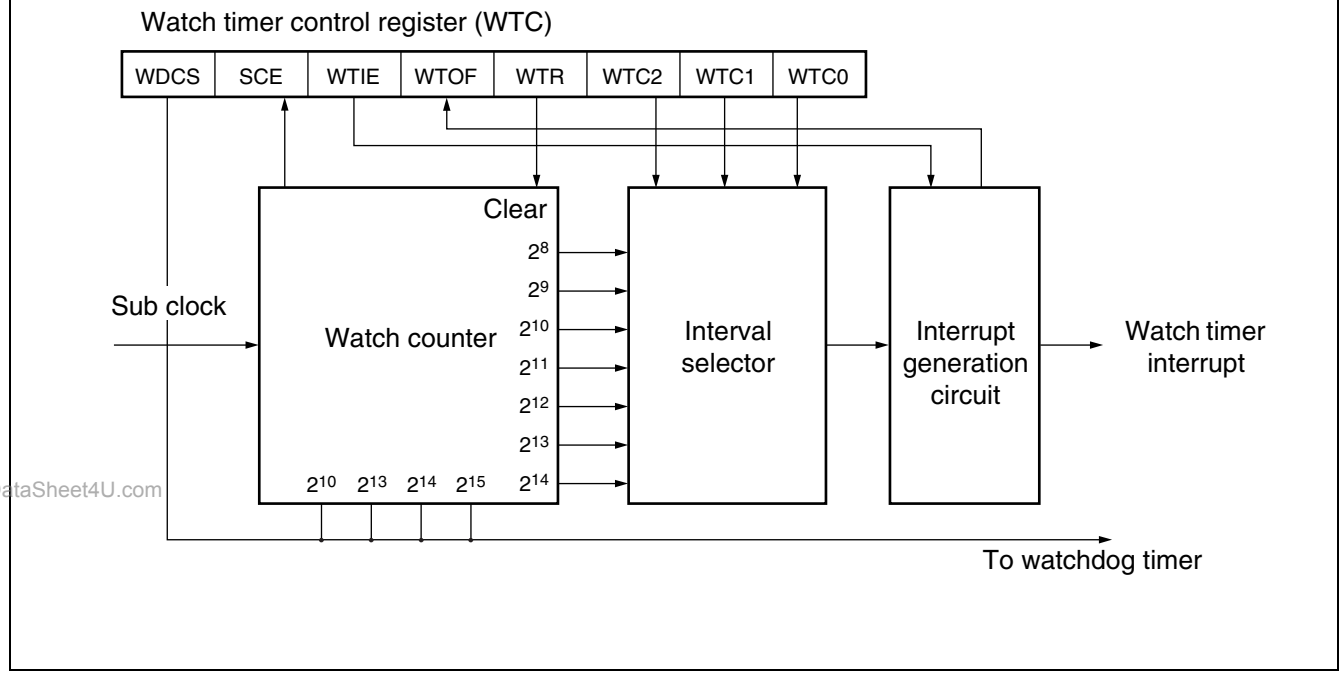
Watch timer control register (WTC)

Address : 0000AA$_H$

bit	7	6	5	4	3	2	1	0
	WDCS	SCE	WTIE	WTOF	WTR	WTC2	WTC1	WTC0
	(R/W)	(R)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)

Initial Value
10001000$_B$

• Block Diagram



5. 16-bit reload timer

The 16-bit reload timer has the internal clock mode to decrement in synchronization with 3 different internal clocks and the event count mode to decrement upon detection of an arbitrary edge of the pulse input to the external pin. Either can be selected. This timer defines when the count value changes from 0000_H to $FFFF_H$ as an underflow. The timer therefore causes an underflow when the count reaches [reload register setting + 1]. Either mode can be selected for the count operation from the reload mode which repeats the count by reloading the count setting value at the underflow occurrence or the one-shot mode which stops the count at the underflow occurrence. The interrupt can be generated at the counter underflow occurrence so as to correspond to the EI^2OS.

• Register list

• TMCSR (Timer control status register 0 to 2)

Timer control status register (upper) (TMCSR0 to TMCSR2)

	bit	15	14	13	12	11	10	9	8	Initial Value
Address : 000063_H		—	—	—	—	CSL1	CSL0	MOD2	MOD1	$XXXX0000_B$
000067_H		(—)	(—)	(—)	(—)	(R/W)	(R/W)	(R/W)	(R/W)	
$00006B_H$										

Timer control status register (lower) (TMCSR0 to TMCSR2)

	bit	7	6	5	4	3	2	1	0	Initial Value
Address : 000062_H		MOD0	OUTE	OUTL	RELD	INTE	UF	CNTE	TRG	00000000_B
000066_H		(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
$00006A_H$										

• 16-bit timer register/16-bit reload register

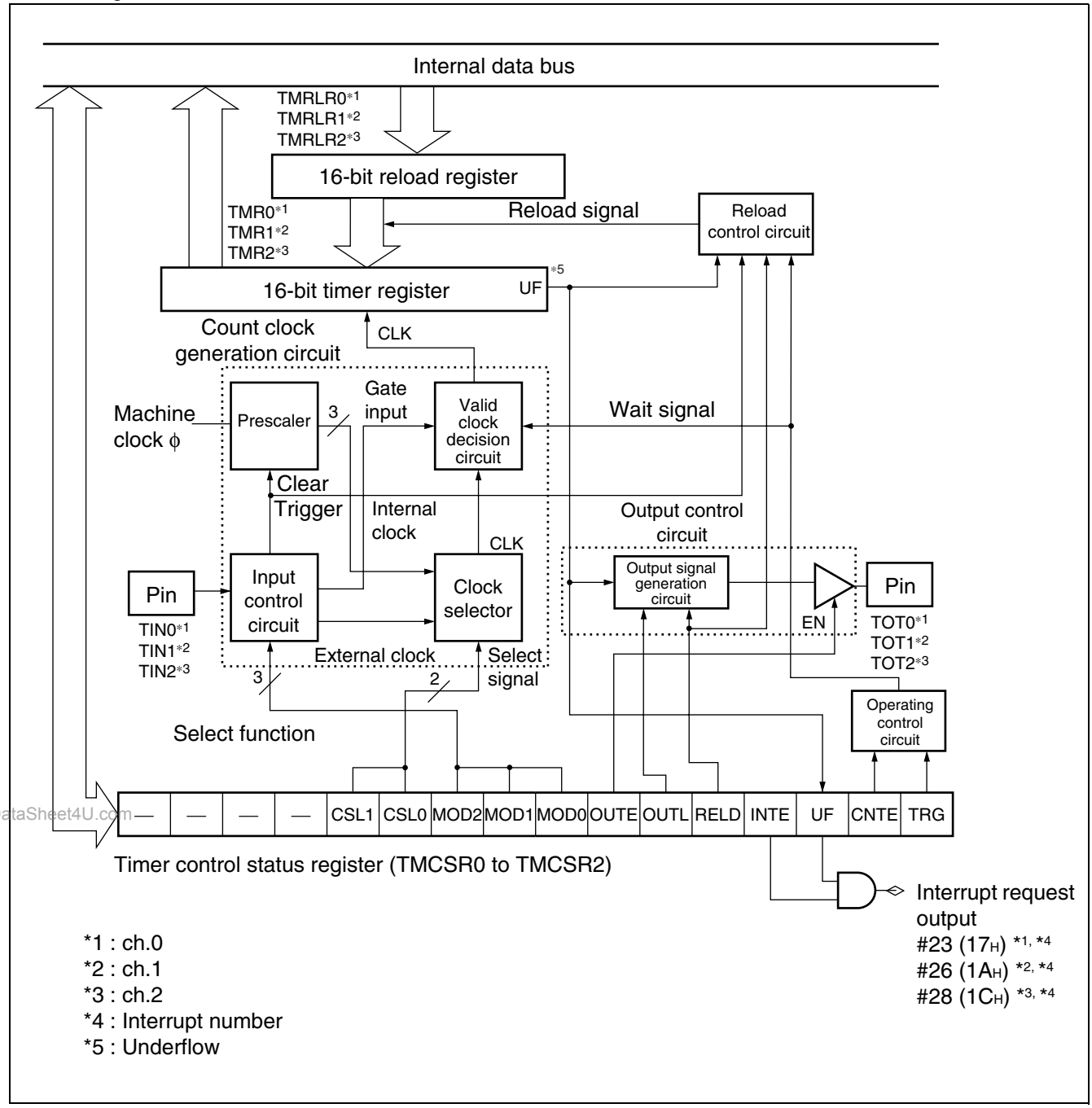
TMR0 to TMR2/TMRLR0 to TMRLR2 (upper)

	bit	15	14	13	12	11	10	9	8	Initial Value
Address : 000065_H		D15	D14	D13	D12	D11	D10	D09	D08	$XXXXXXXX_B$
000069_H		(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
$00006D_H$										

TMR0 to TMR2/TMRLR0 to TMRLR2 (lower)

	bit	7	6	5	4	3	2	1	0	Initial Value
Address : 000064_H		D07	D06	D05	D04	D03	D02	D01	D00	$XXXXXXXX_B$
000068_H		(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
$00006C_H$										

• Block diagram



*1 : ch.0
*2 : ch.1
*3 : ch.2
*4 : Interrupt number
*5 : Underflow

6. Multi function timer

The multi-function timer enables the following based on the 16-bit free-run timer.
- Output of independent waveform
- Measurement of input pulse width
- Measurement of external clock cycle

• Configuration of a multi-functional timer

16-bit free-run timer	16-bit Output Compare	16-bit Input Capture	8/16-bit PPG timer	16-bit PWC timer
1 channel	4 channels	4 channels	8-bit × 6 channels (16-bit × 3 channels)	1 channel

• 16-bit free-run timer : 1 channel

The 16-bit free-run timer consists of a 16-bit up counter (timer data register (TCDT)), compare clear register (CPCLR), timer control status register (TCCS), and prescaler.

The counter output value of the 16-bit free-run timer is used as the base timer for the output compare and input capture units.
- The count clock can be set, selected from among the following eight types.
  1/ϕ, 2/ϕ, 4/ϕ, 8/ϕ, 16/ϕ, 32/ϕ, 64/ϕ, 128/ϕ
  ϕ : Machine clock frequency
- During the following conditions, the interrupt should be output.
  - The counter value of 16-bit free run timer will be overflowed.
  - The counter value of 16-bit free run timer will be cleared after the counter value of 16-bit free run timer = the compare clear register value (CPCLR) (TCCS : ICRE = “1”, MODE = “1”)
- The counter value of 16-bit free run timer should be cleared to “0000$_H$” during the following conditions.
  - Reset
  - When setting the clear bit (SCLR) of timer control status register (TCCS) to “1”
  - When the counter value of the 16-bit free run timer = the compare clear register value (CPCLR) (TCCS : MODE = “1”)
  - When setting “0000$_H$” to the timer data register (TCDT)

• Output compare : 4 channels

The output compare unit consists of compare registers (OCCP0 to OCCP3), compare control registers (OCS0 to OCS3), and a compare output latch.

The output compare unit can invert the output level and output an interrupt when a compare register (OCCP0 to OCCP3) value matches the counter value of the 16-bit free-run timer.
- Output compare registers can operate as 4 independent channels. The output compare registers (OCCP0 to OCCP3) of each channel have interrupt request flags of their respective output pins.
- Pin output can be inverted by using 2 channels of output compare registers (OCCP0 to OCCP3).
- If the counter value of 16-bit free run timer = the output compare register (OCCP0 to OCCP3) (OCS0, OCS2 : ICP0 = “1”, ICP1 = “1”), the interrupt request should be generated. (OCS0, OCS2 : ICE0 = “1”, ICE1 = “1”)
- The initial value for pin output of each channel can be set.

• Input capture : 4 channels

The input capture unit consists of the input capture data registers (IPCP0 to IPCP3) corresponding to external input pins (IN0 to IN3) and input capture control registers (ICS01, ICS23).

The input capture unit can capture the counter value of the 16-bit free-run timer into the input capture data register (IPCP0 to IPCP3) to generated an interrupt request upon detection of the effective edge of the signal input through the external input.

- The input capture unit in each channel can operate independently.
- The effective edge of the external signal can be selected (rising edge, falling edge, both edges).
- An interrupt request can be generated upon detection of the selected effective edge of the external signal.(ICS01, ICS2 : ICE0 = “1”, ICE1 = “1”, ICE2 = “1”, ICE3 = “1”).

• Register list (16-bit free-run timer)

Compare clear register (CPCLR)

bit	15	14	13	12	11	10	9	8	Initial Value
Address : 00008B$_H$	CL15	CL14	CL13	CL12	CL11	CL10	CL09	CL08	XXXXXXXX$_B$
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

bit	7	6	5	4	3	2	1	0	Initial Value
Address : 00008A$_H$	CL07	CL06	CL05	CL04	CL03	CL02	CL01	CL00	XXXXXXXX$_B$
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

Timer data register (TCDT)

bit	15	14	13	12	11	10	9	8	Initial Value
Address : 000087$_H$	T15	T14	T13	T12	T11	T10	T09	T08	00000000$_B$
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

bit	7	6	5	4	3	2	1	0	Initial Value
Address : 000086$_H$	T07	T06	T05	T04	T03	T02	T01	T00	00000000$_B$
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

Timer control/status register (TCCS)

bit	15	14	13	12	11	10	9	8	Initial Value
Address : 000089$_H$	ECKE	—	—	MSI2	MSI1	MSI0	ICLR	ICRE	0--00000$_B$
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

bit	7	6	5	4	3	2	1	0	Initial Value
Address : 000088$_H$	IVF	IVFE	STOP	MODE	SCLR	CLK2	CLK1	CLK0	00000000$_B$
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

• Register list (output compare)

Compare register (OCCP0 to OCCP3)

Address : 007919H, 00791BH, 00791DH, 00791FH

bit	15	14	13	12	11	10	9	8	Initial Value
	C15	C14	C13	C12	C11	C10	C09	C08	XXXXXXXXB
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

Address : 007918H, 00791AH, 00791CH, 00791EH

bit	7	6	5	4	3	2	1	0	Initial Value
	C07	C06	C05	C04	C03	C02	C01	C00	XXXXXXXXB
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

Control register (OCS1/OCS3)

Address : 000055H, 000057H

bit	15	14	13	12	11	10	9	8	Initial Value
	—	—	—	CMOD	OTE1	OTE0	OTD1	OTD0	---00000B
	(—)	(—)	(—)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

Control register (OCS0/OCS2)

Address : 000054H, 000056H

bit	7	6	5	4	3	2	1	0	Initial Value
	ICP1	ICP0	ICE1	ICE0	—	—	CST1	CST0	0000--00B
	(R/W)	(R/W)	(R/W)	(R/W)	(—)	(—)	(R/W)	(R/W)	

• Register list (input capture)

Input capture data register (IPCP0 to IPCP3)

bit	15	14	13	12	11	10	9	8	Initial Value
Address : 007911H 007913H 007915H 007917H	CP15	CP14	CP13	CP12	CP11	CP10	CP09	CP08	XXXXXXXXB
	(R)	(R)	(R)	(R)	(R)	(R)	(R)	(R)	

bit	7	6	5	4	3	2	1	0	Initial Value
Address : 007910H 007912H 007914H 007916H	CP07	CP06	CP05	CP04	CP03	CP02	CP01	CP00	XXXXXXXXB
	(R)	(R)	(R)	(R)	(R)	(R)	(R)	(R)	

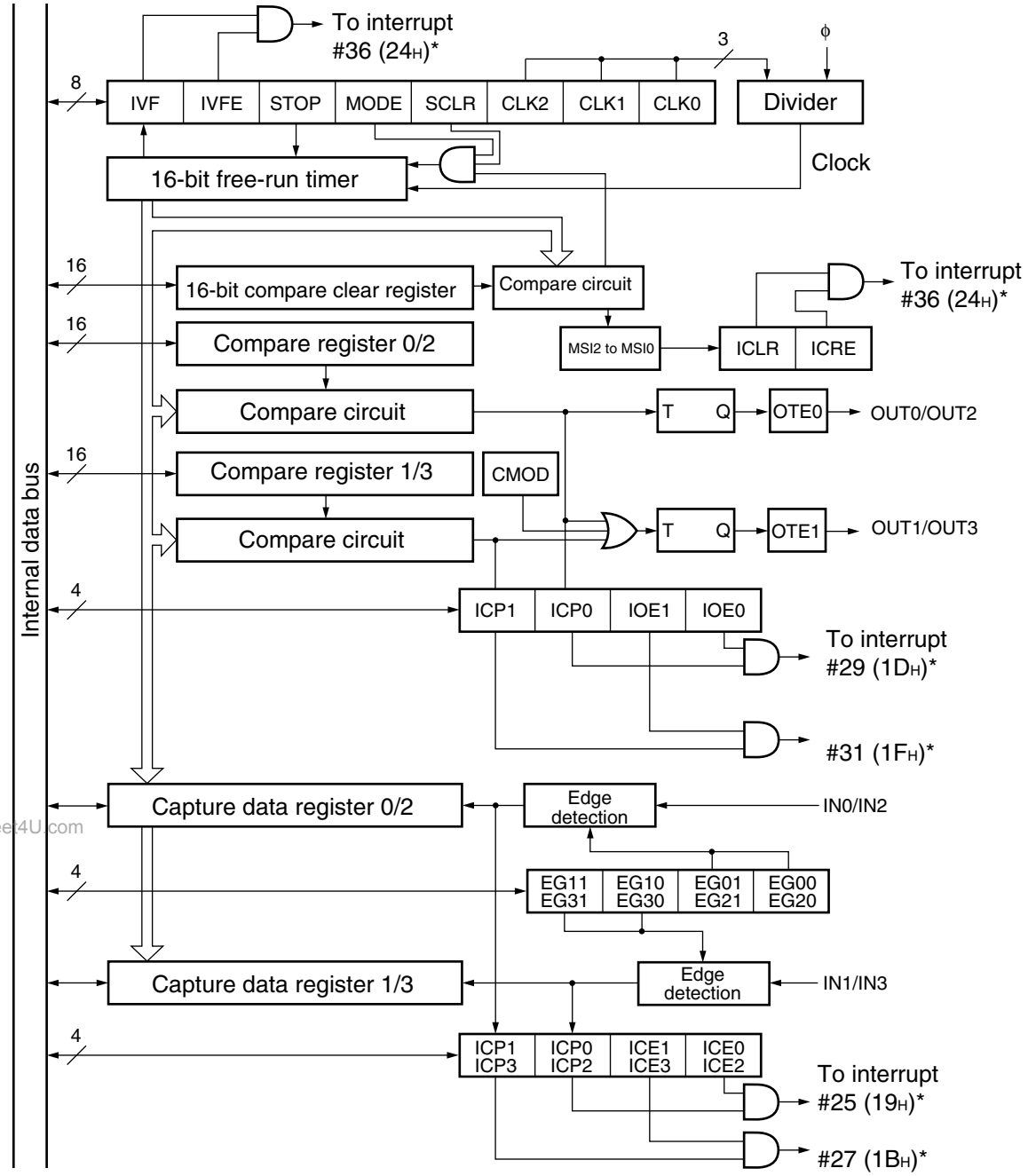
Input capture control status register (ICS23)

bit	15	14	13	12	11	10	9	8	Initial Value
Address : 000053H	ICP3	ICP2	ICE3	ICE2	EG31	EG30	EG21	EG20	00000000B
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

Input capture control status register (ICS01)

bit	7	6	5	4	3	2	1	0	Initial Value
Address : 000052H	ICP1	ICP0	ICE1	ICE0	EG11	EG10	EG01	EG00	00000000B
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

• Block diagram of the 16-bit free-run timer, input capture units, and output compare units



* : Interrupt number
ϕ : Machine clock frequency

- 8/16-bit PPG timer (8-bit : 6 channels, 16-bit : 3 channels)

  8/16-bit PPG timer consists of an 8-bit down counter (PCNT), PPG operation mode control register (PPGC0 to PPGC5), PPG output control register (PPG01, PPG23, PPG45) and PPG reload register (PRLL0 to PRLL5, PRLH0 to PRLH5).
  When used as an 8-/16-bit reload timer, the PPG timer serves as an event timer. It can also output pulses of an arbitrary duty ratio at an arbitrary frequency.
  - 8-bit PPG mode
    Each channel operates as an independent 8-bit PPG.
  - 8-bit prescaler + 8-bit PPG mode
    Operates as an arbitrary-cycle 8-bit PPG with PPG0 (PPG2, PPG4) operating as an 8-bit prescaler and PPG1 (PPG3, PPG5) counted by the borrow output of PPG0 (PPG2, PPG4).
  - 16-bit PPG mode
    Operates as a 16-bit PPG with PPG0 (PPG2, PPG4) and PPG1 (PPG3, PPG5) connected.
  - PPG operation

  The PPG timer outputs pulses of an arbitrary duty ratio (the ratio between the High and Low level periods of pulse waveform) at an arbitrary frequency. This can also be used as a D/A converter by an external circuit.

• Register list

PPG operation mode control register
(PPGC1/PPGC3/PPGC5)

bit	15	14	13	12	11	10	9	8	Initial Value
Address : 000047H 000049H 00004BH	PEN1	—	PE10	PIE1	PUF1	MD1	MD0	Reserved	0X000001B
	(R/W)	(—)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

(PPGC0/PPGC2/PPGC4)

bit	7	6	5	4	3	2	1	0	Initial Value
Address : 000046H 000048H 00004AH	PEN0	—	PE00	PIE0	PUF0	—	—	Reserved	0X000XX1B
	(R/W)	(—)	(R/W)	(R/W)	(R/W)	(—)	(—)	(R/W)	

PPG output control register (PPG01/PPG23/PPG45)

bit	7	6	5	4	3	2	1	0	Initial Value
Address : 00004CH 00004EH 000050H	PCS2	PCS1	PCS0	PCM2	PCM1	PCM0	Reserved	Reserved	000000XXB
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

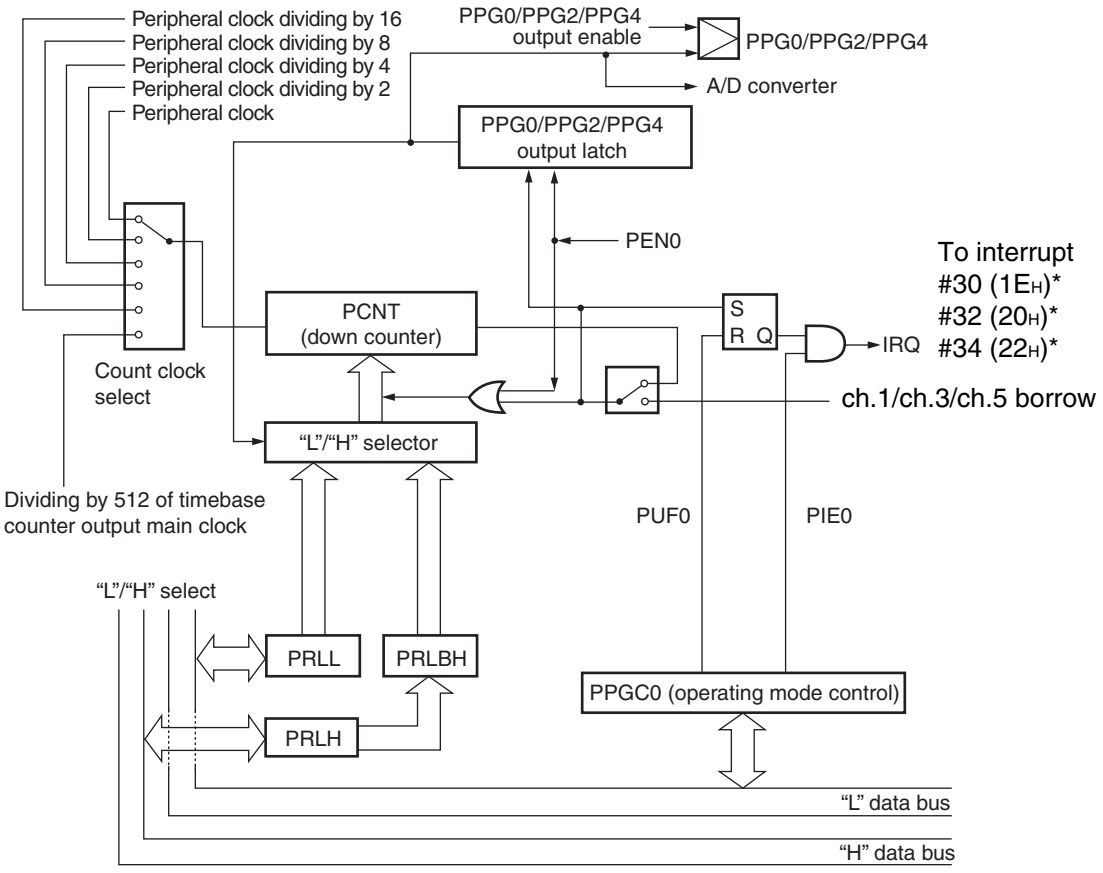
PPG reload register
(PRLH0 to PRLH5)

bit	15	14	13	12	11	10	9	8	Initial Value
Address : 007901H 007903H 007905H 007907H 007909H 00790BH	D15	D14	D13	D12	D11	D10	D09	D08	XXXXXXXXB
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

(PRLL0 to PRLL5)

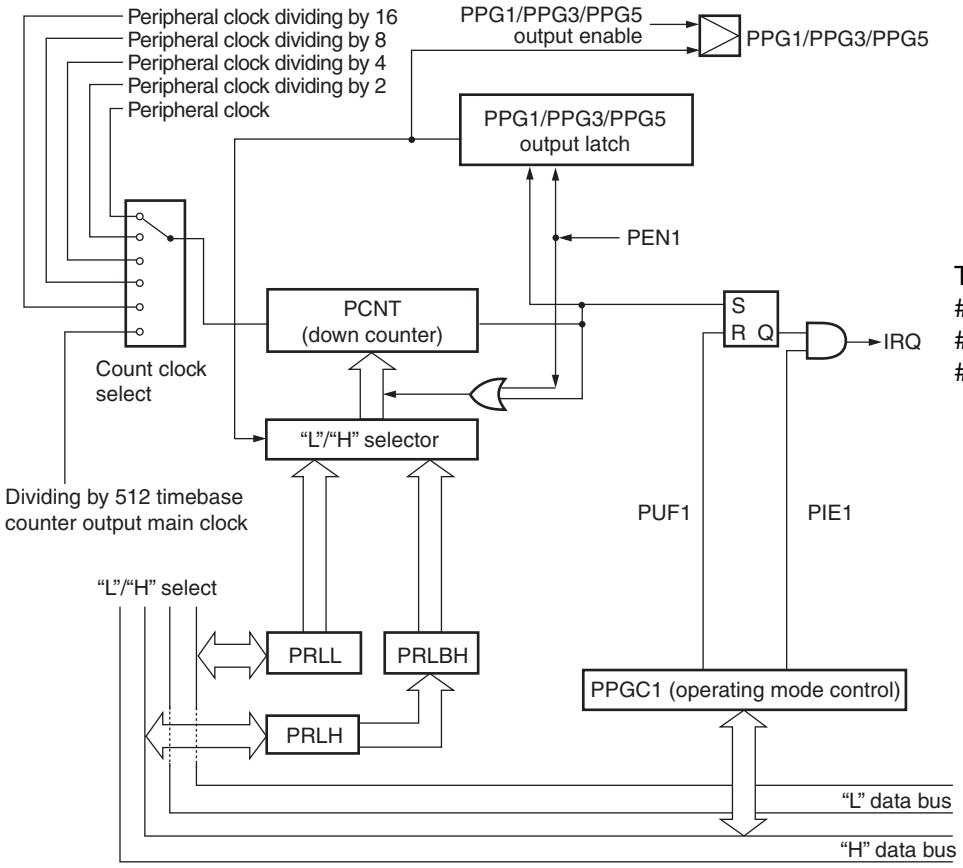
bit	7	6	5	4	3	2	1	0	Initial Value
Address : 007900H 007902H 007904H 007906H 007908H 00790AH	D07	D06	D05	D04	D03	D02	D01	D00	XXXXXXXXB
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

• 8/16-bit PPG ch.0/ch.2/ch.4 block diagram



* : Interrupt number

• 8-bit PPG ch.1/ch.3/ch.5 block diagram



* : Interrupt number

• PWC timer

The PWC timer is a 16-bit multi-function up-count timer capable of measuring the input signal pulse width.

• Register list

PWC control status register (PWCSR)

Address : 00005D$_H$

bit	15	14	13	12	11	10	9	8
	STRT	STOP	EDIR	EDIE	OVIR	OVIE	ERR	Reserved
	(R/W)	(R/W)	(R)	(R/W)	(R/W)	(R/W)	(R)	(R/W)

Initial Value 0000000X$_B$

Address : 00005C$_H$

bit	7	6	5	4	3	2	1	0
	CKS1	CKS0	PIS1	PIS0	S/C	MOD2	MOD1	MOD0
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)

Initial Value 00000000$_B$

PWC data buffer register (PWCR)

Address : 00005F$_H$

bit	15	14	13	12	11	10	9	8
	D15	D14	D13	D12	D11	D10	D9	D8
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)

Initial Value 00000000$_B$

Address : 00005E$_H$

bit	7	6	5	4	3	2	1	0
	D7	D6	D5	D4	D3	D2	D1	D0
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)

Initial Value 00000000$_B$

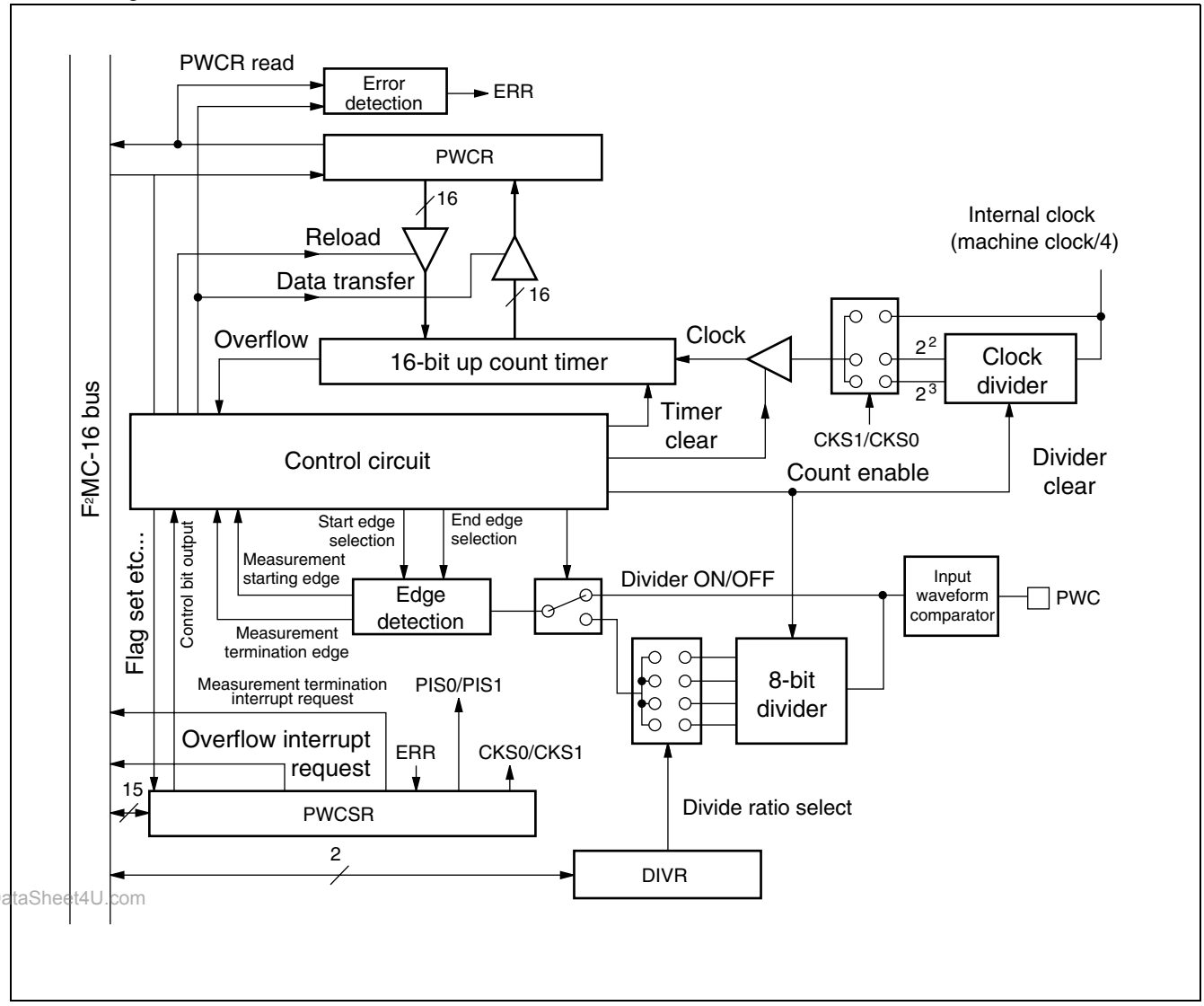
PWC ratio of dividing frequency control register (DIVR)

Address : 000060$_H$

bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	DIV1	DIV0
	(—)	(—)	(—)	(—)	(—)	(—)	(R/W)	(R/W)

Initial Value ------00$_B$

• Block Diagram



7. UART

UART is a general purpose serial communication interface for synchronous or asynchronous (start-stop synchronization) communications with external devices. It supports bi-directional communication (normal mode) and master/slave communication (multi-processor mode: supported on master side only). An interrupt can be generated upon completion of reception, detection of a reception error, or completion of transmission. EI²OS is supported.

• UART functions

UART, or a generic serial data communication interface that sends and receives serial data to and from other CPU and peripherals, has the functions listed in following.

	Function
Data buffer	Full-duplex double-buffered
Transmission mode	• Clock synchronous (without start/stop bit) • Clock asynchronous (start-stop synchronous)
Baud rate	• Special-purpose baud-rate generator It is optional from 8 kinds. • Baud rate by external clock (SCK0/SCK1/SCK2/SCK3 terminal input)
Data length	• 8-bit or 7-bit (in the asynchronous normal mode only) • 1-bit to 8-bit (synchronous mode only)
Signal system	Non Return to Zero (NRZ) system
Reception error detection	• Framing error • Overrun error • Parity error (Not supported in operation mode 1)
Interrupt request	• Receive interrupt (reception completed, reception error detected) • Transmission interrupt (transmission completed) • Both the transmission and reception support EI²OS.
Master/slave type communication function (multi processor mode)	Capable of 1 (master) to many (slaves) communication (available just as master)

Note : In clock synchronous transfer mode, the UART transfers only data with no start or stop bit added.

• UART operation modes

Operation mode		Data length		Synchronization	Stop bit length
		Without parity	With parity		
0	Normal mode	7-bit or 8-bit		Asynchronous	1-bit or 2-bit *2
1	Multi processor mode	8-bit + 1*1	—	Asynchronous	
2	Normal mode	1 to 8-bit	—	Synchronous	No

— : Setting disabled

*1 : + 1 is an address/data setting bit (A/D) which is used for communication control.

*2 : Only one bit can be detected as a stop bit at reception.

• Register list

Serial mode register (SMR0 to SMR3)

Address :	bit	7	6	5	4	3	2	1	0	Initial Value
000020H 000026H 00002CH 000032H		MD1	MD0	SCKL	M2L2	M2L1	M2L0	SCKE	SOE	00100000B
		(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

Serial control register (SCR0 to SCR3)

Address :	bit	15	14	13	12	11	10	9	8	Initial Value
000021H 000027H 00002DH 000033H		PEN	P	SBL	CL	A/D	REC	RXE	TXE	00000100B
		(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(W)	(R/W)	(R/W)	

Serial input/output data register (SIDR0 to SIDR3 / SODR0 to SODR3)

Address :	bit	7	6	5	4	3	2	1	0	Initial Value
000022H 000028H 00002EH 000034H		D7	D6	D5	D4	D3	D2	D1	D0	XXXXXXXXB
		(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

Serial status register (SSR0 to SSR3)

Address :	bit	15	14	13	12	11	10	9	8	Initial Value
000023H 000029H 00002FH 000035H		PE	ORE	FRE	RDRF	TDRE	BDS	RIE	TIE	00001000B
		(R)	(R)	(R)	(R)	(R)	(R/W)	(R/W)	(R/W)	

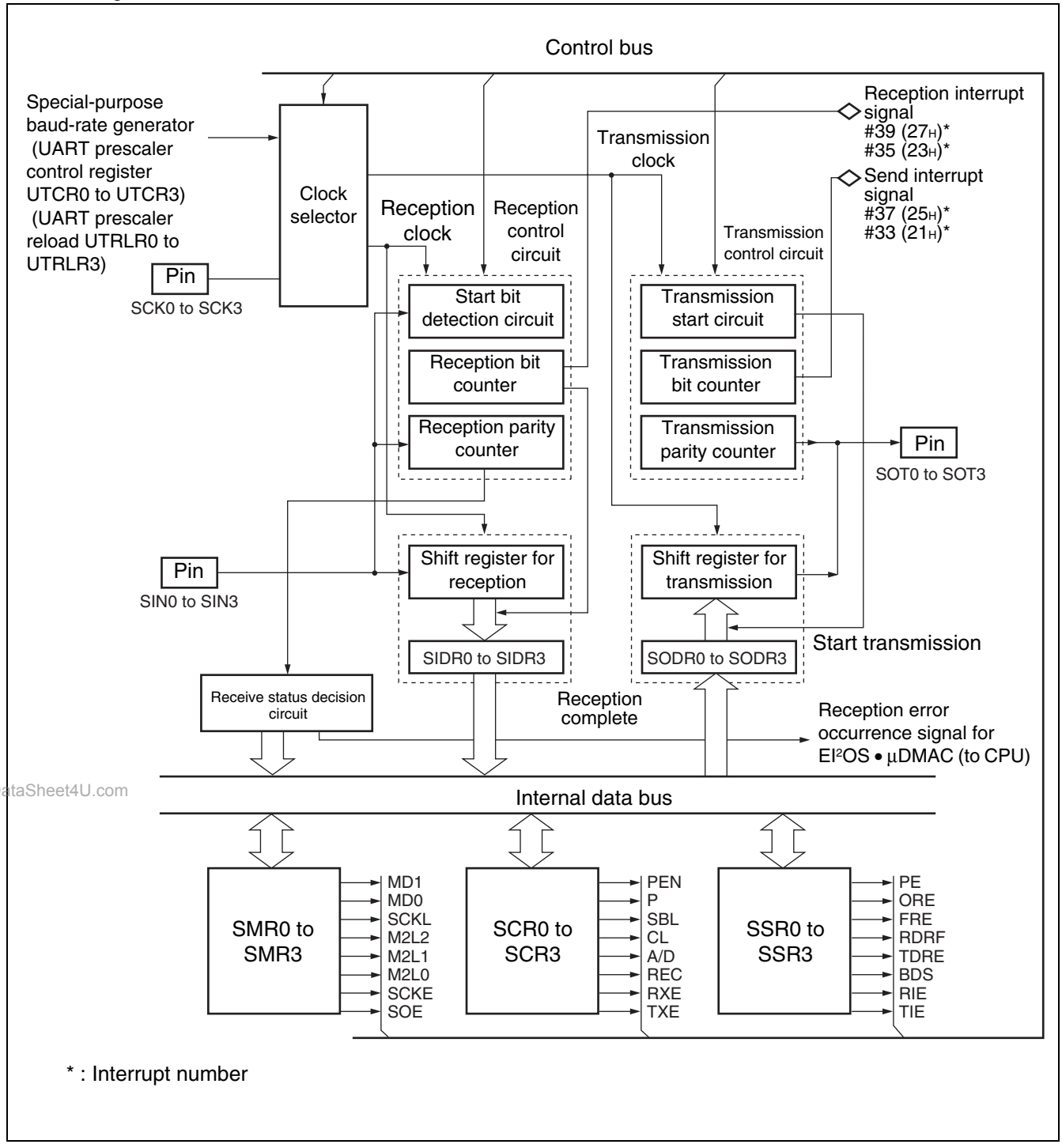
UART prescaler reload register (UTRLR0 to UTRLR3)

Address :	bit	7	6	5	4	3	2	1	0	Initial Value
000024H 00002AH 000030H 000036H		D7	D6	D5	D4	D3	D2	D1	D0	00000000B
		(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

UART prescaler control register (UTCR0 to UTCR3)

Address :	bit	15	14	13	12	11	10	9	8	Initial Value
000025H 00002BH 000031H 000037H		MD	SRST	CKS	Reserved	—	D10	D9	D8	0000-000B
		(R/W)	(R/W)	(R/W)	(R/W)	(—)	(R/W)	(R/W)	(R/W)	

• Block Diagram



* : Interrupt number

8. Extended I/O serial interface

The extended I/O serial interface is a serial I/O interface in an 8-bit, single-channel, capable of clock synchronous data transfer. LSB-first or MSB-first transfer mode can be selected for data transfer.

There are 2 serial I/O operation modes available:

- Internal shift clock mode: Transfer data in synchronization with the internal clock.
- External shift clock mode: Transfer data in synchronization with the clock supplied via the external pin (SCK). By manipulating the general-purpose port sharing the external pin (SCK) in this mode, data can also be transferred by a CPU instruction.

• Register list

Serial mode control status register (SMCS)

bit	15	14	13	12	11	10	9	8	Initial Value
Address : 000059H	SMD2	SMD1	SMD0	SIE	SIR	BUSY	STOP	STRT	00000010B
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R)	(R/W)	(R/W)	

bit	7	6	5	4	3	2	1	0	Initial Value
Address : 000058H	—	—	—	—	MODE	BDS	SOE	SCOE	XXXX0000B
	(—)	(—)	(—)	(—)	(R/W)	(R/W)	(R/W)	(R/W)	

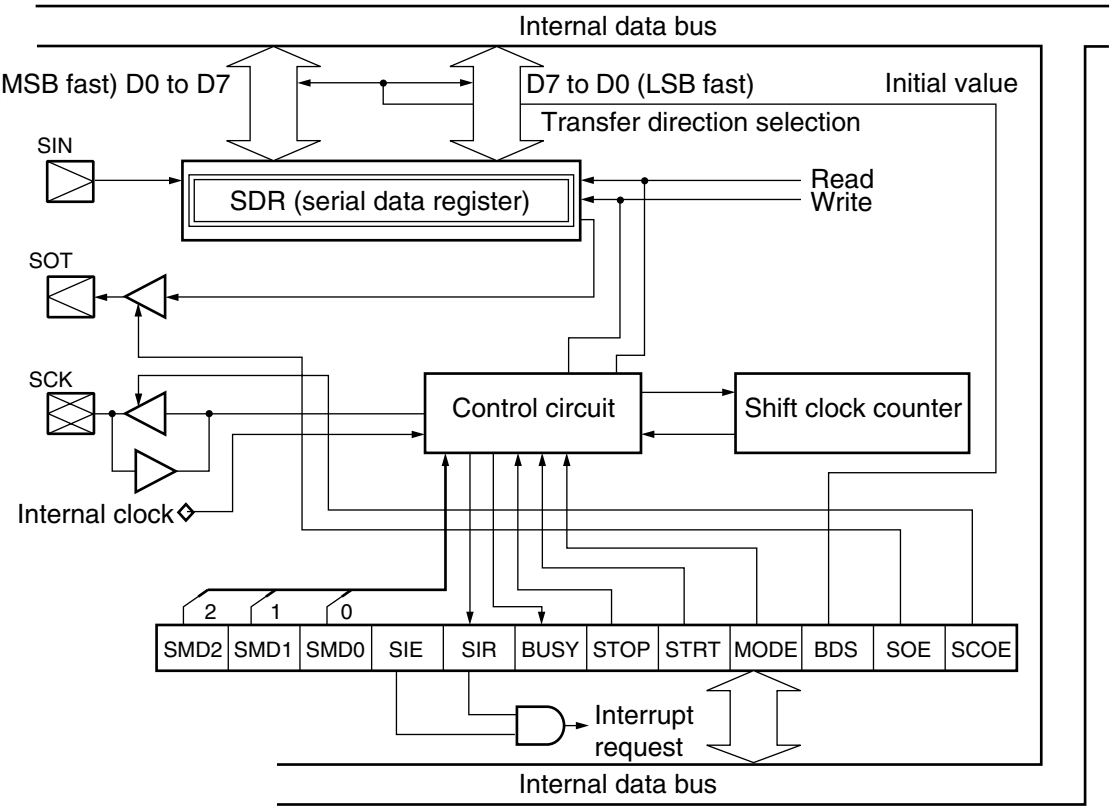
Serial data register (SDR)

bit	7	6	5	4	3	2	1	0	Initial Value
Address : 00005AH	D7	D6	D5	D4	D3	D2	D1	D0	XXXXXXXXB
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

Communication prescaler control register (SDCR)

bit	15	14	13	12	11	10	9	8	Initial Value
Address : 00005BH	MD	—	—	—	DIV3	DIV2	DIV1	DIV0	0XXX0000B
	(R/W)	(—)	(—)	(—)	(R/W)	(R/W)	(R/W)	(R/W)	

• Block Diagram



9. I²C Interface

The I²C interface is a serial I/O port supporting the Inter IC BUS. It serves as a master/slave device on the I²C bus and has the following features.

- Master/slave sending and receiving
- Arbitration function
- Clock synchronization function
- Slave address and general call address detection function
- Detecting transmitting direction function
- Start condition repeated generation and detection function
- Bus error detection function

• Register list

I²C bus status register (IBSR0 to IBSR2)

	bit	7	6	5	4	3	2	1	0	Initial Value
Address : 000070H 000076H 00007CH		BB	RSC	AL	LRB	TRX	AAS	GCA	FBT	00000000B
		(R)	(R)	(R)	(R)	(R)	(R)	(R)	(R)	

I²C bus control register (IBCR0 to IBCR2)

	bit	15	14	13	12	11	10	9	8	Initial Value
Address : 000071H 000077H 00007DH		BER	BEIE	SCC	MSS	ACK	GCAA	INTE	INT	00000000B
		(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

I²C bus clock control register (ICCR0 to ICCR2)

	bit	7	6	5	4	3	2	1	0	Initial Value
Address : 000072H 000078H 00007EH		—	—	EN	CS4	CS3	CS2	CS1	CS0	XX0XXXXXB
		(—)	(—)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

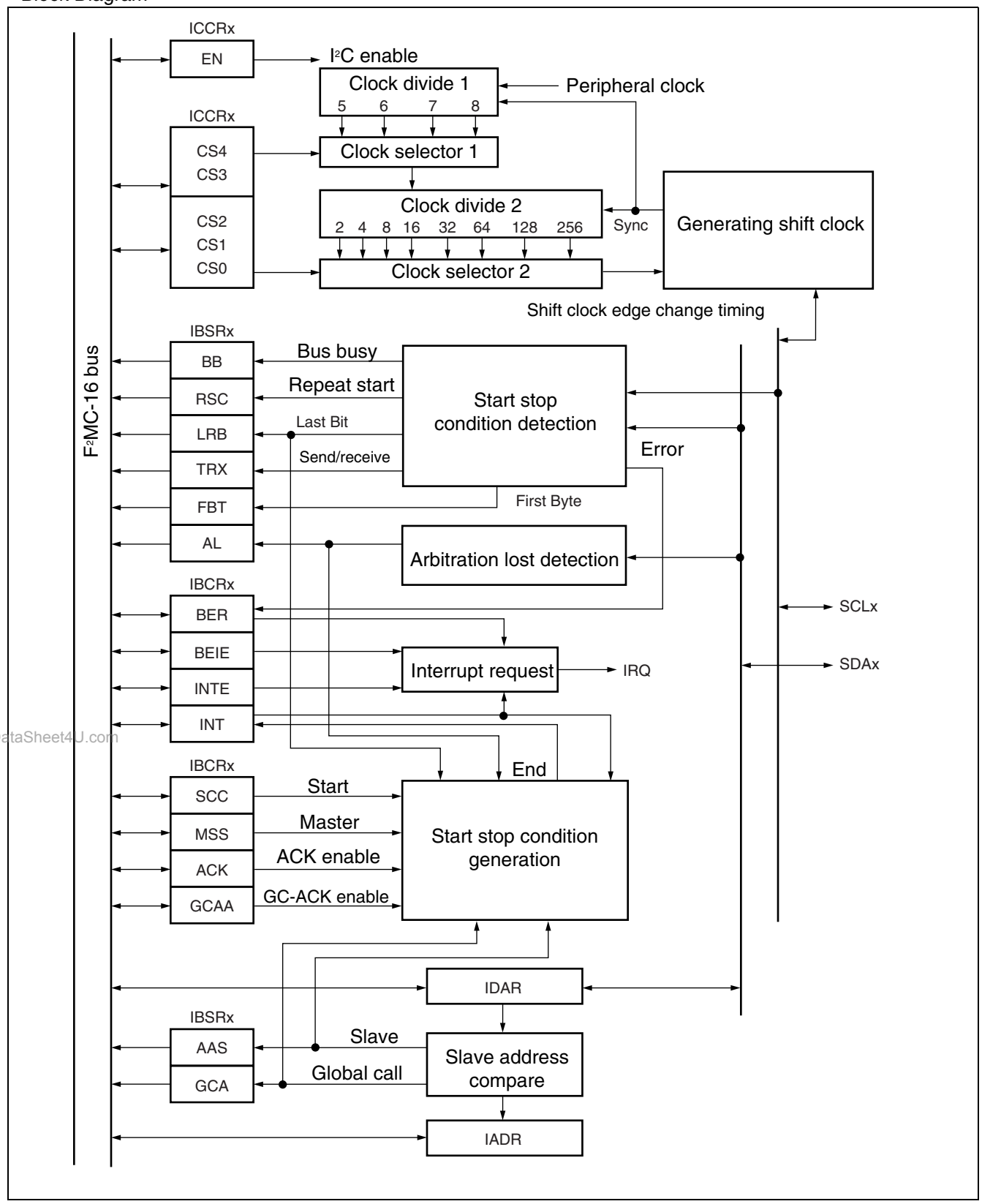
I²C bus address register (IADR0 to IADR2)

	bit	15	14	13	12	11	10	9	8	Initial Value
Address : 000073H 000079H 00007FH		—	A6	A5	A4	A3	A2	A1	A0	XXXXXXXXB
		(—)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

I²C bus data register (IDAR0 to IDAR2)

	bit	7	6	5	4	3	2	1	0	Initial Value
Address : 000074H 00007AH 000080H		D7	D6	D5	D4	D3	D2	D1	D0	XXXXXXXXB
		(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

• Block Diagram



10. USB Function

The USB function is an interface supporting the USB (Universal Serial Bus) communications protocol.

- Feature of USB function
  - Correspond to USB Full Speed
  - Full speed (12 Mbps) is supported.
  - The device status is auto-answer.
  - Bit stripping, bit stuffing, and automatic generation and check of CRC5 and CRC16
  - Toggle check by data synchronization bit
  - Automatic response to all standard commands except Get/SetDescriptor and SynchFrame commands (these 3 commands can be processed the same way as the class vendor commands).
  - The class vendor commands can be received as data and responded via firmware.
  - Supports up to 6 EndPoints (EndPoint0 is fixed to control transfer)
  - 2 transfer data buffers integrated for each end point (one IN buffer and one OUT buffer for EndPoint 0)
  - Supports automatic transfer mode for transfer data via DMA (except buffers for EndPoint 0)

- Register list

UDC control register (UDCC)

bit	7	6	5	4	3	2	1	0	Initial Value
Address : 0000D0H	RST	RESUM	$\overline{\text{HCON}}$	USTP	Reserved	Reserved	RFBK	PWC	10100000B
	(R/W)	(R/W)	(R/W)	(R/W)	(—)	(—)	(R/W)	(R/W)	

bit	15	14	13	12	11	10	9	8	Initial Value
Address : 0000D1H	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	00000000B
	(—)	(—)	(—)	(—)	(—)	(—)	(—)	(—)	

EP0 control register (EP0C)

bit	7	6	5	4	3	2	1	0	Initial Value
Address : 0000D2H	Reserved	PKS0	PKS0	PKS0	PKS0	PKS0	PKS0	PKS0	01000000B
	(—)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

bit	15	14	13	12	11	10	9	8	Initial Value
Address : 0000D3H	—	—	—	—	Reserved	Reserved	STAL	Reserved	XXXX0000B
	(—)	(—)	(—)	(—)	(—)	(—)	(R/W)	(—)	

EP1 control register (EP1C)

bit	7	6	5	4	3	2	1	0	Initial Value
Address : 0000D4H	PKS1	PKS1	PKS1	PKS1	PKS1	PKS1	PKS1	PKS1	00000000B
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

bit	15	14	13	12	11	10	9	8	Initial Value
Address : 0000D5H	EPEN	TYPE	TYPE	DIR	DMAE	NULE	STAL	PKS1	01100001B
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

(Continued)

EP2/3/4/5 control register (EP2C to EP5C)

bit	7	6	5	4	3	2	1	0	Initial Value
Address : 0000D6H 0000D8H 0000DAH 0000DCH	Reserved	PKS2 to 5	PKS2 to 5	PKS2 to 5	PKS2 to 5	PKS2 to 5	PKS2 to 5	PKS2 to 5	01000000B
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

bit	15	14	13	12	11	10	9	8	Initial Value
Address : 0000D7H 0000D9H 0000DBH 0000DDH	EPEN	TYPE	TYPE	DIR	DMAE	NULE	STAL	Reserved	01100000B
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

Time stamp register (TMSP)

bit	7	6	5	4	3	2	1	0	Initial Value
Address : 0000DEH	TMSP	TMSP	TMSP	TMSP	TMSP	TMSP	TMSP	TMSP	00000000B
	(R)	(R)	(R)	(R)	(R)	(R)	(R)	(R)	

bit	15	14	13	12	11	10	9	8	Initial Value
Address : 0000DFH	—	—	—	—	—	TMSP	TMSP	TMSP	XXXXX000B
	(—)	(—)	(—)	(—)	(—)	(R)	(R)	(R)	

UDC status register (UDCS)

bit	7	6	5	4	3	2	1	0	Initial Value
Address : 0000E0H	—	—	SUSP	SOF	BRST	WKUP	SETP	CONF	XX000000B
	(—)	(—)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

UDC Interrupt enable register (UDCIE)

bit	15	14	13	12	11	10	9	8	Initial Value
Address : 0000E1H	Reserved	Reserved	SUSPIE	SOFIE	BRSTIE	WKUPIE	CONFN	CONFIE	00000000B
	(—)	(—)	(R/W)	(R/W)	(R/W)	(R/W)	(R)	(R/W)	

EP0I status register (EP0IS)

bit	7	6	5	4	3	2	1	0	Initial Value
Address : 0000E2H	—	—	—	—	—	—	—	—	XXXXXXXXB
	(—)	(—)	(—)	(—)	(—)	(—)	(—)	(—)	

bit	15	14	13	12	11	10	9	8	Initial Value
Address : 0000E3H	BFINI	DRQIIE	—	—	—	DRQI	—	—	10XXX1XXB
	(R/W)	(R/W)	(—)	(—)	(—)	(R/W)	(—)	(—)	

(Continued)

(Continued)

EP0O status register (EP0OS)

Address : 0000E4H

bit	7	6	5	4	3	2	1	0	Initial Value
	Reserved	SIZE	SIZE	SIZE	SIZE	SIZE	SIZE	SIZE	0XXXXXXXB
	(—)	(R)	(R)	(R)	(R)	(R)	(R)	(R)	

Address : 0000E5H

bit	15	14	13	12	11	10	9	8	Initial Value
	BFINI	DRQOIE	SPKIE	—	—	DRQO	SPK	Reserved	100XX000B
	(R/W)	(R/W)	(R/W)	(—)	(—)	(R/W)	(R/W)	(—)	

EP1 status register (EP1S)

Address : 0000E6H

bit	7	6	5	4	3	2	1	0	Initial Value
	SIZE	SIZE	SIZE	SIZE	SIZE	SIZE	SIZE	SIZE	XXXXXXXXB
	(R)	(R)	(R)	(R)	(R)	(R)	(R)	(R)	

Address : 0000E7H

bit	15	14	13	12	11	10	9	8	Initial Value
	BFINI	DRQIE	SPKIE	Reserved	BUSY	DRQ	SPK	SIZE	1000000XB
	(R/W)	(R/W)	(R/W)	(—)	(R)	(R/W)	(R/W)	(R)	

EP2/3/4/5 status register (EP2S to EP5S)

Address : 0000E8H
0000EAH
0000ECH
0000EEH

bit	7	6	5	4	3	2	1	0	Initial Value
	Reserved	SIZE	SIZE	SIZE	SIZE	SIZE	SIZE	SIZE	XXXXXXXXB
	(—)	(R)	(R)	(R)	(R)	(R)	(R)	(R)	

Address : 0000E9H
0000EBH
0000EDH
0000EFH

bit	15	14	13	12	11	10	9	8	Initial Value
	BFINI	DRQIE	SPKIE	Reserved	BUSY	DRQ	SPK	Reserved	10000000B
	(R/W)	(R/W)	(R/W)	(—)	(R)	(R/W)	(R/W)	(—)	

EP0/1/2/3/4/5 data register (EP0DT to EP5DT)

Address : 0000F0H
0000F2H
0000F4H
0000F6H
0000F8H
0000FAH

bit	7	6	5	4	3	2	1	0	Initial Value
	BFDT	BFDT	BFDT	BFDT	BFDT	BFDT	BFDT	BFDT	XXXXXXXXB
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

Address : 0000F1H
0000F3H
0000F5H
0000F7H
0000F9H
0000FBH

bit	15	14	13	12	11	10	9	8	Initial Value
	BFDT	BFDT	BFDT	BFDT	BFDT	BFDT	BFDT	BFDT	XXXXXXXXB
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

11. USB Mini-HOST

USB Mini-HOST provides minimal host operations required and is a function that enables data to be transferred to and from Device without PC intervention.

- Feature of USB Mini-HOST
  - Automatic detection of Low Speed/Full Speed transfer
  - Low Speed/Full Speed transfer support
  - Automatic detection of connection and cutting device
  - Reset sending function support to USB-bus
  - Support of IN/OUT/SETUP/SOF token
  - In-token handshake packet automatic transmission (excluding STALL)
  - Out-token handshake packet automatic detection
  - Supports a maximum packet length of 256 bytes.
  - Error (CRC error/toggle error/time-out) various supports
  - Wake-Up function support

- Differences between the USB HOST and USB Mini-HOST

		HOST	Mini-HOST
Hub support		○	×
Transfer	Bulk transfer	○	○
	Control transfer	○	○
	Interrupt transfer	○	○
	ISO transfer	○	×
Transfer speed	Low Speed	○	○
	Full Speed	○	○
PRE packet support		○	×
SOF packet support		○	○
Error	CRC error	○	○
	Toggle error	○	○
	Time-out	○	○
	Maximum packet < receive data	○	○
Detection of connection and cutting of device		○	○
Transfer speed detection		○	○

○ : Supported
× : Not supported

• Register list

Host control register 0 (HCNT0)

Address : 0000C0H

bit	7	6	5	4	3	2	1	0	Initial Value
	RWKIRE	URIRE	CMPIRE	CNNIRE	DIRE	SOFIRE	URST	HOST	00000000B
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

Host control register 1 (HCNT1)

Address : 0000C1H

bit	15	14	13	12	11	10	9	8	Initial Value
	Reserved	Reserved	Reserved	Reserved	Reserved	SOFSTEP	CANCEL	RETRY	00000001B
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

Host interruption register (HIRQ)

Address : 0000C2H

bit	7	6	5	4	3	2	1	0	Initial Value
	TCAN	Reserved	RWKIRQ	URIRQ	CMPIRQ	CNNIRQ	DIRQ	SOFIRQ	00000000B
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

Host error status register (HERR)

Address : 0000C3H

bit	15	14	13	12	11	10	9	8	Initial Value
	LSTSOF	RERR	TOUT	CRC	TGERR	STUFF	HS	HS	00000011B
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

Host state status register (HSTATE)

Address : 0000C4H

bit	7	6	5	4	3	2	1	0	Initial Value
	—	—	ALIVE	CLKSEL	SOFBUSY	SUSP	TMODE	CSTAT	XX010010B
	(—)	(—)	(R/W)	(R/W)	(R/W)	(R/W)	(R)	(R)	

SOF interruption FRAME comparison register (HFCOMP)

Address : 0000C5H

bit	15	14	13	12	11	10	9	8	Initial Value
	FRAME COMP	FRAME COMP	FRAME COMP	FRAME COMP	FRAME COMP	FRAME COMP	FRAME COMP	FRAME COMP	00000000B
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

(Continued)

(Continued)

Retry timer setting register (HRTIMER)

Address : 0000C6H

bit	7	6	5	4	3	2	1	0	Initial Value
	RTIMER0	RTIMER0	RTIMER0	RTIMER0	RTIMER0	RTIMER0	RTIMER0	RTIMER0	00000000B
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

Address : 0000C7H

bit	15	14	13	12	11	10	9	8	Initial Value
	RTIMER1	RTIMER1	RTIMER1	RTIMER1	RTIMER1	RTIMER1	RTIMER1	RTIMER1	00000000B
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

Address : 0000C8H

bit	7	6	5	4	3	2	1	0	Initial Value
	—	—	—	—	—	—	RTIMER2	RTIMER2	XXXXXX00B
	(—)	(—)	(—)	(—)	(—)	(—)	(R/W)	(R/W)	

Host address register (HADR)

Address : 0000C9H

bit	15	14	13	12	11	10	9	8	Initial Value
	—	ADDRESS	ADDRESS	ADDRESS	ADDRESS	ADDRESS	ADDRESS	ADDRESS	X0000000B
	(—)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

EOF setting register (HEOF)

Address : 0000CAH

bit	7	6	5	4	3	2	1	0	Initial Value
	EOF0	EOF0	EOF0	EOF0	EOF0	EOF0	EOF0	EOF0	00000000B
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

Address : 0000CBH

bit	15	14	13	12	11	10	9	8	Initial Value
	—	—	EOF1	EOF1	EOF1	EOF1	EOF1	EOF1	XX000000B
	(—)	(—)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

FRAME setting register (HFRAME)

Address : 0000CCH

bit	7	6	5	4	3	2	1	0	Initial Value
	FRAME0	FRAME0	FRAME0	FRAME0	FRAME0	FRAME0	FRAME0	FRAME0	00000000B
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

Address : 0000CDH

bit	15	14	13	12	11	10	9	8	Initial Value
	—	—	—	—	—	FRAME1	FRAME1	FRAME1	XXXXX000B
	(—)	(—)	(—)	(—)	(—)	(R/W)	(R/W)	(R/W)	

Host token end point register (HTOKEN)

Address : 0000CEH

bit	7	6	5	4	3	2	1	0	Initial Value
	TGGL	TKNEN	TKNEN	TKNEN	ENDPT	ENDPT	ENDPT	ENDPT	00000000B
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

12. 8/10-bit A/D converter

The A/D converter converts analog input voltages into digital values and has the following features.

- RC sequential compare conversion method with sample and hold circuit
- Selectable 8-bit resolution or 10-bit resolution
- Analog input program-selectable from among 16 channels

Single conversion mode : Convert 1 selected channel

Scan conversion mode : Continuous plural channels (maximum 16 channels can be programmed) are converted.

Continuous conversion mode : Repeatedly convert the specified channels.

Stop conversion mode: Convert 1 channel then suspend conversion to remain on standby until the next activation (Simultaneous conversion start available).

- An interrupt request to the CPU can be generated upon completion of A/D conversion. Suitable for continuous processing as this interrupt activates μDMA to transfer the data resulting from A/D conversion to memory.
- The activation source can be selected from among software, external trigger (falling edge), and timer (rising edge).

• Register list

A/D control status register lower/upper (ADCS0/ADCS1)

bit	7	6	5	4	3	2	1	0	Initial Value
Address : 000040H	MD1	MD0	—	—	—	—	—	Reserved	00 - - - - - 0B
	(R/W)	(R/W)	(—)	(—)	(—)	(—)	(—)	(R/W)	

bit	15	14	13	12	11	10	9	8	Initial Value
Address : 000041H	BUSY	INT	INTE	PAUS	STS1	STS0	STRT	Reserved	00000000B
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(W)	(R/W)	

A/D data register lower/upper (ADCR0/ADCR1)

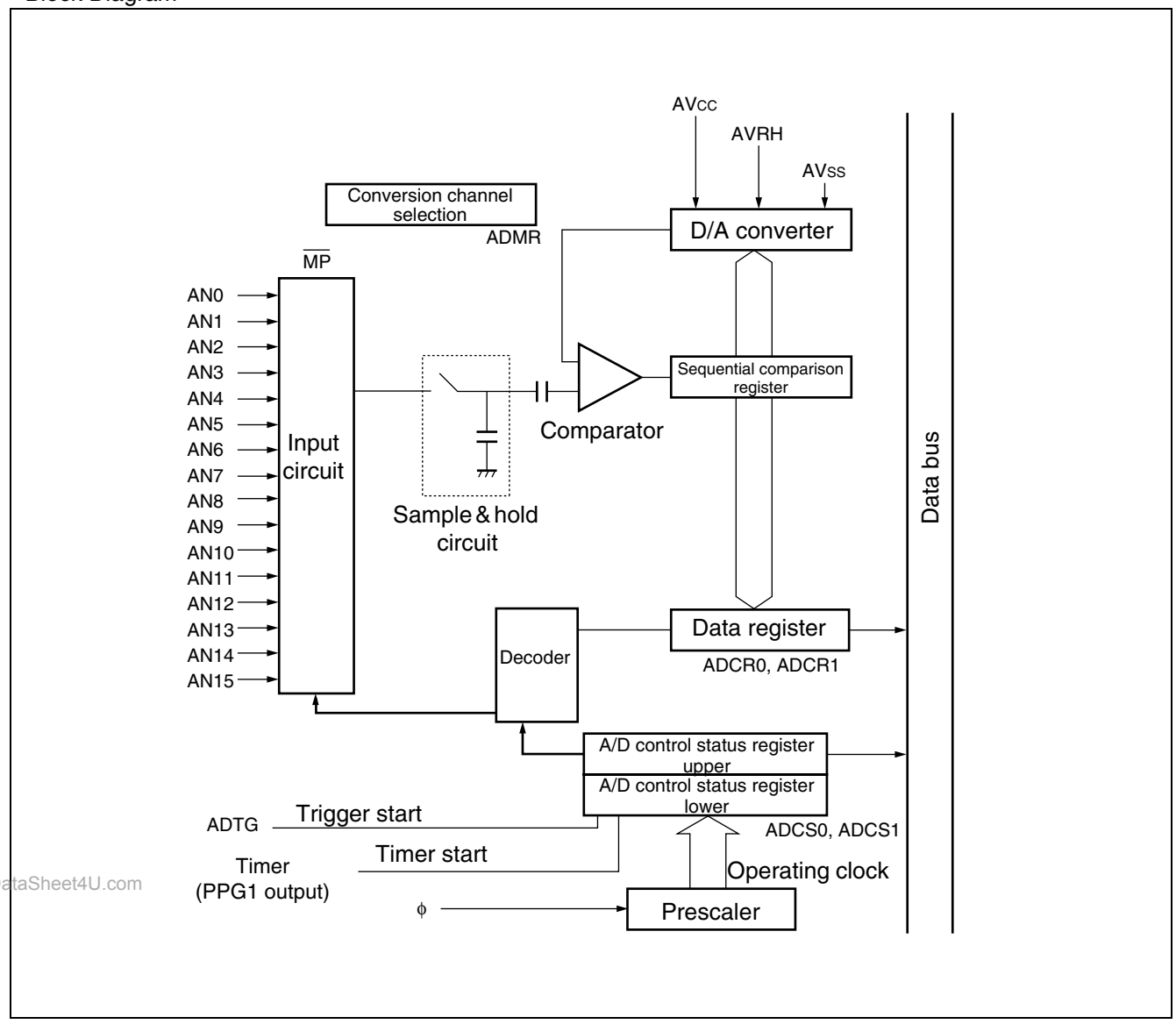
bit	7	6	5	4	3	2	1	0	Initial Value
Address : 000042H	D7	D6	D5	D4	D3	D2	D1	D0	XXXXXXXXB
	(R)	(R)	(R)	(R)	(R)	(R)	(R)	(R)	

bit	15	14	13	12	11	10	9	8	Initial Value
Address : 000043H	S10	ST1	ST0	CT1	CT0	—	D9	D8	00101XXXB
	(R/W)	(W)	(W)	(W)	(W)	(—)	(R)	(R)	

A/D conversion channel selection register (ADMR)

bit	15	14	13	12	11	10	9	8	Initial Value
Address : 000045H	ANS3	ANS2	ANS1	ANS0	ANE3	ANE2	ANE1	ANE0	00000000B
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

• Block Diagram



13. DTP/External interrupt circuit

DTP (Data Transfer Peripheral)/External interrupt circuit detects the interrupt request input from the external interrupt input terminal (INT7 to INT0) , and outputs the interrupt request.

- DTP/External interrupt circuit function

The DTP/External interrupt function outputs an interrupt request upon detection of the edge or level signal input to the external interrupt input pins (INT7 to INT0).

If CPU accepts the interrupt request, and if the extended intelligent I/O service (EI²OS) is enabled, branches to the interrupt handling routine after completing the automatic data transfer (DTP function) performed by EI²OS. And if EI²OS is disabled, it branches to the interrupt handling routine without activating the automatic data transfer (DTP function) performed by EI²OS.

- Overview of DTP/External interrupt circuit

	External interrupt	DTP function
Input pin	8 channels (P60/INT0, P61/INT1, P62/INT2/SIN, P63/INT3/SOT, P64/INT4/SCK, P65/INT5/PWC, P66/INT6/SCL0, P67/INT7/SDA0)	
Interrupt source	The detection level or the type of the edge for each terminal can be set in the request level setting register (ELVR).	
	Input of H level/L level/rising edge/falling edge.	
Interrupt number	#18 (12_H), #20 (14_H), #22 (16_H), #24 (18_H)	
Interrupt control	Enabling/disabling the interrupt request output using the DTP/interrupt enable register (ENIR)	
Interrupt flag	Holding the interrupt causes using the DTP/interrupt cause register (EIRR)	
Process setting	Disable EI²OS (ICR: ISE="0")	Enable EI²OS (ICR: ISE="1")
Process	Branched to the interrupt handling routine	After an automatic data transfer by EI²OS, branched to the interrupt handling routine

• Register list

DTP/Interrupt enable register (ENIR)

Address : 00003C$_H$

bit	7	6	5	4	3	2	1	0	Initial Value
	EN7	EN6	EN5	EN4	EN3	EN2	EN1	EN0	00000000$_B$
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

DTP/Interrupt source register (EIRR)

Address : 00003D$_H$

bit	15	14	13	12	11	10	9	8	Initial Value
	ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0	00000000$_B$
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

Request level setting register (ELVR)

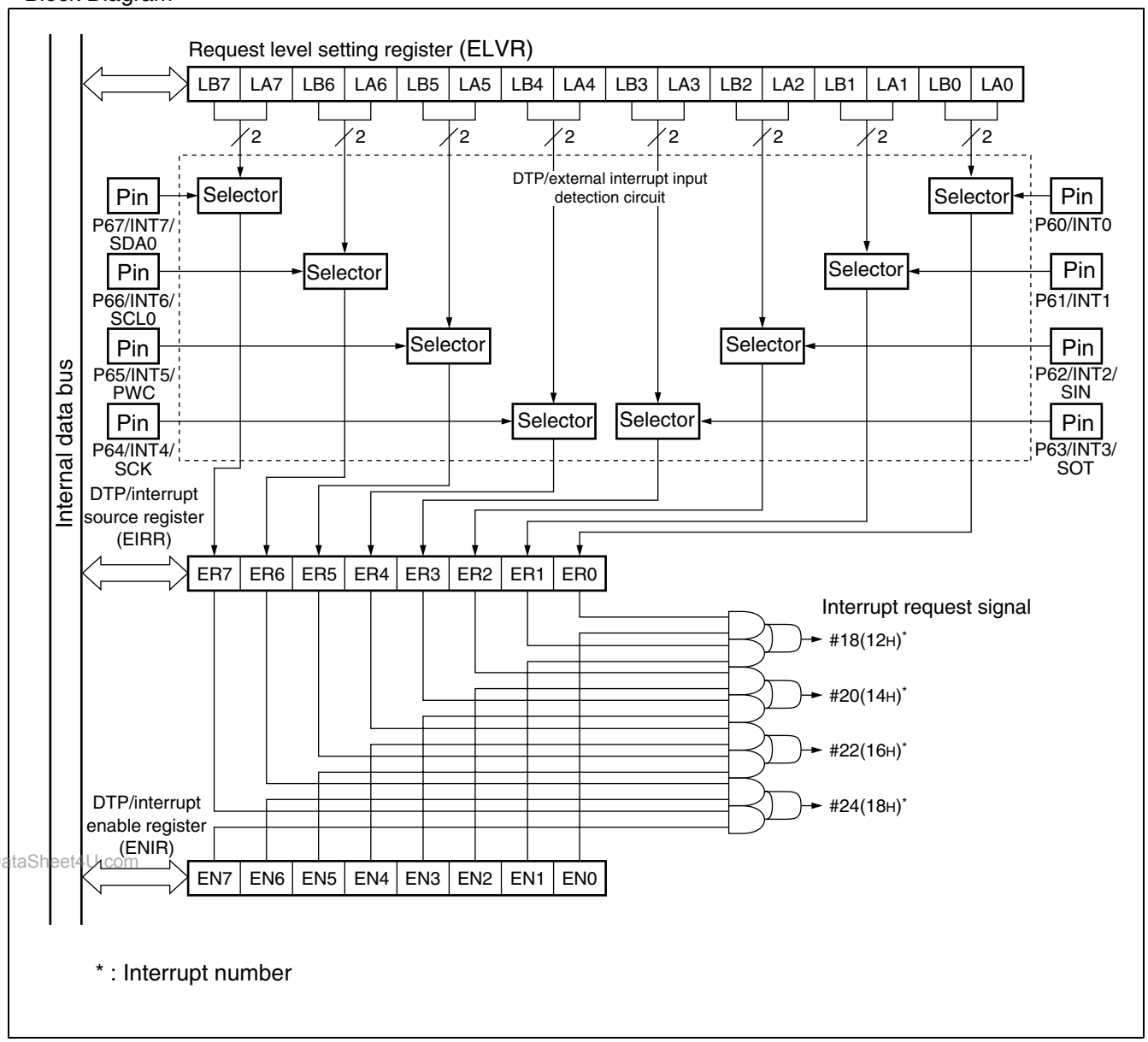
Address : 00003E$_H$

bit	7	6	5	4	3	2	1	0	Initial Value
	LB3	LA3	LB2	LA2	LB1	LA1	LB0	LA0	00000000$_B$
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

Address : 00003F$_H$

bit	15	14	13	12	11	10	9	8	Initial Value
	LB7	LA7	LB6	LA6	LB5	LA5	LB4	LA4	00000000$_B$
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

• Block Diagram



* : Interrupt number

14. Interrupt controller

The interrupt control register is located inside the interrupt controller; it exists for every I/O having an interrupt function. This register has the following functions.

- Setting of the interrupt levels of relevant resources

- Register list

Interrupt control register (ICR01, ICR03, ICR05, ICR07, ICR09, ICR11, ICR13, ICR15)

Address : ICR01 : 0000B1H
ICR03 : 0000B3H
ICR05 : 0000B5H
ICR07 : 0000B7H
ICR09 : 0000B9H
ICR11 : 0000BBH
ICR13 : 0000BDH
ICR15 : 0000BFH

bit	15	14	13	12	11	10	9	8	Initial Value
	ICS3	ICS2	ICS1	ICS0	ISE	IL2	IL1	IL0	00000111B
	(W)	(W)	(W)	(W)	(R/W)	(R/W)	(R/W)	(R/W)	

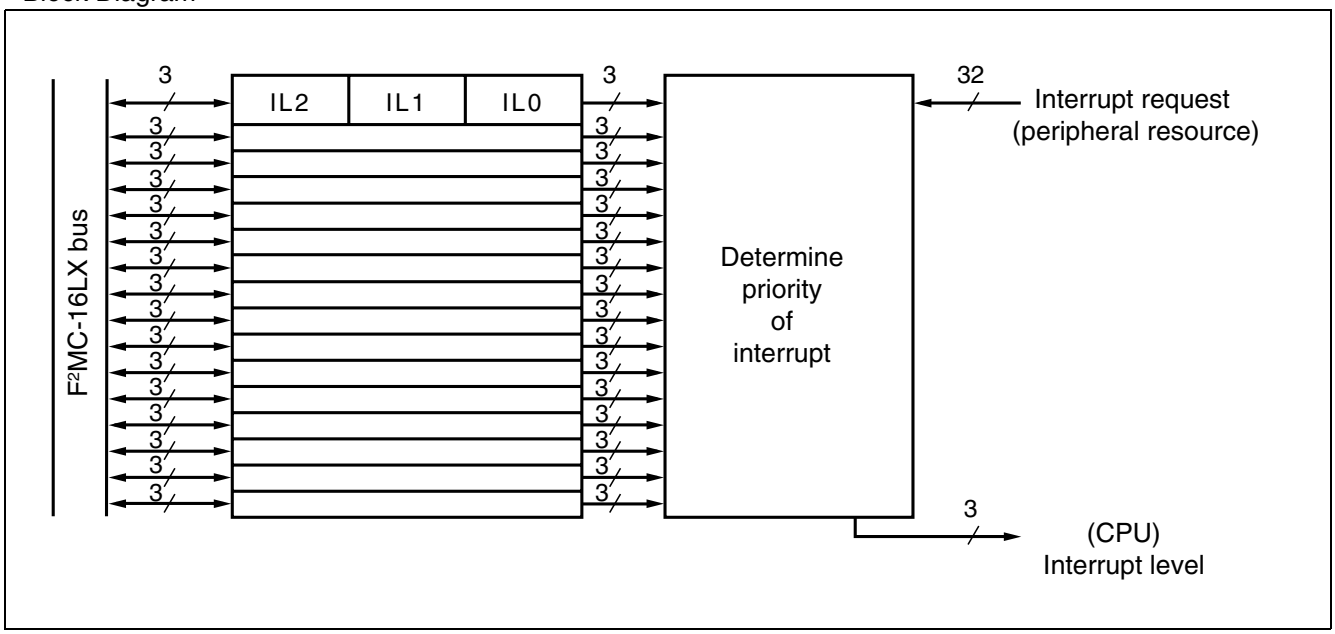
Interrupt control register (ICR00, ICR02, ICR04, ICR06, ICR08, ICR10, ICR12, ICR14)

Address : ICR00 : 0000B0H
ICR02 : 0000B2H
ICR04 : 0000B4H
ICR06 : 0000B6H
ICR08 : 0000B8H
ICR10 : 0000BAH
ICR12 : 0000BCH
ICR14 : 0000BEH

bit	7	6	5	4	3	2	1	0	Initial Value
	ICS3	ICS2	ICS1	ICS0	ISE	IL2	IL1	IL0	00000111B
	(W)	(W)	(W)	(W)	(R/W)	(R/W)	(R/W)	(R/W)	

Note : Do not access interrupt control registers using any read modify write instruction because it causes a malfunction.

• Block Diagram



15. μDMAC

μDMAC is simple DMA with the function equal with EI²OS. It has 16 channels DMA transfer channels with the following features.

- Performs automatic data transfer between the peripheral resource (I/O) and memory
- The program execution of CPU stops in the DMA start-up
- Capable of selecting whether to increment the transfer source and destination addresses
- DMA transfer is controlled by the DMA enable register, DMA stop status register, DMA status register, and descriptor.
- A STOP request is available for stopping DMA transfer from the resource.
  Upon completion of DMA transfer, the flag bit corresponding to the transfer completed channel in the DMA status register is set and a termination interrupt is output to the transfer controller.

• Register list

DMA enable register upper (DERH)

bit	15	14	13	12	11	10	9	8	Initial Value
Address : 0000AD$_H$	EN15	EN14	EN13	EN12	EN11	EN10	EN9	EN8	00000000$_B$
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

DMA enable register lower (DERL)

bit	7	6	5	4	3	2	1	0	Initial Value
Address : 0000AC$_H$	EN7	EN6	EN5	EN4	EN3	EN2	EN1	EN0	00000000$_B$
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

DMA stop status register (DSSR)

bit	7	6	5	4	3	2	1	0	Initial Value
Address : 0000A4$_H$	STP7 STP15	STP6 STP14	STP5 STP13	STP4 STP12	STP3 STP11	STP2 STP10	STP1 STP9	STP0 STP8	00000000$_B$
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	*

DMA status register upper (DSRH)

bit	15	14	13	12	11	10	9	8	Initial Value
Address : 00009D$_H$	DTE15	DTE14	DTE13	DTE12	DTE11	DTE10	DTE9	DTE8	00000000$_B$
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

DMA status register lower (DSRL)

bit	7	6	5	4	3	2	1	0	Initial Value
Address : 00009C$_H$	DTE7	DTE6	DTE5	DTE4	DTE3	DTE2	DTE1	DTE0	00000000$_B$
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

DMA descriptor channel specification register (DCSR)

bit	15	14	13	12	11	10	9	8	Initial Value
Address : 00009B$_H$	STP	Reserved	Reserved	Reserved	DCSR3	DCSR2	DCSR1	DCSR0	00000000$_B$
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

* : The DSSR is lower when the STP bit of DCSR in the DSSR is “0”.
The DSSR is upper when the STP bit of DCSR in the DSSR is “1”.

(Continued)

(Continued)

DMA buffer address pointer lower 8-bit (DBAPL)

Address : 007920H

bit	7	6	5	4	3	2	1	0	Initial Value
	DBAPL	DBAPL	DBAPL	DBAPL	DBAPL	DBAPL	DBAPL	DBAPL	XXXXXXXXB
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

DMA buffer address pointer middle 8-bit (DBAPM)

Address : 007921H

bit	15	14	13	12	11	10	9	8	Initial Value
	DBAPM	DBAPM	DBAPM	DBAPM	DBAPM	DBAPM	DBAPM	DBAPM	XXXXXXXXB
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

DMA buffer address pointer upper 8-bit (DBAPH)

Address : 007922H

bit	7	6	5	4	3	2	1	0	Initial Value
	DBAPH	DBAPH	DBAPH	DBAPH	DBAPH	DBAPH	DBAPH	DBAPH	XXXXXXXXB
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

DMA control register (DMACS)

Address : 007923H

bit	15	14	13	12	11	10	9	8	Initial Value
	RDY2	RDY1	BYTEL	IF	BW	BF	DIR	SE	XXXXXXXXB
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

DMA I/O register address pointer lower 8-bit (DIOAL)

Address : 007924H

bit	7	6	5	4	3	2	1	0	Initial Value
	A07	A06	A05	A04	A03	A02	A01	A00	XXXXXXXXB
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

DMA I/O register address pointer upper 8-bit (DIOAH)

Address : 007925H

bit	15	14	13	12	11	10	9	8	Initial Value
	A15	A14	A13	A12	A11	A10	A09	A08	XXXXXXXXB
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

DMA data counter lower 8-bit (DDCTL)

Address : 007926H

bit	7	6	5	4	3	2	1	0	Initial Value
	B07	B06	B05	B04	B03	B02	B01	B00	XXXXXXXXB
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

DMA data counter upper 8-bit (DDCTH)

Address : 007927H

bit	15	14	13	12	11	10	9	8	Initial Value
	B15	B14	B13	B12	B11	B10	B09	B08	XXXXXXXXB
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

Note : The above register is switched for each channel depending on the DCSR.

16. External bus pin control circuit

The external bus pin control circuit controls external bus pins to extend the CPU address and data buses to externals.

• Register list

• Automatic ready function selection register (ARSR)

Address : 0000A5H

bit	15	14	13	12	11	10	9	8	Initial Value
	ICR1	ICR0	HMR1	HMR0	—	—	LMR1	LMR0	0011- - 00B
	(W)	(W)	(W)	(W)	(—)	(—)	(W)	(W)	

• External address output control register (HACR)

Address : 0000A6H

bit	7	6	5	4	3	2	1	0	Initial Value
	E23	E22	E21	E20	E19	E18	E17	E16	********B
	(W)	(W)	(W)	(W)	(W)	(W)	(W)	(W)	

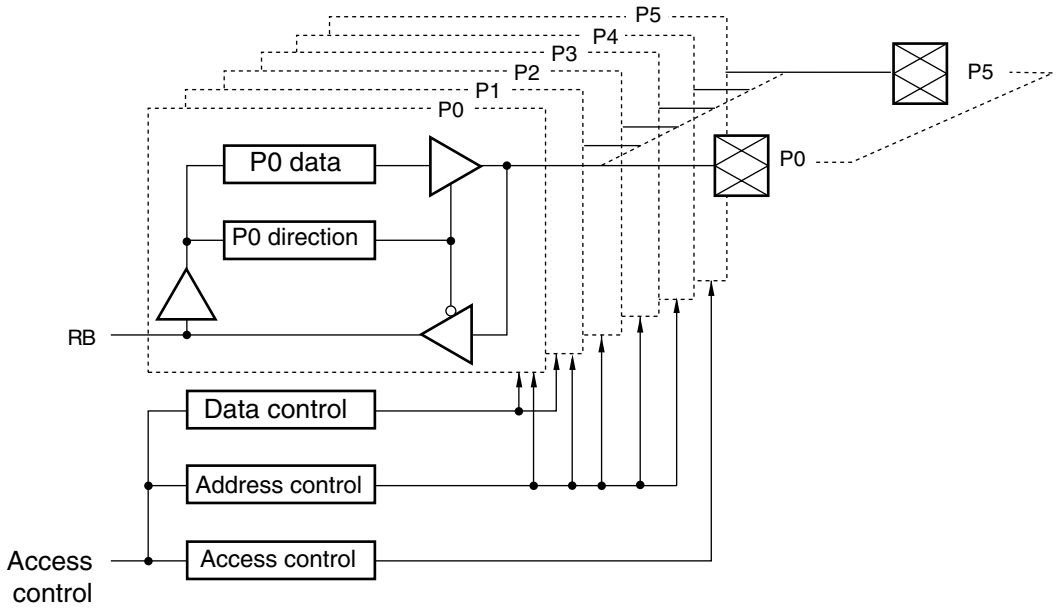
• Bus control signal selection register (EPCR)

Address : 0000A7H

bit	15	14	13	12	11	10	9	8	Initial Value
	CKE	RYE	HDE	Reserved	HMBS	(W)RE	LMBS	—	1000*10 -B
	(W)	(W)	(W)	(W)	(W)	(W)	(W)	(—)	

W :Write only
– :Unused
* :“1” or “0”

• Block Diagram



17. Address matching detection function

When the address is equal to the value set in the address detection register, the instruction code to be read into the CPU is forcibly replaced with the INT9 instruction code (01_H). As a result, the CPU executes the INT9 instruction when executing the set instruction. By performing processing by the INT#9 interrupt routine, the program patch function is enabled.

2 address detection registers are provided, for each of which there is an interrupt enable bit. When the address matches the value set in the address detection register with the interrupt enable bit set to 1, the instruction code to be read into the CPU is forcibly replaced with the INT9 instruction code.

• Register list

• Program address detect register 0 to 2 (PADR0)

PADR0 (lower) bit

Address : $001FF0_H$

7	6	5	4	3	2	1	0
(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)

Initial Value $XXXXXXXX_B$

PADR0 (middle) bit

Address : $001FF1_H$

15	14	13	12	11	10	9	8
(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)

Initial Value $XXXXXXXX_B$

PADR0 (upper) bit

Address : $001FF2_H$

7	6	5	4	3	2	1	0
(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)

Initial Value $XXXXXXXX_B$

• Program address detect register 3 to 5 (PADR1)

PADR1 (lower) bit

Address : $001FF3_H$

15	14	13	12	11	10	9	8
(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)

Initial Value $XXXXXXXX_B$

PADR1 (middle) bit

Address : $001FF4_H$

7	6	5	4	3	2	1	0
(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)

Initial Value $XXXXXXXX_B$

PADR1 (upper) bit

Address : $001FF5_H$

15	14	13	12	11	10	9	8
(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)

Initial Value $XXXXXXXX_B$

• Program address detection control status register (PACSR)

PACSR bit

Address : $00009E_H$

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	ADIE	Reserved	ADDE	Reserved
(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)

Initial Value 00000000_B

R/W : Readable and Writable
X : Undefined

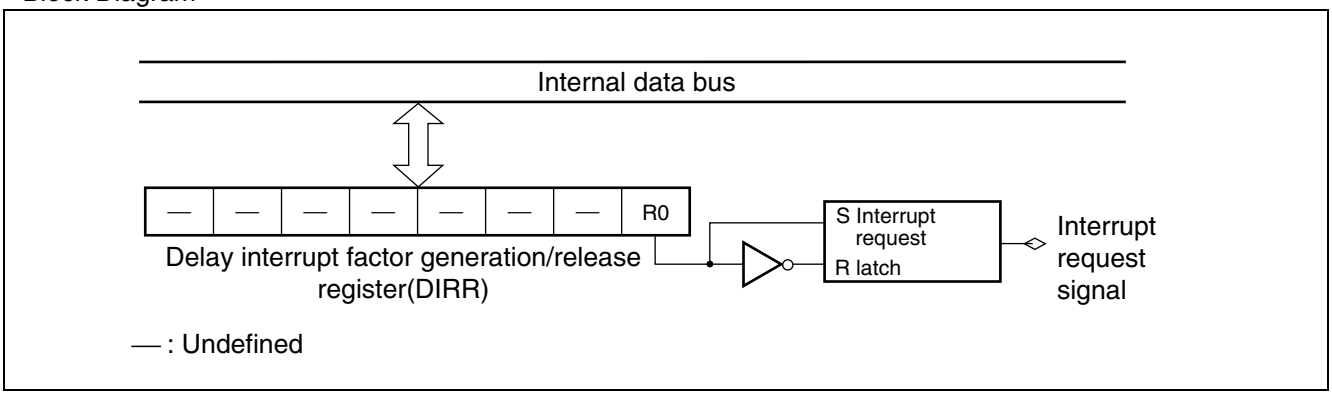
18. Delay interrupt generator module

The delay interrupt generation module is a module that generates interrupts for switching tasks. A hardware interrupt can be generated by software.

• Delay interrupt generator module function

	Function and control
Interrupt source	• Setting the R0 bit in the delayed interrupt request generation/release register to 1 (DIRR: R0 = 1) generates a delayed interrupt request. • Setting the R0 bit in the delayed interrupt request generation/release register to 0 (DIRR: R0 = 0) cancels the delayed interrupt request.
Interrupt control	No setting of permission register is provided.
Interrupt flag	Set in bit R0 of the delayed interrupt request generation /clear register (DIRR : R0)
EI²OS support	Not ready for extended intelligent I/O service (EI²OS).

• Block Diagram



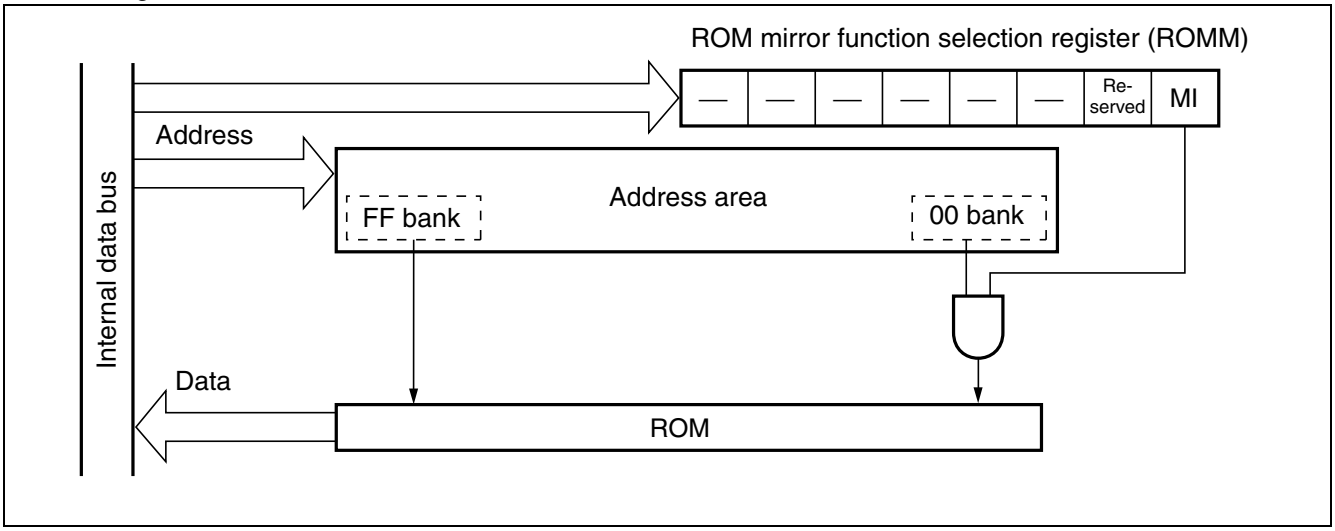
19. ROM mirror function selection module

The ROM mirror function select module can make a setting so that ROM data located in bank FF can be read by accessing bank 00.

• ROM mirroring function selection module function

	Description
Mirror setting address	FFFFFF$_H$ to FF8000$_H$ in the FF bank can be read through 00FFFF$_H$ to 008000$_H$ in the 00 bank.
Interrupt source	None.
EI^{2}OS support	Not ready for extended intelligent I/O service (EI^{2}OS) .

• Block Diagram



20. Low power consumption (standby) mode

The F²MC-16LX can be set to save power consumption by selecting and setting the low power consumption mode.

• CPU operation mode and functional description

CPU operating clock	Operation mode	Description
PLL clock	Normal run	The CPU and peripheral resources operate at the clock frequency obtained by PLL multiplication of oscillator clock (HCLK) frequency.
	Sleep	Only peripheral resources operate at the clock frequency obtained by PLL multiplication of the oscillator clock (HCLK) .
	Time-base timer	Only the time-base timer operates at the clock frequency obtained by PLL multiplication of the oscillator clock (HCLK) frequency.
	Stop	The CPU and peripheral resources are suspended with the oscillator clock stopped.
Main clock	Normal run	The CPU and peripheral resources operate at the clock frequency obtained by dividing the oscillator clock (HCLK) frequency by two.
	Sleep	Only peripheral resources operate at the clock frequency obtained by dividing the oscillator clock (HCLK) frequency by two.
	Time-base timer	Only the time-base timer operates at the clock frequency obtained by dividing the oscillator clock (HCLK) frequency by two.
	Stop	The CPU and peripheral resources are suspended with the oscillator clock stopped.
Sub clock	Normal run	The CPU and peripheral resources operate at the clock frequency obtained by dividing the sub clock (SCLK) frequency by four.
	Sleep	Only peripheral resources operate at the clock frequency obtained by dividing the sub clock (SCLK) frequency by four.
	Watch mode	Only the watch timer operates at the clock frequency obtained by dividing the sub clock (SCLK) frequency by four.
	Stop	The CPU and peripheral resources are suspended with the sub clock stopped.
CPU intermittent operation mode	Normal run	The halved or PLL-multiplied oscillator clock (HCLK) frequency or the sub clock (SCLK) frequency is used for operation while being decimated in a certain period.

• Register list

Low power consumption mode control register (LPMCR)

Address : 0000A0H

bit	7	6	5	4	3	2	1	0
	STP	SLP	SPL	RST	TMD	CG1	CG0	Reserved
	(W)	(W)	(R/W)	(W)	(R/W)	(R/W)	(R/W)	(R/W)

Initial Value
00011000B

21. Clock

The clock generator controls the internal clock as the operating clock for the CPU and peripheral resources. The internal clock is referred to as machine clock whose one cycle is defined as machine cycle. The clock based on source oscillation is referred to as oscillator clock while the clock based on internal PLL oscillation is referred to as PLL clock.

• Register list

Clock selection register (CKSCR)

Address : 0000A1H

bit	15	14	13	12	11	10	9	8	Initial Value
	SCM	MCM	WS1	WS0	SCS	MCS	CS1	CS0	11111100B
	(R)	(R)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

22. 3 Mbits flash memory

This section explains the flash memory built in the MB90F334A. Therefore, it is not applicable to evaluation ROM or MASK ROM.

The flash memory is located in bank FF in the CPU memory map.

• Function of flash memory

	Description
Memory capacity	3072 Kbits (384 Kbytes)
Memory configuration	384 Kwords × 8 bits/192 Kwords × 16 bits
Sector configuration	64 Kbytes × 5 + 32 Kbytes + 8 Kbytes × 2 + 16 Kbytes
Sector protect function	Capable of setting up with a recommendation parallel writer
Program algorithm	Automatic program algorithm (Embedded Algorithm : Similar to MBM29LV400TC)
Operation command	• Compatibility with the JEDEC standard-type command • Built-in function of erase pause/erasure resume • Detection of programming/erasure completion using data polling and the toggle bit • Capable of erasing data sector by sector (in arbitrary combination of sectors)
Program/Erase cycle	At least 10000 times guaranteed
How to program and erase memory	• Parallel programmer available for programming and erasure • Write/erase operation with a dedicated serial writer • Write/erase operation by program execution
Interrupt source	Programming/erasure completion sources
EI²OS supports	Not ready for expanded intelligent I/O service (EI²OS).

• Sector configuration of flash memory

Flash Memory	CPU address	Writer address *
Prohibited	F80000H F8FFFFH	00000H 0FFFFH
SA0 (64 Kbytes)	F90000H F9FFFFH	10000H 1FFFFH
SA1 (64 Kbytes)	FA0000H FAFFFFH	20000H 2FFFFH
SA2 (64 Kbytes)	FB0000H FBFFFFH	30000H 3FFFFH
Prohibited	FC0000H FCFFFFH	40000H 4FFFFH
SA3 (64 Kbytes)	FD0000H FDFFFFH	50000H 5FFFFH
SA4 (64 Kbytes)	FE0000H FEFFFFH	60000H 6FFFFH
SA5 (32 Kbytes)	FF0000H FF7FFFH	70000H 77FFFH
SA6 (8 Kbytes)	FF8000H FF9FFFH	78000H 79FFFH
SA7 (8 Kbytes)	FFA000H FFBFFFH	7A000H 7BFFFH
SA8 (16 Kbytes)	FFC000H FFFFFFH	7C000H 7FFFFH

* : The writer address is relative to the CPU address when data is programmed into flash memory by a parallel programmer. Programming and erasing by the general-purpose parallel programmer are executed based on writer addresses.

• Register list

Flash memory control status register (FMCS)

Address : 0000AEH

bit	7	6	5	4	3	2	1	0
	INTE	RDYINT	WE	RDY	Reserved	Reserved	Reserved	Reserved
	(R/W)	(R/W)	(R/W)	(R)	(W)	(W)	(W)	(W)

Initial Value
000X0000B

23. 4 Mbits flash memory

This section explains the flash memory built in the MB90F335A. Therefore, it is not applicable to evaluation ROM or MASK ROM.

The flash memory is located in bank FF in the CPU memory map.

• Function of flash memory

	Description
Memory capacity	4096 Kbits (512 Kbytes)
Memory configuration	512 Kwords × 8 bits/256 Kwords × 16 bits
Sector configuration	64 Kbytes × 6 + 32 Kbytes × 2 + 8 Kbytes × 4 + 16 Kbytes × 2
Sector protect function	Capable of setting up with a recommendation parallel writer
Program algorithm	Automatic program algorithm (Embedded Algorithm : Similar to MBM29LV400TC)
Operation command	• Compatibility with the JEDEC standard-type command •Built-in function of erase pause/erasure resume • Detection of programming/erasure completion using data polling and the toggle bit • Capable of erasing data sector by sector (in arbitrary combination of sectors)
Program/Erase cycle	At least 10000 times guaranteed
How to program and erase memory	• Parallel programmer available for programming and erasure • Write/erase operation with a dedicated serial writer • Write/erase operation by program execution
Interrupt source	Programming/erasure completion sources
EI²OS supports	Not ready for expanded intelligent I/O service (EI²OS).

• Sector configuration of flash memory

Flash Memory	CPU address	Writer address *
SA0 (64 Kbytes)	F80000H F8FFFFH	00000H 0FFFFH
SA1 (64 Kbytes)	F90000H F9FFFFH	10000H 1FFFFH
SA2 (64 Kbytes)	FA0000H FAFFFFH	20000H 2FFFFH
SA3 (32Kbytes)	FB0000H FB7FFFH	30000H 37FFFH
SA4 (8 Kbytes)	FB8000H FB9FFFH	38000H 39FFFH
SA5 (8 Kbytes)	FBA000H FBBFFFH	3A000H 3BFFFH
SA6 (16 Kbytes)	FBC000H FBFFFFH	3C000H 3FFFFH
SA7 (64 Kbytes)	FC0000 FCFFFF	40000H 4FFFFH
SA8 (64 Kbytes)	FD0000 FDFFFF	50000H 5FFFFH
SA9 (64 Kbytes)	FE0000H FEFFFFH	60000H 6FFFFH
SA10 (32 Kbytes)	FF0000H FF7FFFH	70000H 77FFFH
SA11 (8 Kbytes)	FF8000H FF9FFFH	78000H 79FFFH
SA12 (8 Kbytes)	FFA000H FFBFFFH	7A000H 7BFFFH
SA13 (16 Kbytes)	FFC000H FFFFFFH	7C000H 7FFFFH

* : The writer address is relative to the CPU address when data is programmed into flash memory by a parallel programmer. Programming and erasing by the general-purpose parallel programmer are executed based on writer addresses.

• Register list

Flash memory control status register (FMCS)

Address : 0000AEH

bit	7	6	5	4	3	2	1	0
	INTE	RDYINT	WE	RDY	Reserved	Reserved	Reserved	Reserved
	(R/W)	(R/W)	(R/W)	(R)	(W)	(W)	(W)	(W)

Initial Value
000X0000B

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V_{CC}	V_{SS} – 0.3	V_{SS} + 4.0	V	
	AV_{CC}	V_{SS} – 0.3	V_{SS} + 4.0	V	$V_{CC} \geq AV_{CC}$*2
	AVRH	V_{SS} – 0.3	V_{SS} + 4.0	V	$AV_{CC} \geq AVR \geq 0$ V*3
Input voltage*1	V_I	V_{SS} – 0.3	V_{SS} + 4.0	V	*4
		V_{SS} – 0.3	V_{SS} + 6.0	V	N-ch open-drain (Withstand voltage of 5 V I/O)*5
		– 0.5	V_{SS} + 4.5	V	USB I/O
Output voltage*1	V_O	V_{SS} – 0.3	V_{SS} + 4.0	V	*4
		– 0.5	V_{SS} + 4.5	V	USB I/O
Maximum clamp current	I_{CLAMP}	– 2.0	+2.0	mA	*6
Total maximum clamp current	$\Sigma \lvert I_{CLAMP} \rvert$	—	20	mA	*6
“L” level maximum output current	I_{OL1}	—	10	mA	Other than USB I/O*7
	I_{OL2}	—	43	mA	USB I/O*7
“L” level average output current	I_{OLAV1}	—	4	mA	*8
	I_{OLAV2}	—	15/4.5	mA	USB-IO (Full speed/ Low speed) *8
“L” level maximum total output current	ΣI_{OL}	—	100	mA	
“L” level average total output current	ΣI_{OLAV}	—	50	mA	*9
“H” level maximum output current	I_{OH1}	—	– 10	mA	Other than USB I/O*7
	I_{OH2}	—	– 43	mA	USB I/O*7
“H” level average output current	I_{OHAV1}	—	– 4	mA	*8
	I_{OHAV2}	—	–15/–4.5	mA	USB-IO (Full speed/ Low speed) *8
“H” level maximum total output current	ΣI_{OH}	—	– 100	mA	
“H” level average total output current	ΣI_{OHAV}	—	– 50	mA	*9
Power consumption	Pd	—	340	mW	
Operating temperature	T_A	– 40	+ 85	°C	
Storage temperature	Tstg	– 55	+ 150	°C	
		– 55	+ 125	°C	USB I/O

*1 : The parameter is based on $V_{SS} = AV_{SS} = 0.0$ V.

*2 : Be careful not to let AV_{CC} exceed V_{CC}, for example, when the power is turned on.

*3 : Be careful not to let AVRH exceed AVcc.

*4 : V_I and V_O must not exceed Vcc + 0.3 V. However, if the maximum current to/from an input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating.

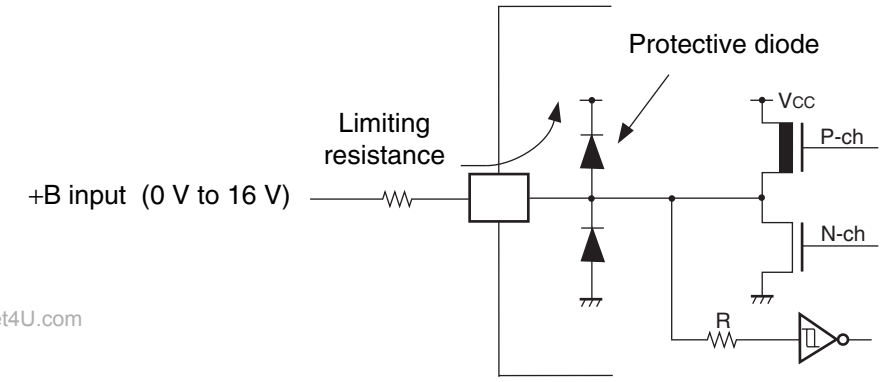
*5 : Applicable to pins : P60 to P67, P96, PA0 to PA7, PB0 to PB4, UTEST

(Continued)

(Continued)

*6 :
- Applicable to pins: P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P70 to P77, P80 to P87, P90 to P95, PB5, PB6
- Use within recommended operating conditions.
- Use at DC voltage (current)
- The +B signal should always be applied a limiting resistance placed between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V) , the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on reset.
- Care must be taken not to leave the +B input pin open.
- Note that analog system input/output pins other than P60 to P67, P96, PA0 to PA7, PB0 to PB4, DVP, DVM, HVP, HVM, UTEST, $\overline{HCON}$
- Sample recommended circuits:

• Input/output equivalent circuits



*7 : A peak value of an applicable one pin is specified as a maximum output current.

*8 : The average output current specifies the mean value of the current flowing in the relevant single pin during a period of 100 ms.

*9 : The average total output current specifies the mean value of the currents flowing in all of the relevant pins during a period of 100 ms.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

(V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC}	3.0	3.6	V	At normal operation (when using USB)
		2.7	3.6	V	At normal operation (when not using USB)
		1.8	3.6	V	Hold state of stop operation
Input “H” voltage	V_{IH}	0.7 V_{CC}	V_{CC} + 0.3	V	CMOS input pin
	V_{IHS1}	0.8 V_{CC}	V_{CC} + 0.3	V	CMOS hysteresis input pin
	V_{IHS2}	0.8 V_{CC}	V_{SS} + 5.3	V	N-ch open-drain (Withstand voltage of 5 V I/O)*
	V_{IHM}	V_{CC} – 0.3	V_{CC} + 0.3	V	MD pin input
	V_{IHUSB}	2.0	V_{CC} + 0.3	V	USB pin input
Input “L” voltage	V_{IL}	V_{SS} – 0.3	0.3 V_{CC}	V	CMOS input pin
	V_{ILS}	V_{SS} – 0.3	0.2 V_{CC}	V	CMOS hysteresis input pin
	V_{ILM}	V_{SS} – 0.3	V_{SS} + 0.3	V	MD pin input
	V_{ILUSB}	V_{SS}	0.8	V	USB pin input
Differential input sensitivity	V_{DI}	0.2	—	V	USB pin input
Differential common mode input voltage range	V_{CM}	0.8	2.5	V	USB pin input
Operating temperature	T_A	– 40	+ 85	°C	When not using USB
		0	+ 70	°C	When using USB

* : Applicable to pins : P60 to P67, P96, PA0 to PA7, PB0 to PB4, UTEST

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

3. DC Characteristics

(V_{CC} = AV_{CC} = 3.3 V ± 0.3 V, V_{SS} = AV_{SS} = 0.0 V, T_A = – 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Output "H" voltage	V_{OH}	Output pins other than P60 to P67, P96, PA0 to PA7, PB0 to PB4, HVP, HVM, DVP, DVM	I_{OH} = – 4.0 mA	V_{CC} – 0.5	—	Vcc	V	
		HVP, HVM, DVP, DVM	R_L = 15 kΩ ± 5%	2.8	—	3.6	V	
Output "L" voltage	V_{OL}	Output pins other than HVP, HVM, DVP, DVM	I_{OL} = 4.0 mA	Vss	—	Vss + 0.4	V	
		HVP, HVM, DVP, DVM	R_L = 1.5 kΩ ± 5%	0	—	0.3	V	
Input leak current	I_{IL}	Output pins other than P60 to P67, P96, PA0 to PA7, PB0 to PB4, HVP, HVM, DVP, DVM	V_{CC} = 3.3 V, Vss < V_I < V_{CC}	– 10	—	+ 10	µA	
		HVP, HVM, DVP, DVM	—	– 5	—	+ 5	µA	
Pull-up resistance	R_{PULL}	P00 to P07, P10 to P17	V_{CC} = 3.3 V, T_A = + 25 °C	25	50	100	kΩ	
Open drain output current	I_{LIOD}	P60 to P67, P96, PA0 to PA7, PB0 to PB4	—	—	0.1	10	µA	
Power supply current	I_{CC}	V_{CC}	V_{CC} = 3.3 V, Internal frequency 24 MHz, At normal operating At USB operating (USTP = 0)	—	75	85	mA	MB90F334A MB90F335A
				—	65	75	mA	MB90333A
			V_{CC} = 3.3 V, Internal frequency 24 MHz, At normal operating At non-operating USB (USTP = 1)	—	70	80	mA	MB90F334A MB90F335A
				—	60	70	mA	MB90333A
	I_{CCS}		V_{CC} = 3.3 V, Internal frequency 24 MHz, At sleep mode	—	27	40	mA	
	I_{CTS}		V_{CC} = 3.3 V, Internal frequency 24 MHz, At timer mode	—	3.5	10	mA	
			V_{CC} = 3.3 V, Internal frequency 3 MHz, At timer mode	—	1	2	mA	
	I_{CCL}		V_{CC} = 3.3 V, Internal frequency 8 kHz, At sub clock operation, (T_A = +25 °C)	—	25	150	µA	

(Continued)

(Continued)

(V_{CC} = AV_{CC} = 3.3 V ± 0.3 V, V_{SS} = AV_{SS} = 0.0 V, T_A = – 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current	I_{CCLS}	V_{CC}	V_{CC} = 3.3 V, Internal frequency 8 kHz, At sub clock, At sleep operating, (T_A = + 25 °C)	—	10	50	µA	
	I_{CCT}		V_{CC} = 3.3 V, Internal frequency 8 kHz, Watch mode, (T_A = + 25 °C)	—	1.5	40	µA	
	I_{CCH}		T_A = + 25 °C, At stop	—	1	40	µA	
Input capacitance	C_{IN}	Other than AVcc, AVss, Vcc, Vss	—	—	5	15	pF	
Pull-up resistor	R_{up}	$\overline{RST}$	—	25	50	100	kΩ	
USB I/O output impedance	Z_{USB}	DVP, DVM HVP, HVM	—	3	—	14	Ω	

Note : P60 to P67, P96, PA0 to PA7, and PB0 to PB4 are N-ch open-drain pins usually used as CMOS.

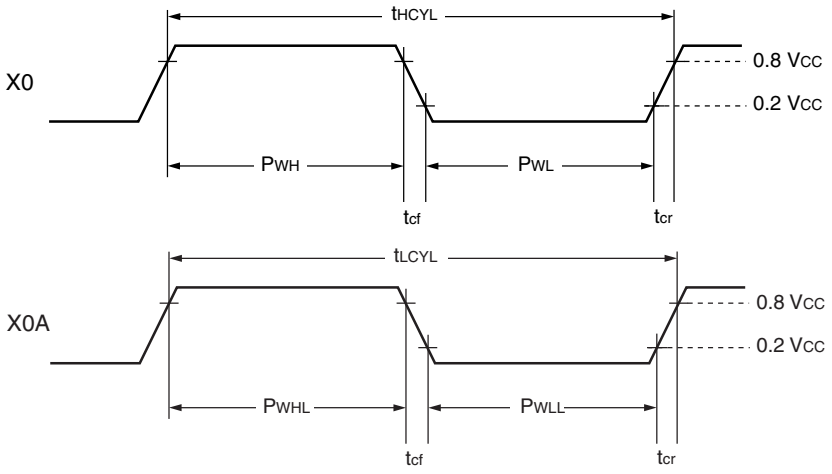
4. AC Characteristics

(1)Clock input timing

(V_{CC} = AV_{CC} = 3.3 V ± 0.3 V, V_{SS} = AV_{SS} = 0.0 V, T_A = – 40 °C to + 85 °C)

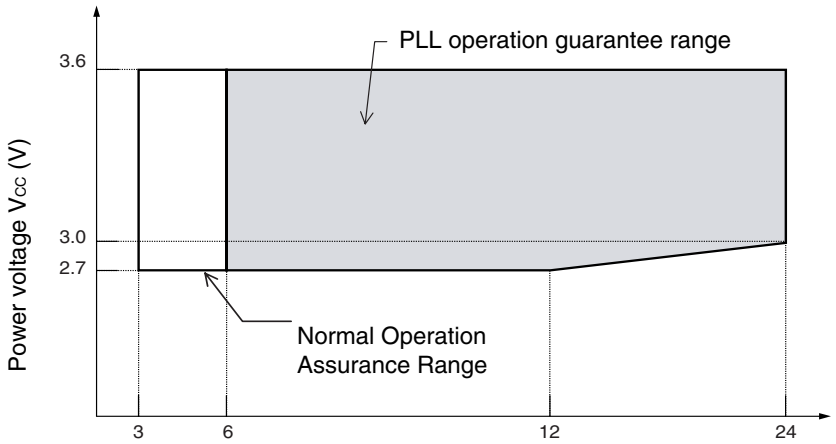
Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_{CH}	X0, X1	—	6	—	MHz	When oscillator is used
			6	—	24	MHz	External clock input
	f_{CL}	X0A, X1A	—	32.768	—	kHz	
Clock cycle time	t_{HCYL}	X0, X1	—	166.7	—	ns	When oscillator is used
			166.7	—	41.7	ns	External clock input
	t_{LCYL}	X0A, X1A	—	30.5	—	s	
Input clock pulse width	P_{WH} P_{WL}	X0	10	—	—	ns	A reference duty ratio is 30% to 70%.
	P_{WHL} P_{WLL}	X0A	—	15.2	—	s	
Input clock rise time and fall time	tcr tcf	X0	—	—	5	ns	At external clock
Internal operating clock frequency	f_{CP}	—	3	—	24	MHz	When main clock is used
	f_{CPL}	—	—	8.192	—	kHz	When sub clock is used
Internal operating clock cycle time	t_{CP}	—	42	—	333	ns	When main clock is used
	t_{CPL}	—	—	122.1	—	s	When sub clock is used

• Clock Timing



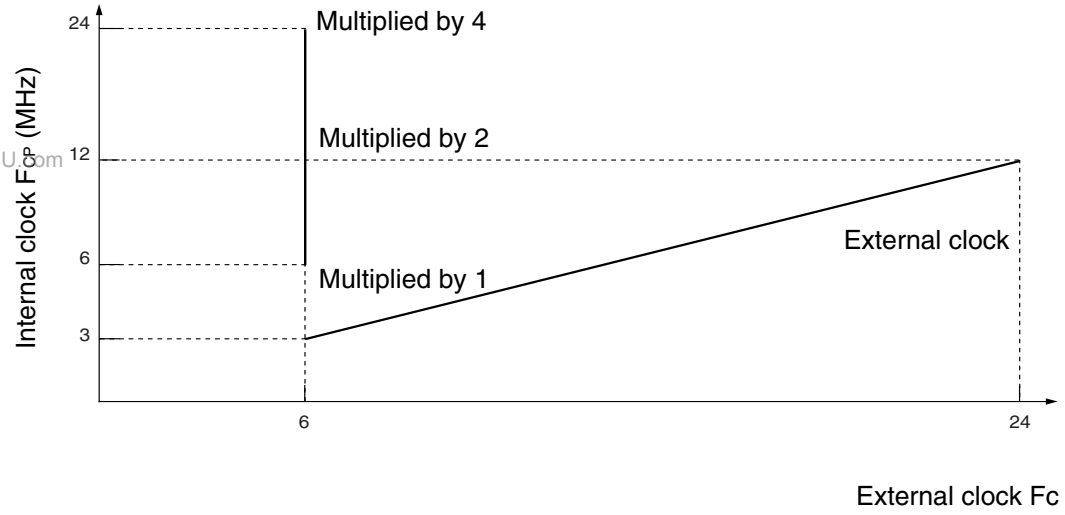
• PLL operation guarantee range

Relation between power supply voltage and internal operation clock frequency



Note : When the USB is used, operation is guaranteed at voltages between 3.0 V and 3.6 V.

Relation between internal operation clock frequency and external clock frequency



The AC standards assume the following measurement reference voltages.

- Input signal waveform

Hysteresis input pin

Hysteresis input/other than MD input pin

- Output signal waveform

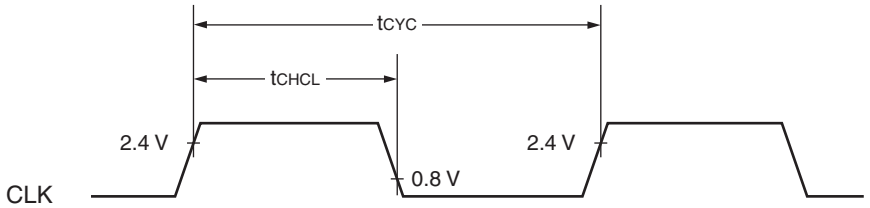
Output pin

(2)Clock output timing

(V_{SS} = AV_{SS} = 0.0 V, T_A = – 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Cycle time	t_{CYC}	CLK	—	t_{CP}	—	ns	
CLK↑→CLK↓	t_{CHCL}	CLK	V_{CC} = 3.0 V to 3.6 V	$t_{CP}/2$ – 15	$t_{CP}/2$ + 15	ns	At f_{cp} = 24 MHz
				$t_{CP}/2$ – 20	$t_{CP}/2$ + 20	ns	At f_{cp} = 12 MHz
				$t_{CP}/2$ – 64	$t_{CP}/2$ + 64	ns	At f_{cp} = 6 MHz

Note : t_{CP} : Refer to “ (1) Clock input timing”.



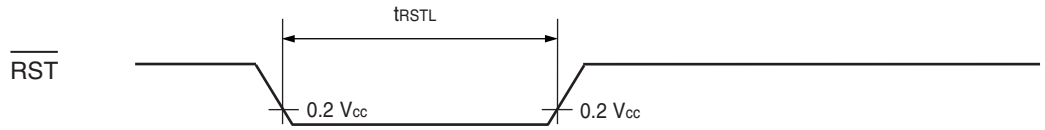
(3) Reset

(V_{CC} = AV_{CC} = 3.3 V ± 0.3 V, V_{SS} = AV_{SS} = 0.0 V, T_A = – 40 °C to + 85 °C)

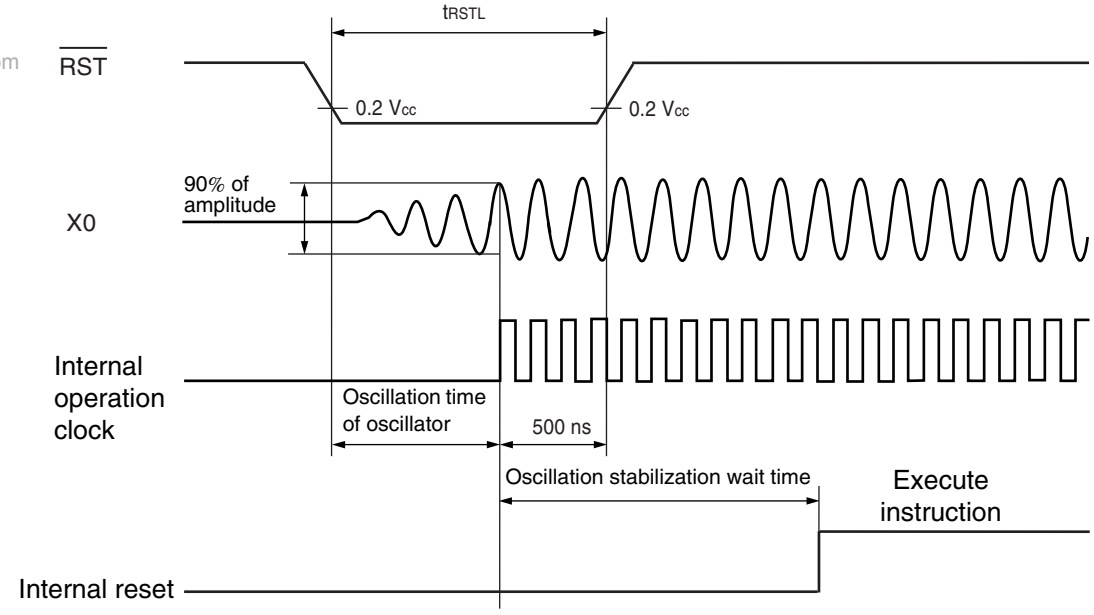
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Reset input time	t_{RSTL}	$\overline{RST}$	—	500	—	ns	At normal operating, At time base timer mode, At main sleep mode, At PLL sleep mode
				Oscillation time of oscillator* + 500 ns	—	µs	At stop mode, At sub clock mode, At sub sleep mode, At watch mode

* : Oscillation time of oscillator is the time that the amplitude reaches 90%. It takes several milliseconds to several dozens of milliseconds on a crystal oscillator, several hundreds of microseconds to several milliseconds on a ceramic oscillator, and 0 milliseconds on an external clock.

• During normal operation, time-base timer mode, main sleep mode and PLL sleep mode



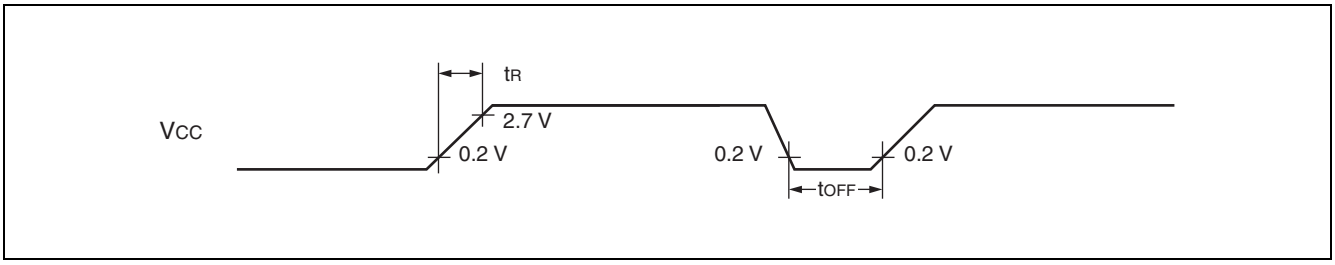
• During stop mode, sub clock mode, sub-sleep mode and watch mode



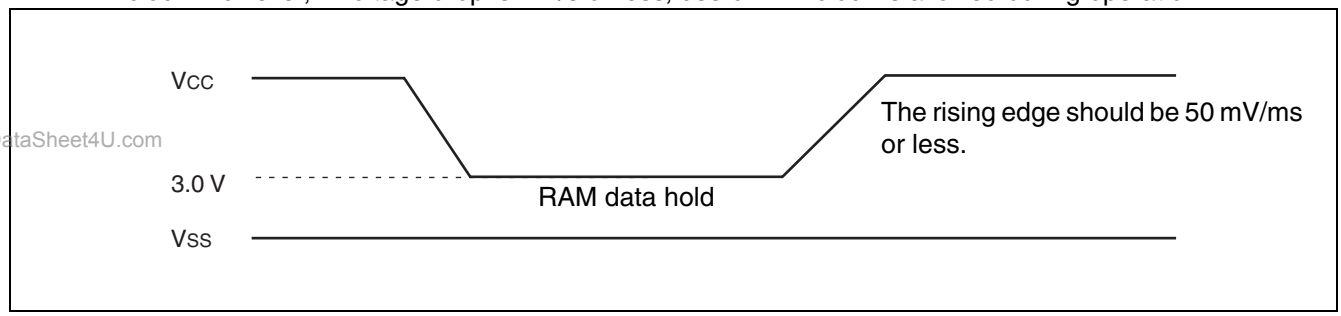
(4) Power-on reset

(V_{CC} = AV_{CC} = 3.3 V ± 0.3 V, V_{SS} = AV_{SS} = 0.0 V, T_A = – 40 °C to +85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Power supply rising time	t_R	V_{CC}	—	0.05	30	ms	
Power supply shutdown time	t_{OFF}	V_{CC}		1	—	ms	Waiting time until power-on



Notes :
- V_{CC} must be lower than 0.2 V before the power supply is turned on.
- The above standard is a value for performing a power-on reset.
- In the device, there are internal registers which is initialized only by a power-on reset. When the initialization of these items is expected, turn on the power supply according to the standards.
- Sudden change of power supply voltage may activate the power-on reset function. When changing the power supply voltage during operation as illustrated below, voltage fluctuation should be minimized so that the voltage rises as smoothly as possible. When raising the power, do not use PLL clock. However, if voltage drop is 1 V/s or less, use of PLL clock is allowed during operation.



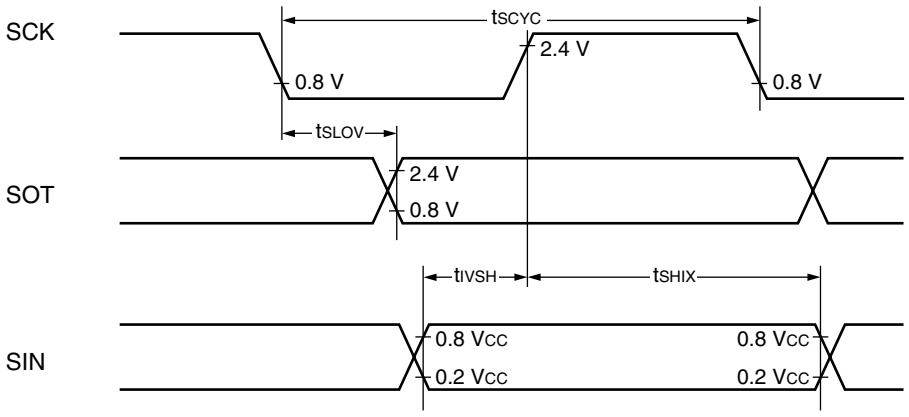
(5) UART0, UART1, UART2, UART3 I/O extended serial timing

(V_{CC} = AV_{CC} = 3.3 V ± 0.3 V, V_{SS} = AV_{SS} = 0.0 V, T_A = – 40 °C to + 85 °C)

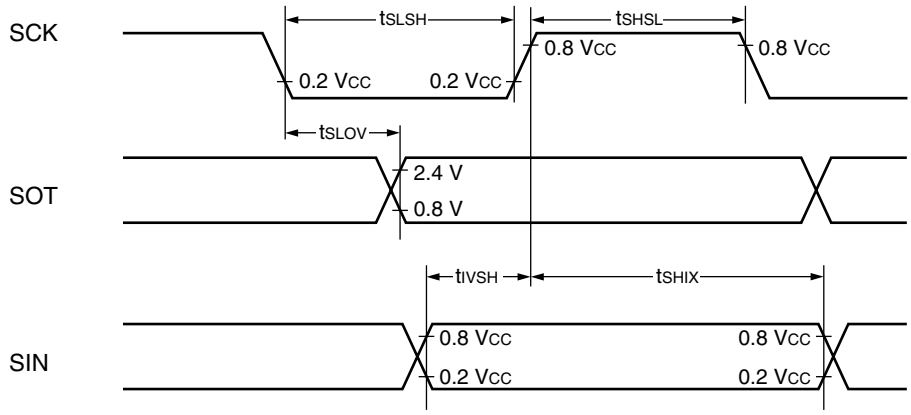
Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock mode output pin is : C_L = 80 pF + 1TTL	8 t_{CP}	—	ns
SCK↓→SOT delay time	t_{SLOV}	SCKx, SOTx		– 80	+ 80	ns
Valid SIN→SCK↑	t_{IVSH}	SCKx, SINx		100	—	ns
SCK↑→valid SIN hold time	t_{SHIX}	SCKx, SINx		60	—	ns
Serial clock H pulse width	t_{SHSL}	SCKx, SINx	External shift clock mode output pin is : C_L = 80 pF + 1TTL	4 t_{CP}	—	ns
Serial clock L pulse width	t_{SLSH}	SCKx, SINx		4 t_{CP}	—	ns
SCK↓→SOT delay time	t_{SLOV}	SCKx, SOTx		—	150	ns
Valid SIN→SCK↑	t_{IVSH}	SCKx, SINx		60	—	ns
SCK↑→valid SIN hold time	t_{SHIX}	SCKx, SINx		60	—	ns

Notes : • Above rating is the case of CLK synchronous mode.
• C_L is a load capacitance value on pins for testing.
• t_{CP} : Refer to " (1) Clock input timing".

• Internal shift clock mode



• External shift clock mode



(6) I²C timing

(V_{CC} = AV_{CC} = 3.3 V ± 0.3 V, V_{SS} = AV_{SS} = 0.0 V, T_A = – 40 °C to + 85 °C)

Parameter	Symbol	Conditions	Value		Unit
			Min	Max	
SCL clock frequency	f_{SCL}	Power-supply voltage of external pull-up resistor at 5.0 V. R = 1.2 kΩ, C = 50 pF*2 Power-supply voltage of external pull-up resistor at 3.6 V. R = 1.0 kΩ, C = 50 pF*2	0	100	kHz
(Repeat) [start] condition hold time SDA ↓ → SCL ↓	t_{HDSTA}		4.0	—	µs
SCL clock "L" width	t_{LOW}		4.7	—	µs
SCL clock "H" width	t_{HIGH}		4.0	—	µs
Repeat [start] condition setup time SCL ↑ → SDA ↓	t_{SUSTA}		4.7	—	µs
Data hold time SCL ↓ → SDA ↓ ↑	t_{HDDAT}		0	3.45*3	µs
Data setup time SDA ↓ ↑ → SCL ↑	t_{SUDAT}	Power-supply voltage of external pull-up resistor at 5.0 V. f_{CP}*1 ≤ 20 MHz, R = 1.2 kΩ, C = 50 pF*2 Power-supply voltage of external pull-up resistor at 3.6 V. f_{CP}*1 ≤ 20 MHz, R = 1.0 kΩ, C = 50 pF*2	250*4	—	ns
		Power-supply voltage of external pull-up resistor at 5.0 V. f_{CP}*1 > 20 MHz, R = 1.2 kΩ, C = 50 pF*2 Power-supply voltage of external pull-up resistor at 3.6 V. f_{CP}*1 > 20 MHz, R = 1.0 kΩ, C = 50 pF*2	200*4	—	
[Stop] condition setup time SCL ↑ → SDA ↑	t_{SUSTO}	Power-supply voltage of external pull-up resistor at 5.0 V. R = 1.2 kΩ, C = 50 pF*2 Power-supply voltage of external pull-up resistor at 3.6 V. R = 1.0 kΩ, C = 50 pF*2	4.0	—	µs
Bus free time between [stop] condition and [start] condition	t_{BUS}		4.7	—	µs

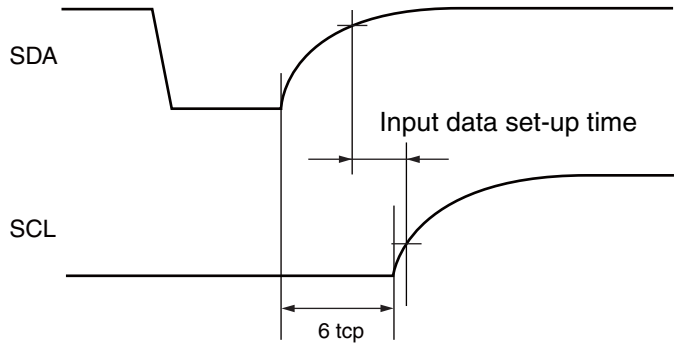
*1 : f_{CP} is internal operating clock frequency. Refer to " (1) Clock input timing".

*2 : R and C are pull-up resistance of SCL and SDA lines and load capacitance.

*3 : The maximum t_{HDDAT} only has to be met if the device does not stretch the "L" width (t_{LOW}) of the SCL signal.

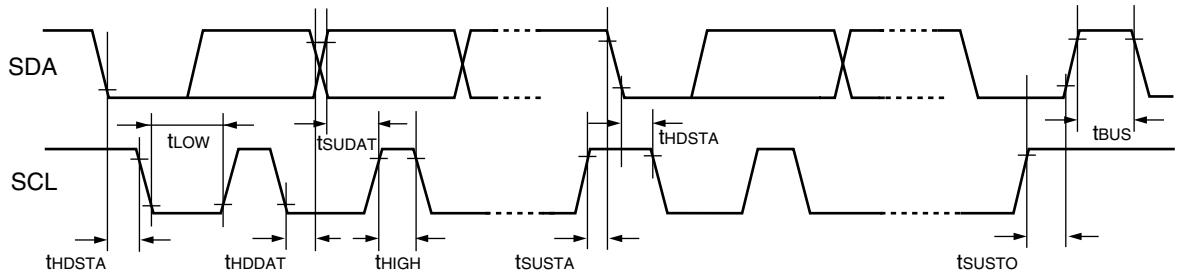
*4 : Refer to "• Note of SDA, SCL set-up time".

• Note of SDA, SCL set-up time



Note : The rating of the input data set-up time in the device connected to the bus cannot be satisfied depending on the load capacitance or pull-up resistor. Be sure to adjust the pull-up resistor of SDA and SCL if the rating of the input data set-up time cannot be satisfied.

•Timing definition

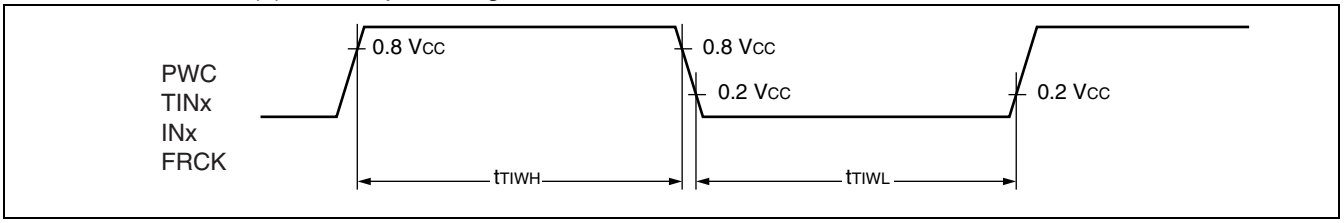


(7) Timer input timing

(V_{CC} = AV_{CC} = 3.3 V ± 0.3 V, V_{SS} = AV_{SS} = 0.0 V, T_A = – 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Input pulse width	t_{TIWH} t_{TIWL}	FRCK, INx, TINx, PWC	—	4 t_{CP}	—	ns

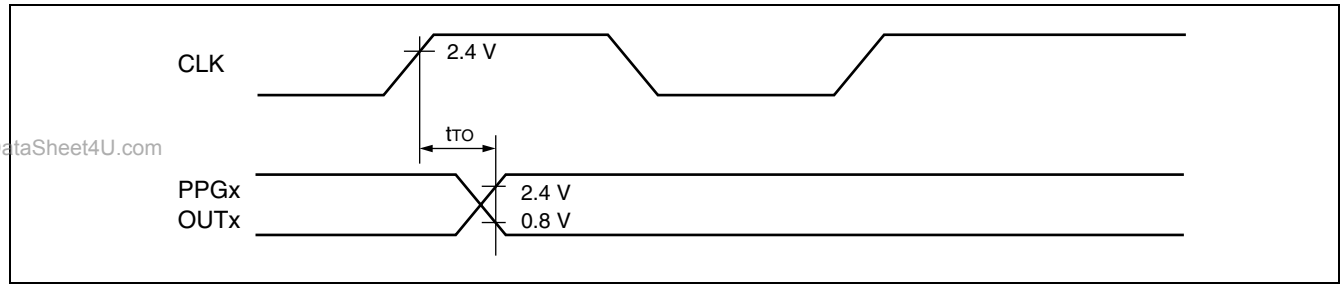
Note : t_{CP} : Refer to " (1) Clock input timing".



(8) Timer output timing

(V_{CC} = AV_{CC} = 3.3 V ± 0.3 V, V_{SS} = AV_{SS} = 0.0 V, T_A = – 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
CLK↑→T_{OUT} change time PPG0 to PPG5 change time OUT0 to OUT3 change time	t_{TO}	TOTx, PPGx, OUTx	—	30	—	ns

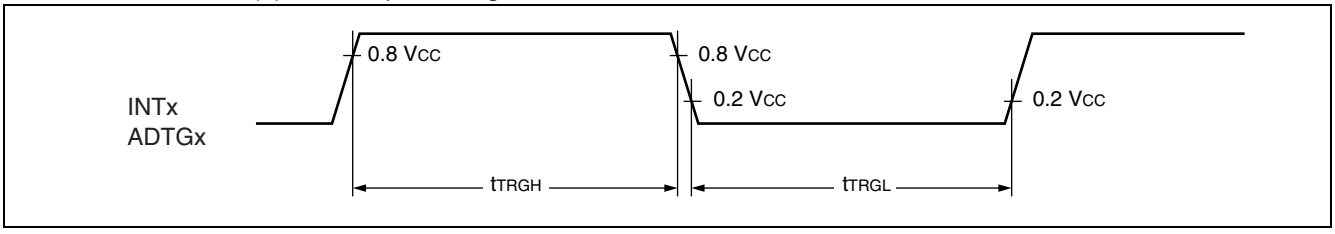


(9) Trigger input timing

(V_{CC} = AV_{CC} = 3.3 V ± 0.3 V, V_{SS} = AV_{SS} = 0.0 V, T_A = – 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH} t_{TRGL}	INTx, ADTG	—	5 t_{CP}	—	ns	At normal operating
				1	—	µs	In Stop mode

Note : t_{CP} : Refer to " (1) Clock input timing".

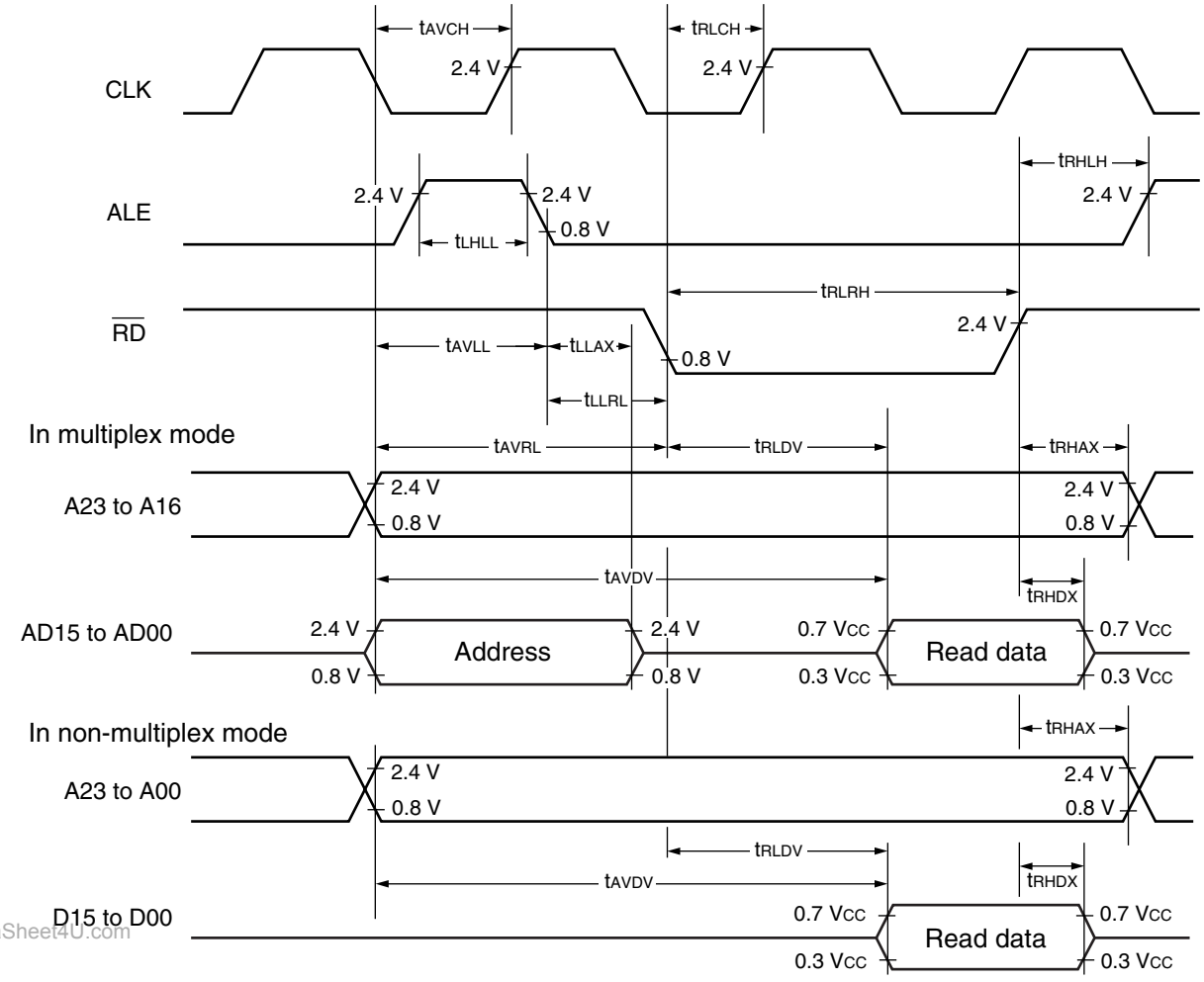


(10) Bus read timing

(V_{CC} = AV_{CC} = 3.3 V ± 0.3 V, V_{SS} = AV_{SS} = 0.0 V, T_A = 0 °C to + 70 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
ALE pulse width	t_{LHLL}	ALE	—	$t_{CP}/2 - 15$	—	ns	At f_{cp} = 24 MHz
				$t_{CP}/2 - 20$	—	ns	At f_{cp} = 12 MHz
				$t_{CP}/2 - 35$	—	ns	At f_{cp} = 6 MHz
Valid address→ALE↓time	t_{AVLL}	Address, ALE	—	$t_{CP}/2 - 17$	—	ns	
				$t_{CP}/2 - 40$	—	ns	At f_{cp} = 6 MHz
ALE↓→Address valid time	t_{LLAX}	ALE, Address	—	$t_{CP}/2 - 15$	—	ns	
Valid address→$\overline{RD}$↓time	t_{AVRL}	$\overline{RD}$, Address	—	$t_{CP} - 25$	—	ns	
Valid address→valid data input	t_{AVDV}	Address/ data	—	—	$5\ t_{CP}/2 - 55$	ns	
				—	$5\ t_{CP}/2 - 80$	ns	At f_{cp} = 6 MHz
$\overline{RD}$ pulse width	t_{RLRH}	$\overline{RD}$	—	$3\ t_{CP}/2 - 25$	—	ns	At f_{cp} = 24 MHz
				$3\ t_{CP}/2 - 20$	—	ns	At f_{cp} = 12 MHz
$\overline{RD}$↓→valid data input	t_{RLDV}	$\overline{RD}$, Data	—	—	$3\ t_{CP}/2 - 55$	ns	
				—	$3\ t_{CP}/2 - 80$	ns	At f_{cp} = 6 MHz
$\overline{RD}$↓→data hold time	t_{RHDX}	$\overline{RD}$, Data	—	0	—	ns	
$\overline{RD}$↑→ALE↑time	t_{RHLH}	$\overline{RD}$, ALE	—	$t_{CP}/2 - 15$	—	ns	
$\overline{RD}$↑→address valid time	t_{RHAX}	Address, $\overline{RD}$	—	$t_{CP}/2 - 10$	—	ns	
Valid address→CLK↑time	t_{AVCH}	Address, CLK	—	$t_{CP}/2 - 17$	—	ns	
$\overline{RD}$↓→CLK↑time	t_{RLCH}	$\overline{RD}$, CLK	—	$t_{CP}/2 - 17$	—	ns	
ALE↓→$\overline{RD}$↓time	t_{LLRL}	$\overline{RD}$, ALE	—	$t_{CP}/2 - 15$	—	ns	

Note : t_{CP} : Refer to " (1) Clock input timing".

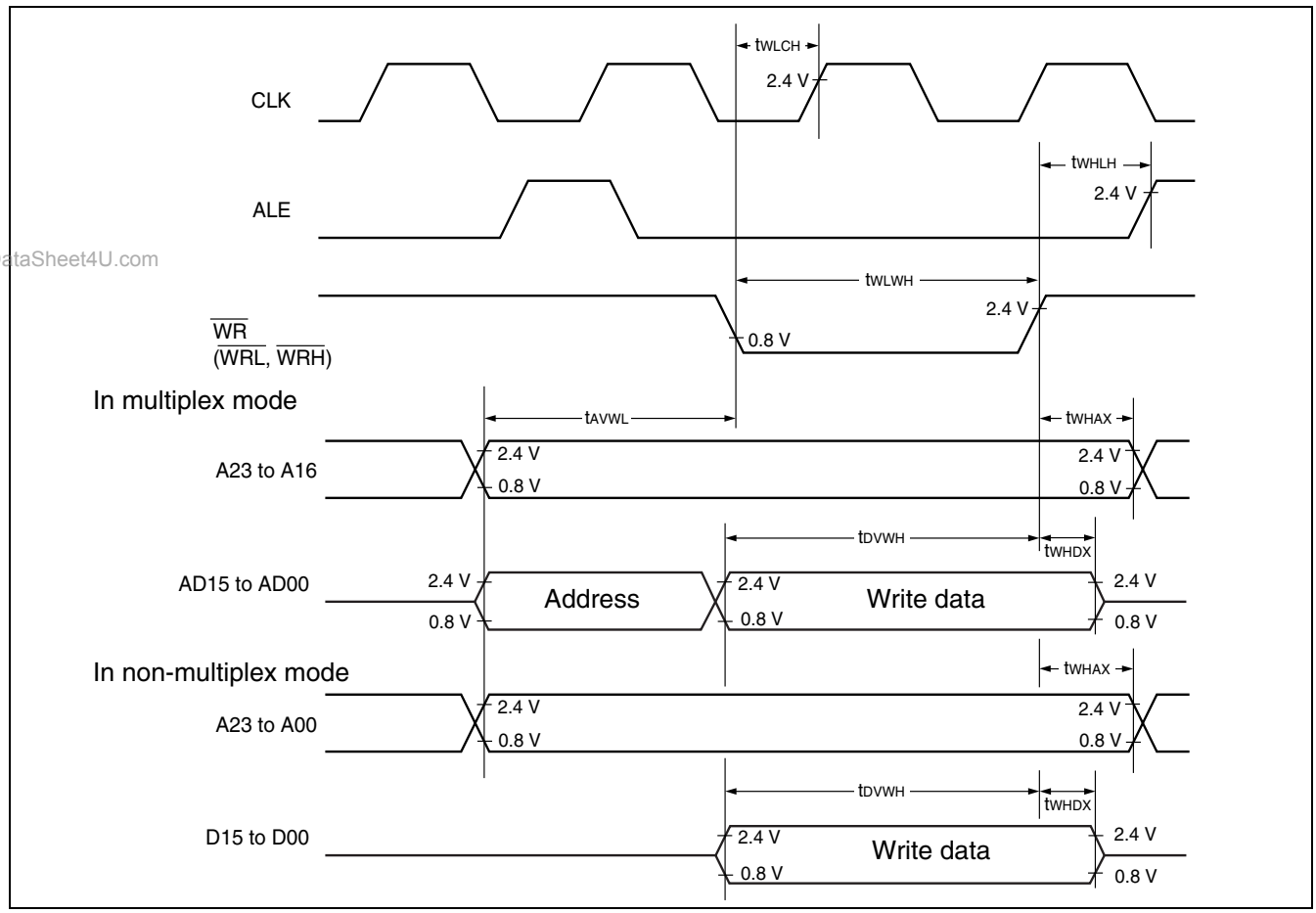


(11) Bus write timing

(V_{CC} = AV_{CC} = 3.3 V ± 0.3 V, V_{SS} = AV_{SS} = 0.0 V, T_A = 0 °C to + 70 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Valid address→$\overline{WR}$↓ time	t_{AVWL}	Address, $\overline{WR}$	—	t_{CP} – 15	—	ns	
$\overline{WR}$ pulse width	t_{WLWH}	$\overline{WRL}$, $\overline{WRH}$	—	3 t_{CP}/2 – 25	—	ns	At f_{cp} = 24 MHz
			—	3 t_{CP}/2 – 20	—	ns	At f_{cp} = 12 MHz
Valid data output→$\overline{WR}$↑ time	t_{DVWH}	Data, $\overline{WR}$	—	3 t_{CP}/2 – 15	—	ns	
$\overline{WR}$↑→data hold time	t_{WHDX}	$\overline{WR}$, Data	—	10	—	ns	At f_{cp} = 24 MHz
			—	20	—	ns	At f_{cp} = 12 MHz
			—	30	—	ns	At f_{cp} = 6 MHz
$\overline{WR}$↑→address valid time	t_{WHAX}	$\overline{WR}$, Address	—	t_{CP}/2 – 10	—	ns	
$\overline{WR}$↑→ALE↑time	t_{WHLH}	$\overline{WR}$, ALE	—	t_{CP}/2 – 15	—	ns	
$\overline{WR}$↓→CLK↑time	t_{WLCH}	$\overline{WR}$, CLK	—	t_{CP}/2 – 17	—	ns	

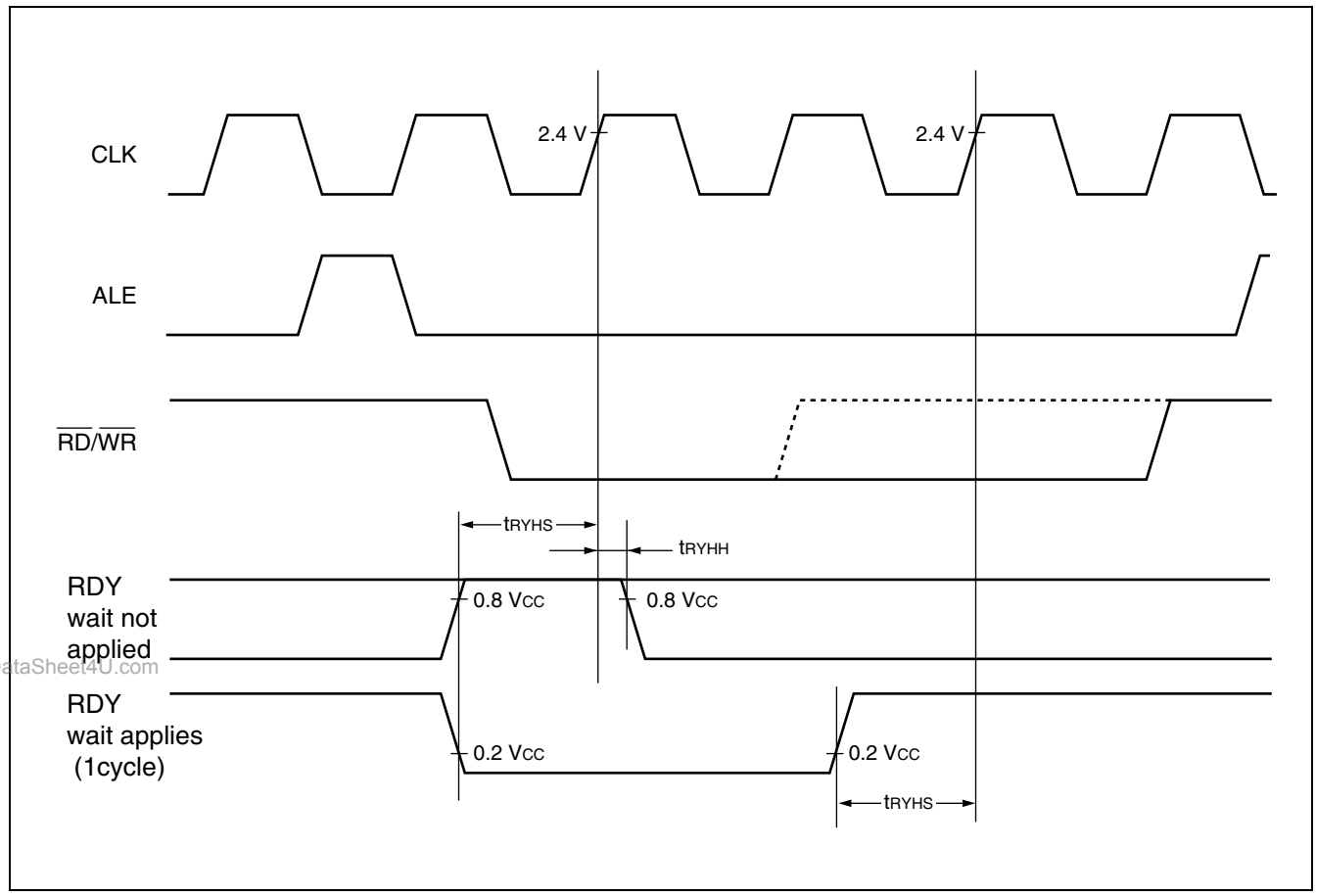
Note : t_{CP} : Refer to " (1) Clock input timing".



(12) Ready input timing

(V_{CC} = AV_{CC} = 3.3 V ± 0.3 V, V_{SS} = AV_{SS} = 0.0 V, T_A = 0 °C to + 70 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
RDY set-up time	t_{RYHS}	RDY	—	35	—	ns	
			—	70	—	ns	f_{cp} = 6 MHz
RDY hold time	t_{RYHH}		—	0	—	ns	

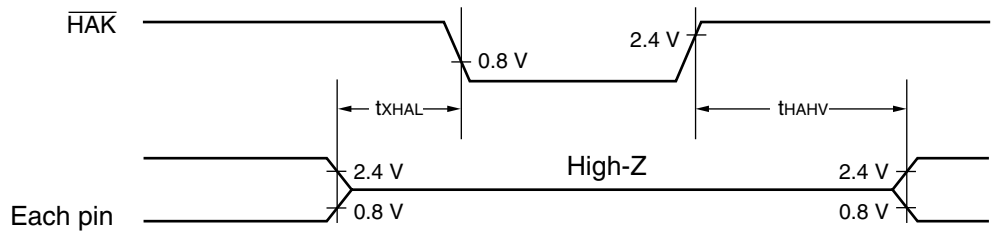


(13) Hold timing

(V_{CC} = AV_{CC} = 3.3 V ± 0.3 V, V_{SS} = AV_{SS} = 0.0 V, T_A = 0 °C to + 70 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Pin floating → $\overline{HAK}$ ↓ time	t_{XHAL}	$\overline{HAK}$	—	30	t_{CP}	ns
$\overline{HAK}$ ↓ → pin valid time	t_{HAHV}	$\overline{HAK}$		t_{CP}	2 t_{CP}	ns

Notes : • It takes one cycle or more for $\overline{HAK}$ to change after the HRQ pin is captured.
• t_{CP} : Refer to " (1) Clock input timing".



5. Electrical Characteristics for the A/D Converter

(V_{CC} = AV_{CC} = 3.3 V ± 0.3 V, V_{SS} = AV_{SS} = 0.0 V, T_A = – 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	10	bit	
Total error	—	—	—	—	± 3.0	LSB	
Nonlinear error	—	—	—	—	± 2.5	LSB	
Differential linear error	—	—	—	—	± 1.9	LSB	
Zero transition voltage	V_{OT}	AN0 to AN15	AV_{SS} – 1.5 LSB	AV_{SS} + 0.5 LSB	AV_{SS} + 2.5 LSB	V	1 LSB = (AVRH – AV_{SS})/1024
Full-scale transition voltage	V_{FST}	AN0 to AN15	AVRH – 3.5 LSB	AVRH – 1.5 LSB	AVRH + 0.5 LSB	V	
Conversion time	—	—	—	176 t_{CP}*1	—	ns	
Sampling time	—	—	—	64 t_{CP}*1	—	ns	
Analog port input current	I_{AIN}	AN0 to AN15	—	—	10	µA	
Analog input voltage	V_{AIN}	AN0 to AN15	0	—	AVRH	V	
Reference voltage	—	AVRH	2.7	—	AV_{CC}	V	
Power supply current	I_A	AV_{CC}	—	1.4	3.5	mA	
	I_{AH}	AV_{CC}	—	—	5	µA	*2
Reference voltage supplying current	I_R	AVRH	—	95	170	µA	
	I_{RH}	AVRH	—	—	5	µA	*2
Interchannel disparity	—	AN0 to AN15	—	—	4	LSB	

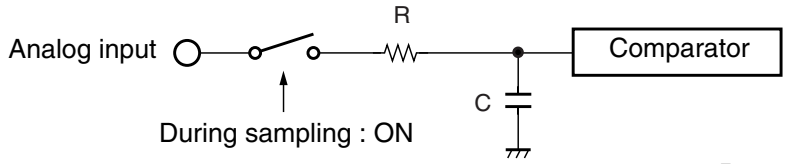
*1 : t_{CP} : Refer to " 4. AC Characteristics (1) Clock input timing".

*2 : The current when the CPU is in stop mode and the A/D converter is not operating (For V_{CC} = AV_{CC} = AVRH = 3.3 V).

Notes :

- **About the external impedance of the analog input and its sampling time**
  - A/D converter with sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting A/D conversion precision.

- Analog input circuit model



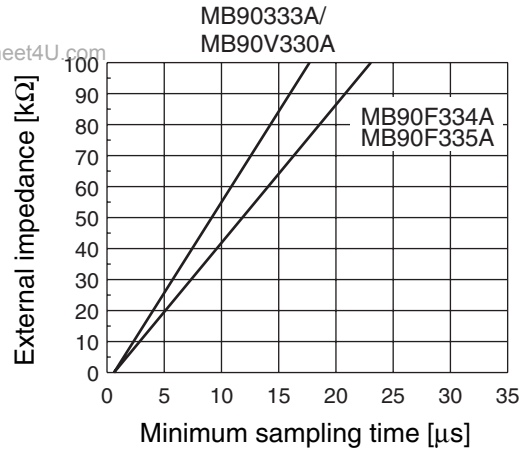
	R	C
MB90333A	1.9 kΩ (Max)	32.3 pF (Max)
MB90F334A	1.9 kΩ (Max)	25.0 pF (Max)
MB90F335A	1.9 kΩ (Max)	25.0 pF (Max)
MB90V330A	1.9 kΩ (Max)	32.3 pF (Max)

Note : The values are reference values.

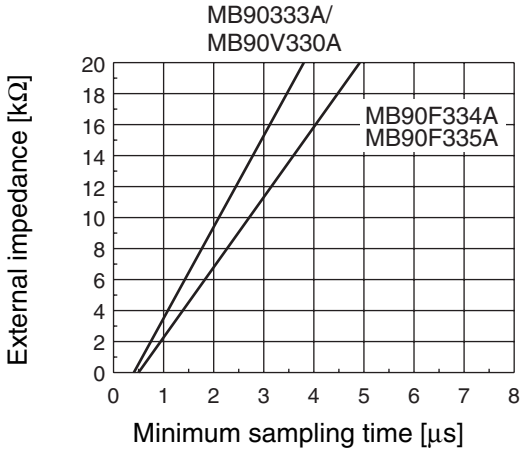
- To satisfy the A/D conversion precision standard, consider the relationship between the external impedance and minimum sampling time and either adjust the resistor value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value.

- The relationship between the external impedance and minimum sampling time

(External impedance = 0 kΩ to 100 kΩ)



(External impedance = 0 kΩ to 20 kΩ)



- If the sampling time cannot be sufficient, connect a capacitor of about 0.1 µF to the analog input pin.

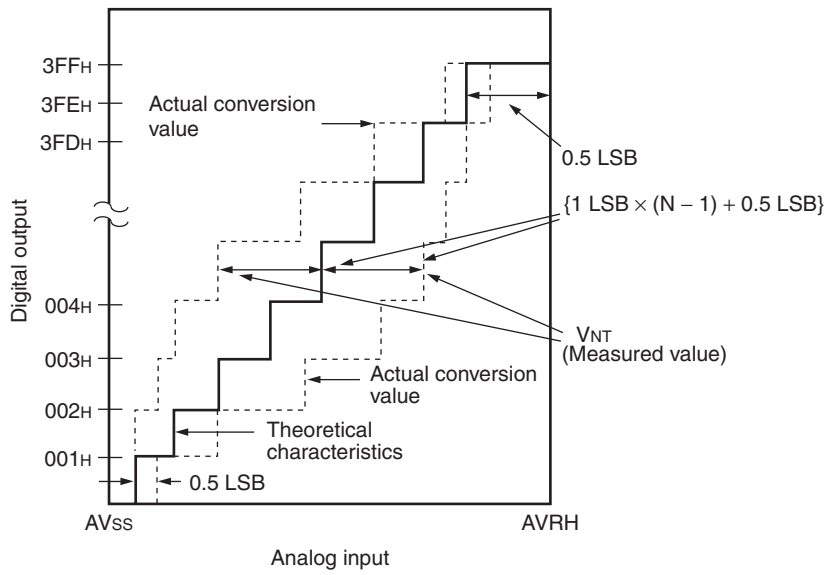
- **About errors**

As |AVRH| becomes smaller, values of relative errors grow larger.

A/D Converter Glossary

Resolution :	Analog changes that are identifiable with the A/D converter.
Linearity error :	The deviation of the straight line connecting the zero transition point (“00 0000 0000” ↔ “00 0000 0001”) with the full-scale transition point (“11 1111 1110” ↔ “11 1111 1111”) from actual conversion characteristics.
Differential linearity error :	The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value.
Total error :	The total error is defined as a difference between the actual value and the theoretical value, which includes zero-transition error/full-scale transition error and linearity error.

Total error



$$\text{Total error for digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$1\ \text{LSB (Theoretical value)} = \frac{AVRH - AVss}{1024}\ [V]$$

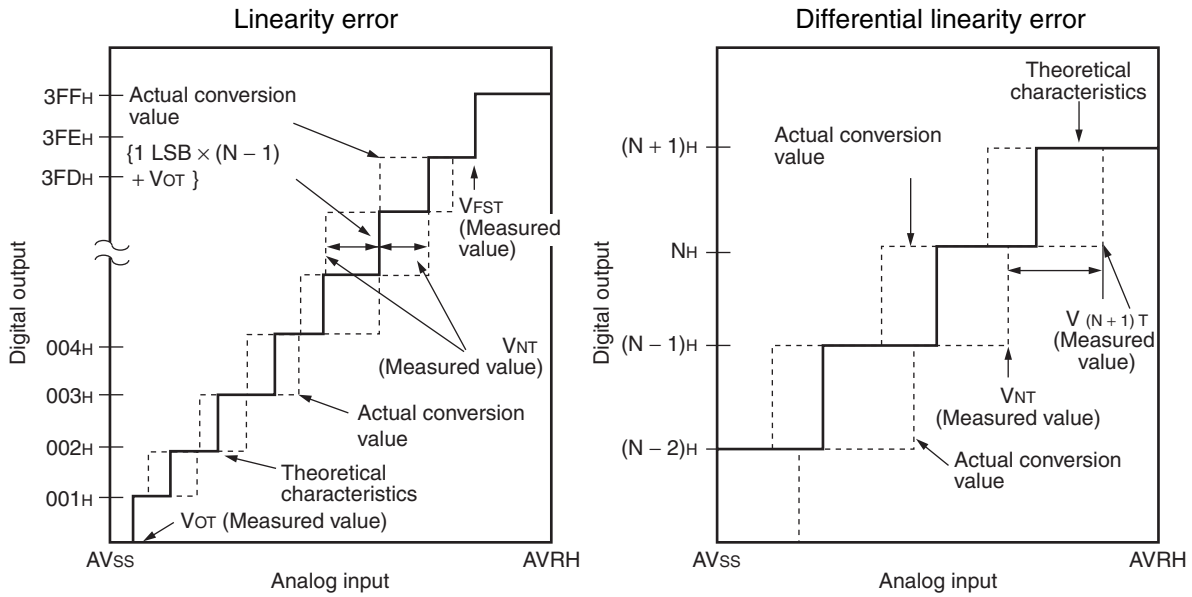
V_{OT} (Theoretical value) = AVss + 0.5 LSB [V]

V_{FST} (Theoretical value) = AVRH – 1.5 LSB [V]

V_{NT} : Voltage at a transition of digital output from (N - 1) H to N_H

(Continued)

(Continued)



$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + V_{OT}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$\text{Differential linearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\ [\text{LSB}]$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ [\text{V}]$$

V_{OT} : Voltage at transition of digital output from "000_H" to "001_H"
V_{FST} : Voltage at transition of digital output from "$3FE_H$" to "$3FF_H$"

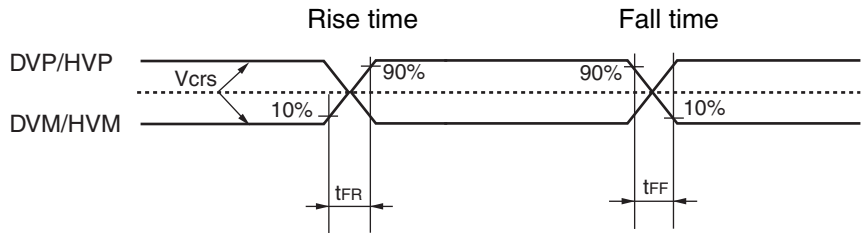
6. USB characteristics

(V_{CC} = AV_{CC} = 3.3 V ± 0.3 V, V_{SS} = AV_{SS} = 0.0 V, T_A = 0 °C to + 70 °C)

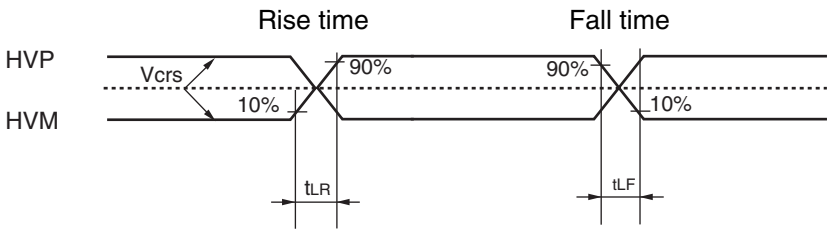
Parameter		Symbol	Value		Unit	Remarks
			Min	Max		
Input characteristics	Input High level voltage	V_{IH}	2.0	—	V	
	Input Low level voltage	V_{IL}	—	0.8	V	
	Differential input sensitivity	V_{DI}	0.2	—	V	
	Differential common mode range	V_{CM}	0.8	2.5	V	
Output characteristics	Output High level voltage	V_{OH}	2.8	3.6	V	I_{OH} = – 200 µA
	Output Low level voltage	V_{OL}	0.0	0.3	V	I_{OL} = 2 mA
	Cross over voltage	V_{CRS}	1.3	2.0	V	
	Rise time	t_{FR}	4	20	ns	Full Speed
		t_{LR}	75	300	ns	Low Speed
	Fall time	t_{FF}	4	20	ns	Full Speed
		t_{LF}	75	300	ns	Low Speed
	Rising/falling time matching	t_{RFM}	90	111.11	%	(T_{FR}/T_{FF})
		t_{RLM}	80	125	%	(T_{LR}/T_{LF})
	Output impedance	Z_{DRV}	28	44	Ω	Including Rs = 27 Ω
Series resistance		R_S	25	30	Ω	Recommended value = 27 Ω at using USB*

* : Arrange the series resistance R_S values in order to set the impedance value within the output impedance ZSRV.

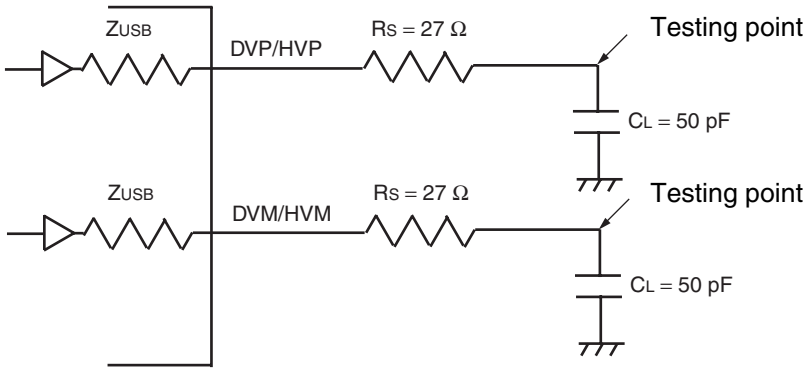
• Data signal timing (Full Speed)



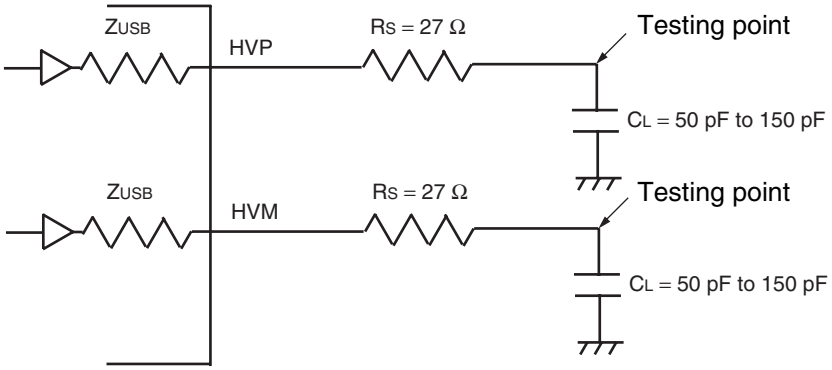
• Data signal timing (Low Speed)



• Load condition (Full Speed)



• Load condition (Low Speed)



7. Flash memory write/erase characteristics

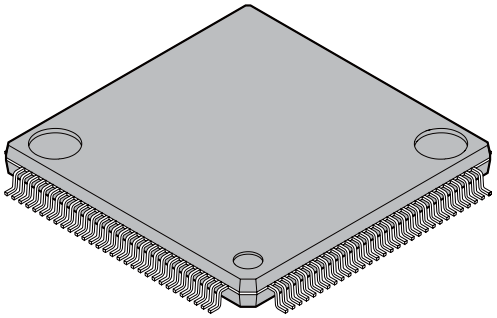
Parameter	Condition	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	T_A = + 25 °C V_{CC} = 3.0 V	—	1	15	s	Excludes 00H programming prior to erasure.
Chip erase time		—	9	—	s	*:MB90F334A (384 Kbytes) Excludes 00H programming prior to erasure.
		—	14	—		*:MB90F335A (512 Kbytes) Excludes 00H programming prior to erasure.
Word (16-bit width) programming time		—	16	3600	µs	Except for over head time of system level
Programming/erase cycle	—	10000	—	—	cycle	
Flash memory data retaining period	Average T_A = + 85 °C	20	—	—	year	*

* : This value comes from the technology qualification. (using Arrhenius equation to translate high temperature measurements into normalized value at + 85 °C)

■ ORDERING INFORMATION

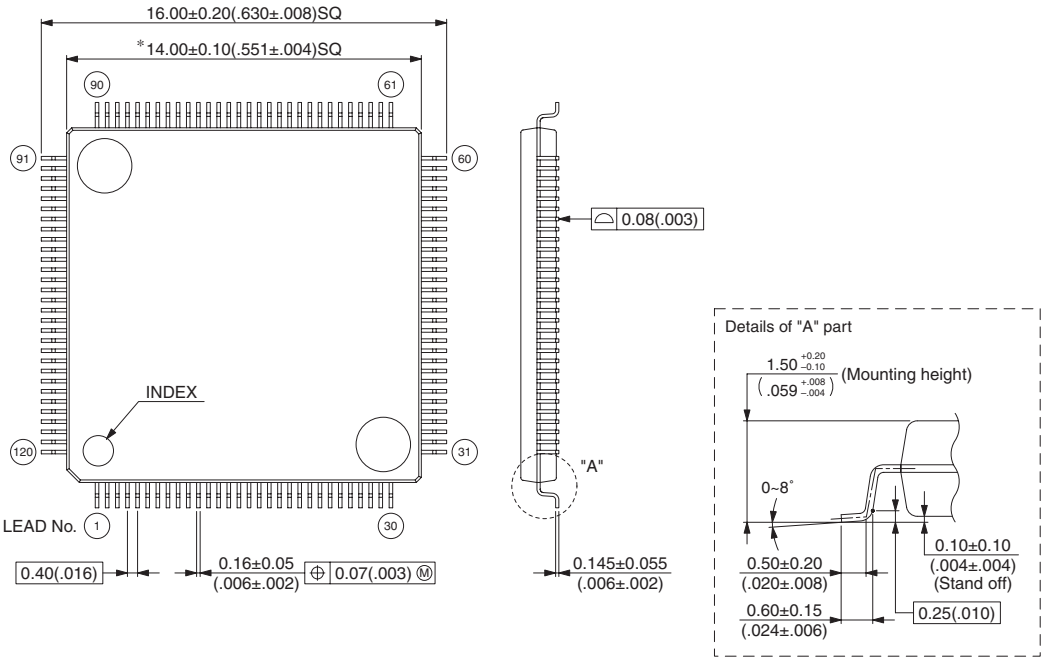
Part number	Package	Remarks
MB90F334APMC1 MB90F335APMC1 MB90333APMC1	120-pin plastic LQFP (FPT-120P-M24)	
MB90F334APMC MB90F335APMC MB90333APMC	120-pin plastic LQFP (FPT-120P-M21)	
MB90V330A	299-pin ceramic PGA (PGA-299C-A01)	For evaluation

■ PACKAGE DIMENSIONS

120-pin plastic LQFP		
	Lead pitch	0.40 mm
	Package width × package length	14.0 mm × 14.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Code (Reference)	P-LFQFP120-14×14-0.40
(FPT-120P-M24)		

120-pin plastic LQFP
(FPT-120P-M24)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.

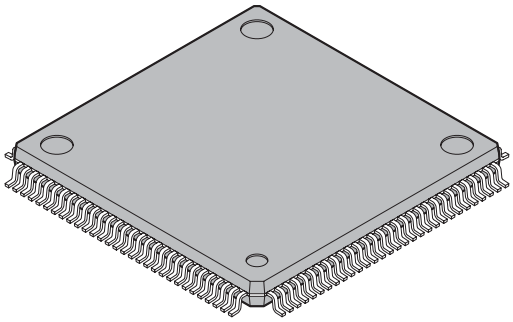


Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please confirm the latest Package dimension by following URL.
http://edevice.fujitsu.com/package/en-search/

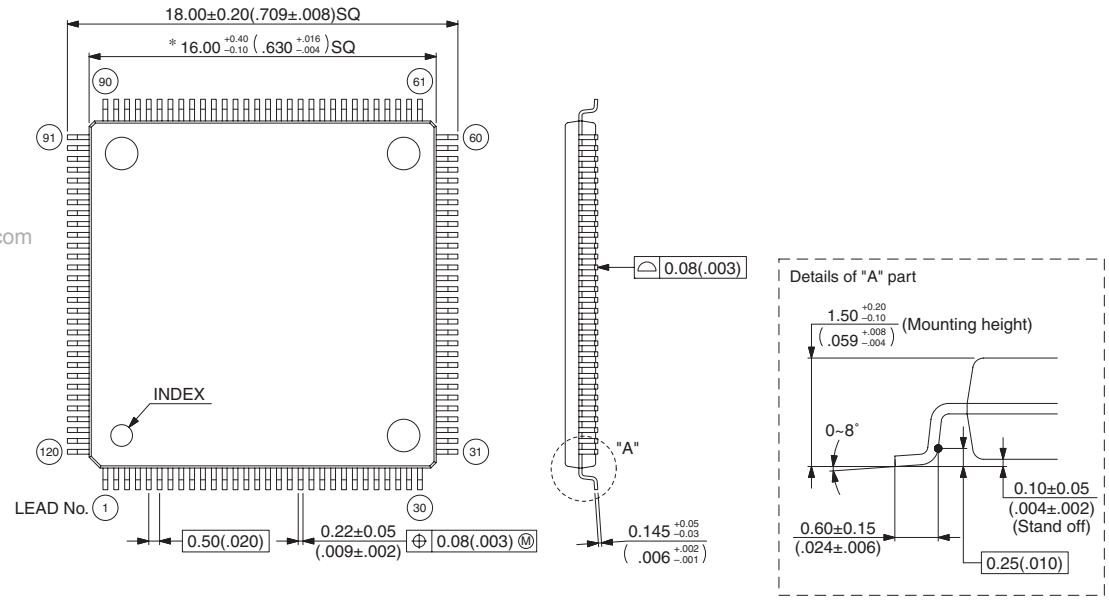
(Continued)

(Continued)

120-pin plastic LQFP		
	Lead pitch	0.50 mm
	Package width × package length	16.0 × 16.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.88 g
(FPT-120P-M21)	Code (Reference)	P-LFQFP120-16×16-0.50

120-pin plastic LQFP
(FPT-120P-M21)

Note 1) * : These dimensions do not include resin protrusion.
Resin protrusion is +0.25(.010) MAX(each side).
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please confirm the latest Package dimension by following URL.
http://edevice.fujitsu.com/package/en-search/

■ MAIN CHANGES IN THIS EDITION

Page	Section	Change Results
5	■ PACKAGES AND PRODUCT MODELS	Changed the status; Under development -> ○
20	■ MEMORY MAP	Changed the note.
86	■ PERIPHERAL RESOURCES 22. 3 Mbits flash memory • Register list	For LPM1 and LPM0, changed to Reserved, and changed R/W to W.
88	23. 4 Mbits flash memory • Register list	
117	■ ORDERING INFORMATION	Added the part number; MB90F335APMC1

The vertical lines marked in the left side of the page show the changes.

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