FUJITSU SEMICONDUCTOR
ADVANCE INFORMATION

XXXX-XXXXX-XE

16-bit Proprietary Microcontroller

CMOS

F²MC-16LX MB90350 Series

MB90F352/C(S), MB90V340(S)

■ DESCRIPTION

The MB90350-series with one FULL-CAN interface (MB90V340: 2ch) and FLASH ROM is especially designed for automotive and industrial applications. Its main feature is the on board CAN Interface, which conforms to V2.0 Part A and Part B, while supporting a very flexible message buffer scheme and so offering more functions than a normal full CAN approach. With the new 0.35 µm CMOS technology, Fujitsu now offers on-chip FLASH-ROM program memory up to 128 Kbytes. An internal voltage booster removes the necessity for a second programming voltage.

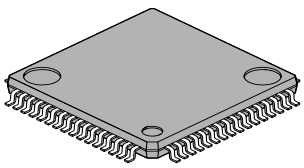
An on board voltage regulator provides 3 V to the internal MCU core. This creates a major advantage in terms of EMI and power consumption.

The internal PLL clock frequency multiplier provides an internal 42 ns instruction cycle time from an external 4 MHz clock.

The unit features an 4 channel Output Compare Unit and 6 channel Input Capture Unit with two separate 16-bit free running timers. 2 UARTs (MB90V340: 3 UARTs) constitute additional functionality for communication purposes.

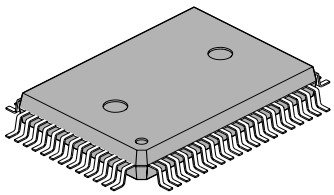
■ PACKAGES

64-pin Plastic LQFP



(FPT-64P-M09)

64-pin Plastic QFP



(FPT-64P-M06)

FUJITSU

■ FEATURES

- 16-bit core CPU; 4 MHz external clock (24 MHz internal, 42 ns instr. cycle time)
- New 0.35 µm CMOS Process Technology
- Internal voltage regulator supports 3 V MCU core, offering low EMI and low power consumption figures
- One FULL-CAN interface (MB90V340: 2ch); conforming to Version 2.0 Part A and Part B, flexible message buffering (mailbox and FIFO buffering can be mixed)
- Powerful interrupt functions (8 progr. priority levels; 8 external interrupts)
- EI2OS - Automatic transfer function indep.of CPU; 16 ch. of intelligent I/O Services
- DMA
- 18-bit Time-base counter
- Watchdog Timer
- 2 full duplex UARTs (SCI/LIN) (MB90V340: 3 UARTs)
- One ch I^2C with 400 kbit/s (devices with C-suffix)
- A/D Converter : 15 ch. analog inputs (Resolution 10 bits or 8 bit, conversion time 3µs)
- 16-bit reload timer ×4 ch
- ICU (Input capture) 16 bit x6 ch
- OCU (Output compare) 16 bit ×4 ch
- 16-bit free running timer ×2 ch (FRT0 : ICU 0/1, FRT1 : ICU 4/5/6/7, OCU 4/5/6/7)
- 8/16-bit Programmable Pulse Generator 6ch×16-bit / 10ch×8-bit (MB90V340: 8ch×16bit / 12ch×8bit)
- Optimized instruction set for controller applications (bit, byte, word and long-word data types; 23 different addressing modes; barrel shift; variety of pointers)
- 4-byte instruction execution queue
- signed multiply (16 bit×16 bit) and divide (32 bit/16 bit) instructions available
- Program Patch Function
- Fast Interrupt processing
- Low Power Consumption - 10 different power saving modes : (Sleep, Stop, CPU intermittent mode, ...)
- 32 kHz Subsytem Clock (devices without S-suffix)
- External bus interface
- Programmable input levels (Automotive / CMOS-Schmitt (initial level is Automotive), for external bus also TTL level)
- Packages : 64-pin plastic QFP, 64-pin plastic LQFP

Controller Area Network (CAN) - License of Robert Bosch GmbH

■ PRODUCT LINEUP

Part Number / Parameter	MB90F352/C(S)	MB90V340(S)
CPU	F^2MC-16LX CPU	
System clock	On-chip PLL clock multiplier (×1, ×2, ×3, ×4, x6, x8 ,1/2 when PLL stops) Minimum instruction execution time : 42 ns (4 MHz osc. PLL ×6)	
ROM	Boot-block, Flash memory 128 Kbytes	External
RAM	4 Kbytes	30 Kbytes
Emulator-specific power supply*1	—	None
Technology	0.35 µm CMOS with on-chip voltage regulator for internal power supply + Flash memory with On-chip charge pump for programming voltage	0.35 µm CMOS with on-chip voltage regulator for internal power supply
Operating voltage range	3.5 - 5.5 V (4.5 - 5.5 V if A/D Converter is used)	5 V ± 10%
Temperature range	–40 °C to 105 °C	—
Package	QFP-64, LQFP-64	PGA-299
UART	2 channels	3 channels
	Wide range of baud rate settings using a dedicated reload timer Special synchronous options for adapting to different synchronous serial protocols LIN functionality working either as master or slave LIN device	
I^2C (400 kbit/s)	devices with 'C'-suffix: 1 channel devices without 'C'-suffix: —	2 channels
A/D Converter	15 channels	15 channels
	10-bit or 8-bit resolution Conversion time : Min 3 µs include sample time (per one channel)	
16-bit Reload Timer (4 channels)	Operation clock frequency : fsys/2^1, fsys/2^3, fsys/2^5 (fsys = System clock frequency) Supports External Event Count function for 2 channels (Ch.1 and Ch.3)	
16-bit I/O Timer (2 channels)	Signals an interrupt when overflowing Operation clock freq. : fsys, fsys/2^1, fsys/2^2, fsys/2^3, fsys/2^4, fsys/2^5, fsys/2^6, fsys/2^7 (fsys = System clock freq.) I/O Timer 0 (clock input FRCK0) corresponds to ICU 0/1 I/O Timer 1 (clock input FRCK1) corresponds to ICU 4/5/6/7, OCU 4/5/6/7	
	Both I/O Timers support Timer Clear when a match with Output Compare (Channel 4)	I/O Timer 1 supports Timer Clear when a match with Output Compare (Channel 4)
16-bit Output Compare (4 channels)	Signals an interrupt when a match with 16-bit I/O Timer. 16-bit compare registers. Four compare registers can be used to generate three PWM output signals.	
16-bit Input Capture (6 channels)	Rising edge, falling edge or rising & falling edge sensitive Signals an interrupt upon external event	

(Continued)

Part Number / Parameter	MB90F352/C(S)	MB90V340(S)
8/16-bit Programmable Pulse Generator	10 ch (8 bit) / 6 ch (16 bit) 12 8-bit reload counters	12 ch (8 bit) / 8 ch (16 bit) 16 8-bit reload counters
	Supports 8-bit and 16-bit operation modes A pair of 8-bit reload counters can be configured as one 16-bit reload counter or as 8-bit prescaler plus 8-bit reload counter Operation clock freq. : fsys, fsys/2^1, fsys/2^2, fsys/2^3, fsys/2^4 or 102.4 µs@fosc = 5 MHz (fsys = System clock frequency, fosc = Oscillation clock frequency)	
CAN Interface	1 channel	2 channels
	Conforms to CAN Specification Version 2.0 Part A and B Automatic re-transmission in case of error Automatic transmission responding to Remote Frame Prioritized 16 message buffers for data and ID's Supports multiple messages Flexible configuration of acceptance filtering : Full bit compare/Full bit mask/Two partial bit masks Supports up to 1 Mbps	
External Interrupt (8 channels)	Can be programmed edge sensitive or level sensitive	
32 kHz Subclock for low power operation	devices without 'S'-suffix: yes devices with 'S'-suffix: —	
I/O Ports	Virtually all external pins can be used as general purpose I/O All push-pull outputs Bit-wise programmable as input/output or peripheral signal Programmable in groups of 8 as CMOS schmitt trigger/ automotive inputs (default) TTL input level programmable for external bus (default for external reset vector fetch)	
Flash Memory	Supports automatic programming, Embedded Algorithm™*2 Write/Erase/Erase-Suspend/Resume commands A flag indicating completion of the algorithm Number of erase cycles : 10,000 times Data retention time : 10 years Boot block configuration Erase can be performed on each block Block protection with external programming voltage	—

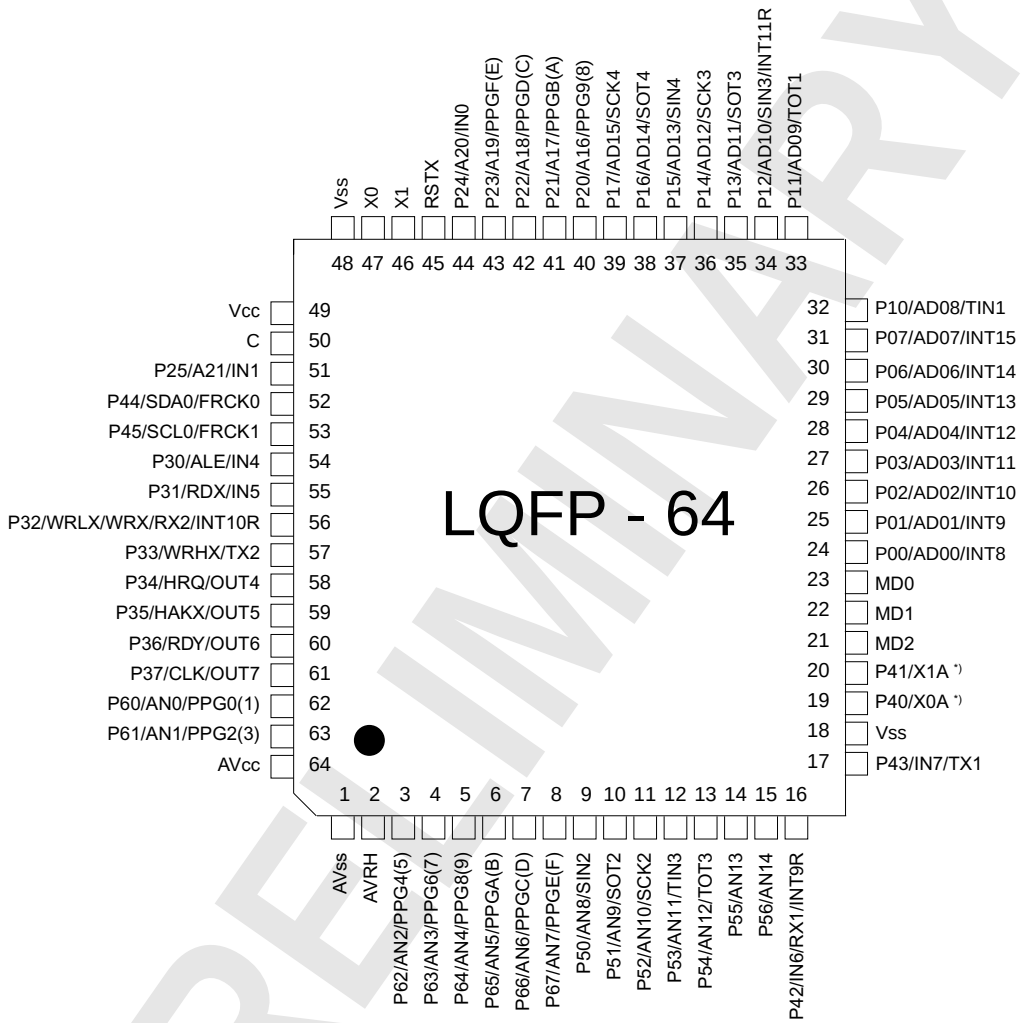
*1 : It is setting of Jumper switch SI when Emulation Pod (MB2147) is used.
Please refer to the Emulator hardware manual about details.

*2 : Embedded Algorithm is a trade mark of Advanced Micro Devices Inc.

■ PIN ASSIGNMENTS

- MB90V340(S) as seen with probe cable for LQFP-64

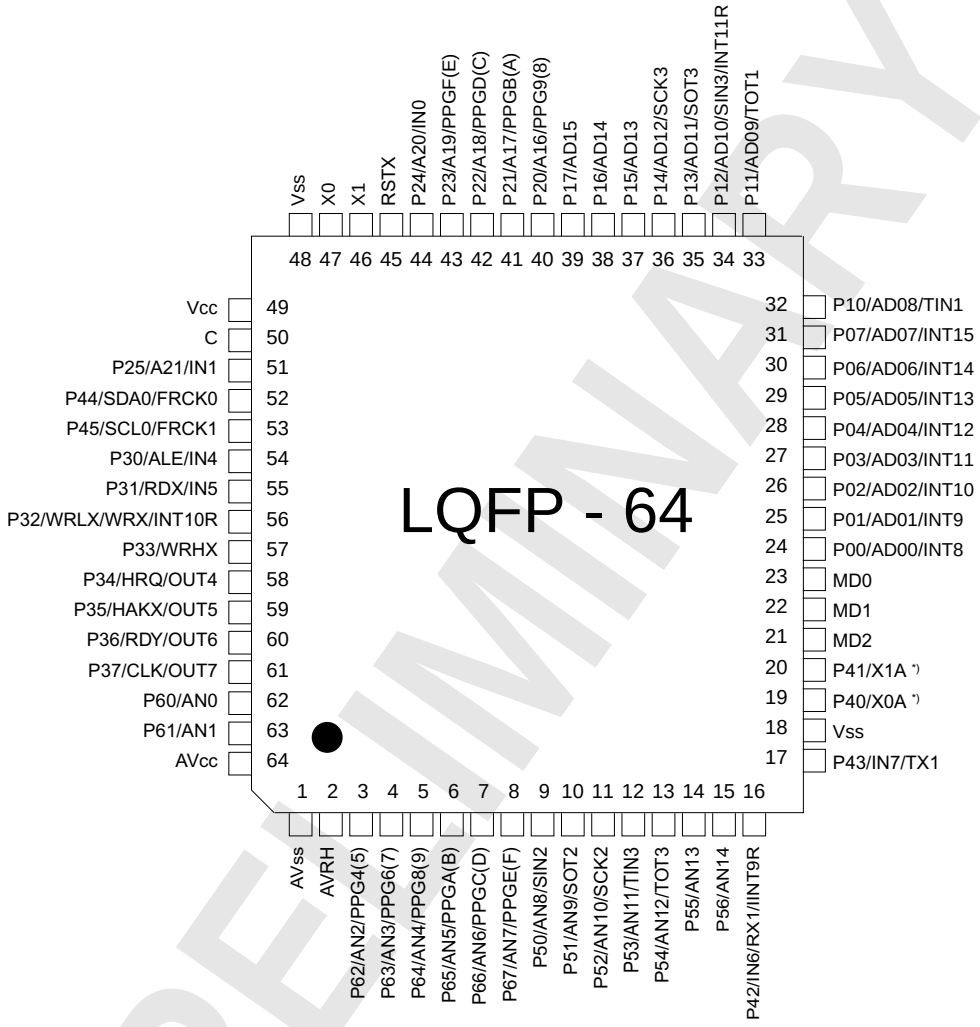
(TOP VIEW)
(FPT-64P-M09)



*) MB90V340: X0A, X1A
MB90V340S: P40, P41

- MB90F352(S)

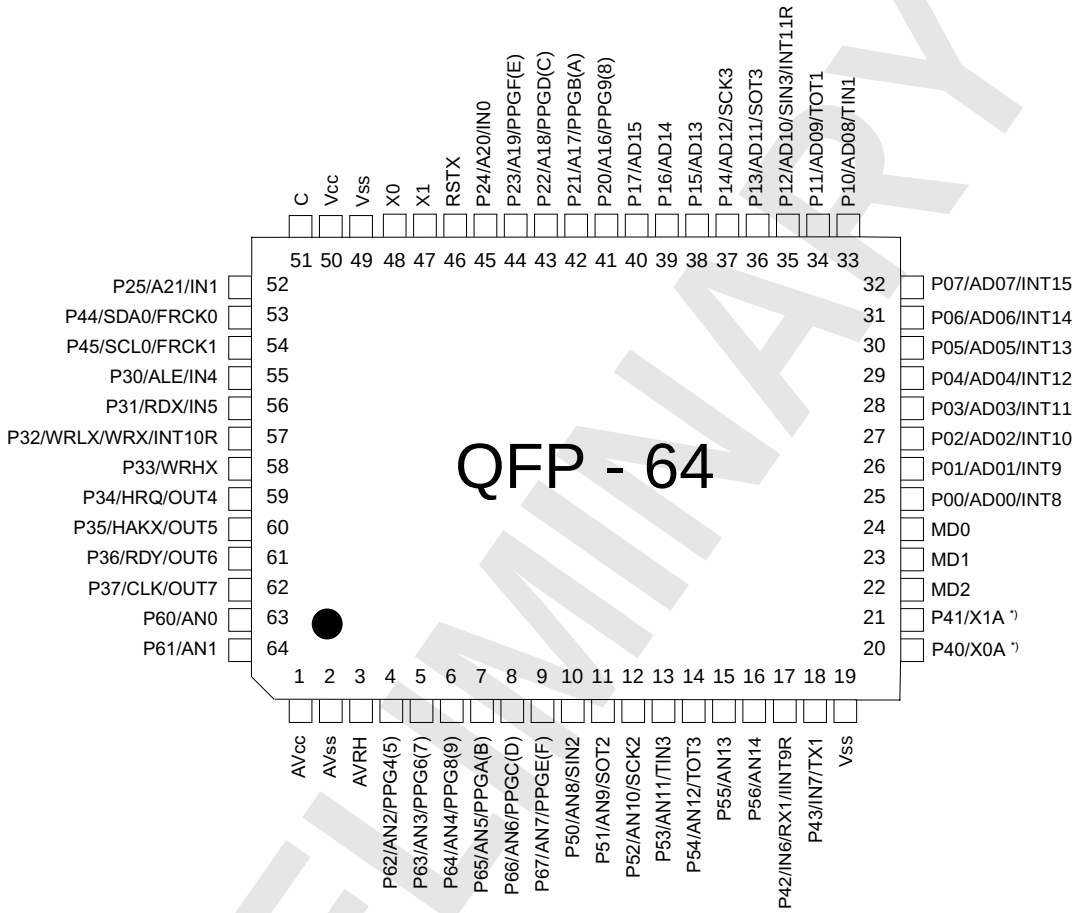
(TOP VIEW)
(FPT-64P-M09)



*) MB90F352: X0A, X1A
MB90F352S: P40, P41

- MB90F352(S)

(TOP VIEW)
(FPT-64P-M06)



*) MB90F352: X0A, X1A
MB90F352S: P40, P41

■ PIN DESCRIPTION

Pin No.		Pin name	Circuit type	Function
FPT-64P-M06	FPT-64P-M09			
46	45	RSTX	E	Reset input
48	47	X0	A	Oscillation input
47	46	X1		Oscillation output
25 to 31	24 to 31	P00 to P07	G	General purpose IO
		AD00 to AD07		I/O pins for 8 lower bits of the external address/data bus. This function is enabled when the external bus is enabled.
		INT8 to INT15		External interrupt request input pins for INT8 to INT15.
33	32	P10	G	General purpose IO
		AD08		I/O pin for 8th bit of the external address/data bus. This function is enabled when the external bus is enabled.
		TIN1		Event input pin for the reload timers 1.
34	33	P11	G	General purpose IO
		AD09		I/O pin for 9th bit of the external address/data bus. This function is enabled when the external bus is enabled.
		TOT1		Output pin for the reload timer 1.
35	34	P12	G	General purpose IO
		AD10		I/O pin for 10th bit of the external address/data bus. This function is enabled when the external bus is enabled.
		SIN3		Serial data input pin for UART3.
		INT11R		Second external interrupt request input pin for INT11.
36	35	P13	G	General purpose IO
		AD11		I/O pin for 11th bit of the external address/data bus. This function is enabled when the external bus is enabled.
		SOT3		Serial data output pin for UART3.
37	36	P14	G	General purpose IO
		AD12		I/O pin for 12th bit of the external address/data bus. This function is enabled when the external bus is enabled.
		SCK3		Clock I/O pin for UART3.
38	37	P15	G	General purpose IO
		AD13		I/O pin for 13th bit of the external address/data bus. This function is enabled when the external bus is enabled.
		SIN4		Serial data input pin for UART4 (MB90V340 only).
39	38	P16	G	General purpose IO
		AD14		I/O pin for 14th bit of the external address/data bus. This function is enabled when the external bus is enabled.
		SOT4		Serial data output pin for UART4 (MB90V340 only).

■ PIN DESCRIPTION

(continued)

Pin No.		Pin name	Circuit type	Function
FPT-64P-M06	FPT-64P-M09			
40	39	P17	G	General purpose IO
		AD15		I/O pin for 15th bit of the external address/data bus. This function is enabled when the external bus is enabled.
		SCK4		Clock I/O pin for UART4 (MB90V340 only).
41 to 44	40 to 43	P20 to P23	G	General purpose IO
		A16 to A19		Output pins for A16 to A17 of the external address bus. This function is enabled when the external bus is enabled.
		PPG9,PPGB, PPGD,PPGF		Output pins for PPGs.
45	44	P24	G	General purpose IO
		A20		Output pin for A20 of the external address bus. This function is enabled when the external bus is enabled.
		IN0		Data sample input pins for input capture ICU0.
52	51	P25	G	General purpose IO
		A21		Output pin for A21 of the external address bus. This function is enabled when the external bus is enabled.
		IN1		Data sample input pin for input capture ICU1.
55	54	P30	G	General purpose IO
		ALE		Address latch enable output pin. This function is enabled when the external bus is enabled.
		IN4		Data sample input pin for input capture ICU4.
56	55	P31	G	General purpose IO
		RDX		Read strobe output pin for the data bus. This function is enabled when the external bus is enabled.
		IN5		Data sample input pin for input capture ICU5.
57	56	P32	G	General purpose IO
		WRLX / WRX		Write strobe output pin for the data bus. This function is enabled when both the external bus and the WR/WRL pin output are enabled. WRL is used to write-strobe 8 lower bits of the data bus in 16-bit access while WR is used to write-strobe 8 bits of the data bus in 8-bit access.
		RX2		RX input pin for CAN2 Interface (MB90V340 only).
		INT10R		Second external interrupt request input pin for INT10.

■ PIN DESCRIPTION

(continued)

Pin No.		Pin name	Circuit type	Function
FPT-64P-M06	FPT-64P-M09			
58	57	P33	G	General purpose IO
		WRHX		Write strobe output pin for the 8 higher bits of the data bus. This function is enabled when the external bus is enabled, when the external bus 16-bit mode is selected, and when the WRH output pin is enabled.
		TX2		TX Output pin for CAN2 (MB90V340 only).
59	58	P34	G	General purpose IO
		HRQ		Hold request input pin. This function is enabled when both the external bus and the hold function are enabled.
		OUT4		Waveform output pin for output compares OCU4.
60	59	P35	G	General purpose IO
		HAKX		Hold acknowledge output pin. This function is enabled when both the external bus and the hold function are enabled.
		OUT5		Waveform output pin for output compares OCU5.
61	60	P36	G	General purpose IO
		RDY		Ready input pin. This function is enabled when both the external bus and the external ready function are enabled.
		OUT6		Waveform output pin for output compares OCU6.
62	61	P37	G	General purpose IO
		CLK		CLK output pin. This function is enabled when both the external bus and CLK output are enabled.
		OUT7		Waveform output pin for output compares OCU7.
63 to 64	62 to 63	P60 to P61	I	General purpose IO
		AN0 to AN1		Analog input pins for the A/D converter.
		PPG0,2		Output pins for PPGs (MB90V340 only).
4 to 9	3 to 8	P62 to P67	I	General purpose IO
		AN2 to AN7		Analog input pins for the A/D converter.
		PPG4,6,8 PPGA,C,E		Output pins for PPGs.
10	9	P50	I	General purpose IO
		AN8		Analog input pin for the A/D converter
		SIN2		Serial data input pin for UART2.
11	10	P51	I	General purpose IO
		AN9		Analog input pin for the A/D converter
		SOT2		Serial data output pin for UART2.

■ PIN DESCRIPTION

(continued)

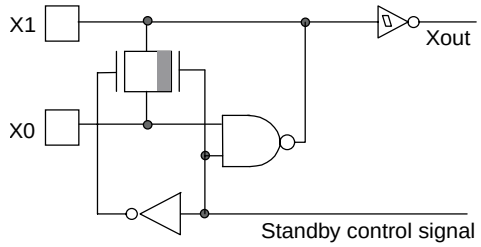
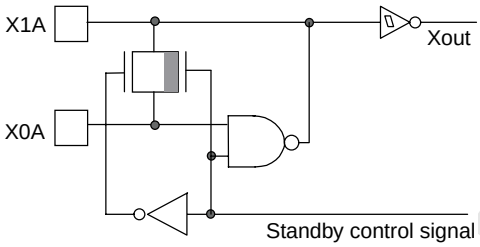
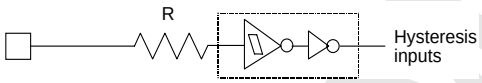
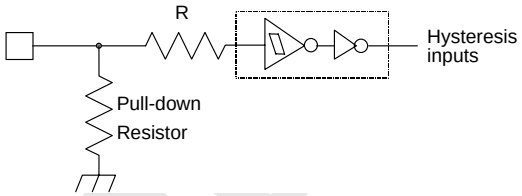
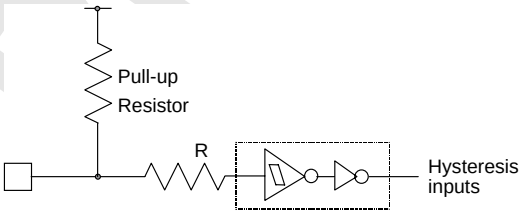
Pin No.		Pin name	Circuit type	Function
FPT-64P-M06	FPT-64P-M09			
12	11	P52	I	General purpose IO
		AN10		Analog input pin for the A/D converter
		SCK2		Clock I/O pin for UART2.
13	12	P53	I	General purpose IO
		AN11		Analog input pin for the A/D converter
		TIN3		Event input pin for the reload timer 3.
14	13	P54	I	General purpose IO
		AN12		Analog input pin for the A/D converter
		TOT3		Output pin for the reload timer 3.
15 to 16	14 to 15	P55 to P56	I	General purpose IO
		AN13 to AN14		Analog input pins for the A/D converter
17	16	P42	F	General purpose IO
		IN6		Data sample input pin for input capture ICU6.
		RX1		RX input pin for CAN1 Interface.
		INT9R		Second external interrupt request input pin for INT10.
18	17	P43	F	General purpose IO
		IN7		Data sample input pin for input capture ICU7.
		TX1		TX Output pin for CAN1.
53	52	P44	H	General purpose IO
		SDA0		Serial data I/O pin for I2C 0 (only devices with C-suffix)
		FRCK0		Input for the 16-bit IO Timer 0
54	53	P45	H	General purpose IO
		SCL0		Serial clock I/O pin for I2C 0 (only devices with C-suffix)
		FRCK1		Input for the 16-bit IO Timer 1
20 to 21	19 to 20	P40 to P41	F	General purpose IO (only for devices with S-suffix)
		X0A , X1A	B	Oscillator input pins for sub-clock (only for devices without S-suffix)
22	21	MD2	D	Input pin for specifying the operating mode. The pins must be directly connected to Vcc or Vss
23 to 24	22 to 23	MD1 to MD0	C	Input pins for specifying the operating mode. The pins must be directly connected to Vcc or Vss
19 49	18 48	VSS		Power (0V) input pins
50	49	VCC		Power (3.5V to 5.5V) input pin

■ PIN DESCRIPTION

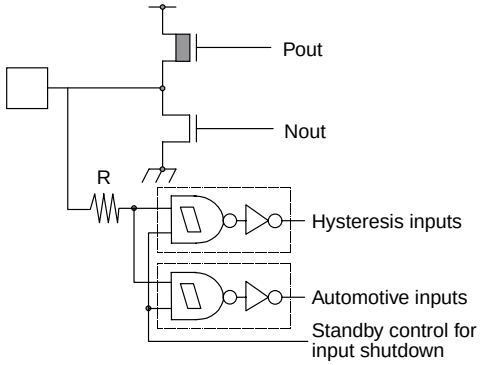
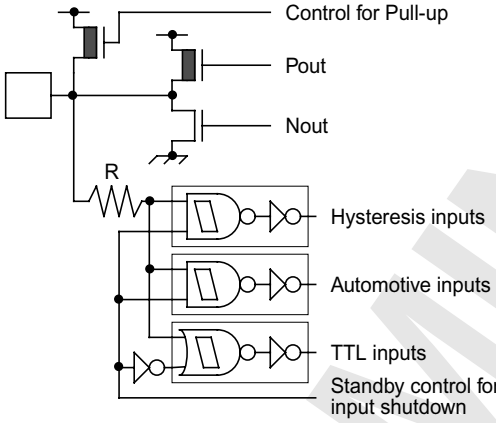
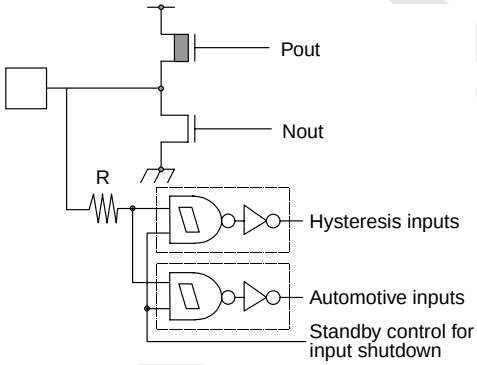
(continued)

Pin No.		Pin name	Circuit type	Function
FPT-64P-M06	FPT-64P-M09			
51	50	C	K	This is the power supply stabilization capacitor pin. It should be connected to a higher than or equal to 0.1µF ceramic capacitor.
1	64	AVCC	K	Vcc power input pin for analog circuits
2	1	AVSS	K	Vss power input pin for analog circuits and lower reference voltage input for the A/D Converter
3	2	AVRH	L	Reference voltage input for the A/D Converter. This power supply must be turned on or off while a voltage higher than or equal to AVRH is applied to AVCC .

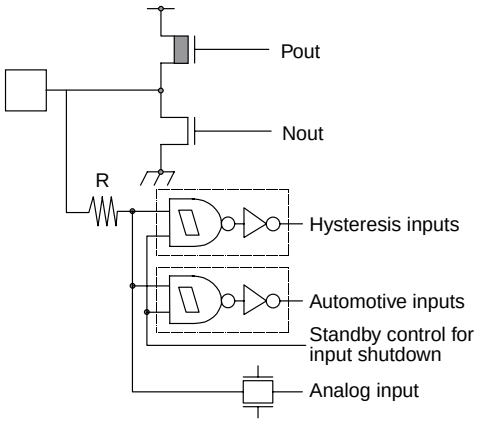
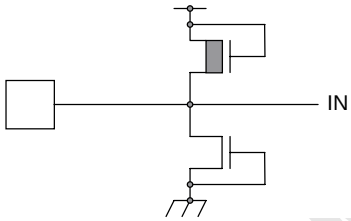
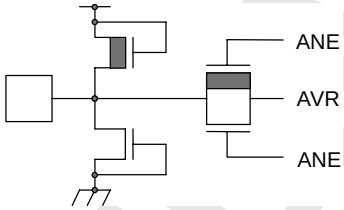
■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		Oscillation circuit • High-speed oscillation feedback resistor = approx. 1 MΩ
B		Oscillation circuit • Low-speed oscillation feedback resistor = approx. 1 MΩ
C		Mask ROM and EVA device: • CMOS Hysteresis input pin • Resistor value : approx. 50 kΩ (TYP) Flash device: • CMOS input pin • Resistor value : approx. 50 kΩ (TYP)
D		Mask ROM and EVA device: • CMOS Hysteresis input pin • Resistor value : approx. 50 kΩ (TYP) • Pull-down resistor valule: approx. 50 kΩ Flash device: • CMOS input pin • Resistor value : approx. 50 kΩ (TYP) • No Pull-down
E		CMOS Hysteresis input pin • Resistor value : approx. 50 kΩ (TYP) • Pull-up resistor valule: approx. 50 kΩ

(continued)

Type	Circuit	Remarks
F		• CMOS level output(I_{OL} = 4 mA) • CMOS hysteresis inputs (With the standby-time input shutdown function) • Automotive input (With the standby-time input shutdown function)
G		• CMOS level output(I_{OL} = 4 mA) • CMOS hysteresis inputs (With the standby-time input shutdown function) • Automotive input (With the standby-time input shutdown function) • TTL input (With the standby-time input shutdown function) • Programmalble pullup resistor: 50kΩ approx.
H		• CMOS level output(I_{OL} = 3 mA) • CMOS hysteresis inputs (With the standby-time input shutdown function) • Automotive input (With the standby-time input shutdown function)

(continued)

Type	Circuit	Remarks
I		• CMOS level output(I_{OL} = 4 mA) • CMOS hysteresis inputs (With the standby-time input shutdown function) • Automotive input (With the standby-time input shutdown function) • A/D analog input
K		Power supply input protection circuit
L		• A/D converter ref+ (AVRH) power supply input pin, With the protection circuit • Flash devices do not have a protection circuit against VCC for pin AVRH

■ HANDLING DEVICES

Special care is required for the following when handling the device :

- Preventing latch-up
- Treatment of unused pins
- Using external clock
- Power supply pins (V_{CC}/V_{SS})
- Pull-up/down resistors
- Crystal Oscillator Circuit
- Turning-on Sequence of Power Supply to A/D Converter and Analog Inputs
- Connection of Unused Pins of A/D Converter
- Notes on Energization
- Initialization

1. Preventing latch-up

CMOS IC chips may suffer latch-up under the following conditions :

- A voltage higher than V_{CC} or lower than V_{SS} is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between V_{CC} and V_{SS}.
- The AV_{CC} power supply is applied before the V_{CC} voltage.

Latch-up may increase the power supply current drastically, causing thermal damage to the device.

For the same reason, also be careful not to let the analog power-supply voltage (AV_{CC}, AVRH) exceed the digital power-supply voltage.

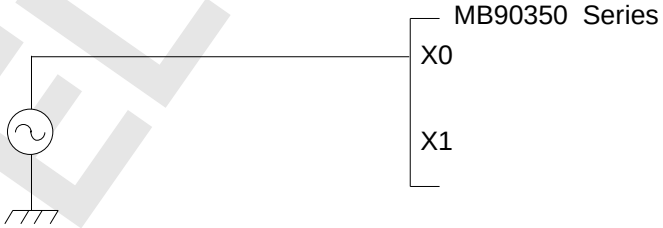
2. Handling unused pins

Leaving unused input pins open may result in misbehavior or latch up and possible permanent damage of the device. Therefore they must be pulled up or pulled down through resistors. In this case those resistors should be more than 2 KΩ .

Unused bidirectional pins should be set to the output state and can be left open, or the input state with the above described connection.

3. Using external clock

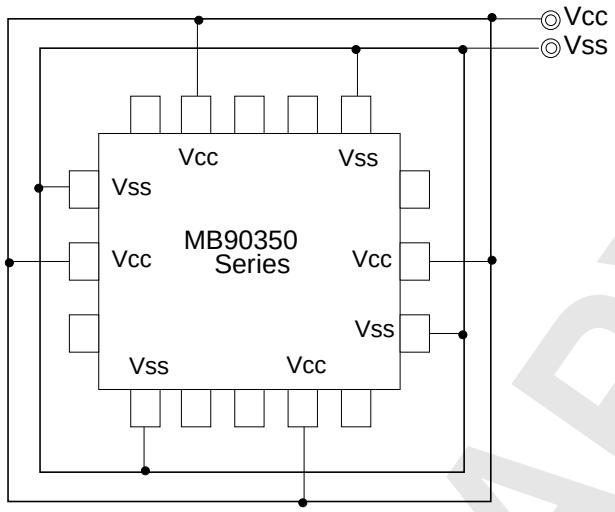
To use external clock, drive the X0 pin and leave X1 pin open.



4. Power supply pins (V_{CC}/V_{SS})

- If there are multiple V_{CC} and V_{SS} pins, from the point of view of device design, pins to be of the same potential are connected the inside of the device to prevent such malfunctioning as latch up.
  To reduce unnecessary radiation, prevent malfunctioning of the strobe signal due to the rise of ground level, and observe the standard for total output current, be sure to connect the V_{CC} and V_{SS} pins to the power supply and ground externally.
- Connect V_{CC} and V_{SS} to the device from the current supply source at a low impedance.

- As a measure against power supply noise, connect a capacitor of about 0.1 µF as a bypass capacitor between V_{CC} and V_{SS} in the vicinity of V_{CC} and V_{SS} pins of the device



5. Pull-up/down resistors

The MB90340 Series does not support internal pull-up/down resistors (except Port0 - Port3: programmable pull-up resistors). Use external components where needed.

6. Crystal Oscillator Circuit

Noises around X0 or X1 pins may be possible causes of abnormal operations. Make sure to provide bypass capacitors via shortest distance from X0, X1 pins, crystal oscillator (or ceramic resonator) and ground lines, and make sure, to the utmost effort, that lines of oscillation circuit not cross the lines of other circuits.

It is highly recommended to provide a printed circuit board art work surrounding X0 and X1 pins with a ground area for stabilizing the operation.

7. Turning-on Sequence of Power Supply to A/D Converter and Analog Inputs

Make sure to turn on the A/D converter power supply (AV_{CC}, AVRH) and analog inputs (AN0 to AN11) after turning-on the digital power supply (V_{CC}) .

Turn-off the digital power after turning off the A/D converter supply and analog inputs. In this case, make sure that the voltage not exceed AVRH or AV_{CC} (turning on/off the analog and digital power supplies simultaneously is acceptable) .

8. Connection of Pins of A/D Converter if A/D Converter is not used

Connect pins of unused A/D converter to $AV_{CC} = V_{CC}$, $AV_{SS} = AVRH = V_{SS}$.

9. Notes on Energization

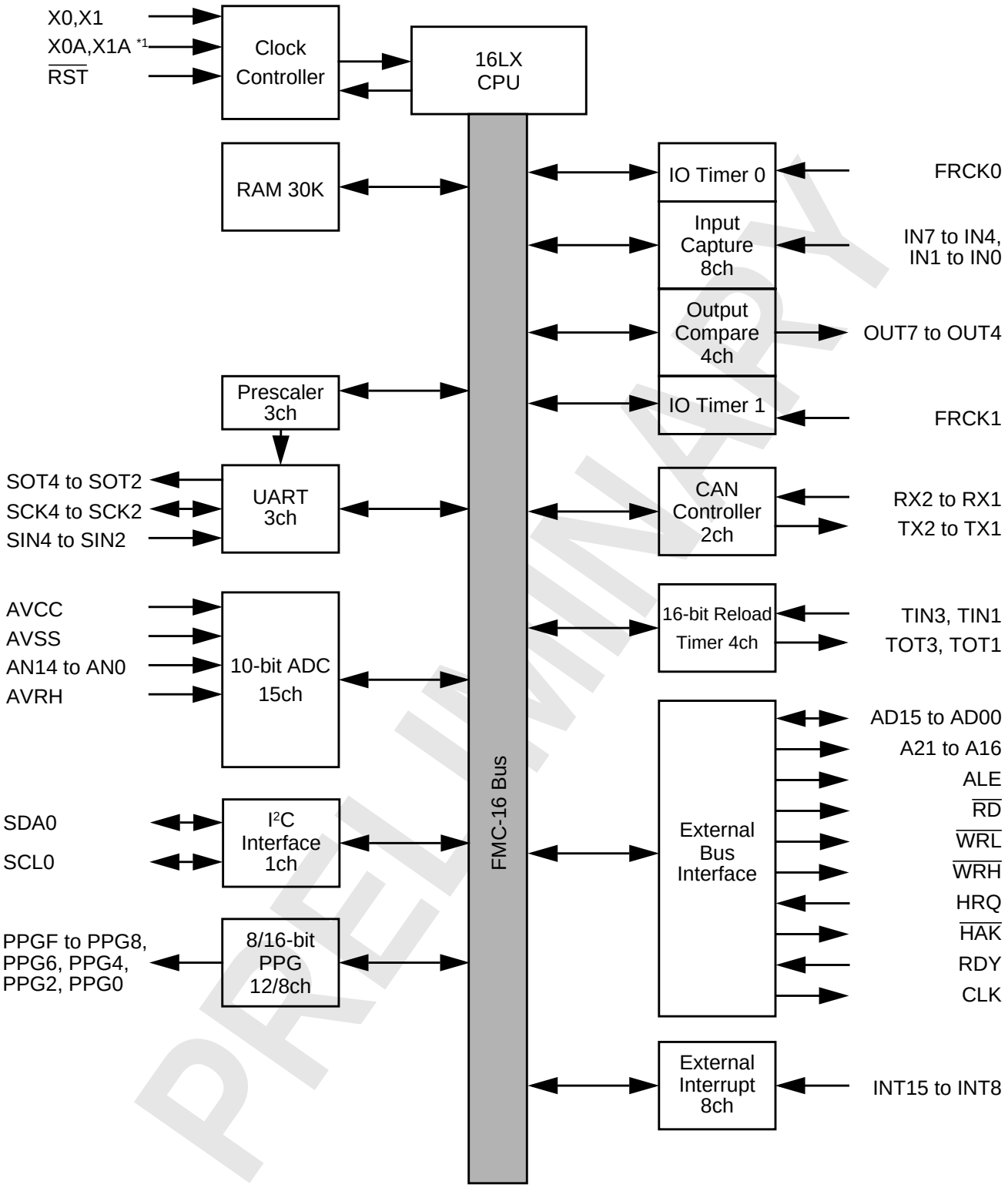
To prevent the internal regulator circuit from malfunctioning, set the voltage rise time during energization at 50 or more µs (0.2 V to 2.7 V)

10. Initialization

In the device, there are internal registers which is initialized only by a power-on reset. To initialize these registers, turn on the power again.

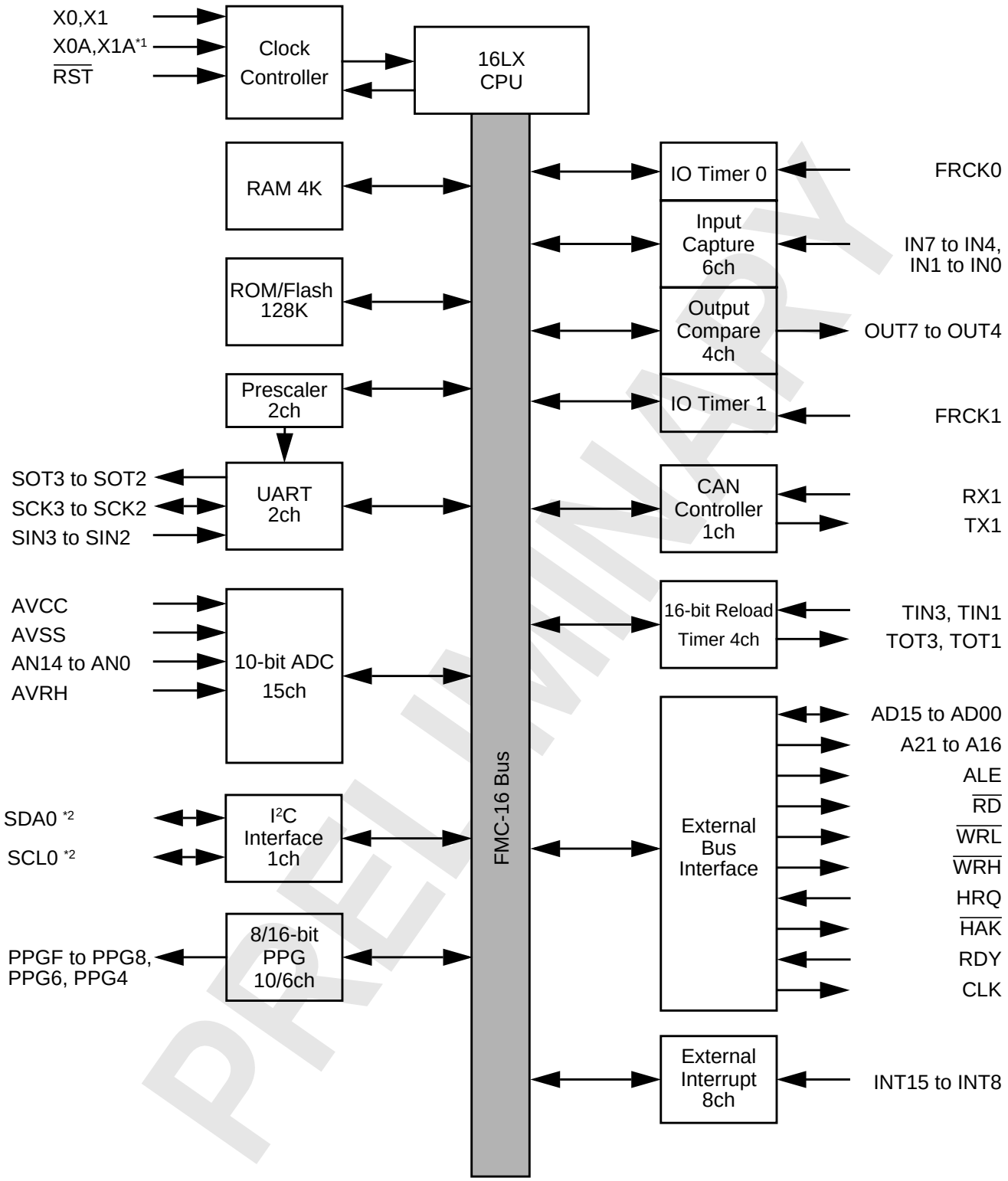
■ BLOCK DIAGRAMS

MB90V340(S)



***1) Only for MB90V340**

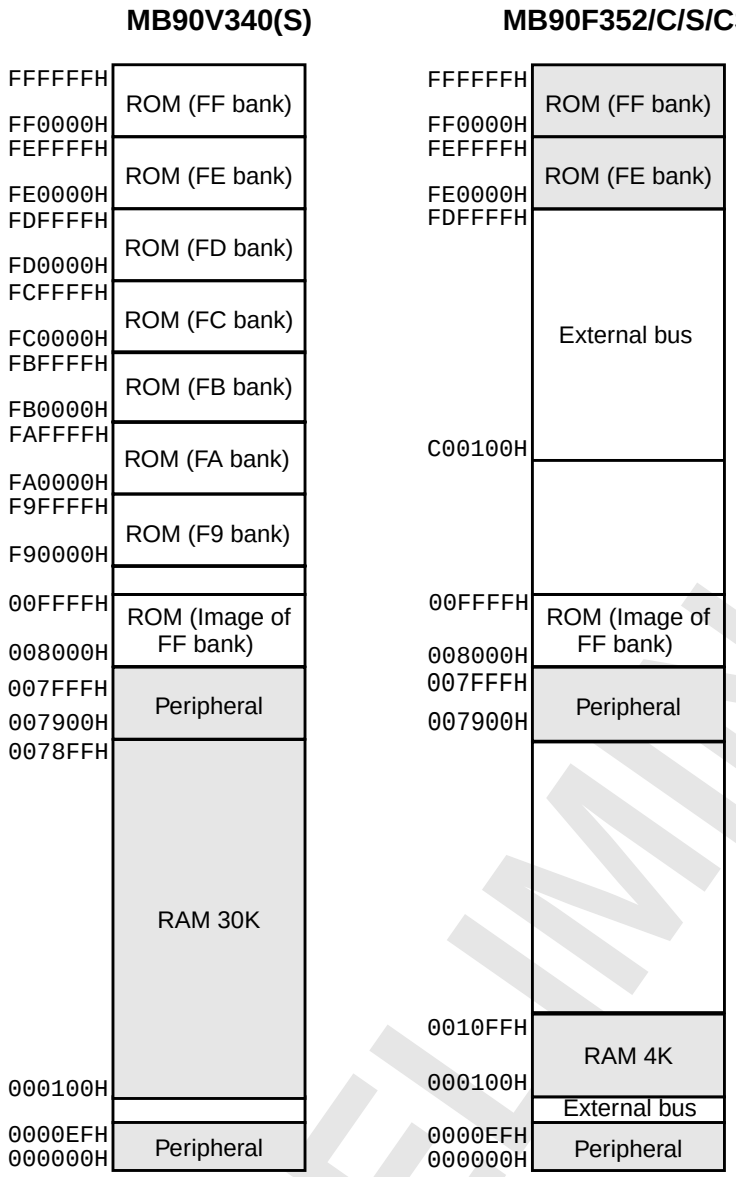
MB90F352/C(S)



***1) Only for devices without 'S' Suffix**

***2) Only for devices with 'C' Suffix**

■ MEMORY SPACE



Note : The high-order portion of bank 00 gives the image of the FF bank ROM to make the small model of the C compiler effective. Since the low-order 16 bits are the same, the table in ROM can be referenced without using the far specification in the pointer declaration.
For example, an attempt to access 00C000H accesses the value at FFC000H in ROM.
The ROM area in bank FF exceeds 32 Kbytes, and its entire image cannot be shown in bank 00.
The image between FF8000H and FFFFFFH is visible in bank 00, while the image between FF0000H and FF7FFFH is visible only in bank FF.