MB91520 Series

32-bit Microcontroller
FR Family FR81S
MB91F522B/D/F/J/K/L,MB91F523B/D/F/J/K/L,
MB91F524B/D/F/J/K/L,MB91F525B/D/F/J/K/L,MB91F526B/D/F/J/K/L*

Data Sheet (Full Production)

Publication Number MB91F526L_DS705-00011 Revision 2.0 Issue Date January 31, 2014

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Data Sheet (Full Production)

■ DESCRIPTION

The MB91520 series is a Spansion 32-bit microcontroller designed for automotive devices. This series contains the FR81S CPU which is compatible with the FR family.

Note: FR is a line of products of Spansion Inc.

*:This series is a composition of the kind that adds HB/JB/KB/LB/SB/UB/WB/YB to the end of the above-mentioned each name of articles of presence, According to Presence of sub-clock, CSV initial value and LVD initial value.
Please see "■ORDERING INFORMATION" for details.

Spansion provides information facilitating product development via the following website.
The website contains information useful for customers.

http://www.spansion.com/Support/microcontrollers/Pages/default.aspx

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■ FEATURES

● FR81S CPU Core

- 32-bit RISC, load/store architecture, pipeline 5-stage structure
- Maximum operating frequency: 80 MHz (Source oscillation = 4.0 MHz and 20 multiplied (PLL clock multiplication system))
- General-purpose register : 32 bits × 16 sets
- 16-bit fixed length instructions (basic instruction), 1 instruction per cycle
- Instructions appropriate to embedded applications
  - Memory-to-memory transfer instruction
  - Bit processing instruction
  - Barrel shift order etc.
- High-level language support instructions
- Function entry/exit instructions
- Register content multi-load and store instructions
- Bit search instructions
  Logical 1 detection, 0 detection, and change-point detection
- Branch instructions with delay slot
  Overhead reduction during branch process
- Register interlock function
  Easy assembler writing
- The support at the built-in / instruction level of the multiplier
  Signed 32-bit multiplication: 5 cycles
  Signed 16-bit multiplication: 3 cycles
- Interrupt (PC/PS saving)
  6 cycles (16 priority levels)
- The Harvard architecture allows simultaneous execution of program and data access.
- Instruction compatibility with the FR Family
- Built-in memory protection function (MPU)
  - Eight protection areas can be specified commonly for instructions and the data.
  - Control access privilege in both privilege mode and user mode.
- Built-in FPU (floating point arithmetic)
  - IEEE754 compliant
  - Floating-point register 32-bit × 16 sets

● Peripheral functions

- Clock generation (equipped with SSCG function)
  - Main oscillation (4MHz to 16MHz)
  - Sub oscillation (32kHz to 100kHz) or none sub oscillation
  - PLL multiplication rate : 1 to 20 times
- Built-in program flash memory capacity
  MB91F522:256+64KB
  MB91F523:384+64KB
  MB91F524:512+64KB
  MB91F525:768+64KB
  MB91F526:1024+64KB
- Flash memory for built-in data (WorkFlash) 64KB
- Built-in RAM capacity
  - Main RAM
    MB91F522:48KB
    MB91F523:48KB
    MB91F524:64KB
    MB91F525:96KB
    MB91F526:128KB
  - Backup RAM 8KB

- General-purpose ports:
  MB91F52xB 44 sets (No sub oscillation), 42 sets (sub oscillation)
  MB91F52xD 56 sets (No sub oscillation), 54 sets (sub oscillation)
  MB91F52xF 76 sets (No sub oscillation), 74 sets (sub oscillation)
  MB91F52xJ 96 sets (No sub oscillation), 94 sets (sub oscillation)
  MB91F52xK 120 sets (No sub oscillation), 118 sets (sub oscillation)
  MB91F52xL 152 sets (No sub oscillation), 150 sets (sub oscillation)
  Included I^2C open drain corresponding ports:16 sets
- External bus interface
  - 22-bit address, 16-bit data
- DMA Controller
  - Up to 16 channels can be started simultaneously.
  - 2 transfer factors (Internal peripheral request and software)
- A/D converter (successive approximation type)
  - 12-bit resolution : Max.48ch (32ch+16ch)
  - Conversion time : 1µs
- D/A converter (R-2R type)
  - 8-bit resolution : 2ch
- External interrupt input: 8 channels × 2 units total 16 channels
  - Level ("H" / "L"), or edge detection (rising or falling) enabled
- Multi-function serial communication (built-in transmission/reception FIFO memory) : Max.12 channels
  - 5V tolerant input: 4 channels ch.6, ch.8, ch.9, ch.11 CMOS hysteresis input
    < UART (Asynchronous serial interface) >
  - Full-duplex double buffering system, 64-step transmission FIFO memory, 64-step reception FIFO memory
  - Parity or no parity is selectable.
  - Built-in dedicated baud rate generator
  - An external clock can be used as the transfer clock
  - Parity, frame, and overrun error detection functions provided
  - DMA transfer support
    <CSIO (Synchronous serial interface) >
  - Full-duplex double buffering system, 64-step transmission FIFO memory, 64-step reception FIFO memory
  - SPI supported; master and slave systems supported; 5 to 16, 20, 24, 32-bit data length can be set.
  - Built-in dedicated baud rate generator (Master operation)
  - An external clock can be entered. (Slave operation)
  - Overrun error detection function is provided
  - DMA transfer support
  - Serial chip select SPI function
    <LIN (Asynchronous Serial Interface for LIN) >
  - Full-duplex double buffering system, 64-step transmission FIFO memory, 64-step reception FIFO memory
  - LIN protocol revision 2.1 supported
  - Master and slave systems supported
  - Framing error and overrun error detection
  - LIN synch break generation and detection; LIN synch delimiter generation
  - Built-in dedicated baud rate generator
  - An external clock can be adjusted by the reload counter
  - DMA transfer support
  - Hard assist function
    < I^2C >
  - 2 channels ch.3 , ch.4 Standard mode/high-speed mode supported.
  - 6 channels ch.5 to ch.8, ch.10, ch.11 Standard mode supported.
  - Full-duplex double buffering system, 64-step transmission FIFO memory, 64-step reception FIFO memory
  - Standard mode (Max. 100kbps) / high-speed mode (Max. 400kbps) supported
  - DMA transfer supported (for transmission only)

- CAN Controller (CAN) : 3 channels
  - Transfer speed : Up to 1Mbps
  - 128-transmission/reception message buffering : 1 channel (ch.0),
    64-transmission/reception message buffering : 2 channels (ch.1 and ch.2)
- PPG: 16-bit × Max. 48 channels
  - LED drive output 4 channels 11ch to 14ch
  - Reload timer : 16-bit × Max.8 channels
  - Free-run timer :
    16-bit × 3 channels
    32-bit × Max 3 channels
- Input capture :
  16-bit × 4 channels (linked to the free-run timer)
  32-bit × Max 6 channels (linked to the free-run timer)
- Output compare :
  16-bit × 6 channels (linked to the free-run timer)
  32-bit × Max 6 channels (linked to the free-run timer)
- Waveform generator : 6 channels
- Up/Down counter
  - 8/16-bit Up/Down counter × 2 channels
- Real-time clock (RTC) (for day, hours, minutes, seconds)
  - Main or sub oscillation frequency can be selected for the operation clock
- Calibration: Real-time clock (RTC) of the subclock drive
  - The main clock to sub clock ratio can be corrected by setting the real-time clock prescaler
- Clock Supervisor
  - Monitoring abnormality (by damaged quartz, etc.) of suboscillation (32kHz) (dual clock products) of the outside and main oscillation (4 MHz)
  - When abnormality is detected, it switches to the CR clock.
  - Initial value ON/OFF can be selected by the part number.
- Base timer : Max.2 channels
  - 16-bit timer
  - Any of four PWM/PPG/PWC/reload timer functions can be selected and used
  - A 32-bit timer can be used in 2 channels of cascade mode
- CRC generation
- Watchdog timer
  - Hardware watchdog
  - Software watchdog (possible to set the valid range for counter clearing)
- NMI (non-maskable interrupt)
- Interrupt controller
- Interrupt request batch read
  - The interrupt existence from two or more peripherals can be read by a series of register.
- I/O relocation
  - Peripheral function pins can be reassigned.
- Low-power consumption mode
  - Sleep / Stop / Watch / Sub RUN mode
  - Stop (power shutdown) / Watch (power shutdown) mode
- Power-on reset
- Low-voltage detection reset (independently monitor the external power supply and the internal power supply)
  - The external power supply can select initial value ON/OFF by the part number.
- Device Package : LQFP-176/144/120/100/80/64
- CMOS 90nm Technology
- Power supplies
  - 5V Power supply
  - The internal 1.2V is generated from 5V with the voltage step-down circuit.

■ PRODUCT LINEUP

● Product lineup comparison 64pins

	MB91F522B	MB91F523B	MB91F524B	MB91F525B	MB91F526B
System Clock	On chip PLL Clock multiple method				
Minimum instruction execution time	12.5ns (80MHz)				
Flash Capacity (Program)	(256+64)KB	(384+64)KB	(512+64)KB	(768+64)KB	(1024+64)KB
Flash Capacity (Data)	64KB				
RAM Capacity	(48+8)KB		(64+8)KB	(96+8)KB	(128+8)KB
External BUS I/F (22address/16data/4cs)	None				
DMA Transfer	16ch				
16-bit Base Timer	None				
Free-run Timer	16bit×3ch 32bit×1ch				
Input capture	16bit×4ch 32bit×5ch				
Output Compare	16bit×6ch 32bit×4ch				
16-bit Reload Timer	7ch				
PPG	16bit×21ch				
Up/down Counter	2ch				
Clock Supervisor	Yes				
External Interrupt	8ch×2units				
A/D converter	12bit×13ch (1unit) 12bit×13ch (1unit)				
D/A converter (8bit)	1ch				
Multi-Function Serial Interface	8ch				
CAN	64msg×2ch/128msg×1ch				
Hardware Watchdog Timer	Yes				
CRC Formation	Yes				
Low-voltage detection reset	Yes				
Flash Security	Yes				
ECC Flash/WorkFlash	Yes				
ECC RAM	Yes				
Memory Protection Function (MPU)	Yes				
Floating point arithmetic (FPU)	Yes				
Real Time Clock (RTC)	Yes				
General-purpose port (#GPIOs)	44 ports				
SSCG	Yes				
Sub clock	Yes				
CR oscillator	Yes				
OCD (On Chip Debug)	Yes				
TPU (Timing Protection Unit)	Yes				
Key code register	Yes				
Waveform generator	6ch				
NMI request function	Yes				
Operation guaranteed temperature (T_A)	-40°C to +125°C				
Power supply	2.7V to 5.5V				
Package	LQFP-64				

● Product lineup comparison 80pins

	MB91F522D	MB91F523D	MB91F524D	MB91F525D	MB91F526D
System Clock	On chip PLL Clock multiple method				
Minimum instruction execution time	12.5ns (80MHz)				
Flash Capacity (Program)	(256+64)KB	(384+64)KB	(512+64)KB	(768+64)KB	(1024+64)KB
Flash Capacity (Data)	64KB				
RAM Capacity	(48+8)KB		(64+8)KB	(96+8)KB	(128+8)KB
External BUS I/F (22address/16data/4cs)	None				
DMA Transfer	16ch				
16-bit Base Timer	1ch				
Free-run Timer	16bit×3ch 32bit×2ch				
Input capture	16bit×4ch 32bit×5ch				
Output Compare	16bit×6ch 32bit×4ch				
16-bit Reload Timer	7ch				
PPG	16bit×27ch				
Up/down Counter	2ch				
Clock Supervisor	Yes				
External Interrupt	8ch×2units				
A/D converter	12bit×16ch (1unit) 12bit×16ch (1unit)				
D/A converter (8bit)	1ch				
Multi-Function Serial Interface	9ch				
CAN	64msg×2ch/128msg×1ch				
Hardware Watchdog Timer	Yes				
CRC Formation	Yes				
Low-voltage detection reset	Yes				
Flash Security	Yes				
ECC Flash/WorkFlash	Yes				
ECC RAM	Yes				
Memory Protection Function (MPU)	Yes				
Floating point arithmetic (FPU)	Yes				
Real Time Clock (RTC)	Yes				
General-purpose port (#GPIOs)	56 ports				
SSCG	Yes				
Sub clock	Yes				
CR oscillator	Yes				
NMI request function	Yes				
OCD (On Chip Debug)	Yes				
TPU (Timing Protection Unit)	Yes				
Key code register	Yes				
Waveform generator	6ch				
Operation guaranteed temperature (T_A)	-40°C to +125°C				
Power supply	2.7V to 5.5V				
Package	LQFP-80				

● Product lineup comparison 100pins

	MB91F522F	MB91F523F	MB91F524F	MB91F525F	MB91F526F
System Clock	On chip PLL Clock multiple method				
Minimum instruction execution time	12.5ns (80MHz)				
Flash Capacity (Program)	(256+64)KB	(384+64)KB	(512+64)KB	(768+64)KB	(1024+64)KB
Flash Capacity (Data)	64KB				
RAM Capacity	(48+8)KB		(64+8)KB	(96+8)KB	(128+8)KB
External BUS I/F (22address/16data/4cs)	None				
DMA Transfer	16ch				
16-bit Base Timer	1ch				
Free-run Timer	16bit×3ch 32bit×3ch				
Input capture	16bit×4ch 32bit×6ch				
Output Compare	16bit×6ch 32bit×6ch				
16-bit Reload Timer	8ch				
PPG	16bit×34ch				
Up/down Counter	2ch				
Clock Supervisor	Yes				
External Interrupt	8ch×2units				
A/D converter	12bit×21ch (1unit) 12bit×16ch (1unit)				
D/A converter (8bit)	2ch				
Multi-Function Serial Interface	12ch				
CAN	64msg×2ch/128msg×1ch				
Hardware Watchdog Timer	Yes				
CRC Formation	Yes				
Low-voltage detection reset	Yes				
Flash Security	Yes				
ECC Flash/WorkFlash	Yes				
ECC RAM	Yes				
Memory Protection Function (MPU)	Yes				
Floating point arithmetic (FPU)	Yes				
Real Time Clock (RTC)	Yes				
General-purpose port (#GPIOs)	76 ports				
SSCG	Yes				
Sub clock	Yes				
CR oscillator	Yes				
NMI request function	Yes				
OCD (On Chip Debug)	Yes				
TPU (Timing Protection Unit)	Yes				
Key code register	Yes				
Waveform generator	6ch				
Operation guaranteed temperature (T_A)	-40°C to +125°C				
Power supply	2.7V to 5.5V				
Package	LQFP-100				

● Product lineup comparison 120pins

	MB91F522J	MB91F523J	MB91F524J	MB91F525J	MB91F526J
System Clock	On chip PLL Clock multiple method				
Minimum instruction execution time	12.5ns (80MHz)				
Flash Capacity (Program)	(256+64)KB	(384+64)KB	(512+64)KB	(768+64)KB	(1024+64)KB
Flash Capacity (Data)	64KB				
RAM Capacity	(48+8)KB		(64+8)KB	(96+8)KB	(128+8)KB
External BUS I/F (22address/16data/4cs)	None				
DMA Transfer	16ch				
16-bit Base Timer	2ch				
Free-run Timer	16bit×3ch 32bit×3ch				
Input capture	16bit×4ch 32bit×6ch				
Output Compare	16bit×6ch 32bit×6ch				
16-bit Reload Timer	8ch				
PPG	16bit×38ch				
Up/down Counter	2ch				
Clock Supervisor	Yes				
External Interrupt	8ch×2units				
A/D converter	12bit×26ch (1unit) 12bit×16ch (1unit)				
D/A converter (8bit)	2ch				
Multi-Function Serial Interface	12ch				
CAN	64msg×2ch/128msg×1ch				
Hardware Watchdog Timer	Yes				
CRC Formation	Yes				
Low-voltage detection reset	Yes				
Flash Security	Yes				
ECC Flash/WorkFlash	Yes				
ECC RAM	Yes				
Memory Protection Function (MPU)	Yes				
Floating point arithmetic (FPU)	Yes				
Real Time Clock (RTC)	Yes				
General-purpose port (#GPIOs)	96 ports				
SSCG	Yes				
Sub clock	Yes				
CR oscillator	Yes				
NMI request function	Yes				
OCD (On Chip Debug)	Yes				
TPU (Timing Protection Unit)	Yes				
Key code register	Yes				
Waveform generator	6ch				
Operation guaranteed temperature (T_A)	-40°C to +125°C				
Power supply	2.7V to 5.5V				
Package	LQFP-120				

● Product lineup comparison 144pins

	MB91F522K	MB91F523K	MB91F524K	MB91F525K	MB91F526K
System Clock	On chip PLL Clock multiple method				
Minimum instruction execution time	12.5ns (80MHz)				
Flash Capacity (Program)	(256+64)KB	(384+64)KB	(512+64)KB	(768+64)KB	(1024+64)KB
Flash Capacity (Data)	64KB				
RAM Capacity	(48+8)KB		(64+8)KB	(96+8)KB	(128+8)KB
External BUS I/F (22address/16data/4cs)	Yes				
DMA Transfer	16ch				
16-bit Base Timer	2ch				
Free-run Timer	16bit×3ch 32bit×3ch				
Input capture	16bit×4ch 32bit×6ch				
Output Compare	16bit×6ch 32bit×6ch				
16-bit Reload Timer	8ch				
PPG	16bit×44ch				
Up/down Counter	2ch				
Clock Supervisor	Yes				
External Interrupt	8ch×2units				
A/D converter	12bit×32ch (1unit) 12bit×16ch (1unit)				
D/A converter (8bit)	2ch				
Multi-Function Serial Interface	12ch				
CAN	64msg×2ch/128msg×1ch				
Hardware Watchdog Timer	Yes				
CRC Formation	Yes				
Low-voltage detection reset	Yes				
Flash Security	Yes				
ECC Flash/WorkFlash	Yes				
ECC RAM	Yes				
Memory Protection Function (MPU)	Yes				
Floating point arithmetic (FPU)	Yes				
Real Time Clock (RTC)	Yes				
General-purpose port (#GPIOs)	120 ports				
SSCG	Yes				
Sub clock	Yes				
CR oscillator	Yes				
NMI request function	Yes				
OCD (On Chip Debug)	Yes				
TPU (Timing Protection Unit)	Yes				
Key code register	Yes				
Waveform generator	6ch				
Operation guaranteed temperature (T_A)	-40°C to +125°C				
Power supply	2.7V to 5.5V				
Package	LQFP-144				

● Product lineup comparison 176pins

	MB91F522L	MB91F523L	MB91F524L	MB91F525L	MB91F526L
System Clock	On chip PLL Clock multiple method				
Minimum instruction execution time	12.5ns (80MHz)				
Flash Capacity (Program)	(256+64)KB	(384+64)KB	(512+64)KB	(768+64)KB	(1024+64)KB
Flash Capacity (Data)	64KB				
RAM Capacity	(48+8)KB		(64+8)KB	(96+8)KB	(128+8)KB
External BUS I/F (22address/16data/4cs)	Yes				
DMA Transfer	16ch				
16-bit Base Timer	2ch				
Free-run Timer	16bit×3ch 32bit×3ch				
Input capture	16bit×4ch 32bit×6ch				
Output Compare	16bit×6ch 32bit×6ch				
16-bit Reload Timer	8ch				
PPG	16bit×48ch				
Up/down Counter	2ch				
Clock Supervisor	Yes				
External Interrupt	8ch×2units				
A/D converter	12bit×32ch (1unit) 12bit×16ch (1unit)				
D/A converter (8bit)	2ch				
Multi-Function Serial Interface	12ch				
CAN	64msg×2ch/128msg×1ch				
Hardware Watchdog Timer	Yes				
CRC Formation	Yes				
Low-voltage detection reset	Yes				
Flash Security	Yes				
ECC Flash/WorkFlash	Yes				
ECC RAM	Yes				
Memory Protection Function (MPU)	Yes				
Floating point arithmetic (FPU)	Yes				
Real Time Clock (RTC)	Yes				
General-purpose port (#GPIOs)	152 ports				
SSCG	Yes				
Sub clock	Yes				
CR oscillator	Yes				
NMI request function	Yes				
OCD (On Chip Debug)	Yes				
TPU (Timing Protection Unit)	Yes				
Key code register	Yes				
Waveform generator	6ch				
Operation guaranteed temperature (T_A)	-40°C to +125°C				
Power supply	2.7V to 5.5V				
Package	LQFP-176				

- **Table for clock supervisor and external low voltage detection reset initial value ON/OFF**

Clock	CSV Initial value	LVD Initial value	Function
single	ON	ON	S
		OFF	U
	OFF	ON	H
		OFF	K
Dual	ON	ON	W
		OFF	Y
	OFF	ON	J
		OFF	L

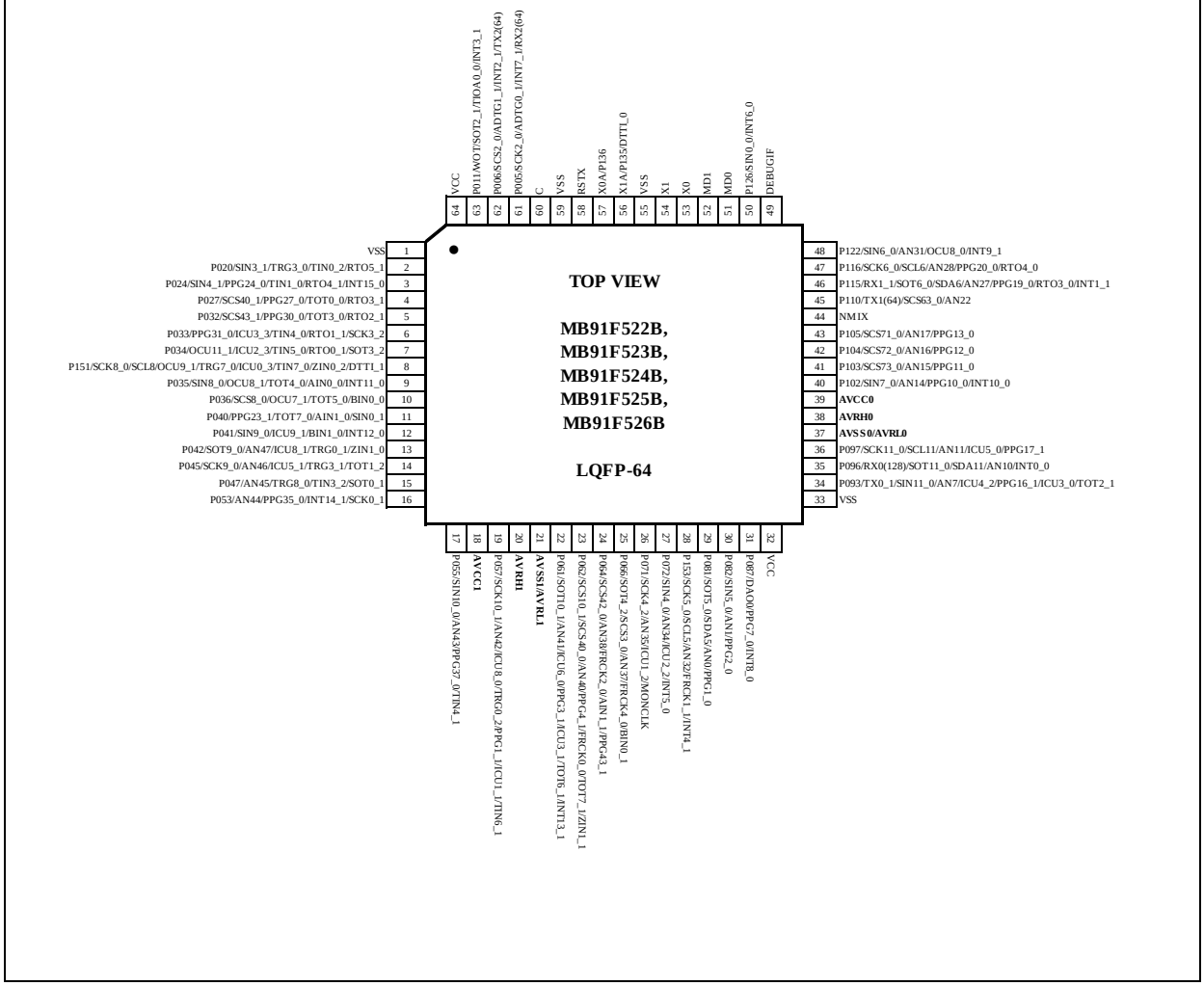
```
ＭＢ９１Ｆ５２Ｘ□△○
            │ │ │ └→Ｒｅｖｉｓｉｏｎ：Ｂ
            │ │ └──→Ｆｕｎｃｔｉｏｎ：See the table for clock supervisor and external
            │ │                    low voltage detection reset initial value ON/OFF.
            │ └───→ＰＫＧ Ｔｙｐｅ：Ｂ ６４ｐｉｎ
            │                    Ｄ ８０ ｐｉｎ
            │                    Ｆ １００ ｐｉｎ
            │                    Ｊ １２０ ｐｉｎ
            │                    Ｋ １４４ ｐｉｎ
            │                    Ｌ １７６ ｐｉｎ
            └────→Ｍｅｍｏｒｙ Ｓｉｚｅ：２ ２５６ＫＢ
                                   ３ ３８４ＫＢ
                                   ４ ５１２ＫＢ
                                   ５ ７６８ＫＢ
                                   ６ １ＭＢ
```

■ PIN ASSIGNMENT

● MB91F52xB

MB91F522B, MB91F523B, MB91F524B, MB91F525B, MB91F526B

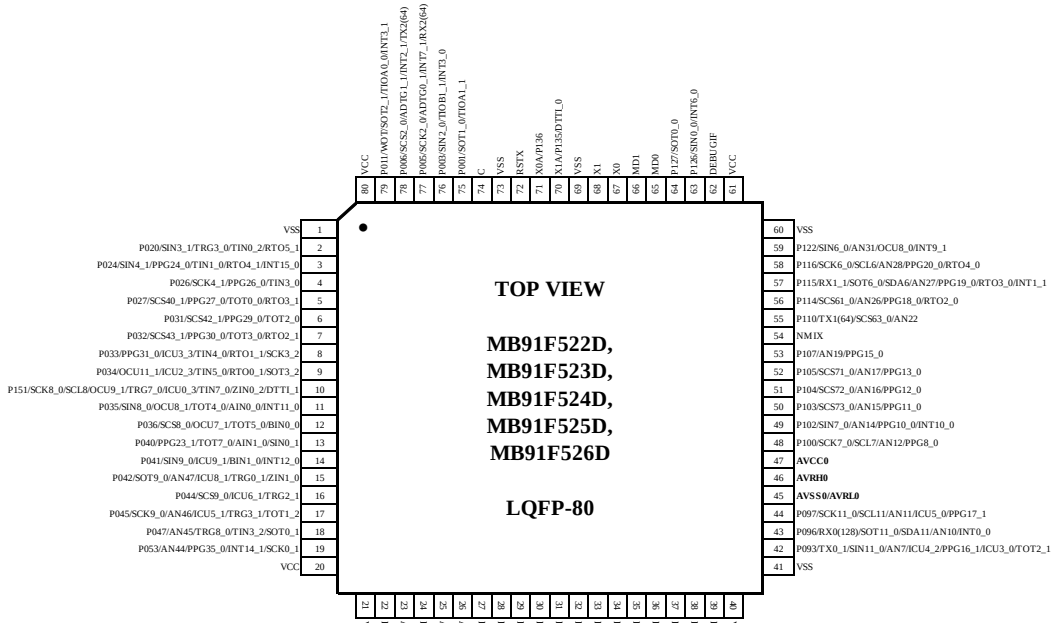
(TOP VIEW)



● MB91F52xD

MB91F522D, MB91F523D, MB91F524D, MB91F525D, MB91F526D

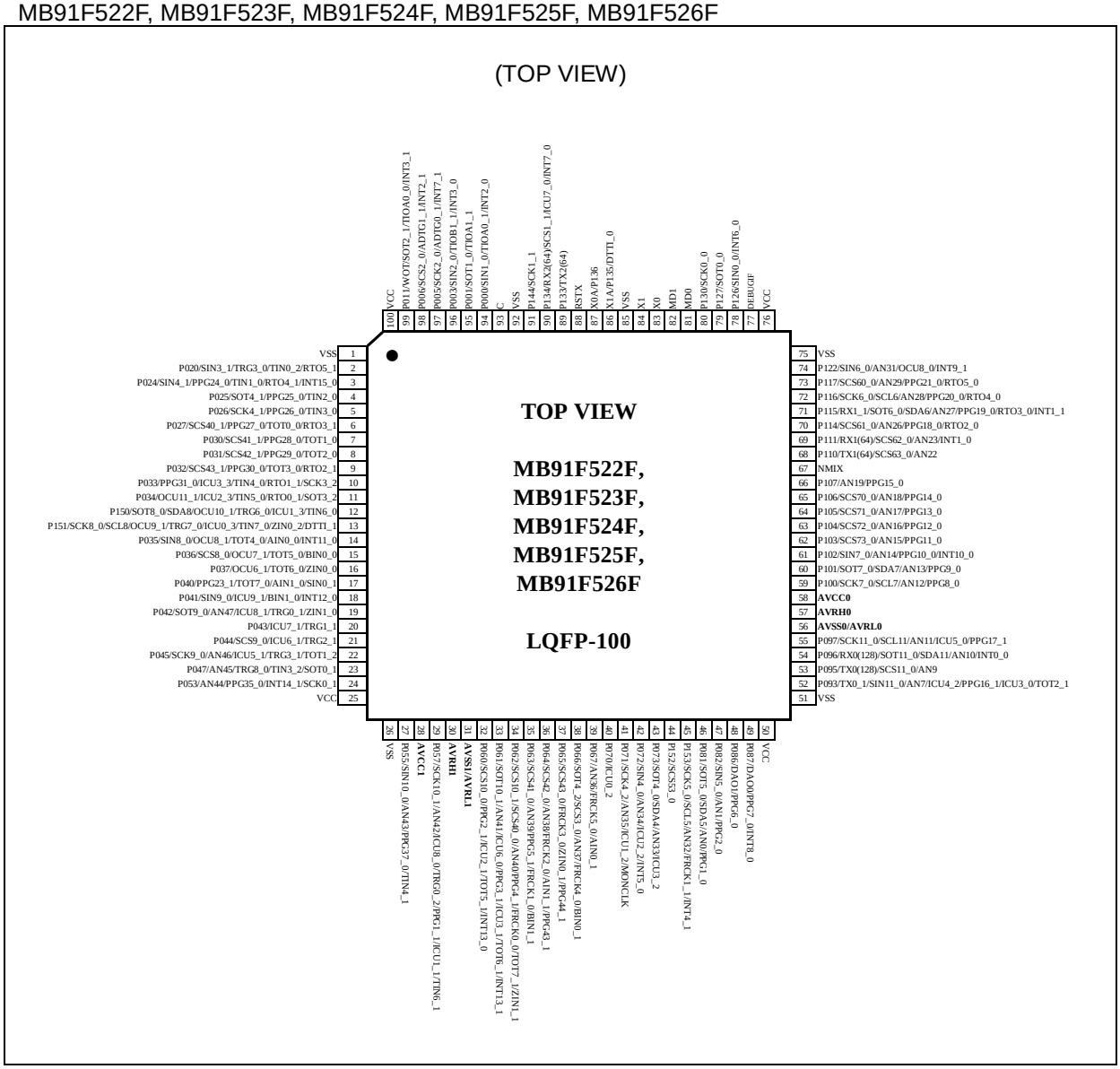
(TOP VIEW)



● MB91F52xF

MB91F522F, MB91F523F, MB91F524F, MB91F525F, MB91F526F

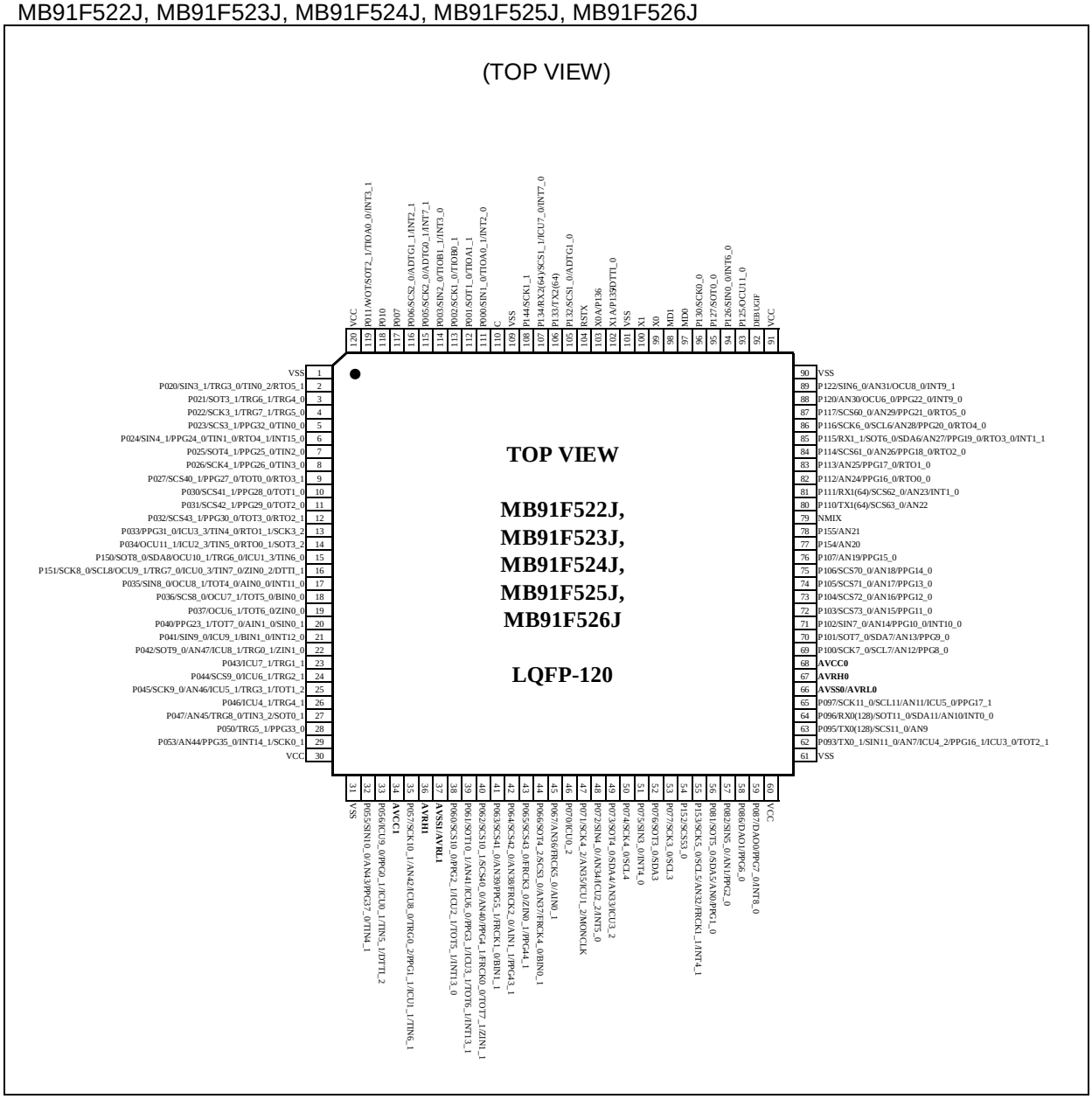
(TOP VIEW)



● MB91F52xJ

MB91F522J, MB91F523J, MB91F524J, MB91F525J, MB91F526J

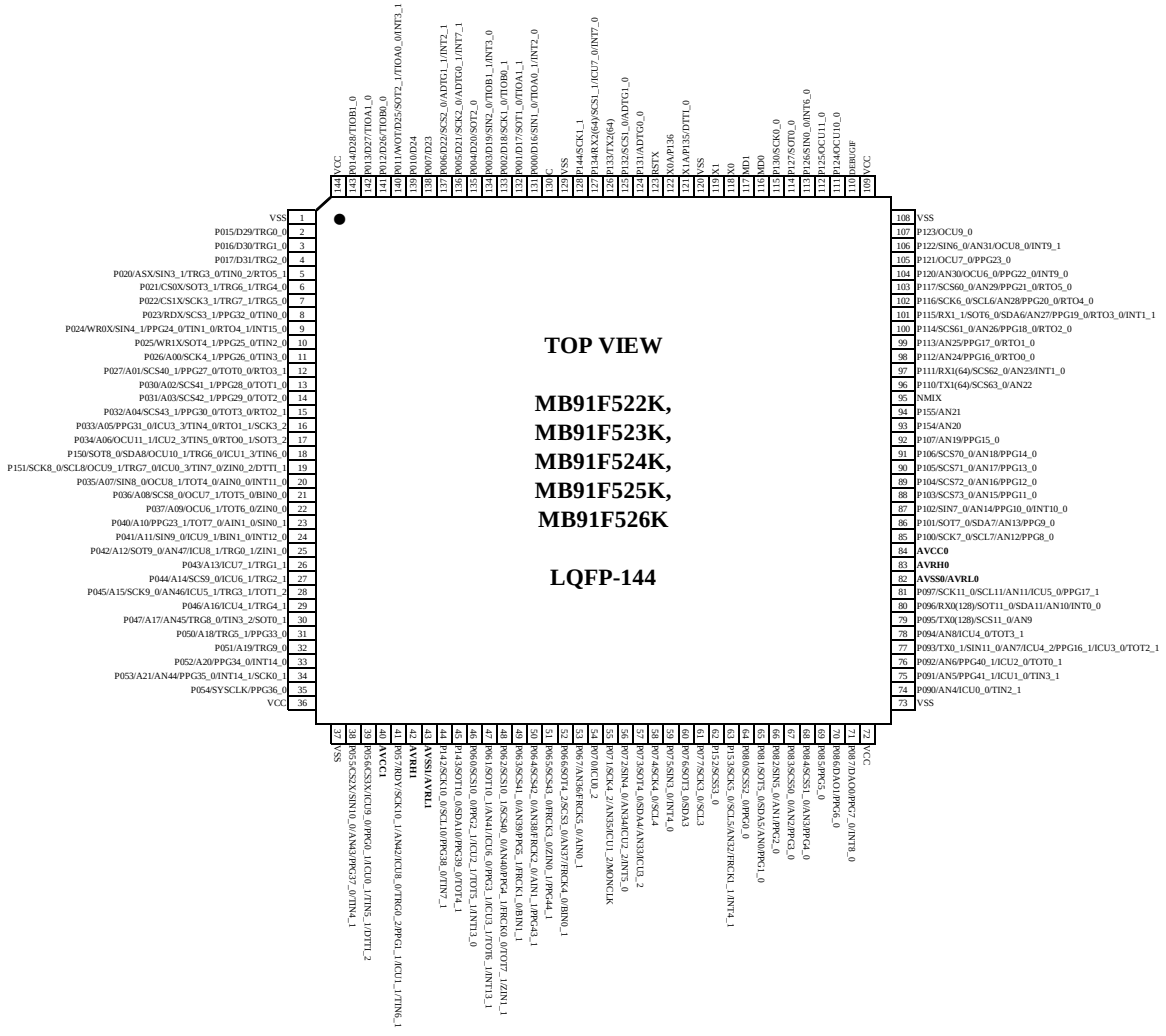
(TOP VIEW)



● MB91F52xK

MB91F522K, MB91F523K, MB91F524K, MB91F525K, MB91F526K

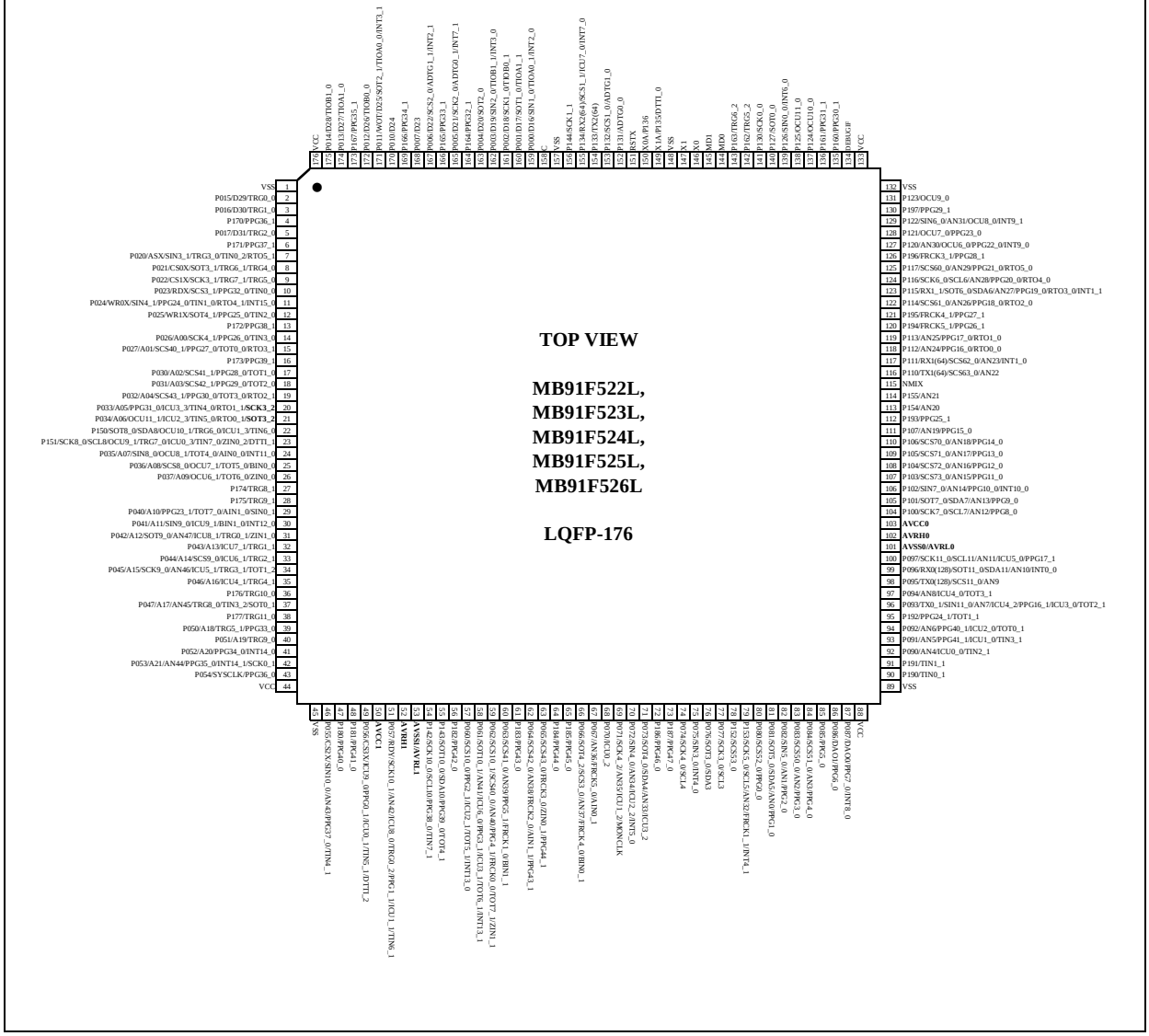
(TOP VIEW)



● MB91F52xL

MB91F522L, MB91F523L, MB91F524L, MB91F525L, MB91F526L

(TOP VIEW)



■ PIN DESCRIPTION

Pin no.						Pin Name	Polarity	I/O circuit types*1	Function*2
64	80	100	120	144	176				
-	-	-	-	2	2	P015	-	A	General-purpose I/O port
						D29	-		External bus data bit29 I/O (0)
						TRG0_0	-		PPG trigger 0 input (0)
-	-	-	-	3	3	P016	-	A	General-purpose I/O port
						D30	-		External bus data bit30 I/O (0)
						TRG1_0	-		PPG trigger 1 input (0)
-	-	-	-	-	4	P170	-	A	General-purpose I/O port
						PPG36_1	-		PPG ch.36 output (1)
-	-	-	-	4	5	P017	-	A	General-purpose I/O port
						D31	-		External bus data bit31 I/O (0)
						TRG2_0	-		PPG trigger 2 input (0)
-	-	-	-	-	6	P171	-	A	General-purpose I/O port
						PPG37_1	-		PPG ch.37 output (1)
2	2	2	2	5	7	P020	-	F	General-purpose I/O port
						ASX	-		External bus/Address strobe output
						SIN3_1	-		Multi-function serial ch.3 serial data input (1)
						TRG3_0	-		PPG trigger 3 input (0)
						TIN0_2	-		Reload timer ch.0 event input (2)
						RTO5_1	-		Waveform generator ch.5 output pin (1)
-	-	-	3	6	8	P021	-	A	General-purpose I/O port
						CS0X	-		External bus chip select 0 output
						SOT3_1	-		Multi-function serial ch.3 serial data output (1)
						TRG6_1	-		PPG trigger 6 input (1)
						TRG4_0	-		PPG trigger 4 input (0)
-	-	-	4	7	9	P022	-	F	General-purpose I/O port
						CS1X	-		External bus chip select 1 output
						SCK3_1	-		Multi-function serial ch.3 clock I/O (1)
						TRG7_1	-		PPG trigger 7 input (1)
						TRG5_0	-		PPG trigger 5 input (0)
-	-	-	5	8	10	P023	-	A	General-purpose I/O port
						RDX	-		External bus/Read strobe output
						SCS3_1	-		Serial chip select 3 output (1)
						PPG32_0	-		PPG ch.32 output (0)
						TIN0_0	-		Reload timer ch.0 event input (0)
3	3	3	6	9	11	P024	-	F	General-purpose I/O port
						WR0X	-		External bus/Write strobe 0 output
						SIN4_1	-		Multi-function serial ch.4 serial data input (1)
						PPG24_0	-		PPG ch.24 output (0)
						TIN1_0	-		Reload timer ch.1 event input (0)
						RTO4_1	-		Waveform generator ch.4 output pin (1)
						INT15_0	-		INT15 External interrupt input (0)

Pin no.						Pin Name	Polarity	I/O circuit types*1	Function*2
64	80	100	120	144	176				
-	-	4	7	10	12	P025	-	A	General-purpose I/O port
						WR1X	-		External bus/Write strobe 1 output
						SOT4_1	-		Multi-function serial ch.4 serial data output (1)
						PPG25_0	-		PPG ch.25 output (0)
						TIN2_0	-		Reload timer ch.2 event input (0)
-	-	-	-	-	13	P172	-	A	General-purpose I/O port
						PPG38_1	-		PPG ch.38 output (1)
-	4	5	8	11	14	P026	-	F	General-purpose I/O port
						A00	-		External bus/Address bit0 output (0)
						SCK4_1	-		Multi-function serial ch.4 clock I/O (1)
						PPG26_0	-		PPG ch.26 output (0)
						TIN3_0	-		Reload timer ch.3 event input (0)
4	5	6	9	12	15	P027	-	A	General-purpose I/O port
						A01	-		External bus/Address bit1 output (0)
						SCS40_1	-		Serial chip select 40 I/O (1)
						PPG27_0	-		PPG ch.27 output (0)
						TOT0_0	-		Reload timer ch.0 output (0)
						RTO3_1	-		Waveform generator ch.3 output pin (1)
-	-	-	-	-	16	P173	-	A	General-purpose I/O port
						PPG39_1	-		PPG ch.39 output (1)
-	-	7	10	13	17	P030	-	A	General-purpose I/O port
						A02	-		External bus/Address bit2 output (0)
						SCS41_1	-		Serial chip select 41 output (1)
						PPG28_0	-		PPG ch.28 output (0)
						TOT1_0	-		Reload timer ch.1 output (0)
-	6	8	11	14	18	P031	-	A	General-purpose I/O port
						A03	-		External bus/Address bit3 output (0)
						SCS42_1	-		Serial chip select 42 output (1)
						PPG29_0	-		PPG ch.29 output (0)
						TOT2_0	-		Reload timer ch.2 output (0)
5	7	9	12	15	19	P032	-	A	General-purpose I/O port
						A04	-		External bus/Address bit4 output (0)
						SCS43_1	-		Serial chip select 43 output (1)
						PPG30_0	-		PPG ch.30 output (0)
						TOT3_0	-		Reload timer ch.3 output (0)
						RTO2_1	-		Waveform generator ch.2 output pin (1)
6	8	10	13	16	20	P033	-	A	General-purpose I/O port
						A05	-		External bus/Address bit5 output (0)
						PPG31_0	-		PPG ch.31 output (0)
						ICU3_3	-		Input capture ch.3 input (3)
						TIN4_0	-		Reload timer ch.4 event input (0)
						RTO1_1	-		Waveform generator ch.1 output pin (1)
						SCK3_2	-		Multi-function serial ch.3 clock I/O (2)

Pin no.						Pin Name	Polarity	I/O circuit types*1	Function*2
64	80	100	120	144	176				
7	9	11	14	17	21	P034	-	A	General-purpose I/O port
						A06	-		External bus/Address bit6 output (0)
						OCU11_1	-		Output compare ch.11 output (1)
						ICU2_3	-		Input capture ch.2 input (3)
						TIN5_0	-		Reload timer ch.5 event input (0)
						RTO0_1	-		Waveform generator ch.0 output pin (1)
						SOT3_2	-		Multi-function serial ch.3 serial data output (2)
-	-	12	15	18	22	P150	-	F	General-purpose I/O port
						SOT8_0/ SDA8	-		Multi-function serial ch.8 serial data output (0)/ I^2C bus serial data I/O
						OCU10_1	-		Output compare ch.10 output (1)
						TRG6_0	-		PPG trigger 6 input (0)
						ICU1_3	-		Input capture ch.1 input (3)
						TIN6_0	-		Reload timer ch.6 event input (0)
8	10	13	16	19	23	P151	-	F	General-purpose I/O port
						SCK8_0/ SCL8	-		Multi-function serial ch.8 clock I/O (0)/ I^2C bus serial clock I/O
						OCU9_1	-		Output compare ch.9 output (1)
						TRG7_0	-		PPG trigger 7 input (0)
						ICU0_3	-		Input capture ch.0 input (3)
						TIN7_0	-		Reload timer ch.7 event input (0)
						ZIN0_2	-		U/D counter ch.0 ZIN input (2)
						DTTI_1	-		Waveform generator ch.1 input pin (1)
9	11	14	17	20	24	P035	-	I	General-purpose I/O port
						A07	-		External bus/Address bit7 output
						SIN8_0	-		Multi-function serial ch.8 serial data input (0)
						OCU8_1	-		Output compare ch.8 output (1)
						TOT4_0	-		Reload timer ch.4 output (0)
						AIN0_0	-		U/D counter ch.0 AIN input (0)
						INT11_0	-		INT11 External interrupt input (0)
10	12	15	18	21	25	P036	-	A	General-purpose I/O port
						A08	-		External bus/Address bit8 output (0)
						SCS8_0	-		Serial chip select 8 I/O (0)
						OCU7_1	-		Output compare ch.7 output (1)
						TOT5_0	-		Reload timer ch.5 output (0)
						BIN0_0	-		U/D counter ch.0 BIN input (0)
-	-	16	19	22	26	P037	-	A	General-purpose I/O port
						A09	-		External bus/Address bit9 output (0)
						OCU6_1	-		Output compare ch.6 output (1)
						TOT6_0	-		Reload timer ch.6 output (0)
						ZIN0_0	-		U/D counter ch.0 ZIN input (0)
-	-	-	-	-	27	P174	-	A	General-purpose I/O port
						TRG8_1	-		PPG trigger 8 input (1)
-	-	-	-	-	28	P175	-	A	General-purpose I/O port
						TRG9_1	-		PPG trigger 9 input (1)

Pin no.						Pin Name	Polarity	I/O circuit types*1	Function*2
64	80	100	120	144	176				
11	13	17	20	23	29	P040	-	A	General-purpose I/O port
						A10	-		External bus/Address bit10 output (0)
						PPG23_1	-		PPG ch.23 output (1)
						TOT7_0	-		Reload timer ch.7 output (0)
						AIN1_0	-		U/D counter ch.1 AIN input (0)
						SIN0_1	-		Multi-function serial ch.0 serial data input (1)
12	14	18	21	24	30	P041	-	I	General-purpose I/O port
						A11	-		External bus/Address bit11 output (0)
						SIN9_0	-		Multi-function serial ch.9 serial data input (0)
						ICU9_1	-		Input capture ch.9 input (1)
						BIN1_0	-		U/D counter ch.1 BIN input (0)
						INT12_0	-		INT12 External interrupt input (0)
13	15	19	22	25	31	P042	-	B	General-purpose I/O port
						A12	-		External bus/Address bit12 output
						SOT9_0	-		Multi-function serial ch.9 serial data output (0)
						AN47	-		ADC analog 47 input
						ICU8_1	-		Input capture ch.8 input (1)
						TRG0_1	-		PPG trigger 0 input (1)
						ZIN1_0	-		U/D counter ch.1 ZIN input (0)
-	-	20	23	26	32	P043	-	A	General-purpose I/O port
						A13	-		External bus/Address bit13 output (0)
						ICU7_1	-		Input capture ch.7 input (1)
						TRG1_1	-		PPG trigger 1 input (1)
-	16	21	24	27	33	P044	-	A	General-purpose I/O port
						A14	-		External bus/Address bit14 output (0)
						SCS9_0	-		Serial chip select 9 I/O (0)
						ICU6_1	-		Input capture ch.6 input (1)
						TRG2_1	-		PPG trigger 2 input (1)
14	17	22	25	28	34	P045	-	G	General-purpose I/O port
						A15	-		External bus/Address bit15 output (0)
						SCK9_0	-		Multi-function serial ch.9 clock I/O (0)
						AN46	-		ADC analog 46 input
						ICU5_1	-		Input capture ch.5 input (1)
						TRG3_1	-		PPG trigger 3 input (1)
						TOT1_2	-		Reload timer ch.1 output (2)
-	-	-	26	29	35	P046	-	A	General-purpose I/O port
						A16	-		External bus/Address bit16 output (0)
						ICU4_1	-		Input capture ch.4 input (1)
						TRG4_1	-		PPG trigger 4 input (1)
-	-	-	-	-	36	P176	-	A	General-purpose I/O port
						TRG10_0	-		PPG trigger 10 input (0)

Pin no.						Pin Name	Polarity	I/O circuit types*1	Function*2
64	80	100	120	144	176				
15	18	23	27	30	37	P047	-	B	General-purpose I/O port
						A17	-		External bus/Address bit17 output (0)
						AN45	-		ADC analog 45 input
						TRG8_0	-		PPG trigger 8 input (0)
						TIN3_2	-		Reload timer ch.3 event input (2)
						SOT0_1	-		Multi-function serial ch.0 serial data output (1)
-	-	-	-	-	38	P177	-	A	General-purpose I/O port
						TRG11_0	-		PPG trigger 11 input (0)
-	-	-	28	31	39	P050	-	A	General-purpose I/O port
						A18	-		External bus/Address bit18 output
						TRG5_1	-		PPG trigger 5 input (1)
						PPG33_0	-		PPG ch.33 output (0)
-	-	-	-	32	40	P051	-	A	General-purpose I/O port
						A19	-		External bus/Address bit19 output
						TRG9_0	-		PPG trigger 9 input (0)
-	-	-	-	33	41	P052	-	A	General-purpose I/O port
						A20	-		External bus/Address bit20 output
						PPG34_0	-		PPG ch.34 output (0)
						INT14_0	-		INT14 External interrupt input (0)
16	19	24	29	34	42	P053	-	B	General-purpose I/O port
						A21	-		External bus/Address bit21 output
						AN44	-		ADC analog 44 input
						PPG35_0	-		PPG ch.35 output (0)
						INT14_1	-		INT14 External interrupt input (1)
						SCK0_1	-		Multi-function serial ch.0 clock I/O (1)
-	-	-	-	35	43	P054	-	A	General-purpose I/O port
						SYSCLK	-		External bus/System clock output
						PPG36_0	-		PPG ch.36 output (0)
17	22	27	32	38	46	P055	-	G	General-purpose I/O port
						CS2X	-		External bus chip select 2 output (0)
						SIN10_0	-		Multi-function serial ch.10 serial data input (0)
						AN43	-		ADC analog 43 input
						PPG37_0	-		PPG ch.37 output (0)
						TIN4_1	-		Reload timer ch.4 event input (1)
-	-	-	-	-	47	P180	-	A	General-purpose I/O port
						PPG40_0	-		PPG ch.40 output (0)
-	-	-	-	-	48	P181	-	A	General-purpose I/O port
						PPG41_0	-		PPG ch.41 output (0)
-	-	-	33	39	49	P056	-	A	General-purpose I/O port
						CS3X	-		External bus chip select 3 output (0)
						ICU9_0	-		Input capture ch.9 input (0)
						PPG0_1	-		PPG ch.0 output (1)
						ICU0_1	-		Input capture ch.0 input (1)
						TIN5_1	-		Reload timer ch.5 event input (1)
						DTTI_2	-		Waveform generator ch.0-ch.5 input pin (2)

Pin no.						Pin Name	Polarity	I/O circuit types*1	Function*2
64	80	100	120	144	176				
19	24	29	35	41	51	P057	-	G	General-purpose I/O port
						RDY	-		External bus/Ready input (0)
						SCK10_1	-		Multi-function serial ch.10 clock I/O (1)
						AN42	-		ADC analog 42 input
						ICU8_0	-		Input capture ch.8 input (0)
						TRG0_2	-		PPG trigger 0 input (2)
						PPG1_1	-		PPG ch.1 output (1)
						ICU1_1	-		Input capture ch.1 input (1)
						TIN6_1	-		Reload timer ch.6 event input (1)
-	-	-	-	44	54	P142	-	F	General-purpose I/O port
						SCK10_0/ SCL10	-		Multi-function serial ch.10 clock I/O (0)/ I^2C bus serial clock I/O
						PPG38_0	-		PPG ch.38 output (0)
						TIN7_1	-		Reload timer ch.7 event input (1)
-	-	-	-	45	55	P143	-	F	General-purpose I/O port
						SOT10_0/ SDA10	-		Multi-function serial ch.10 serial data output (0)/ I^2C bus serial data I/O
						PPG39_0	-		PPG ch.39 output (0)
						TOT4_1	-		Reload timer ch.4 output (1)
-	-	-	-	-	56	P182	-	A	General-purpose I/O port
						PPG42_0	-		PPG ch.42 output (0)
-	-	32	38	46	57	P060	-	A	General-purpose I/O port
						SCS10_0	-		Serial chip select 10 I/O (0)
						PPG2_1	-		PPG ch.2 output (1)
						ICU2_1	-		Input capture ch.2 input (1)
						TOT5_1	-		Reload timer ch.5 output (1)
						INT13_0	-		INT13 External interrupt input (0)
22	27	33	39	47	58	P061	-	B	General-purpose I/O port
						SOT10_1	-		Multi-function serial ch.10 serial data output (1)
						AN41	-		ADC analog 41 input
						ICU6_0	-		Input capture ch.6 input (0)
						PPG3_1	-		PPG ch.3 output (1)
						ICU3_1	-		Input capture ch.3 input (1)
						TOT6_1	-		Reload timer ch.6 output (1)
						INT13_1	-		INT13 External interrupt input (1)
23	28	34	40	48	59	P062	-	B	General-purpose I/O port
						SCS10_1	-		Serial chip select 10 I/O (1)
						SCS40_0	-		Serial chip select 40 I/O (0)
						AN40	-		ADC analog 40 input
						PPG4_1	-		PPG ch.4 output (1)
						FRCK0_0	-		Free-run timer 0 clock input (0)
						TOT7_1	-		Reload timer ch.7 output (1)
						ZIN1_1	-		U/D counter ch.1 ZIN input (1)

Pin no.						Pin Name	Polarity	I/O circuit types*1	Function*2
64	80	100	120	144	176				
-	29	35	41	49	60	P063	-	B	General-purpose I/O port
						SCS41_0	-		Serial chip select 41 output (0)
						AN39	-		ADC analog 39 input
						PPG5_1	-		PPG ch.5 output (1)
						FRCK1_0	-		Free-run timer 1 clock input (0)
						BIN1_1	-		U/D counter ch.1 BIN input (1)
-	-	-	-	-	61	P183	-	A	General-purpose I/O port
						PPG43_0	-		PPG ch.43 output (0)
24	30	36	42	50	62	P064	-	B	General-purpose I/O port
						SCS42_0	-		Serial chip select 42 output (0)
						AN38	-		ADC analog 38 input
						FRCK2_0	-		Free-run timer 2 clock input (0)
						AIN1_1	-		U/D counter ch.1 AIN input (1)
						PPG43_1	-		PPG ch.43 output (1)
-	-	37	43	51	63	P065	-	A	General-purpose I/O port
						SCS43_0	-		Serial chip select 43 output (0)
						FRCK3_0	-		Free-run timer 3 clock input (0)
						ZIN0_1	-		U/D counter ch.0 ZIN input (1)
						PPG44_1	-		PPG ch.44 output (1)
-	-	-	-	-	64	P184	-	A	General-purpose I/O port
						PPG44_0	-		PPG ch.44 output (0)
-	-	-	-	-	65	P185	-	A	General-purpose I/O port
						PPG45_0	-		PPG ch.45 output (0)
25	31	38	44	52	66	P066	-	B	General-purpose I/O port
						SOT4_2	-		Multi-function serial ch.4 serial data output (2)
						SCS3_0	-		Serial chip select 3 I/O (0)
						AN37	-		ADC analog 37 input
						FRCK4_0	-		Free-run timer 4 clock input (0)
						BIN0_1	-		U/D counter ch.0 BIN input (1)
-	32	39	45	53	67	P067	-	B	General-purpose I/O port
						AN36	-		ADC analog 36 input
						FRCK5_0	-		Free-run timer 5 clock input (0)
						AIN0_1	-		U/D counter ch.0 AIN input (1)
-	-	40	46	54	68	P070	-	A	General-purpose I/O port
						ICU0_2	-		Input capture ch.0 input (2)
26	33	41	47	55	69	P071	-	G	General-purpose I/O port
						SCK4_2	-		Multi-function serial ch.4 clock I/O (2)
						AN35	-		ADC analog 35 input
						ICU1_2	-		Input capture ch.1 input (2)
						MONCLK	-		Clock monitor output pin

Pin no.						Pin Name	Polarity	I/O circuit types*1	Function*2
64	80	100	120	144	176				
27	34	42	48	56	70	P072	-	G	General-purpose I/O port
						SIN4_0	-		Multi-function serial ch.4 serial data input (0)
						AN34	-		ADC analog 34 input
						ICU2_2	-		Input capture ch.2 input (2)
						INT5_0	-		INT5 External interrupt input (0)
-	35	43	49	57	71	P073	-	D	General-purpose I/O port
						SOT4_0/ SDA4	-		Multi-function serial ch.4 serial data output (0)/I^2C bus serial data I/O
						AN33	-		ADC analog 33 input
						ICU3_2	-		Input capture ch.3 input (2)
-	-	-	-	-	72	P186	-	A	General-purpose I/O port
						PPG46_0	-		PPG ch.46 output (0)
-	-	-	-	-	73	P187	-	A	General-purpose I/O port
						PPG47_0	-		PPG ch.47 output (0)
-	-	-	50	58	74	P074	-	E	General-purpose I/O port
						SCK4_0/ SCL4	-		Multi-function serial ch.4 clock I/O (0)/ I^2C bus serial clock I/O
-	-	-	51	59	75	P075	-	F	General-purpose I/O port
						SIN3_0	-		Multi-function serial ch.3 serial data input (0)
						INT4_0	-		INT4 External interrupt input (0)
-	-	-	52	60	76	P076	-	E	General-purpose I/O port
						SOT3_0/ SDA3	-		Multi-function serial ch.3 serial data output (0)/I^2C bus serial data I/O
-	-	-	53	61	77	P077	-	E	General-purpose I/O port
						SCK3_0/ SCL3	-		Multi-function serial ch.3 clock I/O (0)/ I^2C bus serial clock I/O
-	-	44	54	62	78	P152	-	A	General-purpose I/O port
						SCS53_0	-		Serial chip select 53 output (0)
28	36	45	55	63	79	P153	-	G	General-purpose I/O port
						SCK5_0/ SCL5	-		Multi-function serial ch.5 clock I/O (0)/ I^2C bus serial clock I/O
						AN32	-		ADC analog 32 input
						FRCK1_1	-		Free-run timer 1 clock input (1)
						INT4_1	-		INT4 External interrupt input (1)
-	-	-	-	64	80	P080	-	A	General-purpose I/O port
						SCS52_0	-		Serial chip select 52 output (0)
						PPG0_0	-		PPG ch.0 output (0)
29	37	46	56	65	81	P081	-	G	General-purpose I/O port
						SOT5_0/ SDA5	-		Multi-function serial ch.5 serial data output (0)/I^2C bus serial data I/O
						AN0	-		ADC analog 0 input
						PPG1_0	-		PPG ch.1 output (0)
30	38	47	57	66	82	P082	-	G	General-purpose I/O port
						SIN5_0	-		Multi-function serial ch.5 serial data input (0)
						AN1	-		ADC analog 1 input
						PPG2_0	-		PPG ch.2 output (0)

Pin no.						Pin Name	Polarity	I/O circuit types*1	Function*2
64	80	100	120	144	176				
-	-	-	-	67	83	P083	-	B	General-purpose I/O port
						SCS50_0	-		Serial chip select 50 I/O (0)
						AN2	-		ADC analog 2 input
						PPG3_0	-		PPG ch.3 output (0)
-	-	-	-	68	84	P084	-	B	General-purpose I/O port
						SCS51_0	-		Serial chip select 51 output (0)
						AN3	-		ADC analog 3 input
						PPG4_0	-		PPG ch.4 output (0)
-	-	-	-	69	85	P085	-	A	General-purpose I/O port
						PPG5_0	-		PPG ch.5 output (0)
-	-	48	58	70	86	P086	-	C	General-purpose I/O port
						DAO1	-		DAC analog 1 output
						PPG6_0	-		PPG ch.6 output (0)
31	39	49	59	71	87	P087	-	C	General-purpose I/O port
						DAO0	-		DAC analog 0 output
						PPG7_0	-		PPG ch.7 output (0)
						INT8_0	-		INT8 External interrupt input (0)
-	-	-	-	-	90	P190	-	A	General-purpose I/O port
						TIN0_1	-		Reload timer ch.0 event input (1)
-	-	-	-	-	91	P191	-	A	General-purpose I/O port
						TIN1_1	-		Reload timer ch.1 event input (1)
-	-	-	-	74	92	P090	-	B	General-purpose I/O port
						AN4	-		ADC analog 4 input
						ICU0_0	-		Input capture ch.0 input (0)
						TIN2_1	-		Reload timer ch.2 event input (1)
-	-	-	-	75	93	P091	-	B	General-purpose I/O port
						AN5	-		ADC analog 5 input
						PPG41_1	-		PPG ch.41 output (1)
						ICU1_0	-		Input capture ch.1 input (0)
						TIN3_1	-		Reload timer ch.3 event input (1)
-	-	-	-	76	94	P092	-	B	General-purpose I/O port
						AN6	-		ADC analog 6 input
						PPG40_1	-		PPG ch.40 output (1)
						ICU2_0	-		Input capture ch.2 input (0)
						TOT0_1	-		Reload timer ch.0 output (1)
-	-	-	-	-	95	P192	-	A	General-purpose I/O port
						PPG24_1	-		PPG ch.24 output (1)
						TOT1_1	-		Reload timer ch.1 output (1)
34	42	52	62	77	96	P093	-	J	General-purpose I/O port
						TX0_1	-		CAN transmission data 0 output (1)
						SIN11_0	-		Multi-function serial ch.11 serial data input (0)
						AN7	-		ADC analog 7 input
						ICU4_2	-		Input capture ch.4 input (2)
						PPG16_1	-		PPG ch.16 output (1)
						ICU3_0	-		Input capture ch.3 input (0)
						TOT2_1	-		Reload timer ch.2 output (1)

Pin no.						Pin Name	Polarity	I/O circuit types*1	Function*2
64	80	100	120	144	176				
-	-	-	-	78	97	P094	-	B	General-purpose I/O port
						AN8	-		ADC analog 8 input
						ICU4_0	-		Input capture ch.4 input (0)
						TOT3_1	-		Reload timer ch.3 output (1)
-	-	53	63	79	98	P095	-	B	General-purpose I/O port
						TX0(128)	-		CAN transmission data 0 output
						SCS11_0	-		Serial chip select 11 I/O (0)
						AN9	-		ADC analog 9 input
35	43	54	64	80	99	P096	-	G	General-purpose I/O port
						RX0(128)	-		CAN reception data 0 input
						SOT11_0/ SDA11	-		Multi-function serial ch.11 serial data output (0)/I2C bus serial data I/O
						AN10	-		ADC analog 10 input
						INT0_0	-		INT0 External interrupt input (0)
36	44	55	65	81	100	P097	-	G	General-purpose I/O port
						SCK11_0/ SCL11	-		Multi-function serial ch.11 clock I/O (0)/ I2C bus serial clock I/O
						AN11	-		ADC analog 11 input
						ICU5_0	-		Input capture ch.5 input (0)
						PPG17_1	-		PPG ch.17 output (1)
-	48	59	69	85	104	P100	-	G	General-purpose I/O port
						SCK7_0/ SCL7	-		Multi-function serial ch.7 clock I/O (0)/ I2C bus serial clock I/O
						AN12	-		ADC analog 12 input
						PPG8_0	-		PPG ch.8 output (0)
-	-	60	70	86	105	P101	-	G	General-purpose I/O port
						SOT7_0/ SDA7	-		Multi-function serial ch.7 serial data output (0)/I2C bus serial data I/O
						AN13	-		ADC analog 13 input
						PPG9_0	-		PPG ch.9 output (0)
40	49	61	71	87	106	P102	-	G	General-purpose I/O port
						SIN7_0	-		Multi-function serial ch.7 serial data input (0)
						AN14	-		ADC analog 14 input
						PPG10_0	-		PPG ch.10 output (0)
						INT10_0	-		INT10 External interrupt input (0)
41	50	62	72	88	107	P103	-	H	General-purpose I/O port
						SCS73_0	-		Serial chip select 73 output (0)
						AN15	-		ADC analog 15 input
						PPG11_0	-		PPG ch.11 output (0)
42	51	63	73	89	108	P104	-	H	General-purpose I/O port
						SCS72_0	-		Serial chip select 72 output (0)
						AN16	-		ADC analog 16 input
						PPG12_0	-		PPG ch.12 output (0)
43	52	64	74	90	109	P105	-	H	General-purpose I/O port
						SCS71_0	-		Serial chip select 71 output (0)
						AN17	-		ADC analog 17 input
						PPG13_0	-		PPG ch.13 output (0)

Pin no.						Pin Name	Polarity	I/O circuit types*1	Function*2
64	80	100	120	144	176				
-	-	65	75	91	110	P106	-	H	General-purpose I/O port
						SCS70_0	-		Serial chip select 70 I/O (0)
						AN18	-		ADC analog 18 input
						PPG14_0	-		PPG ch.14 output (0)
-	53	66	76	92	111	P107	-	B	General-purpose I/O port
						AN19	-		ADC analog 19 input
						PPG15_0	-		PPG ch.15 output (0)
-	-	-	-	-	112	P193	-	A	General-purpose I/O port
						PPG25_1	-		PPG ch.25 output (1)
-	-	-	77	93	113	P154	-	B	General-purpose I/O port
						AN20	-		ADC analog 20 input
-	-	-	78	94	114	P155	-	B	General-purpose I/O port
						AN21	-		ADC analog 21 input
44	54	67	79	95	115	NMIX	N	M	Non-masking interrupt input
45	55	68	80	96	116	P110	-	B	General-purpose I/O port
						TX1(64)	-		CAN transmission data 1 output
						SCS63_0	-		Serial chip select 63 output (0)
						AN22	-		ADC analog 22 input
-	-	69	81	97	117	P111	-	G	General-purpose I/O port
						RX1(64)	-		CAN reception data 1 input
						SCS62_0	-		Serial chip select 62 output (0)
						AN23	-		ADC analog 23 input
						INT1_0	-		INT1 External interrupt input (0)
-	-	-	82	98	118	P112	-	B	General-purpose I/O port
						AN24	-		ADC analog 24 input
						PPG16_0	-		PPG ch.16 output (0)
						RTO0_0	-		Waveform generator ch. 0 output pin (0)
-	-	-	83	99	119	P113	-	B	General-purpose I/O port
						AN25	-		ADC analog 25 input
						PPG17_0	-		PPG ch.17 output (0)
						RTO1_0	-		Waveform generator ch. 1 output pin (0)
-	-	-	-	-	120	P194	-	A	General-purpose I/O port
						FRCK5_1	-		Free-run timer 5 clock input (1)
						PPG26_1	-		PPG ch.26 output (1)
-	-	-	-	-	121	P195	-	A	General-purpose I/O port
						FRCK4_1	-		Free-run timer 4 clock input (1)
						PPG27_1	-		PPG ch.27 output (1)
-	56	70	84	100	122	P114	-	B	General-purpose I/O port
						SCS61_0	-		Serial chip select 61 output (0)
						AN26	-		ADC analog 26 input
						PPG18_0	-		PPG ch.18 output (0)
						RTO2_0	-		Waveform generator ch.2 output pin (0)

Pin no.						Pin Name	Polarity	I/O circuit types*1	Function*2
64	80	100	120	144	176				
46	57	71	85	101	123	P115	-	G	General-purpose I/O port
						RX1_1	-		CAN reception data 1 input (1)
						SOT6_0/ SDA6	-		Multi-function serial ch.6 serial data output (0)/I2C bus serial data I/O
						AN27	-		ADC analog 27 input
						PPG19_0	-		PPG ch.19 output (0)
						RTO3_0	-		Waveform generator ch.3 output pin (0)
						INT1_1	-		INT1 External interrupt input (1)
47	58	72	86	102	124	P116	-	G	General-purpose I/O port
						SCK6_0/ SCL6	-		Multi-function serial ch.6 clock I/O (0)/ I2C bus serial clock I/O
						AN28	-		ADC analog 28 input
						PPG20_0	-		PPG ch.20 output (0)
						RTO4_0	-		Waveform generator ch.4 output pin (0)
-	-	73	87	103	125	P117	-	B	General-purpose I/O port
						SCS60_0	-		Serial chip select 60 I/O (0)
						AN29	-		ADC analog 29 input
						PPG21_0	-		PPG ch.21 output (0)
						RTO5_0	-		Waveform generator ch.5 output pin (0)
-	-	-	-	-	126	P196	-	A	General-purpose I/O port
						FRCK3_1	-		Free-run timer 3 clock input (1)
						PPG28_1	-		PPG ch.28 output (1)
-	-	-	88	104	127	P120	-	B	General-purpose I/O port
						AN30	-		ADC analog 30 input
						OCU6_0	-		Output compare ch.6 output (0)
						PPG22_0	-		PPG ch.22 output (0)
						INT9_0	-		INT9 External interrupt input (0)
-	-	-	-	105	128	P121	-	A	General-purpose I/O port
						OCU7_0	-		Output compare ch.7 output (0)
						PPG23_0	-		PPG ch.23 output (0)
48	59	74	89	106	129	P122	-	J	General-purpose I/O port
						SIN6_0	-		Multi-function serial ch.6 serial data input (0)
						AN31	-		ADC analog 31 input
						OCU8_0	-		Output compare ch.8 output (0)
						INT9_1	-		INT9 External interrupt input (1)
-	-	-	-	-	130	P197	-	A	General-purpose I/O port
						PPG29_1	-		PPG ch.29 output (1)
-	-	-	-	107	131	P123	-	A	General-purpose I/O port
						OCU9_0	-		Output compare ch.9 output (0)
49	62	77	92	110	134	DEBUGIF	-	L	MDI I/O for debugger (OCD)
-	-	-	-	-	135	P160	-	A	General-purpose I/O port
						PPG30_1	-		PPG ch.30 output (1)
-	-	-	-	-	136	P161	-	A	General-purpose I/O port
						PPG31_1	-		PPG ch.31 output (1)
-	-	-	-	111	137	P124	-	A	General-purpose I/O port
						OCU10_0	-		Output compare ch.10 output (0)

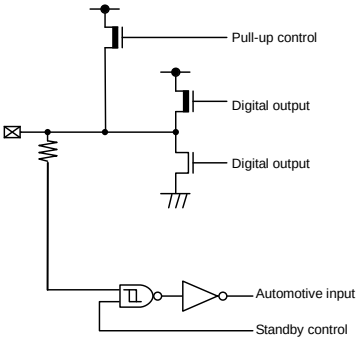
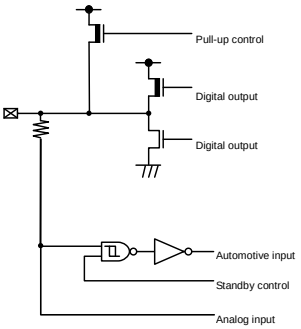
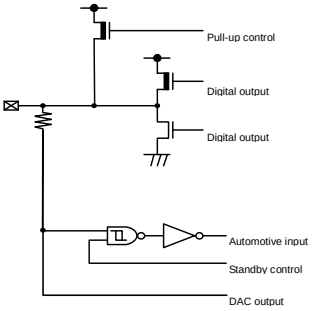
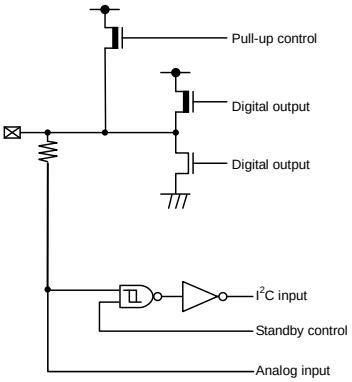
Pin no.						Pin Name	Polarity	I/O circuit types*1	Function*2
64	80	100	120	144	176				
-	-	-	93	112	138	P125	-	A	General-purpose I/O port
						OCU11_0	-		Output compare ch.11 output (0)
50	63	78	94	113	139	P126	-	F	General-purpose I/O port
						SIN0_0	-		Multi-function serial ch.0 serial data input (0)
						INT6_0	-		INT6 External interrupt input (0)
-	64	79	95	114	140	P127	-	A	General-purpose I/O port
						SOT0_0	-		Multi-function serial ch.0 serial data output (0)
-	-	80	96	115	141	P130	-	F	General-purpose I/O port
						SCK0_0	-		Multi-function serial ch.0 clock I/O (0)
-	-	-	-	-	142	P162	-	A	General-purpose I/O port
						TRG5_2	-		PPG trigger 5 input (2)
-	-	-	-	-	143	P163	-	A	General-purpose I/O port
						TRG6_2	-		PPG trigger 6 input (2)
51	65	81	97	116	144	MD0	-	K	Mode pin 0
52	66	82	98	117	145	MD1	-	K	Mode pin 1
53	67	83	99	118	146	X0	-	N	Main clock oscillation input
54	68	84	100	119	147	X1	-	N	Main clock oscillation output
56	70	86	102	121	149	P135	-	A	General-purpose I/O port
						DTTI_0	-		Waveform generator ch.0-ch.5 input pin (0)
						X1A	-	O	Sub clock oscillation output
57	71	87	103	122	150	P136	-	A	General-purpose I/O port
						X0A	-	O	Sub clock oscillation input
58	72	88	104	123	151	RSTX	N	M	External reset input
-	-	-	-	124	152	P131	-	A	General-purpose I/O port
						ADTG0_0	-		A/D converter external trigger input 0 (0)
-	-	-	105	125	153	P132	-	A	General-purpose I/O port
						SCS1_0	-		Serial chip select 1 I/O (0)
						ADTG1_0	-		A/D converter external trigger input 1 (0)
-	-	89	106	126	154	P133	-	A	General-purpose I/O port
						TX2(64)	-		CAN transmission data 2 output
-	-	90	107	127	155	P134	-	F	General-purpose I/O port
						RX2(64)	-		CAN reception data 2 input
						SCS1_1	-		Serial chip select 1 I/O (1)
						ICU7_0	-		Input capture ch.7 input (0)
						INT7_0	-		INT7 External interrupt input (0)
-	-	91	108	128	156	P144	-	F	General-purpose I/O port
						SCK1_1	-		Multi-function serial ch.1 clock I/O (1)
-	-	94	111	131	159	P000	-	F	General-purpose I/O port
						D16	-		External bus data bit16 I/O (0)
						SIN1_0	-		Multi-function serial ch.1 serial data input (0)
						TIOA0_1	-		TIOA output of Base timer ch.0 (1)
						INT2_0	-		INT2 External interrupt input (0)
-	75	95	112	132	160	P001	-	A	General-purpose I/O port
						D17	-		External bus data bit17 I/O
						SOT1_0	-		Multi-function serial ch.1 serial data output (0)
						TIOA1_1	-		TIOA I/O of Base timer ch.1 (1)

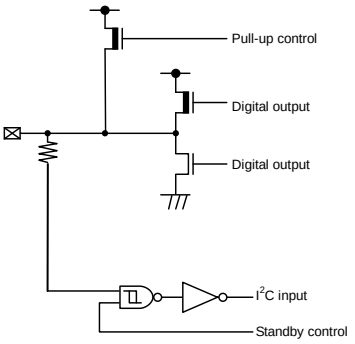
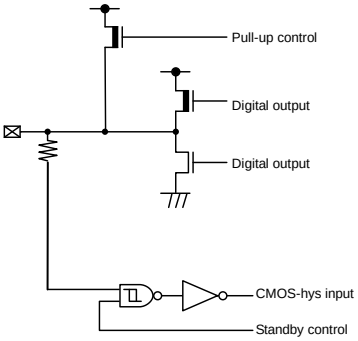
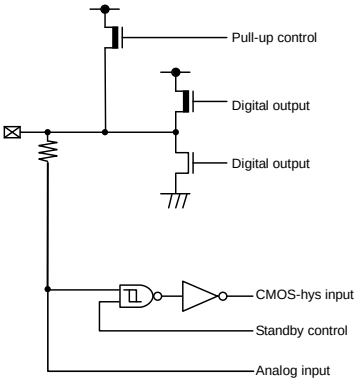
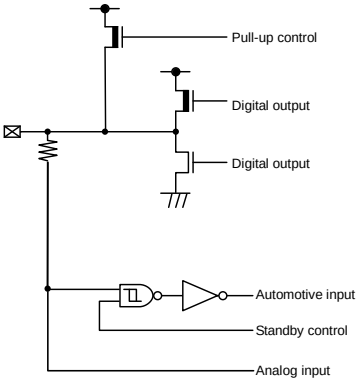
Pin no.						Pin Name	Polarity	I/O circuit types*1	Function*2
64	80	100	120	144	176				
-	-	-	113	133	161	P002	-	F	General-purpose I/O port
						D18	-		External bus data bit18 I/O
						SCK1_0	-		Multi-function serial ch.1 clock I/O (0)
						TIOB0_1	-		TIOB input of Base timer ch.0 (1)
-	76	96	114	134	162	P003	-	F	General-purpose I/O port
						D19	-		External bus data bit19 I/O
						SIN2_0	-		Multi-function serial ch.2 serial data input (0)
						TIOB1_1	-		TIOB input of Base timer ch.1 (1)
						INT3_0	-		INT3 External interrupt input (0)
-	-	-	-	135	163	P004	-	A	General-purpose I/O port
						D20	-		External bus data bit20 I/O (0)
						SOT2_0	-		Multi-function serial ch.2 serial data output (0)
-	-	-	-	-	164	P164	-	A	General-purpose I/O port
						PPG32_1	-		PPG ch.32 output (1)
61	77	97	115	136	165	P005	-	F	General-purpose I/O port
						D21	-		External bus data bit21 I/O (0)
						SCK2_0	-		Multi-function serial ch.2 clock I/O (0)
						ADTG0_1	-		A/D converter external trigger input 0 (1)
						INT7_1	-		INT7 External interrupt input (1)
						(RX2(64))	-		(CAN reception data 2 input MB91F52xB ,MB91F52xD only)
-	-	-	-	-	166	P165	-	A	General-purpose I/O port
						PPG33_1	-		PPG ch.33 output (1)
62	78	98	116	137	167	P006	-	A	General-purpose I/O port
						D22	-		External bus data bit22 I/O (0)
						SCS2_0	-		Serial chip select 2 I/O (0)
						ADTG1_1	-		A/D converter external trigger input 1 (1)
						INT2_1	-		INT2 External interrupt input (1)
						(TX2(64))	-		(CAN transmission data 2 output MB91F52xB ,MB91F52xD only)
-	-	-	117	138	168	P007	-	A	General-purpose I/O port
						D23	-		External bus data bit23 I/O
-	-	-	-	-	169	P166	-	A	General-purpose I/O port
						PPG34_1	-		PPG ch.34 output (1)
-	-	-	118	139	170	P010	-	A	General-purpose I/O port
						D24	-		External bus data bit24 I/O
63	79	99	119	140	171	P011	-	A	General-purpose I/O port
						WOT	-		RTC output signal
						D25	-		External bus data bit25 I/O
						SOT2_1	-		Multi-function serial ch.2 serial data output (1)
						TIOA0_0	-		TIOA output of Base timer ch.0 (0)
						INT3_1	-		INT3 External interrupt input (1)
-	-	-	-	141	172	P012	-	A	General-purpose I/O port
						D26	-		External bus data bit26 I/O
						TIOB0_0	-		TIOB input of Base timer ch.0 (0)
-	-	-	-	-	173	P167	-	A	General-purpose I/O port
						PPG35_1	-		PPG ch.35 output (1)

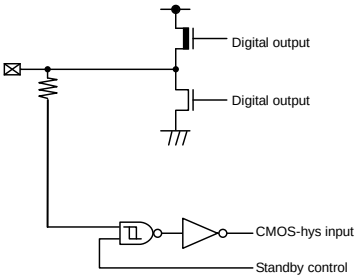
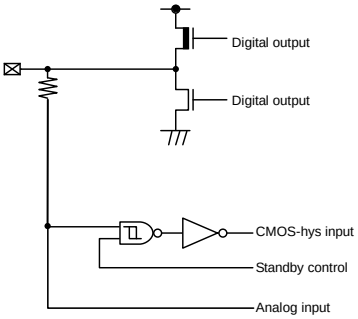
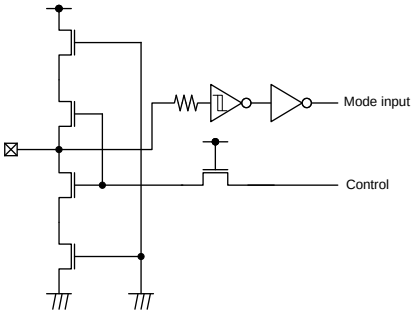
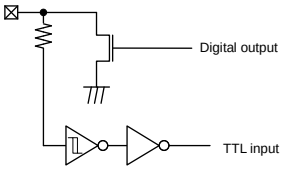
Pin no.						Pin Name	Polarity	I/O circuit types*1	Function*2
64	80	100	120	144	176				
-	-	-	-	142	174	P013	-	A	General-purpose I/O port
						D27	-		External bus data bit27 I/O
						TIOA1_0	-		TIOA I/O of Base timer ch.1 (0)
-	-	-	-	143	175	P014	-	A	General-purpose I/O port
						D28	-		External bus data bit28 I/O
						TIOB1_0	-		TIOB input of Base timer ch.1 (0)
18	23	28	34	40	50	AVCC1	-	-	Analog power supply for AD/DA convertor unit1
39	47	58	68	84	103	AVCC0	-	-	Analog power supply for AD/DA convertor unit0
20	25	30	36	42	52	AVRH1	-	-	Upper limit reference voltage for AD convertor unit1
38	46	57	67	83	102	AVRH0	-	-	Upper limit reference voltage for AD convertor unit0
21	26	31	37	43	53	AVSS1/ AVRL1	-	-	GND for AD/DA convertor unit1 Lower limit reference voltage for AD convertor unit1
37	45	56	66	82	101	AVSS0/ AVRL0	-	-	GND for AD/DA convertor unit0 Lower limit reference voltage for AD convertor unit0
60	74	93	110	130	158	C	-	-	External capacity connection output
-	20	25	30	36	44	VCC	-	-	+5.0V power supply
32	40	50	60	72	88				
-	61	76	91	109	133				
64	80	100	120	144	176				
1	1	1	1	1	1	VSS	-	-	GND
-	21	26	31	37	45				
33	41	51	61	73	89				
-	60	75	90	108	132				
55	69	85	101	120	148				
59	73	92	109	129	157				

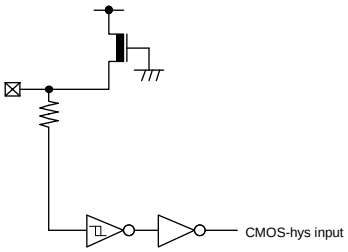
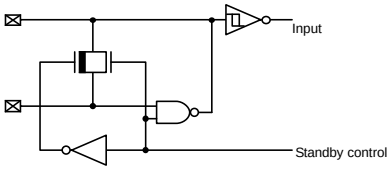
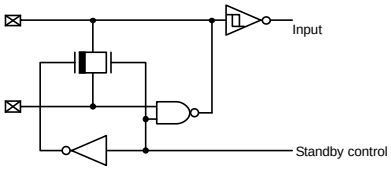
*1: For the I/O circuit types, see "■I/O CIRCUIT TYPE".
*2: For switching, see "I/O Port" in HARDWARE MANUAL.

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		•General-purpose I/O port •Output 4mA •Pull-up resistor control 50kΩ •Automotive input
B		•Analog input, General-purpose I/O port •Output 4mA •Pull-up resistor control 50kΩ •Automotive input
C		•DAC output, General-purpose I/O port •Output 4mA •Pull-up resistor control 50kΩ •Automotive input
D		•I²C Analog input, General-purpose I/O port •Output 3mA •Pull-up resistor control 50kΩ •I²C hysteresis input

Type	Circuit	Remarks
E		•I2C,General-purpose I/O port •Output 3mA •Pull-up resistor control 50kΩ •I2C hysteresis input
F		•General-purpose I/O port •Output 4mA •Pull-up resistor control 50kΩ •CMOS hysteresis input
G		•Analog input, General-purpose I/O port •Output 4mA •Pull-up resistor control 50kΩ • CMOS hysteresis input
H		•Analog input, General-purpose I/O port •Output 12mA •Pull-up resistor control 50kΩ •Automotive input

Type	Circuit	Remarks
I		•3V pad power supply (5V tolerant), General-purpose I/O port •Output 4mA • CMOS hysteresis input
J		•3V pad power supply (5V tolerant), Analog input,General-purpose I/O port •Output 4mA • CMOS hysteresis input
K		•Mode I/O • CMOS hysteresis input
L		•Open-drain I/O •Output 25mA (NOD) •TTL input

Type	Circuit	Remarks
M		• CMOS hysteresis input •Pull-up resistor 50kΩ (5V cont)
N		•Main oscillation I/O
O		•Sub oscillation I/O

■ HANDLING PRECAUTIONS

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Spansion semiconductor devices.

1. Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

- Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

- Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

- Processing and Protection of Pins

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

(1) Preventing Over-Voltage and Over-Current Conditions

Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.

(2) Protection of Output Pins

Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device.
Therefore, avoid this type of connection.

(3) Handling of Unused Input Pins

Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

- Latch-up

Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNPN junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

(1) Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.

(2) Be sure that abnormal current flows do not occur during the power-on sequence.

- Observance of Safety Regulations and Standards

  Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

- Fail-Safe Design

  Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

- Precautions Related to Usage of Devices

  Spansion semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

  CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

2. Precautions for Package Mounting

   Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Spansion's recommended conditions. For detailed information about mount conditions, contact your sales representative.

- Lead Insertion Type

  Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

  Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Spansion recommended mounting conditions.

  If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

- Surface Mount Type

  Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

  You must use appropriate mounting techniques. Spansion recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Spansion ranking of recommended conditions.

- Lead-Free Packaging

  CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

- Storage of Semiconductor Devices

  Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

  (1) Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.

  (2) Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5°C and 30°C.
  When you open Dry Package that recommends humidity 40% to 70% relative humidity.

  (3) When necessary, Spansion packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.

  (4) Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

- Baking

  Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Spansion recommended conditions for baking.

  Condition: 125°C/24 h

- Static Electricity

  Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

  (1) Maintain relative humidity in the working environment between 40% and 70%. Use of an apparatus for ion generation may be needed to remove electricity.

  (2) Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.

  (3) Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ).
  Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.

  (4) Ground all fixtures and instruments, or protect with anti-static measures.

  (5) Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

3. Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

(1) Humidity

Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.

(2) Discharge of Static Electricity

When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.

(3) Corrosive Gases, Dust, or Oil

Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.

(4) Radiation, Including Cosmic Radiation

Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.

(5) Smoke, Flame

CAUTION: Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Spansion products in other special environmental conditions should consult with sales representatives.

Please check the latest handling precautions at the following URL.
http://www.spansion.com/fjdocuments/fj/datasheet/e-ds/DS00-00004.pdf

■ HANDLING DEVICES

This section explains the latch-up prevention and pin processing.

• For latch-up prevention

If a voltage higher than VCC or a voltage lower than VSS is applied to an I/O pin, or if a voltage exceeding the ratings is applied between VCC and VSS pins, a latch-up may occur in CMOS IC. If the latch-up occurs, the power supply current increases excessively and device elements may be damaged by heat. Take care to prevent any voltage from exceeding the maximum ratings in device application.

Also, the analog power supply (AVCC, AVRH) and analog input must not be exceed the digital power supply (VCC) when the power supply to the analog system is turned on or off.

In the correct power-on sequence of the microcontroller, turn on the digital power supply (VCC) and analog power supplies (AVCC, AVRH) simultaneously. Or, turn on the digital power supply (VCC), and then turn on analog power supplies (AVCC, AVRH).

• Treatment of unused pins

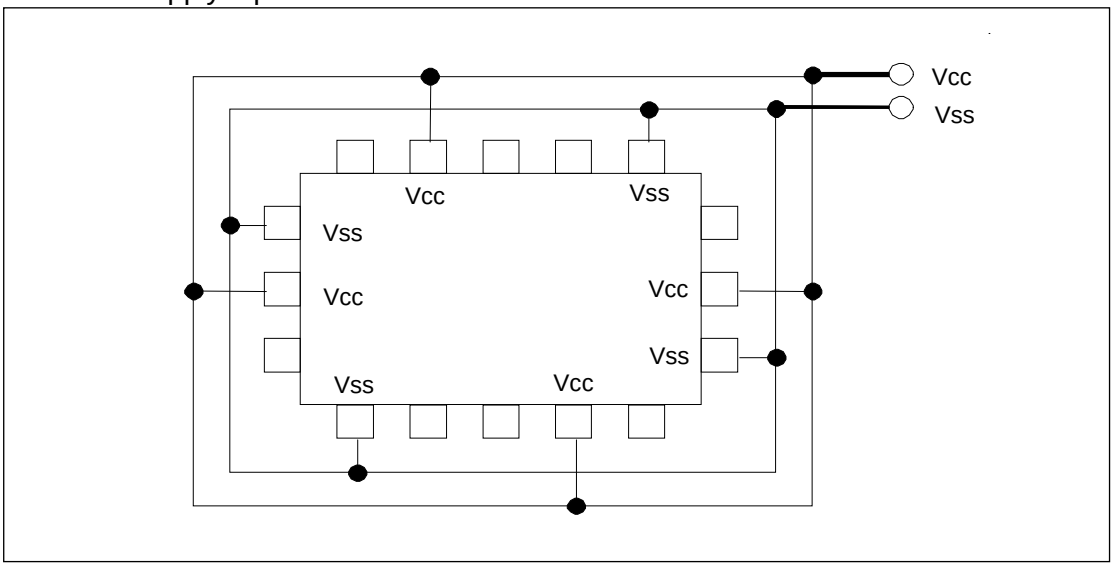
If unused input pins are left open, they may cause a permanent damage to the device due to malfunction or latch-up. Connect at least a 2kΩ resistor to each of the unused pins for pull-up or pull-down processing.

Also, if I/O pins are not used, they must be set to the output state for releasing or they must be set to the input state and treated in the same way as for the input pins.

• Power supply pins

The device is designed to ensure that if the device contains multiple VCC or VSS pins, the pins that should be at the same potential are interconnected to prevent latch-up or other malfunctions. Further, connect these pins to an external power supply or ground to reduce unwanted radiation, prevent strobe signals from malfunctioning due to a raised ground level, and fulfill the total output current standard, etc. As shown in figure 1, all Vss power supply pins must be treated in the similar way. If multiple Vcc or Vss systems are connected, the device cannot operate correctly even within the guaranteed operating range.

Figure 1 Power Supply Input Pins



The power supply pins should be connected to VCC and VSS pins of this device at the low impedance from the power supply source.

In the area close to this device, a ceramic capacitor having the capacitance larger than the capacitor of C pin is recommended to use as a bypass capacitor between VCC and VSS pins.

- **Crystal oscillation circuit**

  An external noise to the X0 or X1 pin may cause a device malfunction. The printed circuit board must be designed to lay out X0 and X1 pins, crystal oscillator (or ceramic resonator), and the bypass capacitor to be grounded to the close position to the device.

  The printed circuit board artwork is recommended to surround the X0 and X1 pins by ground circuits.

- **Mode pins (MD1, MD0)**

  Connect the MD1and MD0 mode pins to the VCC or VSS pin directly. To prevent an erroneous selection of test mode caused by the noise, reduce the pattern length between each mode pin and VCC or VSS pin on the printed circuit board. Also, use the low-impedance pin connection.

- **During power-on**

  To prevent a malfunction of the voltage step-down circuit built in the device, set the voltage rising time to have 50µs or longer (between 0.2V and 2.7V) during power-on.

- **Notes during PLL clock operation**

  When the PLL clock is selected and if the oscillator is disconnected or if the input is stopped, this clock may continue to operate at the free running frequency of the self-oscillator circuit built in the PLL clock. This operation is not guaranteed.

- **Treatment of A/D converter power supply pins**

  Connect the pins to have AVCC=AVRH=VCC and AVSS/AVRL=VSS even if the A/D converter is not used.

- **Notes on using external clock**

  An external clock is not supported. None of the external direct clock input can be used for both main clock and sub clock.

- **Power-on sequence of A/D converter analog inputs**

  Be sure to turn on the digital power supply (Vcc) first, and then turn on the A/D converter power supplies (AVcc, AVRH, AVRL) and analog inputs (AN0 to AN47). Also, turn off the A/D converter power supplies and analog inputs first, and then turn off the digital power supply (Vcc). When the AVRH pin voltage is turned on or off, it must not exceed AVCC. Even if a common analog input pin is used as an input port, its input voltage must not exceed AVcc. (However, the analog power supply and digital power supply can be turned on or off simultaneously.)

- **Treatment of C pin**

  This device contains a voltage step-down circuit. A capacitor must always be connected to the C pin to assure the internal stabilization of the device. For the standard values, see the "Recommended Operating Conditions" of the latest data sheet.

  Note: Please see the latest data sheet for a detailed specification of the operation voltage.

- **Function switching of a multiplexed port**

  To switch between the port function and the multiplexed pin function, use the PFR (port function register). However, if a pin is also used for an external bus, its function is switched by the external bus setting. For details, see " I/O PORTS" in the hardware manual.

- **Low-power consumption mode**

  To transit to the sleep mode, watch mode, stop mode, watch mode(power-off) or stop mode(power-off), follow the procedure explained in "Activating the sleep mode, watch mode, or stop mode" or "Activating the watch mode (power-off) or stop mode(power-off)" of " POWER CONSUMPTION CONTROL" in the hardware manual.

  Take the following notes when using a monitor debugger.

  - Do not set a break point for the low-power consumption transition program.
  - Do not execute an operation step for the low-power consumption transition program.

- **Notes When Writing Data in a Register Having the Status Flag**

  When writing data in the register that has a status flag (especially, an interrupt request flag) to control function, taking care not to clear its status flag erroneously must be followed.

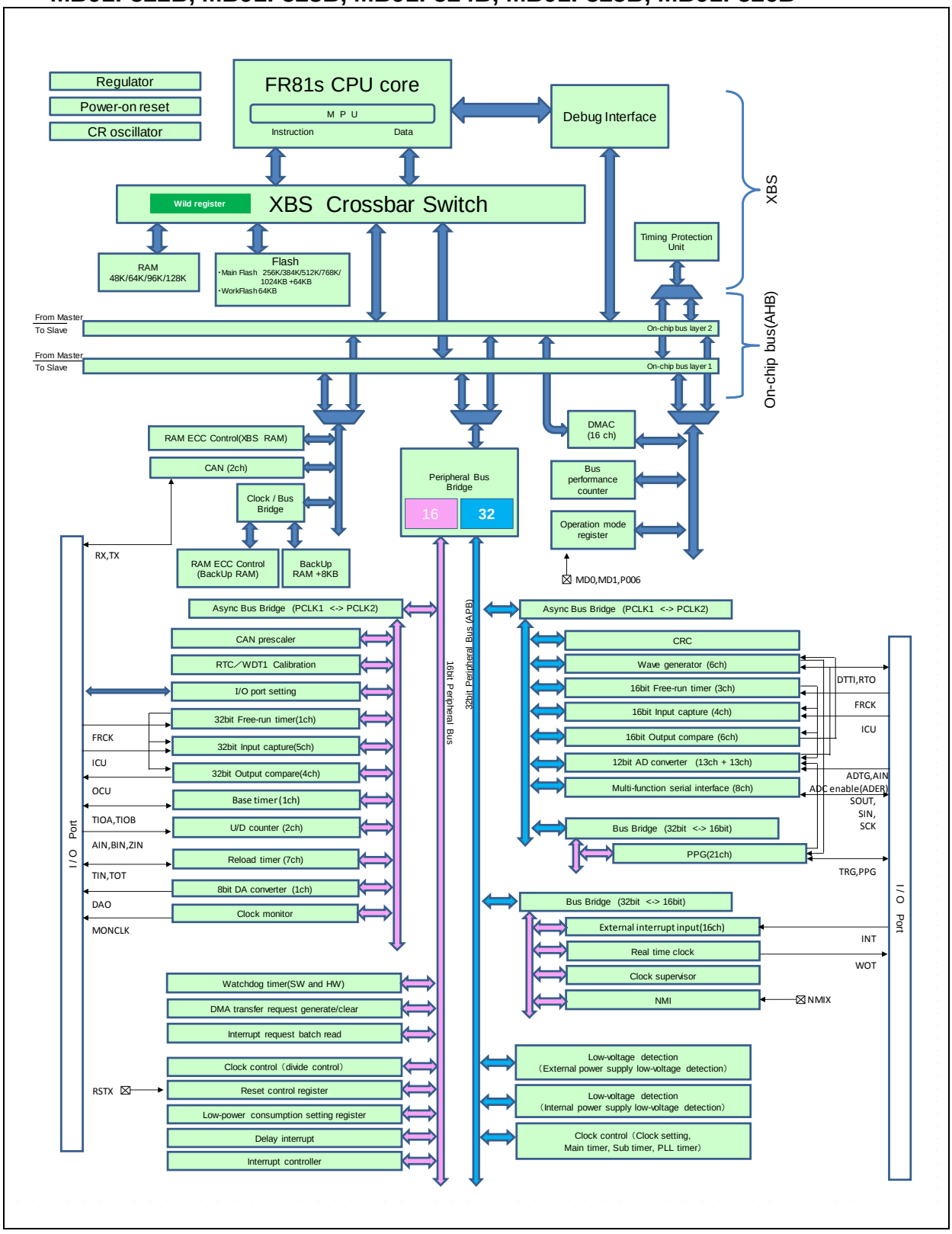
  The program must be written not to clear the flag to the status bit, and then to set the control bits to have the desired value.

  Especially, if multiple control bits are used, the bit instruction cannot be used. (The bit instruction can access to a single bit only.) By the Byte, Half-word, or Word access, data is written to the control bits and status flag simultaneously. During this time, take care not to clear other bits (in this case, the bits of status flag) erroneously.

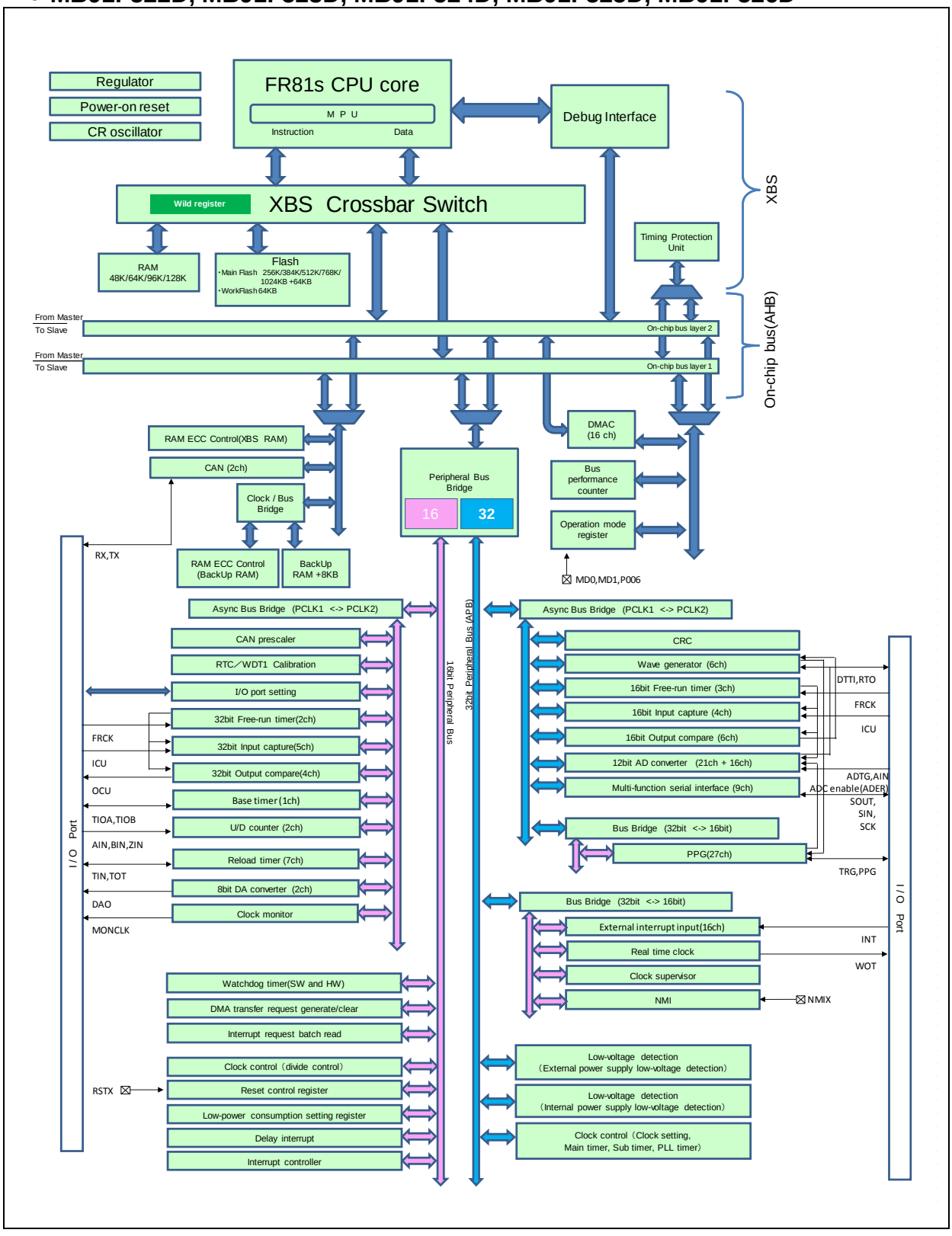
  Note: These points can be ignored because the bit instructions are already taken the points into consideration.

■ BLOCK DIAGRAM

● MB91F522B, MB91F523B, MB91F524B, MB91F525B, MB91F526B



● MB91F522D, MB91F523D, MB91F524D, MB91F525D, MB91F526D



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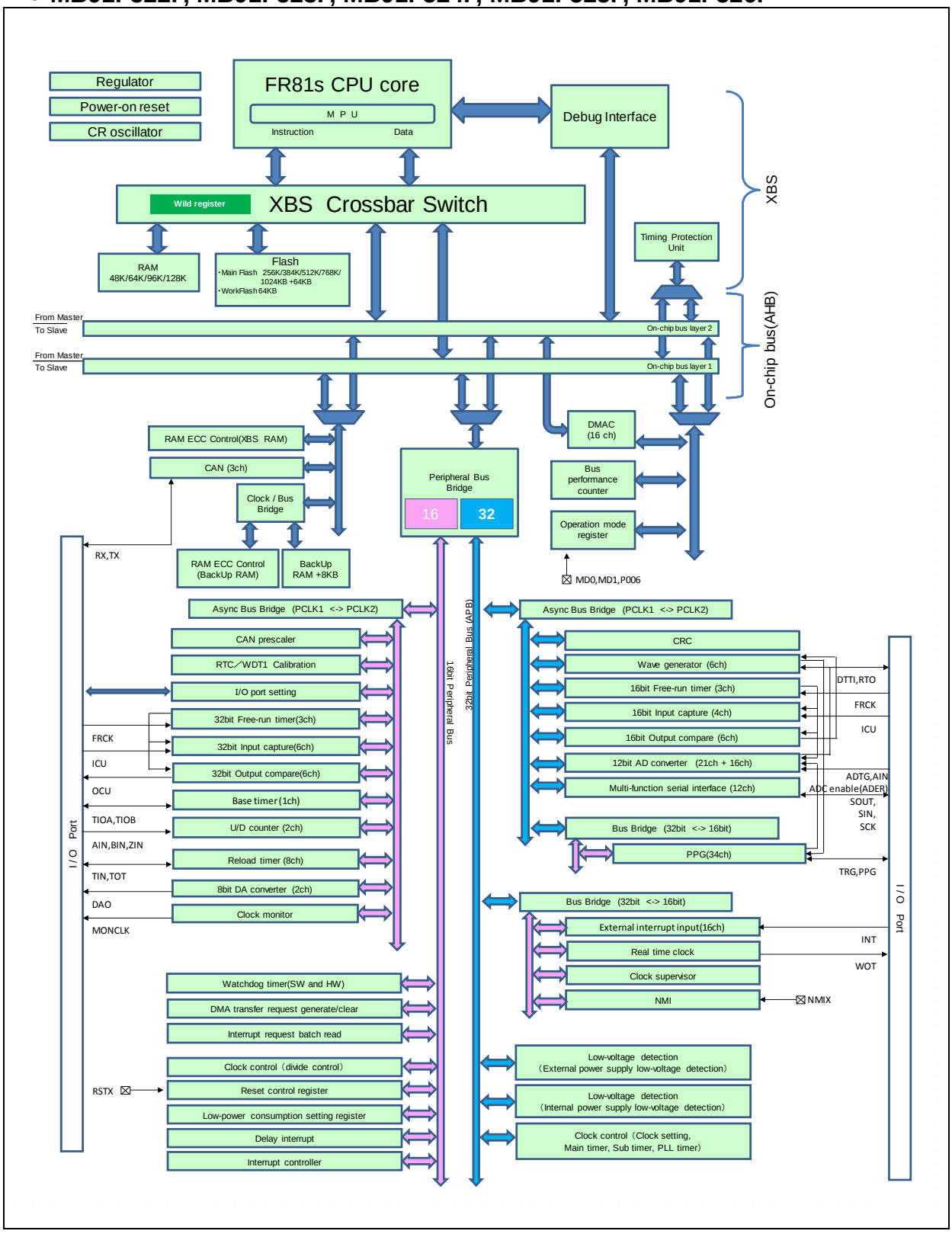
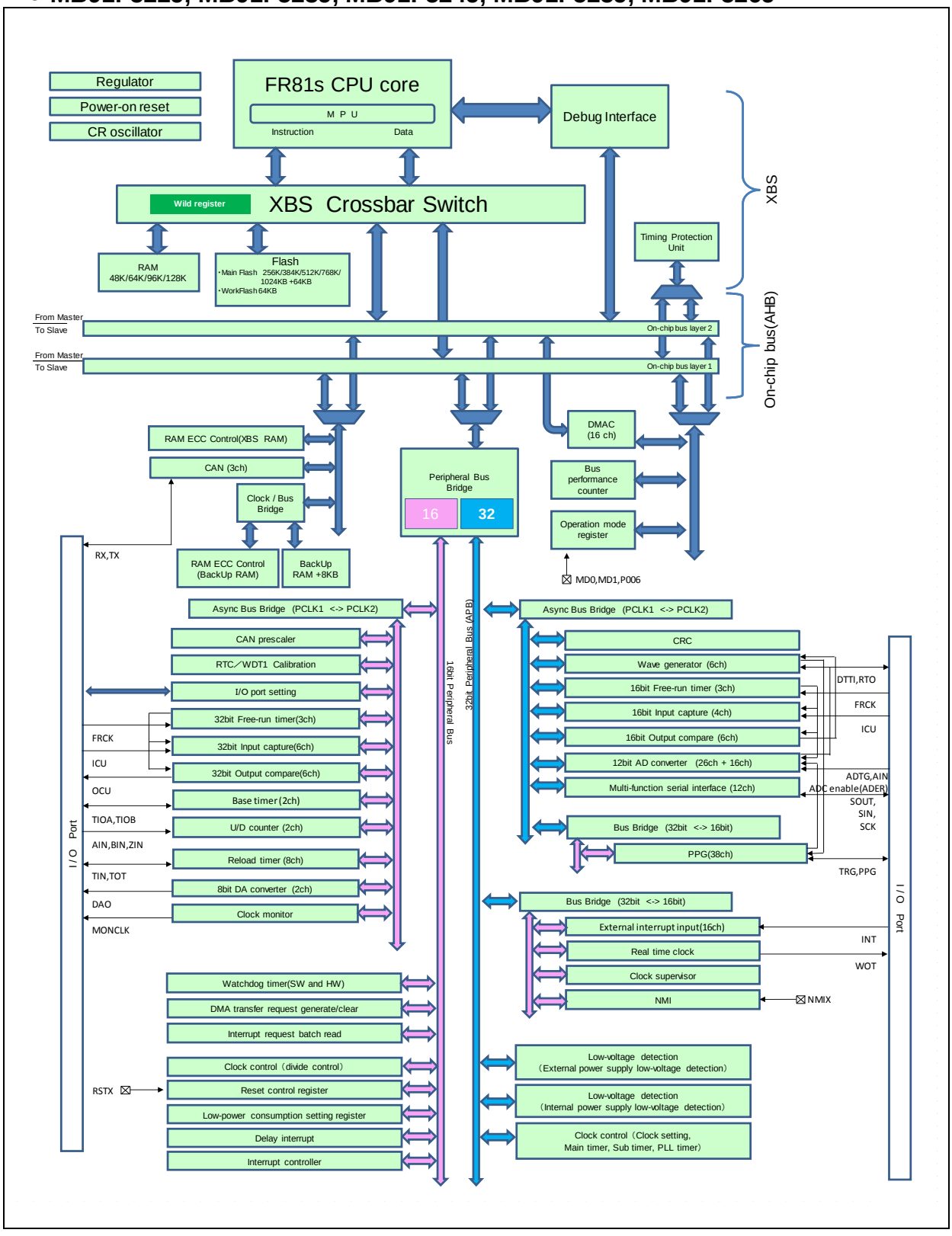
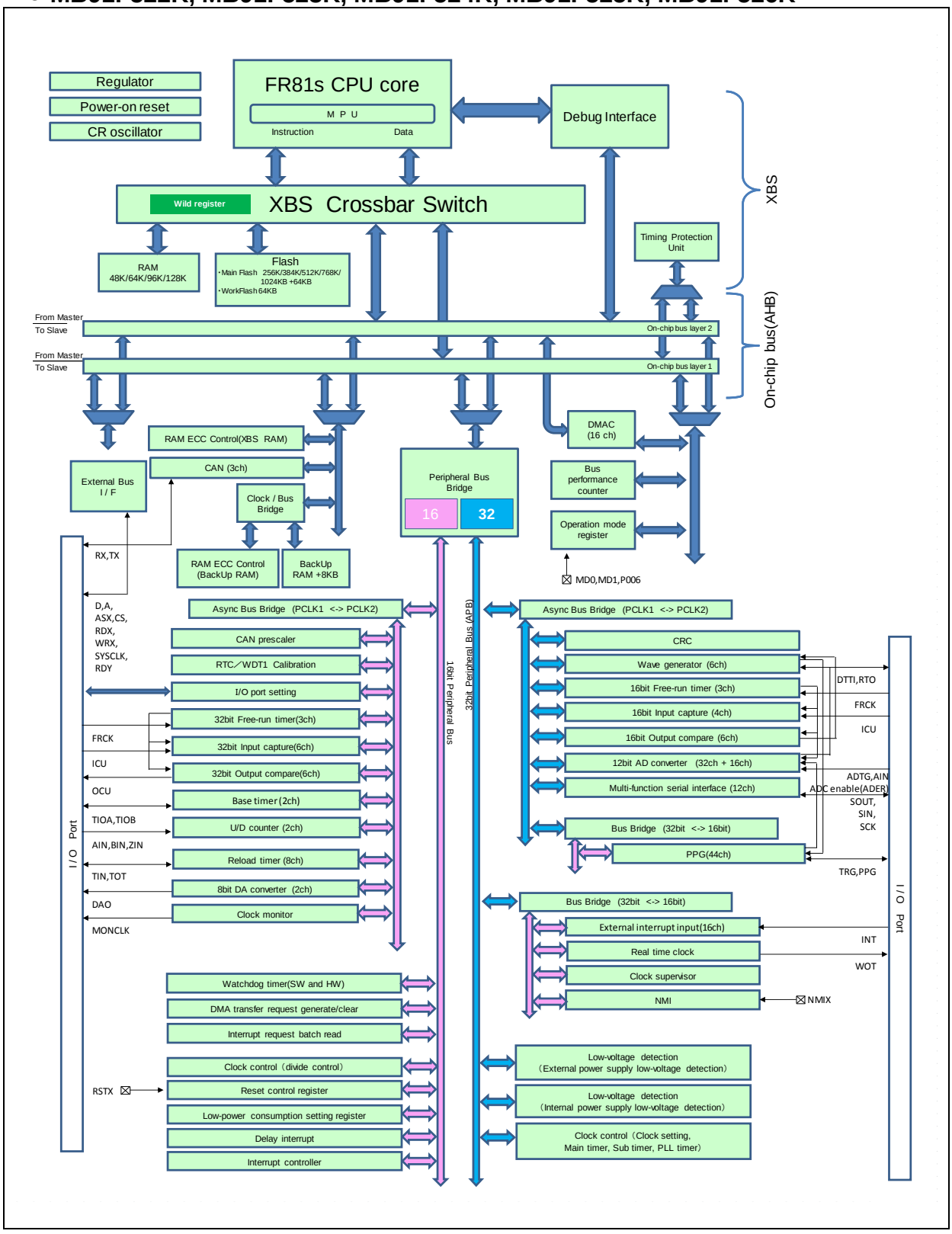


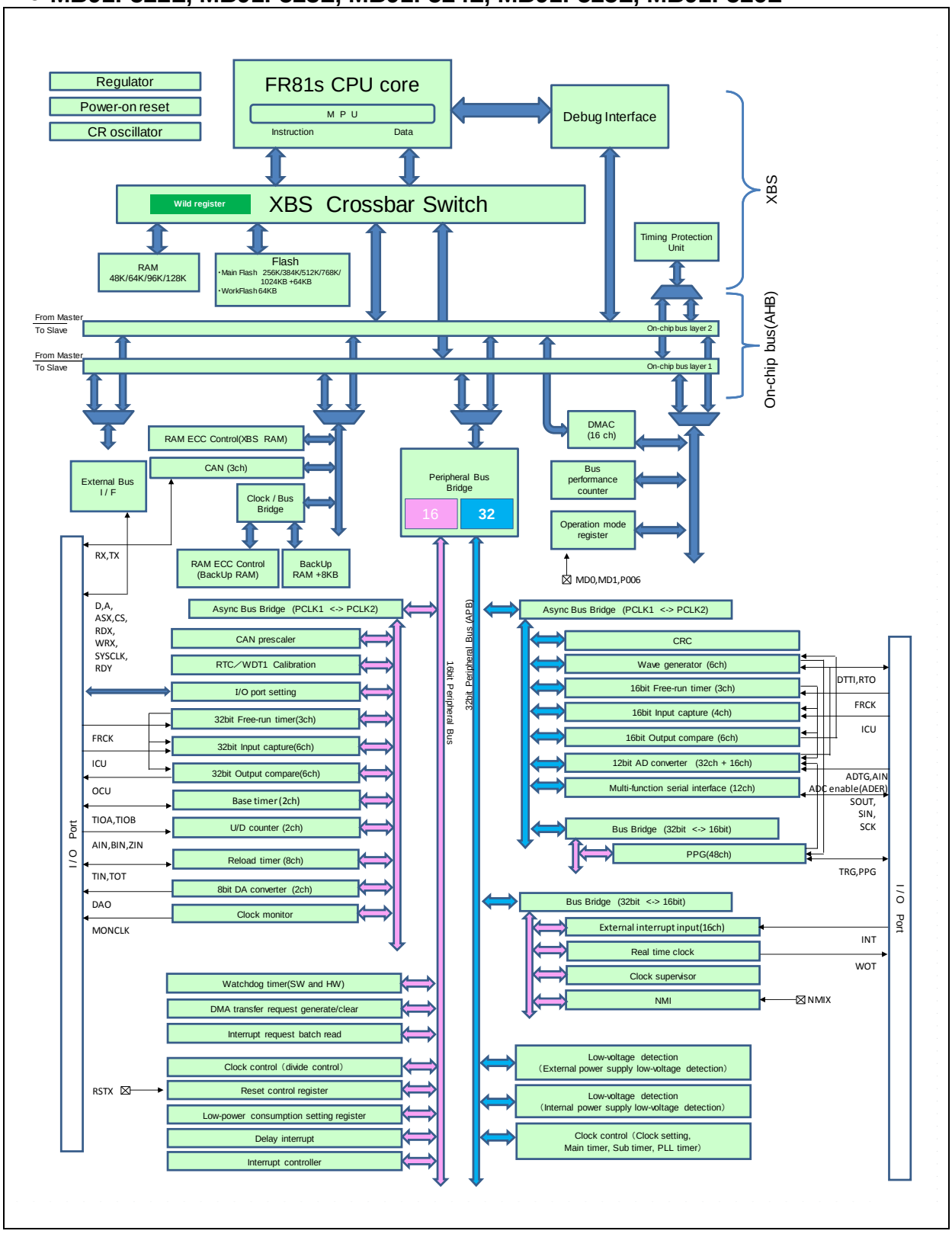
● MB91F522J, MB91F523J, MB91F524J, MB91F525J, MB91F526J



● MB91F522K, MB91F523K, MB91F524K, MB91F525K, MB91F526K

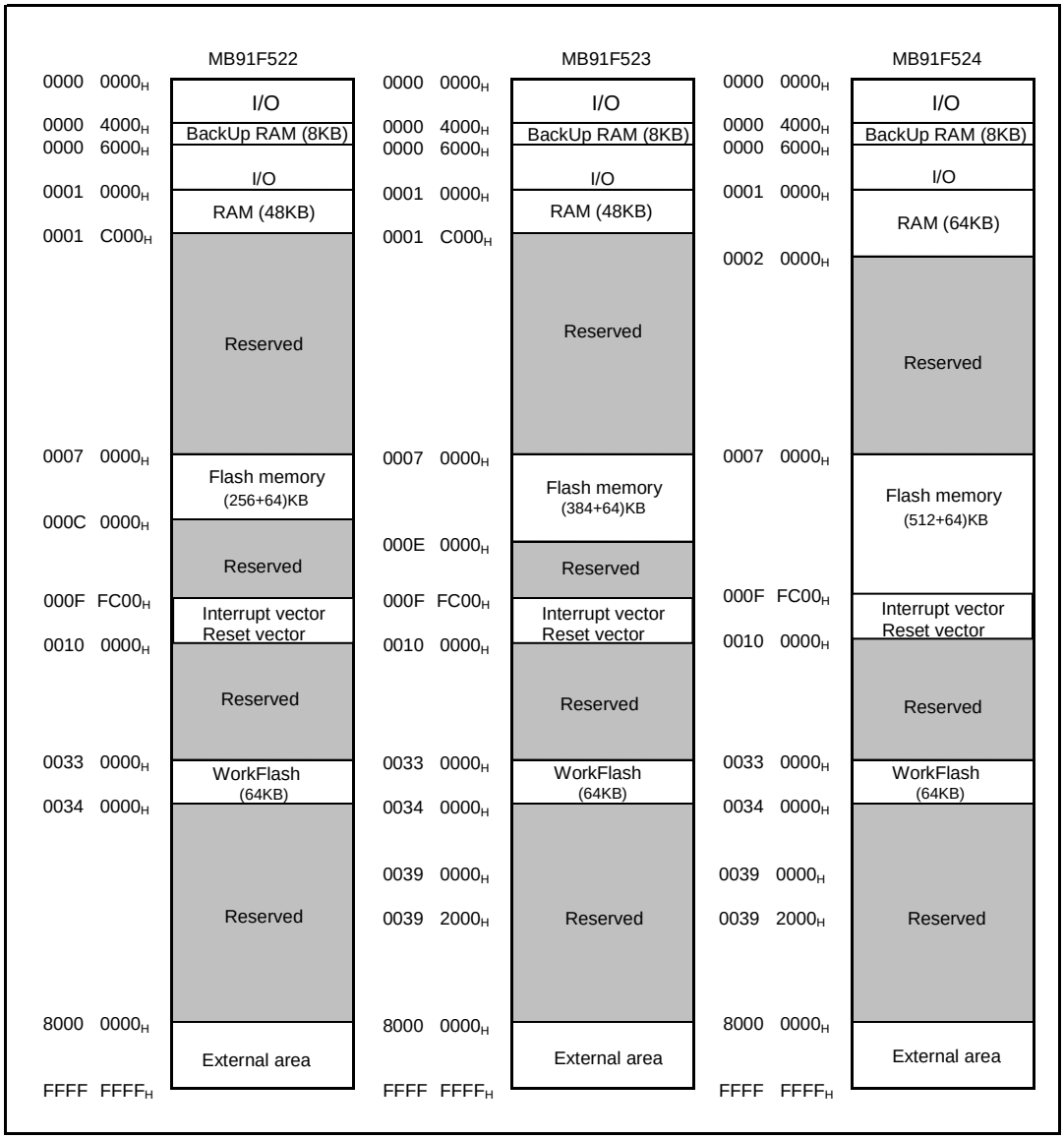


● MB91F522L, MB91F523L, MB91F524L, MB91F525L, MB91F526L

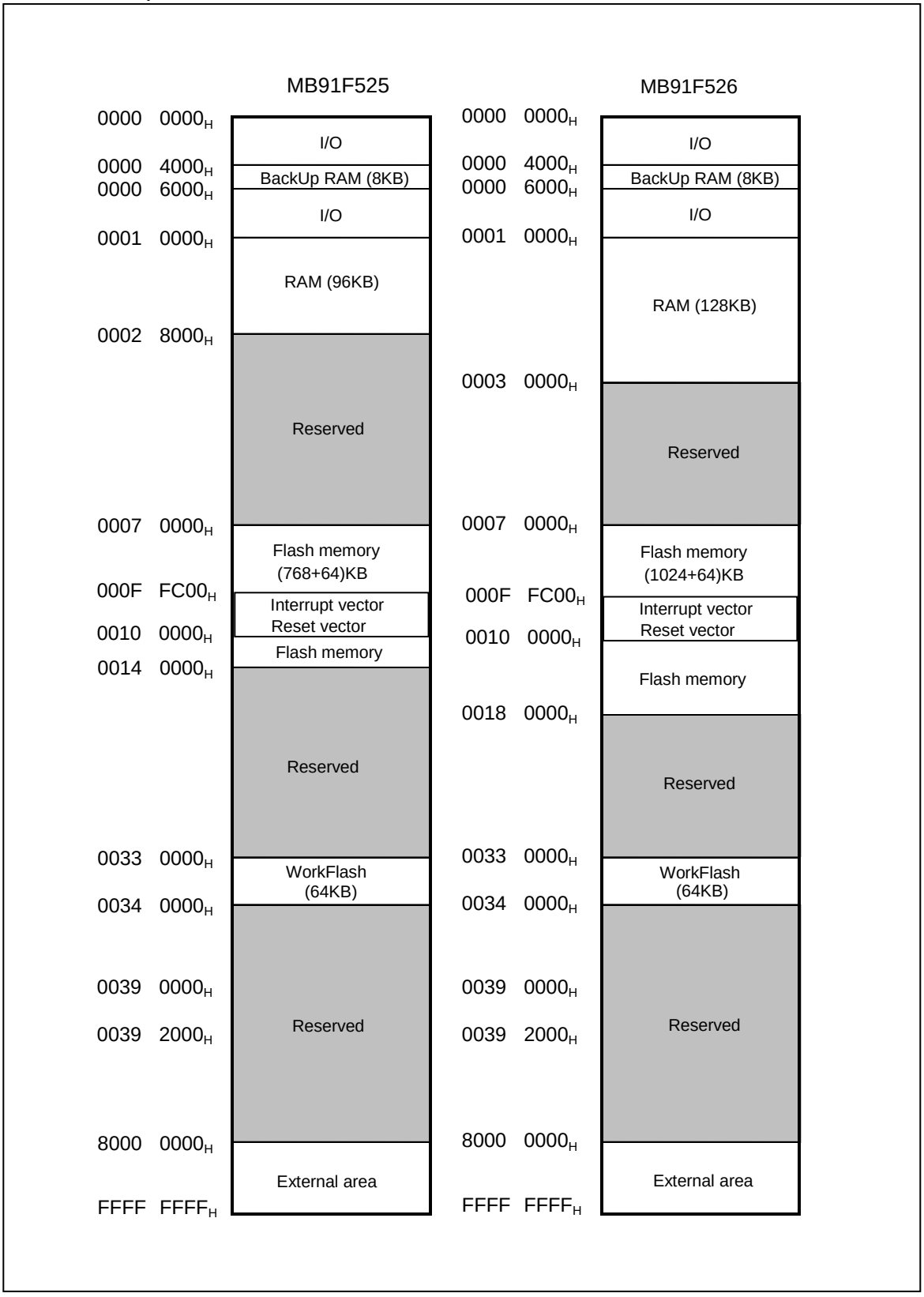


■ MEMORY MAP

● MB91F522, MB91F523, MB91F524



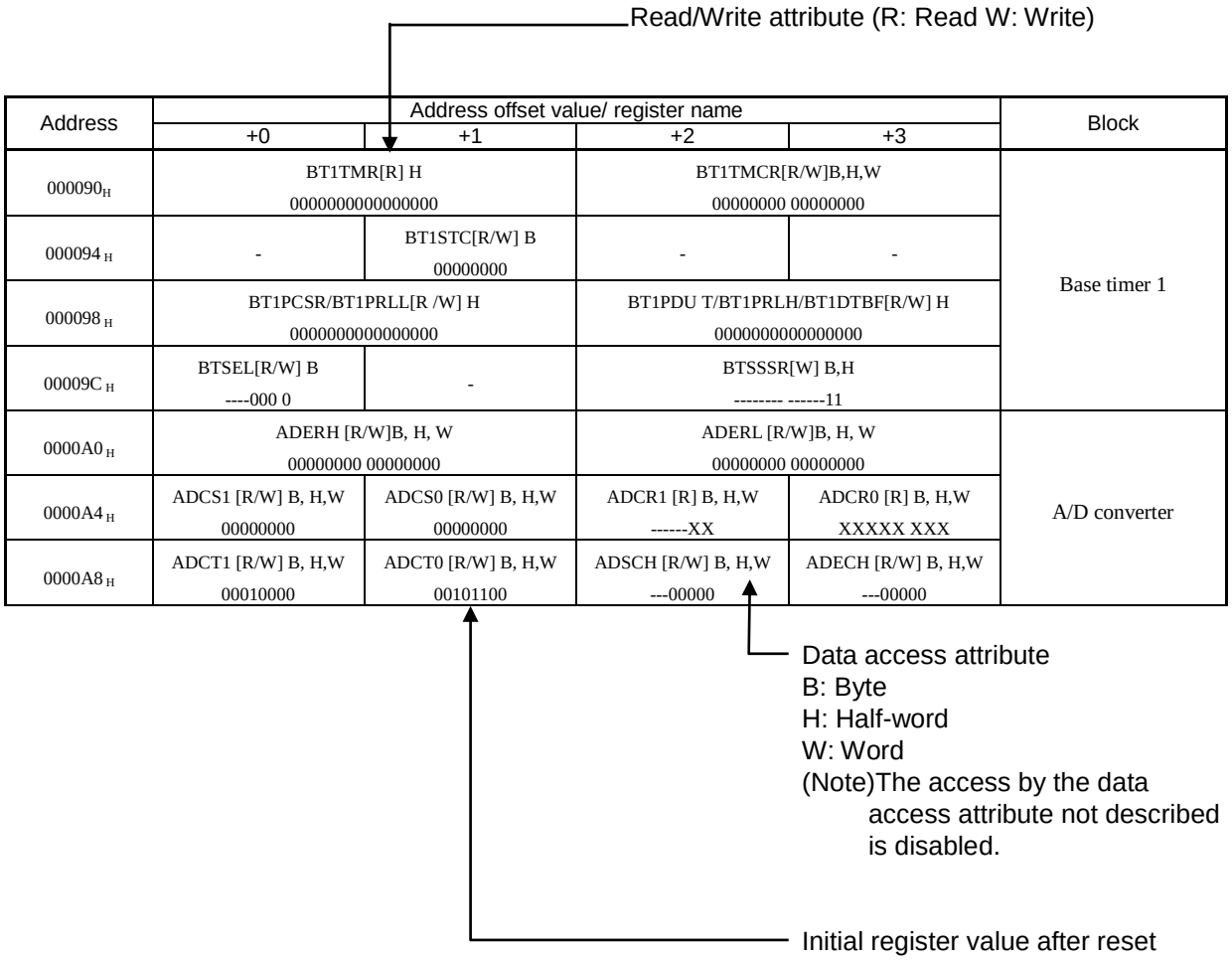
● MB91F525, MB91F526



■ I/O MAP

The following I/O map shows the relationship between memory space and registers for peripheral resources.

Legend of I/O Map



Address	Address offset value/ register name				Block
	+0	+1	+2	+3	
000090$_H$	BT1TMR[R] H 0000000000000000		BT1TMCR[R/W]B,H,W 00000000 00000000		Base timer 1
000094$_H$	-	BT1STC[R/W] B 00000000	-	-	
000098$_H$	BT1PCSR/BT1PRLL[R /W] H 0000000000000000		BT1PDU T/BT1PRLH/BT1DTBF[R/W] H 0000000000000000		
00009C$_H$	BTSEL[R/W] B ----000 0	-	BTSSSR[W] B,H -------- ------11		
0000A0$_H$	ADERH [R/W]B, H, W 00000000 00000000		ADERL [R/W]B, H, W 00000000 00000000		A/D converter
0000A4$_H$	ADCS1 [R/W] B, H,W 00000000	ADCS0 [R/W] B, H,W 00000000	ADCR1 [R] B, H,W ------XX	ADCR0 [R] B, H,W XXXXX XXX	
0000A8$_H$	ADCT1 [R/W] B, H,W 00010000	ADCT0 [R/W] B, H,W 00101100	ADSCH [R/W] B, H,W ---00000	ADECH [R/W] B, H,W ---00000	

The initial register value after reset indicates as follows:

- "1": Initial value "1"
- "0": Initial value "0"
- "X": Initial value undefined
- "-": Reserved bit/Undefined bit
- "*": Initial value "0" or "1" according to the setting

Note: The access to addresses not described is disabled.

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000000_H	PDR00 [R/W] B,H,W XXXXXXXX	PDR01 [R/W] B,H,W XXXXXXXX	PDR02 [R/W] B,H,W XXXXXXXX	PDR03 [R/W] B,H,W XXXXXXXX	Port Data Register
000004_H	PDR04 [R/W] B,H,W XXXXXXXX	PDR05 [R/W] B,H,W XXXXXXXX	PDR06 [R/W] B,H,W XXXXXXXX	PDR07 [R/W] B,H,W XXXXXXXX	
000008_H	PDR08 [R/W] B,H,W XXXXXXXX	PDR09 [R/W] B,H,W XXXXXXXX	PDR10 [R/W] B,H,W XXXXXXXX	PDR11 [R/W] B,H,W XXXXXXXX	
$00000C_H$	PDR12 [R/W] B,H,W XXXXXXXX	PDR13 [R/W] B,H,W -XXXXXXX	PDR14 [R/W] B,H,W ---XXX--	PDR15 [R/W] B,H,W --XXXXXX	
000010_H	—	—	—	—	
000014_H	—	—	—	—	
000018_H	PDR16 [R/W] B,H,W XXXXXXXX	PDR17 [R/W] B,H,W XXXXXXXX	PDR18 [R/W] B,H,W XXXXXXXX	PDR19 [R/W] B,H,W XXXXXXXX	
$00001C_H$ to 000034_H	—	—	—	—	Reserved
000038_H	WDTECR0 [R/W] B,H,W ---00000	—	—	—	Watchdog Timer [S]
$00003C_H$	WDTCR0 [R/W] B,H,W -0--0000	WDTCPR0 [W] B,H,W 00000000	WDTCR1 [R] B,H,W ----0110	WDTCPR1 [W] B,H,W 00000000	
000040_H	—	—	—	—	Reserved
000044_H	DICR [R/W] B,H,W -------0	—	—	—	Delayed Interrupt
000048_H to $00005C_H$	—	—	—	—	Reserved
000060_H	TMRLRA0 [R/W] H XXXXXXXX XXXXXXXX		TMR0 [R] H XXXXXXXX XXXXXXXX		Reload Timer 0
000064_H	TMRLRB0 [R/W] H XXXXXXXX XXXXXXXX		TMCSR0 [R/W] B,H,W 00000000 0-000000		
000068_H	TMRLRA7 [R/W] H XXXXXXXX XXXXXXXX		TMR7 [R] H XXXXXXXX XXXXXXXX		Reload Timer 7
$00006C_H$	TMRLRB7 [R/W] H XXXXXXXX XXXXXXXX		TMCSR7 [R/W] B,H,W 00000000 0-000000		
000070_H	—	FRS8 [R/W] B,H,W --00--00 --00--00 --00--00			Free-run timer selection register 8
000074_H	—	FRS9 [R/W] B,H,W --00--00 --00--00 --00--00			Free-run timer selection register 9
000078_H	—	—	—	OCLS67 [R/W] B,H,W ----0000	OCU67 Output level control register

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$00007C_H$	—	—	—	OCLS89 [R/W] B,H,W ----0000	OCU89 Output level control register
000080_H	BT0TMR [R] H 00000000 00000000		BT0TMCR [R/W] H -000--00 -000-000		Base Timer 0
000084_H	BT0TMCR2 [R/W] B -------0	BT0STC [R/W] B -0-0-0-0	—	—	
000088_H	BT0PCSR/BT0PRLL [R/W] H 00000000 00000000		BT0PDUT/BT0PRLH/BT0DTBF [R/W] H 00000000 00000000		
$00008C_H$	—	—	—	—	Reserved
000090_H	BT1TMR [R] H 00000000 00000000		BT1TMCR [R/W] H -000--00 -000-000		Base Timer 1
000094_H	BT1TMCR2 [R/W] B -------0	BT1STC [R/W] B -0-0-0-0	—	—	
000098_H	BT1PCSR/BT1PRLL [R/W] H 00000000 00000000		BT1PDUT/BT1PRLH/BT1DTBF [R/W] H 00000000 00000000		
$00009C_H$	BTSEL01 [R/W] B ----0000	—	BTSSSR [W] B,H -------- ------11		Base Timer 0,1
$0000A0_H$ to $0000FC_H$	—	—	—	—	Reserved
000100_H	TMRLRA1 [R/W] H XXXXXXXX XXXXXXXX		TMR1 [R] H XXXXXXXX XXXXXXXX		Reload Timer 1
000104_H	TMRLRB1 [R/W] H XXXXXXXX XXXXXXXX		TMCSR1 [R/W] B, H,W 00000000 0-000000		
000108_H	TMRLRA2 [R/W] H XXXXXXXX XXXXXXXX		TMR2 [R] H XXXXXXXX XXXXXXXX		Reload Timer 2
$00010C_H$	TMRLRB2 [R/W] H XXXXXXXX XXXXXXXX		TMCSR2 [R/W] B,H,W 00000000 0-000000		
000110_H	TMRLRA3 [R/W] H XXXXXXXX XXXXXXXX		TMR3 [R] H XXXXXXXX XXXXXXXX		Reload Timer 3
000114_H	TMRLRB3 [R/W] H XXXXXXXX XXXXXXXX		TMCSR3 [R/W] B,H,W 00000000 0-000000		
000118_H	MSCY4 [R] H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Input Capture 4,5 Cycle measurement data register 45
$00011C_H$	MSCY5 [R] H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000120_H	OCCP6 [R/W] W 00000000 00000000 00000000 00000000				Output Compare 6,7 32-bit OCU
000124_H	OCCP7 [R/W] W 00000000 00000000 00000000 00000000				
000128_H	—	—	OCSH67 [R/W] B,H,W ---0--00	OCSL67 [R/W] B,H,W 0000--00	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$00012C_H$	OCCP8 [R/W] W 00000000 00000000 00000000 00000000				Output Compare 8,9 32-bit OCU
000130_H	OCCP9 [R/W] W 00000000 00000000 00000000 00000000				
000134_H	—	—	OCSH89 [R/W] B,H,W ---0--00	OCSL89 [R/W] B,H,W 0000--00	
000138_H to $0001B4_H$	—	—	—	—	Reserved
$0001B8_H$	EPFR64 [R/W] B,H,W -----00-	EPFR65 [R/W] B,H,W 0000-000	EPFR66 [R/W] B,H,W --000000	EPFR67 [R/W] B,H,W ----0000	Extended port function register
$0001BC_H$	EPFR68 [R/W] B,H,W ----0000	EPFR69 [R/W] B,H,W ----0000	EPFR70 [R/W] B,H,W ---00000	EPFR71 [R/W] B,H,W -0-0-0-0	
$0001C0_H$	EPFR72 [R/W] B,H,W 000000-0	EPFR73 [R/W] B,H,W 00000000	EPFR74 [R/W] B,H,W 00000000	EPFR75 [R/W] B,H,W 00000000	
$0001C4_H$	EPFR76 [R/W] B,H,W 00000000	EPFR77 [R/W] B,H,W --000000	EPFR78 [R/W] B,H,W ------00	EPFR79 [R/W] B,H,W 00000000	
$0001C8_H$	EPFR80 [R/W] B,H,W ---00000	EPFR81 [R/W] B,H,W 00000000	EPFR82 [R/W] B,H,W 00000000	EPFR83 [R/W] B,H,W -0000000	
$0001CC_H$	EPFR84 [R/W] B,H,W 00000000	EPFR85 [R/W] B,H,W --000000	EPFR86 [R/W] B,H,W ---00000	EPFR87 [R/W] B,H,W ------00	
$0001D0_H$	EPFR88 [R/W] B,H,W -------0	—	—	—	
$0001D4_H$	—	—	—	—	Reserved
$0001D8_H$	TMRLRA4 [R/W] H XXXXXXXX XXXXXXXX		TMR4 [R] H XXXXXXXX XXXXXXXX		Reload Timer 4
$0001DC_H$	TMRLRB4 [R/W] H XXXXXXXX XXXXXXXX		TMCSR4 [R/W] B, H,W 00000000 0-000000		
$0001E0_H$ to $0001EC_H$	—	—	—	—	Reserved
$0001F0_H$	TMRLRA5 [R/W] H XXXXXXXX XXXXXXXX		TMR5 [R] H XXXXXXXX XXXXXXXX		Reload Timer 5
$0001F4_H$	TMRLRB5 [R/W] H XXXXXXXX XXXXXXXX		TMCSR5 [R/W] B, H,W 00000000 0-000000		
$0001F8_H$	TMRLRA6 [R/W] H XXXXXXXX XXXXXXXX		TMR6 [R] H XXXXXXXX XXXXXXXX		Reload Timer 6
$0001FC_H$	TMRLRB6 [R/W] H XXXXXXXX XXXXXXXX		TMCSR6 [R/W] B, H,W 00000000 0-000000		
000200_H to 000238_H	—	—	—	—	Reserved
$00023C_H$	DACR0 [R/W] B,H,W -------0	DADR0 [R/W] B,H,W XXXXXXXX	DACR1 [R/W] B,H,W -------0	DADR1 [R/W] B,H,W XXXXXXXX	DA Converter

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000240_H	CPCLR3 [R/W] W 11111111 11111111 11111111 11111111				Free-run Timer 3 32-bit FRT
000244_H	TCDT3 [R/W] W 00000000 00000000 00000000 00000000				
000248_H	TCCSH3 [R/W] B,H,W 0-----00	TCCSL3 [R/W] B,H,W -1-00000	—	—	
$00024C_H$	CPCLR4 [R/W] W 11111111 11111111 11111111 11111111				Free-run Timer 4 32-bit FRT
000250_H	TCDT4 [R/W] W 00000000 00000000 00000000 00000000				
000254_H	TCCSH4 [R/W] B,H,W 0-----00	TCCSL4 [R/W] B,H,W -1-00000	—	—	
000258_H to $0002C0_H$	—	—	—	—	Reserved
$0002C4_H$ to $0002FC_H$	—	—	—	—	Reserved
000300_H to $00030C_H$	—	—	—	—	Reserved
000310_H	—	—	MPUCR [R/W] H 000000-0 ----0100		MPU [S] (Only CPU core can access this area)
000314_H	—	—	—	—	
000318_H	—				
$00031C_H$	—	—	—		
000320_H	DPVAR [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000324_H	—	—	DPVSR [R/W] H -------- 00000--0		
000328_H	DEAR [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00032C_H$	—	—	DESR [R/W] H -------- 00000--0		
000330_H	PABR0 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
000334_H	—	—	PACR0 [R/W] H 000000-0 00000--0		
000338_H	PABR1 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
$00033C_H$	—	—	PACR1 [R/W] H 000000-0 00000--0		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000340_H	PABR2 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				MPU [S] (Only CPU core can access this area)
000344_H	—	—	PACR2 [R/W] H 000000-0 00000--0		
000348_H	PABR3 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
$00034C_H$	—	—	PACR3 [R/W] H 000000-0 00000--0		
000350_H	PABR4 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
000354_H	—	—	PACR4 [R/W] H 000000-0 00000--0		
000358_H	PABR5 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
$00035C_H$	—	—	PACR5 [R/W] H 000000-0 00000--0		
000360_H	PABR6 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
000364_H	—	—	PACR6 [R/W] H 000000-0 00000--0		
000368_H	PABR7 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
$00036C_H$	—	—	PACR7 [R/W] H 000000-0 00000--0		
000370_H to $0003AC_H$	—				Reserved [S]
$0003B0_H$ to $0003FC_H$	—	—	—	—	Reserved [S]
000400_H	ICSEL0 [R/W] B,H,W -----000	ICSEL1 [R/W] B,H,W -----000	ICSEL2 [R/W] B,H,W -------0	ICSEL3 [R/W] B,H,W -------0	DMA request generation and clear
000404_H	—	ICSEL5 [R/W] B,H,W -----000	ICSEL6 [R/W] B,H,W ----0000	ICSEL7 [R/W] B,H,W ----0000	
000408_H	ICSEL8 [R/W] B,H,W ------00	ICSEL9 [R/W] B,H,W ------00	ICSEL10 [R/W] B,H,W ------00	ICSEL11 [R/W] B,H,W -----000	
$00040C_H$	—	ICSEL13 [R/W] B,H,W ------00	ICSEL14 [R/W] B,H,W ------00	ICSEL15 [R/W] B,H,W ------00	
000410_H	ICSEL16 [R/W] B,H,W ----0000	ICSEL17 [R/W] B,H,W ------00	ICSEL18 [R/W] B,H,W ---00000	ICSEL19 [R/W] B,H,W -----000	
000414_H	ICSEL20 [R/W] B,H,W -----000	ICSEL21 [R/W] B,H,W ------00	ICSEL22 [R/W] B,H,W ------00	ICSEL23 [R/W] B,H,W ------00	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000418_H	IRPR0H [R] B,H,W 00------	IRPR0L [R] B,H,W 00------	IRPR1H [R] B,H,W 00------	IRPR1L [R] B,H,W 00------	Interrupt Request Batch Reading Register
$00041C_H$	—	—	IRPR3H [R] B,H,W 000000--	IRPR3L [R] B,H,W 000000--	
000420_H	IRPR4H [R] B,H,W 0000----	IRPR4L [R] B,H,W 0000----	IRPR5H [R] B,H,W 0000----	IRPR5L [R] B,H,W 000-----	
000424_H	IRPR6H [R] B,H,W --00----	IRPR6L [R] B,H,W 0000----	IRPR7H [R] B,H,W -0-00---	IRPR7L [R] B,H,W ------00	
000428_H	IRPR8H [R] B,H,W --0-----	IRPR8L [R] B,H,W -00-----	IRPR9H [R] B,H,W -0------	IRPR9L [R] B,H,W -0------	
$00042C_H$	IRPR10H [R] B,H,W -0------	IRPR10L [R] B,H,W -0------	IRPR11H [R] B,H,W 0-------	IRPR11L [R] B,H,W 0-------	
000430_H	IRPR12H [R] B,H,W --0000--	IRPR12L [R] B,H,W ----00--	IRPR13H [R] B,H,W 00------	IRPR13L [R] B,H,W 00------	
000434_H	IRPR14H [R] B,H,W 00000000	IRPR14L [R] B,H,W 00000000	IRPR15H [R] B,H,W 000-----	IRPR15L [R] B,H,W 0000000-	
000438_H	ICSEL24 [R/W] B,H,W ------00	ICSEL25 [R/W] B,H,W ---00000	ICSEL26 [R/W] B,H,W -------0	ICSEL27 [R/W] B,H,W -------0	DMA request generation and clear
$00043C_H$	—	—	—	—	Reserved [S]
000440_H	ICR00 [R/W] B,H,W ---11111	ICR01 [R/W] B,H,W ---11111	ICR02 [R/W] B,H,W ---11111	ICR03 [R/W] B,H,W ---11111	Interrupt Controller [S]
000444_H	ICR04 [R/W] B,H,W ---11111	ICR05 [R/W] B,H,W ---11111	ICR06 [R/W] B,H,W ---11111	ICR07 [R/W] B,H,W ---11111	
000448_H	ICR08 [R/W] B,H,W ---11111	ICR09 [R/W] B,H,W ---11111	ICR10 [R/W] B,H,W ---11111	ICR11 [R/W] B,H,W ---11111	
$00044C_H$	ICR12 [R/W] B,H,W ---11111	ICR13 [R/W] B,H,W ---11111	ICR14 [R/W] B,H,W ---11111	ICR15 [R/W] B,H,W ---11111	
000450_H	ICR16 [R/W] B,H,W ---11111	ICR17 [R/W] B,H,W ---11111	ICR18 [R/W] B,H,W ---11111	ICR19 [R/W] B,H,W ---11111	
000454_H	ICR20 [R/W] B,H,W ---11111	ICR21 [R/W] B,H,W ---11111	ICR22 [R/W] B,H,W ---11111	ICR23 [R/W] B,H,W ---11111	
000458_H	ICR24 [R/W] B,H,W ---11111	ICR25 [R/W] B,H,W ---11111	ICR26 [R/W] B,H,W ---11111	ICR27 [R/W] B,H,W ---11111	
$00045C_H$	ICR28 [R/W] B,H,W ---11111	ICR29 [R/W] B,H,W ---11111	ICR30 [R/W] B,H,W ---11111	ICR31 [R/W] B,H,W ---11111	
000460_H	ICR32 [R/W] B,H,W ---11111	ICR33 [R/W] B,H,W ---11111	ICR34 [R/W] B,H,W ---11111	ICR35 [R/W] B,H,W ---11111	
000464_H	ICR36 [R/W] B,H,W ---11111	ICR37 [R/W] B,H,W ---11111	ICR38 [R/W] B,H,W ---11111	ICR39 [R/W] B,H,W ---11111	
000468_H	ICR40 [R/W] B,H,W ---11111	ICR41 [R/W] B,H,W ---11111	ICR42 [R/W] B,H,W ---11111	ICR43 [R/W] B,H,W ---11111	
$00046C_H$	ICR44 [R/W] B,H,W ---11111	ICR45 [R/W] B,H,W ---11111	ICR46 [R/W] B,H,W ---11111	ICR47 [R/W] B,H,W ---11111	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000470_H to $00047C_H$	—	—	—	—	Reserved [S]
000480_H	RSTRR [R] B,H,W XXXX--XX	RSTCR [R/W] B,H,W 111----0	STBCR [R/W] B,H,W * 000---11	—	Reset Control [S] Power Control [S] *: Writing STBCR by DMA is forbidden
000484_H	—	—	—	—	Reserved [S]
000488_H	DIVR0 [R/W] B,H,W 000-----	DIVR1 [R/W] B,H,W 0001----	DIVR2 [R/W] B,H,W 0011----	—	Clock Control [S]
$00048C_H$	—	—	—	—	Reserved [S]
000490_H	IORR0 [R/W] B,H,W -0000000	IORR1 [R/W] B,H,W -0000000	IORR2 [R/W] B,H,W -0000000	IORR3 [R/W] B,H,W -0000000	DMA request by peripheral [S]
000494_H	IORR4 [R/W] B,H,W -0000000	IORR5 [R/W] B,H,W -0000000	IORR6 [R/W] B,H,W -0000000	IORR7 [R/W] B,H,W -0000000	
000498_H	IORR8 [R/W] B,H,W -0000000	IORR9 [R/W] B,H,W -0000000	IORR10 [R/W] B,H,W -0000000	IORR11 [R/W] B,H,W -0000000	
$00049C_H$	IORR12 [R/W] B,H,W -0000000	IORR13 [R/W] B,H,W -0000000	IORR14 [R/W] B,H,W -0000000	IORR15 [R/W] B,H,W -0000000	
$0004A0_H$	—	—	—	—	Reserved
$0004A4_H$	CANPRE [R/W] B,H,W ---00000	—	—	—	CAN prescaler
$0004A8_H$	—	—	CSCFG[R/W]B,H,W ---0----	CMCFG[R/W]B,H,W 00000000	Clock monitor control register
$0004AC_H$	ADERH0[R/W] B,H 11111111 11111111		ADERL0[R/W] B,H 11111111 11111111		Analog input control register 0
$0004B0_H$	—		ADERL1[R/W] B,H 11111111 11111111		Analog input control register 1
$0004B4_H$	—	—	—	—	Reserved
$0004B8_H$	CUCR0 [R/W] B,H,W -------- ---0--00		CUTD0 [R/W] B,H,W 10000000 00000000		RTC/WDT1 calibration
$0004BC_H$	CUTR0 [R] B,H,W -------- 00000000 00000000 00000000				
$0004C0_H$	—	—	—	—	
$0004C4_H$	CUCR1 [R/W] B,H,W -------- ---0--00		CUTD1 [R/W] B,H,W 11000011 01010000		
$0004C8_H$	CUTR1 [R] B,H,W -------- 00000000 00000000 00000000				
$0004CC_H$ to $00050C_H$	—	—	—	—	Reserved

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000510_H	CSELR [R/W] B,H,W 001---00	CMONR [R] B,H,W 001---00	MTMCR [R/W] B,H,W 00001111	STMCR [R/W] B,H,W 0000-111	Clock Control [S]
000514_H	PLLCR [R/W] B,H,W -------- 11110000		CSTBR [R/W] B,H,W -0000000	PTMCR [R/W] B,H,W 00------	
000518_H	—	—	CPUAR [R/W] B,H,W 0----XXX	—	Reset Control [S]
$00051C_H$	—	—	—	—	Reserved [S]
000520_H	CCPSSELR [R/W] B,H,W -------0	—	—	CCPSDIVR [R/W] B,H,W -000-000	Clock Control 2 [S]
000524_H	—	CCPLLFBR [R/W] B,H,W -0000000	CCSSFBR0 [R/W] B,H,W --000000	CCSSFBR1 [R/W] B,H,W ---00000	
000528_H	—	CCSSCCR0 [R/W] B,H,W ----0000	CCSSCCR1 [R/W] H,W 000----- --------		
$00052C_H$	—	CCCGRCR0 [R/W] B,H,W 00----00	CCCGRCR1 [R/W] B,H,W 00000000	CCCGRCR2 [R/W] B,H,W 00000000	
000530_H	CCRTSELR [R/W] B,H,W 0------0	—	CCPMUCR0 [R/W] B,H,W 0-----00	CCPMUCR1 [R/W] B,H,W 0--00000	
000534_H to $00054C_H$	—	—	—	—	Reserved
000550_H	EIRR0 [R/W] B,H,W XXXXXXXX	ENIR0 [R/W] B,H,W 00000000	ELVR0 [R/W] B,H,W 00000000 00000000		External Interrupt (INT0 to 7)
000554_H	EIRR1 [R/W] B,H,W XXXXXXXX	ENIR1 [R/W] B,H,W 00000000	ELVR1 [R/W] B,H,W 00000000 00000000		External Interrupt (INT8 to 15)
000558_H	—	—	—	—	Reserved
$00055C_H$	—	—	WTDR [R/W] H 00000000 00000000		Real Time Clock (RTC)
000560_H	—	WTCRH [R/W] B ------00	WTCRM [R/W] B,H 00000000	WTCRL [R/W] B,H ----00-0	
000564_H	—	WTBRH [R/W] B --XXXXXX	WTBRM [R/W] B XXXXXXXX	WTBRL [R/W] B XXXXXXXX	
000568_H	WTHR [R/W] B,H ---00000	WTMR [R/W] B,H --000000	WTSR [R/W] B --000000	—	
$00056C_H$	—	CSVCR [R/W] B 000111--	—	—	Clock Supervisor
000570_H to $00057C_H$	—	—	—	—	Reserved

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000580_H	REGSEL [R/W] B,H,W 0110011-	—	—	—	Regulator Control / Low Voltage Detection
000584_H	LVD5R [R/W] B,H,W -------1	LVD5F [R/W] B,H,W 00000001	LVD [R/W] B,H,W 01000--0	—	
000588_H to $00058C_H$	—	—	—	—	Reserved
000590_H	PMUSTR [R/W] B,H,W 0-----1X	PMUCTLR [R/W] B,H,W 0-00----	PWRTMCTL [R/W] B,H,W -----011	—	PMU
000594_H	PMUINTF0 [R/W] B,H,W 00000000	PMUINTF1 [R/W] B,H,W 00000000	PMUINTF2 [R/W] B,H,W 0000----	—	
000598_H	—	—	—	—	
$00059C_H$ to $0005BC_H$	—	—	—	—	Reserved
$0005C0_H$ to $0005FC_H$	—	—	—	—	Reserved
000600_H	ASR0 [R/W] W 00000000 00000000 -------- 1111-001				External Bus Interface [S]
000604_H	ASR1 [R/W] W XXXXXXXX XXXXXXXX -------- XXXX-XX0				
000608_H	ASR2 [R/W] W XXXXXXXX XXXXXXXX -------- XXXX-XX0				
$00060C_H$	ASR3 [R/W] W XXXXXXXX XXXXXXXX -------- XXXX-XX0				
000610_H to $00063C_H$	—	—	—	—	Reserved [S]
000640_H	ACR0 [R/W] W -------- -------- -------- 01--00--				External Bus Interface [S]
000644_H	ACR1 [R/W] W -------- -------- -------- XX--XX--				
000648_H	ACR2 [R/W] W -------- -------- -------- XX--XX--				
$00064C_H$	ACR3 [R/W] W -------- -------- -------- XX--XX--				
000650_H to $00067C_H$	—	—	—	—	Reserved [S]
000680_H	AWR0 [R/W] W ----1111 00000000 11110000 00000-0-				External Bus Interface [S]
000684_H	AWR1 [R/W] W ----XXXX XXXXXXXX XXXXXXXX XXXXX-X-				

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000688_H	AWR2 [R/W] W ----XXXX XXXXXXXX XXXXXXXX XXXXX-X-				External Bus Interface [S]
$00068C_H$	AWR3 [R/W] W ----XXXX XXXXXXXX XXXXXXXX XXXXX-X-				
000690_H to $0006FC_H$	—	—	—	—	Reserved [S]
000700_H to $00070C_H$	—	—	—	—	Reserved
000710_H	BPCCRA [R/W] B 00000000	BPCCRB [R/W] B 00000000	BPCCRC [R/W] B 00000000	—	Bus Performance Counter
000714_H	BPCTRA [R/W] W 00000000 00000000 00000000 00000000				
000718_H	BPCTRB [R/W] W 00000000 00000000 00000000 00000000				
$00071C_H$	BPCTRC [R/W] W 00000000 00000000 00000000 00000000				
000720_H to $0007F8_H$	—	—	—	—	Reserved
$0007FC_H$	BMODR [R] B, H, W XXXXXXXX	—	—	—	Mode Register
000800_H to $00083C_H$	—	—	—	—	Reserved [S]
000840_H	FCTLR [R/W] H -0--1000 0--0----		—	FSTR [R/W] B -----001	Flash Memory Register [S]
000844_H to 000854_H	—	—	—	—	Reserved [S]
000858_H	—	—	WREN [R/W] H 00000000 00000000		Wild Register [S]
$00085C_H$ to $00087C_H$	—	—	—	—	Reserved [S]
000880_H	WRAR00 [R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				Wild Register [S]
000884_H	WRDR00 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000888_H	WRAR01 [R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$00088C_H$	WRDR01 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000890_H	WRAR02 [R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
000894_H	WRDR02 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000898_H	WRAR03 [R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				Wild Register [S]
$00089C_H$	WRDR03 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008A0_H$	WRAR04 [R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008A4_H$	WRDR04 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008A8_H$	WRAR05 [R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008AC_H$	WRDR05 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008B0_H$	WRAR06 [R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008B4_H$	WRDR06 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008B8_H$	WRAR07 [R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008BC_H$	WRDR07 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008C0_H$	WRAR08 [R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008C4_H$	WRDR08 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008C8_H$	WRAR09 [R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008CC_H$	WRDR09 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008D0_H$	WRAR10 [R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008D4_H$	WRDR10 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008D8_H$	WRAR11 [R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008DC_H$	WRDR11 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008E0_H$	WRAR12 [R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008E4_H$	WRDR12 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008E8_H$	WRAR13 [R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008EC_H$	WRDR13 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008F0_H$	WRAR14 [R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$0008F4_H$	WRDR14 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Wild Register [S]
$0008F8_H$	WRAR15 [R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008FC_H$	WRDR15 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000900_H	TPUUNLOCK [R/W] W 00000000 00000000 00000000 00000000				Time Protection Unit [S]
000904_H	TPULST [R] B,H,W -------0	—	TPUVST [R/W] B,H,W -----000	—	
000908_H	TPUCFG [R/W] B,H,W -------0 0-000000 -------- -------0				
$00090C_H$	TPUTIR [R] B,H,W 00000000	—	—	—	
000910_H	TPUTST [R] B,H,W 00000000	—	—	—	
000914_H	TPUTIE [R/W] B,H,W 00000000	—	—	—	
000918_H	TPUTMID [R] B,H,W 00000000 00000000 00000000 00000000				
$00091C_H$ to $00092C_H$	—	—	—	—	
000930_H	TPUTCN00 [R/W] B,H,W 000000-- 00000000 00000000 00000000				
000934_H	TPUTCN01 [R/W] B,H,W 000000-- 00000000 00000000 00000000				
000938_H	TPUTCN02 [R/W] B,H,W 000000-- 00000000 00000000 00000000				
$00093C_H$	TPUTCN03 [R/W] B,H,W 000000-- 00000000 00000000 00000000				
000940_H	TPUTCN04 [R/W] B,H,W 000000-- 00000000 00000000 00000000				
000944_H	TPUTCN05 [R/W] B,H,W 000000-- 00000000 00000000 00000000				
000948_H	TPUTCN06 [R/W] B,H,W 000000-- 00000000 00000000 00000000				
$00094C_H$	TPUTCN07 [R/W] B,H,W 000000-- 00000000 00000000 00000000				
000950_H	TPUTCN10 [R/W] B,H,W ---00000	—	—	—	
000954_H	TPUTCN11 [R/W] B,H,W ---00000	—	—	—	
000958_H	TPUTCN12 [R/W] B,H,W ---00000	—	—	—	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$00095C_H$	TPUTCN13 [R/W] B,H,W ---00000	—	—	—	Time Protection Unit [S]
000960_H	TPUTCN14 [R/W] B,H,W ---00000	—	—	—	
000964_H	TPUTCN15 [R/W] B,H,W ---00000	—	—	—	
000968_H	TPUTCN16 [R/W] B,H,W ---00000	—	—	—	
$00096C_H$	TPUTCN17 [R/W] B,H,W ---00000	—	—	—	
000970_H	TPUTCC0 [R] B,H,W -------- 00000000 00000000 00000000				
000974_H	TPUTCC1 [R] B,H,W -------- 00000000 00000000 00000000				
000978_H	TPUTCC2 [R] B,H,W -------- 00000000 00000000 00000000				
$00097C_H$	TPUTCC3 [R] B,H,W -------- 00000000 00000000 00000000				
000980_H	TPUTCC4 [R] B,H,W -------- 00000000 00000000 00000000				
000984_H	TPUTCC5 [R] B,H,W -------- 00000000 00000000 00000000				
000988_H	TPUTCC6 [R] B,H,W -------- 00000000 00000000 00000000				
$00098C_H$	TPUTCC7 [R] B,H,W -------- 00000000 00000000 00000000				
000990_H to $0009FC_H$	—	—	—	—	
$000A00_H$ to $000BEC_H$	—	—	—	—	Reserved
$000BF0_H$	HSCFR [R/W] B,H,W -------- ------00 00000000 00000000				OCDU
$000BF4_H$	—	—	—	—	
$000BF8_H$	—	—	MBR [R/W] B,H,W 00------ XXXXXXXX		
$000BFC_H$	—	—	UER [W] B,H,W -------- -------X		
$000C00_H$	DCCR0 [R/W] W 0----000 --00--00 00000000 0-000000				DMA Controller [S]
$000C04_H$	DCSR0 [R/W] H 0------- -----000		DTCR0 [R/W] H 00000000 00000000		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$000C08_H$	DSAR0 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				DMA Controller [S]
$000C0C_H$	DDAR0 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C10_H$	DCCR1 [R/W] W 0----000 --00--00 00000000 0-000000				
$000C14_H$	DCSR1 [R/W] H 0------- -----000		DTCR1 [R/W] H 00000000 00000000		
$000C18_H$	DSAR1 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C1C_H$	DDAR1 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C20_H$	DCCR2 [R/W] W 0----000 --00--00 00000000 0-000000				
$000C24_H$	DCSR2 [R/W] H 0------- -----000		DTCR2 [R/W] H 00000000 00000000		
$000C28_H$	DSAR2 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C2C_H$	DDAR2 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C30_H$	DCCR3 [R/W] W 0----000 --00--00 00000000 0-000000				
$000C34_H$	DCSR3 [R/W] H 0------- -----000		DTCR3 [R/W] H 00000000 00000000		
$000C38_H$	DSAR3 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C3C_H$	DDAR3 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C40_H$	DCCR4 [R/W] W 0----000 --00--00 00000000 0-000000				
$000C44_H$	DCSR4 [R/W] H 0------- -----000		DTCR4 [R/W] H 00000000 00000000		
$000C48_H$	DSAR4 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C4C_H$	DDAR4 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C50_H$	DCCR5 [R/W] W 0----000 --00--00 00000000 0-000000				
$000C54_H$	DCSR5 [R/W] H 0------- -----000		DTCR5 [R/W] H 00000000 00000000		
$000C58_H$	DSAR5 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C5C_H$	DDAR5 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C60_H$	DCCR6 [R/W] W 0----000 --00--00 00000000 0-000000				
$000C64_H$	DCSR6 [R/W] H 0------- -----000		DTCR6 [R/W] H 00000000 00000000		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$000C68_H$	DSAR6 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				DMA Controller [S]
$000C6C_H$	DDAR6 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C70_H$	DCCR7 [R/W] W 0----000 --00--00 00000000 0-000000				
$000C74_H$	DCSR7 [R/W] H 0------- -----000		DTCR7 [R/W] H 00000000 00000000		
$000C78_H$	DSAR7 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C7C_H$	DDAR7 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C80_H$	DCCR8 [R/W] W 0----000 --00--00 00000000 0-000000				
$000C84_H$	DCSR8 [R/W] H 0------- -----000		DTCR8 [R/W] H 00000000 00000000		
$000C88_H$	DSAR8 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C8C_H$	DDAR8 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C90_H$	DCCR9 [R/W] W 0----000 --00--00 00000000 0-000000				
$000C94_H$	DCSR9 [R/W] H 0------- -----000		DTCR9 [R/W] H 00000000 00000000		
$000C98_H$	DSAR9 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C9C_H$	DDAR9 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000CA0_H$	DCCR10 [R/W] W 0----000 --00--00 00000000 0-000000				
$000CA4_H$	DCSR10 [R/W] H 0------- -----000		DTCR10 [R/W] H 00000000 00000000		
$000CA8_H$	DSAR10 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000CAC_H$	DDAR10 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000CB0_H$	DCCR11 [R/W] W 0----000 --00--00 00000000 0-000000				
$000CB4_H$	DCSR11 [R/W] H 0------- -----000		DTCR11 [R/W] H 00000000 00000000		
$000CB8_H$	DSAR11 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000CBC_H$	DDAR11 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$000CC0_H$	DCCR12 [R/W] W 0----000 --00--00 00000000 0-000000				DMA Controller [S]
$000CC4_H$	DCSR12 [R/W] H 0------- -----000		DTCR12 [R/W] H 00000000 00000000		
$000CC8_H$	DSAR12 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000CCC_H$	DDAR12 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000CD0_H$	DCCR13 [R/W] W 0----000 --00--00 00000000 0-000000				
$000CD4_H$	DCSR13 [R/W] H 0------- -----000		DTCR13 [R/W] H 00000000 00000000		
$000CD8_H$	DSAR13 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000CDC_H$	DDAR13 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000CE0_H$	DCCR14 [R/W] W 0----000 --00--00 00000000 0-000000				
$000CE4_H$	DCSR14 [R/W] H 0------- -----000		DTCR14 [R/W] H 00000000 00000000		
$000CE8_H$	DSAR14 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000CEC_H$	DDAR14 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000CF0_H$	DCCR15 [R/W] W 0----000 --00--00 00000000 0-000000				
$000CF4_H$	DCSR15 [R/W] H 0------- -----000		DTCR15 [R/W] H 00000000 00000000		
$000CF8_H$	DSAR15 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000CFC_H$	DDAR15 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000D00_H$ to $000DF0_H$	—	—	—	—	Reserved [S]
$000DF4_H$	—	—	DNMIR [R/W] B 0------0	DILVR [R/W] B ---11111	DMA Controller [S]
$000DF8_H$	DMACR[R/W] W 0------- -------- 0------- --------				
$000DFC_H$	—	—	—	—	Reserved [S]
$000E00_H$	DDR00 [R/W] B,H,W 00000000	DDR01 [R/W] B,H,W 00000000	DDR02 [R/W] B,H,W 00000000	DDR03 [R/W] B,H,W 00000000	Data Direction Register
$000E04_H$	DDR04 [R/W] B,H,W 00000000	DDR05 [R/W] B,H,W 00000000	DDR06 [R/W] B,H,W 00000000	DDR07 [R/W] B,H,W 00000000	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$000E08_H$	DDR08 [R/W] B,H,W 00000000	DDR09 [R/W] B,H,W 00000000	DDR10 [R/W] B,H,W 00000000	DDR11 [R/W] B,H,W 00000000	Data Direction Register
$000E0C_H$	DDR12 [R/W] B,H,W 00000000	DDR13 [R/W] B,H,W -0000000	DDR14 [R/W] B,H,W ---000--	DDR15 [R/W] B,H,W --000000	
$000E10_H$	—	—	—	—	
$000E14_H$	—	—	—	—	
$000E18_H$	DDR16 [R/W] B,H,W 00000000	DDR17 [R/W] B,H,W 00000000	DDR18 [R/W] B,H,W 00000000	DDR19 [R/W] B,H,W 00000000	
$000E1C_H$	—	—	—	—	Reserved
$000E20_H$	PFR00 [R/W] B,H,W 00000000	PFR01 [R/W] B,H,W 00000000	PFR02 [R/W] B,H,W 00000000	PFR03 [R/W] B,H,W 00000000	Port Function Register
$000E24_H$	PFR04 [R/W] B,H,W 00000000	PFR05 [R/W] B,H,W 00000000	PFR06 [R/W] B,H,W 00000000	PFR07 [R/W] B,H,W 00000000	
$000E28_H$	PFR08 [R/W] B,H,W 00000000	PFR09 [R/W] B,H,W 00000000	PFR10 [R/W] B,H,W 00000000	PFR11 [R/W] B,H,W 00000000	
$000E2C_H$	PFR12 [R/W] B,H,W 00000000	PFR13 [R/W] B,H,W -0000000	PFR14 [R/W] B,H,W ---000--	PFR15 [R/W] B,H,W --000000	
$000E30_H$	—	—	—	—	
$000E34_H$	—	—	—	—	
$000E38_H$	PFR16 [R/W] B,H,W 00000000	PFR17 [R/W] B,H,W 00000000	PFR18 [R/W] B,H,W 00000000	PFR19 [R/W] B,H,W 00000000	
$000E3C_H$	—	—	—	—	Reserved
$000E40_H$	PDDR00 [R] B,H,W XXXXXXXX	PDDR01 [R] B,H,W XXXXXXXX	PDDR02 [R] B,H,W XXXXXXXX	PDDR03 [R] B,H,W XXXXXXXX	Port Direct Read Register
$000E44_H$	PDDR04 [R] B,H,W XXXXXXXX	PDDR05 [R] B,H,W XXXXXXXX	PDDR06 [R] B,H,W XXXXXXXX	PDDR07 [R] B,H,W XXXXXXXX	
$000E48_H$	PDDR08 [R] B,H,W XXXXXXXX	PDDR09 [R] B,H,W XXXXXXXX	PDDR10 [R] B,H,W XXXXXXXX	PDDR11 [R] B,H,W XXXXXXXX	
$000E4C_H$	PDDR12 [R] B,H,W XXXXXXXX	PDDR13 [R] B,H,W -XXXXXXX	PDDR14 [R] B,H,W ---XXX--	PDDR15 [R] B,H,W --XXXXXX	
$000E50_H$	—	—	—	—	
$000E54_H$	—	—	—	—	
$000E58_H$	PDDR16 [R] B,H,W XXXXXXXX	PDDR17 [R] B,H,W XXXXXXXX	PDDR18 [R] B,H,W XXXXXXXX	PDDR19 [R] B,H,W XXXXXXXX	
$000E5C_H$	—	—	—	—	Reserved
$000E60_H$	EPFR00 [R/W] B,H,W 00000000	EPFR01 [R/W] B,H,W -0-0-000	EPFR02 [R/W] B,H,W ----0000	EPFR03 [R/W] B,H,W ---000-0	Extended Port Function Register
$000E64_H$	EPFR04 [R/W] B,H,W ----00-0	EPFR05 [R/W] B,H,W ----0000	EPFR06 [R/W] B,H,W ----000-	EPFR07 [R/W] B,H,W ---00000	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$000E68_H$	EPFR08 [R/W] B,H,W ---00000	EPFR09 [R/W] B,H,W -----00-	EPFR10 [R/W] B,H,W ----0000	EPFR11 [R/W] B,H,W ----0000	Extended Port Function Register
$000E6C_H$	EPFR12 [R/W] B,H,W ----0000	EPFR13 [R/W] B,H,W ------00	EPFR14 [R/W] B,H,W ------00	EPFR15 [R/W] B,H,W -----000	
$000E70_H$	—	—	—	—	
$000E74_H$	—	—	—	—	
$000E78_H$	—	—	EPFR26 [R/W] B,H,W 00000000	EPFR27 [R/W] B,H,W ---0----	
$000E7C_H$	EPFR28 [R/W] B,H,W --000-0-	EPFR29 [R/W] B,H,W 00000000	—	—	
$000E80_H$	—	EPFR33 [R/W] B,H,W -----00-	EPFR34 [R/W] B,H,W -----00-	EPFR35 [R/W] B,H,W ---00000	
$000E84_H$	EPFR36 [R/W] B,H,W ----000-	—	—	—	
$000E88_H$	—	—	EPFR42 [R/W] B,H,W ------00	EPFR43 [R/W] B,H,W 0--0000-	
$000E8C_H$	EPFR44 [R/W] B,H,W -00---0-	EPFR45 [R/W] B,H,W -0000000	—	—	
$000E90_H$	—	—	—	—	
$000E94_H$	—	—	—	—	
$000E98_H$	EPFR56 [R/W] B,H,W -----0-0	EPFR57 [R/W] B,H,W ----00-0	EPFR58 [R/W] B,H,W ----00-0	EPFR59 [R/W] B,H,W ----00-0	
$000E9C_H$	EPFR60 [R/W] B,H,W ----00-0	EPFR61 [R/W] B,H,W -----00-	EPFR62 [R/W] B,H,W -----00-	EPFR63 [R/W] B,H,W ---0000-	
$000EA0_H$ to $000EBC_H$	—	—	—	—	Reserved
$000EC0_H$	PPER00 [R/W] B,H,W 00000000	PPER01 [R/W] B,H,W 00000000	PPER02 [R/W] B,H,W 00000000	PPER03 [R/W] B,H,W 00000000	Port Pull-up/down Enable Register
$000EC4_H$	PPER04 [R/W] B,H,W 00000000	PPER05 [R/W] B,H,W 00000000	PPER06 [R/W] B,H,W 00000000	PPER07 [R/W] B,H,W 00000000	
$000EC8_H$	PPER08 [R/W] B,H,W 00000000	PPER09 [R/W] B,H,W 00000000	PPER10 [R/W] B,H,W 00000000	PPER11 [R/W] B,H,W 00000000	
$000ECC_H$	PPER12 [R/W] B,H,W 00000000	PPER13 [R/W] B,H,W -0000000	PPER14 [R/W] B,H,W ---000--	PPER15 [R/W] B,H,W --000000	
$000ED0_H$	—	—	—	—	
$000ED4_H$	—	—	—	—	
$000ED8_H$	PPER16 [R/W] B,H,W 00000000	PPER17 [R/W] B,H,W 00000000	PPER18 [R/W] B,H,W 00000000	PPER19 [R/W] B,H,W 00000000	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$000EDC_H$ to $000F3C_H$	—	—	—	—	Reserved
$000F40_H$	PORTEN [R/W] B,H,W -------0	—	—	—	Port Enable Register
$000F44_H$	KEYCDR [R/W] H 00000000 00000000		—	—	KeyCodeRegister
$000F48_H$ to $000F64_H$	—	—	—	—	Reserved
$000F68_H$	MSCY6 [R] H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Input Capture 6,7 Cycle measurement data register 67
$000F6C_H$	MSCY7 [R] H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000F70_H$	RCRH0 [W] H,W XXXXXXXX	RCRL0 [W] B,H,W XXXXXXXX	UDCRH0 [R] H,W 00000000	UDCRL0 [R] B,H,W 00000000	Up/Down Counter 0
$000F74_H$	CCR0 [R/W] B,H 00000000 -0001000		—	CSR0 [R/W] B 00000000	
$000F78_H$ to $000F7C_H$	—	—	—	—	Reserved
$000F80_H$	RCRH1 [W] H,W XXXXXXXX	RCRL1 [W] B,H,W XXXXXXXX	UDCRH1 [R] H,W 00000000	UDCRL1 [R] B,H,W 00000000	Up/Down Counter 1
$000F84_H$	CCR1 [R/W] B,H 00000000 -0001000		—	CSR1 [R/W] B 00000000	
$000F88_H$	—	—	MSCH45 [R] B,H,W 00000000	MSCL45 [R/W] B,H,W ------00	Input Capture 4,5 32-bit ICU Cycle and pulse width measurement control 45
$000F8C_H$	—	—	MSCH67 [R] B,H,W 00000000	MSCL67 [R/W] B,H,W ------00	Input Capture 6,7 32-bit ICU Cycle and pulse width measurement control 67
$000F90_H$	OCCP10 [R/W] W 00000000 00000000 00000000 00000000				Output Compare 10,11 32-bit OCU
$000F94_H$	OCCP11 [R/W] W 00000000 00000000 00000000 00000000				
$000F98_H$	—	—	OCSH1011 [R/W] B,H,W ---0--00	OCSL1011 [R/W] B,H,W 0000--00	
$000F9C_H$	—	—	—	OCLS1011 [R/W] B,H,W ----0000	OCU1011 Output level control register

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$000FA0_H$	CPCLR5 [R/W] W 11111111 11111111 11111111 11111111				Free-run Timer 5 32-bit FRT
$000FA4_H$	TCDT5 [R/W] W 00000000 00000000 00000000 00000000				
$000FA8_H$	TCCSH5 [R/W]B,H,W 0-----00	TCCSL5 [R/W]B,H,W -1-00000	—	—	
$000FAC_H$ to $000FCC_H$	—	—	—	—	Reserved
$000FD0_H$	IPCP4 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Input Capture 4,5 32-bit ICU
$000FD4_H$	IPCP5 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000FD8_H$	—	—	LSYNS1 [R/W] B,H,W 00000000	ICS45 [R/W] B,H,W 00000000	
$000FDC_H$	IPCP6 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Input Capture 6,7 32-bit ICU
$000FE0_H$	IPCP7 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000FE4_H$	—	—	—	ICS67 [R/W] B,H,W 00000000	
$000FE8_H$	IPCP8 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Input Capture 8,9 32-bit ICU
$000FEC_H$	IPCP9 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000FF0_H$	—	—	—	ICS89 [R/W] B,H,W 00000000	
$000FF4_H$	MSCY8 [R] H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Input Capture 8,9 32-bit ICU Cycle measurement data register 89
$000FF8_H$	MSCY9 [R] H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000FFC_H$	—	—	MSCH89 [R] B,H,W 00000000	MSCL89 [R/W] B,H,W ------00	Cycle and pulse width measurement control 89
001000_H	SACR [R/W] B,H,W -------0	PICD [R/W] B,H,W ----0011	—	—	Clock Control
001004_H to $00112C_H$	—	—	—	—	Reserved
001130_H	—	—	—	CRCCR [R/W] B,H,W -0000000	CRC calculation unit
001134_H	CRCINIT [R/W] B,H,W 11111111 11111111 11111111 11111111				
001138_H	CRCIN [R/W] B,H,W 00000000 00000000 00000000 00000000				
$00113C_H$	CRCR [R] B,H,W 11111111 11111111 11111111 11111111				

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001140_H to $0011FC_H$	—	—	—	—	Reserved
001200_H	TCGS [R/W] B,H,W ------00	—	—	TCGSE [R/W] B,H,W -----000	16-bit Free-run timer synchronous activation
001204_H	CPCLRB0/CPCLR0 [W] H,W 11111111 11111111		TCDT0 [R/W] H,W 00000000 00000000		16-bit Free-run Timer 0
001208_H	TCCS0 [R/W] B,H,W 00000000 01000000 ----0000 --------				
$00120C_H$	CPCLRB1/CPCLR1 [W] H,W 11111111 11111111		TCDT1 [R/W] H,W 00000000 00000000		16-bit Free-run Timer 1
001210_H	TCCS1 [R/W] B,H,W 00000000 01000000 ----0000 --------				
001214_H	CPCLRB2/CPCLR2 [W] H,W 11111111 11111111		TCDT2 [R/W] H,W 00000000 00000000		16-bit Free-run Timer 2
001218_H	TCCS2 [R/W] B,H,W 00000000 01000000 ----0000 --------				
$00121C_H$ to 001230_H	—	—	—	—	Reserved
001234_H	FRS0 [R/W] B,H,W -------- --00--00 --00--00 --00--00				16-bit Free-run timer selection
001238_H	—		FRS1 [R/W] B,H,W --00--00 --00--00		
$00123C_H$	FRS2 [R/W] B,H,W --00--00 --00--00 --00--00 --00--00				
001240_H	FRS3 [R/W] B,H,W --00--00 --00--00 --00--00 --00--00				
001244_H	FRS4 [R/W] B,H,W --00--00 --00--00 --00--00 --00--00				
001248_H	—	—	—	—	Reserved
$00124C_H$	OCCPB0/OCCP0 [R/W] H,W 00000000 00000000		OCCPB1/OCCP1 [R/W] H,W 00000000 00000000		16-bit Output compare 0/1
001250_H	OCS01 [R/W] B,H,W -110--00 00001100		—	OCMOD01 [R/W] B,H,W ------00	
001254_H	OCCPB2/OCCP2 [R/W] H,W 00000000 00000000		OCCPB3/OCCP3 [R/W] H,W 00000000 00000000		16-bit Output compare 2/3
001258_H	OCS23 [R/W] B,H,W -110--00 00001100		—	OCMOD23 [R/W] B,H,W ------00	
$00125C_H$	OCCPB4/OCCP4 [R/W] H,W 00000000 00000000		OCCPB5/OCCP5 [R/W] H,W 00000000 00000000		16-bit Output compare 4/5
001260_H	OCS45 [R/W] B,H,W -110--00 00001100		—	OCMOD45 [R/W] B,H,W ------00	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001264_H to 001278_H	—	—	—	—	Reserved
$00127C_H$	IPCP0 [R] H,W 00000000 00000000		IPCP1 [R] H,W 00000000 00000000		16-bit Input capture 0/1
001280_H	ICS01 [R/W] B,H,W ------00 00000000		—	LSYNS [R/W] B,H,W ----0000	
001284_H	IPCP2 [R] H,W 00000000 00000000		IPCP3 [R] H,W 00000000 00000000		16-bit Input capture 2/3
001288_H	ICS23 [R/W] B,H,W ------00 00000000		—	—	
$00128C_H$ to 001298_H	—	—	—	—	Reserved
$00129C_H$	—	—	—	—	Reserved
$0012A0_H$	TMRR0 [R/W] H,W 00000000 00000001		TMRR1 [R/W] H,W 00000000 00000001		Waveform generator 0/1/2
$0012A4_H$	TMRR2 [R/W] H,W 00000000 00000001		—	—	
$0012A8_H$	DTSCR0 [R/W] B,H,W 00000000	DTSCR1 [R/W] B,H,W 00000000	DTSCR2 [R/W] B,H,W 00000000	—	
$0012AC_H$	—	DTIR0 [R/W] B,H,W 000000--	—	DTMNS0 [R/W] B,H,W 00---000	
$0012B0_H$	—	SIGCR10 [R/W] B,H,W 00000000	—	SIGCR20 [R/W] B,H,W 000000-1	
$0012B4_H$	PICS0 [R/W] B,H,W 000000-- -------- -------- --------				
$0012B8_H$ to $0012CC_H$	—	—	—	—	Reserved
$0012D0_H$	FRS5 [R/W] B,H,W --00--00 --00--00 --00--00 --00--00				16-bit Free-run timer selection A/D activation compare
$0012D4_H$	FRS6 [R/W] B,H,W --00--00 --00--00 --00--00 --00--00				
$0012D8_H$	FRS7 [R/W] B,H,W --00--00 --00--00 --00--00 --00--00				
$0012DC_H$ to $0012FC_H$	—	—	—	—	Reserved
001300_H	—				Reserved
001304_H	ADTSS0[R/W] B,H,W -------0	—	—	—	12-bit A/D converter 1/2 unit
001308_H	ADTSE0[R/W] B,H,W 00000000 00000000 00000000 00000000				

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$00130C_H$	ADCOMP0/ADCOMPB0[R/W] H,W 00000000 00000000		ADCOMP1/ADCOMPB1[R/W] H,W 00000000 00000000		12-bit A/D converter 1/2 unit
001310_H	ADCOMP2/ADCOMPB2[R/W] H,W 00000000 00000000		ADCOMP3/ADCOMPB3[R/W] H,W 00000000 00000000		
001314_H	ADCOMP4/ADCOMPB4[R/W] H,W 00000000 00000000		ADCOMP5/ADCOMPB5[R/W] H,W 00000000 00000000		
001318_H	ADCOMP6/ADCOMPB6[R/W] H,W 00000000 00000000		ADCOMP7/ADCOMPB7[R/W] H,W 00000000 00000000		
$00131C_H$	ADCOMP8/ADCOMPB8[R/W] H,W 00000000 00000000		ADCOMP9/ADCOMPB9[R/W] H,W 00000000 00000000		
001320_H	ADCOMP10/ADCOMPB10[R/W] H,W 00000000 00000000		ADCOMP11/ADCOMPB11[R/W] H,W 00000000 00000000		
001324_H	ADCOMP12/ADCOMPB12[R/W] H,W 00000000 00000000		ADCOMP13/ADCOMPB13[R/W] H,W 00000000 00000000		
001328_H	ADCOMP14/ADCOMPB14[R/W] H,W 00000000 00000000		ADCOMP15/ADCOMPB15[R/W] H,W 00000000 00000000		
$00132C_H$	ADCOMP16/ADCOMPB16[R/W] H,W 00000000 00000000		ADCOMP17/ADCOMPB17[R/W] H,W 00000000 00000000		
001330_H	ADCOMP18/ADCOMPB18[R/W] H,W 00000000 00000000		ADCOMP19/ADCOMPB19[R/W] H,W 00000000 00000000		
001334_H	ADCOMP20/ADCOMPB20[R/W] H,W 00000000 00000000		ADCOMP21/ADCOMPB21[R/W] H,W 00000000 00000000		
001338_H	ADCOMP22/ADCOMPB22[R/W] H,W 00000000 00000000		ADCOMP23/ADCOMPB23[R/W] H,W 00000000 00000000		
$00133C_H$	ADCOMP24/ADCOMPB24[R/W] H,W 00000000 00000000		ADCOMP25/ADCOMPB25[R/W] H,W 00000000 00000000		
001340_H	ADCOMP26/ADCOMPB26[R/W] H,W 00000000 00000000		ADCOMP27/ADCOMPB27[R/W] H,W 00000000 00000000		
001344_H	ADCOMP28/ADCOMPB28[R/W] H,W 00000000 00000000		ADCOMP29/ADCOMPB29[R/W] H,W 00000000 00000000		
001348_H	ADCOMP30/ADCOMPB30[R/W] H,W 00000000 00000000		ADCOMP31/ADCOMPB31[R/W] H,W 00000000 00000000		
$00134C_H$	ADTCS0[R/W] B,H,W 00000000 0010----		ADTCS1[R/W] B,H,W 00000000 0010----		
001350_H	ADTCS2[R/W] B,H,W 00000000 0010----		ADTCS3[R/W] B,H,W 00000000 0010----		
001354_H	ADTCS4[R/W] B,H,W 00000000 0010----		ADTCS5[R/W] B,H,W 00000000 0010----		
001358_H	ADTCS6[R/W] B,H,W 00000000 0010----		ADTCS7[R/W] B,H,W 00000000 0010----		
$00135C_H$	ADTCS8[R/W] B,H,W 00000000 0010----		ADTCS9[R/W] B,H,W 00000000 0010----		
001360_H	ADTCS10[R/W] B,H,W 00000000 0010----		ADTCS11[R/W] B,H,W 00000000 0010----		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001364_H	ADTCS12[R/W] B,H,W 00000000 0010----		ADTCS13[R/W] B,H,W 00000000 0010----		12-bit A/D converter 1/2 unit
001368_H	ADTCS14[R/W] B,H,W 00000000 0010----		ADTCS15[R/W] B,H,W 00000000 0010----		
$00136C_H$	ADTCS16[R/W] B,H,W 00000000 0010----		ADTCS17[R/W] B,H,W 00000000 0010----		
001370_H	ADTCS18[R/W] B,H,W 00000000 0010----		ADTCS19[R/W] B,H,W 00000000 0010----		
001374_H	ADTCS20[R/W] B,H,W 00000000 0010----		ADTCS21[R/W] B,H,W 00000000 0010----		
001378_H	ADTCS22[R/W] B,H,W 00000000 0010----		ADTCS23[R/W] B,H,W 00000000 0010----		
$00137C_H$	ADTCS24[R/W] B,H,W 00000000 0010----		ADTCS25[R/W] B,H,W 00000000 0010----		
001380_H	ADTCS26[R/W] B,H,W 00000000 0010----		ADTCS27[R/W] B,H,W 00000000 0010----		
001384_H	ADTCS28[R/W] B,H,W 00000000 0010----		ADTCS29[R/W] B,H,W 00000000 0010----		
001388_H	ADTCS30[R/W] B,H,W 00000000 0010----		ADTCS31[R/W] B,H,W 00000000 0010----		
$00138C_H$	ADTCD0[R] B,H,W 10--0000 00000000		ADTCD1[R] B,H,W 10--0000 00000000		
001390_H	ADTCD2[R] B,H,W 10--0000 00000000		ADTCD3[R] B,H,W 10--0000 00000000		
001394_H	ADTCD4[R] B,H,W 10--0000 00000000		ADTCD5[R] B,H,W 10--0000 00000000		
001398_H	ADTCD6[R] B,H,W 10--0000 00000000		ADTCD7[R] B,H,W 10--0000 00000000		
$00139C_H$	ADTCD8[R] B,H,W 10--0000 00000000		ADTCD9[R] B,H,W 10--0000 00000000		
$0013A0_H$	ADTCD10[R] B,H,W 10--0000 00000000		ADTCD11[R] B,H,W 10--0000 00000000		
$0013A4_H$	ADTCD12[R] B,H,W 10--0000 00000000		ADTCD13[R] B,H,W 10--0000 00000000		
$0013A8_H$	ADTCD14[R] B,H,W 10--0000 00000000		ADTCD15[R] B,H,W 10--0000 00000000		
$0013AC_H$	ADTCD16[R] B,H,W 10--0000 00000000		ADTCD17[R] B,H,W 10--0000 00000000		
$0013B0_H$	ADTCD18[R] B,H,W 10--0000 00000000		ADTCD19[R] B,H,W 10--0000 00000000		
$0013B4_H$	ADTCD20[R] B,H,W 10--0000 00000000		ADTCD21[R] B,H,W 10--0000 00000000		
$0013B8_H$	ADTCD22[R] B,H,W 10--0000 00000000		ADTCD23[R] B,H,W 10--0000 00000000		
$0013BC_H$	ADTCD24[R] B,H,W 10--0000 00000000		ADTCD25[R] B,H,W 10--0000 00000000		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$0013C0_H$	ADTCD26[R] B,H,W 10--0000 00000000		ADTCD27[R] B,H,W 10--0000 00000000		12-bit A/D converter 1/2 unit
$0013C4_H$	ADTCD28[R] B,H,W 10--0000 00000000		ADTCD29[R] B,H,W 10--0000 00000000		
$0013C8_H$	ADTCD30[R] B,H,W 10--0000 00000000		ADTCD31[R] B,H,W 10--0000 00000000		
$0013CC_H$	ADTECS0[R/W] B,H,W -------0 ---00000		ADTECS1[R/W] B,H,W -------0 ---00000		
$0013D0_H$	ADTECS2[R/W] B,H,W -------0 ---00000		ADTECS3[R/W] B,H,W -------0 ---00000		
$0013D4_H$	ADTECS4[R/W] B,H,W -------0 ---00000		ADTECS5[R/W] B,H,W -------0 ---00000		
$0013D8_H$	ADTECS6[R/W] B,H,W -------0 ---00000		ADTECS7[R/W] B,H,W -------0 ---00000		
$0013DC_H$	ADTECS8[R/W] B,H,W -------0 ---00000		ADTECS9[R/W] B,H,W -------0 ---00000		
$0013E0_H$	ADTECS10[R/W] B,H,W -------0 ---00000		ADTECS11[R/W] B,H,W -------0 ---00000		
$0013E4_H$	ADTECS12[R/W] B,H,W -------0 ---00000		ADTECS13[R/W] B,H,W -------0 ---00000		
$0013E8_H$	ADTECS14[R/W] B,H,W -------0 ---00000		ADTECS15[R/W] B,H,W -------0 ---00000		
$0013EC_H$	ADTECS16[R/W] B,H,W -------0 ---00000		ADTECS17[R/W] B,H,W -------0 ---00000		
$0013F0_H$	ADTECS18[R/W] B,H,W -------0 ---00000		ADTECS19[R/W] B,H,W -------0 ---00000		
$0013F4_H$	ADTECS20[R/W] B,H,W -------0 ---00000		ADTECS21[R/W] B,H,W -------0 ---00000		
$0013F8_H$	ADTECS22[R/W] B,H,W -------0 ---00000		ADTECS23[R/W] B,H,W -------0 ---00000		
$0013FC_H$	ADTECS24[R/W] B,H,W -------0 ---00000		ADTECS25[R/W] B,H,W -------0 ---00000		
001400_H	ADTECS26[R/W] B,H,W -------0 ---00000		ADTECS27[R/W] B,H,W -------0 ---00000		
001404_H	ADTECS28[R/W] B,H,W -------0 ---00000		ADTECS29[R/W] B,H,W -------0 ---00000		
001408_H	ADTECS30[R/W] B,H,W -------0 ---00000		ADTECS31[R/W] B,H,W -------0 ---00000		
$00140C_H$	ADRCUT0[R/W] B,H,W ----0000 00000000		ADRCLT0[R/W] B,H,W ----0000 00000000		
001410_H	ADRCUT1[R/W] B,H,W ----0000 00000000		ADRCLT1[R/W] B,H,W ----0000 00000000		
001414_H	ADRCUT2[R/W] B,H,W ----0000 00000000		ADRCLT2[R/W] B,H,W ----0000 00000000		
001418_H	ADRCUT3[R/W] B,H,W ----0000 00000000		ADRCLT3[R/W] B,H,W ----0000 00000000		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$00141C_H$	ADRCCS0[R/W] B,H,W 00000000	ADRCCS1[R/W] B,H,W 00000000	ADRCCS2[R/W] B,H,W 00000000	ADRCCS3[R/W] B,H,W 00000000	12-bit A/D converter 1/2 unit
001420_H	ADRCCS4[R/W] B,H,W 00000000	ADRCCS5[R/W] B,H,W 00000000	ADRCCS6[R/W] B,H,W 00000000	ADRCCS7[R/W] B,H,W 00000000	
001424_H	ADRCCS8[R/W] B,H,W 00000000	ADRCCS9[R/W] B,H,W 00000000	ADRCCS10[R/W] B,H,W 00000000	ADRCCS11[R/W] B,H,W 00000000	
001428_H	ADRCCS12[R/W] B,H,W 00000000	ADRCCS13[R/W] B,H,W 00000000	ADRCCS14[R/W] B,H,W 00000000	ADRCCS15[R/W] B,H,W 00000000	
$00142C_H$	ADRCCS16[R/W] B,H,W 00000000	ADRCCS17[R/W] B,H,W 00000000	ADRCCS18[R/W] B,H,W 00000000	ADRCCS19[R/W] B,H,W 00000000	
001430_H	ADRCCS20[R/W] B,H,W 00000000	ADRCCS21[R/W] B,H,W 00000000	ADRCCS22[R/W] B,H,W 00000000	ADRCCS23[R/W] B,H,W 00000000	
001434_H	ADRCCS24[R/W] B,H,W 00000000	ADRCCS25[R/W] B,H,W 00000000	ADRCCS26[R/W] B,H,W 00000000	ADRCCS27[R/W] B,H,W 00000000	
001438_H	ADRCCS28[R/W] B,H,W 00000000	ADRCCS29[R/W] B,H,W 00000000	ADRCCS30[R/W] B,H,W 00000000	ADRCCS31[R/W] B,H,W 00000000	
$00143C_H$	ADRCOT0[R] B,H,W 00000000 00000000 00000000 00000000				
001440_H	ADRCIF0[R,W] B,H,W 00000000 00000000 00000000 00000000				
001444_H	ADSCANS0[R/W] B,H,W 000-----	—	—	—	
001448_H	ADNCS0[R/W] B,H,W 0-000-00	ADNCS1[R/W] B,H,W 0-000-00	ADNCS2[R/W] B,H,W 0-000-00	ADNCS3[R/W] B,H,W 0-000-00	
$00144C_H$	ADNCS4[R/W] B,H,W 0-000-00	ADNCS5[R/W] B,H,W 0-000-00	ADNCS6[R/W] B,H,W 0-000-00	ADNCS7[R/W] B,H,W 0-000-00	
001450_H	ADNCS8[R/W] B,H,W 0-000-00	ADNCS9[R/W] B,H,W 0-000-00	ADNCS10[R/W] B,H,W 0-000-00	ADNCS11[R/W] B,H,W 0-000-00	
001454_H	ADNCS12[R/W] B,H,W 0-000-00	ADNCS13[R/W] B,H,W 0-000-00	ADNCS14[R/W] B,H,W 0-000-00	ADNCS15[R/W] B,H,W 0-000-00	
001458_H	ADPRTF0[R] B,H,W 00000000 00000000 00000000 00000000				
$00145C_H$	ADEOCF0[R] B,H,W 11111111 11111111 11111111 11111111				
001460_H	ADCS0[R] B,H,W 0------- --------		ADCH0[R] B,H,W ---00000	ADMD0[R/W] B,H,W 0---0000	
001464_H	ADSTPCS0[R/W] B,H,W 00000000	ADSTPCS1[R/W] B,H,W 00000000	ADSTPCS2[R/W] B,H,W 00000000	ADSTPCS3[R/W] B,H,W 00000000	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001468_H	ADSTPCS4[R/W] B,H,W 00000000	ADSTPCS5[R/W] B,H,W 00000000	ADSTPCS6[R/W] B,H,W 00000000	ADSTPCS7[R/W] B,H,W 00000000	12-bit A/D converter 1/2 unit
$00146C_H$	—				12-bit A/D converter 2/2 unit
001470_H	ADTSS1[R/W] B,H,W -------0	—	—	—	
001474_H	ADTSE1[R/W] B,H,W -------- -------- 00000000 00000000				
001478_H	ADCOMP32/ADCOMPB32[R/W] H,W 00000000 00000000		ADCOMP33/ADCOMPB33[R/W] H,W 00000000 00000000		
$00147C_H$	ADCOMP34/ADCOMPB34[R/W] H,W 00000000 00000000		ADCOMP35/ADCOMPB35[R/W] H,W 00000000 00000000		
001480_H	ADCOMP36/ADCOMPB36[R/W] H,W 00000000 00000000		ADCOMP37/ADCOMPB37[R/W] H,W 00000000 00000000		
001484_H	ADCOMP38/ADCOMPB38[R/W] H,W 00000000 00000000		ADCOMP39/ADCOMPB39[R/W] H,W 00000000 00000000		
001488_H	ADCOMP40/ADCOMPB40[R/W] H,W 00000000 00000000		ADCOMP41/ADCOMPB41[R/W] H,W 00000000 00000000		
$00148C_H$	ADCOMP42/ADCOMPB42[R/W] H,W 00000000 00000000		ADCOMP43/ADCOMPB43[R/W] H,W 00000000 00000000		
001490_H	ADCOMP44/ADCOMPB44[R/W] H,W 00000000 00000000		ADCOMP45/ADCOMPB45[R/W] H,W 00000000 00000000		
001494_H	ADCOMP46/ADCOMPB46[R/W] H,W 00000000 00000000		ADCOMP47/ADCOMPB47[R/W] H,W 00000000 00000000		
001498_H to $0014B4_H$	—	—	—	—	Reserved
$0014B8_H$	ADTCS32[R/W] B,H,W 00000000 0010----		ADTCS33[R/W] B,H,W 00000000 0010----		12-bit A/D converter 2/2 unit
$0014BC_H$	ADTCS34[R/W] B,H,W 00000000 0010----		ADTCS35[R/W] B,H,W 00000000 0010----		
$0014C0_H$	ADTCS36[R/W] B,H,W 00000000 0010----		ADTCS37[R/W] B,H,W 00000000 0010----		
$0014C4_H$	ADTCS38[R/W] B,H,W 00000000 0010----		ADTCS39[R/W] B,H,W 00000000 0010----		
$0014C8_H$	ADTCS40[R/W] B,H,W 00000000 0010----		ADTCS41[R/W] B,H,W 00000000 0010----		
$0014CC_H$	ADTCS42[R/W] B,H,W 00000000 0010----		ADTCS43[R/W] B,H,W 00000000 0010----		
$0014D0_H$	ADTCS44[R/W] B,H,W 00000000 0010----		ADTCS45[R/W] B,H,W 00000000 0010----		
$0014D4_H$	ADTCS46[R/W] B,H,W 00000000 0010----		ADTCS47[R/W] B,H,W 00000000 0010----		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$0014D8_H$ to $0014F4_H$	—	—	—	—	Reserved
$0014F8_H$	ADTCD32[R] B,H,W 10--0000 00000000		ADTCD33[R] B,H,W 10--0000 00000000		12-bit A/D converter 2/2 unit
$0014FC_H$	ADTCD34[R] B,H,W 10--0000 00000000		ADTCD35[R] B,H,W 10--0000 00000000		
001500_H	ADTCD36[R] B,H,W 10--0000 00000000		ADTCD37[R] B,H,W 10--0000 00000000		
001504_H	ADTCD38[R] B,H,W 10--0000 00000000		ADTCD39[R] B,H,W 10--0000 00000000		
001508_H	ADTCD40[R] B,H,W 10--0000 00000000		ADTCD41[R] B,H,W 10--0000 00000000		
$00150C_H$	ADTCD42[R] B,H,W 10--0000 00000000		ADTCD43[R] B,H,W 10--0000 00000000		
001510_H	ADTCD44[R] B,H,W 10--0000 00000000		ADTCD45[R] B,H,W 10--0000 00000000		
001514_H	ADTCD46[R] B,H,W 10--0000 00000000		ADTCD47[R] B,H,W 10--0000 00000000		
001518_H to 001534_H	—	—	—	—	Reserved
001538_H	ADTECS32[R/W] B,H,W -------0 ----0000		ADTECS33[R/W] B,H,W -------0 ----0000		12-bit A/D converter 2/2 unit
$00153C_H$	ADTECS34[R/W] B,H,W -------0 ----0000		ADTECS35[R/W] B,H,W -------0 ----0000		
001540_H	ADTECS36[R/W] B,H,W -------0 ----0000		ADTECS37[R/W] B,H,W -------0 ----0000		
001544_H	ADTECS38[R/W] B,H,W -------0 ----0000		ADTECS39[R/W] B,H,W -------0 ----0000		
001548_H	ADTECS40[R/W] B,H,W -------0 ----0000		ADTECS41[R/W] B,H,W -------0 ----0000		
$00154C_H$	ADTECS42[R/W] B,H,W -------0 ----0000		ADTECS43[R/W] B,H,W -------0 ----0000		
001550_H	ADTECS44[R/W] B,H,W -------0 ----0000		ADTECS45[R/W] B,H,W -------0 ----0000		
001554_H	ADTECS46[R/W] B,H,W -------0 ----0000		ADTECS47[R/W] B,H,W -------0 ----0000		
001558_H to 001574_H	—	—	—	—	Reserved
001578_H	ADRCUT4[R/W] B,H,W ----0000 00000000		ADRCLT4[R/W] B,H,W ----0000 00000000		12-bit A/D converter 2/2 unit
$00157C_H$	ADRCUT5[R/W] B,H,W ----0000 00000000		ADRCLT5[R/W] B,H,W ----0000 00000000		
001580_H	ADRCUT6[R/W] B,H,W ----0000 00000000		ADRCLT6[R/W] B,H,W ----0000 00000000		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001584_H	ADRCUT7[R/W] B,H,W ----0000 00000000		ADRCLT7[R/W] B,H,W ----0000 00000000		12-bit A/D converter 2/2 unit
001588_H	ADRCCS32[R/W] B,H,W 00000000	ADRCCS33[R/W] B,H,W 00000000	ADRCCS34[R/W] B,H,W 00000000	ADRCCS35[R/W] B,H,W 00000000	
$00158C_H$	ADRCCS36[R/W] B,H,W 00000000	ADRCCS37[R/W] B,H,W 00000000	ADRCCS38[R/W] B,H,W 00000000	ADRCCS39[R/W] B,H,W 00000000	
001590_H	ADRCCS40[R/W] B,H,W 00000000	ADRCCS41[R/W] B,H,W 00000000	ADRCCS42[R/W] B,H,W 00000000	ADRCCS43[R/W] B,H,W 00000000	
001594_H	ADRCCS44[R/W] B,H,W 00000000	ADRCCS45[R/W] B,H,W 00000000	ADRCCS46[R/W] B,H,W 00000000	ADRCCS47[R/W] B,H,W 00000000	
001598_H to $0015A4_H$	—	—	—	—	Reserved
$0015A8_H$	ADRCOT1 [R] B,H,W -------- -------- 00000000 00000000				12-bit A/D converter 2/2 unit
$0015AC_H$	ADRCIF1 [R,W] B,H,W -------- -------- 00000000 00000000				
$0015B0_H$	ADSCANS1 [R/W] B,H,W 000-----	—	—	—	
$0015B4_H$	ADNCS16 [R/W] B,H,W 0-000-00	ADNCS17 [R/W] B,H,W 0-000-00	ADNCS18 [R/W] B,H,W 0-000-00	ADNCS19 [R/W] B,H,W 0-000-00	
$0015B8_H$	ADNCS20 [R/W] B,H,W 0-000-00	ADNCS21 [R/W] B,H,W 0-000-00	ADNCS22 [R/W] B,H,W 0-000-00	ADNCS23 [R/W] B,H,W 0-000-00	
$0015BC_H$	—	—	—	—	
$0015C0_H$	—	—	—	—	
$0015C4_H$	ADPRTF1 [R] B,H,W -------- -------- 00000000 00000000				
$0015C8_H$	ADEOCF1 [R] B,H,W -------- -------- 11111111 11111111				
$0015CC_H$	ADCS1 [R] B,H,W 0------- --------		ADCH1 [R] B,H,W ---00000	ADMD1 [R/W] B,H,W 0---0000	
$0015D0_H$	ADSTPCS8 [R/W] B,H,W 00000000	ADSTPCS9 [R/W] B,H,W 00000000	ADSTPCS10 [R/W] B,H,W 00000000	ADSTPCS11 [R/W] B,H,W 00000000	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$0015D4_H$ to $00174C_H$	—	—	—	—	Reserved
001750_H	SCR0/(IBCR0)[R/W] B,H,W 0--00000	SMR0[R/W] B,H,W 000-00-0	SSR0[R/W] B,H,W 0-000011	ESCR0/(IBSR0)[R/W] B,H,W 00000000	Multi-UART0 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I^2C mode is not set immediately after reset. *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
001754_H	— /(RDR10/(TDR10))[R/W] B,H,W -------- -------- *3		RDR00/(TDR00)[R/W] B,H,W -------0 00000000 *1		
001758_H	SACSR0[R/W] B,H,W 0----000 00000000		STMR0[R] B,H,W 00000000 00000000		
$00175C_H$	STMCR0[R/W] B,H,W 00000000 00000000		— /(SCSCR0/SFUR0)[R/W] B,H,W -------- -------- *3 *4		
001760_H	— /(SCSTR30)/ (LAMSR0) [R/W] B,H,W -------- *3	— /(SCSTR20)/ (LAMCR0) [R/W] B,H,W -------- *3	— /(SCSTR10) /(SFLR10) [R/W] B,H,W -------- *3	— /(SCSTR00)/ (SFLR00) [R/W] B,H,W -------- *3	
001764_H	—	— /(SCSFR20) [R/W] B,H,W -------- *3	— /(SCSFR10) [R/W] B,H,W -------- *3	— /(SCSFR00) [R/W] B,H,W -------- *3	
001768_H	—/(TBYTE30)/ (LAMESR0) [R/W] B,H,W -------- *3	—/(TBYTE20) /(LAMERT0) [R/W] B,H,W -------- *3	—/(TBYTE10)/ (LAMIER0) [R/W] B,H,W -------- *3	TBYTE00/(LAMRID0) / (LAMTID0) [R/W] B,H,W 00000000	
$00176C_H$	BGR0[R/W] H, W 00000000 00000000		— /(ISMK0) [R/W] B,H,W -------- *2	— /(ISBA0) [R/W] B,H,W -------- *2	
001770_H	FCR10[R/W] B,H,W ---00100	FCR00[R/W] B,H,W -0000000	FBYTE0[R/W] B,H,W 00000000 00000000		
001774_H	FTICR0[R/W] B,H,W 00000000 00000000		—	—	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001778_H	SCR1/(IBCR1) [R/W] B,H,W 0--00000	SMR1[R/W] B,H,W 000-00-0	SSR1[R/W] B,H,W 0-000011	ESCR1/(IBSR1)[R/W] B,H,W 00000000	Multi-UART1 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I^2C mode is not set immediately after reset. *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
$00177C_H$	— /(RDR11/(TDR11))[R/W] B,H,W -------- -------- *3		RDR01/(TDR01)[R/W] B,H,W -------0 00000000 *1		
001780_H	SACSR1[R/W] B,H,W 0----000 00000000		STMR1[R] B,H,W 00000000 00000000		
001784_H	STMCR1[R/W] B,H,W 00000000 00000000		— /(SCSCR1/SFUR1)[R/W] B,H,W -------- -------- *3 *4		
001788_H	— /(SCSTR31)/ (LAMSR1) [R/W] B,H,W -------- *3	— /(SCSTR21)/ (LAMCR1) [R/W] B,H,W -------- *3	— /(SCSTR11)/ (SFLR11) [R/W] B,H,W -------- *3	— /(SCSTR01)/ (SFLR01) [R/W] B,H,W -------- *3	
$00178C_H$	—	— /(SCSFR21)[R/W] B,H,W -------- *3	— /(SCSFR11) [R/W] B,H,W -------- *3	— /(SCSFR01) [R/W] B,H,W -------- *3	
001790_H	—/(TBYTE31)/ (LAMESR1) [R/W] B,H,W -------- *3	—/(TBYTE21)/ (LAMERT1) [R/W] B,H,W -------- *3	—/(TBYTE11)/ (LAMIER1) [R/W] B,H,W -------- *3	TBYTE01/(LAMRID1) / (LAMTID1) [R/W] B,H,W 00000000	
001794_H	BGR1[R/W] H,W 00000000 00000000		— /(ISMK1)[R/W] B,H,W -------- *2	— /(ISBA1)[R/W] B,H,W -------- *2	
001798_H	FCR11[R/W] B,H,W ---00100	FCR01[R/W] B,H,W -0000000	FBYTE1[R/W] B,H,W 00000000 00000000		
$00179C_H$	FTICR1[R/W] B,H,W 00000000 00000000		—	—	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$0017A0_H$	SCR2/(IBCR2)[R/W] B,H,W 0--00000	SMR2[R/W] B,H,W 000-00-0	SSR2[R/W] B,H,W 0-000011	ESCR2/(IBSR2)[R/W] B,H,W 00000000	Multi-UART2 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I^2C mode is not set immediately after reset. *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
$0017A4_H$	— /(RDR12/(TDR12))[R/W] B,H,W -------- -------- *3		RDR02/(TDR02)[R/W] B,H,W -------0 00000000 *1		
$0017A8_H$	SACSR2[R/W] B,H,W 0----000 00000000		STMR2[R] B,H,W 00000000 00000000		
$0017AC_H$	STMCR2[R/W] B,H,W 00000000 00000000		— /(SCSCR2/SFUR2)[R/W] B,H,W -------- -------- *3 *4		
$0017B0_H$	— /(SCSTR32)/ (LAMSR2) [R/W] B,H,W -------- *3	— /(SCSTR22)/ (LAMCR2) [R/W] B,H,W -------- *3	— /(SCSTR12)/ (SFLR12) [R/W] B,H,W -------- *3	— /(SCSTR02)/ (SFLR02) [R/W] B,H,W -------- *3	
$0017B4_H$	—	— /(SCSFR22) [R/W] B,H,W -------- *3	— /(SCSFR12) [R/W] B,H,W -------- *3	— /(SCSFR02) [R/W] B,H,W -------- *3	
$0017B8_H$	—/(TBYTE32)/ (LAMESR2) [R/W] B,H,W -------- *3	—/(TBYTE22)/ (LAMERT2) [R/W] B,H,W -------- *3	—/(TBYTE12)/ (LAMIER2) [R/W] B,H,W -------- *3	TBYTE02/(LAMRID2) / (LAMTID2) [R/W] B,H,W 00000000	
$0017BC_H$	BGR2[R/W] H, W 00000000 00000000		— /(ISMK2)[R/W] B,H,W -------- *2	— /(ISBA2)[R/W] B,H,W -------- *2	
$0017C0_H$	FCR12[R/W] B,H,W ---00100	FCR02[R/W] B,H,W -0000000	FBYTE2[R/W] B,H,W 00000000 00000000		
$0017C4_H$	FTICR2[R/W] B,H,W 00000000 00000000		—	—	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
0017C8$_H$	SCR3/(IBCR3) [R/W] B,H,W 0--00000	SMR3[R/W] B,H,W 000-00-0	SSR3[R/W] B,H,W 0-000011	ESCR3/(IBSR3)[R/W] B,H,W 00000000	Multi-UART3 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I^{2}C mode is not set immediately after reset. *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
0017CC$_H$	— /(RDR13/(TDR13))[R/W] B,H,W -------- -------- *3		RDR03/(TDR03)[R/W] B,H,W -------0 00000000 *1		
0017D0$_H$	SACSR3[R/W] B,H,W 0----000 00000000		STMR3[R] B,H,W 00000000 00000000		
0017D4$_H$	STMCR3[R/W] B,H,W 00000000 00000000		— /(SCSCR3/SFUR3)[R/W] B,H,W -------- -------- *3 *4		
0017D8$_H$	— /(SCSTR33)/ (LAMSR3) [R/W] B,H,W -------- *3	— /(SCSTR23)/ (LAMCR3) [R/W] B,H,W -------- *3	— /(SCSTR13)/ (SFLR13) [R/W] B,H,W -------- *3	— /(SCSTR03)/ (SFLR03) [R/W] B,H,W -------- *3	
0017DC$_H$	—	— /(SCSFR23) [R/W] B,H,W -------- *3	— /(SCSFR13) [R/W] B,H,W -------- *3	— /(SCSFR03) [R/W] B,H,W -------- *3	
0017E0$_H$	—/(TBYTE33)/ (LAMESR3) [R/W] B,H,W -------- *3	—/(TBYTE23)/ (LAMERT3) [R/W] B,H,W -------- *3	—/(TBYTE13)/ (LAMIER3) [R/W] B,H,W -------- *3	TBYTE03/(LAMRID3) / (LAMTID3) [R/W] B,H,W 00000000	
0017E4$_H$	BGR3[R/W] H, W 00000000 00000000		— /(ISMK3)[R/W] B,H,W -------- *2	— /(ISBA3)[R/W] B,H,W -------- *2	
0017E8$_H$	FCR13[R/W] B,H,W ---00100	FCR03[R/W] B,H,W -0000000	FBYTE3[R/W] B,H,W 00000000 00000000		
0017EC$_H$	FTICR3[R/W] B,H,W 00000000 00000000		—	—	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$0017F0_H$	SCR4/(IBCR4) [R/W] B,H,W 0--00000	SMR4[R/W] B,H,W 000-00-0	SSR4[R/W] B,H,W 0-000011	ESCR4/(IBSR4)[R/W] B,H,W 00000000	Multi-UART4 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I^2C mode is not set immediately after reset. *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
$0017F4_H$	— /(RDR14/(TDR14))[R/W] B,H,W -------- -------- *3		RDR04/(TDR04)[R/W] B,H,W -------0 00000000 *1		
$0017F8_H$	SACSR4[R/W] B,H,W 0----000 00000000		STMR4[R] B,H,W 00000000 00000000		
$0017FC_H$	STMCR4[R/W] B,H,W 00000000 00000000		— /(SCSCR4/SFUR4)[R/W] B,H,W -------- -------- *3 *4		
001800_H	— /(SCSTR34)/ (LAMSR4) [R/W] B,H,W -------- *3	— /(SCSTR24)/ (LAMCR4) [R/W] B,H,W -------- *3	— /(SCSTR14)/ (SFLR14) [R/W] B,H,W -------- *3	— /(SCSTR04)/ (SFLR04) [R/W] B,H,W -------- *3	
001804_H	—	— /(SCSFR24) [R/W] B,H,W -------- *3	— /(SCSFR14) [R/W] B,H,W -------- *3	— /(SCSFR04) [R/W] B,H,W -------- *3	
001808_H	—/(TBYTE34)/ (LAMESR4) [R/W] B,H,W -------- *3	—/(TBYTE24)/ (LAMERT4) [R/W] B,H,W -------- *3	—/(TBYTE14)/ (LAMIER4) [R/W] B,H,W -------- *3	TBYTE04/(LAMRID4) / (LAMTID4) [R/W] B,H,W 00000000	
$00180C_H$	BGR4[R/W] H, W 00000000 00000000		— /(ISMK4)[R/W] B,H,W -------- *2	— /(ISBA4)[R/W] B,H,W -------- *2	
001810_H	FCR14[R/W] B,H,W ---00100	FCR04[R/W] B,H,W -0000000	FBYTE4[R/W] B,H,W 00000000 00000000		
001814_H	FTICR4[R/W] B,H,W 00000000 00000000		—	—	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001818_H	SCR5/(IBCR5) [R/W] B,H,W 0--00000	SMR5[R/W] B,H,W 000-00-0	SSR5[R/W] B,H,W 0-000011	ESCR5/(IBSR5)[R/W] B,H,W 00000000	Multi-UART5 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I^2C mode is not set immediately after reset. *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
$00181C_H$	— /(RDR15/(TDR15))[R/W] B,H,W -------- -------- *3		RDR05/(TDR05)[R/W] B,H,W -------0 00000000 *1		
001820_H	SACSR5[R/W] B,H,W 0----000 00000000		STMR5[R] B,H,W 00000000 00000000		
001824_H	STMCR5[R/W] B,H,W 00000000 00000000		— /(SCSCR5/SFUR5)[R/W] B,H,W -------- -------- *3 *4		
001828_H	— /(SCSTR35)/ (LAMSR5) [R/W] B,H,W -------- *3	— /(SCSTR25)/ (LAMCR5) [R/W] B,H,W -------- *3	— /(SCSTR15)/ (SFLR15) [R/W] B,H,W -------- *3	— /(SCSTR05)/ (SFLR05) [R/W] B,H,W -------- *3	
$00182C_H$	—	— /(SCSFR25) [R/W] B,H,W -------- *3	— /(SCSFR15) [R/W] B,H,W -------- *3	— /(SCSFR05) [R/W] B,H,W -------- *3	
001830_H	—/(TBYTE35)/ (LAMESR5) [R/W] B,H,W -------- *3	—/(TBYTE25)/ (LAMERT5) [R/W] B,H,W -------- *3	—/(TBYTE15)/ (LAMIER5) [R/W] B,H,W -------- *3	TBYTE05/(LAMRID5) / (LAMTID5) [R/W] B,H,W 00000000	
001834_H	BGR5[R/W] H, W 00000000 00000000		— /(ISMK5)[R/W] B,H,W -------- *2	— /(ISBA5)[R/W] B,H,W -------- *2	
001838_H	FCR15[R/W] B,H,W ---00100	FCR05[R/W] B,H,W -0000000	FBYTE5[R/W] B,H,W 00000000 00000000		
$00183C_H$	FTICR5[R/W] B,H,W 00000000 00000000		—	—	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001840_H	SCR6/(IBCR6) [R/W] B,H,W 0--00000	SMR6[R/W] B,H,W 000-00-0	SSR6[R/W] B,H,W 0-000011	ESCR6/(IBSR6)[R/W] B,H,W 00000000	Multi-UART6 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I^2C mode is not set immediately after reset. *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
001844_H	— /(RDR16/(TDR16))[R/W] B,H,W -------- -------- *3		RDR06/(TDR06)[R/W] B,H,W -------0 00000000 *1		
001848_H	SACSR6[R/W] B,H,W 0----000 00000000		STMR6[R] B,H,W 00000000 00000000		
$00184C_H$	STMCR6[R/W] B,H,W 00000000 00000000		— /(SCSCR6/SFUR6)[R/W] B,H,W -------- -------- *3 *4		
001850_H	— /(SCSTR36)/ (LAMSR6) [R/W] B,H,W -------- *3	— /(SCSTR26)/ (LAMCR6) [R/W] B,H,W -------- *3	— /(SCSTR16)/ (SFLR16) [R/W] B,H,W -------- *3	— /(SCSTR06)/ (SFLR06) [R/W] B,H,W -------- *3	
001854_H	—	— /(SCSFR26) [R/W] B,H,W -------- *3	— /(SCSFR16) [R/W] B,H,W -------- *3	— /(SCSFR06) [R/W] B,H,W -------- *3	
001858_H	—/(TBYTE36)/ (LAMESR6) [R/W] B,H,W -------- *3	—/(TBYTE26)/ (LAMERT6) [R/W] B,H,W -------- *3	—/(TBYTE16)/ (LAMIER6) [R/W] B,H,W -------- *3	TBYTE06/(LAMRID6) / (LAMTID6) [R/W] B,H,W 00000000	
$00185C_H$	BGR6[R/W] H, W 00000000 00000000		— /(ISMK6)[R/W] B,H,W -------- *2	— /(ISBA6)[R/W] B,H,W -------- *2	
001860_H	FCR16[R/W] B,H,W ---00100	FCR06[R/W] B,H,W -0000000	FBYTE6[R/W] B,H,W 00000000 00000000		
001864_H	FTICR6[R/W] B,H,W 00000000 00000000		—	—	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001868_H	SCR7/(IBCR7) [R/W] B,H,W 0--00000	SMR7[R/W] B,H,W 000-00-0	SSR7[R/W] B,H,W 0-000011	ESCR7/(IBSR7)[R/W] B,H,W 00000000	Multi-UART7 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I^2C mode is not set immediately after reset. *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
$00186C_H$	— /(RDR17/(TDR17))[R/W] B,H,W -------- -------- *3		RDR07/(TDR07)[R/W] B,H,W -------0 00000000 *1		
001870_H	SACSR7[R/W] B,H,W 0----000 00000000		STMR7[R] B,H,W 00000000 00000000		
001874_H	STMCR7[R/W] B,H,W 00000000 00000000		— /(SCSCR7/SFUR7)[R/W] B,H,W -------- -------- *3 *4		
001878_H	— /(SCSTR37)/ (LAMSR7) [R/W] B,H,W -------- *3	— /(SCSTR27)/ (LAMCR7) [R/W] B,H,W -------- *3	— /(SCSTR17)/ (SFLR17) [R/W] B,H,W -------- *3	— /(SCSTR07)/ (SFLR07) [R/W] B,H,W -------- *3	
$00187C_H$	—	— /(SCSFR27) [R/W] B,H,W -------- *3	— /(SCSFR17) [R/W] B,H,W -------- *3	— /(SCSFR07) [R/W] B,H,W -------- *3	
001880_H	—/(TBYTE37)/ (LAMESR7) [R/W] B,H,W -------- *3	—/(TBYTE27)/ (LAMERT7) [R/W] B,H,W -------- *3	—/(TBYTE17)/ (LAMIER7) [R/W] B,H,W -------- *3	TBYTE07/(LAMRID7) / (LAMTID7) [R/W] B,H,W 00000000	
001884_H	BGR7[R/W] H, W 00000000 00000000		— /(ISMK7)[R/W] B,H,W -------- *2	— /(ISBA7)[R/W] B,H,W -------- *2	
001888_H	FCR17[R/W] B,H,W ---00100	FCR07[R/W] B,H,W -0000000	FBYTE7[R/W] B,H,W 00000000 00000000		
$00188C_H$	FTICR7[R/W] B,H,W 00000000 00000000		—	—	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001890_H	SCR8/(IBCR8) [R/W] B,H,W 0--00000	SMR8[R/W] B,H,W 000-00-0	SSR8[R/W] B,H,W 0-000011	ESCR8/(IBSR8)[R/W] B,H,W 00000000	Multi-UART8 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I^2C mode is not set immediately after reset. *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
001894_H	— /(RDR18/(TDR18))[R/W] B,H,W -------- -------- *3		RDR08/(TDR08)[R/W] B,H,W -------0 00000000 *1		
001898_H	SACSR8[R/W] B,H,W 0----000 00000000		STMR8[R] B,H,W 00000000 00000000		
$00189C_H$	STMCR8[R/W] B,H,W 00000000 00000000		— /(SCSCR8/SFUR8)[R/W] B,H,W -------- -------- *3 *4		
$0018A0_H$	— /(SCSTR38)/ (LAMSR8) [R/W] B,H,W -------- *3	— /(SCSTR28)/ (LAMCR8) [R/W] B,H,W -------- *3	— /(SCSTR18)/ (SFLR18) [R/W] B,H,W -------- *3	— /(SCSTR08)/ (SFLR08) [R/W] B,H,W -------- *3	
$0018A4_H$	—	— /(SCSFR28) [R/W] B,H,W -------- *3	— /(SCSFR18) [R/W] B,H,W -------- *3	— /(SCSFR08) [R/W] B,H,W -------- *3	
$0018A8_H$	—/(TBYTE38)/ (LAMESR8) [R/W] B,H,W -------- *3	—/(TBYTE28)/ (LAMERT8) [R/W] B,H,W -------- *3	—/(TBYTE18)/ (LAMIER8) [R/W] B,H,W -------- *3	TBYTE08/(LAMRID8) / (LAMTID8) [R/W] B,H,W 00000000	
$0018AC_H$	BGR8[R/W] H,W 00000000 00000000		— /(ISMK8)[R/W] B,H,W -------- *2	— /(ISBA8)[R/W] B,H,W -------- *2	
$0018B0_H$	FCR18[R/W] B,H,W ---00100	FCR08[R/W] B,H,W -0000000	FBYTE8[R/W] B,H,W 00000000 00000000		
$0018B4_H$	FTICR8[R/W] B,H,W 00000000 00000000		—	—	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
0018B8$_H$	SCR9/(IBCR9) [R/W] B,H,W 0--00000	SMR9[R/W] B,H,W 000-00-0	SSR9[R/W] B,H,W 0-000011	ESCR9/(IBSR9)[R/W] B,H,W 00000000	Multi-UART9 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I^{2}C mode is not set immediately after reset. *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
0018BC$_H$	— /(RDR19/(TDR19))[R/W] B,H,W -------- -------- *3		RDR09/(TDR09)[R/W] B,H,W -------0 00000000 *1		
0018C0$_H$	SACSR9[R/W] B,H,W 0----000 00000000		STMR9[R] B,H,W 00000000 00000000		
0018C4$_H$	STMCR9[R/W] B,H,W 00000000 00000000		— /(SCSCR9/SFUR9)[R/W] B,H,W -------- -------- *3 *4		
0018C8$_H$	— /(SCSTR39)/ (LAMSR9) [R/W] B,H,W -------- *3	— /(SCSTR29)/ (LAMCR9) [R/W] B,H,W -------- *3	— /(SCSTR19)/ (SFLR19) [R/W] B,H,W -------- *3	— /(SCSTR09)/ (SFLR09) [R/W] B,H,W -------- *3	
0018CC$_H$	—	— /(SCSFR29) [R/W] B,H,W -------- *3	— /(SCSFR19) [R/W] B,H,W -------- *3	— /(SCSFR09) [R/W] B,H,W -------- *3	
0018D0$_H$	—/(TBYTE39)/ (LAMESR9) [R/W] B,H,W -------- *3	—/(TBYTE29)/ (LAMERT9) [R/W] B,H,W -------- *3	—/(TBYTE19)/ (LAMIER9) [R/W] B,H,W -------- *3	TBYTE09/(LAMRID9) / (LAMTID9) [R/W] B,H,W 00000000	
0018D4$_H$	BGR9[R/W] H, W 00000000 00000000		— /(ISMK9)[R/W] B,H,W -------- *2	— /(ISBA9)[R/W] B,H,W -------- *2	
0018D8$_H$	FCR19[R/W] B,H,W ---00100	FCR09[R/W] B,H,W -0000000	FBYTE9[R/W] B,H,W 00000000 00000000		
0018DC$_H$	FTICR9[R/W] B,H,W 00000000 00000000		—	—	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$0018E0_H$	SCR10/(IBCR10) [R/W] B,H,W 0--00000	SMR10[R/W] B,H,W 000-00-0	SSR10[R/W] B,H,W 0-000011	ESCR10/(IBSR10) [R/W] B,H,W 00000000	Multi-UART10 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I^2C mode is not set immediately after reset. *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
$0018E4_H$	— /(RDR110/(TDR110))[R/W] B,H,W -------- -------- *3		RDR010/(TDR010)[R/W] B,H,W -------0 00000000 *1		
$0018E8_H$	SACSR10[R/W] B,H,W 0----000 00000000		STMR10[R] B,H,W 00000000 00000000		
$0018EC_H$	STMCR10[R/W] B,H,W 00000000 00000000		— /(SCSCR10/SFUR10)[R/W] B,H,W -------- -------- *3 *4		
$0018F0_H$	— /(SCSTR310)/ (LAMSR10) [R/W] B,H,W -------- *3	— /(SCSTR210)/ (LAMCR10) [R/W] B,H,W -------- *3	— /(SCSTR110)/ (SFLR110)[R/W] B,H,W -------- *3	— /(SCSTR010)/ (SFLR010)[R/W] B,H,W -------- *3	
$0018F4_H$	—	— /(SCSFR210) [R/W] B,H,W -------- *3	— /(SCSFR110) [R/W] B,H,W -------- *3	— /(SCSFR010) [R/W] B,H,W -------- *3	
$0018F8_H$	—/(TBYTE310)/ (LAMESR10) [R/W] B,H,W -------- *3	—/(TBYTE210)/ (LAMERT10) [R/W] B,H,W -------- *3	—/(TBYTE110)/ (LAMIER10) [R/W] B,H,W -------- *3	TBYTE010/(LAMRID 10)/(LAMTID10) [R/W] B,H,W 00000000	
$0018FC_H$	BGR10[R/W] H, W 00000000 00000000		— /(ISMK10)[R/W] B,H,W -------- *2	— /(ISBA10)[R/W] B,H,W -------- *2	
001900_H	FCR110[R/W] B,H,W ---00100	FCR010[R/W] B,H,W -0000000	FBYTE10[R/W] B,H,W 00000000 00000000		
001904_H	FTICR10[R/W] B,H,W 00000000 00000000		—	—	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001908_H	SCR11/(IBCR11) [R/W] B,H,W 0--00000	SMR11[R/W] B,H,W 000-00-0	SSR11[R/W] B,H,W 0-000011	ESCR11/(IBSR11) [R/W] B,H,W 00000000	Multi-UART11 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I^2C mode is not set immediately after reset. *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
$00190C_H$	— /(RDR111/(TDR111))[R/W] B,H,W -------- -------- *3		RDR011/(TDR011)[R/W] B,H,W -------0 00000000 *1		
001910_H	SACSR11[R/W] B,H,W 0----000 00000000		STMR11[R] B,H,W 00000000 00000000		
001914_H	STMCR11[R/W] B,H,W 00000000 00000000		— /(SCSCR11/SFUR11)[R/W] B,H,W -------- -------- *3 *4		
001918_H	— /(SCSTR311)/ (LAMSR11) [R/W] B,H,W -------- *3	— /(SCSTR211)/ (LAMCR11) [R/W] B,H,W -------- *3	— /(SCSTR111)/ (SFLR111)[R/W] B,H,W -------- *3	— /(SCSTR011)/ (SFLR011)[R/W] B,H,W -------- *3	
$00191C_H$	—	— /(SCSFR211) [R/W] B,H,W -------- *3	— /(SCSFR111) [R/W] B,H,W -------- *3	— /(SCSFR011) [R/W] B,H,W -------- *3	
001920_H	—/(TBYTE311)/ (LAMESR11) [R/W] B,H,W -------- *3	—/(TBYTE211)/ (LAMERT11) [R/W] B,H,W -------- *3	—/(TBYTE111)/ (LAMIER11) [R/W] B,H,W -------- *3	TBYTE011/(LAMRID 11)/(LAMTID11) [R/W] B,H,W 00000000	
001924_H	BGR11[R/W] H, W 00000000 00000000		— /(ISMK11)[R/W] B,H,W -------- *2	— /(ISBA11)[R/W] B,H,W -------- *2	
001928_H	FCR111[R/W] B,H,W ---00100	FCR011[R/W] B,H,W -0000000	FBYTE11[R/W] B,H,W 00000000 00000000		
$00192C_H$	FTICR11[R/W] B,H,W 00000000 00000000		—	—	
001930_H to $0019D8_H$	—	—	—	—	Reserved
$0019DC_H$	—	GATEC0 [R/W] B,H,W ------00	—	GATEC2 [R/W] B,H,W ------00	PPG GATE control
$0019E0_H$	—	GATEC4 [R/W] B,H,W ------00	—	—	
$0019E4_H$	—	—	—	—	Reserved
$0019E8_H$	GTRS0 [R/W] B,H,W -0000000 -0000000		GTRS1 [R/W] B,H,W -0000000 -0000000		PPG controller
$0019EC_H$	GTRS2 [R/W] B,H,W -0000000 -0000000		GTRS3 [R/W] B,H,W -0000000 -0000000		
$0019F0_H$	GTRS4 [R/W] B,H,W -0000000 -0000000		GTRS5 [R/W] B,H,W -0000000 -0000000		
$0019F4_H$	GTRS6 [R/W] B,H,W -0000000 -0000000		GTRS7 [R/W] B,H,W -0000000 -0000000		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$0019F8_H$	GTRS8 [R/W] B,H,W -0000000 -0000000		GTRS9 [R/W] B,H,W -0000000 -0000000		PPG controller
$0019FC_H$	GTRS10 [R/W] B,H,W -0000000 -0000000		GTRS11 [R/W] B,H,W -0000000 -0000000		
$001A00_H$	GTRS12 [R/W] B,H,W -0000000 -0000000		GTRS13 [R/W] B,H,W -0000000 -0000000		
$001A04_H$	GTRS14 [R/W] B,H,W -0000000 -0000000		GTRS15 [R/W] B,H,W -0000000 -0000000		
$001A08_H$	GTRS16 [R/W] B,H,W -0000000 -0000000		GTRS17 [R/W] B,H,W -0000000 -0000000		
$001A0C_H$	GTRS18 [R/W] B,H,W -0000000 -0000000		GTRS19 [R/W] B,H,W -0000000 -0000000		
$001A10_H$	GTRS20 [R/W] B,H,W -0000000 -0000000		GTRS21 [R/W] B,H,W -0000000 -0000000		
$001A14_H$	GTRS22 [R/W] B,H,W -0000000 -0000000		GTRS23 [R/W] B,H,W -0000000 -0000000		
$001A18_H$ to $001A2C_H$	—	—	—	—	Reserved
$001A30_H$	—	—	—	—	Reserved
$001A34_H$	—	—	—	—	
$001A38_H$	GTREN0 [R/W] H,W 00000000 00000000		GTREN1 [R/W] H,W 00000000 00000000		PPG controller
$001A3C_H$	GTREN2 [R/W] H,W 00000000 00000000		—	—	
$001A40_H$	PCN0 [R/W] B,H,W 00000000 000000-0		PCSR0 [W] H,W XXXXXXXX XXXXXXXX		PPG0 * for communication
$001A44_H$	PDUT0 [W] H,W XXXXXXXX XXXXXXXX		PTMR0 [R] H,W 11111111 11111111		
$001A48_H$	PCN200 [R/W] B,H,W --000000 -----110		PSDR0 [R/W] H,W 00000000 00000000		
$001A4C_H$	PTPC0 [R/W] H,W 00000000 00000000		PCMDWD0 [R/W] B,H,W -------- ----0000		
$001A50_H$	PHCSR0 [W] H,W XXXXXXXX XXXXXXXX		PLCSR0 [W] H,W XXXXXXXX XXXXXXXX		
$001A54_H$	PHDUT0 [W] H,W XXXXXXXX XXXXXXXX		PLDUT0 [W] H,W XXXXXXXX XXXXXXXX		
$001A58_H$	PCMDDT0 [R/W] H,W 00000000 00000000		—	—	
$001A5C_H$	PCN1 [R/W] B,H,W 00000000 000000-0		PCSR1 [W] H,W XXXXXXXX XXXXXXXX		PPG1 * for communication
$001A60_H$	PDUT1 [W] H,W XXXXXXXX XXXXXXXX		PTMR1 [R] H,W 11111111 11111111		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$001A64_H$	PCN201 [R/W] B,H,W --000000 -----110		PSDR1 [R/W] H,W 00000000 00000000		PPG1 * for communication
$001A68_H$	PTPC1 [R/W] H,W 00000000 00000000		PCMDWD1 [R/W] B,H,W -------- ----0000		
$001A6C_H$	PHCSR1 [W] H,W XXXXXXXX XXXXXXXX		PLCSR1 [W] H,W XXXXXXXX XXXXXXXX		
$001A70_H$	PHDUT1 [W] H,W XXXXXXXX XXXXXXXX		PLDUT1 [W] H,W XXXXXXXX XXXXXXXX		
$001A74_H$	PCMDDT1 [R/W] H,W 00000000 00000000		—	—	
$001A78_H$	PCN2 [R/W] B,H,W 00000000 000000-0		PCSR2 [W] H,W XXXXXXXX XXXXXXXX		PPG2 * for communication
$001A7C_H$	PDUT2 [W] H,W XXXXXXXX XXXXXXXX		PTMR2 [R] H,W 11111111 11111111		
$001A80_H$	PCN202 [R/W] B,H,W --000000 -----110		PSDR2 [R/W] H,W 00000000 00000000		
$001A84_H$	PTPC2 [R/W] H,W 00000000 00000000		PCMDWD2 [R/W] B,H,W -------- ----0000		
$001A88_H$	PHCSR2 [W] H,W XXXXXXXX XXXXXXXX		PLCSR2 [W] H,W XXXXXXXX XXXXXXXX		
$001A8C_H$	PHDUT2 [W] H,W XXXXXXXX XXXXXXXX		PLDUT2 [W] H,W XXXXXXXX XXXXXXXX		
$001A90_H$	PCMDDT2 [R/W] H,W 00000000 00000000		—	—	
$001A94_H$	PCN3 [R/W] B,H,W 00000000 000000-0		PCSR3 [W] H,W XXXXXXXX XXXXXXXX		PPG3 * for communication
$001A98_H$	PDUT3 [W] H,W XXXXXXXX XXXXXXXX		PTMR3 [R] H,W 11111111 11111111		
$001A9C_H$	PCN203 [R/W] B,H,W --000000 -----110		PSDR3 [R/W] H,W 00000000 00000000		
$001AA0_H$	PTPC3 [R/W] H,W 00000000 00000000		PCMDWD3 [R/W] B,H,W -------- ----0000		
$001AA4_H$	PHCSR3 [W] H,W XXXXXXXX XXXXXXXX		PLCSR3 [W] H,W XXXXXXXX XXXXXXXX		
$001AA8_H$	PHDUT3 [W] H,W XXXXXXXX XXXXXXXX		PLDUT3 [W] H,W XXXXXXXX XXXXXXXX		
$001AAC_H$	PCMDDT3 [R/W] H,W 00000000 00000000		—	—	
$001AB0_H$	PCN4 [R/W] B,H,W 00000000 000000-0		PCSR4 [W] H,W XXXXXXXX XXXXXXXX		PPG4
$001AB4_H$	PDUT4 [W] H,W XXXXXXXX XXXXXXXX		PTMR4 [R] H,W 11111111 11111111		
$001AB8_H$	PCN204 [R/W] B,H,W --000000 -----110		PSDR4 [R/W] H,W 00000000 00000000		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$001ABC_H$	PTPC4 [R/W] H,W 00000000 00000000		—	—	PPG4
$001AC0_H$	PCN5 [R/W] B,H,W 00000000 000000-0		PCSR5 [W] H,W XXXXXXXX XXXXXXXX		PPG5
$001AC4_H$	PDUT5 [W] H,W XXXXXXXX XXXXXXXX		PTMR5 [R] H,W 11111111 11111111		
$001AC8_H$	PCN205 [R/W] B,H,W --000000 -----110		PSDR5 [R/W] H,W 00000000 00000000		
$001ACC_H$	PTPC5 [R/W] H,W 00000000 00000000		—	—	
$001AD0_H$	PCN6 [R/W] B,H,W 00000000 000000-0		PCSR6 [W] H,W XXXXXXXX XXXXXXXX		PPG6
$001AD4_H$	PDUT6 [W] H,W XXXXXXXX XXXXXXXX		PTMR6 [R] H,W 11111111 11111111		
$001AD8_H$	PCN206 [R/W] B,H,W --000000 -----110		PSDR6 [R/W] H,W 00000000 00000000		
$001ADC_H$	PTPC6 [R/W] H,W 00000000 00000000		—	—	
$001AE0_H$	PCN7 [R/W] B,H,W 00000000 000000-0		PCSR7 [W] H,W XXXXXXXX XXXXXXXX		PPG7
$001AE4_H$	PDUT7 [W] H,W XXXXXXXX XXXXXXXX		PTMR7 [R] H,W 11111111 11111111		
$001AE8_H$	PCN207 [R/W] B,H,W --000000 -----110		PSDR7 [R/W] H,W 00000000 00000000		
$001AEC_H$	PTPC7 [R/W] H,W 00000000 00000000		—	—	
$001AF0_H$	PCN8 [R/W] B,H,W 00000000 000000-0		PCSR8 [W] H,W XXXXXXXX XXXXXXXX		PPG8
$001AF4_H$	PDUT8 [W] H,W XXXXXXXX XXXXXXXX		PTMR8 [R] H,W 11111111 11111111		
$001AF8_H$	PCN208 [R/W] B,H,W --000000 -----110		PSDR8 [R/W] H,W 00000000 00000000		
$001AFC_H$	PTPC8 [R/W] H,W 00000000 00000000		—	—	
$001B00_H$	PCN9 [R/W] B,H,W 00000000 000000-0		PCSR9 [W] H,W XXXXXXXX XXXXXXXX		PPG9
$001B04_H$	PDUT9 [W] H,W XXXXXXXX XXXXXXXX		PTMR9 [R] H,W 11111111 11111111		
$001B08_H$	PCN209 [R/W] B,H,W --000000 -----110		PSDR9 [R/W] H,W 00000000 00000000		
$001B0C_H$	PTPC9 [R/W] H,W 00000000 00000000		—	—	
$001B10_H$	PCN10 [R/W] B,H,W 00000000 000000-0		PCSR10 [W] H,W XXXXXXXX XXXXXXXX		PPG10
$001B14_H$	PDUT10 [W] H,W XXXXXXXX XXXXXXXX		PTMR10 [R] H,W 11111111 11111111		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$001B18_H$	PCN210 [R/W] B,H,W --000000 -----110		PSDR10 [R/W] H,W 00000000 00000000		PPG10
$001B1C_H$	PTPC10 [R/W] H,W 00000000 00000000		—	—	
$001B20_H$	PCN11 [R/W] B,H,W 00000000 000000-0		PCSR11 [W] H,W XXXXXXXX XXXXXXXX		PPG11
$001B24_H$	PDUT11 [W] H,W XXXXXXXX XXXXXXXX		PTMR11 [R] H,W 11111111 11111111		
$001B28_H$	PCN211 [R/W] B,H,W --000000 -----110		PSDR11 [R/W] H,W 00000000 00000000		
$001B2C_H$	PTPC11 [R/W] H,W 00000000 00000000		—	—	
$001B30_H$	PCN12 [R/W] B,H,W 00000000 000000-0		PCSR12 [W] H,W XXXXXXXX XXXXXXXX		PPG12
$001B34_H$	PDUT12 [W] H,W XXXXXXXX XXXXXXXX		PTMR12 [R] H,W 11111111 11111111		
$001B38_H$	PCN212 [R/W] B,H,W --000000 -----110		PSDR12 [R/W] H,W 00000000 00000000		
$001B3C_H$	PTPC12 [R/W] H,W 00000000 00000000		—	—	
$001B40_H$	PCN13 [R/W] B,H,W 00000000 000000-0		PCSR13 [W] H,W XXXXXXXX XXXXXXXX		PPG13
$001B44_H$	PDUT13 [W] H,W XXXXXXXX XXXXXXXX		PTMR13 [R] H,W 11111111 11111111		
$001B48_H$	PCN213 [R/W] B,H,W --000000 -----110		PSDR13 [R/W] H,W 00000000 00000000		
$001B4C_H$	PTPC13 [R/W] H,W 00000000 00000000		—	—	
$001B50_H$	PCN14 [R/W] B,H,W 00000000 000000-0		PCSR14 [W] H,W XXXXXXXX XXXXXXXX		PPG14
$001B54_H$	PDUT14 [W] H,W XXXXXXXX XXXXXXXX		PTMR14 [R] H,W 11111111 11111111		
$001B58_H$	PCN214 [R/W] B,H,W --000000 -----110		PSDR14 [R/W] H,W 00000000 00000000		
$001B5C_H$	PTPC14 [R/W] H,W 00000000 00000000		—	—	
$001B60_H$	PCN15 [R/W] B,H,W 00000000 000000-0		PCSR15 [W] H,W XXXXXXXX XXXXXXXX		PPG15
$001B64_H$	PDUT15 [W] H,W XXXXXXXX XXXXXXXX		PTMR15 [R] H,W 11111111 11111111		
$001B68_H$	PCN215 [R/W] B,H,W --000000 -----110		PSDR15 [R/W] H,W 00000000 00000000		
$001B6C_H$	PTPC15 [R/W] H,W 00000000 00000000		—	—	
$001B70_H$	PCN16 [R/W] B,H,W 00000000 000000-0		PCSR16 [W] H,W XXXXXXXX XXXXXXXX		PPG16

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$001B74_H$	PDUT16 [W] H,W XXXXXXXX XXXXXXXX		PTMR16 [R] H,W 11111111 11111111		PPG16
$001B78_H$	PCN216 [R/W] B,H,W --000000 -----110		PSDR16 [R/W] H,W 00000000 00000000		
$001B7C_H$	PTPC16 [R/W] H,W 00000000 00000000		—	—	
$001B80_H$	PCN17 [R/W] B,H,W 00000000 000000-0		PCSR17 [W] H,W XXXXXXXX XXXXXXXX		PPG17
$001B84_H$	PDUT17 [W] H,W XXXXXXXX XXXXXXXX		PTMR17 [R] H,W 11111111 11111111		
$001B88_H$	PCN217 [R/W] B,H,W --000000 -----110		PSDR17 [R/W] H,W 00000000 00000000		
$001B8C_H$	PTPC17 [R/W] H,W 00000000 00000000		—	—	
$001B90_H$	PCN18 [R/W] B,H,W 00000000 000000-0		PCSR18 [W] H,W XXXXXXXX XXXXXXXX		PPG18
$001B94_H$	PDUT18 [W] H,W XXXXXXXX XXXXXXXX		PTMR18 [R] H,W 11111111 11111111		
$001B98_H$	PCN218 [R/W] B,H,W --000000 -----110		PSDR18 [R/W] H,W 00000000 00000000		
$001B9C_H$	PTPC18 [R/W] H,W 00000000 00000000		—	—	
$001BA0_H$	PCN19 [R/W] B,H,W 00000000 000000-0		PCSR19 [W] H,W XXXXXXXX XXXXXXXX		PPG19
$001BA4_H$	PDUT19 [W] H,W XXXXXXXX XXXXXXXX		PTMR19 [R] H,W 11111111 11111111		
$001BA8_H$	PCN219 [R/W] B,H,W --000000 -----110		PSDR19 [R/W] H,W 00000000 00000000		
$001BAC_H$	PTPC19 [R/W] H,W 00000000 00000000		—	—	
$001BB0_H$	PCN20 [R/W] B,H,W 00000000 000000-0		PCSR20 [W] H,W XXXXXXXX XXXXXXXX		PPG20
$001BB4_H$	PDUT20 [W] H,W XXXXXXXX XXXXXXXX		PTMR20 [R] H,W 11111111 11111111		
$001BB8_H$	PCN220 [R/W] B,H,W --000000 -----110		PSDR20 [R/W] H,W 00000000 00000000		
$001BBC_H$	PTPC20 [R/W] H,W 00000000 00000000		—	—	
$001BC0_H$	PCN21 [R/W] B,H,W 00000000 000000-0		PCSR21 [W] H,W XXXXXXXX XXXXXXXX		PPG21
$001BC4_H$	PDUT21 [W] H,W XXXXXXXX XXXXXXXX		PTMR21 [R] H,W 11111111 11111111		
$001BC8_H$	PCN221 [R/W] B,H,W --000000 -----110		PSDR21 [R/W] H,W 00000000 00000000		
$001BCC_H$	PTPC21 [R/W] H,W 00000000 00000000		—	—	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$001BD0_H$	PCN22 [R/W] B,H,W 00000000 000000-0		PCSR22 [W] H,W XXXXXXXX XXXXXXXX		PPG22
$001BD4_H$	PDUT22 [W] H,W XXXXXXXX XXXXXXXX		PTMR22 [R] H,W 11111111 11111111		
$001BD8_H$	PCN222 [R/W] B,H,W --000000 -----110		PSDR22 [R/W] H,W 00000000 00000000		
$001BDC_H$	PTPC22 [R/W] H,W 00000000 00000000		—	—	
$001BE0_H$	PCN23 [R/W] B,H,W 00000000 000000-0		PCSR23 [W] H,W XXXXXXXX XXXXXXXX		PPG23
$001BE4_H$	PDUT23 [W] H,W XXXXXXXX XXXXXXXX		PTMR23 [R] H,W 11111111 11111111		
$001BE8_H$	PCN223 [R/W] B,H,W --000000 -----110		PSDR23 [R/W] H,W 00000000 00000000		
$001BEC_H$	PTPC23 [R/W] H,W 00000000 00000000		—	—	
$001BF0_H$	PCN24 [R/W] B,H,W 00000000 000000-0		PCSR24 [W] H,W XXXXXXXX XXXXXXXX		PPG24
$001BF4_H$	PDUT24 [W] H,W XXXXXXXX XXXXXXXX		PTMR24 [R] H,W 11111111 11111111		
$001BF8_H$	PCN224 [R/W] B,H,W --000000 -----110		PSDR24 [R/W] H,W 00000000 00000000		
$001BFC_H$	PTPC24 [R/W] H,W 00000000 00000000		—	—	
$001C00_H$	PCN25 [R/W] B,H,W 00000000 000000-0		PCSR25 [W] H,W XXXXXXXX XXXXXXXX		PPG25
$001C04_H$	PDUT25 [W] H,W XXXXXXXX XXXXXXXX		PTMR25 [R] H,W 11111111 11111111		
$001C08_H$	PCN225 [R/W] B,H,W --000000 -----110		PSDR25 [R/W] H,W 00000000 00000000		
$001C0C_H$	PTPC25 [R/W] H,W 00000000 00000000		—	—	
$001C10_H$	PCN26 [R/W] B,H,W 00000000 000000-0		PCSR26 [W] H,W XXXXXXXX XXXXXXXX		PPG26
$001C14_H$	PDUT26 [W] H,W XXXXXXXX XXXXXXXX		PTMR26 [R] H,W 11111111 11111111		
$001C18_H$	PCN226 [R/W] B,H,W --000000 -----110		PSDR26 [R/W] H,W 00000000 00000000		
$001C1C_H$	PTPC26 [R/W] H,W 00000000 00000000		—	—	
$001C20_H$	PCN27 [R/W] B,H,W 00000000 000000-0		PCSR27 [W] H,W XXXXXXXX XXXXXXXX		PPG27
$001C24_H$	PDUT27 [W] H,W XXXXXXXX XXXXXXXX		PTMR27 [R] H,W 11111111 11111111		
$001C28_H$	PCN227 [R/W] B,H,W --000000 -----110		PSDR27 [R/W] H,W 00000000 00000000		
$001C2C_H$	PTPC27 [R/W] H,W 00000000 00000000		—	—	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$001C30_H$	PCN28 [R/W] B,H,W 00000000 000000-0		PCSR28 [W] H,W XXXXXXXX XXXXXXXX		PPG28
$001C34_H$	PDUT28 [W] H,W XXXXXXXX XXXXXXXX		PTMR28 [R] H,W 11111111 11111111		
$001C38_H$	PCN228 [R/W] B,H,W --000000 -----110		PSDR28 [R/W] H,W 00000000 00000000		
$001C3C_H$	PTPC28 [R/W] H,W 00000000 00000000		—	—	
$001C40_H$	PCN29 [R/W] B,H,W 00000000 000000-0		PCSR29 [W] H,W XXXXXXXX XXXXXXXX		PPG29
$001C44_H$	PDUT29 [W] H,W XXXXXXXX XXXXXXXX		PTMR29 [R] H,W 11111111 11111111		
$001C48_H$	PCN229 [R/W] B,H,W --000000 -----110		PSDR29 [R/W] H,W 00000000 00000000		
$001C4C_H$	PTPC29 [R/W] H,W 00000000 00000000		—	—	
$001C50_H$	PCN30 [R/W] B,H,W 00000000 000000-0		PCSR30 [W] H,W XXXXXXXX XXXXXXXX		PPG30
$001C54_H$	PDUT30 [W] H,W XXXXXXXX XXXXXXXX		PTMR30 [R] H,W 11111111 11111111		
$001C58_H$	PCN230 [R/W] B,H,W --000000 -----110		PSDR30 [R/W] H,W 00000000 00000000		
$001C5C_H$	PTPC30 [R/W] H,W 00000000 00000000		—	—	
$001C60_H$	PCN31 [R/W] B,H,W 00000000 000000-0		PCSR31 [W] H,W XXXXXXXX XXXXXXXX		PPG31
$001C64_H$	PDUT31 [W] H,W XXXXXXXX XXXXXXXX		PTMR31 [R] H,W 11111111 11111111		
$001C68_H$	PCN231 [R/W] B,H,W --000000 -----110		PSDR31 [R/W] H,W 00000000 00000000		
$001C6C_H$	PTPC31 [R/W] H,W 00000000 00000000		—	—	
$001C70_H$	PCN32 [R/W] B,H,W 00000000 000000-0		PCSR32 [W] H,W XXXXXXXX XXXXXXXX		PPG32
$001C74_H$	PDUT32 [W] H,W XXXXXXXX XXXXXXXX		PTMR32 [R] H,W 11111111 11111111		
$001C78_H$	PCN232 [R/W] B,H,W --000000 -----110		PSDR32 [R/W] H,W 00000000 00000000		
$001C7C_H$	PTPC32 [R/W] H,W 00000000 00000000		—	—	
$001C80_H$	PCN33 [R/W] B,H,W 00000000 000000-0		PCSR33 [W] H,W XXXXXXXX XXXXXXXX		PPG33
$001C84_H$	PDUT33 [W] H,W XXXXXXXX XXXXXXXX		PTMR33 [R] H,W 11111111 11111111		
$001C88_H$	PCN233 [R/W] B,H,W --000000 -----110		PSDR33 [R/W] H,W 00000000 00000000		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001C8C$_H$	PTPC33 [R/W] H,W 00000000 00000000		—	—	PPG33
001C90$_H$	PCN34 [R/W] B,H,W 00000000 000000-0		PCSR34 [W] H,W XXXXXXXX XXXXXXXX		PPG34
001C94$_H$	PDUT34 [W] H,W XXXXXXXX XXXXXXXX		PTMR34 [R] H,W 11111111 11111111		
001C98$_H$	PCN234 [R/W] B,H,W --000000 -----110		PSDR34 [R/W] H,W 00000000 00000000		
001C9C$_H$	PTPC34 [R/W] H,W 00000000 00000000		—	—	
001CA0$_H$	PCN35 [R/W] B,H,W 00000000 000000-0		PCSR35 [W] H,W XXXXXXXX XXXXXXXX		PPG35
001CA4$_H$	PDUT35 [W] H,W XXXXXXXX XXXXXXXX		PTMR35 [R] H,W 11111111 11111111		
001CA8$_H$	PCN235 [R/W] B,H,W --000000 -----110		PSDR35 [R/W] H,W 00000000 00000000		
001CAC$_H$	PTPC35 [R/W] H,W 00000000 00000000		—	—	
001CB0$_H$	PCN36 [R/W] B,H,W 00000000 000000-0		PCSR36 [W] H,W XXXXXXXX XXXXXXXX		PPG36
001CB4$_H$	PDUT36 [W] H,W XXXXXXXX XXXXXXXX		PTMR36 [R] H,W 11111111 11111111		
001CB8$_H$	PCN236 [R/W] B,H,W --000000 -----110		PSDR36 [R/W] H,W 00000000 00000000		
001CBC$_H$	PTPC36 [R/W] H,W 00000000 00000000		—	—	
001CC0$_H$	PCN37 [R/W] B,H,W 00000000 000000-0		PCSR37 [W] H,W XXXXXXXX XXXXXXXX		PPG37
001CC4$_H$	PDUT37 [W] H,W XXXXXXXX XXXXXXXX		PTMR37 [R] H,W 11111111 11111111		
001CC8$_H$	PCN237 [R/W] B,H,W --000000 -----110		PSDR37 [R/W] H,W 00000000 00000000		
001CCC$_H$	PTPC37 [R/W] H,W 00000000 00000000		—	—	
001CD0$_H$	PCN38 [R/W] B,H,W 00000000 000000-0		PCSR38 [W] H,W XXXXXXXX XXXXXXXX		PPG38
001CD4$_H$	PDUT38 [W] H,W XXXXXXXX XXXXXXXX		PTMR38 [R] H,W 11111111 11111111		
001CD8$_H$	PCN238 [R/W] B,H,W --000000 -----110		PSDR38 [R/W] H,W 00000000 00000000		
001CDC$_H$	PTPC38 [R/W] H,W 00000000 00000000		—	—	
001CE0$_H$	PCN39 [R/W] B,H,W 00000000 000000-0		PCSR39 [W] H,W XXXXXXXX XXXXXXXX		PPG39
001CE4$_H$	PDUT39 [W] H,W XXXXXXXX XXXXXXXX		PTMR39 [R] H,W 11111111 11111111		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$001CE8_H$	PCN239 [R/W] B,H,W --000000 -----110		PSDR39 [R/W] H,W 00000000 00000000		PPG39
$001CEC_H$	PTPC39 [R/W] H,W 00000000 00000000		—	—	
$001CF0_H$	PCN40 [R/W] B,H,W 00000000 000000-0		PCSR40 [W] H,W XXXXXXXX XXXXXXXX		PPG40
$001CF4_H$	PDUT40 [W] H,W XXXXXXXX XXXXXXXX		PTMR40 [R] H,W 11111111 11111111		
$001CF8_H$	PCN240 [R/W] B,H,W --000000 -----110		PSDR40 [R/W] H,W 00000000 00000000		
$001CFC_H$	PTPC40 [R/W] H,W 00000000 00000000		—	—	
$001D00_H$	PCN41 [R/W] B,H,W 00000000 000000-0		PCSR41 [W] H,W XXXXXXXX XXXXXXXX		PPG41
$001D04_H$	PDUT41 [W] H,W XXXXXXXX XXXXXXXX		PTMR41 [R] H,W 11111111 11111111		
$001D08_H$	PCN241 [R/W] B,H,W --000000 -----110		PSDR41 [R/W] H,W 00000000 00000000		
$001D0C_H$	PTPC41 [R/W] H,W 00000000 00000000		—	—	
$001D10_H$	PCN42 [R/W] B,H,W 00000000 000000-0		PCSR42 [W] H,W XXXXXXXX XXXXXXXX		PPG42
$001D14_H$	PDUT42 [W] H,W XXXXXXXX XXXXXXXX		PTMR42 [R] H,W 11111111 11111111		
$001D18_H$	PCN242 [R/W] B,H,W --000000 -----110		PSDR42 [R/W] H,W 00000000 00000000		
$001D1C_H$	PTPC42 [R/W] H,W 00000000 00000000		—	—	
$001D20_H$	PCN43 [R/W] B,H,W 00000000 000000-0		PCSR43 [W] H,W XXXXXXXX XXXXXXXX		PPG43
$001D24_H$	PDUT43 [W] H,W XXXXXXXX XXXXXXXX		PTMR43 [R] H,W 11111111 11111111		
$001D28_H$	PCN243 [R/W] B,H,W --000000 -----110		PSDR43 [R/W] H,W 00000000 00000000		
$001D2C_H$	PTPC43 [R/W] H,W 00000000 00000000		—	—	
$001D30_H$	PCN44 [R/W] B,H,W 00000000 000000-0		PCSR44 [W] H,W XXXXXXXX XXXXXXXX		PPG44
$001D34_H$	PDUT44 [W] H,W XXXXXXXX XXXXXXXX		PTMR44 [R] H,W 11111111 11111111		
$001D38_H$	PCN244 [R/W] B,H,W --000000 -----110		PSDR44 [R/W] H,W 00000000 00000000		
$001D3C_H$	PTPC44 [R/W] H,W 00000000 00000000		—	—	
$001D40_H$	PCN45 [R/W] B,H,W 00000000 000000-0		PCSR45 [W] H,W XXXXXXXX XXXXXXXX		PPG45

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$001D44_H$	PDUT45 [W] H,W XXXXXXXX XXXXXXXX		PTMR45 [R] H,W 11111111 11111111		PPG45
$001D48_H$	PCN245 [R/W] B,H,W --000000 -----110		PSDR45 [R/W] H,W 00000000 00000000		
$001D4C_H$	PTPC45 [R/W] H,W 00000000 00000000		—	—	
$001D50_H$	PCN46 [R/W] B,H,W 00000000 000000-0		PCSR46 [W] H,W XXXXXXXX XXXXXXXX		PPG46
$001D54_H$	PDUT46 [W] H,W XXXXXXXX XXXXXXXX		PTMR46 [R] H,W 11111111 11111111		
$001D58_H$	PCN246 [R/W] B,H,W --000000 -----110		PSDR46 [R/W] H,W 00000000 00000000		
$001D5C_H$	PTPC46 [R/W] H,W 00000000 00000000		—	—	
$001D60_H$	PCN47 [R/W] B,H,W 00000000 000000-0		PCSR47 [W] H,W XXXXXXXX XXXXXXXX		PPG47
$001D64_H$	PDUT47 [W] H,W XXXXXXXX XXXXXXXX		PTMR47 [R] H,W 11111111 11111111		
$001D68_H$	PCN247 [R/W] B,H,W --000000 -----110		PSDR47 [R/W] H,W 00000000 00000000		
$001D6C_H$	PTPC47 [R/W] H,W 00000000 00000000		—	—	
$001D70_H$ to $001FFC_H$	—	—	—	—	Reserved
002000_H	CTRLR0 [R/W] B,H,W -------- 000-0001		STATR0 [R/W] B,H,W -------- 00000000		CAN0 (128msb)
002004_H	ERRCNT0 [R] B,H,W 00000000 00000000		BTR0 [R/W] B,H,W -0100011 00000001		
002008_H	INTR0 [R] B,H,W 00000000 00000000		TESTR0 [R/W] B,H,W -------- X00000--		
$00200C_H$	BRPER0 [R/W] B,H,W -------- ----0000		—	—	
002010_H	IF1CREQ0 [R/W] B,H,W 0------- 00000001		IF1CMSK0 [R/W] B,H,W -------- 00000000		
002014_H	IF1MSK20 [R/W] B,H,W 11-11111 11111111		IF1MSK10 [R/W] B,H,W 11111111 11111111		
002018_H	IF1ARB20 [R/W] B,H,W 00000000 00000000		IF1ARB10 [R/W] B,H,W 00000000 00000000		
$00201C_H$	IF1MCTR0 [R/W] B,H,W 00000000 0---0000		—	—	
002020_H	IF1DTA10 [R/W] B,H,W 00000000 00000000		IF1DTA20 [R/W] B,H,W 00000000 00000000		
002024_H	IF1DTB10 [R/W] B,H,W 00000000 00000000		IF1DTB20 [R/W] B,H,W 00000000 00000000		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
002028_H	—	—	—	—	CAN0 (128msb)
$00202C_H$	—	—	—	—	
002030_H, 002034_H	Reserved(IF1 data mirror)				
002038_H	—	—	—	—	
$00203C_H$	—	—	—	—	
002040_H	IF2CREQ0 [R/W] B,H,W 0------- 00000001		IF2CMSK0 [R/W] B,H,W -------- 00000000		
002044_H	IF2MSK20 [R/W] B,H,W 11-11111 11111111		IF2MSK10 [R/W] B,H,W 11111111 11111111		
002048_H	IF2ARB20 [R/W] B,H,W 00000000 00000000		IF2ARB10 [R/W] B,H,W 00000000 00000000		
$00204C_H$	IF2MCTR0 [R/W] B,H,W 00000000 0---0000		—	—	
002050_H	IF2DTA10 [R/W] B,H,W 00000000 00000000		IF2DTA20 [R/W] B,H,W 00000000 00000000		
002054_H	IF2DTB10 [R/W] B,H,W 00000000 00000000		IF2DTB20 [R/W] B,H,W 00000000 00000000		
002058_H	—	—	—	—	
$00205C_H$	—	—	—	—	
002060_H, 002064_H	Reserved(IF2 data mirror)				
002068_H to $00207C_H$	—				
002080_H	TREQR20 [R] B,H,W 00000000 00000000		TREQR10 [R] B,H,W 00000000 00000000		
002084_H	TREQR40 [R] B,H,W 00000000 00000000		TREQR30 [R] B,H,W 00000000 00000000		
002088_H	TREQR60 [R] B,H,W 00000000 00000000		TREQR50 [R] B,H,W 00000000 00000000		
$00208C_H$	TREQR80 [R] B,H,W 00000000 00000000		TREQR70 [R] B,H,W 00000000 00000000		
002090_H	NEWDT20 [R] B,H,W 00000000 00000000		NEWDT10 [R] B,H,W 00000000 00000000		
002094_H	NEWDT40 [R] B,H,W 00000000 00000000		NEWDT30 [R] B,H,W 00000000 00000000		
002098_H	NEWDT60 [R] B,H,W 00000000 00000000		NEWDT50 [R] B,H,W 00000000 00000000		
$00209C_H$	NEWDT80 [R] B,H,W 00000000 00000000		NEWDT70 [R] B,H,W 00000000 00000000		
$0020A0_H$	INTPND20 [R] B,H,W 00000000 00000000		INTPND10 [R] B,H,W 00000000 00000000		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$0020A4_H$	INTPND40 [R] B,H,W 00000000 00000000		INTPND30 [R] B,H,W 00000000 00000000		CAN0 (128msb)
$0020A8_H$	INTPND60 [R] B,H,W 00000000 00000000		INTPND50 [R] B,H,W 00000000 00000000		
$0020AC_H$	INTPND80 [R] B,H,W 00000000 00000000		INTPND70 [R] B,H,W 00000000 00000000		
$0020B0_H$	MSGVAL20 [R] B,H,W 00000000 00000000		MSGVAL10 [R] B,H,W 00000000 00000000		
$0020B4_H$	MSGVAL40 [R] B,H,W 00000000 00000000		MSGVAL30 [R] B,H,W 00000000 00000000		
$0020B8_H$	MSGVAL60 [R] B,H,W 00000000 00000000		MSGVAL50 [R] B,H,W 00000000 00000000		
$0020BC_H$	MSGVAL80 [R] B,H,W 00000000 00000000		MSGVAL70 [R] B,H,W 00000000 00000000		
$0020C0_H$ to $0020FC_H$	—				
002100_H	CTRLR1 [R/W] B,H,W -------- 000-0001		STATR1 [R/W] B,H,W -------- 00000000		CAN1 (64msb)
002104_H	ERRCNT1 [R] B,H,W 00000000 00000000		BTR1 [R/W] B,H,W -0100011 00000001		
002108_H	INTR1 [R] B,H,W 00000000 00000000		TESTR1 [R/W] B,H,W -------- X00000--		
$00210C_H$	BRPER1 [R/W] B,H,W -------- ----0000		—	—	
002110_H	IF1CREQ1 [R/W] B,H,W 0------- 00000001		IF1CMSK1 [R/W] B,H,W -------- 00000000		
002114_H	IF1MSK21 [R/W] B,H,W 11-11111 11111111		IF1MSK11 [R/W] B,H,W 11111111 11111111		
002118_H	IF1ARB21 [R/W] B,H,W 00000000 00000000		IF1ARB11 [R/W] B,H,W 00000000 00000000		
$00211C_H$	IF1MCTR1 [R/W] B,H,W 00000000 0---0000		—	—	
002120_H	IF1DTA11 [R/W] B,H,W 00000000 00000000		IF1DTA21 [R/W] B,H,W 00000000 00000000		
002124_H	IF1DTB11 [R/W] B,H,W 00000000 00000000		IF1DTB21 [R/W] B,H,W 00000000 00000000		
002128_H	—	—	—	—	
$00212C_H$	—	—	—	—	
002130_H, 002134_H	Reserved (IF1 data mirror)				
002138_H	—	—	—	—	
$00213C_H$	—	—	—	—	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
002140_H	IF2CREQ1 [R/W] B,H,W 0------- 00000001		IF2CMSK1 [R/W] B,H,W -------- 00000000		CAN1 (64msb)
002144_H	IF2MSK21 [R/W] B,H,W 11-11111 11111111		IF2MSK11 [R/W] B,H,W 11111111 11111111		
002148_H	IF2ARB21 [R/W] B,H,W 00000000 00000000		IF2ARB11 [R/W] B,H,W 00000000 00000000		
$00214C_H$	IF2MCTR1 [R/W] B,H,W 00000000 0---0000		—	—	
002150_H	IF2DTA11 [R/W] B,H,W 00000000 00000000		IF2DTA21 [R/W] B,H,W 00000000 00000000		
002154_H	IF2DTB11 [R/W] B,H,W 00000000 00000000		IF2DTB21 [R/W] B,H,W 00000000 00000000		
002158_H	—	—	—	—	
$00215C_H$	—	—	—	—	
002160_H, 002164_H	Reserved (IF2 data mirror)				
002168_H to $00217C_H$	—				
002180_H	TREQR21 [R] B,H,W 00000000 00000000		TREQR11 [R] B,H,W 00000000 00000000		
002184_H	TREQR41 [R] B,H,W 00000000 00000000		TREQR31 [R] B,H,W 00000000 00000000		
002188_H	—	—	—	—	
$00218C_H$	—	—	—	—	
002190_H	NEWDT21 [R] B,H,W 00000000 00000000		NEWDT11 [R] B,H,W 00000000 00000000		
002194_H	NEWDT41 [R] B,H,W 00000000 00000000		NEWDT31 [R] B,H,W 00000000 00000000		
002198_H	—	—	—	—	
$00219C_H$	—	—	—	—	
$0021A0_H$	INTPND21 [R] B,H,W 00000000 00000000		INTPND11 [R] B,H,W 00000000 00000000		
$0021A4_H$	INTPND41 [R] B,H,W 00000000 00000000		INTPND31 [R] B,H,W 00000000 00000000		
$0021A8_H$	—	—	—	—	
$0021AC_H$	—	—	—	—	
$0021B0_H$	MSGVAL21 [R] B,H,W 00000000 00000000		MSGVAL11 [R] B,H,W 00000000 00000000		
$0021B4_H$	MSGVAL41 [R] B,H,W 00000000 00000000		MSGVAL31 [R] B,H,W 00000000 00000000		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$0021B8_H$	—	—	—	—	CAN1 (64msb)
$0021BC_H$	—	—	—	—	
$0021C0_H$ to $0021FC_H$	—				
002200_H	CTRLR2 [R/W] B,H,W -------- 000-0001		STATR2 [R/W] B,H,W -------- 00000000		CAN2 (64msb)
002204_H	ERRCNT2 [R] B,H,W 00000000 00000000		BTR2 [R/W] B,H,W -0100011 00000001		
002208_H	INTR2 [R] B,H,W 00000000 00000000		TESTR2 [R/W] B,H,W -------- X00000--		
$00220C_H$	BRPER2 [R/W] B,H,W -------- ----0000		—		
002210_H	IF1CREQ2 [R/W] B,H,W 0------- 00000001		IF1CMSK2 [R/W] B,H,W -------- 00000000		
002214_H	IF1MSK22 [R/W] B,H,W 11-11111 11111111		IF1MSK12 [R/W] B,H,W 11111111 11111111		
002218_H	IF1ARB22 [R/W] B,H,W 00000000 00000000		IF1ARB12 [R/W] B,H,W 00000000 00000000		
$00221C_H$	IF1MCTR2 [R/W] B,H,W 00000000 0---0000		—		
002220_H	IF1DTA12 [R/W] B,H,W 00000000 00000000		IF1DTA22 [R/W] B,H,W 00000000 00000000		
002224_H	IF1DTB12 [R/W] B,H,W 00000000 00000000		IF1DTB22 [R/W] B,H,W 00000000 00000000		
002228_H	—	—	—	—	
$00222C_H$	—	—	—	—	
002230_H, 002234_H	Reserved (IF1 data mirror)				
002238_H	—	—	—	—	
$00223C_H$	—	—	—	—	
002240_H	IF2CREQ2 [R/W] B,H,W 0------- 00000001		IF2CMSK2 [R/W] B,H,W -------- 00000000		
002244_H	IF2MSK22 [R/W] B,H,W 11-11111 11111111		IF2MSK12 [R/W] B,H,W 11111111 11111111		
002248_H	IF2ARB22 [R/W] B,H,W 00000000 00000000		IF2ARB12 [R/W] B,H,W 00000000 00000000		
$00224C_H$	IF2MCTR2 [R/W] B,H,W 00000000 0---0000		—		
002250_H	IF2DTA12 [R/W] B,H,W 00000000 00000000		IF2DTA22 [R/W] B,H,W 00000000 00000000		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
002254_H	IF2DTB12 [R/W] B,H,W 00000000 00000000		IF2DTB22 [R/W] B,H,W 00000000 00000000		CAN2 (64msb)
002258_H	—	—	—	—	
$00225C_H$	—	—	—	—	
002260_H, 002264_H	Reserved (IF2 data mirror)				
002268_H to $00227C_H$	—				
002280_H	TREQR22 [R] B,H,W 00000000 00000000		TREQR12 [R] B,H,W 00000000 00000000		
002284_H	TREQR42 [R] B,H,W 00000000 00000000		TREQR32 [R] B,H,W 00000000 00000000		
002288_H	—	—	—	—	
$00228C_H$	—	—	—	—	
002290_H	NEWDT22 [R] B,H,W 00000000 00000000		NEWDT12 [R] B,H,W 00000000 00000000		
002294_H	NEWDT42 [R] B,H,W 00000000 00000000		NEWDT32 [R] B,H,W 00000000 00000000		
002298_H	—	—	—	—	
$00229C_H$	—	—	—	—	
$0022A0_H$	INTPND22 [R] B,H,W 00000000 00000000		INTPND12 [R] B,H,W 00000000 00000000		
$0022A4_H$	INTPND42 [R] B,H,W 00000000 00000000		INTPND32 [R] B,H,W 00000000 00000000		
$0022A8_H$	—	—	—	—	
$0022AC_H$	—	—	—	—	
$0022B0_H$	MSGVAL22 [R] B,H,W 00000000 00000000		MSGVAL12 [R] B,H,W 00000000 00000000		
$0022B4_H$	MSGVAL42 [R] B,H,W 00000000 00000000		MSGVAL32 [R] B,H,W 00000000 00000000		
$0022B8_H$	—	—	—	—	
$0022BC_H$	—	—	—	—	
$0022C0_H$ to $0022FC_H$	—				
002300_H	DFCTLR [R/W] B,H,W -0------ --------		—	DFSTR [R/W] B,H,W -----001	WorkFlash
002304_H	—	—	—	—	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
002308_H	FLIFCTLR [R/W] B,H,W ---0--00	—	FLIFFER1 [R/W] B,H,W --------	FLIFFER2 [R/W] B,H,W --------	Flash / WorkFlash
$00230C_H$ to $0023FC_H$	—				Reserved
002400_H	SEEARX [R] B,H,W -0000000 00000000		DEEARX [R] B,H,W -0000000 00000000		XBS RAM ECC control
002404_H	EECSRX [R/W] B,H,W ----00--	—	EFEARX [R/W] B,H,W -0000000 00000000		
002408_H	—	EFECRX [R/W] B,H,W -------0 00000000 00000000			
$00240C_H$ to $002FFC_H$	—				Reserved
003000_H	SEEARA [R] B,H,W -----000 00000000		DEEARA [R] B,H,W -----000 00000000		Backup RAM ECC control
003004_H	EECSRA [R/W] B,H,W ----00--	—	EFEARA [R/W] B,H,W -----000 00000000		
003008_H	—	EFECRA [R/W] B,H,W -------0 00000000 00000000			
$00300C_H$	TEAR0X[R] B,H,W 000----- -------- -0000000 00000000				RAM/ diagnosis XBS RAM
003010_H	TEAR1X[R] B,H,W 000----- -------- -0000000 00000000				
003014_H	TEAR2X[R] B,H,W 000----- -------- -0000000 00000000				
003018_H	TAEARX [R/W] B,H,W -1111111 11111111		TASARX [R/W] B,H,W -0000000 00000000		
$00301C_H$	TFECRX [R/W] B,H,W ----0000	TICRX [R/W] B,H,W ----0000	TTCRX [R/W] B,H,W ------00 00001100		
003020_H	TSRCRX [W] B,H,W 0-------	—	—	TKCCRX [R/W] B,H,W 00----00	
003024_H to $00302C_H$	—				Reserved
003030_H	TEAR0A[R] B,H,W 000----- -------- -----000 00000000				RAM/ diagnosis Backup RAM
003034_H	TEAR1A[R] B,H,W 000----- -------- -----000 00000000				
003038_H	TEAR2A[R] B,H,W 000----- -------- -----000 00000000				
$00303C_H$	TAEARA[R/W] B,H,W -----111 11111111		TASARA[R/W] B,H,W -----000 00000000		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
003040_H	TFECRA [R/W] B,H,W ----0000	TICRA [R/W] B,H,W ----0000	TTCRA [R/W] B,H,W ------00 00001100		RAM/ diagnosis Backup RAM
003044_H	TSRCRA [R/W] B,H,W 0-------	—	—	TKCCRA [R/W] B,H,W 00----00	
003048_H to $0030FC_H$	—				Reserved
003100_H	BUSDIGSR0[R/W] H,W 00000000 0-----00		BUSDIGSR1[R/W] H,W 00000000 0-----00		BUS diagnosis
003104_H	BUSDIGSR2[R/W] H,W 00000000 0-----00		BUSTSTR0[R/W] H,W 00--0000 00000000		
003108_H	BUSADR0 [R] W 00000000 00000000 00000000 00000000				
$00310C_H$	BUSADR1 [R] W 00000000 00000000 00000000 00000000				
003110_H	BUSADR2 [R] W 00000000 00000000 00000000 00000000				
003114_H	—	—	BUSDIGSR3[R/W] H,W 00000000 0-----00		
003118_H	BUSDIGSR4[R/W] H,W 00000000 0-----00		BUSTSTR1[R/W] H,W 00--000- 00000000		
$00311C_H$	—	—	—	—	
003120_H	BUSADR3 [R] W 00000000 00000000 00000000 00000000				
003124_H	BUSADR4 [R] W 00000000 00000000 00000000 00000000				
003128_H to $003FFC_H$	—				Reserved
004000_H to $005FFC_H$	Backup-RAM				Backup RAM area
006000_H to $00EFFC_H$	—	—	—	—	Reserved
$00F000_H$ to $00FEFC_H$	—	—	—	—	Reserved [S]
$00FF00_H$	DSUCR [R/W] B,H,W -------- -------0		—	—	OCDU [S]
$00FF04_H$ to $00FF0C_H$	—				Reserved [S]
$00FF10_H$	PCSR [R/W] B,H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				OCDU [S]

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$00FF14_H$	PSSR [R/W] B,H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				OCDU [S]
$00FF18_H$ to $00FFF4_H$	—				Reserved [S]
$00FFF8_H$	EDIR1 [R] B,H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				OCDU [S]
$00FFFC_H$	EDIR0 [R] B,H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

[S]: It is a system register. The illegal instruction exception (data access error) is generated in these registers in the user mode when reading and writing to it.

■ INTERRUPT VECTOR TABLE

This list shows the assignments of interrupt factors and interrupt vectors/interrupt control registers.

● Interrupt vector

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Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN
	Decimal	Hexadecimal				
Reset	0	0	-	$3FC_H$	$000FFFFC_H$	-
System reserved	1	1	-	$3F8_H$	$000FFFF8_H$	-
System reserved	2	2	-	$3F4_H$	$000FFFF4_H$	-
System reserved	3	3	-	$3F0_H$	$000FFFF0_H$	-
System reserved	4	4	-	$3EC_H$	$000FFFEC_H$	-
FPU exception	5	5	-	$3E8_H$	$000FFFE8_H$	-
Exception of instruction access protection violation	6	6	-	$3E4_H$	$000FFFE4_H$	-
Exception of data access protection violation	7	7	-	$3E0_H$	$000FFFE0_H$	-
Data access error interrupt	8	8	-	$3DC_H$	$000FFFDC_H$	-
INTE instruction	9	9	-	$3D8_H$	$000FFFD8_H$	-
Instruction break	10	0A	-	$3D4_H$	$000FFFD4_H$	-
System reserved	11	0B	-	$3D0_H$	$000FFFD0_H$	-
System reserved	12	0C	-	$3CC_H$	$000FFFCC_H$	-
System reserved	13	0D	-	$3C8_H$	$000FFFC8_H$	-
Exception of invalid instruction	14	0E	-	$3C4_H$	$000FFFC4_H$	-
NMI request Error generation during internal bus diagnosis XBS RAM double-bit error generation Backup RAM double-bit error generation TPU violation	15	0F	15 (F_H) Fixed	$3C0_H$	$000FFFC0_H$	-
External interrupt 0-7	16	10	ICR00	$3BC_H$	$000FFFBC_H$	0
External interrupt 8-15 External low-voltage detection interrupt	17	11	ICR01	$3B8_H$	$000FFFB8_H$	1*[8]
Reload timer 0/1/4/5	18	12	ICR02	$3B4_H$	$000FFFB4_H$	2*[2]
Reload timer 3/6/7	19	13	ICR03	$3B0_H$	$000FFFB0_H$	3*[2]
Multi-function serial interface ch.0 (reception completed) Multi-function serial interface ch.0 (status)	20	14	ICR04	$3AC_H$	$000FFFAC_H$	4*[1]
Multi-function serial interface ch.0 (transmission completed)	21	15	ICR05	$3A8_H$	$000FFFA8_H$	5*[1]
-	22	16	ICR06	$3A4_H$	$000FFFA4_H$	-*[7]
-	23	17	ICR07	$3A0_H$	$000FFFA0_H$	-*[7]
-	24	18	ICR08	$39C_H$	$000FFF9C_H$	-*[7]
-	25	19	ICR09	398_H	$000FFF98_H$	-*[7]
Multi-function serial interface ch.3 (reception completed) Multi-function serial interface ch.3 (status)	26	1A	ICR10	394_H	$000FFF94_H$	10*[1]
Multi-function serial interface ch.3 (transmission completed)	27	1B	ICR11	390_H	$000FFF90_H$	11
Multi-function serial interface ch.4 (reception completed) Multi-function serial interface ch.4 (status)	28	1C	ICR12	$38C_H$	$000FFF8C_H$	12*[1]

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN
	Decimal	Hexadecimal				
Multi-function serial interface ch.4 (transmission completed)	29	1D	ICR13	388_H	$000FFF88_H$	13
Multi-function serial interface ch.5 (reception completed)	30	1E	ICR14	384_H	$000FFF84_H$	14*[1]
Multi-function serial interface ch.5 (status)						
Multi-function serial interface ch.5 (transmission completed)	31	1F	ICR15	380_H	$000FFF80_H$	15
Multi-function serial interface ch.6 (reception completed)	32	20	ICR16	$37C_H$	$000FFF7C_H$	16*[1]
Multi-function serial interface ch.6 (status)						
Multi-function serial interface ch.6 (transmission completed)	33	21	ICR17	378_H	$000FFF78_H$	17
CAN0	34	22	ICR18	374_H	$000FFF74_H$	-
CAN1	35	23	ICR19	370_H	$000FFF70_H$	-
RAM diagnosis end						
RAM initialization completion						
Error generation during RAM diagnosis						
Backup RAM diagnosis end						
Backup RAM initialization completion						
Error generation during Backup RAM diagnosis						
CAN2	36	24	ICR20	$36C_H$	$000FFF6C_H$	-
Up/down counter 0						
Up/down counter 1						
Real time clock	37	25	ICR21	368_H	$000FFF68_H$	-
-	38	26	ICR22	364_H	$000FFF64_H$	-*[7]
16-bit Free-run timer 0 (0 detection) / (compare clear)	39	27	ICR23	360_H	$000FFF60_H$	23
PPG 1/10/11/20/30/31	40	28	ICR24	$35C_H$	$000FFF5C_H$	24*[3]
16-bit Free-run timer 1 (0 detection) / (compare clear)						
PPG 2/3/12/13/23/43	41	29	ICR25	358_H	$000FFF58_H$	25*[3]
16-bit Free-run timer 2 (0 detection) / (compare clear)						
PPG 4/24/35	42	2A	ICR26	354_H	$000FFF54_H$	26*[3]
PPG 7/16/17/27/37	43	2B	ICR27	350_H	$000FFF50_H$	27*[3]
PPG 19	44	2C	ICR28	$34C_H$	$000FFF4C_H$	28*[3]
16-bit ICU 0 (fetching) / 16-bit ICU 1 (fetching)	45	2D	ICR29	348_H	$000FFF48_H$	29
Main timer	46	2E	ICR30	344_H	$000FFF44_H$	30
Sub timer						
PLL timer						
16-bit ICU 2 (fetching) /16-bit ICU 3 (fetching)						
Clock calibration unit (sub oscillation)	47	2F	ICR31	340_H	$000FFF40_H$	31*[1,4]
Multi-function serial interface ch.9 (reception completed)						
Multi-function serial interface ch.9 (status)						
A/D converter 0/1/7/10/11/14/15/16/17/22/27/28/31	48	30	ICR32	$33C_H$	$000FFF3C_H$	32

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN
	Decimal	Hexadecimal				
Clock calibration unit (CR oscillation) Multi-function serial interface ch.9 (transmission completed) 16-bit OCU 0 (match) / 16-bit OCU 1 (match)	49	31	ICR33	338_H	$000FFF38_H$	33
32-bit Free-run timer 4 16-bit OCU 2 (match) / 16-bit OCU 3 (match)	50	32	ICR34	334_H	$000FFF34_H$	34*6
16-bit OCU 4 (match) / 16-bit OCU 5 (match)	51	33	ICR35	330_H	$000FFF30_H$	35
32-bit ICU6 (fetching/measurement) Multi-function serial interface ch.10 (reception completed) Multi-function serial interface ch.10 (status)	52	34	ICR36	$32C_H$	$000FFF2C_H$	36*1
Multi-function serial interface ch.10 (transmission completed)	53	35	ICR37	328_H	$000FFF28_H$	37
32-bit ICU8 (fetching/measurement) Multi-function serial interface ch.11 (reception completed) Multi-function serial interface ch.11 (status)	54	36	ICR38	324_H	$000FFF24_H$	38*1
32-bit ICU9 (fetching/measurement) WG dead timer underflow 0 / 1/ 2 WG dead timer reload 0 / 1/ 2 WG DTTI 0	55	37	ICR39	320_H	$000FFF20_H$	39
32-bit ICU4 (fetching/measurement) Multi-function serial interface ch.11 (transmission completed)	56	38	ICR40	$31C_H$	$000FFF1C_H$	40
32-bit ICU5 (fetching/measurement) A/D converter 32/34/35/37/38/40/41/42/43/44/45/46/47	57	39	ICR41	318_H	$000FFF18_H$	41
32-bit OCU7/11 (match)	58	3A	ICR42	314_H	$000FFF14_H$	42
32-bit OCU8/9 (match)	59	3B	ICR43	310_H	$000FFF10_H$	43
-	60	3C	ICR44	$30C_H$	$000FFF0C_H$	-*7
- -	61	3D	ICR45	308_H	$000FFF08_H$	-
DMAC0/1/2/3/4/5/6/7/8/9/10/11/12/13/14/15	62	3E	ICR46	304_H	$000FFF04_H$	-
Delay interrupt	63	3F	ICR47	300_H	$000FFF00_H$	-
System reserved (Used for REALOS™*9)	64	40	-	$2FC_H$	$000FFEFC_H$	-
System reserved (Used for REALOS)	65	41	-	$2F8_H$	$000FFEF8_H$	-
Used with the INT instruction	66 | 255	42 | FF	-	$2F4_H$ | 000_H	$000FFEF4_H$ | $000FFC00_H$	-

Note: It does not support a DMA transfer request caused by an interrupt generated from a peripheral to which no RN (Resource Number) is assigned.

*1: It does not support a DMA transfer by the status of the multi-function serial interface and I^2C reception.

*2: Reload timer ch.4 to ch.7 do not support a DMA transfer by the interrupt.

*3: PPG ch.24 to ch.47 do not support a DMA transfer by the interrupt.

*4: The clock calibration unit does not support a DMA transfer by the interrupt.

*5: It does not support a DMA transfer by the interrupt by the RAM ECC bit error.

*6: 32-bit Free-run timer ch.3, ch.4 and ch.5 do not support a DMA transfer by the interrupt.

*7: There is no resource corresponding to the interrupt level.

*8: It does not support a DMA transfer by the external low-voltage detection interrupt.
*9: REALOS is a trademark of Spansion LLC.

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Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN
	Decimal	Hexadecimal				
Reset	0	0	-	$3FC_H$	$000FFFFC_H$	-
System reserved	1	1	-	$3F8_H$	$000FFFF8_H$	-
System reserved	2	2	-	$3F4_H$	$000FFFF4_H$	-
System reserved	3	3	-	$3F0_H$	$000FFFF0_H$	-
System reserved	4	4	-	$3EC_H$	$000FFFEC_H$	-
FPU exception	5	5	-	$3E8_H$	$000FFFE8_H$	-
Exception of instruction access protection violation	6	6	-	$3E4_H$	$000FFFE4_H$	-
Exception of data access protection violation	7	7	-	$3E0_H$	$000FFFE0_H$	-
Data access error interrupt	8	8	-	$3DC_H$	$000FFFDC_H$	-
INTE instruction	9	9	-	$3D8_H$	$000FFFD8_H$	-
Instruction break	10	0A	-	$3D4_H$	$000FFFD4_H$	-
System reserved	11	0B	-	$3D0_H$	$000FFFD0_H$	-
System reserved	12	0C	-	$3CC_H$	$000FFFCC_H$	-
System reserved	13	0D	-	$3C8_H$	$000FFFC8_H$	-
Exception of invalid instruction	14	0E	-	$3C4_H$	$000FFFC4_H$	-
NMI request Error generation during internal bus diagnosis XBS RAM double-bit error generation Backup RAM double-bit error generation TPU violation	15	0F	15 (F_H) Fixed	$3C0_H$	$000FFFC0_H$	-
External interrupt 0-7	16	10	ICR00	$3BC_H$	$000FFFBC_H$	0
External interrupt 8-15 External low-voltage detection interrupt	17	11	ICR01	$3B8_H$	$000FFFB8_H$	1*[8]
Reload timer 0/1/4/5	18	12	ICR02	$3B4_H$	$000FFFB4_H$	2*[2]
Reload timer 3/6/7	19	13	ICR03	$3B0_H$	$000FFFB0_H$	3*[2]
Multi-function serial interface ch.0 (reception completed) Multi-function serial interface ch.0 (status)	20	14	ICR04	$3AC_H$	$000FFFAC_H$	4*[1]
Multi-function serial interface ch.0 (transmission completed)	21	15	ICR05	$3A8_H$	$000FFFA8_H$	5*[1]
-	22	16	ICR06	$3A4_H$	$000FFFA4_H$	-*[7]
-	23	17	ICR07	$3A0_H$	$000FFFA0_H$	-*[7]
Multi-function serial interface ch.2 (reception completed) Multi-function serial interface ch.2 (status)	24	18	ICR08	$39C_H$	$000FFF9C_H$	8*[1]
Multi-function serial interface ch.2 (transmission completed)	25	19	ICR09	398_H	$000FFF98_H$	9*[1]
Multi-function serial interface ch.3 (reception completed) Multi-function serial interface ch.3 (status)	26	1A	ICR10	394_H	$000FFF94_H$	10*[1]
Multi-function serial interface ch.3 (transmission completed)	27	1B	ICR11	390_H	$000FFF90_H$	11
Multi-function serial interface ch.4 (reception completed) Multi-function serial interface ch.4 (status)	28	1C	ICR12	$38C_H$	$000FFF8C_H$	12*[1]

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN
	Decimal	Hexadecimal				
Multi-function serial interface ch.4 (transmission completed)	29	1D	ICR13	388_H	$000FFF88_H$	13
Multi-function serial interface ch.5 (reception completed)	30	1E	ICR14	384_H	$000FFF84_H$	14*[1]
Multi-function serial interface ch.5 (status)						
Multi-function serial interface ch.5 (transmission completed)	31	1F	ICR15	380_H	$000FFF80_H$	15
Multi-function serial interface ch.6 (reception completed)	32	20	ICR16	$37C_H$	$000FFF7C_H$	16*[1]
Multi-function serial interface ch.6 (status)						
Multi-function serial interface ch.6 (transmission completed)	33	21	ICR17	378_H	$000FFF78_H$	17
CAN0	34	22	ICR18	374_H	$000FFF74_H$	-
CAN1	35	23	ICR19	370_H	$000FFF70_H$	-
RAM diagnosis end						
RAM initialization completion						
Error generation during RAM diagnosis						
Backup RAM diagnosis end						
Backup RAM initialization completion						
Error generation during Backup RAM diagnosis						
CAN2	36	24	ICR20	$36C_H$	$000FFF6C_H$	-
Up/down counter 0						
Up/down counter 1						
Real time clock	37	25	ICR21	368_H	$000FFF68_H$	-
-	38	26	ICR22	364_H	$000FFF64_H$	-*[7]
16-bit Free-run timer 0 (0 detection) / (compare clear)	39	27	ICR23	360_H	$000FFF60_H$	23
PPG 1/10/11/20/30/31	40	28	ICR24	$35C_H$	$000FFF5C_H$	24*[3]
16-bit Free-run timer 1 (0 detection) / (compare clear)						
PPG 2/3/12/13/23/43	41	29	ICR25	358_H	$000FFF58_H$	25*[3]
16-bit Free-run timer 2 (0 detection) / (compare clear)						
PPG 4/5/15/24/35	42	2A	ICR26	354_H	$000FFF54_H$	26*[3]
PPG 7/16/17/26/27/37	43	2B	ICR27	350_H	$000FFF50_H$	27*[3]
PPG 8/18/19/29	44	2C	ICR28	$34C_H$	$000FFF4C_H$	28*[3]
16-bit ICU 0 (fetching) / 16-bit ICU 1 (fetching)	45	2D	ICR29	348_H	$000FFF48_H$	29
Main timer	46	2E	ICR30	344_H	$000FFF44_H$	30
Sub timer						
PLL timer						
16-bit ICU 2 (fetching) /16-bit ICU 3 (fetching)						
Clock calibration unit (sub oscillation)	47	2F	ICR31	340_H	$000FFF40_H$	31*[1,4]
Multi-function serial interface ch.9 (reception completed)						
Multi-function serial interface ch.9 (status)						

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN
	Decimal	Hexadecimal				
A/D converter 0/1/7/10/11/12/14/15/16/17/19/22/26/27/28/31	48	30	ICR32	$33C_H$	$000FFF3C_H$	32
Clock calibration unit (CR oscillation) Multi-function serial interface ch.9 (transmission completed) 16-bit OCU 0 (match) / 16-bit OCU 1 (match)	49	31	ICR33	338_H	$000FFF38_H$	33
32-bit Free-run timer 4 16-bit OCU 2 (match) / 16-bit OCU 3 (match)	50	32	ICR34	334_H	$000FFF34_H$	34*[6]
32-bit Free-run timer 5 16-bit OCU 4 (match) / 16-bit OCU 5 (match)	51	33	ICR35	330_H	$000FFF30_H$	35*[6]
32-bit ICU6 (fetching/measurement) Multi-function serial interface ch.10 (reception completed) Multi-function serial interface ch.10 (status)	52	34	ICR36	$32C_H$	$000FFF2C_H$	36*[1]
Multi-function serial interface ch.10 (transmission completed)	53	35	ICR37	328_H	$000FFF28_H$	37
32-bit ICU8 (fetching/measurement) Multi-function serial interface ch.11 (reception completed) Multi-function serial interface ch.11 (status)	54	36	ICR38	324_H	$000FFF24_H$	38*[1]
32-bit ICU9 (fetching/measurement) WG dead timer underflow 0 / 1/ 2 WG dead timer reload 0 / 1/ 2 WG DTTI 0	55	37	ICR39	320_H	$000FFF20_H$	39
32-bit ICU4 (fetching/measurement) Multi-function serial interface ch.11 (transmission completed)	56	38	ICR40	$31C_H$	$000FFF1C_H$	40
32-bit ICU5 (fetching/measurement) A/D converter 32/33/34/35/36/37/38/39/40/41/42/43/44/45/46/47	57	39	ICR41	318_H	$000FFF18_H$	41
32-bit OCU7/11 (match)	58	3A	ICR42	314_H	$000FFF14_H$	42
32-bit OCU8/9 (match)	59	3B	ICR43	310_H	$000FFF10_H$	43
-	60	3C	ICR44	$30C_H$	$000FFF0C_H$	-*[7]
Base timer 1 IRQ0 Base timer 1 IRQ1 - -	61	3D	ICR45	308_H	$000FFF08_H$	45*[5]
DMAC 0/1/2/3/4/5/6/7/8/9/10/11/12/13/14/15	62	3E	ICR46	304_H	$000FFF04_H$	-
Delay interrupt	63	3F	ICR47	300_H	$000FFF00_H$	-
System reserved (Used for REALOS)	64	40	-	$2FC_H$	$000FFEFC_H$	-
System reserved (Used for REALOS)	65	41	-	$2F8_H$	$000FFEF8_H$	-
Used with the INT instruction	66 | 255	42 | FF	-	$2F4_H$ | 000_H	$000FFEF4_H$ | $000FFC00_H$	-

Note: It does not support a DMA transfer request caused by an interrupt generated from a peripheral to which no RN (Resource Number) is assigned.

*1: It does not support a DMA transfer by the status of the multi-function serial interface and I^2C reception.

*2: Reload timer ch.4 to ch.7 do not support a DMA transfer by the interrupt.

*3: PPG ch.24 to ch.47 do not support a DMA transfer by the interrupt.
*4: The clock calibration unit does not support a DMA transfer by the interrupt.
*5: It does not support a DMA transfer by the interrupt by the RAM ECC bit error.
*6: 32-bit Free-run timer ch.3, ch.4 and ch.5 do not support a DMA transfer by the interrupt.
*7: There is no resource corresponding to the interrupt level.
*8: It does not support a DMA transfer by the external low-voltage detection interrupt.

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Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN
	Decimal	Hexadecimal				
Reset	0	0	-	$3FC_H$	$000FFFFC_H$	-
System reserved	1	1	-	$3F8_H$	$000FFFF8_H$	-
System reserved	2	2	-	$3F4_H$	$000FFFF4_H$	-
System reserved	3	3	-	$3F0_H$	$000FFFF0_H$	-
System reserved	4	4	-	$3EC_H$	$000FFFEC_H$	-
FPU exception	5	5	-	$3E8_H$	$000FFFE8_H$	-
Exception of instruction access protection violation	6	6	-	$3E4_H$	$000FFFE4_H$	-
Exception of data access protection violation	7	7	-	$3E0_H$	$000FFFE0_H$	-
Data access error interrupt	8	8	-	$3DC_H$	$000FFFDC_H$	-
INTE instruction	9	9	-	$3D8_H$	$000FFFD8_H$	-
Instruction break	10	0A	-	$3D4_H$	$000FFFD4_H$	-
System reserved	11	0B	-	$3D0_H$	$000FFFD0_H$	-
System reserved	12	0C	-	$3CC_H$	$000FFFCC_H$	-
System reserved	13	0D	-	$3C8_H$	$000FFFC8_H$	-
Exception of invalid instruction	14	0E	-	$3C4_H$	$000FFFC4_H$	-
NMI request Error generation during internal bus diagnosis XBS RAM double-bit error generation Backup RAM double-bit error generation TPU violation	15	0F	15 (F_H) Fixed	$3C0_H$	$000FFFC0_H$	-
External interrupt 0-7	16	10	ICR00	$3BC_H$	$000FFFBC_H$	0
External interrupt 8-15 External low-voltage detection interrupt	17	11	ICR01	$3B8_H$	$000FFFB8_H$	1*[8]
Reload timer 0/1/4/5	18	12	ICR02	$3B4_H$	$000FFFB4_H$	2*[2]
Reload timer 2/3/6/7	19	13	ICR03	$3B0_H$	$000FFFB0_H$	3*[2]
Multi-function serial interface ch.0 (reception completed) Multi-function serial interface ch.0 (status)	20	14	ICR04	$3AC_H$	$000FFFAC_H$	4*[1]
Multi-function serial interface ch.0 (transmission completed)	21	15	ICR05	$3A8_H$	$000FFFA8_H$	5*[1]
Multi-function serial interface ch.1 (reception completed) Multi-function serial interface ch.1 (status)	22	16	ICR06	$3A4_H$	$000FFFA4_H$	6*[1]
Multi-function serial interface ch.1 (transmission completed)	23	17	ICR07	$3A0_H$	$000FFFA0_H$	7*[1]
Multi-function serial interface ch.2 (reception completed) Multi-function serial interface ch.2 (status)	24	18	ICR08	$39C_H$	$000FFF9C_H$	8*[1]
Multi-function serial interface ch.2 (transmission completed)	25	19	ICR09	398_H	$000FFF98_H$	9*[1]
Multi-function serial interface ch.3 (reception completed) Multi-function serial interface ch.3 (status)	26	1A	ICR10	394_H	$000FFF94_H$	10*[1]
Multi-function serial interface ch.3 (transmission completed)	27	1B	ICR11	390_H	$000FFF90_H$	11

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN
	Decimal	Hexadecimal				
Multi-function serial interface ch.4 (reception completed)	28	1C	ICR12	$38C_H$	$000FFF8C_H$	12*[1]
Multi-function serial interface ch.4 (status)						
Multi-function serial interface ch.4 (transmission completed)	29	1D	ICR13	388_H	$000FFF88_H$	13
Multi-function serial interface ch.5 (reception completed)	30	1E	ICR14	384_H	$000FFF84_H$	14*[1]
Multi-function serial interface ch.5 (status)						
Multi-function serial interface ch.5 (transmission completed)	31	1F	ICR15	380_H	$000FFF80_H$	15
Multi-function serial interface ch.6 (reception completed)	32	20	ICR16	$37C_H$	$000FFF7C_H$	16*[1]
Multi-function serial interface ch.6 (status)						
Multi-function serial interface ch.6 (transmission completed)	33	21	ICR17	378_H	$000FFF78_H$	17
CAN0	34	22	ICR18	374_H	$000FFF74_H$	-
CAN1	35	23	ICR19	370_H	$000FFF70_H$	-
RAM diagnosis end						
RAM initialization completion						
Error generation during RAM diagnosis						
Backup RAM diagnosis end						
Backup RAM initialization completion						
Error generation during Backup RAM diagnosis						
CAN2	36	24	ICR20	$36C_H$	$000FFF6C_H$	-
Up/down counter 0						
Up/down counter 1						
Real time clock	37	25	ICR21	368_H	$000FFF68_H$	-
Multi-function serial interface ch.7 (reception completed)	38	26	ICR22	364_H	$000FFF64_H$	22*[1]
Multi-function serial interface ch.7 (status)						
16-bit Free-running timer 0 (0 detection) / (compare clear)	39	27	ICR23	360_H	$000FFF60_H$	23
Multi-function serial interface ch.7 (transmission completed)						
PPG 1/10/11/20/21/30/31	40	28	ICR24	$35C_H$	$000FFF5C_H$	24*[3]
16-bit Free-run timer 1 (0 detection) / (compare clear)						
PPG 2/3/12/13/23/32/43	41	29	ICR25	358_H	$000FFF58_H$	25*[3]
16-bit Free-run timer 2 (0 detection) / (compare clear)						
PPG 4/5/14/15/24/25/35/44	42	2A	ICR26	354_H	$000FFF54_H$	26*[3]
PPG 6/7/16/17/26/27/37	43	2B	ICR27	350_H	$000FFF50_H$	27*[3]
PPG 8/9/18/19/28/29	44	2C	ICR28	$34C_H$	$000FFF4C_H$	28*[3]
Multi-function serial interface ch.8 (reception completed)	45	2D	ICR29	348_H	$000FFF48_H$	29*[1]
Multi-function serial interface ch.8 (status)						
16-bit ICU 0 (fetching) / 16-bit ICU 1 (fetching)						

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN
	Decimal	Hexadecimal				
Main timer Sub timer PLL timer Multi-function serial interface ch.8 (transmission completed) 16-bit ICU 2 (fetching) /16-bit ICU 3 (fetching)	46	2E	ICR30	344_H	$000FFF44_H$	30
Clock calibration unit (sub oscillation) Multi-function serial interface ch.9 (reception completed) Multi-function serial interface ch.9 (status)	47	2F	ICR31	340_H	$000FFF40_H$	31*1, *4
A/D converter 0/1/7/9/10/11/12/13/14/15/16 17/18/19/22/23/26/27/28/29/31	48	30	ICR32	$33C_H$	$000FFF3C_H$	32
Clock calibration unit (CR oscillation) Multi-function serial interface ch.9 (transmission completed) 16-bit OCU 0 (match) / 16-bit OCU 1 (match)	49	31	ICR33	338_H	$000FFF38_H$	33
32-bit Free-run timer 4 16-bit OCU 2 (match) / 16-bit OCU 3 (match)	50	32	ICR34	334_H	$000FFF34_H$	34*6
32-bit Free-run timer 3/5 16-bit OCU 4 (match) / 16-bit OCU 5 (match)	51	33	ICR35	330_H	$000FFF30_H$	35*6
32-bit ICU6 (fetching/measurement) Multi-function serial interface ch.10 (reception completed) Multi-function serial interface ch.10 (status)	52	34	ICR36	$32C_H$	$000FFF2C_H$	36*1
32-bit ICU7 (fetching/measurement) Multi-function serial interface ch.10 (transmission completed)	53	35	ICR37	328_H	$000FFF28_H$	37
32-bit ICU8 (fetching/measurement) Multi-function serial interface ch.11 (reception completed) Multi-function serial interface ch.11 (status)	54	36	ICR38	324_H	$000FFF24_H$	38*1
32-bit ICU9 (fetching/measurement) WG dead timer underflow 0/1/2 WG dead timer reload 0/1/2 WG DTTI 0	55	37	ICR39	320_H	$000FFF20_H$	39
32-bit ICU4 (fetching/measurement) Multi-function serial interface ch.11 (transmission completed)	56	38	ICR40	$31C_H$	$000FFF1C_H$	40
32-bit ICU5 (fetching/measurement) A/D converter 32/33/34/35/36/37/38/39/40/41/42/43/44/45/46/47	57	39	ICR41	318_H	$000FFF18_H$	41
32-bit OCU 6/7/10/11 (match)	58	3A	ICR42	314_H	$000FFF14_H$	42
32-bit OCU 8/9 (match)	59	3B	ICR43	310_H	$000FFF10_H$	43
Base timer 0 IRQ0 Base timer 0 IRQ1	60	3C	ICR44	$30C_H$	$000FFF0C_H$	44

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN
	Decimal	Hexadecimal				
Base timer 1 IRQ0 Base timer 1 IRQ1 - -	61	3D	ICR45	308_H	$000FFF08_H$	45*[5]
DMAC 0/1/2/3/4/5/6/7/8/9/10/11/12/13/14/15	62	3E	ICR46	304_H	$000FFF04_H$	-
Delay interrupt	63	3F	ICR47	300_H	$000FFF00_H$	-
System reserved (Used for REALOS)	64	40	-	$2FC_H$	$000FFEFC_H$	-
System reserved (Used for REALOS)	65	41	-	$2F8_H$	$000FFEF8_H$	-
Used with the INT instruction	66 | 255	42 | FF	-	$2F4_H$ | 000_H	$000FFEF4_H$ | $000FFC00_H$	-

Note: It does not support a DMA transfer request caused by an interrupt generated from a peripheral to which no RN (Resource Number) is assigned.

*1: It does not support a DMA transfer by the status of the multi-function serial interface and I^2C reception.

*2: Reload timer ch.4 to ch.7 do not support a DMA transfer by the interrupt.

*3: PPG ch.24 to ch.47 do not support a DMA transfer by the interrupt.

*4: The clock calibration unit does not support a DMA transfer by the interrupt.

*5: It does not support a DMA transfer by the interrupt by the RAM ECC bit error.

*6: 32-bit Free-run timer ch.3, ch.4 and ch.5 do not support a DMA transfer by the interrupt.

*7: There is no resource corresponding to the interrupt level.

*8: It does not support a DMA transfer by the external low-voltage detection interrupt.

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Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN
	Decimal	Hexadecimal				
Reset	0	0	-	$3FC_H$	$000FFFFC_H$	-
System reserved	1	1	-	$3F8_H$	$000FFFF8_H$	-
System reserved	2	2	-	$3F4_H$	$000FFFF4_H$	-
System reserved	3	3	-	$3F0_H$	$000FFFF0_H$	-
System reserved	4	4	-	$3EC_H$	$000FFFEC_H$	-
FPU exception	5	5	-	$3E8_H$	$000FFFE8_H$	-
Exception of instruction access protection violation	6	6	-	$3E4_H$	$000FFFE4_H$	-
Exception of data access protection violation	7	7	-	$3E0_H$	$000FFFE0_H$	-
Data access error interrupt	8	8	-	$3DC_H$	$000FFFDC_H$	-
INTE instruction	9	9	-	$3D8_H$	$000FFFD8_H$	-
Instruction break	10	0A	-	$3D4_H$	$000FFFD4_H$	-
System reserved	11	0B	-	$3D0_H$	$000FFFD0_H$	-
System reserved	12	0C	-	$3CC_H$	$000FFFCC_H$	-
System reserved	13	0D	-	$3C8_H$	$000FFFC8_H$	-
Exception of invalid instruction	14	0E	-	$3C4_H$	$000FFFC4_H$	-
NMI request Error generation during internal bus diagnosis XBS RAM double-bit error generation Backup RAM double-bit error generation TPU violation	15	0F	15 (F_H) Fixed	$3C0_H$	$000FFFC0_H$	-
External interrupt 0-7	16	10	ICR00	$3BC_H$	$000FFFBC_H$	0
External interrupt 8-15 External low-voltage detection interrupt	17	11	ICR01	$3B8_H$	$000FFFB8_H$	$1*^{8}$
Reload timer 0/1/4/5	18	12	ICR02	$3B4_H$	$000FFFB4_H$	$2*^{2}$
Reload timer 2/3/6/7	19	13	ICR03	$3B0_H$	$000FFFB0_H$	$3*^{2}$
Multi-function serial interface ch.0 (reception completed) Multi-function serial interface ch.0 (status)	20	14	ICR04	$3AC_H$	$000FFFAC_H$	$4*^{1}$
Multi-function serial interface ch.0 (transmission completed)	21	15	ICR05	$3A8_H$	$000FFFA8_H$	$5*^{1}$
Multi-function serial interface ch.1 (reception completed) Multi-function serial interface ch.1 (status)	22	16	ICR06	$3A4_H$	$000FFFA4_H$	$6*^{1}$
Multi-function serial interface ch.1 (transmission completed)	23	17	ICR07	$3A0_H$	$000FFFA0_H$	$7*^{1}$
Multi-function serial interface ch.2 (reception completed) Multi-function serial interface ch.2 (status)	24	18	ICR08	$39C_H$	$000FFF9C_H$	$8*^{1}$
Multi-function serial interface ch.2 (transmission completed)	25	19	ICR09	398_H	$000FFF98_H$	$9*^{1}$
Multi-function serial interface ch.3 (reception completed) Multi-function serial interface ch.3 (status)	26	1A	ICR10	394_H	$000FFF94_H$	$10*^{1}$
Multi-function serial interface ch.3 (transmission completed)	27	1B	ICR11	390_H	$000FFF90_H$	11

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN
	Decimal	Hexadecimal				
Multi-function serial interface ch.4 (reception completed)	28	1C	ICR12	$38C_H$	$000FFF8C_H$	12*[1]
Multi-function serial interface ch.4 (status)						
Multi-function serial interface ch.4 (transmission completed)	29	1D	ICR13	388_H	$000FFF88_H$	13
Multi-function serial interface ch.5 (reception completed)	30	1E	ICR14	384_H	$000FFF84_H$	14*[1]
Multi-function serial interface ch.5 (status)						
Multi-function serial interface ch.5 (transmission completed)	31	1F	ICR15	380_H	$000FFF80_H$	15
Multi-function serial interface ch.6 (reception completed)	32	20	ICR16	$37C_H$	$000FFF7C_H$	16*[1]
Multi-function serial interface ch.6 (status)						
Multi-function serial interface ch.6 (transmission completed)	33	21	ICR17	378_H	$000FFF78_H$	17
CAN0	34	22	ICR18	374_H	$000FFF74_H$	-
CAN1	35	23	ICR19	370_H	$000FFF70_H$	-
RAM diagnosis end						
RAM initialization completion						
Error generation during RAM diagnosis						
Backup RAM diagnosis end						
Backup RAM initialization completion						
Error generation during Backup RAM diagnosis						
CAN2	36	24	ICR20	$36C_H$	$000FFF6C_H$	-
Up/down counter 0						
Up/down counter 1						
Real time clock	37	25	ICR21	368_H	$000FFF68_H$	-
Multi-function serial interface ch.7 (reception completed)	38	26	ICR22	364_H	$000FFF64_H$	22*[1]
Multi-function serial interface ch.7 (status)						
16-bit Free-run timer 0 (0 detection) / (compare clear)	39	27	ICR23	360_H	$000FFF60_H$	23
Multi-function serial interface ch.7 (transmission completed)						
PPG 0/1/10/11/20/21/30/31	40	28	ICR24	$35C_H$	$000FFF5C_H$	24*[3]
16-bit Free-run timer 1 (0 detection) / (compare clear)						
PPG 2/3/12/13/22/23/32/33/42/43	41	29	ICR25	358_H	$000FFF58_H$	25*[3]
16-bit Free-run timer 2 (0 detection) / (compare clear)						
PPG 4/5/14/15/24/25/35/44	42	2A	ICR26	354_H	$000FFF54_H$	26*[3]
PPG 6/7/16/17/26/27/37	43	2B	ICR27	350_H	$000FFF50_H$	27*[3]
PPG 8/9/18/19/28/29	44	2C	ICR28	$34C_H$	$000FFF4C_H$	28*[3]
Multi-function serial interface ch.8 (reception completed)	45	2D	ICR29	348_H	$000FFF48_H$	29*[1]
Multi-function serial interface ch.8 (status)						
16-bit ICU 0 (fetching) / 16-bit ICU 1 (fetching)						

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN
	Decimal	Hexadecimal				
Main timer Sub timer PLL timer Multi-function serial interface ch.8 (transmission completed) 16-bit ICU 2 (fetching) /16-bit ICU 3 (fetching)	46	2E	ICR30	344_H	$000FFF44_H$	30
Clock calibration unit (sub oscillation) Multi-function serial interface ch.9 (reception completed) Multi-function serial interface ch.9 (status)	47	2F	ICR31	340_H	$000FFF40_H$	31*1, *4
A/D converter 0/1/7/9/10/11/12/13/14/15/16/ 17/18/19/20/21/22/23/24/25/26/27/28/29/30/31	48	30	ICR32	$33C_H$	$000FFF3C_H$	32
Clock calibration unit (CR oscillation) Multi-function serial interface ch.9 (transmission completed) 16-bit OCU 0 (match) / 16-bit OCU 1 (match)	49	31	ICR33	338_H	$000FFF38_H$	33
32-bit Free-run timer 4 16-bit OCU 2 (match) / 16-bit OCU 3 (match)	50	32	ICR34	334_H	$000FFF34_H$	34*6
32-bit Free-run timer 3/5 16-bit OCU 4 (match) / 16-bit OCU 5 (match)	51	33	ICR35	330_H	$000FFF30_H$	35*6
32-bit ICU6 (fetching/measurement) Multi-function serial interface ch.10 (reception completed) Multi-function serial interface ch.10 (status)	52	34	ICR36	$32C_H$	$000FFF2C_H$	36*1
32-bit ICU7 (fetching/measurement) Multi-function serial interface ch.10 (transmission completed)	53	35	ICR37	328_H	$000FFF28_H$	37
32-bit ICU8 (fetching/measurement) Multi-function serial interface ch.11 (reception completed) Multi-function serial interface ch.11 (status)	54	36	ICR38	324_H	$000FFF24_H$	38*1
32-bit ICU9 (fetching/measurement) WG dead timer underflow 0/1/2 WG dead timer reload 0/1/2 WG DTTI 0	55	37	ICR39	320_H	$000FFF20_H$	39
32-bit ICU4 (fetching/measurement) Multi-function serial interface ch.11 (transmission completed)	56	38	ICR40	$31C_H$	$000FFF1C_H$	40
32-bit ICU5 (fetching/measurement) A/D converter 32/33/34/35/36/37/38/39/40/41/42/43/44/45/46/47	57	39	ICR41	318_H	$000FFF18_H$	41
32-bit OCU 6/7/10/11 (match)	58	3A	ICR42	314_H	$000FFF14_H$	42
32-bit OCU 8/9 (match)	59	3B	ICR43	310_H	$000FFF10_H$	43
Base timer 0 IRQ0 Base timer 0 IRQ1	60	3C	ICR44	$30C_H$	$000FFF0C_H$	44
Base timer 1 IRQ0 Base timer 1 IRQ1 - -	61	3D	ICR45	308_H	$000FFF08_H$	45*5

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN
	Decimal	Hexadecimal				
DMAC0/1/2/3/4/5/6/7/8/9/10/11/12/13/14/15	62	3E	ICR46	304_H	$000FFF04_H$	-
Delay interrupt	63	3F	ICR47	300_H	$000FFF00_H$	-
System reserved (Used for REALOS)	64	40	-	$2FC_H$	$000FFEFC_H$	-
System reserved (Used for REALOS)	65	41	-	$2F8_H$	$000FFEF8_H$	-
Used with the INT instruction	66 | 255	42 | FF	-	$2F4_H$ | 000_H	$000FFEF4_H$ | $000FFC00_H$	-

Note: It does not support a DMA transfer request caused by an interrupt generated from a peripheral to which no RN (Resource Number) is assigned.

*1: It does not support a DMA transfer by the status of the multi-function serial interface and I^2C reception.

*2: Reload timer ch.4 to ch.7 do not support a DMA transfer by the interrupt.

*3: PPG ch.24 to ch.47 do not support a DMA transfer by the interrupt.

*4: The clock calibration unit does not support a DMA transfer by the interrupt.

*5: It does not support a DMA transfer by the interrupt by the RAM ECC bit error.

*6: 32-bit Free-run timer ch.3, ch.4 and ch.5 do not support a DMA transfer by the interrupt.

*7: There is no resource corresponding to the interrupt level.

*8: It does not support a DMA transfer by the external low-voltage detection interrupt.

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Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN
	Decimal	Hexadecimal				
Reset	0	0	-	$3FC_H$	$000FFFFC_H$	-
System reserved	1	1	-	$3F8_H$	$000FFFF8_H$	-
System reserved	2	2	-	$3F4_H$	$000FFFF4_H$	-
System reserved	3	3	-	$3F0_H$	$000FFFF0_H$	-
System reserved	4	4	-	$3EC_H$	$000FFFEC_H$	-
FPU exception	5	5	-	$3E8_H$	$000FFFE8_H$	-
Exception of instruction access protection violation	6	6	-	$3E4_H$	$000FFFE4_H$	-
Exception of data access protection violation	7	7	-	$3E0_H$	$000FFFE0_H$	-
Data access error interrupt	8	8	-	$3DC_H$	$000FFFDC_H$	-
INTE instruction	9	9	-	$3D8_H$	$000FFFD8_H$	-
Instruction break	10	0A	-	$3D4_H$	$000FFFD4_H$	-
System reserved	11	0B	-	$3D0_H$	$000FFFD0_H$	-
System reserved	12	0C	-	$3CC_H$	$000FFFCC_H$	-
System reserved	13	0D	-	$3C8_H$	$000FFFC8_H$	-
Exception of invalid instruction	14	0E	-	$3C4_H$	$000FFFC4_H$	-
NMI request Error generation during internal bus diagnosis XBS RAM double-bit error generation Backup RAM double-bit error generation TPU violation	15	0F	15 (F_H) Fixed	$3C0_H$	$000FFFC0_H$	-
External interrupt 0-7	16	10	ICR00	$3BC_H$	$000FFFBC_H$	0
External interrupt 8-15 External low-voltage detection interrupt	17	11	ICR01	$3B8_H$	$000FFFB8_H$	1*8
Reload timer 0/1/4/5	18	12	ICR02	$3B4_H$	$000FFFB4_H$	2*2
Reload timer 2/3/6/7	19	13	ICR03	$3B0_H$	$000FFFB0_H$	3*2
Multi-function serial interface ch.0 (reception completed) Multi-function serial interface ch.0 (status)	20	14	ICR04	$3AC_H$	$000FFFAC_H$	4*1
Multi-function serial interface ch.0 (transmission completed)	21	15	ICR05	$3A8_H$	$000FFFA8_H$	5*1
Multi-function serial interface ch.1 (reception completed) Multi-function serial interface ch.1 (status)	22	16	ICR06	$3A4_H$	$000FFFA4_H$	6*1
Multi-function serial interface ch.1 (transmission completed)	23	17	ICR07	$3A0_H$	$000FFFA0_H$	7*1
Multi-function serial interface ch.2 (reception completed) Multi-function serial interface ch.2 (status)	24	18	ICR08	$39C_H$	$000FFF9C_H$	8*1
Multi-function serial interface ch.2 (transmission completed)	25	19	ICR09	398_H	$000FFF98_H$	9*1
Multi-function serial interface ch.3 (reception completed) Multi-function serial interface ch.3 (status)	26	1A	ICR10	394_H	$000FFF94_H$	10*1
Multi-function serial interface ch.3 (transmission completed)	27	1B	ICR11	390_H	$000FFF90_H$	11

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN
	Decimal	Hexadecimal				
Multi-function serial interface ch.4 (reception completed)	28	1C	ICR12	$38C_H$	$000FFF8C_H$	12*[1]
Multi-function serial interface ch.4 (status)						
Multi-function serial interface ch.4 (transmission completed)	29	1D	ICR13	388_H	$000FFF88_H$	13
Multi-function serial interface ch.5 (reception completed)	30	1E	ICR14	384_H	$000FFF84_H$	14*[1]
Multi-function serial interface ch.5 (status)						
Multi-function serial interface ch.5 (transmission completed)	31	1F	ICR15	380_H	$000FFF80_H$	15
Multi-function serial interface ch.6 (reception completed)	32	20	ICR16	$37C_H$	$000FFF7C_H$	16*[1]
Multi-function serial interface ch.6 (status)						
Multi-function serial interface ch.6 (transmission completed)	33	21	ICR17	378_H	$000FFF78_H$	17
CAN0	34	22	ICR18	374_H	$000FFF74_H$	-
CAN1	35	23	ICR19	370_H	$000FFF70_H$	-
RAM diagnosis end						
RAM initialization completion						
Error generation during RAM diagnosis						
Backup RAM diagnosis end						
Backup RAM initialization completion						
Error generation during Backup RAM diagnosis						
CAN2	36	24	ICR20	$36C_H$	$000FFF6C_H$	-
Up/down counter 0						
Up/down counter 1						
Real time clock	37	25	ICR21	368_H	$000FFF68_H$	-
Multi-function serial interface ch.7 (reception completed)	38	26	ICR22	364_H	$000FFF64_H$	22*[1]
Multi-function serial interface ch.7 (status)						
16-bit Free-run timer 0 (0 detection) / (compare clear)	39	27	ICR23	360_H	$000FFF60_H$	23
Multi-function serial interface ch.7 (transmission completed)						
PPG 0/1/10/11/20/21/30/31/40/41	40	28	ICR24	$35C_H$	$000FFF5C_H$	24*[3]
16-bit Free-run timer 1 (0 detection) / (compare clear)						
PPG 2/3/12/13/22/23/32/33/42/43	41	29	ICR25	358_H	$000FFF58_H$	25*[3]
16-bit Free-run timer 2 (0 detection) / (compare clear)						
PPG 4/5/14/15/24/25/34/35/44	42	2A	ICR26	354_H	$000FFF54_H$	26*[3]
PPG 6/7/16/17/26/27/36/37	43	2B	ICR27	350_H	$000FFF50_H$	27*[3]
PPG 8/9/18/19/28/29/38/39	44	2C	ICR28	$34C_H$	$000FFF4C_H$	28*[3]

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN
	Decimal	Hexadecimal				
Multi-function serial interface ch.8 (reception completed) Multi-function serial interface ch.8 (status) 16-bit ICU 0 (fetching) / 16-bit ICU 1 (fetching)	45	2D	ICR29	348_H	$000FFF48_H$	29*[1]
Main timer Sub timer PLL timer Multi-function serial interface ch.8 (transmission completed) 16-bit ICU 2 (fetching) /16-bit ICU 3 (fetching)	46	2E	ICR30	344_H	$000FFF44_H$	30
Clock calibration unit (sub oscillation) Multi-function serial interface ch.9 (reception completed) Multi-function serial interface ch.9 (status)	47	2F	ICR31	340_H	$000FFF40_H$	31*[1, 4]
A/D converter 0/1/2/3/4/5/6/7/8/9/10/11/12/13/14/15/16 17/18/19/20/21/22/23/24/25/26/27/28/29/30/31	48	30	ICR32	$33C_H$	$000FFF3C_H$	32
Clock calibration unit (CR oscillation) Multi-function serial interface ch.9 (transmission completed) 16-bit OCU 0 (match) / 16-bit OCU 1 (match)	49	31	ICR33	338_H	$000FFF38_H$	33
32-bit Free-run timer 4 16-bit OCU 2 (match) / 16-bit OCU 3 (match)	50	32	ICR34	334_H	$000FFF34_H$	34*[6]
32-bit Free-run timer 3/5 16-bit OCU 4 (match) / 16-bit OCU 5 (match)	51	33	ICR35	330_H	$000FFF30_H$	35*[6]
32-bit ICU 6 (fetching/measurement) Multi-function serial interface ch.10 (reception completed) Multi-function serial interface ch.10 (status)	52	34	ICR36	$32C_H$	$000FFF2C_H$	36*[1]
32-bit ICU7 (fetching/measurement) Multi-function serial interface ch.10 (transmission completed)	53	35	ICR37	328_H	$000FFF28_H$	37
32-bit ICU8 (fetching/measurement) Multi-function serial interface ch.11 (reception completed) Multi-function serial interface ch.11 (status)	54	36	ICR38	324_H	$000FFF24_H$	38*[1]
32-bit ICU9 (fetching/measurement) WG dead timer underflow 0 / 1/ 2 WG dead timer reload 0 / 1/ 2 WG DTTI 0	55	37	ICR39	320_H	$000FFF20_H$	39
32-bit ICU4 (fetching/measurement) Multi-function serial interface ch.11 (transmission completed)	56	38	ICR40	$31C_H$	$000FFF1C_H$	40
32-bit ICU5 (fetching/measurement) A/D converter 32/33/34/35/36/37/38/39/40/41/42/43/44/45/46/47	57	39	ICR41	318_H	$000FFF18_H$	41
32-bit OCU 6/7/10/11 (match)	58	3A	ICR42	314_H	$000FFF14_H$	42

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN
	Decimal	Hexadecimal				
32-bit OCU8/9 (match)	59	3B	ICR43	310_H	$000FFF10_H$	43
Base timer 0 IRQ0	60	3C	ICR44	$30C_H$	$000FFF0C_H$	44
Base timer 0 IRQ1						
Base timer 1 IRQ0	61	3D	ICR45	308_H	$000FFF08_H$	45*[5]
Base timer 1 IRQ1						
-						
-						
DMAC 0/1/2/3/4/5/6/7/8/9/10/11/12/13/14/15	62	3E	ICR46	304_H	$000FFF04_H$	-
Delay interrupt	63	3F	ICR47	300_H	$000FFF00_H$	-
System reserved (Used for REALOS)	64	40	-	$2FC_H$	$000FFEFC_H$	-
System reserved (Used for REALOS)	65	41	-	$2F8_H$	$000FFEF8_H$	-
Used with the INT instruction	66 | 255	42 | FF	-	$2F4_H$ | 000_H	$000FFEF4_H$ | $000FFC00_H$	-

Note: It does not support a DMA transfer request caused by an interrupt generated from a peripheral to which no RN (Resource Number) is assigned.

*1: It does not support a DMA transfer by the status of the multi-function serial interface and I^2C reception.

*2: Reload timer ch.4 to ch.7 do not support a DMA transfer by the interrupt.

*3: PPG ch.24 to ch.47 do not support a DMA transfer by the interrupt.

*4: The clock calibration unit does not support a DMA transfer by the interrupt.

*5: It does not support a DMA transfer by the interrupt by the RAM ECC bit error.

*6: 32-bit Free-run timer ch.3, ch.4 and ch.5 do not support a DMA transfer by the interrupt.

*7: There is no resource corresponding to the interrupt level.

*8: It does not support a DMA transfer by the external low-voltage detection interrupt.

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Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN
	Decimal	Hexadecimal				
Reset	0	0	-	$3FC_H$	$000FFFFC_H$	-
System reserved	1	1	-	$3F8_H$	$000FFFF8_H$	-
System reserved	2	2	-	$3F4_H$	$000FFFF4_H$	-
System reserved	3	3	-	$3F0_H$	$000FFFF0_H$	-
System reserved	4	4	-	$3EC_H$	$000FFFEC_H$	-
FPU exception	5	5	-	$3E8_H$	$000FFFE8_H$	-
Exception of instruction access protection violation	6	6	-	$3E4_H$	$000FFFE4_H$	-
Exception of data access protection violation	7	7	-	$3E0_H$	$000FFFE0_H$	-
Data access error interrupt	8	8	-	$3DC_H$	$000FFFDC_H$	-
INTE instruction	9	9	-	$3D8_H$	$000FFFD8_H$	-
Instruction break	10	0A	-	$3D4_H$	$000FFFD4_H$	-
System reserved	11	0B	-	$3D0_H$	$000FFFD0_H$	-
System reserved	12	0C	-	$3CC_H$	$000FFFCC_H$	-
System reserved	13	0D	-	$3C8_H$	$000FFFC8_H$	-
Exception of invalid instruction	14	0E	-	$3C4_H$	$000FFFC4_H$	-
NMI request Error generation during internal bus diagnosis XBS RAM double-bit error generation Backup RAM double-bit error generation TPU violation	15	0F	15 (F_H) Fixed	$3C0_H$	$000FFFC0_H$	-
External interrupt 0-7	16	10	ICR00	$3BC_H$	$000FFFBC_H$	0
External interrupt 8-15 External low-voltage detection interrupt	17	11	ICR01	$3B8_H$	$000FFFB8_H$	1*8
Reload timer 0/1/4/5	18	12	ICR02	$3B4_H$	$000FFFB4_H$	2*2
Reload timer 2/3/6/7	19	13	ICR03	$3B0_H$	$000FFFB0_H$	3*2
Multi-function serial interface ch.0 (reception completed) Multi-function serial interface ch.0 (status)	20	14	ICR04	$3AC_H$	$000FFFAC_H$	4*1
Multi-function serial interface ch.0 (transmission completed)	21	15	ICR05	$3A8_H$	$000FFFA8_H$	5*1
Multi-function serial interface ch.1 (reception completed) Multi-function serial interface ch.1 (status)	22	16	ICR06	$3A4_H$	$000FFFA4_H$	6*1
Multi-function serial interface ch.1 (transmission completed)	23	17	ICR07	$3A0_H$	$000FFFA0_H$	7*1
Multi-function serial interface ch.2 (reception completed) Multi-function serial interface ch.2 (status)	24	18	ICR08	$39C_H$	$000FFF9C_H$	8*1
Multi-function serial interface ch.2 (transmission completed)	25	19	ICR09	398_H	$000FFF98_H$	9*1
Multi-function serial interface ch.3 (reception completed) Multi-function serial interface ch.3 (status)	26	1A	ICR10	394_H	$000FFF94_H$	10*1
Multi-function serial interface ch.3 (transmission completed)	27	1B	ICR11	390_H	$000FFF90_H$	11

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN
	Decimal	Hexadecimal				
Multi-function serial interface ch.4 (reception completed)	28	1C	ICR12	$38C_H$	$000FFF8C_H$	12*[1]
Multi-function serial interface ch.4 (status)						
Multi-function serial interface ch.4 (transmission completed)	29	1D	ICR13	388_H	$000FFF88_H$	13
Multi-function serial interface ch.5 (reception completed)	30	1E	ICR14	384_H	$000FFF84_H$	14*[1]
Multi-function serial interface ch.5 (status)						
Multi-function serial interface ch.5 (transmission completed)	31	1F	ICR15	380_H	$000FFF80_H$	15
Multi-function serial interface ch.6 (reception completed)	32	20	ICR16	$37C_H$	$000FFF7C_H$	16*[1]
Multi-function serial interface ch.6 (status)						
Multi-function serial interface ch.6 (transmission completed)	33	21	ICR17	378_H	$000FFF78_H$	17
CAN0	34	22	ICR18	374_H	$000FFF74_H$	-
CAN1	35	23	ICR19	370_H	$000FFF70_H$	-
RAM diagnosis end						
RAM initialization completion						
Error generation during RAM diagnosis						
Backup RAM diagnosis end						
Backup RAM initialization completion						
Error generation during Backup RAM diagnosis						
CAN2	36	24	ICR20	$36C_H$	$000FFF6C_H$	-
Up/down counter 0						
Up/down counter 1						
Real time clock	37	25	ICR21	368_H	$000FFF68_H$	-
Multi-function serial interface ch.7 (reception completed)	38	26	ICR22	364_H	$000FFF64_H$	22*[1]
Multi-function serial interface ch.7 (status)						
16-bit Free-run timer 0 (0 detection) / (compare clear)	39	27	ICR23	360_H	$000FFF60_H$	23
Multi-function serial interface ch.7 (transmission completed)						
PPG 0/1/10/11/20/21/30/31/40/41	40	28	ICR24	$35C_H$	$000FFF5C_H$	24*[3]
16-bit Free-run timer 1 (0 detection) / (compare clear)						
PPG 2/3/12/13/22/23/32/33/42/43	41	29	ICR25	358_H	$000FFF58_H$	25*[3]
16-bit Free-run timer 2 (0 detection) / (compare clear)						
PPG 4/5/14/15/24/25/34/35/44/45	42	2A	ICR26	354_H	$000FFF54_H$	26*[3]
PPG 6/7/16/17/26/27/36/37/46/47	43	2B	ICR27	350_H	$000FFF50_H$	27*[3]
PPG 8/9/18/19/28/29/38/39	44	2C	ICR28	$34C_H$	$000FFF4C_H$	28*[3]
Multi-function serial interface ch.8 (reception completed)	45	2D	ICR29	348_H	$000FFF48_H$	29*[1]
Multi-function serial interface ch.8 (status)						
16-bit ICU 0 (fetching) / 16-bit ICU 1 (fetching)						

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN
	Decimal	Hexadecimal				
Main timer Sub timer PLL timer Multi-function serial interface ch.8 (transmission completed) 16-bit ICU 2 (fetching) /16-bit ICU 3 (fetching)	46	2E	ICR30	344_H	$000FFF44_H$	30
Clock calibration unit (sub oscillation) Multi-function serial interface ch.9 (reception completed) Multi-function serial interface ch.9 (status)	47	2F	ICR31	340_H	$000FFF40_H$	31*1, *4
A/D converter 0/1/2/3/4/5/6/7/8/9/10/11/12/13/14/15/16 17/18/19/20/21/22/23/24/25/26/27/28/29/30/31	48	30	ICR32	$33C_H$	$000FFF3C_H$	32
Clock calibration unit (CR oscillation) Multi-function serial interface ch.9 (transmission completed) 16-bit OCU 0 (match) / 16-bit OCU 1 (match)	49	31	ICR33	338_H	$000FFF38_H$	33
32-bit Free-run timer 4 16-bit OCU 2 (match) / 16-bit OCU 3 (match)	50	32	ICR34	334_H	$000FFF34_H$	34*6
32-bit Free-run timer 3/5 16-bit OCU 4 (match) / 16-bit OCU 5 (match)	51	33	ICR35	330_H	$000FFF30_H$	35*6
32-bit ICU6 (fetching/measurement) Multi-function serial interface ch.10 (reception completed) Multi-function serial interface ch.10 (status)	52	34	ICR36	$32C_H$	$000FFF2C_H$	36*1
32-bit ICU7 (fetching/measurement) Multi-function serial interface ch.10 (transmission completed)	53	35	ICR37	328_H	$000FFF28_H$	37
32-bit ICU8 (fetching/measurement) Multi-function serial interface ch.11 (reception completed) Multi-function serial interface ch.11 (status)	54	36	ICR38	324_H	$000FFF24_H$	38*1
32-bit ICU9 (fetching/measurement) WG dead timer underflow 0/1/2 WG dead timer reload 0/1/2 WG DTTI 0	55	37	ICR39	320_H	$000FFF20_H$	39
32-bit ICU4 (fetching/measurement) Multi-function serial interface ch.11 (transmission completed)	56	38	ICR40	$31C_H$	$000FFF1C_H$	40
32-bit ICU5 (fetching/measurement) A/D converter 32/33/34/35/36/37/38/39/40/41/42/43/44/45/46/47	57	39	ICR41	318_H	$000FFF18_H$	41
32-bit OCU 6/7/10/11 (match)	58	3A	ICR42	314_H	$000FFF14_H$	42
32-bit OCU 8/9 (match)	59	3B	ICR43	310_H	$000FFF10_H$	43
Base timer 0 IRQ0 Base timer 0 IRQ1	60	3C	ICR44	$30C_H$	$000FFF0C_H$	44

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN
	Decimal	Hexadecimal				
Base timer 1 IRQ0 Base timer 1 IRQ1 - -	61	3D	ICR45	308_H	$000FFF08_H$	45*[5]
DMAC 0/1/2/3/4/5/6/7/8/9/10/11/12/13/14/15	62	3E	ICR46	304_H	$000FFF04_H$	-
Delay interrupt	63	3F	ICR47	300_H	$000FFF00_H$	-
System reserved (Used for REALOS)	64	40	-	$2FC_H$	$000FFEFC_H$	-
System reserved (Used for REALOS)	65	41	-	$2F8_H$	$000FFEF8_H$	-
Used with the INT instruction	66 | 255	42 | FF	-	$2F4_H$ | 000_H	$000FFEF4_H$ | $000FFC00_H$	-

Note: It does not support a DMA transfer request caused by an interrupt generated from a peripheral to which no RN (Resource Number) is assigned.

*1: It does not support a DMA transfer by the status of the multi-function serial interface and I^2C reception.

*2: Reload timer ch.4 to ch.7 do not support a DMA transfer by the interrupt.

*3: PPG ch.24 to ch.47 do not support a DMA transfer by the interrupt.

*4: The clock calibration unit does not support a DMA transfer by the interrupt.

*5: It does not support a DMA transfer by the interrupt by the RAM ECC bit error.

*6: 32-bit Free-run timer ch.3, ch.4 and ch.5 do not support a DMA transfer by the interrupt.

*7: There is no resource corresponding to the interrupt level.

*8: It does not support a DMA transfer by the external low-voltage detection interrupt.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter		Symbol	Rating		Unit	Remarks
			Min	Max		
Power supply voltage *1,*2		V_{CC}	V_{SS}-0.3	V_{SS}+6.0	V	
Analog power supply voltage *1,*2		AV_{CC}	V_{SS}-0.3	V_{SS}+6.0	V	AVRH ≤ AV_{CC} ≤ V_{CC}
Analog reference voltage *1		AVRH	V_{SS}-0.3	V_{SS}+6.0	V	AVRH ≤ AV_{CC}
Input voltage *1		V_I	V_{SS}-0.3	V_{CC}+0.3	V	
Analog pin input voltage *1		V_{IA5}	V_{SS}-0.3	V_{CC}+0.3	V	
Output voltage *1		V_o	V_{SS}-0.3	V_{CC}+0.3	V	
Maximum clamp current		I_{CLAMP}	-	4.0	mA	*6
Total maximum clamp current		$\Sigma\|I_{CLAMP}\|$	-	20	mA	*6
"L" level maximum output current *3		I_{OL1}	-	15	mA	
		I_{OL2}	-	30	mA	
"L" level average output current *4		I_{OLAV1}	-	4	mA	
		I_{OLAV2}	-	12	mA	
"L" level total output current *5		ΣI_{OL1}	-	100	mA	
		ΣI_{OL2}	-	120	mA	
"H" level maximum output current*3		I_{OH1}	-	-15	mA	
		I_{OH2}	-	-30	mA	
"H" level average output current*4		I_{OHAV1}	-	-4	mA	
		I_{OHAV2}	-	-12	mA	
"H" level total output current *5		ΣI_{OH1}	-	-100	mA	
		ΣI_{OH2}	-	-120	mA	
Power consumption	T_A: -40°C to +105°C	P_D	-	882	mW	*8
	T_A: -40°C to +125°C		-	675	mW	*8
Operating temperature		T_A	-40	+105	°C	
			-40	+125	°C	*7
Storage temperature		Tstg	-55	+150	°C	

*1: These parameters are based on the condition that V_{SS}=AV_{SS}=0.0V

*2: Caution must be taken that AV_{CC}, AVRH do not exceed V_{CC} upon power-on and under other circumstances.

*3: The maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

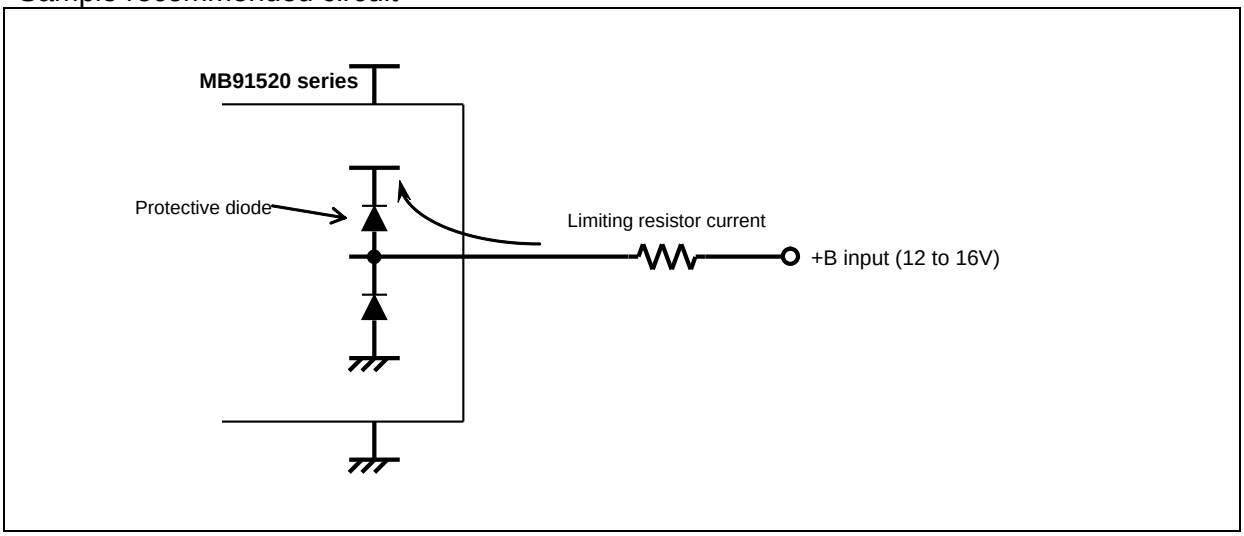
*4: The average output current is defined as the value of the average current flowing through any one of the corresponding pins for a 10 ms period. The average value is the operation current × the operation ratio.

*5: The total output current is defined as the maximum current value flowing through all of corresponding pins.

*6: ・Corresponding pins: all general-purpose ports except P035, 041, 093, 122.
・Use within recommended operating conditions.
・Use at DC voltage (current).
・The + B signal should always be applied by connecting a limiting resistor between the + B signal and the microcontroller.
・The value of the limiting resistor should be set so that the current input to the microcontroller pin does not exceed rated values at any time regardless of instantaneously or constantly when the + B signal is input.
・Note that when the microcontroller drive current is low, such as in the low power consumption modes, the + B input potential can increase the potential at the V_{CC} pin via a protective diode, possibly affecting other devices.
・Note that if the + B signal is input when the microcontroller is off (not fixed at 0 V), since the power is supplied through the pin, the microcontroller may operate incompletely.
・Note that if the +B signal is input at power-on, since the power is supplied through the pin, the power-on reset may not function in the power supply voltage.
・Do not leave + B input pins open.

*7: When it is used under this condition, contact your sales representative.
*8: It is a standard when four-layer substrate is used.

Sample recommended circuit



<WARNING>

Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings. Do not exceed any of these ratings.

2. Recommended operating conditions

(V_{SS}=AV_{SS}=0.0V)

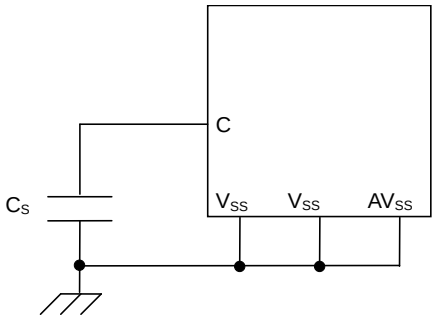
Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC}, AV_{CC}	4.5	5.5	V	Recommended operation guarantee range (When 5.0V is used)
		3.0	3.6	V	Recommended operation guarantee range (When 3.3V is used)
		2.7	5.5	V	Operation guarantee range *1
Smoothing capacitor *2	C_S	4.7 (tolerance within ±50%)		µF	Use a ceramic capacitor or a capacitor that has the similar frequency characteristics. Use a capacitor with a capacitance greater than C_S as the smoothing capacitor on the VCC pin.
Operating temperature	T_A	-40	+105	°C	
		-40	+125	°C	*3

*1: When it is used outside recommended operation guarantee range (range of the operation guarantee),contact your sales representative. Moreover, minimum value with an effective external low-voltage detection reset becomes a voltage until generating low-voltage detection reset.

*2: See the following diagram for details on the connection of smoothing capacitor C_S.

*3: When it is used under this condition, contact your sales representative.

・C Pin Connection Diagram



<WARNING>

The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions.

Any use of semiconductor devices will be under their recommended operating condition. Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure. No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.

3. DC characteristics

(T_A: -40°C to +105°C, V_{CC}= AVcc=5.0V±10%/3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions		Value Min	Value Typ	Value Max	Unit	Remarks
Power supply current	$I_{CC}5$	VCC	Operating frequency F_{CP}=80MHz, Fcpp=40MHz, at normal operation		-	60	80	mA	
			Operating frequency F_{CP}=80MHz, Fcpp=40MHz, at Flash write		-	70	90	mA	
			Operating frequency F_{CP}=80MHz, Fcpp=40MHz, at Flash erase		-	70	90	mA	
			Operating frequency F_{CP}=64MHz, Fcpp=32MHz, at normal operation		-	54	71	mA	
			Operating frequency F_{CP}=64MHz, Fcpp=32MHz, at Flash write		-	64	81	mA	
			Operating frequency F_{CP}=64MHz, Fcpp=32MHz, at Flash erase		-	64	81	mA	
			Operating frequency F_{CP}=48MHz, Fcpp=24MHz, at normal operation		-	46	62	mA	
			Operating frequency F_{CP}=48MHz, Fcpp=24MHz, at Flash write		-	56	72	mA	
			Operating frequency F_{CP}=48MHz, Fcpp=24MHz, at Flash erase		-	56	72	mA	
	$I_{CCS}5$		Operating frequency F_{CP}=80MHz, Fcpp=40MHz, at CPU sleep mode		-	45	61	mA	
	$I_{CCBS}5$		Operating frequency F_{CP}=80MHz, Fcpp=40MHz, at bus sleep mode		-	23	51	mA	
	$I_{CCT}5$		Watch mode	When using crystal 4MHz T_A=+25°C*	-	1500	2610	µA	
				When using built-in CR clock 50kHz T_A=+25°C*	-	450	2000		
				When using sub clock 32kHz T_A=+25°C*	-	460	2000		
	$I_{CCH}5$		Stop mode	T_A=+25°C*	-	450	2000	µA	
	$I_{CCT}52$		Watch mode (power off)	When using crystal 4MHz T_A=+25°C*	-	1100	1300	µA	LVD/ RTC operation, Backup RAM 8KB retention
				When using built-in CR clock 50kHz , T_A=+25°C*	-	77	267		
				When using sub clock 32kHz T_A=+25°C*	-	100	285		
	$I_{CCH}52$		Stop mode (power off)	T_A=+25°C*	-	74	265	µA	Backup RAM 8KB retention

(T_A: -40°C to +125°C, V_{CC}= AVcc=5.0V±10%/3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions		Value Min	Value Typ	Value Max	Unit	Remarks
Power supply current	$I_{CC}5$	VCC	Operating frequency F_{CP}=80MHz, Fcpp=40MHz, at normal operation		-	60	102	mA	
			Operating frequency F_{CP}=80MHz, Fcpp=40MHz, at Flash write		-	70	115	mA	
			Operating frequency F_{CP}=80MHz, Fcpp=40MHz, at Flash erase		-	70	115	mA	
			Operating frequency F_{CP}=64MHz, Fcpp=32MHz, at normal operation		-	54	92	mA	
			Operating frequency F_{CP}=64MHz, Fcpp=32MHz, at Flash write		-	64	105	mA	
			Operating frequency F_{CP}=64MHz, Fcpp=32MHz, at Flash erase		-	64	105	mA	
			Operating frequency F_{CP}=48MHz, Fcpp=24MHz, at normal operation		-	46	82	mA	
			Operating frequency F_{CP}=48MHz, Fcpp=24MHz, at Flash write		-	56	95	mA	
			Operating frequency F_{CP}=48MHz, Fcpp=24MHz, at Flash erase		-	56	95	mA	
	$I_{CCS}5$		Operating frequency F_{CP}=80MHz, Fcpp=40MHz, at CPU sleep mode		-	45	82	mA	
	$I_{CCBS}5$		Operating frequency F_{CP}=80MHz, Fcpp=40MHz, at bus sleep mode		-	23	72	mA	
	$I_{CCT}5$		Watch mode	When using crystal 4MHz T_A=+25°C*	-	1500	2610	µA	
				When using built-in CR clock 50kHz T_A=+25°C*	-	450	2000		
				When using sub clock 32kHz T_A=+25°C*	-	460	2000		
	$I_{CCH}5$		Stop mode	T_A=+25°C*	-	450	2000	µA	
	$I_{CCT}52$		Watch mode (power off)	When using crystal 4MHz T_A=+25°C*	-	1100	1300	µA	LVD/ RTC operation, Backup RAM 8KB retention
				When using built-in CR clock 50kHz , T_A=+25°C*	-	77	267		
				When using sub clock 32kHz T_A=+25°C*	-	100	285		
	$I_{CCH}52$		Stop mode (power off)	T_A=+25°C*	-	74	265	µA	Backup RAM 8KB retention

(T_A: -40°C to +125°C, V_{CC}= AV_{CC}=5.0V ± 10%/Vcc=AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input leak current	I_{IL}	All input pins	V_{CC}=AV_{CC}=5.5V V_{SS}<V_I<V_{CC}	-5	-	5	µA	
Input capacitance 1	C_{IN1}	Other than VCC,VSS, AVCC, AVSS, C	-	-	5	15	pF	
Pull-up resistance	R_{UP1}	RSTX, NMIX	V_{CC}=5.0V±10%	25	-	100	kΩ	
			Vcc=3.3V±0.3V	45	-	140		
	R_{UP2}	P073,074 076,077	V_{CC}=5.0V±10%	25	-	60		
			Vcc=3.3V±0.3V	33	-	90		
	R_{UP3}	Port pin other than P035, 041, 073, 074, 076, 077, 093, 122	V_{CC}=5.0V±10%	25	-	100	kΩ	
			Vcc=3.3V±0.3V	45	-	140		
"H" level output voltage	V_{OH1}	Normal output pin	Vcc=4.5V I_{OH}=-4.0mA	V_{CC} -0.5	-	V_{CC}	V	
			Vcc=3.0V I_{OH}=-2.0mA					
	V_{OH2}	P073,074,076, 077	Vcc=4.5V I_{OH}=-3.0mA	V_{CC} -0.5	-	V_{CC}	V	I^2C pin output
	V_{OH3}	P103 to 106	Vcc=4.5V I_{OH}=-12.0mA	V_{CC} -0.5	-	V_{CC}	V	
			Vcc=3.0V I_{OH}=-8.0mA					
"L" level output voltage	V_{OL1}	Normal output pin	Vcc=4.5V I_{OL}=4.0mA	0	-	0.4	V	
			Vcc=3.0V I_{OL}=2.0mA					
	V_{OL2}	P073,074,076, 077	Vcc=4.5V I_{OL}=3.0mA	0	-	0.4	V	I^2C pin output
	V_{OL3}	P103 to 106	Vcc=4.5V I_{OL}=12.0mA	0	-	0.4	V	
			Vcc=3.0V I_{OL}=8.0mA					
"H" level input voltage	V_{IH1}	P000,002,003, 005,020,022, 024,026,150, 151,035,041, 045,055,057, 071-077,081, 082,093,096, 097,100-102, 111,115,116, 122,126,130, 134,142,143, 144,153	CMOS hysteresis input level	0.7× V_{CC}	-	V_{CC}	V	
	V_{IH3}	Port other than V_{IH1}	Automotive input level	0.8× V_{CC}	-	V_{CC}	V	
	V_{IH5}	RSTX,NMIX, MD0,MD1	CMOS hysteresis input level	0.8× V_{CC}	-	V_{CC}	V	

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
	V_{IHT}	DEBUGIF	TTL input level	2	-	V_{CC}	V	
"L" level input voltage	V_{IL1}	P000,002,003, 005,020,022, 024,026,150, 151,035,041, 045,055,057, 071-077,081, 082,093,096, 097,100-102, 111,115,116, 122,126,130, 134,142,143, 144,153	CMOS hysteresis input level	Vss	-	0.3× V_{CC}	V	
	V_{IL3}	Port other than V_{IH1}	Automotive input level	Vss	-	0.5× V_{CC}	V	
	V_{IL5}	RSTX,NMIX, MD0,MD1	CMOS hysteresis input level	Vss	-	0.2× V_{CC}	V	
	V_{ILT}	DEBUGIF	TTL input level	Vss	-	0.8	V	

*: It is a standard in BRAMSC (Backup RAM sleep control bit)=1(Enter the state of the sleep at the standby mode) condition.

4. AC Characteristics

(1) Main Clock Timing

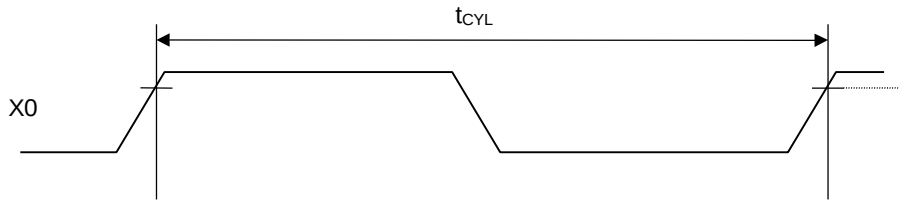
(T_A: -40°C to +125°C, V_{CC}= AV_{CC}=5.0V ± 10%/V_{CC}=AV_{CC}=3.3V±0.3V, V_{SS} =AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Source oscillation clock frequency	F_C	X0, X1	-	-	4	16	MHz	
Source oscillation clock cycle time	t_{CYL}	X0, X1		62.5	250	-	ns	
Internal operating clock frequency*1	F_{CP}	-		2	-	80	MHz	CPU clock
	F_{CPP}			1		40		Peripheral bus clock
	F_{CPT}			1		40		External bus clock (When V_{CC}=5.0V is used) *2
				1		32		External bus clock (When V_{CC}=3.3V is used)
Internal operating clock cycle time*1	t_{CP}	-	-	12.5	-	500	ns	CPU clock
	t_{CPP}			25		1000		Peripheral bus clock
	t_{CPT}			25		1000		External bus clock (When V_{CC}=5.0V is used)
				31.25		1000		External bus clock (When V_{CC}=3.3V is used)
CAN PLL jitter (during lock)	t_{PJ}	-		-10	-	10	ns	F_{CP}=80MHz (4MHz×Multiplied by 20)
Built-in CR oscillation frequency	F_{CCR}	-		50	100	150	kHz	

*1: The maximum / minimum value is defined when using the main clock and PLL clock.

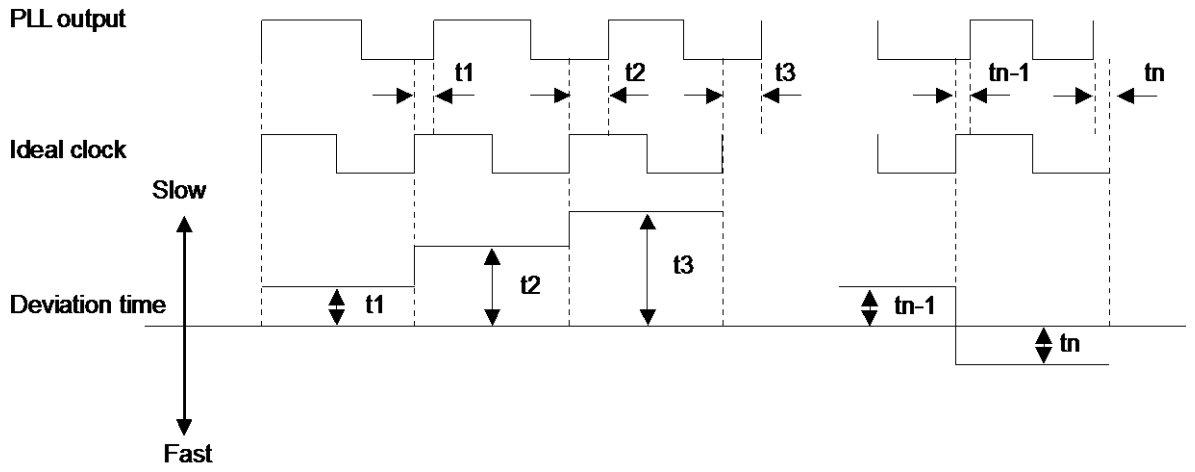
*2: Please use it with external load capacity 12pF or less for VCC=3.3V±0.3V (40MHz operation).

・X0,X1 clock timing



・CAN PLL jitter

Deviation time from the ideal clock is assured per cycle out of 20, 000 cycles.

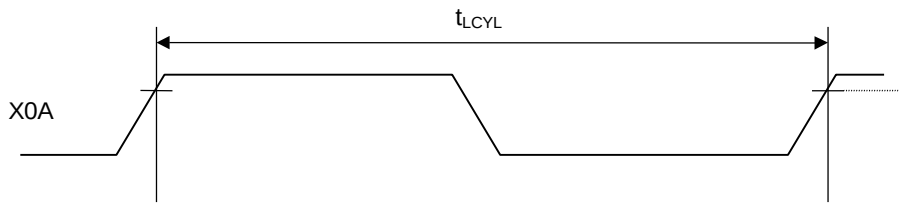


(1-2) Sub clock timing

(T_A: -40°C to +125°C, V_{CC}= AV_{CC}=5.0V ± 10%/V_{CC}=AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

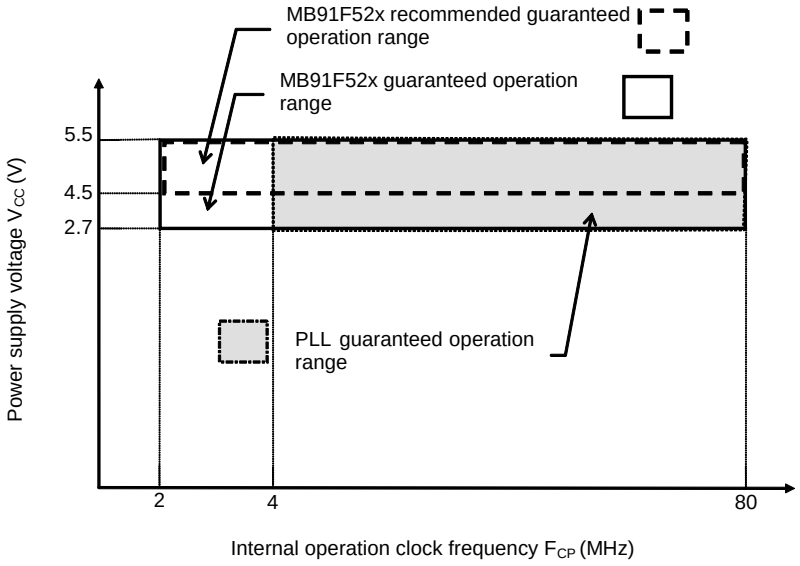
Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Source oscillation clock frequency	F_{CL}	X0A, X1A	-	-	32.768	-	kHz	
Source oscillation clock cycle time	t_{LCYL}	X0A, X1A		-	30.52	-	µs	

・X0A,X1A clock timing



・Guaranteed operation range

Internal operation clock frequency vs. Power supply voltage

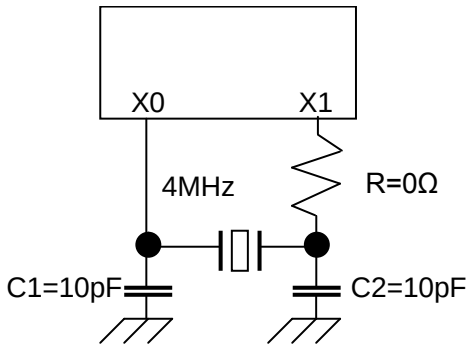


Note: The power supply voltage, which is the low-voltage detection setting voltage or lower, is in the reset state.

Oscillation clock frequency vs. Internal operation clock frequency

		Internal operation clock frequency							
		Main Clock	PLL clock						
			Multiplied by 1	Multiplied by 2	Multiplied by 3	Multiplied by 4	...	Multiplied by 19	Multiplied by 20
Oscillation clock frequency	4MHz	2MHz	4MHz	8MHz	12MHz	16MHz	...	76MHz	80MHz

・Example of oscillation circuit

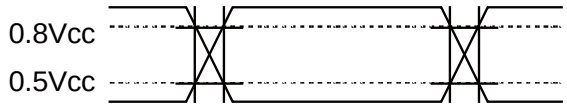


Note: As to the product with its clock supervisor's initial value is "ON", when the oscillator is unable to start within 20ms from the stop state the clock supervisor will detect the oscillation stop. As a result, the CPU moves to the fail safe operation.
Design your print circuit board so that the oscillator can start oscillation within 20ms.
Moreover, it is recommended to be designed after the match evaluation of the circuit is requested to the departure pendulum maker when the oscillation circuit is composed.

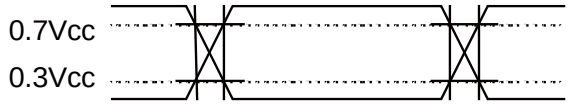
AC characteristics are specified by the following measurement reference voltage values.

● Input Signal Waveform

Hysteresis Input Pin (Automotive)



Hysteresis Input Pin (CMOS schmitt)



● Output Signal Waveform

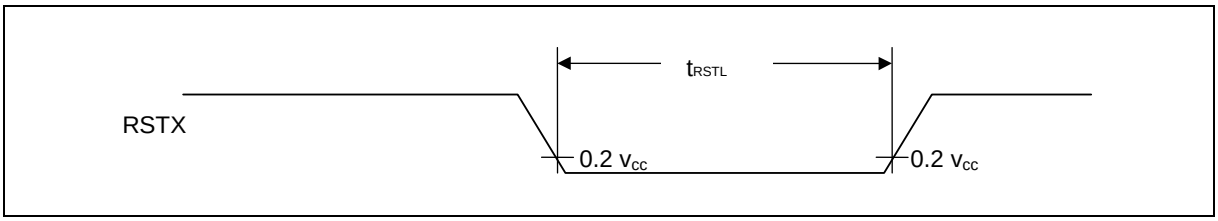
Output Pin

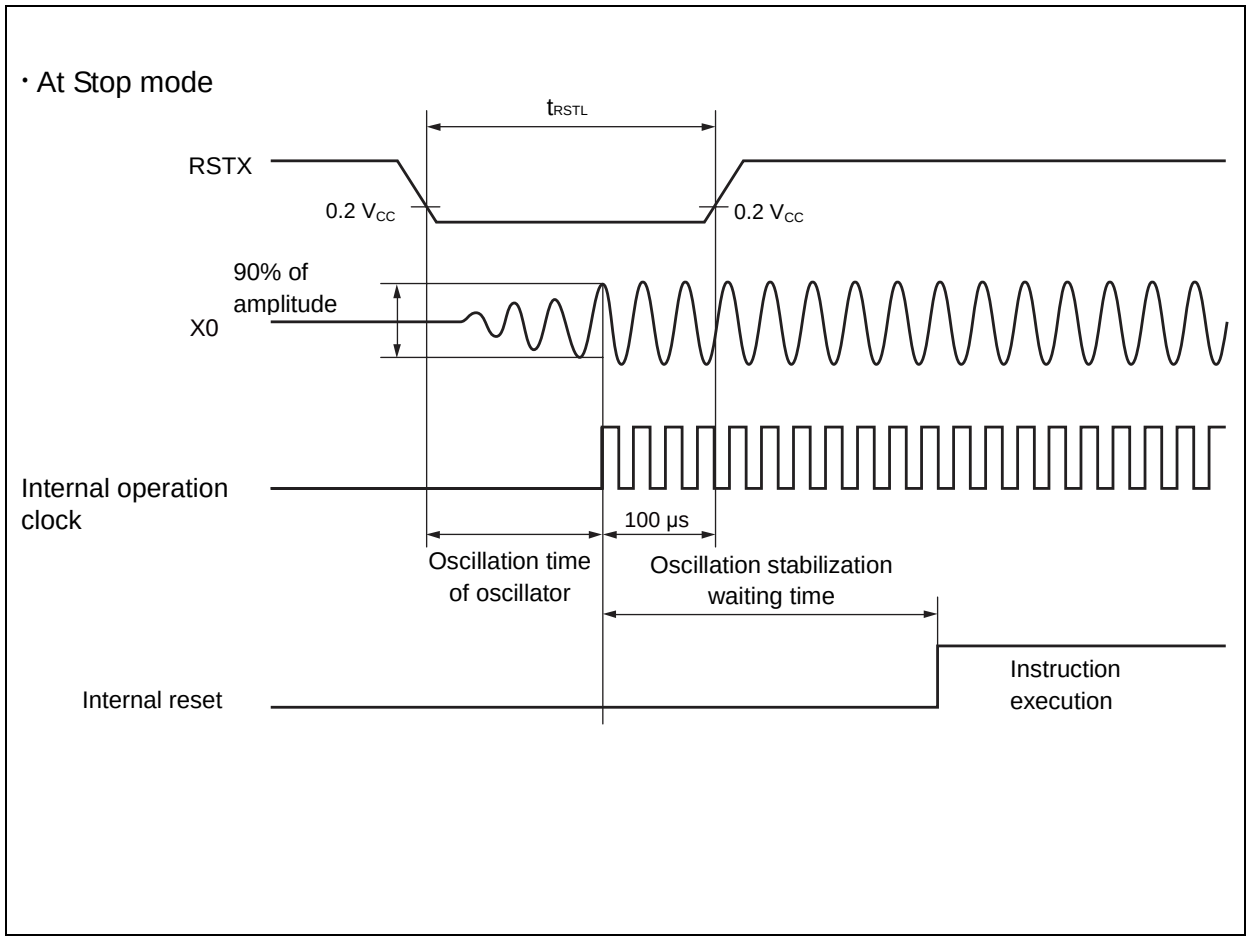
(2) Reset Input

(T_A: -40°C to +125°C, V_{CC}= AV_{CC}=5.0V ± 10%/V_{CC}=AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Reset input time	t_{RSTL}	RSTX	–	10	–	µs	When normal operation
				Oscillation time of oscillator* +100	–	µs	At Stop mode
				100	–	µs	At Watch mode
Width for reset input removal				1	–	µs	

*: The oscillation time of the oscillator is the time it takes for the amplitude of the oscillations to reach 90%. For crystal oscillators, this time is between several ms and several tens of ms, for ceramic oscillators the time is between several hundred µs and several ms, and for an external clock, the time is 0 ms.





(3) Power-on Conditions

(T_A: -40°C to +125°C, V_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Level detection voltage	–	V_{CC}	–	2.024	2.2	2.376	V	
Level detection hysteresis width	–	V_{CC}	–	–	100	–	mV	
Level detection time	–	–	–	–	–	30	µs	*1
Slope detection undetected standard	–	V_{CC}	V_{CC} = at level detection release level time	–	–	4	mV/µs	*2
Power off time	t_{OFF}	V_{CC}	–	50	–	–	ms	*3

*1: If the fluctuation of the power supply is faster than the low voltage detection time, there is the possibility to generate or release after the power supply voltage has exceeded the detection voltage range.

*2: When setting the power supply fluctuation to this standard or less, it is possible to suppress the slope detection. This is the standard when the power supply fluctuation is stable.

*3: This time is to start the slope detection at next power on after power down and internal charge loss.

(4) Multi-function Serial

(4-1) CSIO timing

(4-1-1) Bit setting: SMR: MD2=0, SMR: MD1=1, SMR : MD0=0, SMR: SCINV=0, SCR:SPI=0

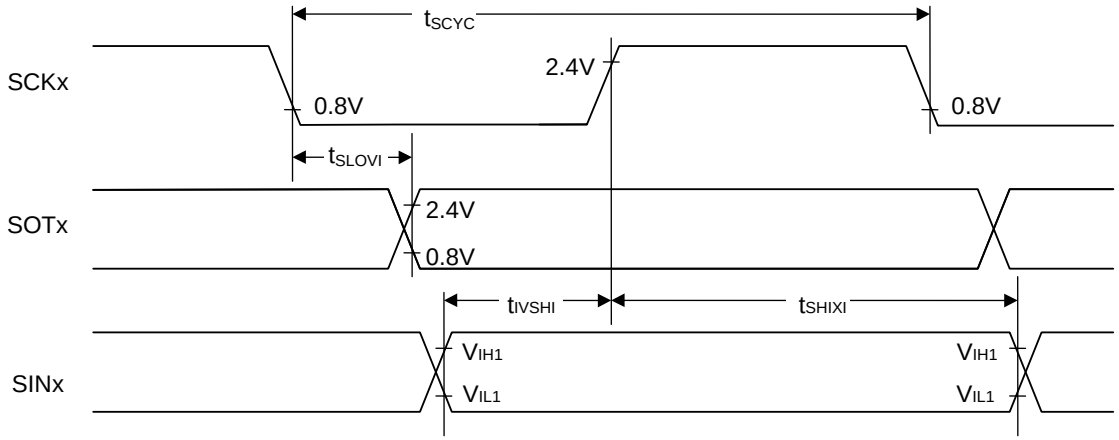
(T_A: -40°C to +125°C, V_{CC}= AV_{CC}=5.0V ± 10%/V_{CC}=AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0 to SCK11	-	$4t_{CPP}$	-	ns	Internal shift clock mode output pin : C_L=50pF
SCK ↓ → SOT delay time	t_{SLOVI}	SCK0 to SCK2, SCK5 to SCK11 SOT0 to SOT2, SOT5 to SOT11		-30	30	ns	
		SCK3 , SCK4 SOT3 , SOT4		-300	300	ns	
Valid SIN → SCK ↑ setup time	t_{IVSHI}	SCK0 to SCK2, SCK5 to SCK11 SIN0 to SIN2, SIN5 to SIN11		34	-	ns	
		SCK3 , SCK4 SIN3 , SIN4		300	-	ns	
SCK ↑ → Valid SIN hold time	t_{SHIXI}	SCK0 to SCK11 SIN0 to SIN11		0	-	ns	
Serial clock "H"pulse width	t_{SHSL}	SCK0 to SCK11	-	t_{CPP}+10	-	ns	External shift clock mode output pin: C_L=50pF
Serial clock "L" pulse width	t_{SLSH}			$2t_{CPP}$-10	-	ns	
SCK ↓ → SOT delay time	t_{SLOVE}	SCK0 to SCK2, SCK5 to SCK11 SOT0 to SOT2, SOT5 to SOT11		-	33	ns	
		SCK3 , SCK4 SOT3 , SOT4		-	300	ns	
Valid SIN → SCK ↑ setup time	t_{IVSHE}	SCK0 to SCK11 SIN0 to SIN11		10	-	ns	
SCK ↑ → Valid SIN hold time	t_{SHIXE}			20	-	ns	
SCK fall time	t_F	SCK0 to SCK11		-	5	ns	
SCK rise time	t_R	SCK0 to SCK11		-	5	ns	

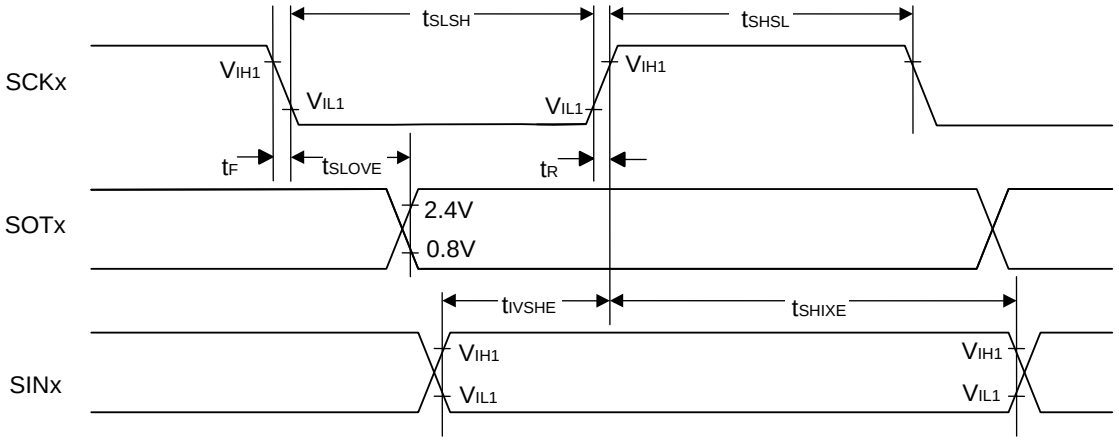
Notes:

- AC characteristic in CLK synchronized mode.
- C_L is the load capacitance applied to pins during testing.
- The maximum bard rate is limited by internal operation clock used and other parameters. Please use ch.3 and ch.4 with maximum baud rate 400kbps or less.
  See Hardware Manual for details.

・Internal shift clock mode



・External shift clock mode



(4-1-2) Bit setting: SMR: MD2=0, SMR: MD1=1, SMR : MD0=0, SMR: SCINV=1, SCR:SPI=0

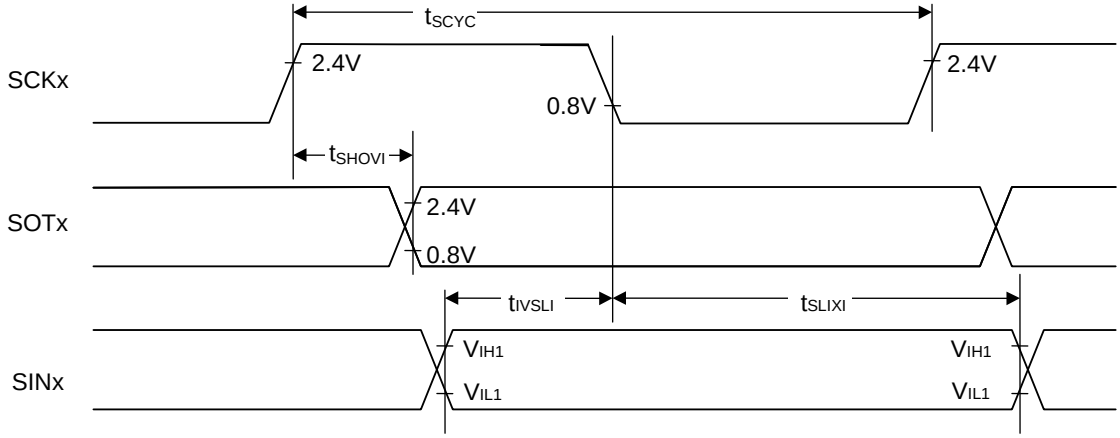
(T_A: -40°C to +125°C, V_{CC}= AV_{CC}=5.0V ± 10%/V_{CC}=AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0 to SCK11	-	$4t_{CPP}$	-	ns	Internal shift clock mode output pin : C_L=50pF
SCK ↑ → SOT delay time	t_{SHOVI}	SCK0 to SCK2, SCK5 to SCK11 SOT0 to SOT2, SOT5 to SOT11		-30	30	ns	
		SCK3 , SCK4 SOT3 , SOT4		-300	300	ns	
Valid SIN → SCK ↓ setup time	t_{IVSLI}	SCK0 to SCK2, SCK5 to SCK11 SIN0 to SIN2, SIN5 to SIN11		34	-	ns	
		SCK3 , SCK4 SIN3, SIN4		300	-	ns	
SCK ↓ → Valid SIN hold time	t_{SLIXI}	SCK0 to SCK11 SIN0 to SIN11		0	-	ns	
Serial clock "H"pulse width	t_{SHSL}	SCK0 to SCK11	-	t_{CPP}+10	-	ns	External shift clock mode output pin: C_L=50pF
Serial clock "L" pulse width	t_{SLSH}			$2t_{CPP}$-10	-	ns	
SCK ↑ → SOT delay time	t_{SHOVE}	SCK0 to SCK2, SCK5 to SCK11 SOT0 to SOT2, SOT5 to SOT11		-	33	ns	
		SCK3 , SCK4 SOT3 , SOT4		-	300	ns	
Valid SIN → SCK ↓ setup time	t_{IVSLE}	SCK0 to SCK11 SIN0 to SIN11		10	-	ns	
SCK ↓ → Valid SIN hold time	t_{SLIXE}			20	-	ns	
SCK fall time	t_F	SCK0 to SCK11		-	5	ns	
SCK rise time	t_R	SCK0 to SCK11		-	5	ns	

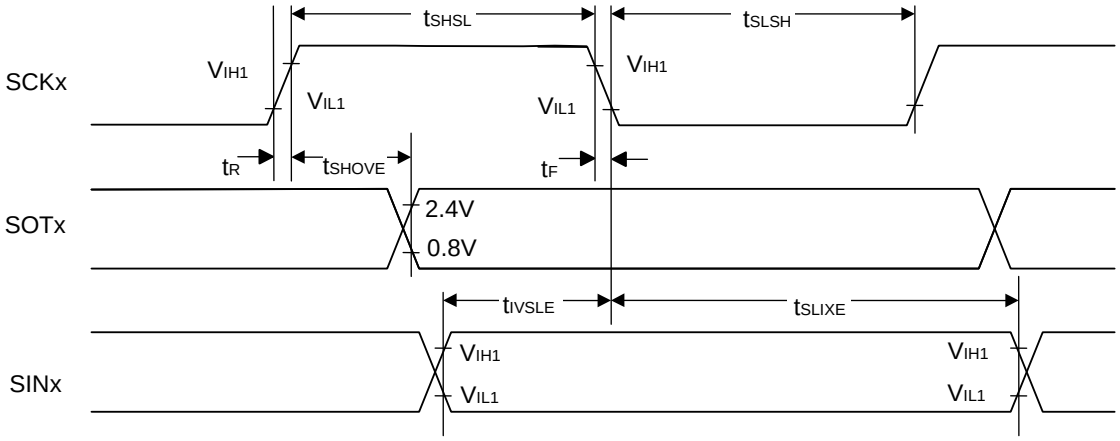
Notes:

- AC characteristic in CLK synchronized mode.
- C_L is the load capacitance applied to pins during testing.
- The maximum bard rate is limited by internal operation clock used and other parameters. Please use ch.3 and ch.4 with maximum baud rate 400kbps or less.
  See Hardware Manual for details.

・Internal shift clock mode



・External shift clock mode



(4-1-3) Bit setting: SMR : MD2=0, SMR:MD1=1, SMR : MD0=0, SMR:SCINV=0, SCR:SPI=1

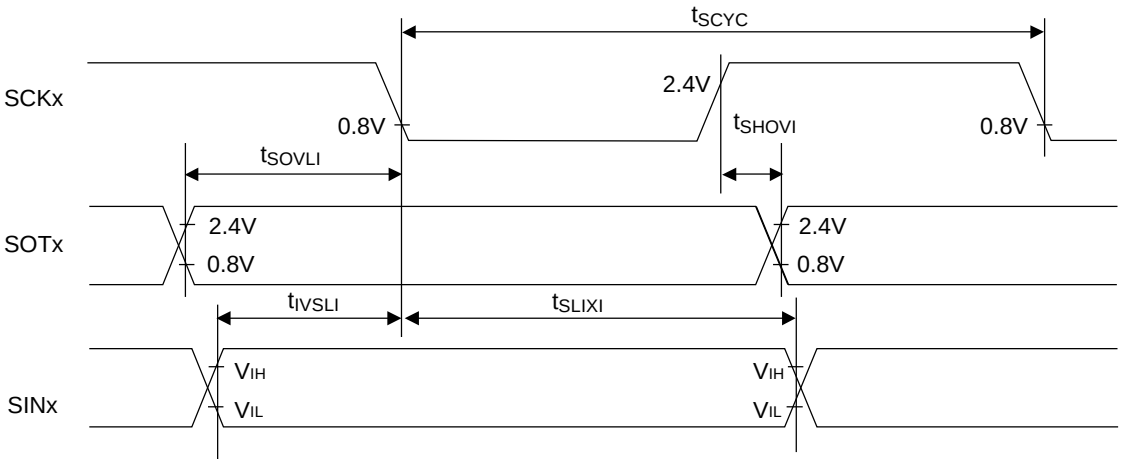
(T_A:-40°C to +125°C, V_{CC}=AV_{CC}=5.0V±10%/V_{CC}=AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0 to SCK11	-	$4t_{CPP}$	-	ns	Internal shift clock mode output pin : C_L=50pF
SCK ↑ → SOT delay time	t_{SHOVI}	SCK0 to SCK2, SCK5 to SCK11 SOT0 to SOT2, SOT5 to SOT11		-30	30	ns	
		SCK3 , SCK4 SOT3 , SOT4		-300	300	ns	
Valid SIN → SCK ↓ setup time	t_{IVSLI}	SCK0 to SCK2, SCK5 to SCK11 SIN0 to SIN2, SIN5 to SIN11		34	-	ns	
		SCK3 , SCK4 SIN3 , SIN4		300	-	ns	
SCK ↓ → Valid SIN hold time	t_{SLIXI}	SCK0 to SCK11 SIN0 to SIN11		0	-	ns	
SOT→SCK ↓ delay time	t_{SOVLI}	SCK0 to SCK11 SOT0 to SOT11		$2t_{CPP}$-30	-	ns	
Serial clock "H"pulse width	t_{SHSL}	SCK0 to SCK11	-	t_{CPP}+10	-	ns	External shift clock mode output pin: C_L=50pF
Serial clock "L" pulse width	t_{SLSH}			$2t_{CPP}$-10	-	ns	
SCK ↑ → SOT delay time	t_{SHOVE}	SCK0 to SCK2, SCK5 to SCK11 SOT0 to SOT2, SOT5 to SOT11		-	33	ns	
		SCK3 , SCK4 SOT3 , SOT4		-	300	ns	
Valid SIN → SCK ↓ setup time	t_{IVSHE}	SCK0 to SCK11 SIN0 to SIN11		10	-	ns	
SCK ↓ → Valid SIN hold time	t_{SLIXE}			20	-	ns	
SCK fall time	t_F	SCK0 to SCK11		-	5	ns	
SCK rise time	t_R	SCK0 to SCK11		-	5	ns	

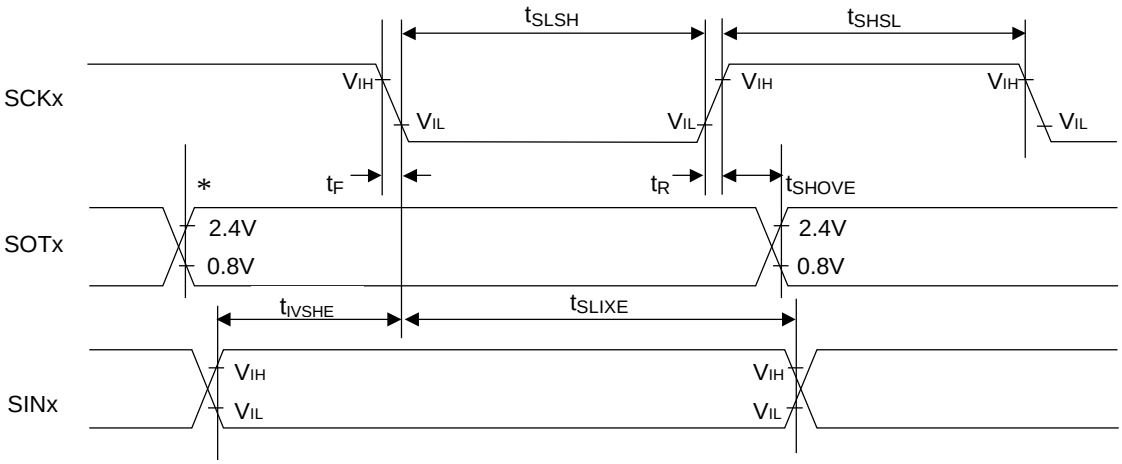
Notes:

- AC characteristic in CLK synchronized mode.
- C_L is the load capacitance applied to pins during testing.
- The maximum bard rate is limited by internal operation clock used and other parameters. Please use ch.3 and ch.4 with maximum baud rate 400kbps or less.
  See Hardware Manual for details.

・Internal shift clock mode



・External shift clock mode



*: It writes in the TDR register and, then, it changes.

(4-1-4) Bit setting: SMR : MD2=0, SMR:MD1=1, SMR : MD0=0, SMR:SCINV=1, SCR:SPI=1

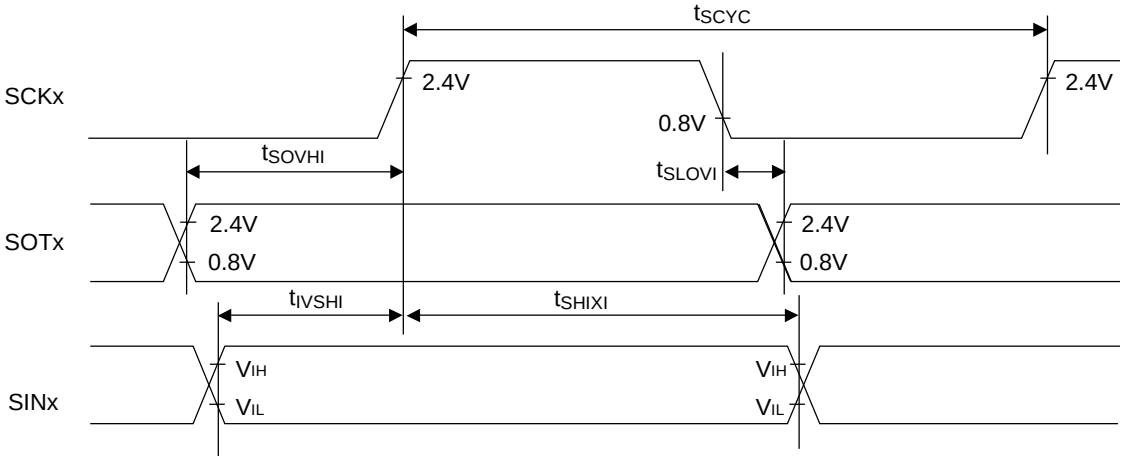
(T_A:-40°C to +125°C, V_{CC}=AV_{CC}=5.0V±10%/V_{CC}=AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0 to SCK11	-	$4t_{CPP}$	-	ns	Internal shift clock mode output pin : C_L=50pF
SCK ↓ → SOT delay time	t_{SLOVI}	SCK0 to SCK2, SCK5 to SCK11 SOT0 to SOT2, SOT5 to SOT11		-30	30	ns	
		SCK3 , SCK4 SOT3 , SOT4		-300	300	ns	
Valid SIN → SCK ↑ setup time	t_{IVSHI}	SCK0 to SCK2, SCK5 to SCK11 SIN0 to SIN2, SIN5 to SIN11		34	-	ns	
		SCK3 , SCK4 SIN3 , SIN4		300	-	ns	
SCK ↑ → Valid SIN hold time	t_{SHIXI}	SCK0 to SCK11 SIN0 to SIN11		0	-	ns	
SOT→SCK ↑ delay time	t_{SOVHI}	SCK0 to SCK11 SOT0 to SOT11		$2t_{CPP}$-30	-	ns	
Serial clock "H"pulse width	t_{SHSL}	SCK0 to SCK11	-	t_{CPP}+10	-	ns	External shift clock mode output pin: C_L=50pF
Serial clock "L" pulse width	t_{SLSH}			$2t_{CPP}$-10	-	ns	
SCK ↓ → SOT delay time	t_{SLOVE}	SCK0 to SCK2, SCK5 to SCK11 SOT0 to SOT2, SOT5 to SOT11		-	33	ns	
		SCK3 , SCK4 SOT3 , SOT4		-	300	ns	
Valid SIN → SCK ↑ setup time	t_{IVSHE}	SCK0 to SCK11 SIN0 to SIN11		10	-	ns	
SCK ↑ → Valid SIN hold time	t_{SHIXE}			20	-	ns	
SCK fall time	t_F	SCK0 to SCK11		-	5	ns	
SCK rise time	t_R	SCK0 to SCK11		-	5	ns	

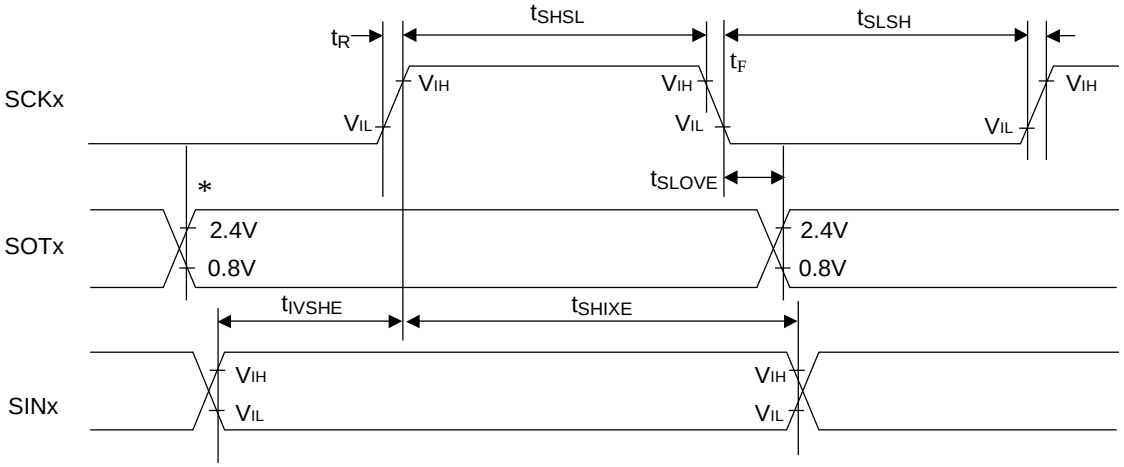
Notes:

- AC characteristic in CLK synchronized mode.
- C_L is the load capacitance applied to pins during testing.
- The maximum bard rate is limited by internal operation clock used and other parameters. Please use ch.3 and ch.4 with maximum baud rate 400kbps or less.
  See Hardware Manual for details.

・Internal shift clock mode



・External shift clock mode



*: It writes in the TDR register and, then, it changes.

(4-1-5) Bit setting: SMR:MD2=0, SMR:MD1=1, SMR:MD0=0,
When Serial chip select is used : SCSCR:CSEN=1,
Serial clock output mark level "H" : SMR,SCSFR:SCINV=0,
Serial chip select Inactive level "H" : SCSCR,SCSFR:CSLVL=1
(T_A:-40°C to +125°C, V_{CC}=AV_{CC}=5.0V±10%/V_{CC}=AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS ↓ →SCK ↓ setup time	t_{CSSI}	SCK1, SCK2, SCK5 to SCK11 SCS1 , SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11	-	t_{CSSU}-50 *1	t_{CSSU}+0 *1	ns	Internal shift clock mode output pin : C_L=50pF
		SCK3 , SCK4 SCS3 , SCS40 to SCS43		t_{CSSU}-50 *1	t_{CSSU}+300 *1	ns	
SCK ↑ →SCS ↑ hold time	t_{CSHI}	SCK1 , SCK2, SCK5 to SCK11 SCS1 , SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11		t_{CSHD}-10 *2	t_{CSHD}+50 *2	ns	
		SCK3 , SCK4 SCS3 , SCS40 to SCS43		t_{CSHD}-300 *2	t_{CSHD}+50 *2	ns	
SCS deselect time	t_{CSDI}	SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11		t_{CSDS}-50 *3	t_{CSDS}+50 *3	ns	
SCS ↓ →SCK ↓ setup time	t_{CSSE}	SCK1 to SCK11 SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11	-	$3t_{CPP}$+30	-	ns	External shift clock mode output pin: C_L=50pF
SCK ↑ →SCS ↑ hold time	t_{CSHE}			+0	-	ns	
SCS deselect time	t_{CSDE}	SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11		$3t_{CPP}$+30	-	ns	
SCS ↓ →SOT delay time	t_{DSE}	SCS1 , SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11 SOT1 , SOT2 , SOT5 to SOT11		-	40	ns	
		SCS3, SCS40 to SCS43 SOT3 , SOT4		-	300	ns	

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS ↑ →SOT delay time	t_{DEE}	SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11 SOT1 to SOT11	-	+0	-	ns	External shift clock mode output pin: C_L=50pF
SCK ↓ →SCS ↓ clock switch time	t_{SCC}	SCK1 , SCK2, SCK5 to SCK11 SCS1 , SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11	-	$3t_{CPP}$-10	$3t_{CPP}$+50	ns	Internal shift clock mode Round operation output pin: C_L=50pF
		SCK3 , SCK4 SCS3 , SCS40 to SCS43		$3t_{CPP}$-300	$3t_{CPP}$+50	ns	

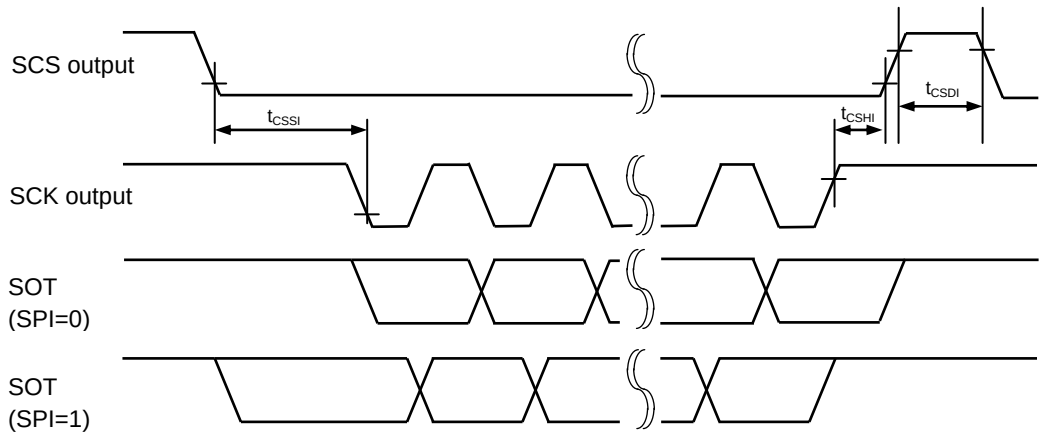
*1: t_{CSSU} =SCSTR:CSSU7-0×Serial chip select timing operating clock

*2: t_{CSHD}=SCSTR:CSHD7-0×Serial chip select timing operating clock

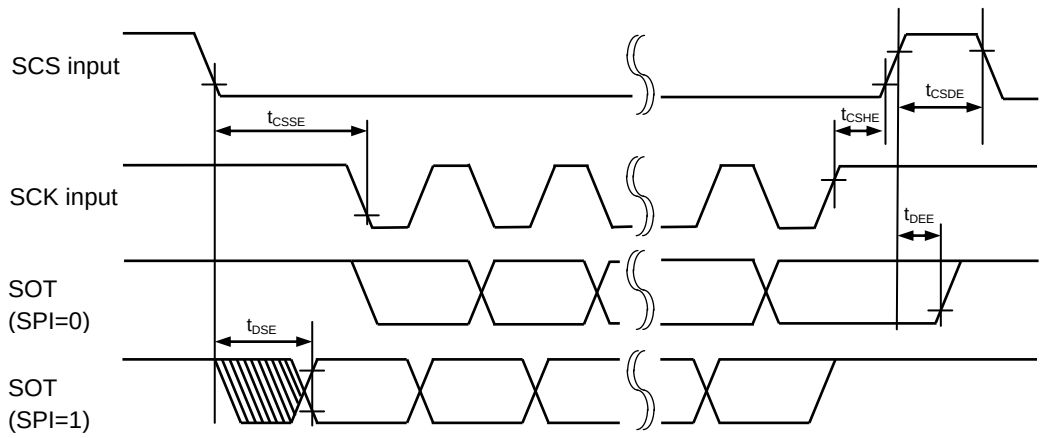
*3: t_{CSDS}=SCSTR:CSDS15-0×Serial chip select timing operating clock

Regardless of the deselect time setting, once after the serial chip select pin becomes inactive, it will take at least five peripheral bus clock cycles to be active again

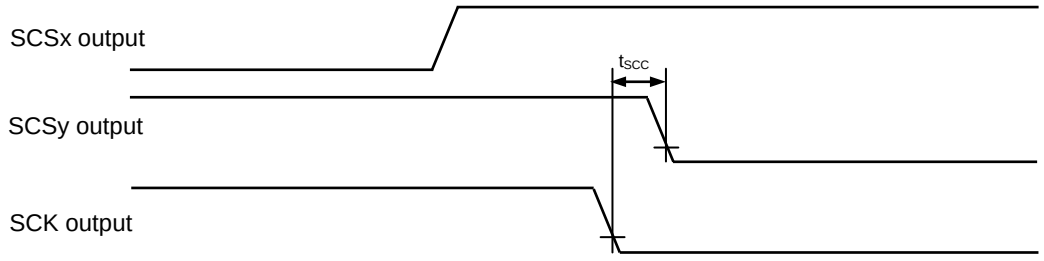
Please see the hardware manual for details of above-mentioned *1,*2, and *3.



When Serial chip select is used , Serial clock output mark level "H"
,Serial chip select Inactive level "H"
Internal shift clock mode



When Serial chip select is used , Serial clock output mark level "H"
,Serial chip select Inactive level "H"
External shift clock mode



When Serial chip select is used , Serial clock output mark level "H"
,Serial chip select Inactive level "H"
Internal shift clock mode , Example of switching clock by round operation (x,y=0,1,2,3)

(4-1-6) Bit setting: SMR:MD2=0, SMR:MD1=1, SMR:MD0=0,
When Serial chip select is used : SCSCR:CSEN=1,
Serial clock output mark level "L" : SMR,SCSFR:SCINV=1,
Serial chip select Inactive level "H" : SCSCR,SCSFR:CSLVL=1
(T_A:-40°C to +125°C, V_{CC}=AV_{CC}=5.0V±10%/V_{CC}=AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS ↓ →SCK ↑ setup time	t_{CSSI}	SCK1 , SCK2, SCK5 to SCK11 SCS1 , SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11	-	t_{CSSU}-50 *1	t_{CSSU}+0 *1	ns	Internal shift clock mode output pin : C_L=50pF
		SCK3 , SCK4 SCS3 , SCS40 to SCS43		t_{CSSU}-50 *1	t_{CSSU}+300 *1	ns	
SCK ↓ →SCS ↑ hold time	t_{CSHI}	SCK1 , SCK2, SCK5 to SCK11 SCS1 , SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11		t_{CSHD}-10 *2	t_{CSHD}+50 *2	ns	
		SCK3 , SCK4 SCS3 , SCS40 to SCS43		t_{CSHD}-300 *2	t_{CSHD}+50 *2	ns	
SCS deselect time	t_{CSDI}	SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11		t_{CSDS}-50 *3	t_{CSDS}+50 *3	ns	
SCS ↓ →SCK ↑ setup time	t_{CSSE}	SCK1 to SCK11 SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11	-	$3t_{CPP}$+30	-	ns	External shift clock mode output pin: C_L=50pF
SCK ↓ →SCS ↑ hold time	t_{CSHE}			+0	-	ns	
SCS deselect time	t_{CSDE}	SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11		$3t_{CPP}$+30	-	ns	
SCS ↓ →SOT delay time	t_{DSE}	SCS1 , SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11 SOT1 , SOT2, SOT5 to SOT11		-	40	ns	
		SCS3, SCS40 to SCS43 SOT3 , SOT4		-	300	ns	

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS ↑ →SOT delay time	t_{DEE}	SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11 SOT1 to SOT11	-	+0	-	ns	External shift clock mode output pin: C_L=50pF
SCK ↑ →SCS ↓ clock switch time	t_{SCC}	SCK1 , SCK2, SCK5 to SCK11 SCS1 , SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11	-	$3t_{CPP}$-10	$3t_{CPP}$+50	ns	Internal shift clock mode Round operation output pin: C_L=50pF
		SCK3 , SCK4 SCS3 , SCS40 to SCS43		$3t_{CPP}$-300	$3t_{CPP}$+50	ns	

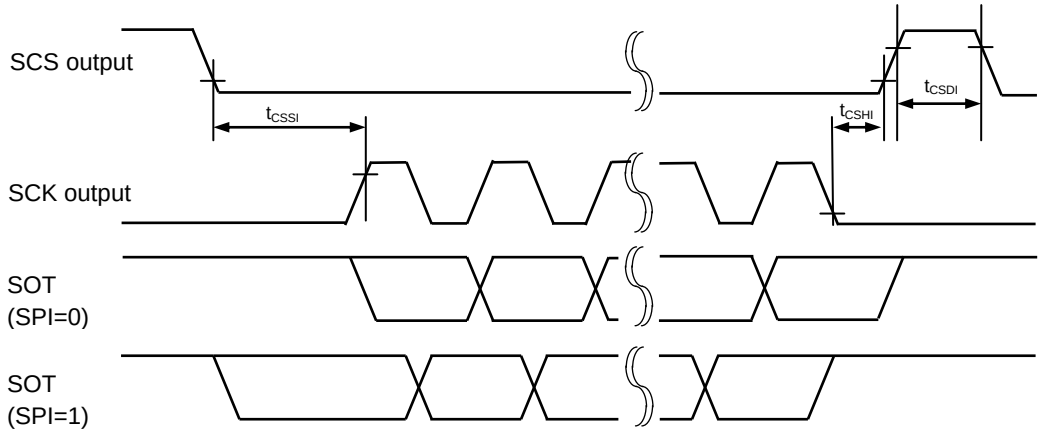
*1: t_{CSSU} =SCSTR:CSSU7-0×Serial chip select timing operating clock

*2: t_{CSHD}=SCSTR:CSHD7-0×Serial chip select timing operating clock

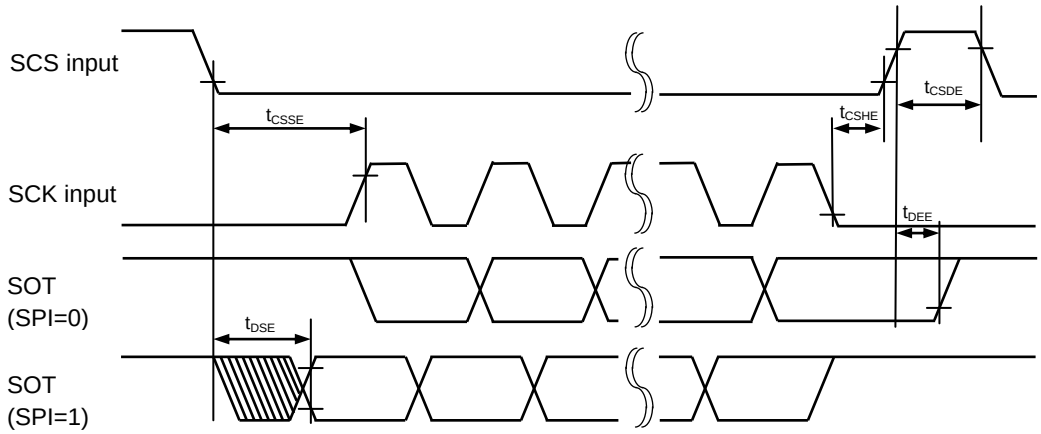
*3: t_{CSDS}=SCSTR:CSDS15-0×Serial chip select timing operating clock

Regardless of the deselect time setting, once after the serial chip select pin becomes inactive, it will take at least five peripheral bus clock cycles to be active again

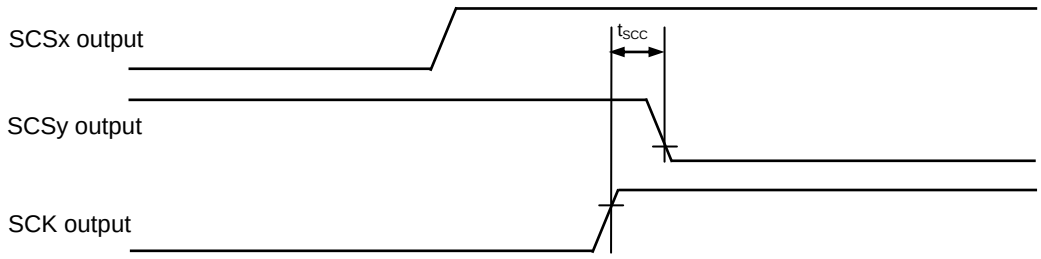
Please see the hardware manual for details of above-mentioned *1,*2, and *3



When Serial chip select is used , Serial clock output mark level "L",
Serial chip select Inactive level "H"
Internal shift clock mode



When Serial chip select is used , Serial clock output mark level "L",
Serial chip select Inactive level "H"
External shift clock mode



When Serial chip select is used , Serial clock output mark level "L",
Serial chip select Inactive level "H"
Internal shift clock mode , Example of switching clock by round operation (x,y=0,1,2,3)

(4-1-7) Bit setting: SMR:MD2=0, SMR:MD1=1, SMR:MD0=0,
When Serial chip select is used : SCSCR:CSEN=1,
Serial clock output mark level "H" : SMR,SCSFR:SCINV=0,
Serial chip select Inactive level "L" : SCSCR,SCSFR:CSLVL=0
(T_A:-40°C to +125°C, V_{CC}=AV_{CC}=5.0V±10%/V_{CC}=AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS ↑ →SCK ↓ setup time	t_{CSSI}	SCK1 , SCK2, SCK5 to SCK11 SCS1 , SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11	-	t_{CSSU}-50 *1	t_{CSSU}+0 *1	ns	Internal shift clock mode output pin : C_L=50pF
		SCK3 , SCK4 SCS3 , SCS40 to SCS43		t_{CSSU}-50 *1	t_{CSSU}+300 *1	ns	
SCK ↑ →SCS ↓ hold time	t_{CSHI}	SCK1 to SCK2, SCK5 to SCK11 SCS1 , SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11		t_{CSHD}-10 *2	t_{CSHD}+50 *2	ns	
		SCK3 , SCK4 SCS3 , SCS40 to SCS43		t_{CSHD}-300 *2	t_{CSHD}+50 *2	ns	
SCS deselect time	t_{CSDI}	SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11		t_{CSDS}-50 *3	t_{CSDS}+50 *3	ns	
SCS ↑ →SCK ↓ setup time	t_{CSSE}	SCK1 to SCK11 SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11	-	$3t_{CPP}$+30	-	ns	External shift clock mode output pin: C_L=50pF
SCK ↑ →SCS ↓ hold time	t_{CSHE}			+0	-	ns	
SCS deselect time	t_{CSDE}	SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11		$3t_{CPP}$+30	-	ns	
SCS ↑ →SOT delay time	t_{DSE}	SCS1 , SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11 SOT1 , SOT2, SOT5 to SOT11		-	40	ns	
		SCS3 , SCS40 to SCS43 SOT3 , SOT4		-	300	ns	

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS ↓ →SOT delay time	t_{DEE}	SCS1 to ~SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11 SOT1 to SOT11	-	+0	-	ns	External shift clock mode output pin: C_L=50pF
SCK ↓ →SCS ↑ clock switch time	t_{SCC}	SCK1 , SCK2, SCK5 to SCK11 SCS1 , SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11	-	$3t_{CPP}$-10	$3t_{CPP}$+50	ns	Internal shift clock mode Round operation output pin: C_L=50pF
		SCK3 , SCK4 SCS3 , SCS40 to SCS43		$3t_{CPP}$-300	$3t_{CPP}$+50	ns	

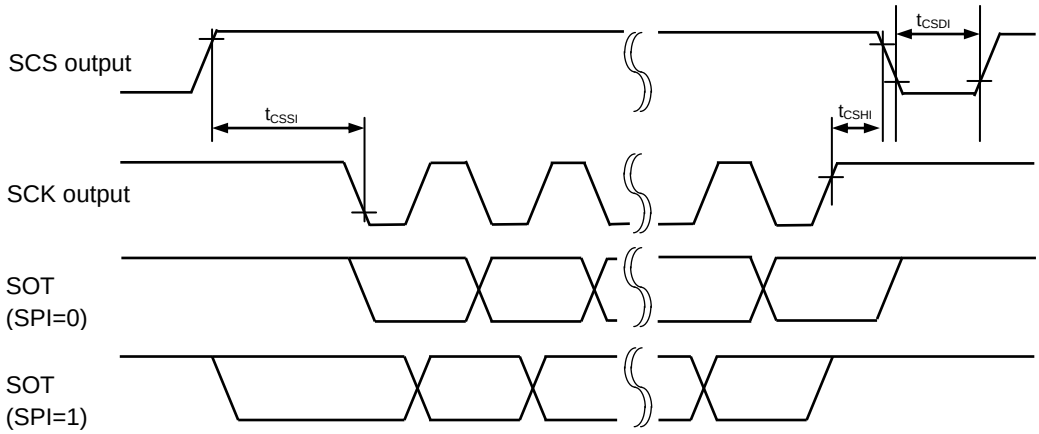
*1: t_{CSSU} =SCSTR:CSSU7-0×Serial chip select timing operating clock

*2: t_{CSHD}=SCSTR:CSHD7-0×Serial chip select timing operating clock

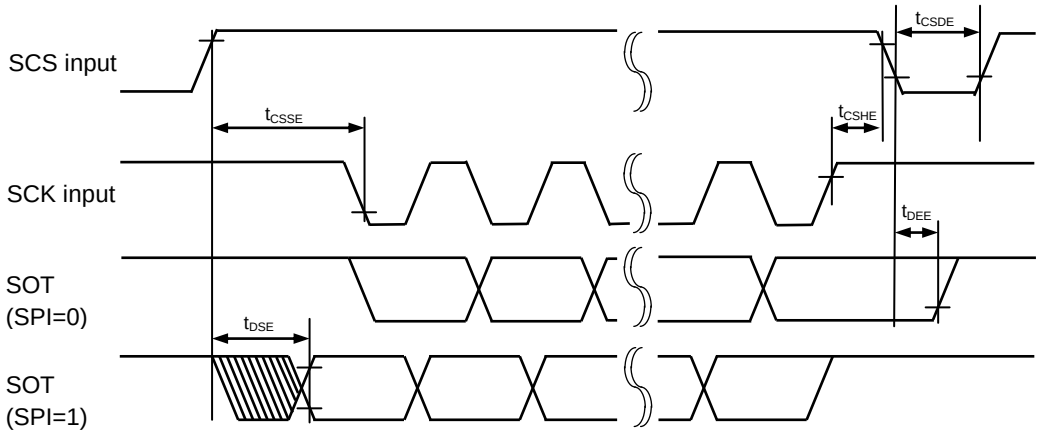
*3: t_{CSDS}=SCSTR:CSDS15-0×Serial chip select timing operating clock

Regardless of the deselect time setting, once after the serial chip select pin becomes inactive, it will take at least five peripheral bus clock cycles to be active again

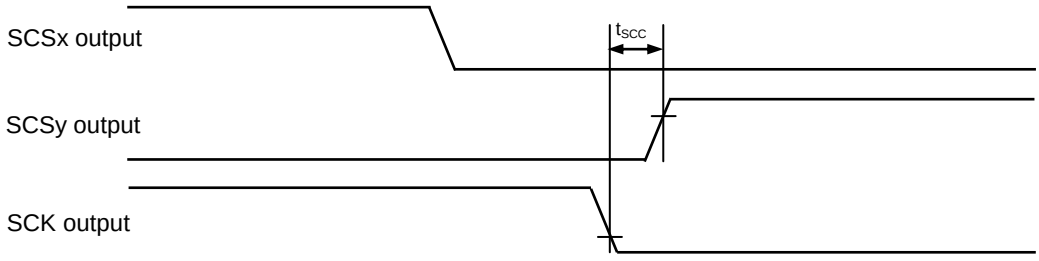
Please see the hardware manual for details of above-mentioned *1,*2, and *3.



When Serial chip select is used , Serial clock output mark level "H",
Serial chip select Inactive level "L"
Internal shift clock mode



When Serial chip select is used , Serial clock output mark level "H",
Serial chip select Inactive level "L"
External shift clock mode



When Serial chip select is used , Serial clock output mark level "H",
Serial chip select Inactive level "L"
Internal shift clock mode , Example of switching clock by round operation (x,y=0,1,2,3)

(4-1-8) Bit setting: SMR:MD2=0, SMR:MD1=1, SMR:MD0=0,
When Serial chip select is used: SCSCR:CSEN=1,
Serial clock output mark level "L" : SMR,SCSFR:SCINV=1,
Serial chip select Inactive level "L" : SCSCR,SCSFR:CSLVL=0
(T_A:-40°C to +125°C, V_{CC}=AV_{CC}=5.0V±10%/V_{CC}=AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS ↑ →SCK ↑ setup time	t_{CSSI}	SCK1 , SCK2, SCK5 to SCK11 SCS1 , SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11	-	t_{CSSU}-50 *1	t_{CSSU}+0 *1	ns	Internal shift clock mode output pin : C_L=50pF
		SCK3 , SCK4 SCS3 , SCS40 to SCS43		t_{CSSU}-50 *1	t_{CSSU}+300 *1	ns	
SCK ↓ →SCS ↓ hold time	t_{CSHI}	SCK1 , SCK2, SCK5 to SCK11 SCS1 , SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11		t_{CSHD}-10 *2	t_{CSHD}+50 *2	ns	
		SCK3 , SCK4 SCS3 , SCS40 to SCS43		t_{CSHD}-300 *2	t_{CSHD}+50 *2	ns	
SCS deselect time	t_{CSDI}	SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11		t_{CSDS}-50 *3	t_{CSDS}+50 *3	ns	
SCS ↑ →SCK ↑ setup time	t_{CSSE}	SCK1 to SCK11 SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11	-	$3t_{CPP}$+30	-	ns	External shift clock mode output pin: C_L=50pF
SCK ↓ →SCS ↓ hold time	t_{CSHE}			+0	-	ns	
SCS deselect time	t_{CSDE}	SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11		$3t_{CPP}$+30	-	ns	
SCS ↑ →SOT delay time	t_{DSE}	SCS1 , SCS2, SCS50~SCS53, SCS60~SCS63, SCS70~SCS73, SCS8~SCS11 SOT1 , SOT2, SOT5~SOT11		-	40	ns	
		SCS3 , SCS40~SCS43 SOT3 ,SOT4		-	300	ns	

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS ↓ →SOT delay time	t_{DEE}	SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11 SOT1 to SOT11	-	+0	-	ns	External shift clock mode output pin: C_L=50pF
SCK ↑ →SCS ↑ clock switch time	t_{SCC}	SCK1 , SCK2, SCK5 to SCK11 SCS1 , SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11	-	$3t_{CPP}$-10	$3t_{CPP}$+50	ns	Internal shift clock mode Round operation output pin: C_L=50pF
		SCK3 , SCK4 SCS3 , SCS40 to SCS43		$3t_{CPP}$-300	$3t_{CPP}$+50		

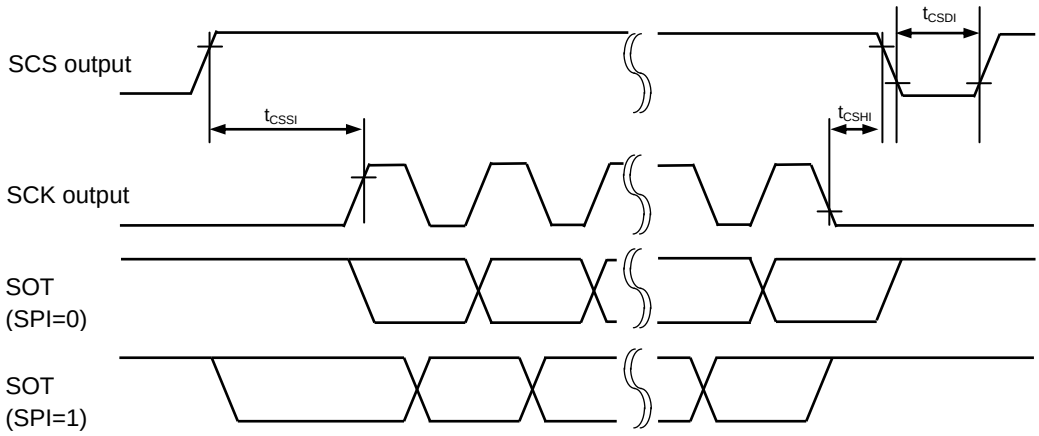
*1: t_{CSSU} =SCSTR:CSSU7-0×Serial chip select timing operating clock

*2: t_{CSHD}=SCSTR:CSHD7-0×Serial chip select timing operating clock

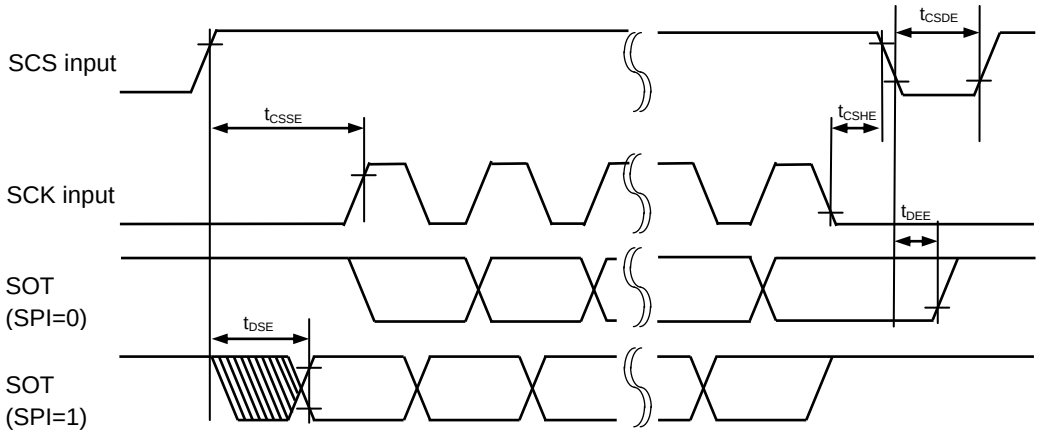
*3: t_{CSDS}=SCSTR:CSDS15-0×Serial chip select timing operating clock

Regardless of the deselect time setting, once after the serial chip select pin becomes inactive, it will take at least five peripheral bus clock cycles to be active again

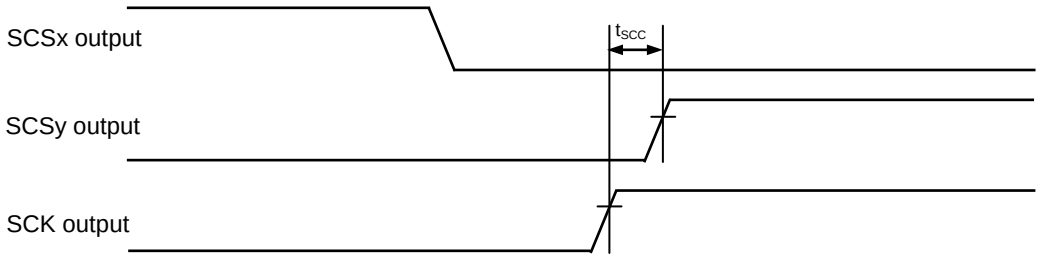
Please see the hardware manual for details of above-mentioned *1,*2, and *3.



When Serial chip select is used , Serial clock output mark level "L",
Serial chip select Inactive level "L"
Master mode



When Serial chip select is used , Serial clock output mark level "L",
Serial chip select Inactive level "L"
Slave mode



When Serial chip select is used , Serial clock output mark level "L",
Serial chip select Inactive level "L"
Master mode, Example of switching clock by round operation (x,y=0,1,2,3)

(4-2) UART (Asynchronous serial interface) timing

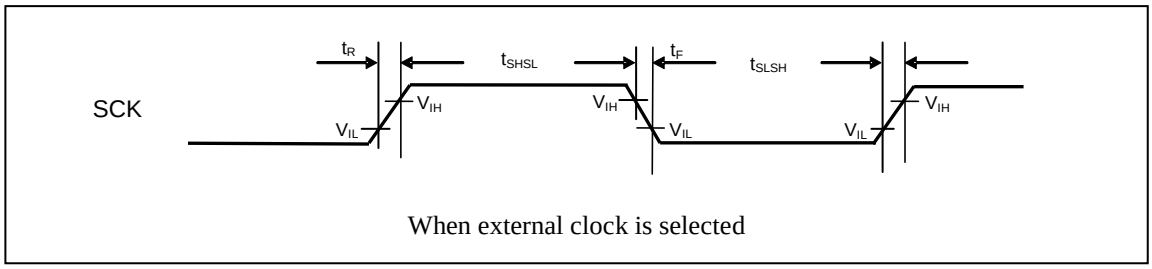
Bit setting: SMR : MD2=0, SMR:MD1=0, SMR : MD0=0

Bit setting: SMR : MD2=0, SMR:MD1=0, SMR : MD0=1

When external clock is selected (BGR:EXT=1)

(T_A:-40°C to +125°C, V_{CC}=AV_{CC}=5.0V±10%/V_{CC}=AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock "L" pulse width	t_{SLSH}	SCK0 to SCK11	-	t_{CPP}+10	-	ns	output pin: C_L=50pF
Serial clock "H"pulse width	t_{SHSL}			t_{CPP}+10	-	ns	
SCK fall time	t_F			-	5	ns	
SCK rise time	t_R			-	5	ns	



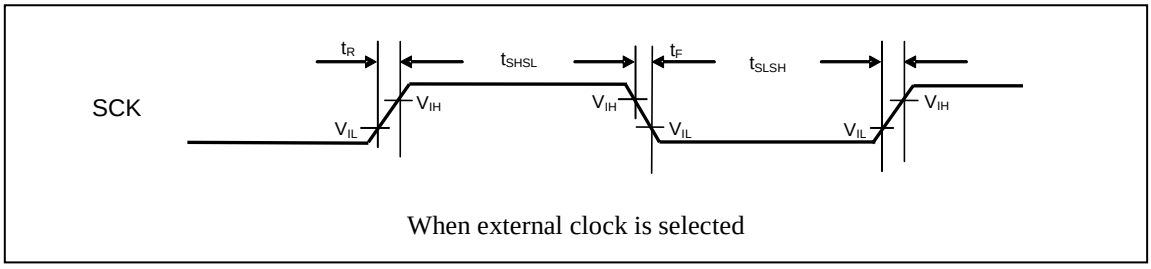
When external clock is selected

(4-3) LIN Interface (v2.1)(Asynchronous Serial Interface for LIN (v2.1)) timing

Bit setting: SMR : MD2=0, SMR:MD1=1, SMR : MD0=1

(T_A:-40°C to +125°C, V_{CC}=AV_{CC}=5.0V±10%/V_{CC}=AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock "L" pulse width	t_{SLSH}	SCK0 to SCK11	-	t_{CPP}+10	-	ns	output pin: C_L=50pF
Serial clock "H"pulse width	t_{SHSL}			t_{CPP}+10	-	ns	
SCK fall time	t_F			-	5	ns	
SCK rise time	t_R			-	5	ns	



When external clock is selected

(4-4) I^2C timing

(T_A: -40°C to +125°C, V_{CC}= AV_{CC}=5.0V ± 10%/V_{CC}=AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Standard mode		High-speed mode*3		Unit	Remarks
				Min	Max	Min	Max		
SCL clock frequency	f_{SCL}	SCK3 to SCK11	C_L=50pF R = (V_P/I_{OL}) *1	0	100	0	400	kHz	
Repeat "start" condition hold time SDA ↓ → SCL ↓	t_{HDSTA}	SOT3 to SOT11, (SDA) SCK3 to SCK11, (SCL)		4.0	–	0.6	–	µs	
Period of "L" for SCL clock	t_{LOW}	SCK3 to SCK11, (SCL)		4.7	–	1.3	–	µs	
Period of "H" for SCL clock	t_{HIGH}	SCK3 to SCK11, (SCL)		4.0	–	0.6	–	µs	
Repeat "start" condition setup time SCL ↑ → SDA ↓	t_{SUSTA}	SCK3 to SCK11, (SCL)		4.7	–	0.6	–	µs	
Data hold time SCL ↓ → SDA ↓ ↑	t_{HDDAT}	SOT3 to SOT11, (SDA) SCK3 to SCK11, (SCL)		0	3.45*2	0	0.9*3	µs	
Data setup time SDA ↓ ↑ → SCL ↑	t_{SUDAT}	SOT3 to SOT11, (SDA) SCK3 to SCK11, (SCL)		250	–	100	–	ns	
"Stop" condition setup time SCL ↑ → SDA ↑	t_{SUSTO}	SOT3 to SOT11, (SDA) SCK3 to SCK11, (SCL)		4.0	–	0.6	–	µs	
Bus-free time between "stop" condition and "start" condition	t_{BUF}	–		4.7	–	1.3	–	µs	
Noise filter	t_{SP}	–	–	$2t_{CPP}$ *4	–	$2t_{CPP}$ *4	–	ns	

Notes: Only ch.3 and ch.4 are standard mode/high-speed mode correspondence. In ch.5-ch.8, ch.10, and ch.11, only a standard mode is correspondences.

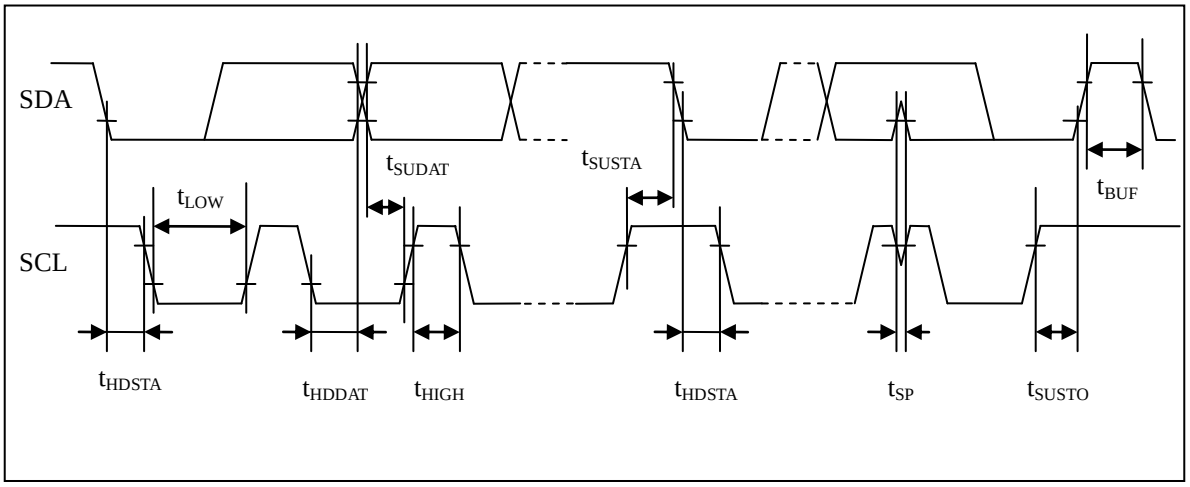
*1: R and C_L represent the pull-up resistance and load capacitance of the SCL and SDA output lines, respectively.
Vp shows that the power-supply voltage of the pull-up resistor and I_{OL} shows the V_{OL} guarantee current.

*2: The maximum t_{HDDAT} only has to be met if the device does not extend the "L" width (t_{LOW}) of the SCL signal.

*3: A high-speed mode I^2C bus device can be used on a standard mode I^2C bus system as long as the device satisfies the requirement of "$t_{SUDAT} \geq 250$ ns".

*4: t_{CPP} is the peripheral clock cycle time. Adjust the clock of the bus in the surrounding to 8MHz or more when use I^2C.

・ I^2C timing

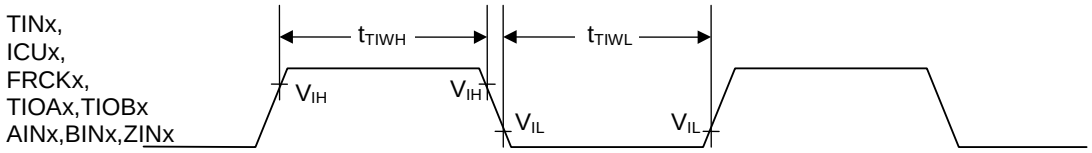

SDA
SCL
tLOW
tSUDAT
tSUSTA
tBUF
tHDSTA
tHDDAT
tHIGH
tHDSTA
tSP
tSUSTO

(5) Timer input timing

(T_A: -40°C to +125°C, V_{CC}= AV_{CC}=5.0V ± 10%/V_{CC}=AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH}, t_{TIWL}	TIN0 to TIN7 ICU0 to ICU9 FRCK0 to FRCK5 TIOA0, TIOA1, TIOB0, TIOB1, AIN0, AIN1, BIN0, BIN1, ZIN0, ZIN1	–	$4t_{CPP}$	–	ns	

・Timer input timing

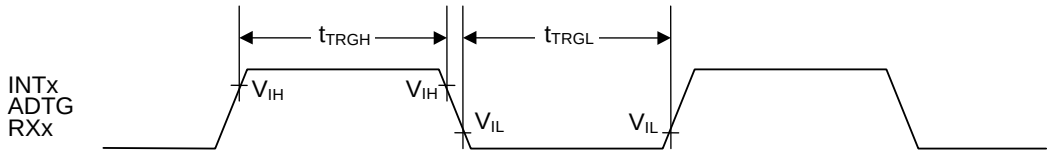


(6) Trigger input timing

(T_A: -40°C to +125°C, V_{CC}= AV_{CC}=5.0V ± 10%/V_{CC}=AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH}, t_{TRGL}	INT0 to INT15, ADTG, RX0, RX1, RX2	–	$5t_{CPP}$	–	ns	
				1	–	µs	At stop mode

・Trigger input timing

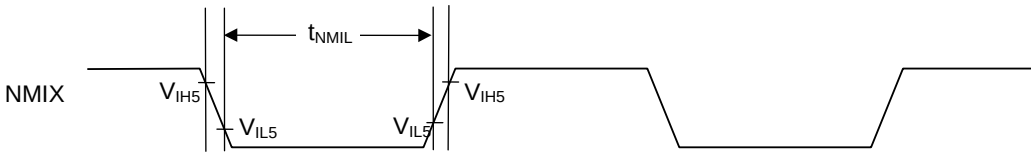


(7) NMI input timing

(T_A: -40°C to +125°C, V_{CC}= AV_{CC}=5.0V ± 10%/V_{CC}=AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{NMIL}	NMIX	–	$4t_{CPP}$	–	ns	

・NMIX input timing



(8) Low voltage detection (External low-voltage detection)

(T_A: -40°C to +125°C, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply voltage range	V_{DP5}	VCC	-	2.7	-	5.5	V	
Detection voltage	V_{DL}		*1	-8%	2.8	+8%	V	When power-supply voltage falls and detection level is set initially
Hysteresis width	V_{HYS}		-	-	0.1	-	V	When power-supply voltage rises
Low voltage detection time	Td	-		-	-	30	µs	
Power supply voltage regulation	-	VCC	-	-2	-	2	V/ms	*2

*1: If the fluctuation of the power supply is faster than the low voltage detection time, there is a possibility to generate or release after the power supply voltage has exceeded the detection voltage range.

*2: Please suppress the change of the power supply within the range of the power-supply voltage regulation to do a low voltage detection by detecting voltage (V_{DL}).

(9) Low voltage detection (Internal low-voltage detection)

(T_A: -40°C to +125°C, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply voltage range	V_{RDP5}	-	-	0.6	-	1.4	V	
Detection voltage	V_{RDL}		*	0.8	0.9	1.0	V	When power-supply voltage falls
Hysteresis width	V_{RHYS}		-	-	0.1	-	V	When power-supply voltage rises
Low voltage detection time	-	-		-	-	30	µs	

*: If the fluctuation of the power supply is faster than the low voltage detection time, there is a possibility to generate or release after the power supply voltage has exceeded the detection voltage range.

(10) External bus I/F (synchronous mode) timing

(T_A: -40°C to +105°C, V_{CC}=AV_{CC}=5.0V±10%/V_{CC}= AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)
(external load capacitance 50pF)

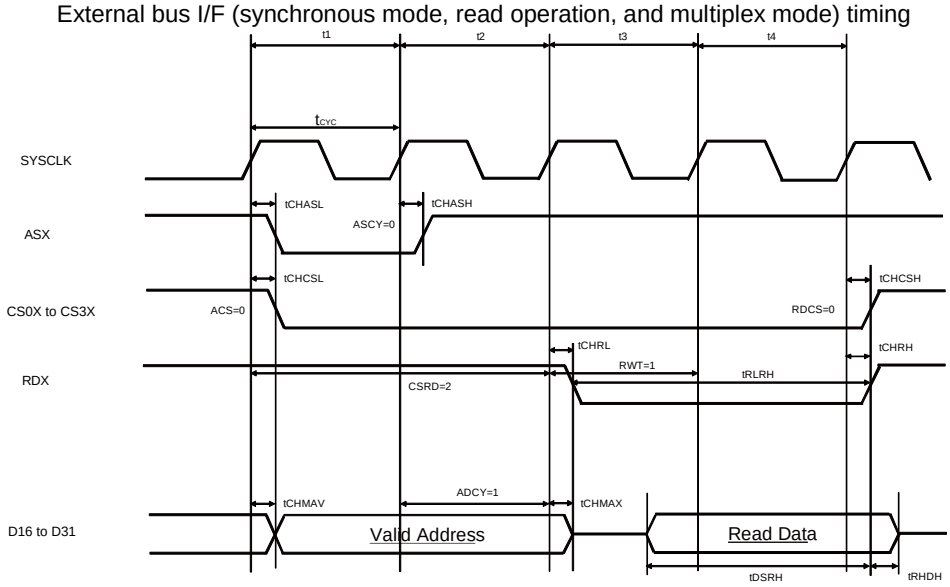
Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
Cycle time	t_{CYC}	SYSCLK	25	-	ns	V_{CC}=5.0V±10%*1
			31.25			V_{CC}=3.3V±0.3V
ASX delay time	t_{CHASL}, t_{CHASH}	SYSCLK ASX	0.5	18	ns	
CS0X to CS3X delay time	t_{CHCSL}, t_{CHCSH}	SYSCLK CS0X to CS3X	0.5	18	ns	
A00 to A21 delay time	t_{CHAV}, t_{CHAX}	SYSCLK A00 to A21	0.5	18	ns	
RDX delay time	t_{CHRL}, t_{CHRH}	SYSCLK RDX	0.5	18	ns	
RDX minimum pulse	t_{RLRH}	RDX	t_{CYC}× 2 - 20	-	ns	RWT=1, set RWT to 1 or more.*2
Data setup → RDX↑time	t_{DSRH}	RDX D16 to D31	18+t_{CYC}	-	ns	Same as above
RDX↑→ data hold	t_{RHDH}		0	-	ns	
WRnX delay time	t_{CHWL}, t_{CHWH}	SYSCLK WR0X, WR1X	0.5	18	ns	
WRnX minimum pulse	t_{WLWH}	WR0X, WR1X	t_{CYC} - 10	-	ns	WWT=0 *2
SYSCLK↑→ data output time	t_{CHDV}	SYSCLK D16 to D31	0.5	18	ns	
SYSCLK↑→ data hold time	t_{CHDX}		-	18	ns	Set WRCS to 1 or more.

Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
SYSCLK↑→ address output time	t_{CHMAV}	SYSCLK D16 to D31	0.5	18	ns	
SYSCLK↑→ address hold time	t_{CHMAX}		-	18	ns	In multiplex mode, set as follows: • Set CSWR and CSRD to 2 or more. • ASCY must satisfy the following conditions because of setting ADCY > ASCY and protocol violation prevention. ADCY +1 ≤ ACS + CSRD ADCY +1 ≤ ACS + CSWR ASCY + 1 ≤ ACS + CSRD ASCY + 1 ≤ ACS + CSWR See Hardware Manual for details.

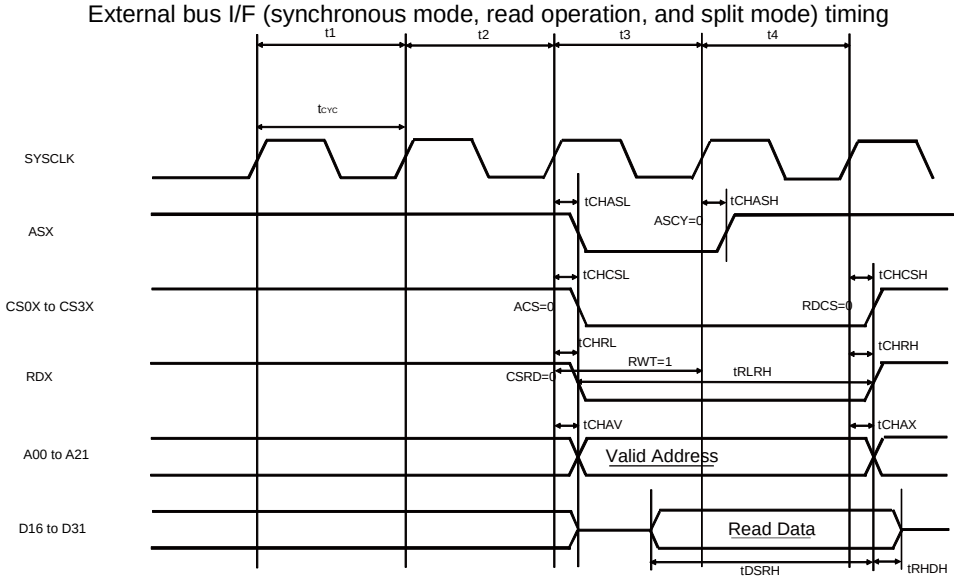
*1: Please use it with external load capacity 12pF or less for VCC=3.3V±0.3V (40MHz operation).

*2: If the bus is expanded by automatic wait insertion or RDY input, add time (t_{CYC} × the number of expanded cycles) to the rated value.

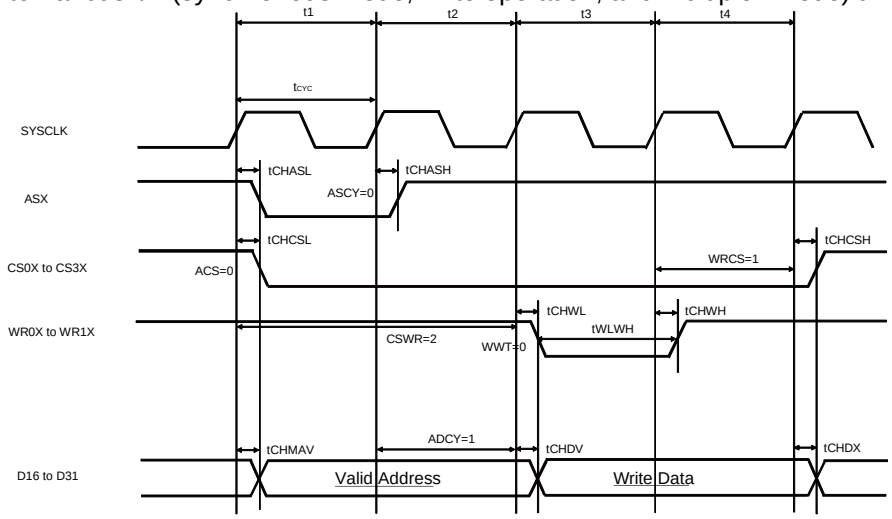
External bus I/F (synchronous mode, read operation, and multiplex mode) timing



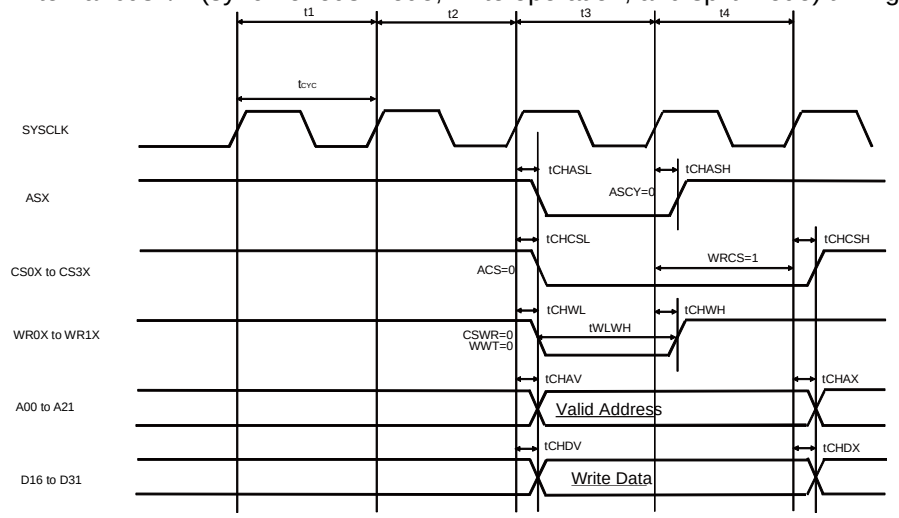
External bus I/F (synchronous mode, read operation, and split mode) timing



External bus I/F (synchronous mode, write operation, and multiplex mode) timing



External bus I/F (synchronous mode, write operation, and split mode) timing



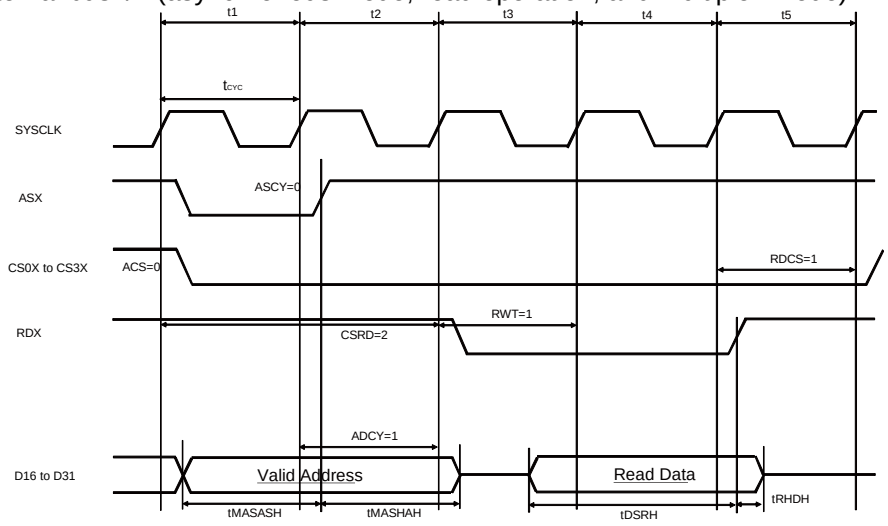
(11) External bus I/F (asynchronous mode) timing

(T_A: -40°C to +105°C, V_{CC}=AV_{CC}=5.0V±10%/V_{CC}= AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)
(external load capacitance 50pF)

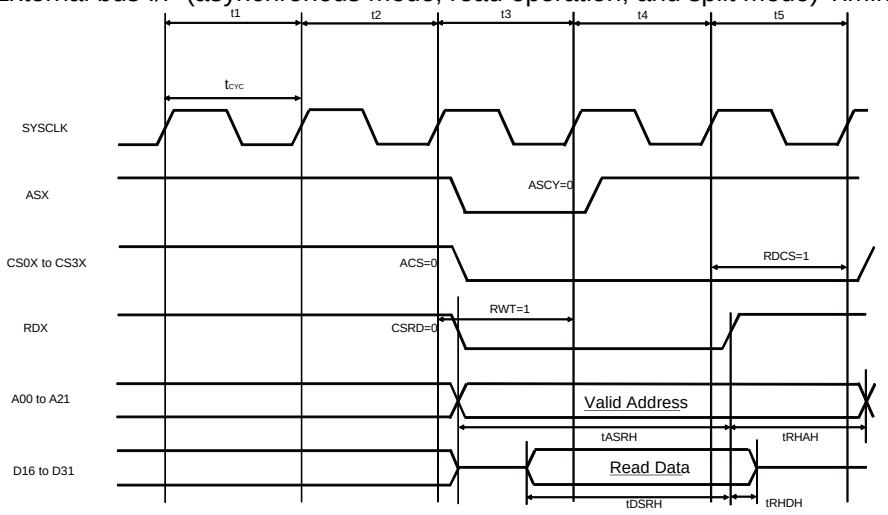
Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
Cycle time	t_{CYC}	SYSCLK	25	-	ns	V_{CC}=5.0V±10%*1
			31.25			V_{CC}=3.3V±0.3V
Address setup → RDX↑time	t_{ASRH}	RDX A00 to A21	$2\times t_{CYC}$ - 12	$2\times t_{CYC}$ + 12	ns	RWT=1, set RWT to 1 or more. *2
RDX↑→ Address hold	t_{RHAH}		t_{CYC} - 12	t_{CYC} + 12	ns	Set RDCS to 1 or more.
Data setup→ RDX↑time	t_{DSRH}	RDX D16 to D31	18 + t_{CYC}	-	ns	RWT=1, set RWT to 1 or more.
RDX↑→ Data hold	t_{RHDH}		0	-	ns	
Address setup→ WRnX↑time	t_{ASWH}	WR0X to WR1X A00 to A21	t_{CYC} - 12	t_{CYC} + 12	ns	WWT=0 *2
WRnX↑→ Address hold	t_{WHAH}		t_{CYC} - 12	t_{CYC} + 12	ns	Set WRCS to 1 or more.
Data setup→ WRnX↑time	t_{DSWH}	WR0X to WR1X D16 to D31	t_{CYC} - 16	t_{CYC} + 16	ns	WWT=0 *2
WRnX↑→ Data hold	t_{WHDH}		t_{CYC} - 16	t_{CYC} + 16	ns	Set WRCS to 1 or more.
Address setup → ASX↑time	t_{MASASH}	ASX D16 to D31	t_{CYC}-16	t_{CYC}+ 16	ns	ASCY=0
ASX↑→Address hold	t_{MASHAH}		t_{CYC}-16	t_{CYC} + 16	ns	In multiplex mode, set as follows: • Set CSWR and CSRD to 2 or more. • ASCY must satisfy the following conditions because of setting ADCY > ASCY and protocol violation prevention. ADCY +1 ≤ ACS + CSRD ADCY +1 ≤ ACS + CSWR ASCY + 1 ≤ ACS + CSRD ASCY + 1 ≤ ACS + CSWR See Hardware Manual for details.

*1: Please use it with external load capacity 12pF or less for VCC=3.3V±0.3V (40MHz operation).
*2: If the bus is expanded by automatic wait insertion or RDY input, add time (t_{CYC} × the number of expanded cycles) to the rated value.

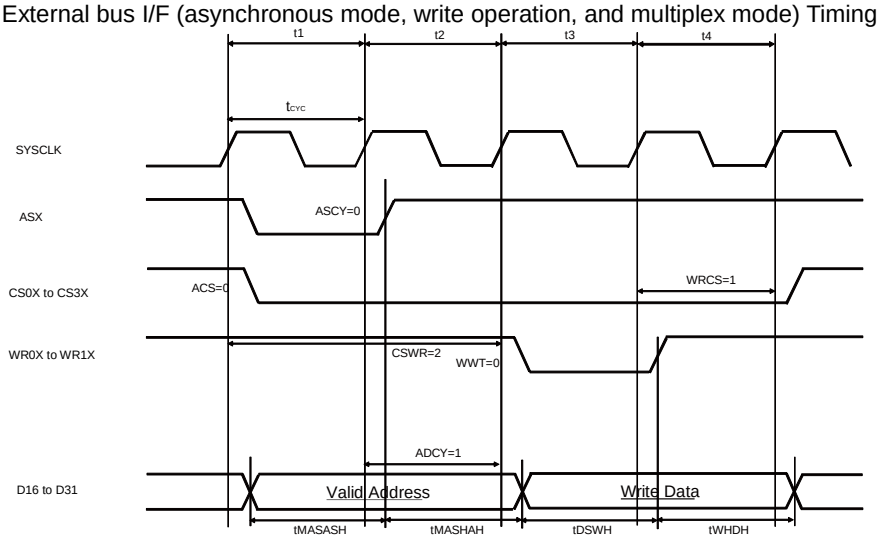
External bus I/F (asynchronous mode, read operation, and multiplex mode) Timing



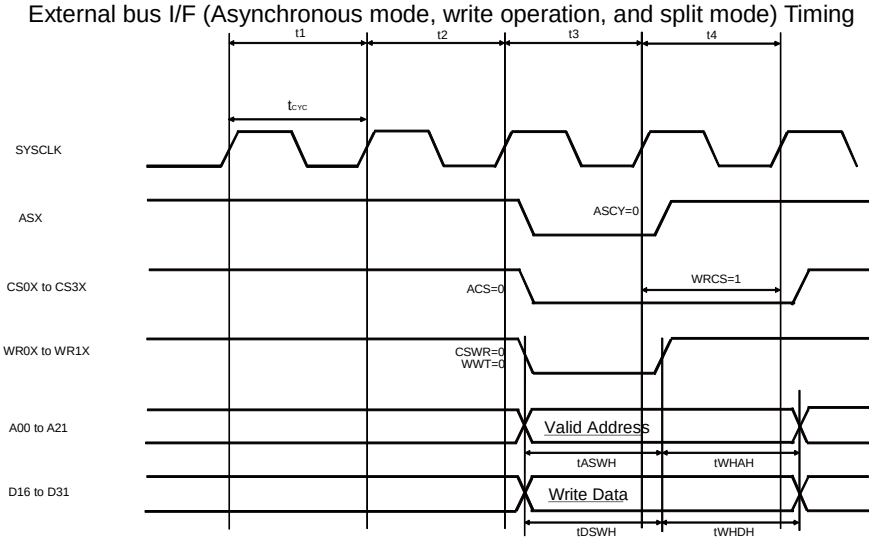
External bus I/F (asynchronous mode, read operation, and split mode) Timing



External bus I/F (asynchronous mode, write operation, and multiplex mode) Timing



External bus I/F (Asynchronous mode, write operation, and split mode) Timing

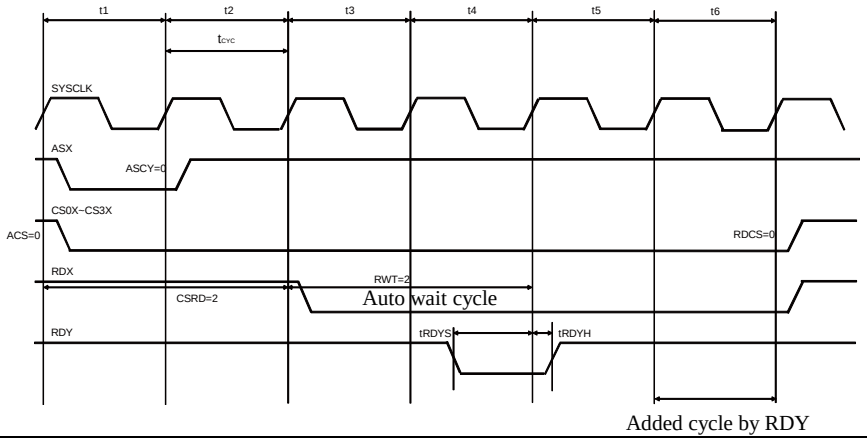


(12) External bus I/F (ready) Timing

(T_A: -40°C to +105°C, V_{CC}=AV_{CC}=5.0V ± 10%/V_{CC}= AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)
(external load capacitance 50pF)

Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
Cycle time	t_{CYC}	SYSCLK	50	-	ns	If using RDY, set SYSCLK to 20 MHz or less.
RDY setup time → SYSCLK↑	t_{RDYS}	SYSCLK, RDY	28	-	ns	
SYSCLK↑→ RDY hold time	t_{RDYH}	SYSCLK, RDY	0	-	ns	

External bus I/F (ready) Timing



5. A/D Converter

(1) 12-bit A/D Converter Electrical Characteristics

(T_A: -40°C to +125°C, V_{CC}=AV_{CC}=5.0V ± 10%/V_{CC}= AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	12	bit	
Total error	-	-	-	-	±12	LSB	
Linearity error	-	-	-	-	± 4.0	LSB	
Differential linearity error	-	-	-	-	± 1.9	LSB	
Zero transition voltage	V_{OT}	AN0 to AN47	AVRL-11.5LSB	-	AVRL+12.5LSB	V	1LSB= (V_{FST}-V_{OT})/4094
Full-scale transition voltage	V_{FST}	AN0 to AN47	AVRH-13.5LSB	-	AVRH+10.5LSB	V	
Sampling time	t_{SMP}	-	0.7	-	-	µs	*1
Compare time	t_{CMP}	-	0.7	-	-	µs	*1
A/D conversion time	t_{CNV}	-	1.4	-	-	µs	*1
Analog port input current	I_{AIN}	AN0 to AN47	-1.0	-	+1.0	µA	$V_{AVSS} \leq V_{AIN} \leq V_{AVCC}$
Analog input voltage	V_{AIN}	AN0 to AN47	AVRL	-	AVRH	V	
Reference voltage	AVRH	AVRH	3.0	-	5.5	V	
	AVRL	AVSS/AVRL	-	0.0	-	V	
Power supply current	I_A	AVCC*3	-	0.47	0.63	mA	Per unit T_A: +105°C
			-	0.47	0.7	mA	Per unit T_A: +125°C
	I_{AH}		-	-	2.5	µA	*2
	I_R	AVRH	-	1	1.96	mA	Per unit
	I_{RH}		-	-	1.6	µA	*2
Variation between channels	-	AN0 to AN47	-	-	4	LSB	

*1: Time for each channel.

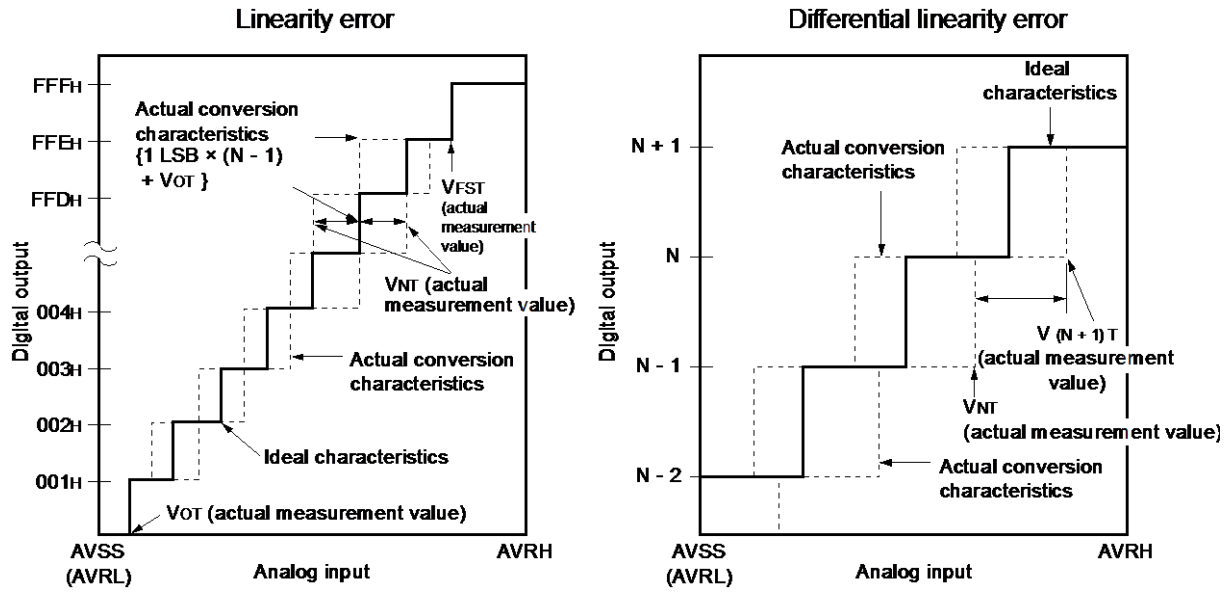
*2: Power supply current (V_{CC} = AV_{CC} = 5.0 V) is specified if A/D converter is not operating and CPU is stopped.

*3: The power supply current described only current value on A/D converter.
The total AVcc current value must be calculated the power supply current for A/D converter and D/A converter.

(Note) Please use the clock of 0.5MHz-20MHz for the output clock of A/D converter to guarantee accuracy.

(2) Definition of A/D Converter Terms

Resolution	: Analog variation that is recognized by an A/D converter.
Linearity error	: Deviation of the actual conversion characteristics from a straight line that connects the zero transition point ("0000 0000 0000"← →"0000 0000 0001") to the full-scale transition point ("1111 1111 1110"← →"1111 1111 1111").
Differential linearity error	: Deviation of the input voltage from the ideal value that is required to change the output code by LSB.



$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1LSB \times (N - 1) + V_{OT}\}}{1LSB} \text{ [LSB]}$$

$$\text{Differential linearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1 \text{ LSB} \quad \text{[LSB]}$$

$$1LSB = \frac{V_{FST} - V_{OT}}{4094} \text{ [V]}$$

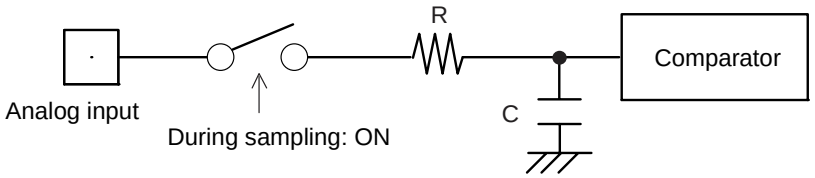
V_{OT} : Voltage at which the digital output changes from "000_H" to "001_H".
V_{FST} : Voltage at which the digital output changes from "FFE_H" to "FFF_H".

(3) Notes on Using A/D Converter

<About the output impedance of the analog input of external circuit>

· When the external impedance is too high, the sampling period for analog voltages may not be sufficient. In this case, it is recommended to connect the capacitor (approx. 0.1 µF) to the analog input pin.

• Analog input circuit model



	R	C	
12bit A/D	1.9kΩ (Max)	8.30pF (Max)	(4.5V ≤ AV_{CC} ≤ 5.5V)
	4.3kΩ (Max)	8.30pF (Max)	(3.0V ≤ AV_{CC} ≤ 3.6V)

Note: Listed values must be considered as reference values.

6. Flash memory

(1) Electrical Characteristics

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time	–	200	800	ms	8 Kbytes sector*1, excluding internal preprogramming time
	–	300	1100	ms	8 Kbytes sector*1, including internal preprogramming time
	–	400	2000	ms	64 Kbytes sector*1, excluding internal preprogramming time
	–	700	3700	ms	64 Kbytes sector*1, including internal preprogramming time
8-bit writing time	–	9	288	µs	Exclusive of overhead time at system level*1
16-bit writing time	–	12	384	µs	Exclusive of overhead time at system level*1
ECC writing time	–	9	288	µs	Exclusive of overhead time at system level*1
Erase cycle*2/ Data retain time	1,000 cycles/ 20 years, 10,000 cycles/ 10 years, 100,000 cycles/ 5 years	–	–	–	Average T_A=+85°C*3

*1: The guaranteed value for erasure up to 100,000 cycles.
*2: Number of erase cycles for each sector.
*3: This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at + 85°C).

(2) Notes

While the Flash memory is written or erased, shutdown of the external power (Vcc) is prohibited.
In the application system where Vcc might be shut down while writing or erasing, be sure to turn the power off by using an external voltage detection function.

To put it concretely, after the external power supply voltage falls below the detection voltage (V_{DL}*), hold Vcc at 2.7V or more within the duration calculated by the following expression:

Td*[µs] + (period of PCLK [µs] × 257) + 50 [µs]

*: See “4.AC Characteristics (8) Low-voltage detection (External low-voltage detection) ”

7. D/A converter

(T_A:-40°C to +125°C, V_{CC}=AV_{CC}=5.0V±10%/V_{CC}= AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

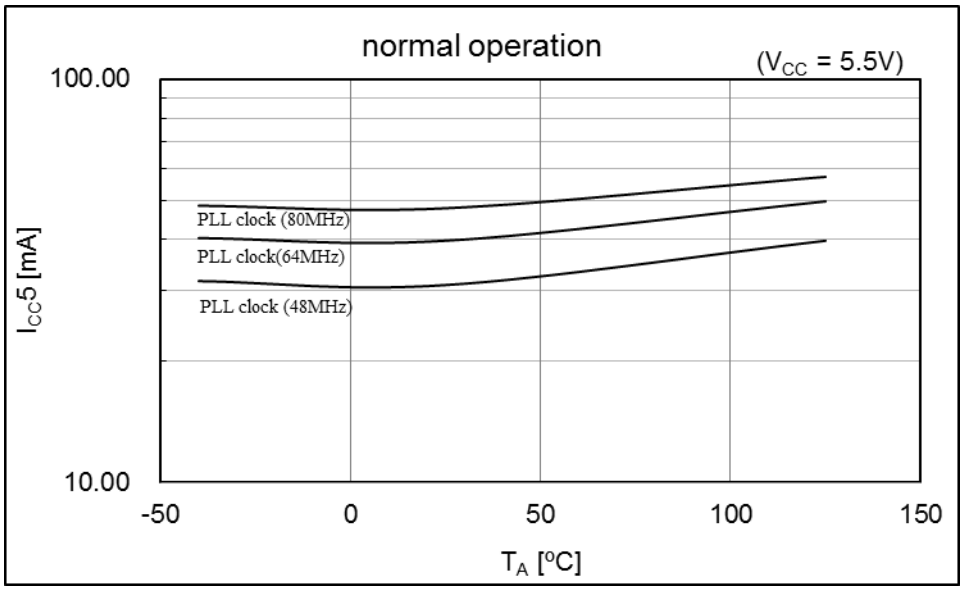
Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Resolution	-	-	–	–	–	8	bit	
Differential linearity error	-	-	–	–	–	± 3.0	LSB	
Conversion time	-	-	–	0.47	0.58	0.69	µs	C_L=20
			–	2.37	2.90	3.43	µs	C_L=100
Output impedance	Ro	DA0, DA1	–	3.1	3.8	4.5	kΩ	
Power supply current *1	IA	AVCC	–	–	475	580	µA	Each channel
	IAH	AVCC	–	–	–	7.5	µA	When powerdown Each channel

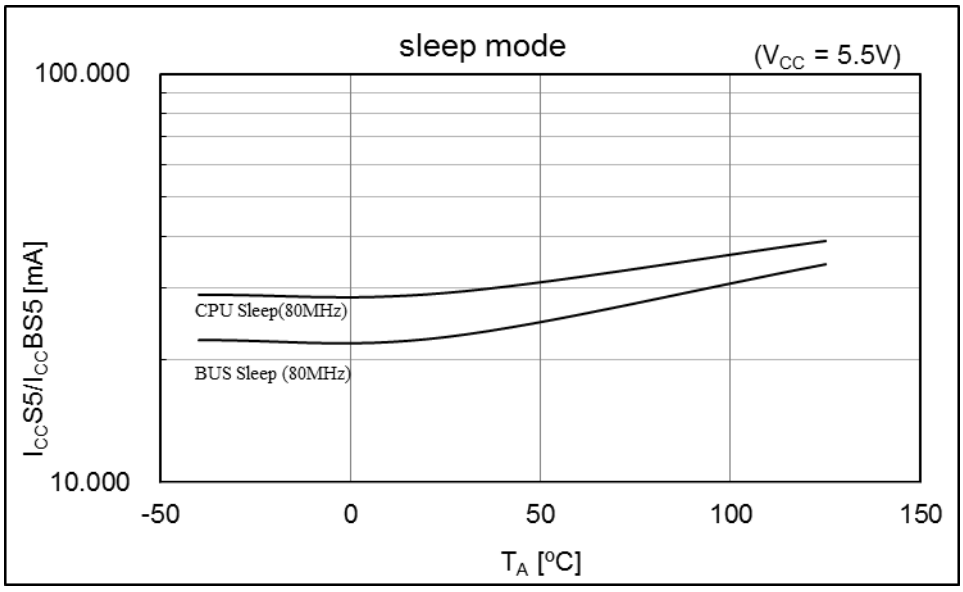
*1: The power supply current described only current value on D/A converter.
The total AVcc current value must be calculated the power supply current for D/A converter and A/D converter.

■ EXAMPLE CHARACTERISTICS

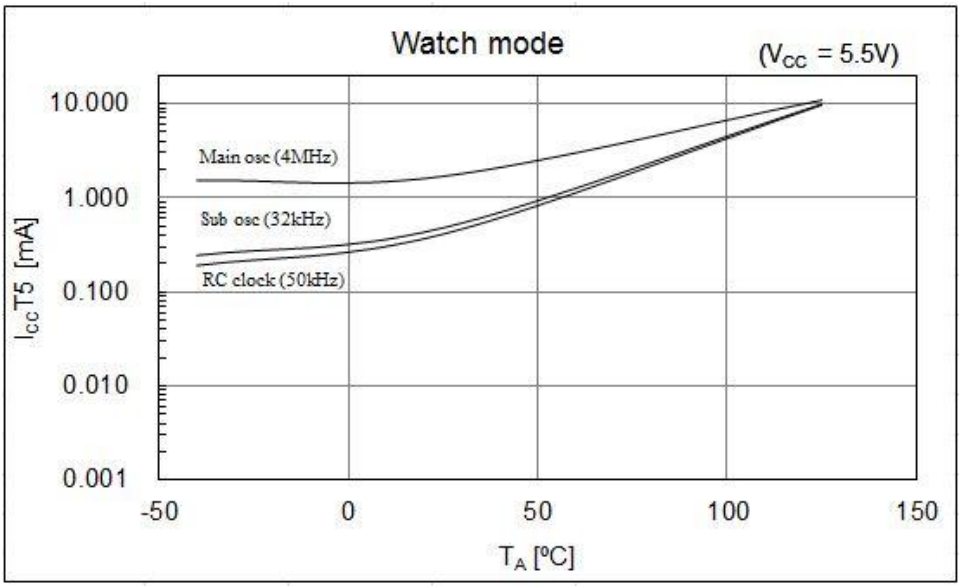
This characteristic is an actual value of the arbitrary sample. It is not the guaranteed value.

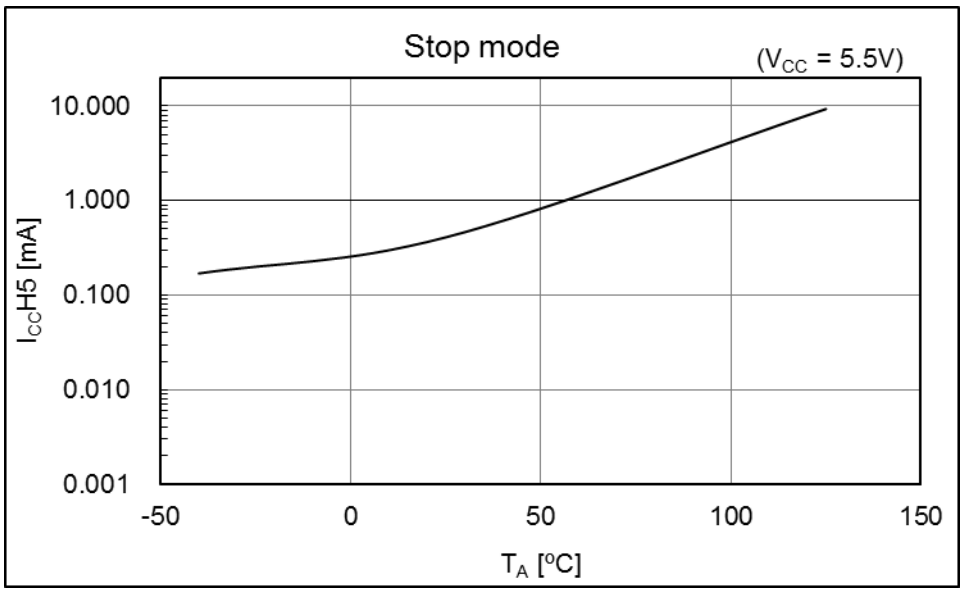
・MB91F526



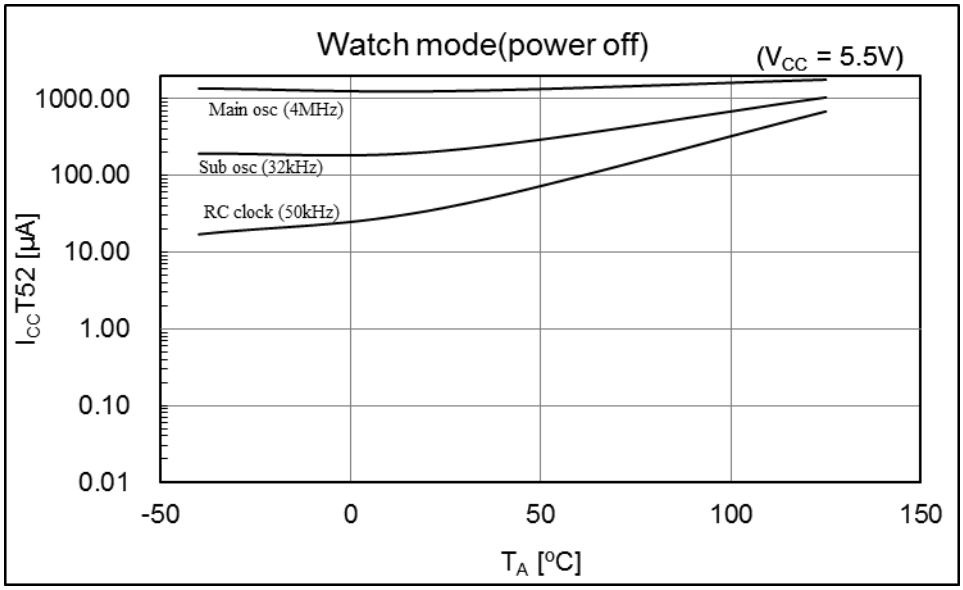


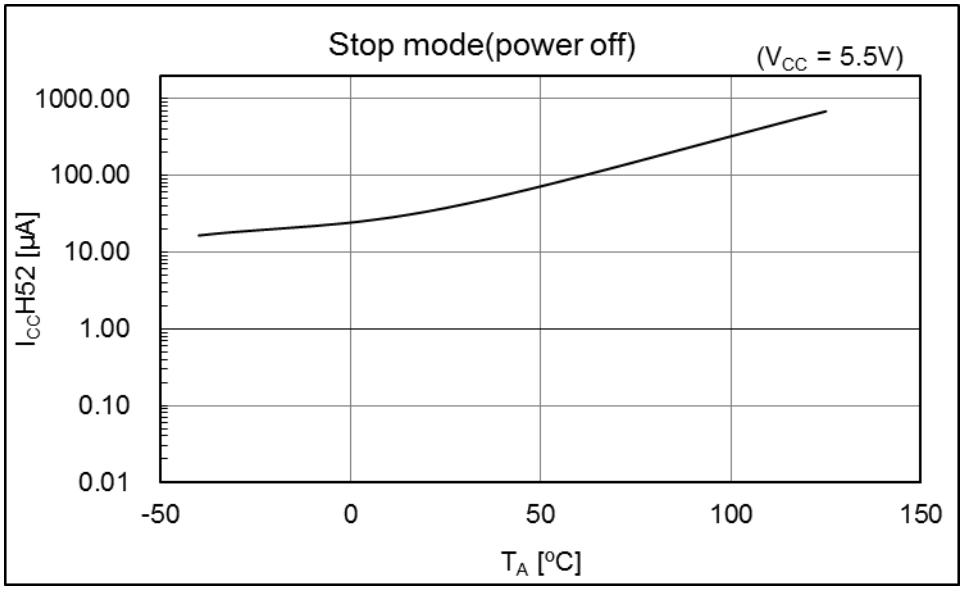
・MB91F526


Watch mode
(V_{CC} = 5.5V)
10.000
1.000
0.100
0.010
0.001
I_{CC}T5 [mA]
Main osc (4MHz)
Sub osc (32kHz)
RC clock (50kHz)
-50
0
50
100
150
T_A [°C]


Stop mode
(V_{CC} = 5.5V)
10.000
1.000
0.100
0.010
0.001
I_{CC}H5 [mA]
-50
0
50
100
150
T_A [°C]

・MB91F526


Watch mode(power off)
(V_{CC} = 5.5V)
1000.00
100.00
10.00
1.00
0.10
0.01
Main osc (4MHz)
Sub osc (32kHz)
RC clock (50kHz)
I_{CC}T52 [µA]
-50
0
50
100
150
T_A [°C]


Stop mode(power off)
(V_{CC} = 5.5V)
1000.00
100.00
10.00
1.00
0.10
0.01
I_{CC}H52 [µA]
-50
0
50
100
150
T_A [°C]

■ ORDERING INFORMATION MB91F52xxxB*1

Part number	Sub clock	CSV Initial value	LVD Initial value	Package*2
MB91F526LWBPMC	Yes	ON	ON	LQFP・176 pin, Plastic (FPT-176P-M07)
MB91F526LYBPMC			OFF	
MB91F526LJBPMC		OFF	ON	
MB91F526LLBPMC			OFF	
MB91F525LWBPMC		ON	ON	
MB91F525LYBPMC			OFF	
MB91F525LJBPMC		OFF	ON	
MB91F525LLBPMC			OFF	
MB91F524LWBPMC		ON	ON	
MB91F524LYBPMC			OFF	
MB91F524LJBPMC		OFF	ON	
MB91F524LLBPMC			OFF	
MB91F523LWBPMC		ON	ON	
MB91F523LYBPMC			OFF	
MB91F523LJBPMC		OFF	ON	
MB91F523LLBPMC			OFF	
MB91F522LWBPMC		ON	ON	
MB91F522LYBPMC			OFF	
MB91F522LJBPMC		OFF	ON	
MB91F522LLBPMC			OFF	
MB91F526LSBPMC	None	ON	ON	
MB91F526LUBPMC			OFF	
MB91F526LHBPMC		OFF	ON	
MB91F526LKBPMC			OFF	
MB91F525LSBPMC		ON	ON	
MB91F525LUBPMC			OFF	
MB91F525LHBPMC		OFF	ON	
MB91F525LKBPMC			OFF	
MB91F524LSBPMC		ON	ON	
MB91F524LUBPMC			OFF	
MB91F524LHBPMC		OFF	ON	
MB91F524LKBPMC			OFF	
MB91F523LSBPMC		ON	ON	
MB91F523LUBPMC			OFF	
MB91F523LHBPMC		OFF	ON	
MB91F523LKBPMC			OFF	
MB91F522LSBPMC		ON	ON	
MB91F522LUBPMC			OFF	
MB91F522LHBPMC		OFF	ON	
MB91F522LKBPMC			OFF	

Part number	Sub clock	CSV Initial value	LVD Initial value	Package*2
MB91F526KWBPMC	Yes	ON	ON	LQFP・144 pin, (Lead pitch 0.5mm) Plastic (FPT-144P-M08)
MB91F526KYBPMC			OFF	
MB91F526KJBPMC		OFF	ON	
MB91F526KLBPMC			OFF	
MB91F525KWBPMC		ON	ON	
MB91F525KYBPMC			OFF	
MB91F525KJBPMC		OFF	ON	
MB91F525KLBPMC			OFF	
MB91F524KWBPMC		ON	ON	
MB91F524KYBPMC			OFF	
MB91F524KJBPMC		OFF	ON	
MB91F524KLBPMC			OFF	
MB91F523KWBPMC		ON	ON	
MB91F523KYBPMC			OFF	
MB91F523KJBPMC		OFF	ON	
MB91F523KLBPMC			OFF	
MB91F522KWBPMC		ON	ON	
MB91F522KYBPMC			OFF	
MB91F522KJBPMC		OFF	ON	
MB91F522KLBPMC			OFF	
MB91F526KSBPMC	None	ON	ON	
MB91F526KUBPMC			OFF	
MB91F526KHBPMC		OFF	ON	
MB91F526KKBPMC			OFF	
MB91F525KSBPMC		ON	ON	
MB91F525KUBPMC			OFF	
MB91F525KHBPMC		OFF	ON	
MB91F525KKBPMC			OFF	
MB91F524KSBPMC		ON	ON	
MB91F524KUBPMC			OFF	
MB91F524KHBPMC		OFF	ON	
MB91F524KKBPMC			OFF	
MB91F523KSBPMC		ON	ON	
MB91F523KUBPMC			OFF	
MB91F523KHBPMC		OFF	ON	
MB91F523KKBPMC			OFF	
MB91F522KSBPMC		ON	ON	
MB91F522KUBPMC			OFF	
MB91F522KHBPMC		OFF	ON	
MB91F522KKBPMC			OFF	

Part number	Sub clock	CSV Initial value	LVD Initial value	Package*2
MB91F526KWBPMC1	Yes	ON	ON	LQFP・144 pin, (Lead pitch 0.4mm) Plastic (FPT-144P-M12)
MB91F526KYBPMC1			OFF	
MB91F526KJBPMC1		OFF	ON	
MB91F526KLBPMC1			OFF	
MB91F525KWBPMC1		ON	ON	
MB91F525KYBPMC1			OFF	
MB91F525KJBPMC1		OFF	ON	
MB91F525KLBPMC1			OFF	
MB91F524KWBPMC1		ON	ON	
MB91F524KYBPMC1			OFF	
MB91F524KJBPMC1		OFF	ON	
MB91F524KLBPMC1			OFF	
MB91F523KWBPMC1		ON	ON	
MB91F523KYBPMC1			OFF	
MB91F523KJBPMC1		OFF	ON	
MB91F523KLBPMC1			OFF	
MB91F522KWBPMC1		ON	ON	
MB91F522KYBPMC1			OFF	
MB91F522KJBPMC1		OFF	ON	
MB91F522KLBPMC1			OFF	
MB91F526KSBPMC1	None	ON	ON	
MB91F526KUBPMC1			OFF	
MB91F526KHBPMC1		OFF	ON	
MB91F526KKBPMC1			OFF	
MB91F525KSBPMC1		ON	ON	
MB91F525KUBPMC1			OFF	
MB91F525KHBPMC1		OFF	ON	
MB91F525KKBPMC1			OFF	
MB91F524KSBPMC1		ON	ON	
MB91F524KUBPMC1			OFF	
MB91F524KHBPMC1		OFF	ON	
MB91F524KKBPMC1			OFF	
MB91F523KSBPMC1		ON	ON	
MB91F523KUBPMC1			OFF	
MB91F523KHBPMC1		OFF	ON	
MB91F523KKBPMC1			OFF	
MB91F522KSBPMC1		ON	ON	
MB91F522KUBPMC1			OFF	
MB91F522KHBPMC1		OFF	ON	
MB91F522KKBPMC1			OFF	

Part number	Sub clock	CSV Initial value	LVD Initial value	Package*2
MB91F526JWBPMC	Yes	ON	ON	LQFP・120 pin, Plastic (FPT-120P-M21)
MB91F526JYBPMC			OFF	
MB91F526JJBPMC		OFF	ON	
MB91F526JLBPMC			OFF	
MB91F525JWBPMC		ON	ON	
MB91F525JYBPMC			OFF	
MB91F525JJBPMC		OFF	ON	
MB91F525JLBPMC			OFF	
MB91F524JWBPMC		ON	ON	
MB91F524JYBPMC			OFF	
MB91F524JJBPMC		OFF	ON	
MB91F524JLBPMC			OFF	
MB91F523JWBPMC		ON	ON	
MB91F523JYBPMC			OFF	
MB91F523JJBPMC		OFF	ON	
MB91F523JLBPMC			OFF	
MB91F522JWBPMC		ON	ON	
MB91F522JYBPMC			OFF	
MB91F522JJBPMC		OFF	ON	
MB91F522JLBPMC			OFF	
MB91F526JSBPMC	None	ON	ON	
MB91F526JUBPMC			OFF	
MB91F526JHBPMC		OFF	ON	
MB91F526JKBPMC			OFF	
MB91F525JSBPMC		ON	ON	
MB91F525JUBPMC			OFF	
MB91F525JHBPMC		OFF	ON	
MB91F525JKBPMC			OFF	
MB91F524JSBPMC		ON	ON	
MB91F524JUBPMC			OFF	
MB91F524JHBPMC		OFF	ON	
MB91F524JKBPMC			OFF	
MB91F523JSBPMC		ON	ON	
MB91F523JUBPMC			OFF	
MB91F523JHBPMC		OFF	ON	
MB91F523JKBPMC			OFF	
MB91F522JSBPMC		ON	ON	
MB91F522JUBPMC			OFF	
MB91F522JHBPMC		OFF	ON	
MB91F522JKBPMC			OFF	

Part number	Sub clock	CSV Initial value	LVD Initial value	Package*2
MB91F526FWBPMC	Yes	ON	ON	LQFP・100 pin, Plastic (FPT-100P-M20)
MB91F526FYBPMC			OFF	
MB91F526FJBPMC		OFF	ON	
MB91F526FLBPMC			OFF	
MB91F525FWBPMC		ON	ON	
MB91F525FYBPMC			OFF	
MB91F525FJBPMC		OFF	ON	
MB91F525FLBPMC			OFF	
MB91F524FWBPMC		ON	ON	
MB91F524FYBPMC			OFF	
MB91F524FJBPMC		OFF	ON	
MB91F524FLBPMC			OFF	
MB91F523FWBPMC		ON	ON	
MB91F523FYBPMC			OFF	
MB91F523FJBPMC		OFF	ON	
MB91F523FLBPMC			OFF	
MB91F522FWBPMC		ON	ON	
MB91F522FYBPMC			OFF	
MB91F522FJBPMC		OFF	ON	
MB91F522FLBPMC			OFF	
MB91F526FSBPMC	None	ON	ON	
MB91F526FUBPMC			OFF	
MB91F526FHBPMC		OFF	ON	
MB91F526FKBPMC			OFF	
MB91F525FSBPMC		ON	ON	
MB91F525FUBPMC			OFF	
MB91F525FHBPMC		OFF	ON	
MB91F525FKBPMC			OFF	
MB91F524FSBPMC		ON	ON	
MB91F524FUBPMC			OFF	
MB91F524FHBPMC		OFF	ON	
MB91F524FKBPMC			OFF	
MB91F523FSBPMC		ON	ON	
MB91F523FUBPMC			OFF	
MB91F523FHBPMC		OFF	ON	
MB91F523FKBPMC			OFF	
MB91F522FSBPMC		ON	ON	
MB91F522FUBPMC			OFF	
MB91F522FHBPMC		OFF	ON	
MB91F522FKBPMC			OFF	

Part number	Sub clock	CSV Initial value	LVD Initial value	Package*2
MB91F526DWBPMC	Yes	ON	ON	LQFP・80 pin, Plastic (FPT-80P-M21)
MB91F526DYBPMC			OFF	
MB91F526DJBPMC		OFF	ON	
MB91F526DLBPMC			OFF	
MB91F525DWBPMC		ON	ON	
MB91F525DYBPMC			OFF	
MB91F525DJBPMC		OFF	ON	
MB91F525DLBPMC			OFF	
MB91F524DWBPMC		ON	ON	
MB91F524DYBPMC			OFF	
MB91F524DJBPMC		OFF	ON	
MB91F524DLBPMC			OFF	
MB91F523DWBPMC		ON	ON	
MB91F523DYBPMC			OFF	
MB91F523DJBPMC		OFF	ON	
MB91F523DLBPMC			OFF	
MB91F522DWBPMC		ON	ON	
MB91F522DYBPMC			OFF	
MB91F522DJBPMC		OFF	ON	
MB91F522DLBPMC			OFF	
MB91F526DSBPMC	None	ON	ON	
MB91F526DUBPMC			OFF	
MB91F526DHBPMC		OFF	ON	
MB91F526DKBPMC			OFF	
MB91F525DSBPMC		ON	ON	
MB91F525DUBPMC			OFF	
MB91F525DHBPMC		OFF	ON	
MB91F525DKBPMC			OFF	
MB91F524DSBPMC		ON	ON	
MB91F524DUBPMC			OFF	
MB91F524DHBPMC		OFF	ON	
MB91F524DKBPMC			OFF	
MB91F523DSBPMC		ON	ON	
MB91F523DUBPMC			OFF	
MB91F523DHBPMC		OFF	ON	
MB91F523DKBPMC			OFF	
MB91F522DSBPMC		ON	ON	
MB91F522DUBPMC			OFF	
MB91F522DHBPMC		OFF	ON	
MB91F522DKBPMC			OFF	

Part number	Sub clock	CSV Initial value	LVD Initial value	Package*2
MB91F526BWBPMC1	Yes	ON	ON	LQFP・64 pin, Plastic (FPT-64P-M24)
MB91F526BYBPMC1			OFF	
MB91F526BJBPMC1		OFF	ON	
MB91F526BLBPMC1			OFF	
MB91F525BWBPMC1		ON	ON	
MB91F525BYBPMC1			OFF	
MB91F525BJBPMC1		OFF	ON	
MB91F525BLBPMC1			OFF	
MB91F524BWBPMC1		ON	ON	
MB91F524BYBPMC1			OFF	
MB91F524BJBPMC1		OFF	ON	
MB91F524BLBPMC1			OFF	
MB91F523BWBPMC1		ON	ON	
MB91F523BYBPMC1			OFF	
MB91F523BJBPMC1		OFF	ON	
MB91F523BLBPMC1			OFF	
MB91F522BWBPMC1		ON	ON	
MB91F522BYBPMC1			OFF	
MB91F522BJBPMC1		OFF	ON	
MB91F522BLBPMC1			OFF	
MB91F526BSBPMC1	None	ON	ON	
MB91F526BUBPMC1			OFF	
MB91F526BHBPMC1		OFF	ON	
MB91F526BKBPMC1			OFF	
MB91F525BSBPMC1		ON	ON	
MB91F525BUBPMC1			OFF	
MB91F525BHBPMC1		OFF	ON	
MB91F525BKBPMC1			OFF	
MB91F524BSBPMC1		ON	ON	
MB91F524BUBPMC1			OFF	
MB91F524BHBPMC1		OFF	ON	
MB91F524BKBPMC1			OFF	
MB91F523BSBPMC1		ON	ON	
MB91F523BUBPMC1			OFF	
MB91F523BHBPMC1		OFF	ON	
MB91F523BKBPMC1			OFF	
MB91F522BSBPMC1		ON	ON	
MB91F522BUBPMC1			OFF	
MB91F522BHBPMC1		OFF	ON	
MB91F522BKBPMC1			OFF	

*1: It is only supported for customers who have already adopted it now. We do not recommend adopting new products.

*2: For details of the package, see "■ PACKAGE DIMENSIONS ".

■ ORDERING INFORMATION MB91F52xxxC

Part number	Sub clock	CSV Initial value	LVD Initial value	Package*
MB91F526LWCPMC	Yes	ON	ON	LQFP・176 pin, Plastic (FPT-176P-M07)
MB91F526LYCPMC			OFF	
MB91F526LJCPMC		OFF	ON	
MB91F526LLCPMC			OFF	
MB91F525LWCPMC		ON	ON	
MB91F525LYCPMC			OFF	
MB91F525LJCPMC		OFF	ON	
MB91F525LLCPMC			OFF	
MB91F524LWCPMC		ON	ON	
MB91F524LYCPMC			OFF	
MB91F524LJCPMC		OFF	ON	
MB91F524LLCPMC			OFF	
MB91F523LWCPMC		ON	ON	
MB91F523LYCPMC			OFF	
MB91F523LJCPMC		OFF	ON	
MB91F523LLCPMC			OFF	
MB91F522LWCPMC		ON	ON	
MB91F522LYCPMC			OFF	
MB91F522LJCPMC		OFF	ON	
MB91F522LLCPMC			OFF	
MB91F526LSCPMC	None	ON	ON	
MB91F526LUCPMC			OFF	
MB91F526LHCPMC		OFF	ON	
MB91F526LKCPMC			OFF	
MB91F525LSCPMC		ON	ON	
MB91F525LUCPMC			OFF	
MB91F525LHCPMC		OFF	ON	
MB91F525LKCPMC			OFF	
MB91F524LSCPMC		ON	ON	
MB91F524LUCPMC			OFF	
MB91F524LHCPMC		OFF	ON	
MB91F524LKCPMC			OFF	
MB91F523LSCPMC		ON	ON	
MB91F523LUCPMC			OFF	
MB91F523LHCPMC		OFF	ON	
MB91F523LKCPMC			OFF	
MB91F522LSCPMC		ON	ON	
MB91F522LUCPMC			OFF	
MB91F522LHCPMC		OFF	ON	
MB91F522LKCPMC			OFF	

Part number	Sub clock	CSV Initial value	LVD Initial value	Package*
MB91F526KWCPMC	Yes	ON	ON	LQFP・144 pin, (Lead pitch 0.5mm) Plastic (FPT-144P-M08)
MB91F526KYCPMC			OFF	
MB91F526KJCPMC		OFF	ON	
MB91F526KLCPMC			OFF	
MB91F525KWCPMC		ON	ON	
MB91F525KYCPMC			OFF	
MB91F525KJCPMC		OFF	ON	
MB91F525KLCPMC			OFF	
MB91F524KWCPMC		ON	ON	
MB91F524KYCPMC			OFF	
MB91F524KJCPMC		OFF	ON	
MB91F524KLCPMC			OFF	
MB91F523KWCPMC		ON	ON	
MB91F523KYCPMC			OFF	
MB91F523KJCPMC		OFF	ON	
MB91F523KLCPMC			OFF	
MB91F522KWCPMC		ON	ON	
MB91F522KYCPMC			OFF	
MB91F522KJCPMC		OFF	ON	
MB91F522KLCPMC			OFF	
MB91F526KSCPMC	None	ON	ON	
MB91F526KUCPMC			OFF	
MB91F526KHCPMC		OFF	ON	
MB91F526KKCPMC			OFF	
MB91F525KSCPMC		ON	ON	
MB91F525KUCPMC			OFF	
MB91F525KHCPMC		OFF	ON	
MB91F525KKCPMC			OFF	
MB91F524KSCPMC		ON	ON	
MB91F524KUCPMC			OFF	
MB91F524KHCPMC		OFF	ON	
MB91F524KKCPMC			OFF	
MB91F523KSCPMC		ON	ON	
MB91F523KUCPMC			OFF	
MB91F523KHCPMC		OFF	ON	
MB91F523KKCPMC			OFF	
MB91F522KSCPMC		ON	ON	
MB91F522KUCPMC			OFF	
MB91F522KHCPMC		OFF	ON	
MB91F522KKCPMC			OFF	

Part number	Sub clock	CSV Initial value	LVD Initial value	Package*
MB91F526KWCPMC1	Yes	ON	ON	LQFP・144 pin, (Lead pitch 0.4mm) Plastic (FPT-144P-M12)
MB91F526KYCPMC1			OFF	
MB91F526KJCPMC1		OFF	ON	
MB91F526KLCPMC1			OFF	
MB91F525KWCPMC1		ON	ON	
MB91F525KYCPMC1			OFF	
MB91F525KJCPMC1		OFF	ON	
MB91F525KLCPMC1			OFF	
MB91F524KWCPMC1		ON	ON	
MB91F524KYCPMC1			OFF	
MB91F524KJCPMC1		OFF	ON	
MB91F524KLCPMC1			OFF	
MB91F523KWCPMC1		ON	ON	
MB91F523KYCPMC1			OFF	
MB91F523KJCPMC1		OFF	ON	
MB91F523KLCPMC1			OFF	
MB91F522KWCPMC1		ON	ON	
MB91F522KYCPMC1			OFF	
MB91F522KJCPMC1		OFF	ON	
MB91F522KLCPMC1			OFF	
MB91F526KSCPMC1	None	ON	ON	
MB91F526KUCPMC1			OFF	
MB91F526KHCPMC1		OFF	ON	
MB91F526KKCPMC1			OFF	
MB91F525KSCPMC1		ON	ON	
MB91F525KUCPMC1			OFF	
MB91F525KHCPMC1		OFF	ON	
MB91F525KKCPMC1			OFF	
MB91F524KSCPMC1		ON	ON	
MB91F524KUCPMC1			OFF	
MB91F524KHCPMC1		OFF	ON	
MB91F524KKCPMC1			OFF	
MB91F523KSCPMC1		ON	ON	
MB91F523KUCPMC1			OFF	
MB91F523KHCPMC1		OFF	ON	
MB91F523KKCPMC1			OFF	
MB91F522KSCPMC1		ON	ON	
MB91F522KUCPMC1			OFF	
MB91F522KHCPMC1		OFF	ON	
MB91F522KKCPMC1			OFF	

Part number	Sub clock	CSV Initial value	LVD Initial value	Package*
MB91F526JWCPMC	Yes	ON	ON	LQFP・120 pin, Plastic (FPT-120P-M21)
MB91F526JYCPMC			OFF	
MB91F526JJCPMC		OFF	ON	
MB91F526JLCPMC			OFF	
MB91F525JWCPMC		ON	ON	
MB91F525JYCPMC			OFF	
MB91F525JJCPMC		OFF	ON	
MB91F525JLCPMC			OFF	
MB91F524JWCPMC		ON	ON	
MB91F524JYCPMC			OFF	
MB91F524JJCPMC		OFF	ON	
MB91F524JLCPMC			OFF	
MB91F523JWCPMC		ON	ON	
MB91F523JYCPMC			OFF	
MB91F523JJCPMC		OFF	ON	
MB91F523JLCPMC			OFF	
MB91F522JWCPMC		ON	ON	
MB91F522JYCPMC			OFF	
MB91F522JJCPMC		OFF	ON	
MB91F522JLCPMC			OFF	
MB91F526JSCPMC	None	ON	ON	
MB91F526JUCPMC			OFF	
MB91F526JHCPMC		OFF	ON	
MB91F526JKCPMC			OFF	
MB91F525JSCPMC		ON	ON	
MB91F525JUCPMC			OFF	
MB91F525JHCPMC		OFF	ON	
MB91F525JKCPMC			OFF	
MB91F524JSCPMC		ON	ON	
MB91F524JUCPMC			OFF	
MB91F524JHCPMC		OFF	ON	
MB91F524JKCPMC			OFF	
MB91F523JSCPMC		ON	ON	
MB91F523JUCPMC			OFF	
MB91F523JHCPMC		OFF	ON	
MB91F523JKCPMC			OFF	
MB91F522JSCPMC		ON	ON	
MB91F522JUCPMC			OFF	
MB91F522JHCPMC		OFF	ON	
MB91F522JKCPMC			OFF	

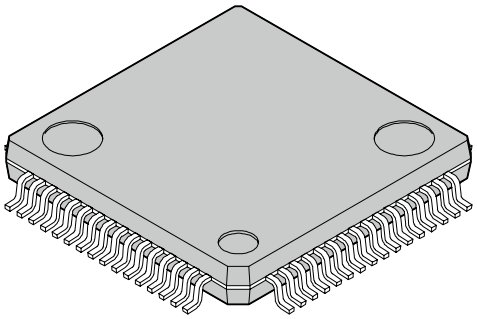
Part number	Sub clock	CSV Initial value	LVD Initial value	Package*
MB91F526FWCPMC	Yes	ON	ON	LQFP・100 pin, Plastic (FPT-100P-M20)
MB91F526FYCPMC			OFF	
MB91F526FJCPMC		OFF	ON	
MB91F526FLCPMC			OFF	
MB91F525FWCPMC		ON	ON	
MB91F525FYCPMC			OFF	
MB91F525FJCPMC		OFF	ON	
MB91F525FLCPMC			OFF	
MB91F524FWCPMC		ON	ON	
MB91F524FYCPMC			OFF	
MB91F524FJCPMC		OFF	ON	
MB91F524FLCPMC			OFF	
MB91F523FWCPMC		ON	ON	
MB91F523FYCPMC			OFF	
MB91F523FJCPMC		OFF	ON	
MB91F523FLCPMC			OFF	
MB91F522FWCPMC		ON	ON	
MB91F522FYCPMC			OFF	
MB91F522FJCPMC		OFF	ON	
MB91F522FLCPMC			OFF	
MB91F526FSCPMC	None	ON	ON	
MB91F526FUCPMC			OFF	
MB91F526FHCPMC		OFF	ON	
MB91F526FKCPMC			OFF	
MB91F525FSCPMC		ON	ON	
MB91F525FUCPMC			OFF	
MB91F525FHCPMC		OFF	ON	
MB91F525FKCPMC			OFF	
MB91F524FSCPMC		ON	ON	
MB91F524FUCPMC			OFF	
MB91F524FHCPMC		OFF	ON	
MB91F524FKCPMC			OFF	
MB91F523FSCPMC		ON	ON	
MB91F523FUCPMC			OFF	
MB91F523FHCPMC		OFF	ON	
MB91F523FKCPMC			OFF	
MB91F522FSCPMC		ON	ON	
MB91F522FUCPMC			OFF	
MB91F522FHCPMC		OFF	ON	
MB91F522FKCPMC			OFF	

Part number	Sub clock	CSV Initial value	LVD Initial value	Package*
MB91F526DWCPMC	Yes	ON	ON	LQFP・80 pin, Plastic (FPT-80P-M21)
MB91F526DYCPMC			OFF	
MB91F526DJCPMC		OFF	ON	
MB91F526DLCPMC			OFF	
MB91F525DWCPMC		ON	ON	
MB91F525DYCPMC			OFF	
MB91F525DJCPMC		OFF	ON	
MB91F525DLCPMC			OFF	
MB91F524DWCPMC		ON	ON	
MB91F524DYCPMC			OFF	
MB91F524DJCPMC		OFF	ON	
MB91F524DLCPMC			OFF	
MB91F523DWCPMC		ON	ON	
MB91F523DYCPMC			OFF	
MB91F523DJCPMC		OFF	ON	
MB91F523DLCPMC			OFF	
MB91F522DWCPMC		ON	ON	
MB91F522DYCPMC			OFF	
MB91F522DJCPMC		OFF	ON	
MB91F522DLCPMC			OFF	
MB91F526DSCPMC	None	ON	ON	
MB91F526DUCPMC			OFF	
MB91F526DHCPMC		OFF	ON	
MB91F526DKCPMC			OFF	
MB91F525DSCPMC		ON	ON	
MB91F525DUCPMC			OFF	
MB91F525DHCPMC		OFF	ON	
MB91F525DKCPMC			OFF	
MB91F524DSCPMC		ON	ON	
MB91F524DUCPMC			OFF	
MB91F524DHCPMC		OFF	ON	
MB91F524DKCPMC			OFF	
MB91F523DSCPMC		ON	ON	
MB91F523DUCPMC			OFF	
MB91F523DHCPMC		OFF	ON	
MB91F523DKCPMC			OFF	
MB91F522DSCPMC		ON	ON	
MB91F522DUCPMC			OFF	
MB91F522DHCPMC		OFF	ON	
MB91F522DKCPMC			OFF	

Part number	Sub clock	CSV Initial value	LVD Initial value	Package*
MB91F526BWCPMC1	Yes	ON	ON	LQFP・64 pin, Plastic (FPT-64P-M24)
MB91F526BYCPMC1			OFF	
MB91F526BJCPMC1		OFF	ON	
MB91F526BLCPMC1			OFF	
MB91F525BWCPMC1		ON	ON	
MB91F525BYCPMC1			OFF	
MB91F525BJCPMC1		OFF	ON	
MB91F525BLCPMC1			OFF	
MB91F524BWCPMC1		ON	ON	
MB91F524BYCPMC1			OFF	
MB91F524BJCPMC1		OFF	ON	
MB91F524BLCPMC1			OFF	
MB91F523BWCPMC1		ON	ON	
MB91F523BYCPMC1			OFF	
MB91F523BJCPMC1		OFF	ON	
MB91F523BLCPMC1			OFF	
MB91F522BWCPMC1		ON	ON	
MB91F522BYCPMC1			OFF	
MB91F522BJCPMC1		OFF	ON	
MB91F522BLCPMC1			OFF	
MB91F526BSCPMC1	None	ON	ON	
MB91F526BUCPMC1			OFF	
MB91F526BHCPMC1		OFF	ON	
MB91F526BKCPMC1			OFF	
MB91F525BSCPMC1		ON	ON	
MB91F525BUCPMC1			OFF	
MB91F525BHCPMC1		OFF	ON	
MB91F525BKCPMC1			OFF	
MB91F524BSCPMC1		ON	ON	
MB91F524BUCPMC1			OFF	
MB91F524BHCPMC1		OFF	ON	
MB91F524BKCPMC1			OFF	
MB91F523BSCPMC1		ON	ON	
MB91F523BUCPMC1			OFF	
MB91F523BHCPMC1		OFF	ON	
MB91F523BKCPMC1			OFF	
MB91F522BSCPMC1		ON	ON	
MB91F522BUCPMC1			OFF	
MB91F522BHCPMC1		OFF	ON	
MB91F522BKCPMC1			OFF	

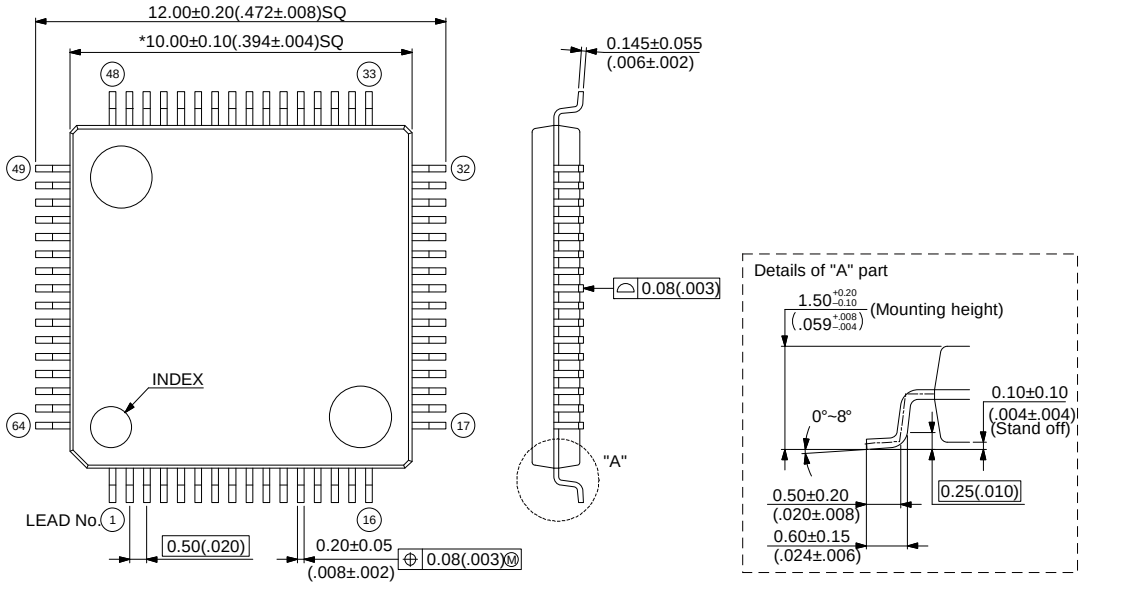
*: For details of the package, see "■ PACKAGE DIMENSIONS ".

■ PACKAGE DIMENSIONS

64-pin plastic LQFP		
	Lead pitch	0.50 mm
	Package width × package length	10.0 × 10.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.32 g
(FPT-64P-M24)	Code (Reference)	P-LFQFP64-10×10-0.50

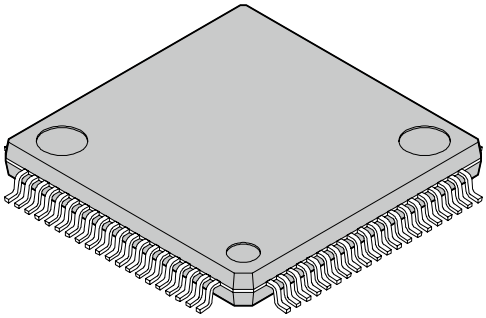
64-pin plastic LQFP
(FPT-64P-M24)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



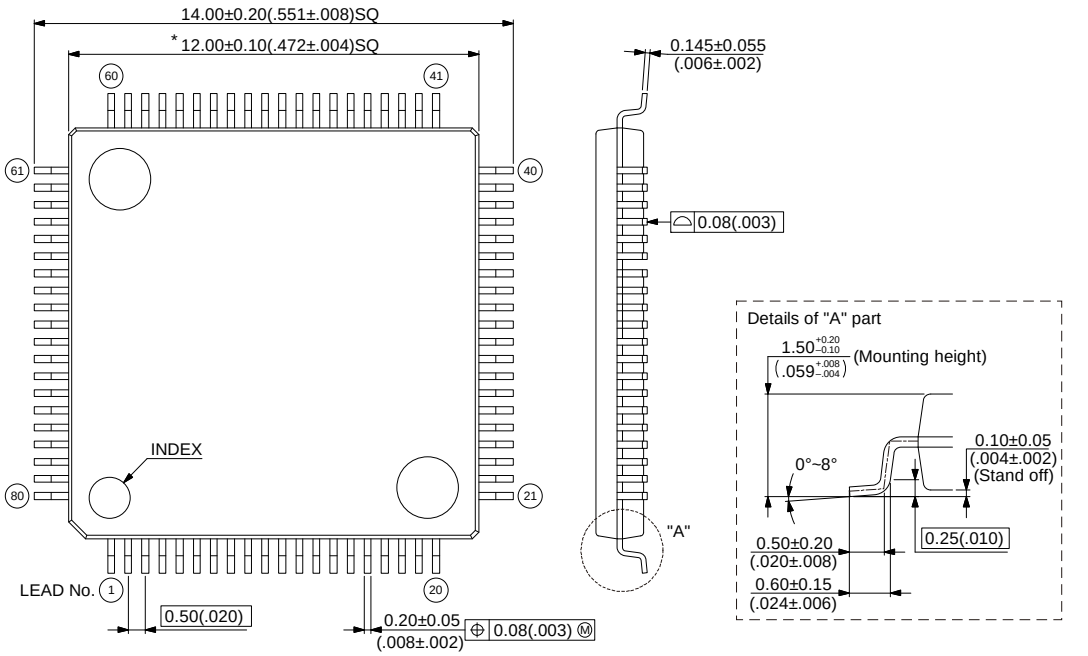
Dimensions in mm (inches).
Note: The values in parentheses are reference values

Please confirm the latest Package dimension by following URL.
http://edevice.fujitsu.com/package/en-search/

80-pin plastic LQFP		
	Lead pitch	0.50 mm
	Package width × package length	12 mm × 12 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm Max
	Weight	0.47 g
(FPT-80P-M21)	Code (Reference)	P-LFQFP80-12×12-0.50

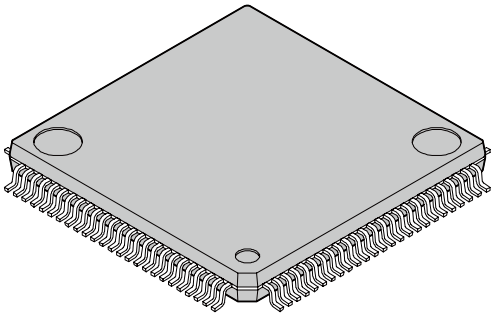
80-pin plastic LQFP
(FPT-80P-M21)

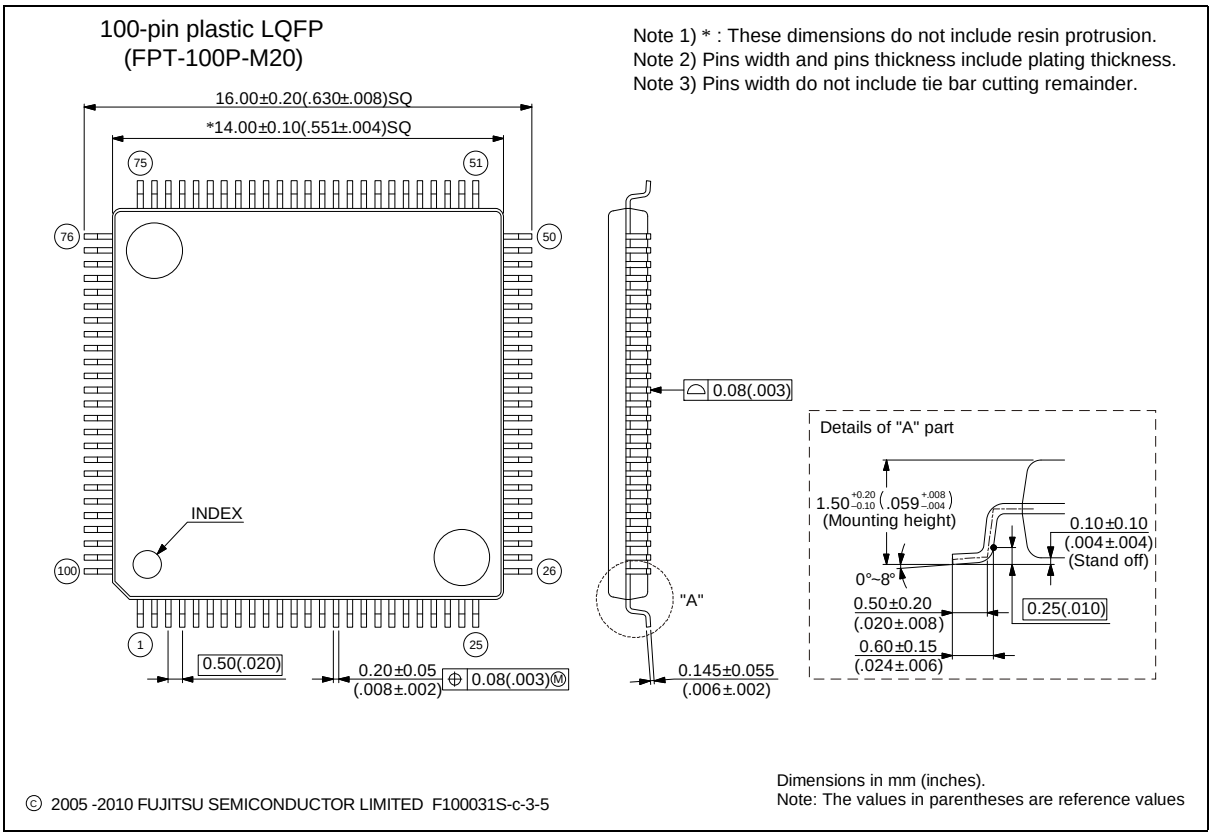
Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



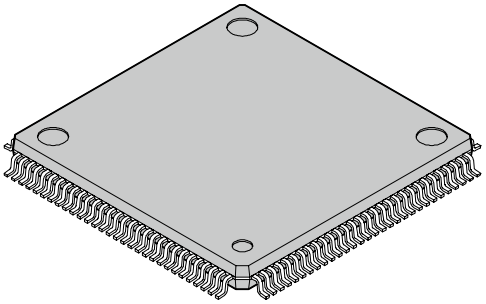
Dimensions in mm (inches).
Note: The values in parentheses are reference values

Please confirm the latest Package dimension by following URL.
http://edevice.fujitsu.com/package/en-search/

100-pin plastic LQFP		
	Lead pitch	0.50 mm
	Package width × package length	14.0 mm × 14.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm Max
	Weight	0.65 g
(FPT-100P-M20)	Code (Reference)	P-LFQFP100-14×14-0.50

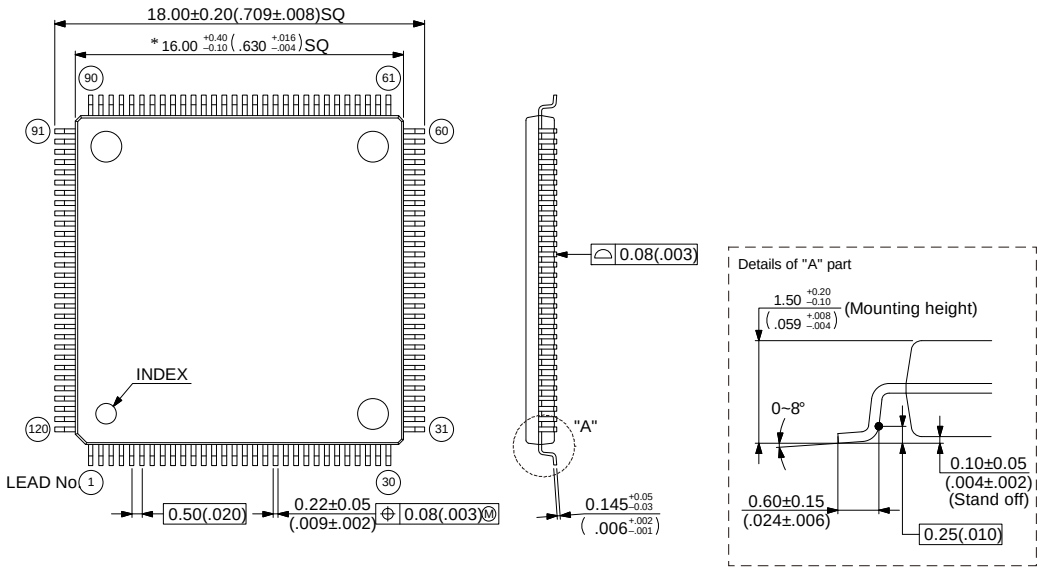


Please confirm the latest Package dimension by following URL.
http://edevice.fujitsu.com/package/en-search/

120-pin plastic LQFP		
	Lead pitch	0.50 mm
	Package width × package length	16.0 × 16.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.88 g
(FPT-120P-M21)	Code (Reference)	P-LFQFP120-16×16-0.50

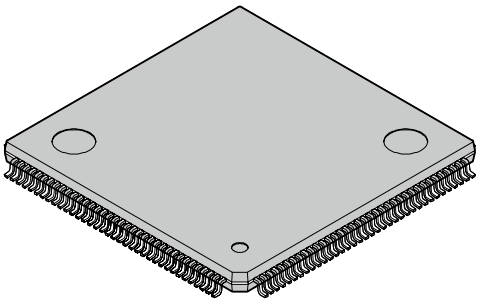
120-pin plastic LQFP
(FPT-120P-M21)

Note 1) * : These dimensions do not include resin protrusion.
Resin protrusion is +0.25(.010) MAX(each side).
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



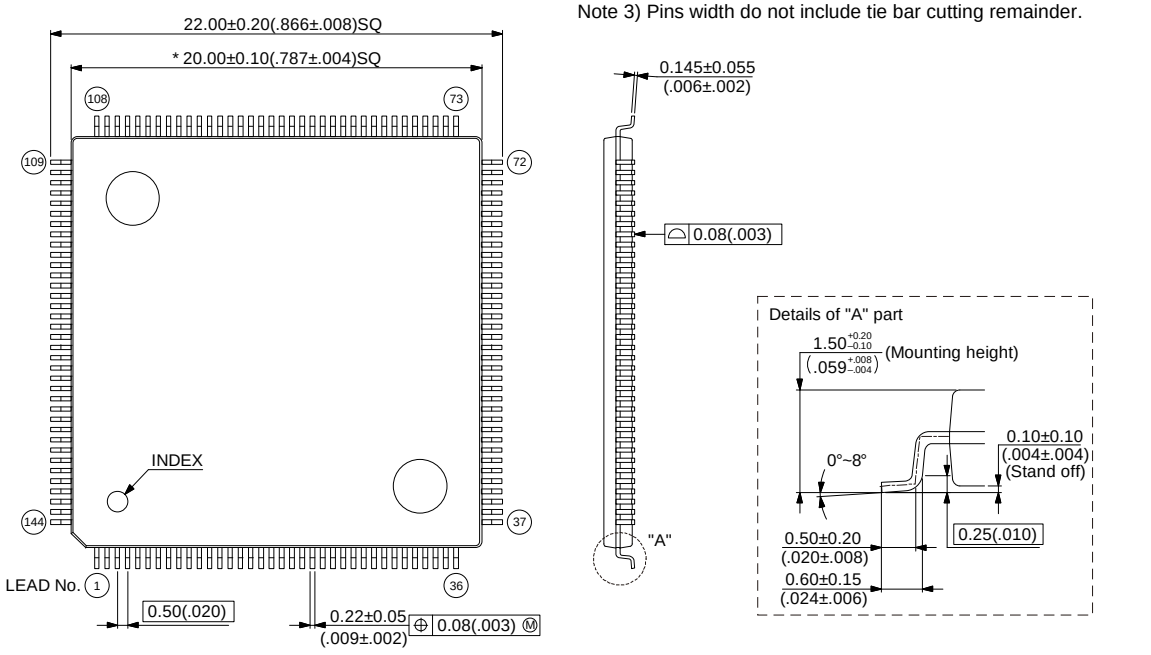
Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please confirm the latest Package dimension by following URL.
http://edevice.fujitsu.com/package/en-search/

144-pin plastic LQFP		
	Lead pitch	0.50 mm
	Package width × package length	20.0 × 20.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	1.20 g
(FPT-144P-M08)	Code (Reference)	P-LFQFP144-20×20-0.50

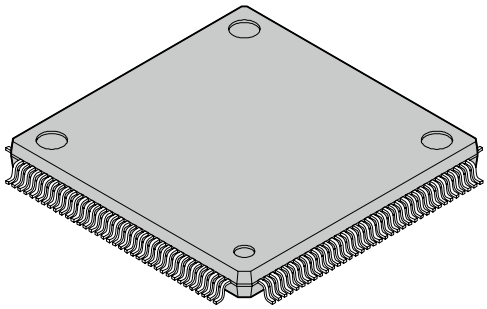
144-pin plastic LQFP
(FPT-144P-M08)

Note 1) *:Values do not include resin protrusion.
Resin protrusion is +0.25(.010)Max(each side).
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



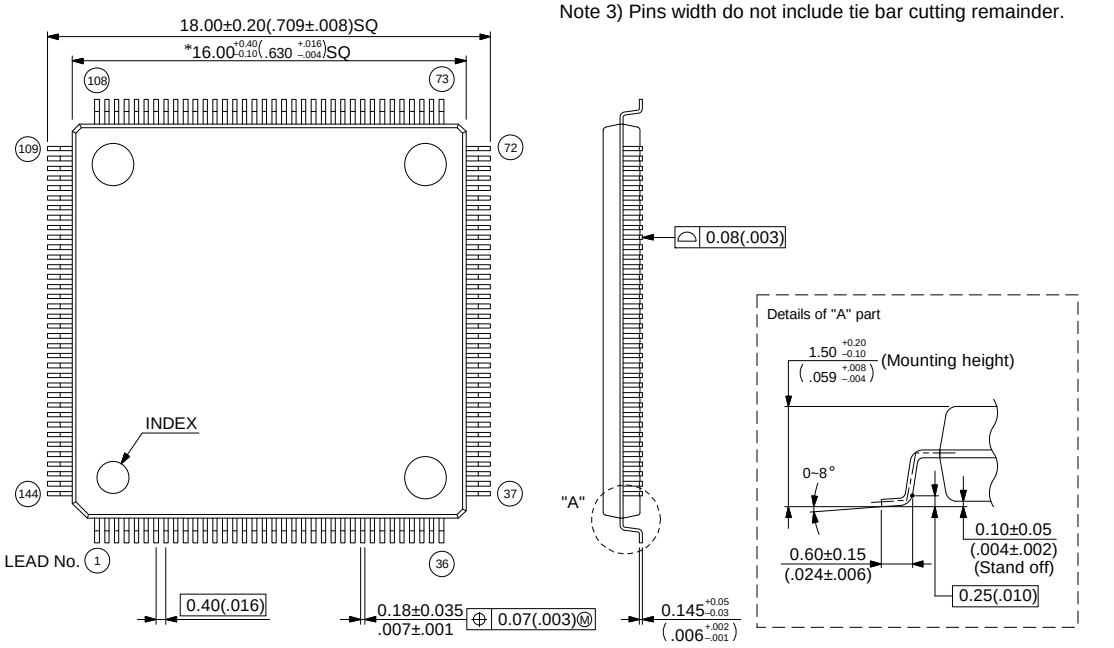
Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please confirm the latest Package dimension by following URL.
http://edevice.fujitsu.com/package/en-search/

144-pin plastic LQFP		
	Lead pitch	0.40 mm
	Package width × package length	16.0 × 16.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.88 g
(FPT-144P-M12)	Code (Reference)	P-LFQFP144-16×16-0.40

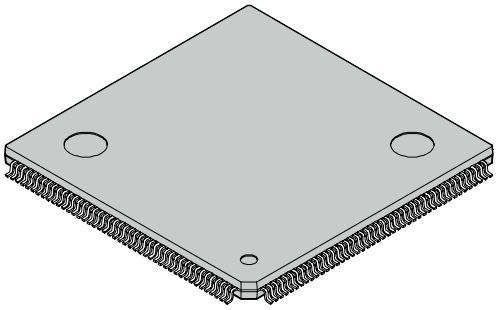
144-pin plastic LQFP
(FPT-144P-M12)

Note 1) * : These dimensions include resin protrusion.
Resin protrusion is +0.25(.010)Max(each side).
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.

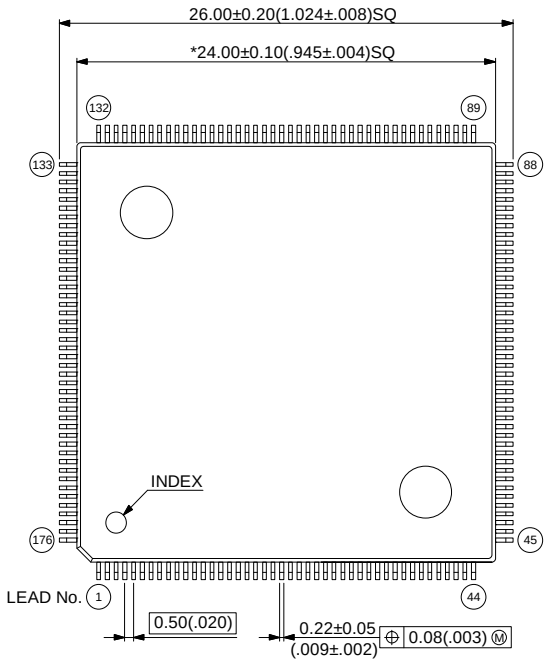


Dimensions in mm (inches).
Note: The values in parentheses are reference values.

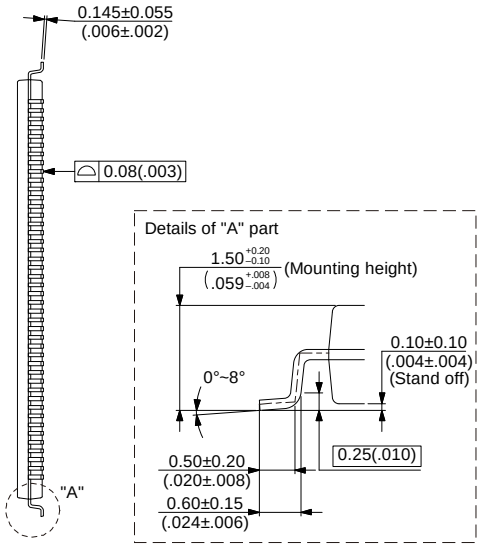
Please confirm the latest Package dimension by following URL.
http://edevice.fujitsu.com/package/en-search/

176-pin plastic LQFP		
 (FPT-176P-M07)	Lead pitch	0.50 mm
	Package width × package length	24.0 × 24.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Code (Reference)	P-LQFP-0176-2424-0.50

176-pin plastic LQFP
(FPT-176P-M07)



Note 1) * : Values do not include resin protrusion.
Resin protrusion is +0.25(.010)Max(each side).
Note 2) Pins width and pins thickness include plating thickness
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please confirm the latest Package dimension by following URL.
http://edevice.fujitsu.com/package/en-search/

■Major Changes

Page	Section	Change Results
Revision 1.0		
-	-	Initial release
Revision 2.0		
3	■FEATURES	Corrected the following description. 5V tolerant input: 4 channels ch.6, ch.8, ch.9, ch.11 Automotive input ↓ 5V tolerant input: 4 channels ch.6, ch.8, ch.9, ch.11 CMOS hysteresis input
33 to 36	■I/O CIRCUIT TYPE	Corrected the following description to "Type F, G, I, J, K, M". Schmitt input → CMOS hysteresis input Corrected the following description to "Type D, E". I^2C Schmitt input → I^2C hysteresis input
44 to 49	■BLOCK DIAGRAM	Corrected the following description. ●MB91F522B, MB91F523B, MB91F524B, MB91F525B, MB91F526B ●MB91F522D, MB91F523D, MB91F524D, MB91F525D, MB91F526D ●MB91F522F, MB91F523F, MB91F524F, MB91F525F, MB91F526F ●MB91F522J, MB91F523J, MB91F524J, MB91F525J, MB91F526J ●MB91F522K, MB91F523K, MB91F524K, MB91F525K, MB91F526K ●MB91F522L, MB91F523L, MB91F524L, MB91F525L, MB91F526L
138	■ELECTRICAL CHARACTERISTICS 2. Recommended operating conditions	Added the following description. *1：When it is used outside recommended operation guarantee range (range of the operation guarantee),contact your sales representative. Moreover, minimum value with an effective external low-voltage detection reset becomes a voltage until generating low-voltage detection reset
139,140	■ELECTRICAL CHARACTERISTICS 3.DC characteristics	Corrected the value of "ICCT5 When using sub clock 32kHz TA=+25°C ". Max 1420µA → Max 2000µA
139	■ELECTRICAL CHARACTERISTICS 3.DC characteristics	Corrected the value of "Power supply voltage range". (TA:-40°C to +105°C,Vcc=AVcc=2.7V to 5.5V,VSS=AVSS=0.0V) ↓ (T_A:-40°C to +105°C,Vcc=AVcc=5.0V±10%/3.3V±0.3V,V_{SS}=AV_{SS}=0.0V)
140,141	■ELECTRICAL CHARACTERISTICS 3.DC characteristics	Corrected the value of "Power supply voltage range". (T_A:-40°C to +125°C,Vcc=AVcc=2.7V to 5.5V,VSS=AVSS=0.0V) ↓ (T_A:-40°C to +125°C,Vcc=AVcc=5.0V±10%/3.3V±0.3V,V_{SS}=AV_{SS}=0.0V)
141	■ELECTRICAL CHARACTERISTICS 3.DC characteristics	Corrected the value of " Pull-up resistance R_{UP1}". Vcc=3.3V±0.3V Min 49 Max 140 →Min 45 Max 140
141	■ELECTRICAL CHARACTERISTICS 3.DC characteristics	Corrected the following description. Pull-up resistance R_{UP2} Port pin other than P035,041,093,122 → P073,074,076,077
141	■ELECTRICAL CHARACTERISTICS 3.DC characteristics	Corrected the value of " Pull-up resistance R_{UP2}". VCC=5.0V±10% Min 25 Max 100 →Min 25 Max 60 VCC=3.3V±0.3V Min 49 Max 140 →Min 33 Max 90
141	■ELECTRICAL CHARACTERISTICS 3.DC characteristics	Added the value of " Pull-up resistance R_{UP3}". Pin name : Port pin other than P035,041,073,074,076,077,093,122 VCC=5.0V±10% Min 25 Max 100 VCC=3.3V±0.3V Min 45 Max 140
150,152, 154,156	■ELECTRICAL CHARACTERISTICS 4. AC characteristics (4) Multi-function Serial (4-1) CSIO timing (4-1-1),(4-1-2),(4-1-3),(4-1-4)	(4-1-1),(4-1-4)SCK↓⇒SOT delay time t_{SLOVI} (4-1-2),(4-1-3)SCK↑⇒SOT delay time t_{SHOVI} Corrected the following description. Pin name: SCK0 to SCK11 SOT0 to SOT11 Value: Min -30 Max 30 ↓ Pin name: SCK0 to SCK2,SCK5 to SCK11 SOT0 to SOT2,SOT5 to SOT11 Value: Min -30 Max 30 Pin name: SCK3,SCK4 SOT3,SOT4 Value: Min -300 Max 300

Page	Section	Change Results
150,152, 154,156	■ELECTRICAL CHARACTERISTICS 4. AC characteristics (4) Multi-function Serial (4-1) CSIO timing (4-1-1),(4-1-2),(4-1-3),(4-1-4)	(4-1-1),(4-1-4)Valid SIN⇒SCK↑ setup time t_{IVSHI} (4-1-2),(4-1-3)Valid SIN⇒SCK↓ setup time t_{IVSLI} Corrected the following description. Pin name: SCK0 to SCK11 SIN0 to SIN11 Value: Min 34 Max - ↓ Pin name: SCK0 to SCK2,SCK5 to SCK11 SIN0 to SIN2,SIN5 to SIN11 Value: Min 34 Max - Pin name: SCK3,SCK4,SIN3,SIN4 Value: Min 300 Max -
150,152, 154,156	■ELECTRICAL CHARACTERISTICS 4. AC characteristics (4) Multi-function Serial (4-1) CSIO timing (4-1-1),(4-1-2),(4-1-3),(4-1-4)	(4-1-1),(4-1-4)SCK↓⇒SOT delay time t_{SLOVE} (4-1-2),(4-1-3)SCK↑⇒SOT delay time t_{SHOVE} Corrected the following description. Pin name: SCK0 to SCK11 SOT0 to SOT11 Value: Min - Max 33 ↓ Pin name: SCK0 to SCK2,SCK5 to SCK11 SOT0 to SOT2,SOT5 to SOT11 Value: Min - Max 33 Pin name: SCK3,SCK4 SOT3,SOT4 Value: Min - Max 300
150,152, 154,156	■ELECTRICAL CHARACTERISTICS 4. AC characteristics (4) Multi-function Serial (4-1) CSIO timing (4-1-1),(4-1-2),(4-1-3),(4-1-4)	(4-1-1),(4-1-2),(4-1-3),(4-1-4)SCK fall time t_F Corrected the following description. Pin name: SCK0 to SCK2,SCK5 to SCK11 Value: Min - Max 5 Pin name: SCK3,SCK4 Value: Min - Max 250 ↓ Pin name: SCK0 to SCK11 Value: Min - Max 5
158,161, 164,167	■ELECTRICAL CHARACTERISTICS 4. AC characteristics (4) Multi-function Serial (4-1) CSIO timing (4-1-5),(4-1-6),(4-1-7),(4-1-8)	(4-1-5)SCS↓⇒SCK↓ setup time t_{CSSI} (4-1-6)SCS↓⇒SCK↑ setup time t_{CSSI} (4-1-7)SCS↑⇒SCK↓ setup time t_{CSSI} (4-1-8)SCS↑⇒SCK↑ setup time t_{CSSI} Corrected the following description. Pin name: SCK1 to SCK11 SCS1 to SCS3,SCS40 to SCS43,SCS50 to SCS53,SCS60 to SCS63,SCS70 to SCS73,SCS8 to SCS11 Value: Min t_{CSSU}+0 Max t_{CSSU}+50 ↓ Pin name: SCK1,SCK2,SCK5 to SCK11 SCS1,SCS2,SCS50 to SCS53,SCS60 to SCS63,SCS70 to SCS73,SCS8 to SCS11 Value: Min t_{CSSU}-50 Max t_{CSSU}+0 Pin name: SCK3,SCK4 SCS3,SCS40 to SCS43 Value: Min t_{CSSU}-50 Max t_{CSSU}+300
158,161, 164,167	■ELECTRICAL CHARACTERISTICS 4. AC characteristics (4) Multi-function Serial (4-1) CSIO timing (4-1-5),(4-1-6),(4-1-7),(4-1-8)	(4-1-5)SCK↑⇒SCS↑hold time t_{CSHI} (4-1-6)SCK↓⇒SCS↑hold time t_{CSHI} (4-1-7)SCK↑⇒SCS↓hold time t_{CSHI} (4-1-8)SCK↓⇒SCS↓hold time t_{CSHI} Corrected the following description. Pin name: SCK1 to SCK11 SCS1 to SCS3,SCS40 to SCS43,SCS50 to SCS53,SCS60 to SCS63,SCS70 to SCS73,SCS8 to SCS11 Value: Min t_{CSHD}-50 Max t_{CSHD}+0 ↓ Pin name: SCK1,SCK2,SCK5 to SCK11 SCS1,SCS2,SCS50 to SCS53,SCS60 to SCS63,SCS70 to SCS73,SCS8 to SCS11 Value: Min t_{CSHD}-10 Max t_{CSHD}+50 Pin name: SCK3,SCK4 SCS3,SCS40 to SCS43 Value: Min t_{CSHD}-300 Max t_{CSHD}+50

Page	Section	Change Results
158,161, 164,167	■ELECTRICAL CHARACTERISTICS 4. AC characteristics (4) Multi-function Serial (4-1) CSIO timing (4-1-5),(4-1-6),(4-1-7),(4-1-8)	(4-1-5),(4-1-6)SCS↓⇒SOT delay time t_{DSE} (4-1-7),(4-1-8)SCS↑⇒SOT delay time t_{DSE} Corrected the following description. Pin name: SCS1 to SCS3,SCS40 to SCS43,SCS50 to SCS53,SCS60 to SCS63,SCS70 to SCS73,SCS8 to SCS11 SOT1 to SOT11 Value: Min - Max 40 ↓ Pin name: SCS1,SCS2,SCS50 to SCS53,SCS60 to SCS63,SCS70 to SCS73,SCS8 to SCS11 SOT1,SOT2,SOT5 to SOT11 Value: Min - Max 40 Pin name: SCS3,SCS40 to SCS43 SOT3,SOT4 Value: Min - Max 300
159,162, 165,168	■ELECTRICAL CHARACTERISTICS 4. AC characteristics (4) Multi-function Serial (4-1) CSIO timing (4-1-5),(4-1-6),(4-1-7),(4-1-8)	(4-1-5)SCK↓⇒SCS↓ clock switch time t_{SCC} (4-1-6)SCK↑⇒SCS↓ clock switch time t_{SCC} (4-1-7)SCK↓⇒SCS↑ clock switch time t_{SCC} (4-1-8)SCK↑⇒SCS↑ clock switch time t_{SCC} Corrected the following description. Pin name: SCK1 to SCK11 SCS1 to SCS3,SCS40 to SCS43,SCS50 to SCS53,SCS60 to SCS63,SCS70 to SCS73,SCS8 to SCS11 Value: Min $3t_{CPP}$+0 Max $3t_{CPP}$+50 ↓ Pin name: SCK1,SCK2,SCK5 to SCK11 SCS1,SCS2,SCS50 to SCS53,SCS60 to SCS63,SCS70 to SCS73,SCS8 to SCS11 Value: Min $3t_{CPP}$-10 Max $3t_{CPP}$+50 Pin name: SCK3,SCK4 SCS3,SCS40 to SCS43 Value: Min $3t_{CPP}$-300 Max $3t_{CPP}$+50
159,162, 165,168	■ELECTRICAL CHARACTERISTICS 4. AC characteristics (4) Multi-function Serial (4-1) CSIO timing (4-1-5),(4-1-6),(4-1-7),(4-1-8)	Added the following description. Regardless of the deselect time setting, once after the serial chip select pin becomes inactive, it will take at least five peripheral bus clock cycles to be active again
184	■ELECTRICAL CHARACTERISTICS 5.A/D Converter (1) 12-bit A/D Converter Electrical Characteristics	Added the value of "Total error". Total error value Min – Typ – Max ±12 LSB
184	■ELECTRICAL CHARACTERISTICS 5.A/D Converter (1) 12-bit A/D Converter Electrical Characteristics	Corrected the value of "Zero transition voltage". Min AVRL+0.5LSB-20mV Max AVRL+0.5LSB+20mV ↓ Min AVRL-11.5LSB Max AVRL+12.5LSB
184	■ELECTRICAL CHARACTERISTICS 5.A/D Converter (1) 12-bit A/D Converter Electrical Characteristics	Corrected the value of "Full-scale transition voltage". Min AVRH-1.5LSB-20mV Max AVRH-1.5LSB+20mV ↓ Min AVRH-13.5LSB Max AVRH+10.5LSB
184	■ELECTRICAL CHARACTERISTICS 5.A/D Converter (1) 12-bit A/D Converter Electrical Characteristics	Added the following description. Parameter : Power supply current I_A AVCC*3 *3: The power supply current described only current value on A/D converter. The total AVcc current value must be calculated the power supply current for A/D converter and D/A converter.
188	■ELECTRICAL CHARACTERISTICS 7.D/A Converter	Added the following description. Parameter : Power supply current *1 *1: The power supply current described only current value on D/A converter.The total Avcc current value must be calculated the power supply current for D/A converter and A/D converter.
187	■ELECTRICAL CHARACTERISTICS 6.Flash memory	Parameter: Erase cycle*2/Data retain time Deleted the following description. Remarks : "Temperature at writing/erasing Tj<+105°C"

Page	Section	Change Results
188	■ELECTRICAL CHARACTERISTICS 7.D/A Converter	Corrected the following description. Parameter : Power supply current Symbol IA Pin name AV_{CC} Symbol IAH Pin name AV_{CC} ↓ Symbol IA Pin name AVCC Symbol IAH Pin name AVCC
190	■EXAMPLE CHARACTERISTICS	Corrected the following description. Watch mode
192	■ORDERING INFORMATION	Corrected the following description. ■ORDERING INFORMATION ↓ ■ORDERING INFORMATION MB91F52xxxB[*1] Package ↓ Package[*2]
198	■ORDERING INFORMATION	Added the following description. [*1]: It is only supported for customers who have already adopted it now. We do not recommend adopting new products.
198	■ORDERING INFORMATION	Corrected the following description. For details of the package, see "■ PACKAGE DIMENSIONS ". ↓ [*2]: For details of the package, see "■ PACKAGE DIMENSIONS ".
199 to 205	■ORDERING INFORMATION	Added the following description. ■ORDERING INFORMATION MB91F52xxxC
-	-	Company name and layout design change

Colophon

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