FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-16502-3E

32-Bit Proprietary Microcontroller

CMOS

FR60 MB91301 Series

MB91302A/V301A

■ DESCRIPTION

The MB91301 series are a line of microcontrollers based on a 32-bit RISC CPU core (FR family) , incorporating a variety of I/O resources and a bus control mechanism for embedded control that requires the processing of a high-performance, fast CPU as well as an SDRAM interface that can connect SDRAM directly to the chip.
The large address space supported by the 32-bit CPU addressing means that operation is primarily based on external bus access although instruction cache memory of 4 Kbytes and RAM of 4 Kbytes(for data) are included for high-speed execution of CPU instructions.
The MB91302A and MB91V301A are FR60 products based on the FR30/40 CPU with enhanced bus access for higher speed operation. The device specifications include a D/A converter to facilitate motor control and are ideal for use in DVD players that support fly-by transfer.

■ FEATURES

The MB91301 series is a line of ICs with various programs embedded in internal ROM.

ROM variation / Product name	Built-in the real time OS version	Built-in IPL (Internal Program Loader) version	User ROM version	Without ROM version
MB91302A	○	○	○	○

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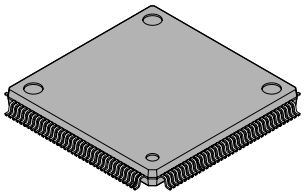
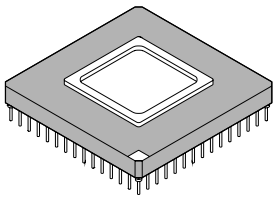
■ PACKAGES

144-pin, Plastic LQFP



(FPT-144P-M12)

179-pin, Ceramic PGA



(PGA-179C-A03)

FUJITSU

1. FR CPU

- 32-bit RISC, load/store architecture, 5-stage pipeline
- 68 MHz internal operating frequency (Max) [external (Max) 68 MHz] (when using PLL with base frequency (Max) = 17 MHz)
- General purpose registers : 32 bits×16
- 16-bit fixed length instructions (basic instructions) , 1 instruction per cycle
- Instruction set optimized for embedded applications: Memory-to-memory transfer, bit manipulation, barrel shift etc.
- Instructions adapted for high-level languages : Function entry/exit instructions, multiple-register load/store instructions
- Easier assembler coding : Register interlock function
- Branch instructions with delay slots : Reduced overhead time in branch executions
- Built-in multiplier with instruction-level support
  Signed 32-bit multiplication : 5 cycles
  Signed 16-bit multiplication : 3 cycles
- Interrupt (PC, PS save) : 6 cycles, 16 priority levels

2. Bus interface

- Operating frequency : Max 68 MHz (when using SDRAM)
- Full 24-bit address output (16 Mbytes memory space)
- 8-bit, 16-bit or 32-bit data input/output
- Built-in pre-fetch buffer
- Unused data and address pins can be used as general-purpose input/output ports.
- Eight fully independent chip select outputs, can be set in minimum 64 Kbytes units.
- Supports the following memory interfaces
  Asynchronous SRAM, asynchronous ROM/Flash
  Page mode ROM/Flash ROM (selectable page size = 1, 2, 4, or 8)
  Burst mode ROM/Flash ROM (MBM29BL160D/161D/162D)
- SDRAM (FCRAM Type, CAS Latency 1 to 8, 2/4 bank products.)
- Address/Data multiplex bus (only 8/16-bit width)
- Basic bus cycle : 2 cycles
- Automatic wait cycle generation function can insert wait cycles, independently programmable for each memory area.
- RDY input for external wait cycles
- Endian setting of byte ordering (Big/Little)
  $\overline{CS0}$ area only for big endian
- Prohibition setting of write (only for Read)
- Permission/prohibition setting of fetch into built-in cache
- Permission/prohibition setting of prefetch function
- DMA supports fly-by transfer with independent I/O wait control
- External bus arbitration can be used using BRQ and $\overline{BGRNT}$.

3. Built-in memory

- 4 Kbytes DATA RAM
- 4 Kbytes RAM (MB91302A)

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4. Instruction cache
- Size : 4 Kbytes
- 2-way set associative
- 128 blocks/way, 4 entries/block
- Lock function enables program code to be made cache-resident
- Areas not used for instruction cache can be used as instruction RAM

5. DMAC (DMA Controller)
- 5-channel (2-channel external-to-external)
- 3 transfer triggers : External pin, internal peripheral, software
- Capable of selecting an internal peripheral as a transfer source freely for each channel
- Addressing using 32-bit full addressing mode (increment, decrement, fixed)
- Transfer modes : Demand transfer, burst transfer, step transfer, or block transfer
- Supports fly-by transfer (between external I/O and memory)
- Selectable transfer data size : 8, 16, or 32-bit

6. Bit search module
- Searches words from MSB for position of first 1/0 bit value change

7. Reload Timers
- 16-bit timer : 3 channels
- Internal clock : 2 clock cycle resolution, divide by 2/8/32 selective

8. UART
- Full duplex, double buffer UART
- Independent 3 channels
- Data length : 7 bits to 9 bits (without parity) , 6 bits to 8 bits (with parity)
- Asynchronous (start-stop synchronized) or CLK-synchronous communications selectable
  Multi-processor mode
- Built-in 16-bit timer (U-TIMER) as a baud rate generator to generate arbitrary baud rates
- External clock can be used as transfer clock
- Variety of error detection functions (parity, frame, overrun)

9. Interrupt controller
- External interrupt input : 1 non-maskable interrupt pin and 8 normal interrupt pins (INT0 to INT7)
- Internal internal resources : UART, DMAC, A/D, U-TIMER, Delay interrupt, I^2C, Free-run timer, Input capture
- Programmable priorities (16 levels) for all interrupts except the non-maskable interrupt

10. A/D converter
- 10-bit resolution, 4 channels
- Successive approximation type, conversion time : 4.1 µs at 34 MHz
- Built-in sample and hold circuit
- Conversion modes : Single conversion mode, scan conversion mode and repeat conversion mode selectable
- Conversion triggers : Software, external trigger and built-in timer selectable

11. I^2C* interface
- Internal 2-channels master/slave transmit/receive
- Internal arbitration function, clock synch function

12. Free-run timer
- 16 bit : 1channel

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13. Input capture

- 4 channels

14. Other interval timers

- 16-bit timer : 3 channels (U-TIMER)
- PPG timer : 4 channels
- Watchdog timer : 1 channel

15. Other features

- Reset resources : watchdog timer/software reset/external reset ($\overline{\text{INIT}}$ pin)
- Power-saving modes : Stop mode, sleep mode
- Clock control
  Gear function : Allows arbitrary different operating clock frequencies to be set for the CPU and peripherals. You can select one of the 16 gear clock factors of 1/1 to 1/16. PLL multiplication can also be selected. Note, however, that peripherals operate at a maximum of 34 MHz.
- CMOS technology : 0.25 µm
- Power supply (analog power supply): 3.3 V ± 0.3 V (internal regulator used)

* : Purchase of Fujitsu I²C components conveys a license under the Philips I²C Patent Rights to use, these components in an I²C system provided that the system conforms to the I²C Standard Specification as defined by Philips.

■ PRODUCT LINEUP

	MB91302A	MB91V301A
Type	Mask ROM product (for volume production)	Evaluation version (For evaluation and development)
RAM	4 Kbytes (only for data)	16 Kbytes (data 8 KB+8 KB)
ROM	4 Kbytes ROM has non-ROM model, the optimal real time OS internal model*1, and the IPL (Internal Program Loader) internal model*2 by adding the user ROM model.	8 Kbytes (RAM)
DSU	—	DSU4
Package	LQFP-144 (0.4 mm pitch)	PGA-179

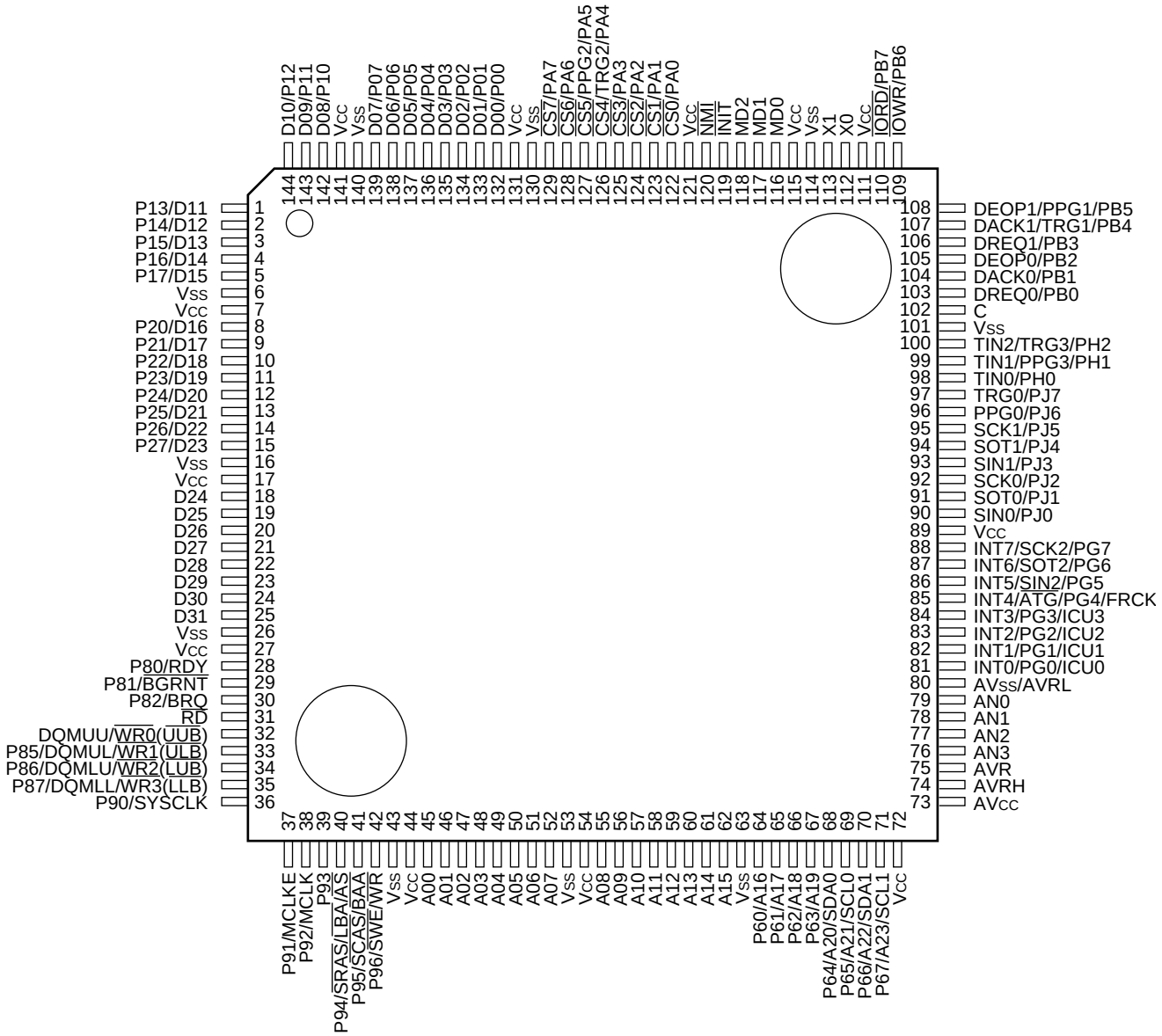
*1 : The Fujitsu product of real time OS REALOS/FR by conforming to the µITRON 3.0 is stored and optimized with the MB91302A.

*2 : The ROM stores the IPL (Internal Program Loader) . Loading various programs can be executed from the external system by the internal UART/SIO. Using this function, for example, writing on board to the Flash memory connected to the external can be executed.

■ PIN ASSIGNMENTS

- MB91302A

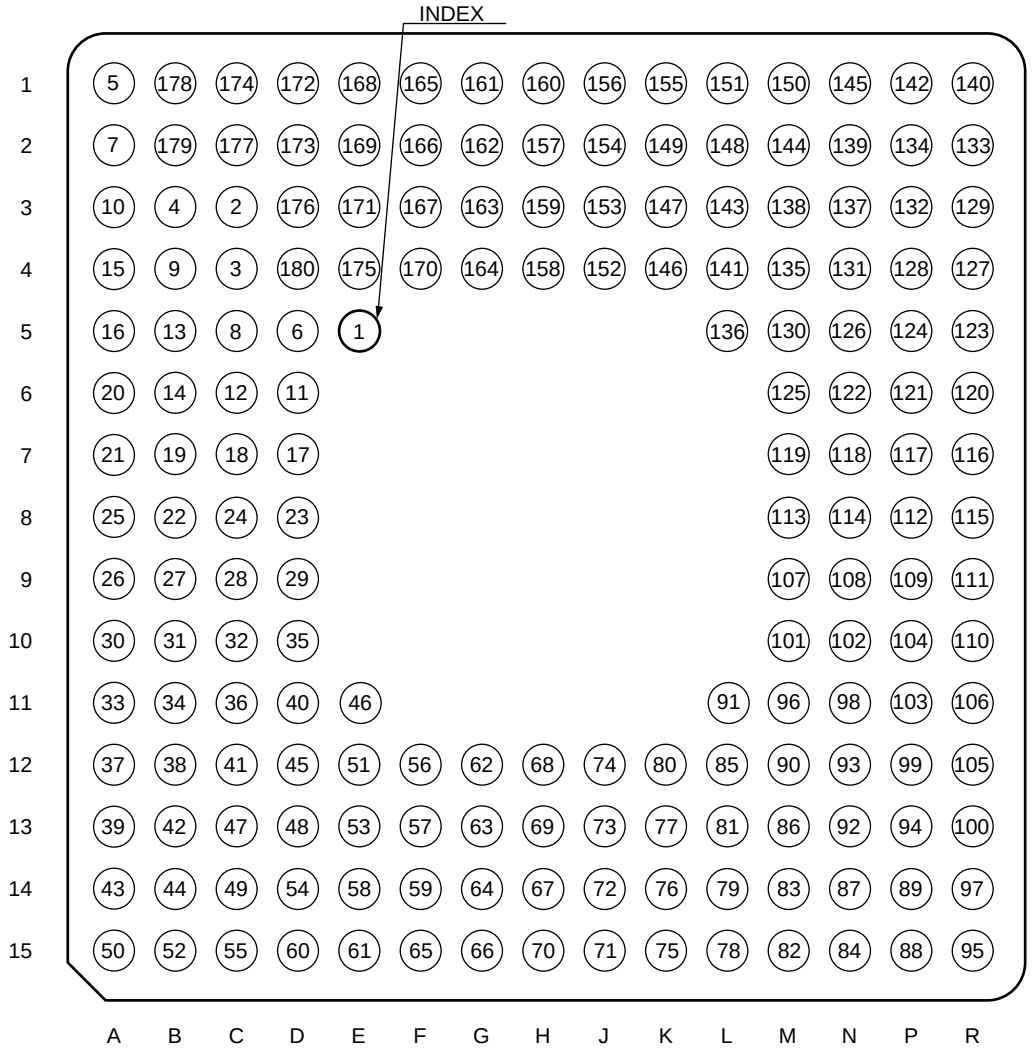
(TOP VIEW)



(FPT-144P-M12)

- MB91V301A

(TOP VIEW)



(PGA-179C-A03)

• **MB91V301A Pin No. Table**

No.	PIN	Pin Name	No.	PIN	Pin Name	No.	PIN	Pin Name
1	E5	N.C.	31	B10	V_{SS}	61	E15	A07
2	C3	P13/D11	32	C10	V_{CC}	62	G12	V_{SS}
3	C4	V_{SS}	33	A11	P80/RDY	63	G13	V_{CC}
4	B3	V_{CC}	34	B11	P81/$\overline{BGRNT}$	64	G14	A08
5	A1	P14/D12	35	D10	P82/BRQ	65	F15	A09
6	D5	P15/D13	36	C11	$\overline{RD}$	66	G15	A10
7	A2	P16/D14	37	A12	DQMUU/$\overline{WR0}$ ($\overline{UUB}$)	67	H14	A11
8	C5	P17/D15	38	B12	P85/DQMUL/$\overline{WR1}$ ($\overline{ULB}$)	68	H12	A12
9	B4	V_{SS}	39	A13	P86/DQMLU/$\overline{WR2}$ ($\overline{LUB}$)	69	H13	A13
10	A3	V_{CC}	40	D11	P87/DQMLL/$\overline{WR3}$ ($\overline{LLB}$)	70	H15	A14
11	D6	P20/D16	41	C12	V_{SS}	71	J15	A15
12	C6	P21/D17	42	B13	V_{CC}	72	J14	V_{SS}
13	B5	P22/D18	43	A14	P90/SYSCLK	73	J13	V_{CC}
14	B6	P23/D19	44	B14	P91/MCLKE	74	J12	P60/A16
15	A4	P24/D20	45	D12	P92/MCLK	75	K15	P61/A17
16	A5	P25/D21	46	E11	P93	76	K14	P62/A18
17	D7	P26/D22	47	C13	V_{SS}	77	K13	P63/A19
18	C7	P27/D23	48	D13	V_{CC}	78	L15	SDA0/P64/A20
19	B7	V_{SS}	49	C14	P94/$\overline{SRAS}$/$\overline{LBA}$/$\overline{AS}$	79	L14	SCL0/P65/A21
20	A6	V_{CC}	50	A15	P95/$\overline{SCAS}$/$\overline{BAA}$	80	K12	SDA1/P66/A22
21	A7	D24	51	E12	P96/$\overline{SWE}$/$\overline{WR}$	81	L13	SCL1/P67/A23
22	B8	D25	52	B15	V_{SS}	82	M15	V_{CC}
23	D8	D26	53	E13	V_{CC}	83	M14	V_{CC}
24	C8	D27	54	D14	A00	84	N15	$\overline{EWR3}$
25	A8	V_{SS}	55	C15	A01	85	L12	$\overline{EWR2}$
26	A9	V_{CC}	56	F12	A02	86	M13	$\overline{EWR1}$
27	B9	D28	57	F13	A03	87	N14	$\overline{EWR0}$
28	C9	D29	58	E14	A04	88	P15	$\overline{ECS}$
29	D9	D30	59	F14	A05	89	P14	EMRAM
30	A10	D31	60	D15	A06	90	M12	ICD3

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No.	PIN	Pin Name	No.	PIN	Pin Name	No.	PIN	Pin Name
91	L11	ICD2	121	P6	SOT0/PJ1	151	L1	V_{CC}
92	N13	ICD1	122	N6	SCK0/PJ2	152	J4	$\overline{INIT}$
93	N12	ICD0	123	R5	SIN1/PJ3	153	J3	$\overline{NMI}$
94	P13	V_{SS}	124	P5	SOT1/PJ4	154	J2	V_{SS}
95	R15	V_{CC}	125	M6	SCK1/PJ5	155	K1	V_{CC}
96	M11	BREAK	126	N5	PPG0/PJ6	156	J1	$\overline{CS0}$/PA0
97	R14	ICLK	127	R4	TRG0/PJ7	157	H2	$\overline{CS1}$/PA1
98	N11	ICS2	128	P4	TIN0/PH0	158	H4	$\overline{CS2}$/PA2
99	P12	ICS1	129	R3	TIN1/PPG3/PH1	159	H3	$\overline{CS3}$/PA3
100	R13	ICS0	130	M5	TIN2/TRG3/PH2	160	H1	$\overline{CS4}$/TRG2/PA4
101	M10	$\overline{TRST}$	131	N4	V_{SS}	161	G1	$\overline{CS5}$/PPG2/PA5
102	N10	C	132	P3	C	162	G2	$\overline{CS6}$/PA6
103	P11	AV_{CC}	133	R2	DREQ0/PB0	163	G3	$\overline{CS7}$/PA7
104	P10	AVRH	134	P2	DACK0/PB1	164	G4	V_{SS}
105	R12	AVR	135	M4	DEOP0/PB2	165	F1	V_{CC}
106	R11	AN3	136	L5	DREQ1/PB3	166	F2	D00/P00
107	M9	AN2	137	N3	DACK1/TRG1/PB4	167	F3	D01/P01
108	N9	AN1	138	M3	DEOP1/PPG1/PB5	168	E1	D02/P02
109	P9	AN0	139	N2	$\overline{IOWR}$/PB6	169	E2	D03/P03
110	R10	AV_{SS}/AVRL	140	R1	$\overline{IORD}$/PB7	170	F4	V_{SS}
111	R9	INT0/PG0/ICU0	141	L4	V_{CC}	171	E3	V_{CC}
112	P8	INT1/PG1/ICU1	142	P1	V_{SS}	172	D1	D04/P04
113	M8	INT2/PG2/ICU2	143	L3	X0	173	D2	D05/P05
114	N8	INT3/PG3/ICU3	144	M2	X1	174	C1	D06/P06
115	R8	INT4/$\overline{ATG}$/PG4/FRCK	145	N1	V_{SS}	175	E4	D07/P07
116	R7	INT5/SIN2/PG5	146	K4	V_{CC}	176	D3	V_{SS}
117	P7	INT6/SOT2/PG6	147	K3	MD0	177	C2	V_{CC}
118	N7	INT7/SCK2/PG7	148	L2	MD1	178	B1	D08/P10
119	M7	V_{CC}	149	K2	MD2	179	B2	D09/P11
120	R6	SIN0/PJ0	150	M1	V_{CC}	180	D4	D10/P12

■ PIN DESCRIPTIONS

• Except for Power supply, GND, and Tool pins

Pin no.		Pin name	I/O circuit type	Function
MB91302A	MB91V301A			
132 to 139	166 to 169, 172 to 175	D00 to D07	J	External data bus bits 0 to 7. It is available in the external bus mode.
		P00 to P07		Can be used as ports in 8-bit or 16-bit external bus mode.
142 to 144, 1 to 5	178 to 180, 2, 5 to 8	D08 to D15	J	External data bus bits 8 to 15. It is available in the external bus mode.
		P10 to P17		Can be used as ports in 8-bit or 16-bit external bus mode.
8 to 15	11 to 18	D16 to D23	J	External data bus bits 16 to 23. It is available in the external bus mode.
		P20 to P27		Can be used as ports in 8-bit external bus mode.
18 to 25	21 to 24, 27 to 30	D24 to D31	C	External data bus bits 24 to 31. It is available in the external bus mode.
28	33	RDY	J	External ready input. The pin has this function when external ready input is enabled.
		P80		General purpose input/output port. The pin has this function when external ready input is disabled.
29	34	$\overline{\text{BGRNT}}$	J	Acknowledge output for external bus release. Outputs "L" when the external bus is released. The pin has this function when output is enabled.
		P81		General purpose input/output port. The pin has this function when output is disabled for external bus release acknowledge.
30	35	BRQ	J	External bus release request input. Input "1" to request release of the external bus. The pin has this function when input is enabled.
		P82		General purpose input/output port. The pin has this function when the external bus release request input is disabled.
31	36	$\overline{\text{RD}}$	C	External bus read strobe output.
32	37	$\overline{\text{WR0}}$/ ($\overline{\text{UUB}}$) / DQMUU	C	External bus write strobe output. When $\overline{\text{WR}}$ is used as the write strobe, this becomes the byte-enable pin ($\overline{\text{UUB}}$). Select signal (DQMUU) of D31 to D24 at using of SDRAM.

(Continued)

Pin no.		Pin name	I/O circuit type	Function
MB91302A	MB91V301A			
33	38	$\overline{WR1}$/ ($\overline{ULB}$) / DQMUL	J	External bus write strobe output. The pin has this function when $\overline{WR1}$ output is enabled. When $\overline{WR}$ is used as the write strobe, this becomes the byte-enable pin ($\overline{ULB}$). Select signal (DQMUL) of D23 to D16 at using of SDRAM.
		P85		General purpose input/output port. The pin has this function when the external bus write-enable output is disabled.
34	39	$\overline{WR2}$/ ($\overline{LUB}$) / DQMLU	J	External bus write strobe output. The pin has this function when $\overline{WR2}$ output is enabled. When $\overline{WR}$ is used as the write strobe, this becomes the byte-enable pin ($\overline{LUB}$). Select signal (DQMLU) of D08 to D05 at using of SDRAM.
		P86		General purpose input/output port. The pin has this function when the external bus write-enable output is disabled.
35	40	$\overline{WR3}$/ ($\overline{LLB}$) / DQMLL	J	External bus write strobe output. The pin has this function when $\overline{WR3}$ output is enabled. When $\overline{WR}$ is used as the write strobe, this becomes the byte-enable pin ($\overline{LLB}$). Select signal (DQMLL) of D07 to D00 at using of SDRAM.
		P87		General purpose input/output port. The pin has this functions when the external bus write-enable output is disabled.
36	43	SYSCLK	C	System clock output. The pin has this function when system clock output is enabled. This outputs the same clock as the external bus operating frequency. (Output halts in stop mode.)
		P90		General purpose input/output port. The pin has this function when system clock output is disabled.
37	40	MCLKE	J	Clock enable signal for memory.
		P91		General purpose input/output port. The pin has this function when clock enable output is disabled.
38	45	MCLK	C	Memory clock output. The pin has this function when memory clock output is enabled. This outputs the same clock as the external bus operating frequency. (Output halts in sleep mode.)
		P92		General purpose input/output port. The pin has this function when memory clock output is disabled.
39	46	P93	C	General purpose input/output port.

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Pin no.		Pin name	I/O circuit type	Function
MB91302A	MB91V301A			
40	49	$\overline{AS}$	J	Address strobe output. The pin has this function when $\overline{ASE}$ bit of port function register 9 is enabled “1”.
		$\overline{LBA}$		Address strobe output for burst flash ROM. The pin has this function when $\overline{ASE}$ bit of port function register 9 is enabled “1”.
		$\overline{SRAS}$		RAS single for SDRAM. This pin has this function when $\overline{ASE}$ bit of port function register 9 is enabled “1”.
		$\overline{P94}$		General purpose input/output port. The pin has this function when $\overline{ASE}$ bit of port function register 9 is "0" general purpose port.
41	50	$\overline{BAA}$	J	Address advance output for burst Flash ROM. The pin has this function when BAAE bit of port function register (PFR9) is enabled.
		$\overline{SCAS}$		CAS signal for SDRAM. This pin has this function when BAAE bit of port function register (PFR9) is enabled.
		$\overline{P95}$		General purpose input/output port. The pin has this function when BAAE bit of port function register is general purpose port.
42	51	$\overline{WR}$	J	Memory write strobe output. This pin has this function when WRXE bit of port function register is enabled.
		$\overline{SWE}$		Write output for SDRAM. This pin has this function when WRXE bit of port function register is enabled.
		P96		General purpose input/output port. This pin has this function when WRXE bit of port function register is general purpose port.
45 to 52	54 to 61	A00 to A07	C	External address bits 0 to 7.
55 to 62	64 to 71	A08 to A15	C	External address bits 8 to 15.
64 to 67	74 to 77	A16 to A19	J	External address bits 16 to 19. It is available in external bus mode.
		P60 to P63		Can be used as ports when external address bus is not used.

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Pin no.		Pin name	I/O circuit type	Function
MB91302A	MB91V301A			
68	78	SDA0	T	Data input pin for I²C bus function. This function is enable when typical operation of I²C is enable. The port output must remains off unless intentionally turned on. (Open drain output) (This function is only for MB91302A, MB91V301A.)
		A20		External address bus bit 20. This function is enable during prohibited I²C operation and using external bus.
		P64		General-purpose I/O port. This function is enable during prohibited I²C and nonused external address bus.
69	79	SCL0	T	CLK input pin for I²C bus function. This function is enable when typical operation of I²C is enable. The port output must remains off unless intentionally turned on. (open drain output) (This function is only for MB91302A, MB91V301A.)
		A21		External address bus bit 21. This function is enable during prohibited I²C operation and using external bus.
		P65		General-purpose I/O port. This function is enable during prohibited I²C and nonused external address bus.
70	80	SDA1	T	DATA input pin for I²C bus function. This function is enable when typical operation of I²C is enable. The output must remains off unless intentionally turned on. (open drain output) (This function is only for MB91302A, MB91V301A.)
		A22		External address bus bit 20. This function is enable during prohibited I²C operation and using external bus.
		P66		General-purpose I/O port. This function is enable during prohibited I²C and nonused external address bus.

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Pin no.		Pin name	I/O circuit type	Function
MB91302A	MB91V301A			
71	81	SCL1	T	CLK input pin for I²C bus function. This function is enable when typical operation of I²C is enable. The port output must remains off unless intentionally turned on. (open drain output) (This function is only for MB91302A, MB91V301A.)
		A23		External address bus bit 21. This function is enable during prohibited I²C operation and using external bus.
		P67		General-purpose I/O port. This function is enable during prohibited I²C operation and nonused external address bus.
76 to 79	106 to 109	AN3 to AN0	D	Analog input pin.
81 to 84	111 to 114	INT0 to INT3	V	External interrupt inputs. These inputs are used continuously when the corresponding external interrupt is enabled. In this case, do not output to these ports unless doing so intentionally.
		PG0 to PG3		General purpose input/output ports.
		ICU0 to ICU3		Input capture input pins. These inputs are used continuously when selected as input capture inputs. In this case, do not output to these ports unless doing so intentionally.
85	115	INT4	V	External interrupt input. These inputs are used continuously when the corresponding external interrupt is enabled. In this case, do not output to these ports unless doing so intentionally.
		$\overline{\text{ATG}}$		External trigger input for A/D converter. This input is used continuously when selected as the A/D converter start trigger. In this case, do not output to this port unless doing so intentionally.
		PG4		General purpose input/output ports.
		FRCK		External clock input pin for free-run timer. This input is used continuously when selected as the external clock input pin for the free-run timer. In this case, do not output to this port unless doing so intentionally.
86	116	INT5	V	External interrupt input. These inputs are used continuously when the corresponding external interrupt is enabled. In this case, do not output to these ports unless doing so intentionally.
		SIN2		UART2 data input pin. This input is used continuously when UART2 is performing input. In this case, do not output to this port unless doing so intentionally.
		PG5		General purpose input/output port.

(Continued)

Pin no.		Pin name	I/O circuit type	Function
MB91302A	MB91V301A			
87	117	INT6	V	External interrupt input. This input is used continuously when the corresponding external interrupt is enabled. In this case, do not output to these ports unless doing so intentionally.
		SOT2		UART2 data output pin. The pin has this function when UART2 data output is enabled.
		PG6		General purpose input/output port.
88	118	INT7	V	External interrupt input. This input is used continuously when the corresponding external interrupt is enabled. In this case, do not output to these ports unless doing so intentionally.
		SCK2		UART2 clock input/output pin. The pin has this function when UART2 clock output is enabled.
		PG7		General purpose input/output port.
90	120	SIN0	U	UART0 data input pin. This input is used continuously when UART0 is performing input. In this case, do not output to this port unless doing so intentionally.
		PJ0		General purpose input/output port.
91	121	SOT0	U	UART0 data output pin. The pin has this function when UART0 data output is enabled.
		PJ1		General purpose input/output port.
92	122	SCK0	U	UART0 clock input/output pin. The pin has this function when UART0 clock output is enabled.
		PJ2		General purpose input/output port.
93	123	SIN1	U	UART1 data input pin. This input is used continuously when UART1 is performing input. In this case, do not output to this port unless doing so intentionally.
		PJ3		General purpose input/output port.
94	124	SOT1	U	UART1 data output pin. The pin has this function when UART1 data output is enabled.
		PJ4		General purpose input/output port.
95	125	SCK1	U	UART1 clock input/output pin. The pin has this function when UART1 clock output is enabled.
		PJ5		General purpose input/output port.
96	126	PPG0	U	PPG timer output. This pin has this function when PPG0 output is enabled.
		PJ6		General purpose input/output port.

(Continued)

Pin no.		Pin name	I/O circuit type	Function
MB91302A	MB91V301A			
97	127	TRG0	U	External trigger input for PPG timer. This input is used continuously when the corresponding timer input is enabled. In this case, do not output to this port unless doing so intentionally.
		PJ7		General purpose input/output port.
98	128	TIN0	J	Reload timer input. This input is used continuously when the corresponding timer input is enabled. In this case, do not output to this port unless doing so intentionally.
		PH0		General purpose input/output port.
99	129	TIN1	J	Reload timer input. This input is used continuously when the corresponding timer input is enabled. In this case, do not output to this port unless doing so intentionally.
		PPG3		PPG timer output. The pin has this function when PPG3 output is enabled.
		PH1		General purpose input/output port.
100	130	TIN2	J	Reload timer input. This input is used continuously when the corresponding timer input is enabled. In this case, do not output to this port unless doing so intentionally.
		TRG3		External trigger input for PPG timer. This input is used continuously when the corresponding timer input is enabled. In this case, do not output to this port unless doing so intentionally.
		PH2		General purpose input/output port.
103	133	DREQ0	J	External input for DMA transfer requests. This input is used continuously when selected as a DMA activation trigger. In this case, do not output to this port unless doing so intentionally.
		PB0		General purpose input/output port.
104	134	DACK0	J	External acknowledge output for DMA transfer requests. The pin has this function when outputting DMA transfer request acknowledgement is enabled.
		PB1		General purpose input/output port.
105	135	DEOP0	J	Completion output for DMA external transfer. The pin has this function when outputting DMA transfer completion is enabled.
		PB2		General purpose input/output port.

(Continued)

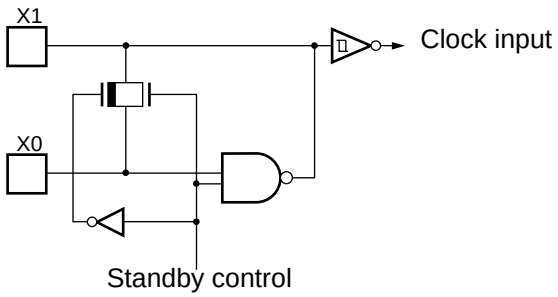
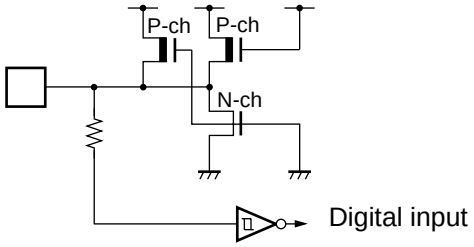
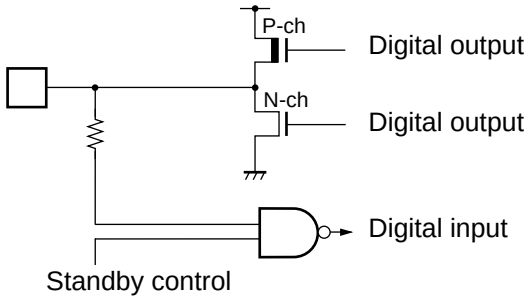
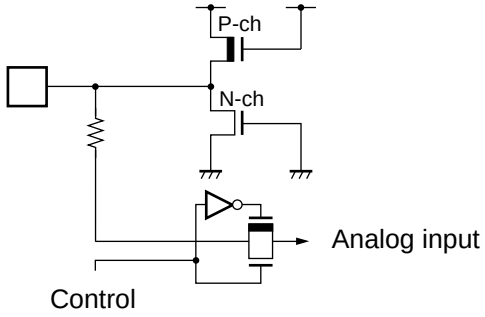
Pin no.		Pin name	I/O circuit type	Function
MB91302A	MB91V301A			
106	136	DREQ1	J	DMA External input for DMA transfer requests. This input is used continuously when selected as a DMA activation trigger. In this case, do not output to this port unless doing so intentionally.
		PB3		General purpose input/output port. The pin has this function when completion output and stop input are disabled for DMA transfer.
107	137	DACK1	J	External acknowledge output for DMA transfer requests. The pin has this function when outputting DMA transfer request acknowledgement is enabled.
		TRG1		External trigger input for PPG timer. This input is used continuously when the corresponding timer input is enabled. In this case, do not output to this port unless doing so intentionally.
		PB4		General purpose input/output port.
108	138	DEOP1	J	Completion output for DMA external transfer. The pin has this function when outputting DMA transfer completion is enabled.
		PPG1		PPG timer output. The pin has this function when PPG1 bit is enabled.
		PB5		General purpose input/output port.
109	139	$\overline{\text{IOWR}}$	J	Write strobe output for DMA fly-by transfer. The pin has this function when outputting a write strobe for DMA fly-by transfer is enabled.
		PB6		General purpose input/output port. The pin has this function when outputting a write strobe for DMA fly-by transfer is disabled.
110	140	$\overline{\text{IORD}}$	J	Read strobe output for DMA fly-by transfer. The pin has this function when outputting a read strobe for DMA fly-by transfer is disabled.
		PB7		General purpose input/output port. The pin has this function when outputting a write strobe for DMA fly-by transfer is disabled.
112	143	X0	A	Clock (oscillation) input.
113	144	X1	A	Clock (oscillation) output.
116 to 118	147 to 149	MD0 to MD2	G	Mode pins 0 to 2. The levels applied to these pins set the basic operating mode. Connect V_{CC} or V_{SS}.
119	152	$\overline{\text{INIT}}$	B	External reset input (Reset to initialize settings) (“L” active)
120	053	$\overline{\text{NMI}}$	M	NMI (Non Maskable Interrupt) input (“L” active)

(Continued)

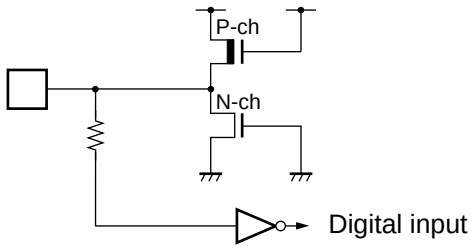
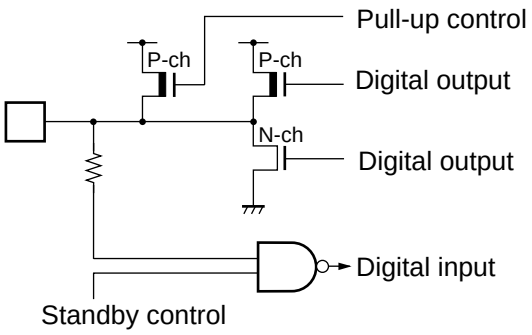
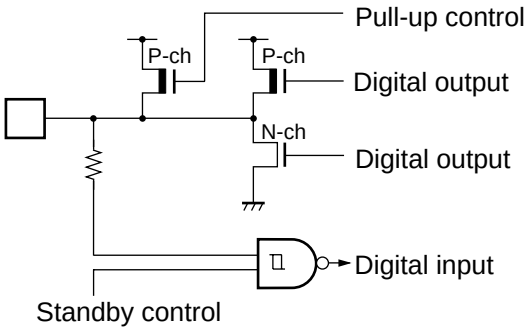
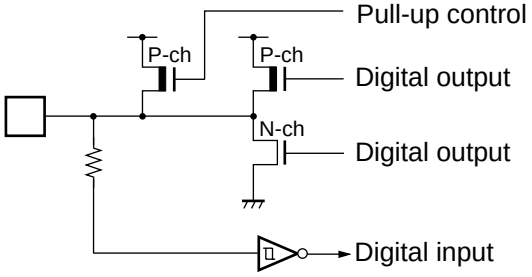
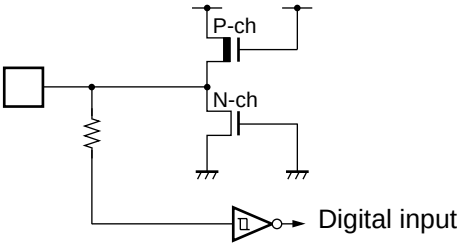
(Continued)

Pin no.		Pin name	I/O circuit type	Function
MB91302A	MB91V301A			
122	156	$\overline{CS0}$	J	Chip select 0 output. The pin has this function when chip select 0 output is enabled.
		PA0		General purpose input/output port. The pin has this function when chip select 0 output is disabled.
123	157	$\overline{CS1}$	J	Chip select 1 output. The pin has this function when chip select 1 output is enabled.
		PA1		General purpose input/output port. The pin has this function when chip select 1 output is disabled.
124	158	$\overline{CS2}$	J	Chip select 2 output. The pin has this function when chip select 2 output are enabled.
		PA2		General purpose input/output port. The pin has this function when chip select 2 output is disabled.
125	159	$\overline{CS3}$	J	Chip select 3 output. The pin has this function when chip select 3 output are enabled.
		PA3		General purpose input/output port. The pin has this function when chip select 3 output is disabled.
126	160	$\overline{CS4}$	J	Chip select 4 output. The pin has this function when chip select 4 output is enabled.
		TRG2		External trigger input for PPG timer. This input is used continuously when the corresponding timer input is enabled. In this case, do not output to this port unless doing so intentionally.
		PA4		General purpose input/output port. The pin has this function when chip select 4 output is disabled.
127	161	$\overline{CS5}$	J	Chip select 5 output. The pin has this function when chip select 5 output are enabled.
		PPG2		PPG timer output. The pin has this function when PPG2 bit is enabled.
		PA5		General purpose input/output port. The pin has this function when chip select 5 output and PPG timer output are disabled.
128	162	$\overline{CS6}$	J	Chip select 6 output. The pin has this function when chip select 6 output is enabled.
		$\overline{PA6}$		General purpose input/output port. The pin has this function when chip select 6 output are disabled.
129	163	$\overline{CS7}$	J	Chip select 7 output. The pin has this function when chip select 7 output are enabled.
		PA7		General purpose input/output port. The pin has this function when chip select 7 output is disabled.

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		• Oscillation feedback resistance approx. 1 MΩ
B		• CMOS hysteresis input with pull-up resistor
C		• CMOS level I/O with standby control • I_{OL} = 4 mA
D		• Analog input With switch

(Continued)

Type	Circuit	Remarks
G		• CMOS level output No standby control
J		• With Pull-up control • CMOS level I/O with standby control • With Pull-up control • I_{OL} = 4 mA
K		• With Pull-up control • CMOS level output CMOS level hysteresis input with standby control • I_{OL} = 4 mA
L		• With Pull-up control • CMOS level output CMOS level hysteresis input no standby control • I_{OL} = 4 mA
M		• CMOS level hysteresis input no standby control

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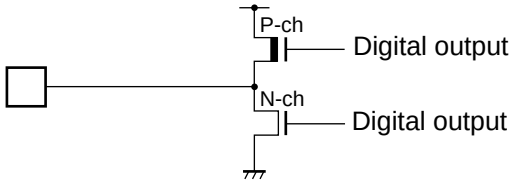
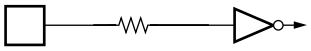
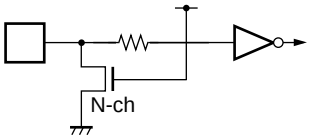
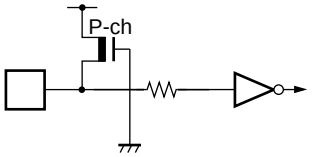
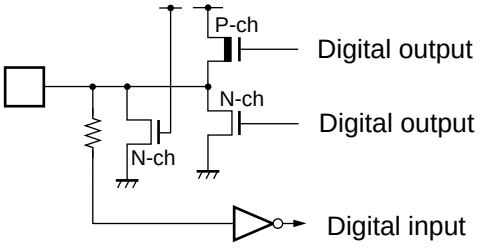
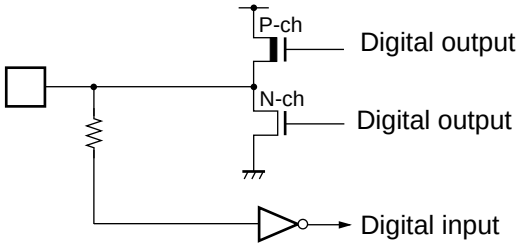
Type	Circuit	Remarks
N		• Output buffer • CMOS level output • I_{OL} = 4 mA
O		• Input buffer • CMOS level input
P		• Input buffer with pull-down • Pull-down resistor value = 25 kΩ approx. (Typ)
Q		• Input buffer with Pull-up
R		• I/O buffer with pull-down • CMOS level output • I_{OL} = 4 mA
S		• I/O buffer • CMOS level output • I_{OL} = 4 mA

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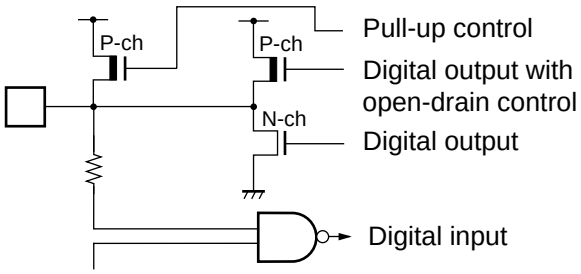
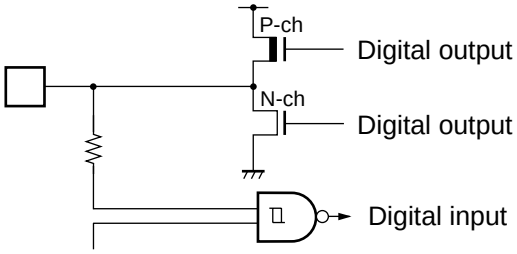
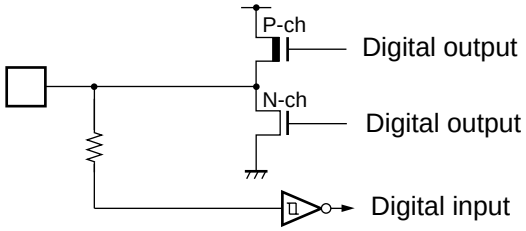
Type	Circuit	Remarks
T		• N-ch open-drain output • CMOS level I/O with standby control • Without pull-up control • I_{OL} = 4 mA
U		• CMOS level output • CMOS level hysteresis input with standby control • 5 V tolerant • I_{OL} = 4 mA
V		• CMOS level output • CMOS level hysteresis input with standby control • 5 V tolerant • I_{OL} = 4 mA

■ HANDLING DEVICES

❍MB91301 series

- **Operation at start-up**

  Always apply a settings initialization (INIT) to the $\overline{\text{INIT}}$ pin immediately after turning on the power.
  Also, in order to provide a delay while the oscillator circuits stabilize immediately after start-up, maintain the “L” level input to the $\overline{\text{INIT}}$ pin for the required stabilization delay time. (The initialization processing (INIT) triggered by the $\overline{\text{INIT}}$ pin initializes the oscillation stabilization delay time to the minimum setting.)

- **External clock input at start-up**

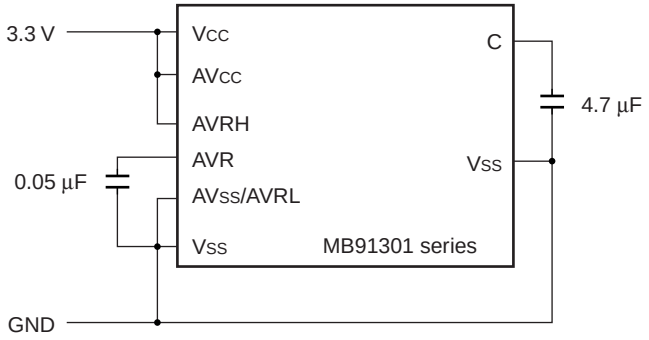
  At power-on start-up, always input a clock signal until the oscillation stabilization delay time is ended.

- **Output indeterminate at power-on time**

  When the power is turned on, the output pin may remain indeterminate until the internal power supply becomes stable.

- **Built-in DC/DC regulator**

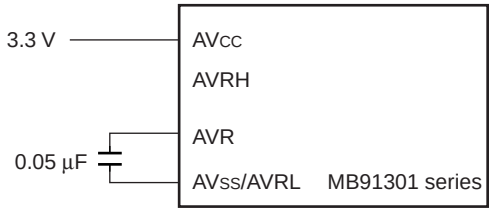
  This device has a built-in regulator, requiring 3.3 V input to the Vcc pin and a bypass capacitor of approximately 4.7 µF connected to the C pin for the regulator.



Note of built-in DC/DC regulator

- **Note on use of the A/D converter**

  As the MB91301 series contains an A/D converter, be sure to supply power to AVcc at 3.3 V and insert a capacitor of at least 0.05 µF between the AVR pin and the AVss/AVRL pin.



Note on Use of A/D Converter

- **Preventing Latchup**

  When CMOS integrated circuit devices are subjected to applied voltages higher than V_{CC} at input and output pins, or to voltages lower than V_{SS}, as well as when voltages in excess of rated levels are applied between V_{CC} and V_{SS}, a phenomenon known as latchup can occur. When a latchup condition occurs, the supply current can increase dramatically and may destroy semiconductor elements. In using semiconductor devices, always take sufficient care to avoid exceeding maximum ratings.

- **Power supply pins**

  Devices with multiple V_{CC} and V_{SS} supply pins are designed to prevent problems such as latchup occurring by providing internal connections between pins at the same potential. However, in order to reduce unwanted radiation, prevent abnormal operation of strobe signals due to a rise in ground level, and to maintain the total output current ratings, all such pins should always be connected externally to power supply or ground. Also, ensure that the impedance of the V_{CC} and V_{SS} connections to the power supply are as low as possible.
  In addition, it is recommended that a bypass capacitor of approximately 0.1µF be connected between V_{CC} and V_{SS}. Connect the capacitor close to the V_{CC} and V_{SS} pins.

- **Crystal oscillators**

  Noise in proximity to the X0 and X1 pins can cause abnormal operation in this device. Printed circuit boards should be designed so that the X0 and X1 pins, crystal (or ceramic) oscillator, and bypass capacitor connected to ground are placed as close together as possible.
  Also, to ensure stable operation, it is strongly recommended that the printed circuit board art work be designed such that the X0 and X1 pins are surrounded by ground.
  Please ask the crystal maker to evaluate the oscillational characteristics of the crystal and this device.

- **Treatment of NC and OPEN pins**

  Pins marked as "NC" or "OPEN" must be left open-circuit.

- **Treatment of unused input pins**

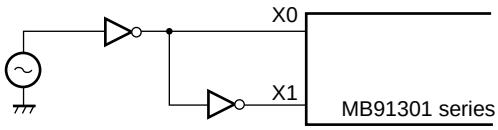
  If unused input pins are left open, abnormal operation may result. Any unused input pins should be connected to pull-up or pull-down resistors.

- **Mode pins (MD0 to MD2)**

  These pins should be connected directly to V_{CC} or V_{SS}. To prevent the device erroneously switching to test mode due to noise, design the printed circuit board such that the distance between the mode pins and V_{CC} or V_{SS} is as short as possible and the connection impedance is low.

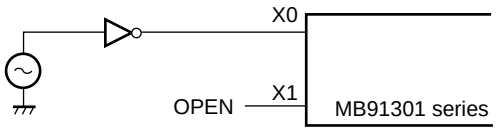
- **Remarks for External Clock Operation**

  When external clock is selected, supply it to X0 pin generally, and simultaneously the opposite phase clock to X0 must be supplied to X1 pin. However, in this case the stop mode must not be used (because X1 pin stops at “H” output in stop mode) .
  When operating at 12.5 MHz or less, the microcontroller can be used with the clock signal supplied only to pin X0.
  “Using an external clock (normal) and (12.5 MHz) ” shows examples of how the MB91301 uses the external clock.



Note: Stop mode (oscillation stop mode) can not be used.

Using an external clock (normal)



Using an external clock (12.5 MHz Max)

- **Notes on during operation of PLL clock mode**

  If the PLL clock mode is selected, the microcontroller attempt to be working with the self-oscillating circuit even when there is no external oscillator or external clock input is stopped. Performance of this operation, however, cannot be guaranteed.

- **Clock control block**

  For L-level input to the $\overline{\text{INIT}}$ pin, allow for the regulator settling time or oscillation settling time.

- **Bit search module**

  The 0-detection, 1-detection, and transition-detection data registers (BSD0, BSD1, and BSDC) are only word-accessible.

- **I/O port access**

  Byte access only for access to port

- **Shared port function switching**

  To switch a pin that also serves as a port, use the port function register (PFR). Note, however, that bus pins are switched depending on external bus settings.

- **D-bus memory**

  Do not set a code area in D-bus memory.
  No instruction fetch is performed to the D-bus.
  Instruction fetches to the D-bus area result in incorrect data interpreted as code, which can cause the micro-controller to lose control.
  Do not set a data area in I-bus memory.

- **I-bus memory**

  Do not set a stack area or vector table in I-bus memory.

  It may cause a hang during EIT processing (including RETI).

  Recovery from the hang requires a reset.

  Do not perform DMA transfer to I-bus memory.

- **Low-power consumption modes**
  - To enter the standby mode, use the synchronous standby mode (set with the SYNCS bit as bit 8 in the TBCR, or time-base counter control register) and be sure to use the following sequence:

```
(LDI    #value_of_standby, R0)
(LDI    #_STCR, R12)
STB     R0, @R12            ; Write to standby control register (STCR)
LDUB    @R12, R0            ; Read STCR for synchronous standby
LDUB    @R12, R0            ; Read STCR again for dummy read
NOP                         ; NOP x 5 for timing adjustment
NOP
NOP
NOP
NOP
```

  - If you use the monitor debugger, follow the precautions below:

    Do not set a breakpoint within the above array of instructions.
    Do not single-step the above array of instructions.

- **Prefetch**

  When accessing a prefetch-enabled little endian area, use word access only (access in 32 bits).
  Byte or halfword access results in wrong data read.

- **MCLK and SYSCLK**

  MCLK causes a stop in SLEEP/STOP mode while SYSCLK causes a stop only in STOP mode. Use either depending on each application.

- **Pull-up control**

  When function pins listed in the AC specifications (such as external bus control pins) have pull-up control, enabling the pull-up resistor for a pin causes the actual pin load conditions to change. As all AC specifications for this device were measured under the condition of pull-up resistors disabled, the values are not guaranteed of AC specifications when pull-up resistors are enabled.

  Even if the pull-up resistor is set to enabled for a pin, if the HIZ bit in the standby control register (STCR) specifies setting output pins to high impedance during stop mode (HIZ = 1) , changing to stop mode (STOP = 1) causes the pull-up resistor to be disabled.

- **R15 (General purpose register)**

  When any of the following instructions is executed, the SSP* or USP* value is not used as R15, resulting in an incorrect value written to memory.

AND	R15, @Ri	ANDH	R15, @Ri	ANDB	R15, @Ri
OR	R15, @Ri	ORH	R15, @Ri	ORB	R15, @Ri
EOR	R15, @Ri	EORH	R15, @Ri	EORB	R15, @Ri
XCHB	@Rj, R15				

  * : R15 is a virtual register. When a program attempts to access R15, the SSP or USP is accessed depending on the status of the “S” flag as an SP flag. When coding the above ten instructions using an assembler, specify a general-purpose register other than R15.

- **RETI instruction**

  Please do not neither control register of the instruction cache nor the data access to RAM of the instruction cache immediately before the instruction of RETI.

- **Notes on the PS register**

  Since some instructions manipulate the PS register earlier, the following exceptions may cause the interrupt handler to break or the PS flag to update its display setting when the debugger is being used. As the microcontroller is designed to carry out reprocessing correctly upon returning from such an EIT event, it performs operations before and after the EIT as specified in either case.

  - The following operations may be performed when the instruction immediately followed by a DIVOU/DIVOS instruction is (a) halted by a user interrupt or NMI, (b) single-stepped, or (c) breaks in response to a data event or emulator menu:
    (1) D0 and D1 flags are updated earlier.
    (2) The EIT handler (user interrupt/NMI or emulator) is executed.
    (3) Upon returning from the EIT, the DIVOU/DIVOS instruction is executed and the D0 and D1 flags are updated to the same values as those in (1) above.
  - The following operations are performed when the ORCCR/STILM/MOV Ri and PS instructions are executed to enable interruptions when a user interrupt or NMI trigger event has occurred.
    (1) The PS register is updated earlier.
    (2) The EIT handler (user interrupt/NMI or emulator) is executed.
    (3) Upon returning from the EIT, the above instructions are executed and the PS register is updated to the same value as that in (1) above.

- **A/D converter**

  When the device is turned on or returns from a reset or stop, it takes time for the external capacitor to be charged, requiring the A/D converter to wait for at least 10 ms.

- **Watchdog timer**

  The watchdog timer function of this model monitors that a program delays a reset within a certain period of time and resets the CPU if the program fails to delay it, for example, because the program runs out of control. Once the watchdog timer function is enabled, therefore, the watchdog timer continues to operate until a reset takes place.

  An exception, for example during stop, sleep and DMA transfer modes, is the automatic delaying of a reset under a condition in which the CPU stops program execution.

  Note, however, that a watchdog reset may not occur in the above state caused when the system runs out of control. If this is the case, use the external $\overline{\text{INIT}}$ pin to cause a reset (INIT) .

❍Unique to the evaluation chip MB91V301A

- **Tool reset**

  On an evaluation board, use the chip with $\overline{\text{INIT}}$ and $\overline{\text{TRST}}$ connected together.

- **Simultaneous occurrences of a software break and a user interrupt/NMI**

  When a software break and a user interrupt /NMI take place at the same time, the emulator debugger can cause the following phenomena:
  - The debugger stops pointing to a location other than the programmed breakpoints.
  - The halted program is not re-executed correctly.

  If these phenomena occur, use a hardware break instead of the software break. If the monitor debugger has been used, avoid setting any break at the relevant location.

- **Single-stepping the RETI instruction**

  If an interrupt occurs frequently during single stepping, execute only the relevant processing routine repeatedly after single-stepping RETI. This will prevent the main routine and low-interrupt-level programs from being executed. Do not single-step the RETI instruction for avoidance purposes. When the debugging of the relevant interrupt routine becomes unnecessary, perform debugging with that interrupt disabled.

- **Operand break**

  A stack pointer placed in an area set for a DSU operand break can cause a malfunction. Do not apply a data event break to access to the area containing the address of a system stack pointer.

- **ICE startup sequence**

  When using the ICE, when you start debugging, ensure that the bus configuration is set correctly for the area being used before downloading. After turning on the power to the target, the states of the $\overline{\text{RD}}$ and $\overline{\text{WR0}}$ to $\overline{\text{WR3}}$ pins are undefined until you perform the above setting. Accordingly, include enabling pull-up as part of the startup sequence. If using these pins as general-purpose ports, set as output ports to prevent conflict with the output signals during the time the pin states are undefined.

External bus width / Pin name	32 bit	16 bit	8 bit
$\overline{\text{RD}}$	Pull-up	Pull-up	Pull-up
$\overline{\text{WR0}}$	Pull-up	Pull-up	Pull-up
$\overline{\text{WR1}}$ (P85)	Pull-up	Pull-up	*
$\overline{\text{WR2}}$ (P86)	Pull-up	*	*
$\overline{\text{WR3}}$ (P87)	Pull-up	*	*

* : Use as output ports.

- **Configuration batch file**

  The example batch file below sets the mode vector and sets up the CS0 configuration register for the download area. Use values appropriate to the hardware in the wait, timing, and other settings.

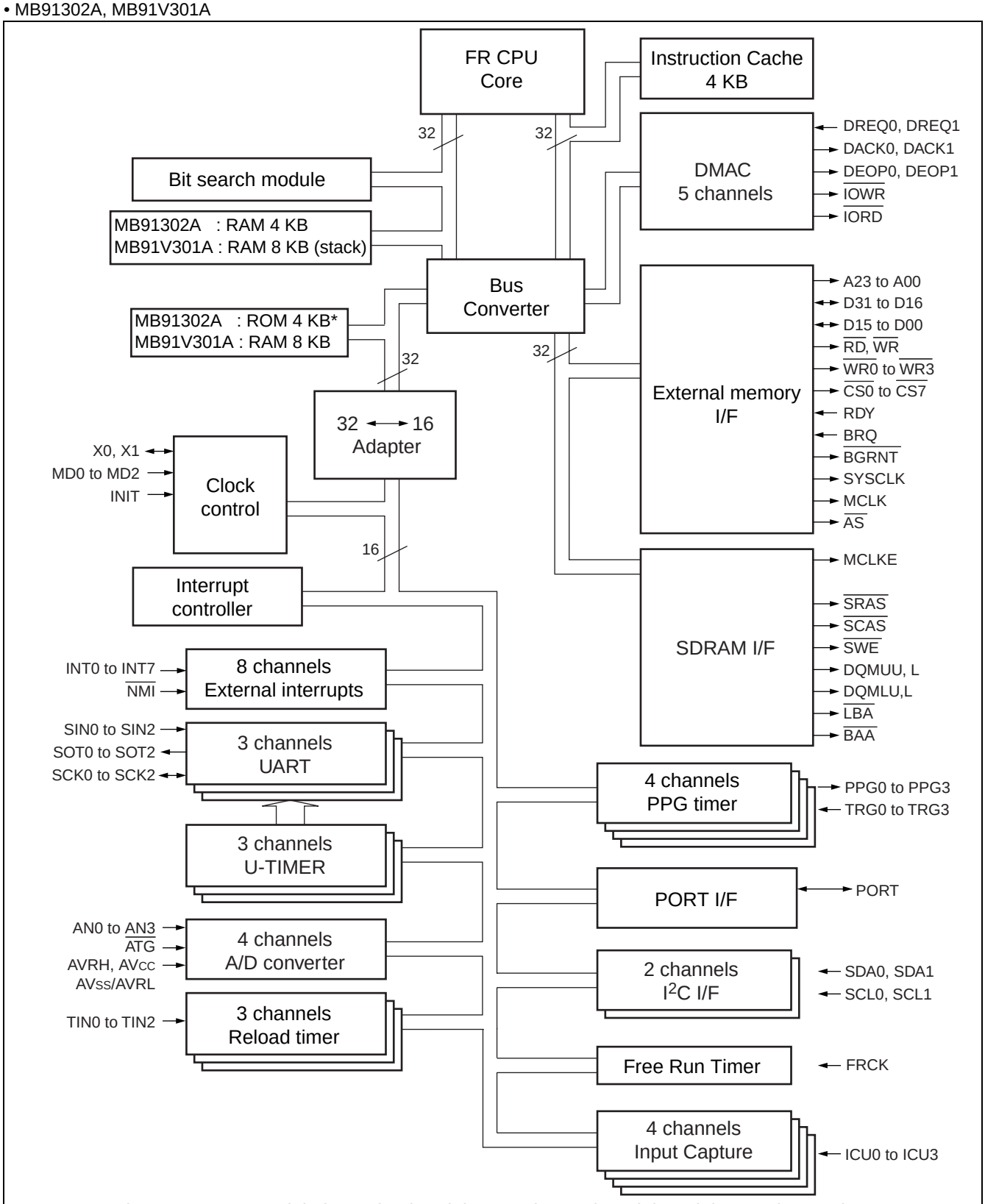
```
#-----------------------------------------------------------
# Set MODR (0x7fd) =Enable In memory+16 bit External Bus
set mem/byte 0x7fd=0x5
#-----------------------------------------------------------
# Set ASR0 (0x640) ; 0x0010_0000 - 0x002f_ffff
set mem/halfword 0x640=0x0010
#-----------------------------------------------------------
# Set ACR0 (0x642)
#                       ; ASZ [3:0]=0101:2 Mbytes
#                       ; DBW [1:0]=01:16 bit width, automatically set from
MODR
#                       ; BST [1:0]=00:1 burst (16 bit x 2)
#                       ; SREN=0:Disable BRQ
#                       ; PFEN=1:Enable Pre fetch buffer
#                       ; WREN=1:Enable Write operation
#                       ; LEND=0: Big endian
#                       ; TYPE [3:0]=0010:WEX: Disable RDY
set mem/harfword 0x642=0x5462
#-----------------------------------------------------------
# Set AWR0 (0x660)
#                       ; W15-12=0010:auto wait=2
#                       ; WR07, 06=01:RD, WR delay=1cycle
#                       ; W05, 04=01:WR->WR delay=1cycle (for WEX)
#                       ; W03  =1:MCLK->RD/WR delay=0.5cycle
#                       ;             :for async Memory
#                       ; W02  =0:ADR->CS delay=0
#                       ; W01  =0:ADR->RD/WR setup 0cycle
#                       ; W00  =RD/WR->ADR hold 0cycle
set mem/halfword 0x660=0x2058
#-----------------------------------------------------------
```

- **Emulation memory**

  If SRAM as the emulation memory is built on target board, SRAM for be accessed by RD, WR signal, and +BYTE control signal can not be used. (The external bus is initialized to the bus mode for accessing $\overline{RD}$, $\overline{WRn}$ after reset.)

■ BLOCK DIAGRAM

• MB91302A, MB91V301A



* : ROM has non-ROM model, the optimal real time OS internal model, and the IPL (Internal Program Loader) internal model by adding the user ROM model.

■ CPU

1. Memory Space

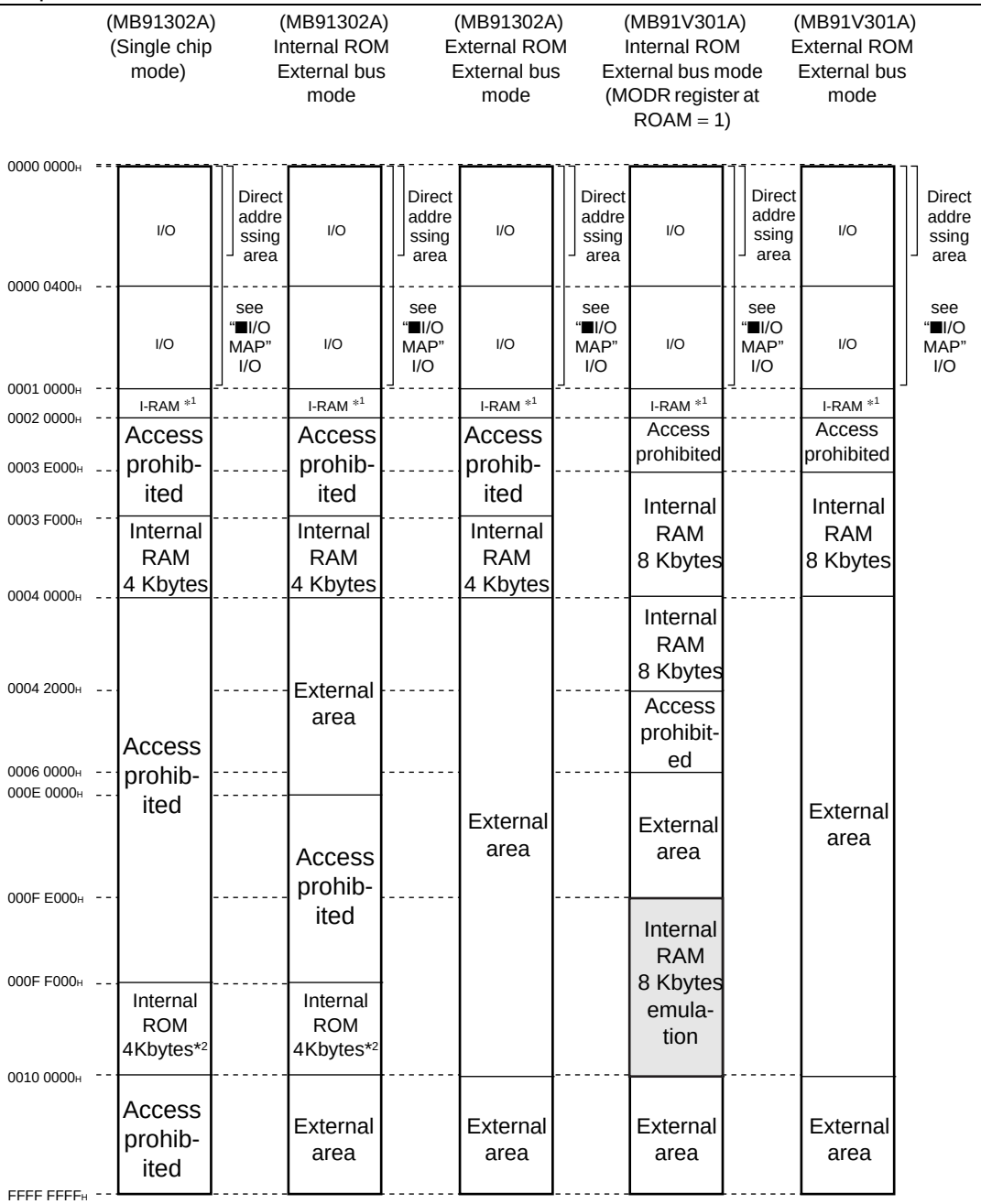
The FR family has 4 Gbytes (2^{32} addresses) of logical address space with linear access from the CPU.

• Direct Addressing Areas

The following areas of address space are used for I/O operations.
These areas are called direct addressing areas, in which the address of an operand can be specified directly during an instruction.
The direct areas differ according to the size of the data accessed, as follows.

→ byte data access : 000_H to $0FF_H$
→ half word data access : 000_H to $1FF_H$
→ word data access : 000_H to $3FF_H$

• Memory map



MB91302A has non-ROM model, the optimal real time OS internal model, and the IPL (Internal program Loader) internal model by adding the user ROM model.

*1 : On specific area between 10000_H and 2000_H, 4 Kbytes RAM can be used.
Refer to "■INSTRUCTION CACHE".

*2 : The real time OS internal model stores the real time OS kernel. The program loader internal model stores the program loader.

Note : Internal ROM emulation : only MB91V301A

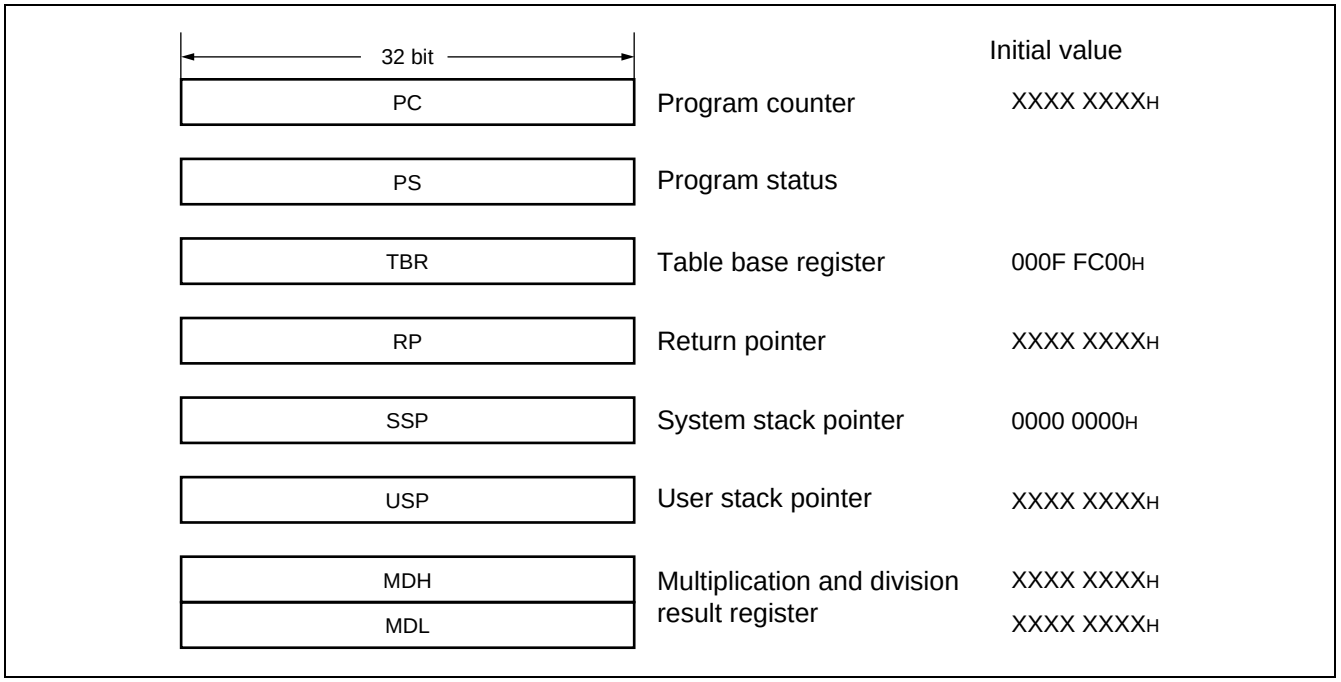
Note : Each mode is set depending on the mode vector fetch after $\overline{INIT}$ is negated. (For mode setting, see "■MODE SETTINGS".)

2. Registers

The FR series has two types of registers: application-specific registers in the CPU and general purpose registers in memory.

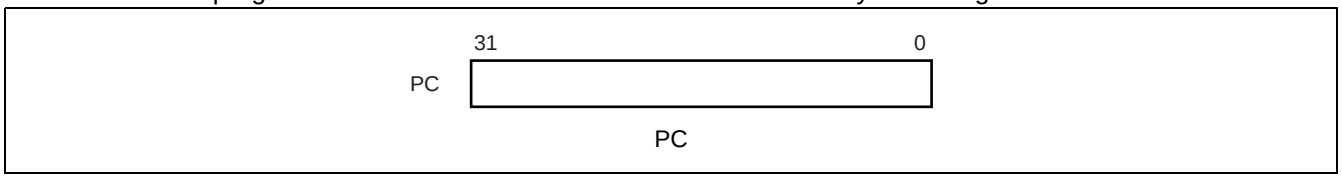
• Dedicated registers

Program counter (PC)	:	32-bit register. Stores the current instruction address.
Program status (PS)	:	32-bit register. Contains the register pointer and condition code.
Table base register (TBR)	:	Stores the top address of the vector table used by the EIT (exception/interrupt/ trap) function.
Return pointer (RP)	:	Stores the subroutine return address.
System stack pointer (SSP)	:	Points to the system stack area.
User stack pointer (USP)	:	Points to the user stack area.
Multiplication and division result register (MDH/MDL)	:	32-bit registers used for multiplication and division.



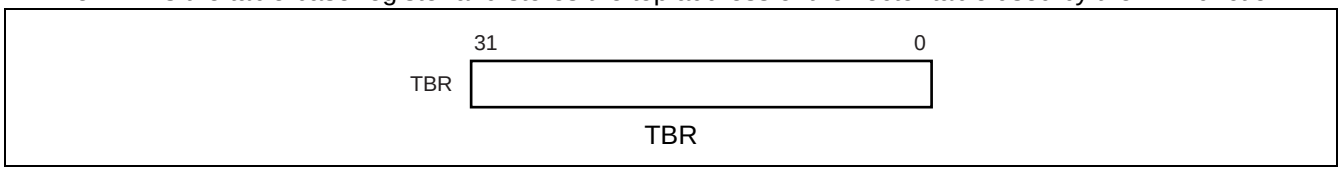
• PC (Program Counter)

The PC is the program counter and stores the address of the currently executing instruction.



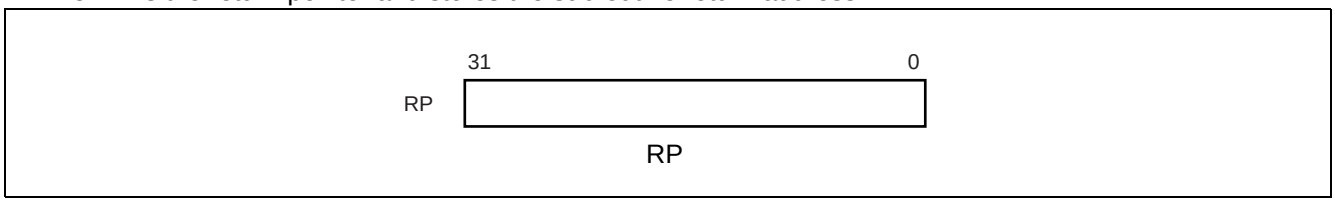
• Table base register (TBR)

The TBR is the table base register and stores the top address of the vector table used by the EIT function.



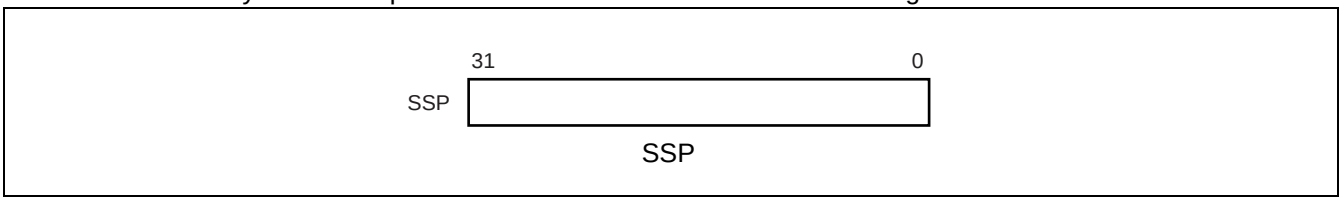
• Return pointer (RP)

The RP is the return pointer and stores the subroutine return address.



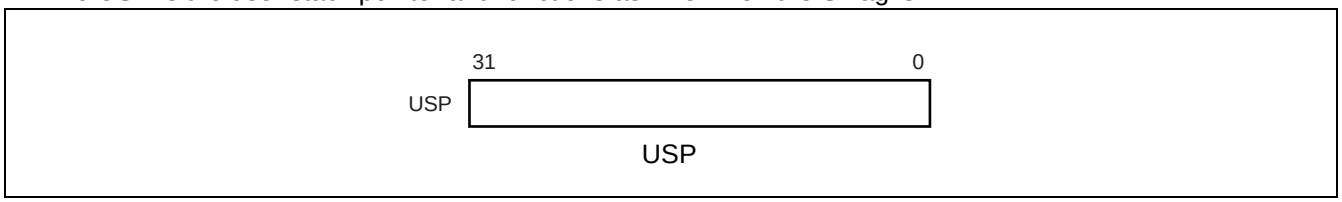
• System stack pointer (SSP)

The SSP is the system stack pointer and functions as R15 when the S flag is “0”.



• User stack pointer (USP)

The USP is the user stack pointer and functions as R15 when the S flag is “1”.

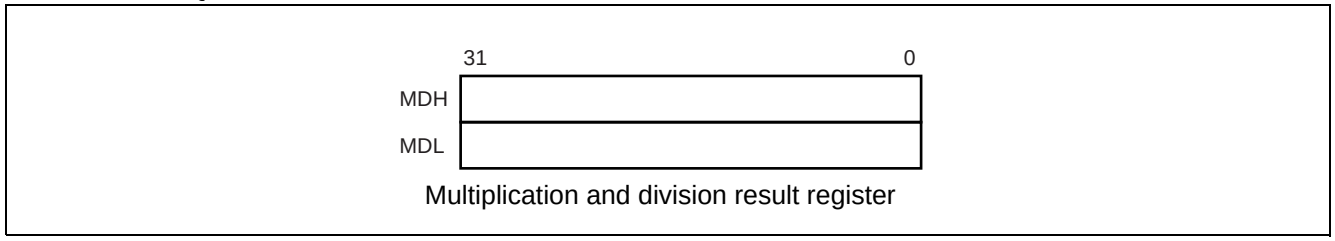


• Multiplication and division result register (MDH/MDL)

MDH/MDL : 32-bit registers used for multiplication and division.

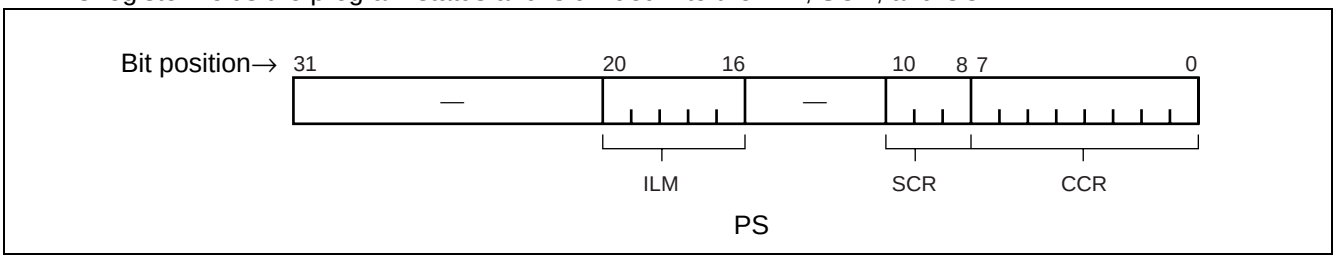
MDH : Remainder

MDL : Quotient



• Program status (PS)

This register holds the program status and is divided into the ILM, SCR, and CCR.



• Condition code register (CCR)

S flag : Specifies which stack pointer to use as R15.

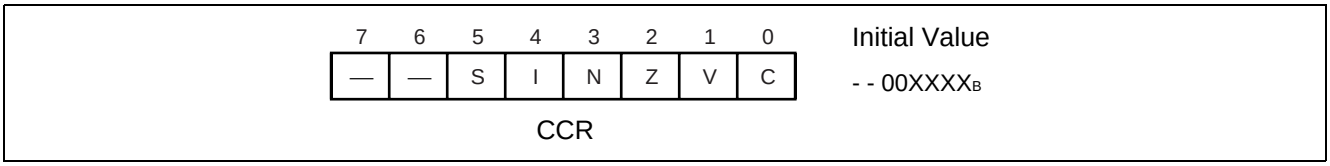
I flag : Enables or disables user interrupt requests.

N flag : Indicates the sign when an operation result is represented as a “2” complement integer.

Z flag : Indicates whether an operation result is “0”.

V flag : Indicates whether an overflow occurred for an operation result when the operation operand is represented as a “2” complement integer.

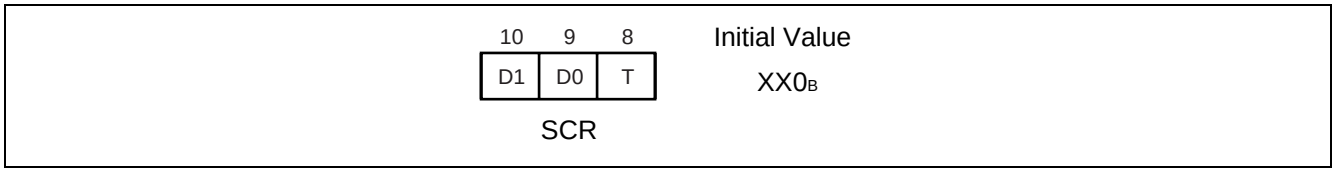
C flag : Indicates whether an operation resulted in a borrow or a carry from the most significant bit.



• System condition code register (SCR)

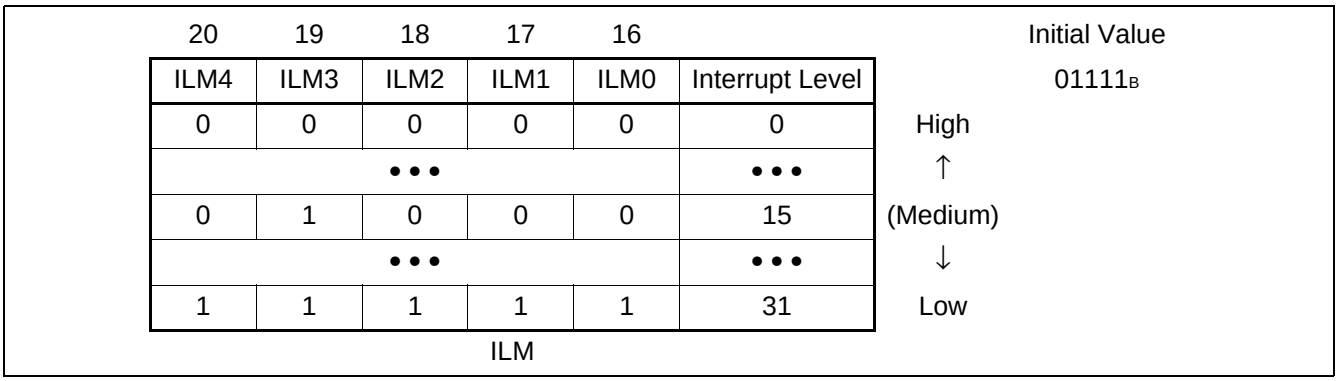
D1, D0 flags : Stores intermediate data for stepwise multiplication operations.

T flags : A flag specifying whether the step trace trap function is enabled or not.



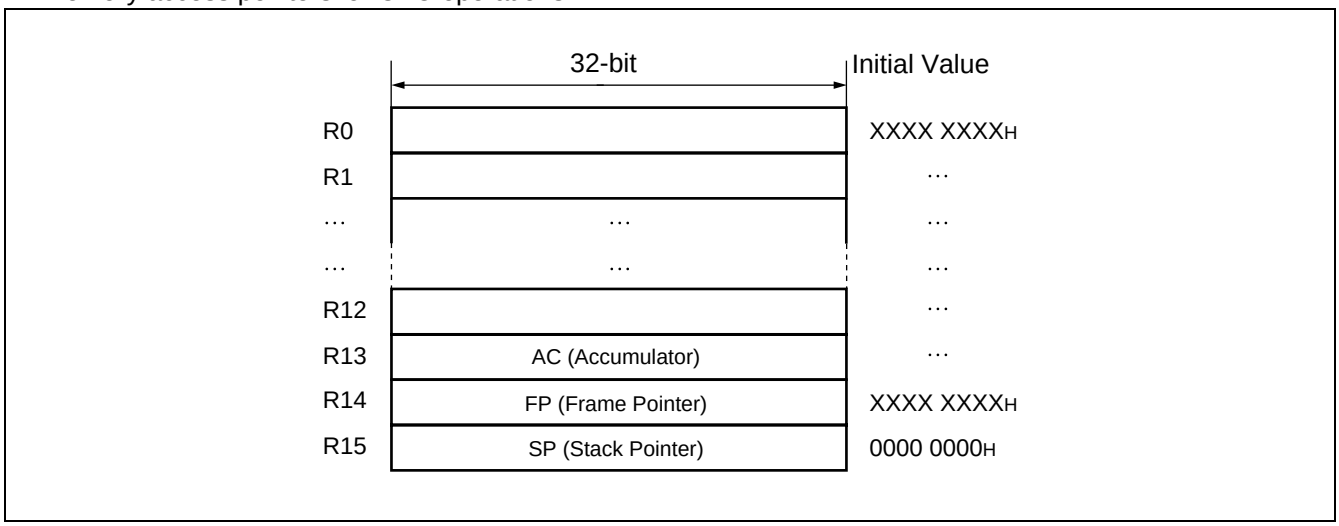
• Interrupt level mask register(ILM)

ILM4 to ILM0 : This register stores the interrupt level mask value. The value in the ILM register is used as the level mask. Only interrupt requests to the CPU that have an interrupt level that is higher than the level specified in ILM are accepted.



■ GENERAL PURPOSE REGISTERS

General purpose registers R0 to R15 are used by the CPU. The registers are used as the accumulator and memory access pointers for CPU operations.



The following three registers are treated as having special meanings to enhance the operation of some instructions.

R13 : Virtual accumulator (AC)

R14 : Frame pointer (FP)

R15 : Stack pointer (SP)

The values of R0 to R14 after a reset are undefined. R15 is initialized to 0000 0000H (SSP value) .

■ MODE SETTINGS

In the FR series, the mode is set by the mode pins (MD2, MD1, and MD0) and mode register (MODR).

1. Mode Pins

The MD2, MD1, and MD0 pins specify how the mode vector fetch is performed.

Mode Pins			Mode name	Reset vector access area	Remarks
MD2	MD1	MD0			
0	0	0	Internal ROM vector mode	Internal	Single-chip mode*
0	0	1	External ROM vector mode	External	The bus width is specified by the mode register.

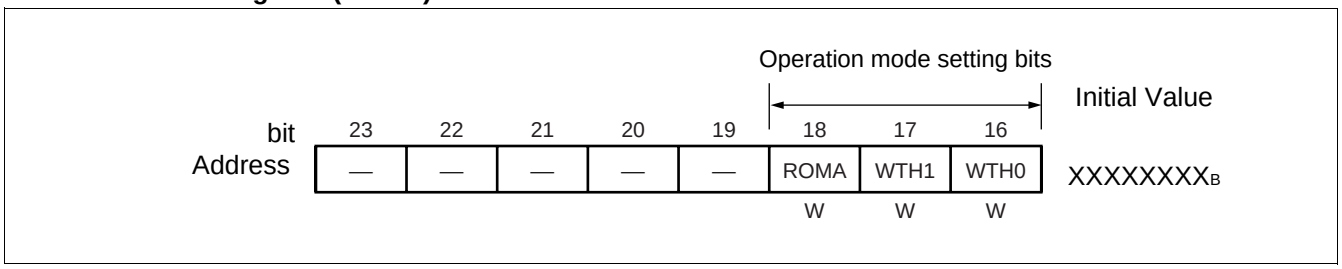
Values other than those listed in the table are prohibited.

* : Single chip mode is able to set only MB91302A.

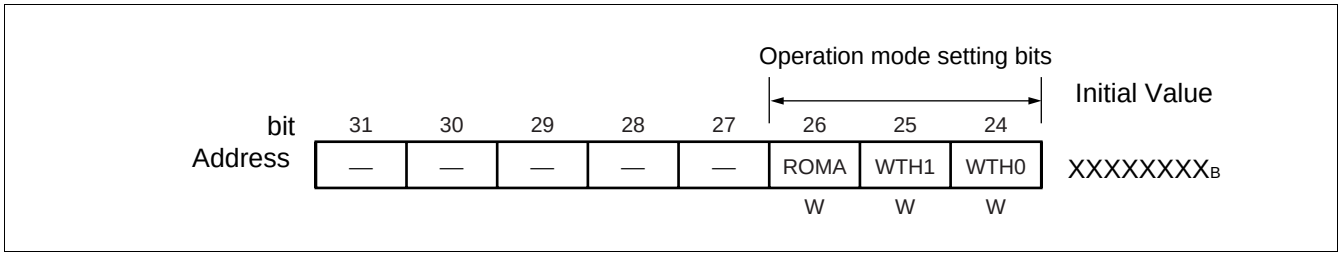
2. Mode Register (MODR)

- Details of mode register (MODR)
  The data written to the mode register by the mode vector fetch operation (see “3.11.3 reset sequences”) is called the mode data.
  After the data is set to the mode register (MODR), the device operates with the operating mode specified by this data. The mode register is set by all types of reset. The register cannot be written to by user programs.

<Details of mode register (MODR) >

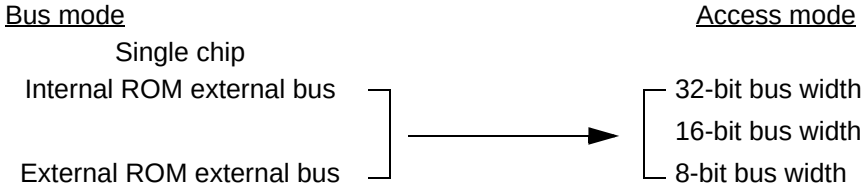


<Details of mode data>



Bit31 to bit24 are all reserved bits.
Be sure to set this bit to “00000.”
Operation is not guaranteed when any value other than “00000.” is set.

- Operating mode



- Bus mode
  The bus mode controls the operations of internal ROM and the external access function. It is specified with the mode setting pins (MD2, MD1, and MD0) and the ROMA bit in mode data.

- Access mode
  The access mode controls the external data bus width. It is specified with the WTH1 and WTH0 bits in the mode register and the DBW1 and DBW0 bits in area configuration registers 0 to 7 (ACR0 to ACR7).

- Bus Modes
  The FR family has three bus modes: bus mode 0 (single-chip mode), bus mode 1 (internal-ROM, external-bus mode), and bus mode 2 (external-ROM, external-bus mode).
  The MB91V301A supports only bus mode 2 (external-ROM, external-bus mode).
  See “1. Memory Space” in ■CPU for details.

- Bus mode0 (single chip mode) (only MB91302A)
  The internal I/O, 4 Kbytes D-bus RAM, 32 Kbytes F-bus RAM (FRAM) and 96 Kbytes F-bus ROM are valid, while access to any other areas is invalid under this mode. The function of external pin is peripheral or general-purpose port. The pin can not be used as the bus pin.

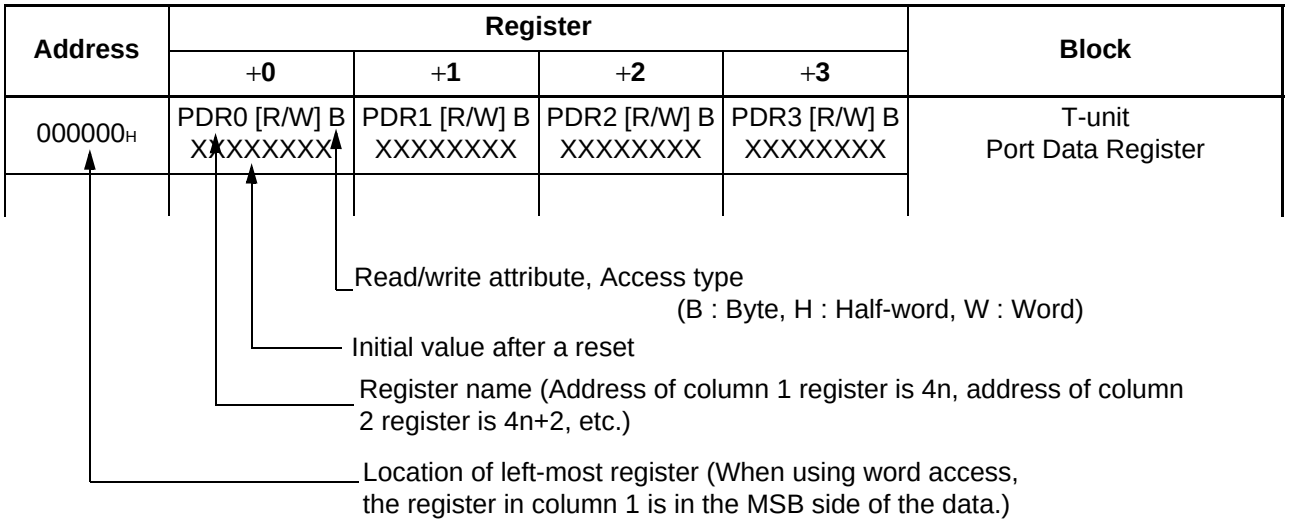
- Bus mode 1 (internal ROM external bus mode)
  The internal I/O, D-bus RAM, F-bus RAM (FRAM) and F-bus ROM are valid, and access to areas where external access is enabled will access external space under this mode. A part of an external terminal functions as a bus terminal.

- Bus mode 2 (External-ROM, external-bus mode)
  This mode enables internal I/O and D-bus RAM, in which any access is access to external space. Some external pins serve as bus pins.

■ I/O MAP

This shows the location of the various peripheral resource registers in the memory space.

[How to read the table]



Note : Initial values of register bits are represented as follows :

“1” : Initial value“1”

“0” : Initial value“0”

“X” : Initial value“X”

“-” : No physical register at this location

Address	Register				Block
	+0	+1	+2	+3	
000000H	PDR0 [R/W] B XXXXXXXX	PDR1 [R/W] B XXXXXXXX	PDR2 [R/W] B XXXXXXXX	—	T-unit Port Data Register
000004H	—	—	PDR6 [R/W] B XXXXXXXX	—	
000008H	PDR8 [R/W] B XXXXXXXX	PDR9 [R/W] B -XXXXXXX	PDRA [R/W] B XXXXXXXX	PDRB [R/W] B XXXXXXXX	
00000CH	—				
000010H	PDRG [R/W] B XXXXXXXX	PDRH [R/W] B -----XXX	—	PDRJ [R/W] B XXXXXXXX	R-bus Port Data Register
000014H to 00003CH	—				Reserved
000040H	EIRR [R/W] B, H, W 00000000	ENIR [R/W] B, H, W 00000000	ELVR [R/W] B, H, W 00000000		Ext int
000044H	DICR [R/W] B, H, W -------0	HRCL [R/W] B, H, W 0--11111	—		DLYI/I-unit
000048H	TMRLR0 [W] H, W XXXXXXXX XXXXXXXX		TMR0 [R] H, W XXXXXXXX XXXXXXXX		Reload Timer 0
00004CH	—		TMCSR0 [R/W] B, H, W --XX0000 00000000		
000050H	TMRLR1 [W] H, W XXXXXXXX XXXXXXXX		TMR1 [R] H, W XXXXXXXX XXXXXXXX		Reload Timer 1
000054H	—		TMCSR1 [R/W] B, H, W --XX0000 00000000		
000058H	TMRLR2 [W] H, W XXXXXXXX XXXXXXXX		TMR2 [R] H, W XXXXXXXX XXXXXXXX		Reload Timer 2
00005CH	—		TMCSR2 [R/W] B, H, W --XX0000 00000000		
000060H	SSR0 [R/W] B, H, W 00001000	SIDR0 [R] SODR0 [W] B, H, W XXXXXXXX	SCR0 [R/W] B, H, W 00000100	SMR0 [R/W] B, H, W 00--0-0-	UART0
000064H	UTIM0 [R] H, W (UTIMR0 [W] H, W) 00000000 00000000		DRCL0 [W] B --------	UTIMC0 [R/W] B 0--00001	U-TIMER 0
000068H	SSR1 [R/W] B, H, W 00001000	SIDR1 [R] SODR1 [W] B, H, W XXXXXXXX	SCR1 [R/W] B, H, W 00000100	SMR1 [R/W] B, H, W 00--0-0-	UART1
00006CH	UTIM1 [R] H, W (UTIMR1 [W] H, W) 00000000 00000000		DRCL1 [W] B --------	UTIMC1 [R/W] B 0--00001	U-TIMER 1

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
000070H	SSR2 [R/W] B, H, W 00001000	SIDR2 [R] SODR2 [W] B, H, W XXXXXXXX	SCR2 [R/W] B, H, W 00000100	SMR2 [R/W] B, H, W 00 - - 0 - 0 -	UART2
000074H	UTIM2 [R] H, W (UTIMR2 [W] H, W) 00000000 00000000		DRCL2 [W] B - - - - - - - -	UTIMC2 [R/W] B 0 - - 00001	U-TIMER 2
000078H	ADCR [R] B, H, W 000000XX XXXXXXXX		ADCS [R/W] B, H, W 00000000 00000000		A/D Converter Sequential Comparator
00007CH	ADCR0 [R] B, H, W XXXXXXXX	ADCR1 [R] B, H, W XXXXXXXX	ADCR2 [R] B, H, W XXXXXXXX	ADCR3 [R] B, H, W XXXXXXXX	
000080H to 000090H	—				Reserved
000094H	IBCR0 [R/W] B, H, W 00000000	IBSR0 [R] B, H, W 00000000	ITBA0 [R, R/W] B, H, W 00000000 00000000		I²C interface0
000098H	ITMK0 [R, R/W] B, H, W 00111111 11111111		ISMK0 [R/W] B, H, W 01111111	ISBA0 [R, R/W] B, H, W 00000000	
00009CH	—	IDAR0 [R/W] B, H, W 00000000	ICCR0 [R, W, R/W] B, H, W 00011111	IDBL0 [R, R/W] B, H, W 00000000	
0000A0H	—	—	—	—	Reserved
0000A4H	—	—	—	—	
0000A8H to 0000B0H	—				Reserved
0000B4H	IBCR1 [R/W] B, H, W 00000000	IBSR1 [R] B, H, W 00000000	ITBA1 [R, R/W] B, H, W 00000000 00000000		I²C interface1
0000B8H	ITMK1 [R, R/W] B, H, W 00111111 11111111		ISMK1 [R/W] B, H, W 01111111	ISBA1 [R, R/W] B, H, W 00000000	
0000BCH	—	IDAR1 [R/W] B, H, W 00000000	ICCR1 [R, W, R/W] B, H, W 00011111	IDBL1 [R, R/W] B, H, W 00000000	
0000C0H	—	—	—	—	Reserved
0000C4H	—	—	—	—	
0000C8H to 0000D0H	—	—	—	—	
0000D4H	TCDT [R/W] H, W 00000000 00000000		—	TCCS [R/W] B, H, W 00000000	16 bit Free Run Timer
0000D8H	IPCP1 [R/W] H, W XXXXXXXX_XXXXXXXX		IPCP0 [R/W] H, W XXXXXXXX_XXXXXXXX		16 bit Input Capture

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
0000DC$_H$	IPCP3 [R/W] H, W XXXXXXXX_XXXXXXXX		IPCP2 [R/W] H, W XXXXXXXX_XXXXXXXX		16 bit Input capture
0000E0$_H$	—	ICS23 [R/W] B, H, W 00000000	—	ICS01 [R/W] B, H, W 00000000	
0000E4$_H$ to 000114$_H$	—				Reserved
000118$_H$	GCN10 [R/W] H 00110010 00010000		—	GCN20 [R/W] B 00000000	PPG timer
000011C$_H$	—				Reserved
000120$_H$	PTMR0 [R] H 11111111 11111111		PCSR0 [W] H, W XXXXXXXX XXXXXXXX		PPG0
000124$_H$	PDUT0 [W] H, W XXXXXXXX XXXXXXXX		PCNH0 [R/W] B 00000000	PCNL0 [R/W] B 000000X0	
000128$_H$	PTMR1[R] H 11111111 11111111		PCSR1 [W] H, W XXXXXXXX XXXXXXXX		PPG1
00012C$_H$	PDUT1 [W] H, W XXXXXXXX XXXXXXXX		PCNH1 [R/W] B 00000000	PCNL1 [R/W] B 000000X0	
000130$_H$	PTMR2 [R] H 11111111 11111111		PCSR2 [W] H, W XXXXXXXX XXXXXXXX		PPG2
000134$_H$	PDUT2 [W] H, W XXXXXXXX XXXXXXXX		PCNH2 [R/W] B 00000000	PCNL2 [R/W] B 000000X0	
000138$_H$	PTMR3[R] H 11111111 11111111		PCSR3 [W] H, W XXXXXXXX XXXXXXXX		PPG3
00013C$_H$	PDUT3 [W] H, W XXXXXXXX XXXXXXXX		PCNH3 [R/W] B 00000000	PCNL3 [R/W] B 000000X0	
000140$_H$ to 0001FC$_H$	—				Reserved
000200$_H$	DMACA0 [R/W] B, H, W*[1] 00000000 0000XXXX XXXXXXXX XXXXXXXX				DMAC
000204$_H$	DMACB0 [R/W] B, H, W 00000000 00000000 XXXXXXXX XXXXXXXX				
000208$_H$	DMACA1 [R/W] B, H, W*[1] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
00020C$_H$	DMACB1 [R/W] B, H, W 00000000 00000000 XXXXXXXX XXXXXXXX				
000210$_H$	DMACA2 [R/W] B, H, W*[1] 00000000 0000XXXX XXXXXXXX XXXXXXXX				

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
000214H	DMACB2 [R/W] B, H, W 00000000 00000000 XXXXXXXX XXXXXXXX				DMAC
000218H	DMACA3 [R/W] B, H, W*1 00000000 0000XXXX XXXXXXXX XXXXXXXX				
00021CH	DMACB3 [R/W] B, H, W 00000000 00000000 XXXXXXXX XXXXXXXX				
000220H	DMACA4 [R/W] B, H, W*1 00000000 0000XXXX XXXXXXXX XXXXXXXX				
000224H	DMACB4 [R/W] B, H, W 00000000 00000000 XXXXXXXX XXXXXXXX				
000228H to 00023CH	—				Reserved
000240H	DMACR [R/W] B 0XX00000 XXXXXXXX XXXXXXXX XXXXXXXX				DMAC
000244H to 000300H	—				Reserved
000304H	—			ISIZE [R/W] B, H, W ------10	I-Cache
000308H to 0003E0H	—				Reserved
0003E4H	—			ICHCR [R/W] B, H, W 0-000000	I-Cache
0003E8H to 0003EFH	—				Reserved
0003F0H	BSD0 [W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Bit Search Module
0003F4H	BSD1 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0003F8H	BSDC [W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0003FCH	BSRR [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000400H	DDRG [R/W] B 00000000	DDRH [R/W] B -----000	—	DDRJ [R/W] B 00000000	R-bus Data Direction Register

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
000404H to 00040CH	—				Reserved
000410H	PFRG [R/W] B 00------	PFRH [R/W] B ------0-	—	PFRJ [R/W] B -000-00-	R-bus Port Function Register
000414H to 00041CH	—				Reserved
000420H	—	PCRH [R/W] B -----000	—	—	R-bus Pull-up Resistance Control Register
000424H to 00043CH	—				Reserved
000440H	ICR00 [R/W] B, H, W ---11111	ICR01 [R/W] B, H, W ---11111	ICR02 [R/W] B, H, W ---11111	ICR03 [R/W] B, H, W ---11111	Interrupt Controller
000444H	ICR04 [R/W] B, H, W ---11111	ICR05 [R/W] B, H, W ---11111	ICR06 [R/W] B, H, W ---11111	ICR07 [R/W] B, H, W ---11111	
000448H	ICR08 [R/W] B, H, W ---11111	ICR09 [R/W] B, H, W ---11111	ICR10 [R/W] B, H, W ---11111	ICR11 [R/W] B, H, W ---11111	
00044CH	ICR12 [R/W] B, H, W ---11111	ICR13 [R/W] B, H, W ---11111	ICR14 [R/W] B, H, W ---11111	ICR15 [R/W] B, H, W ---11111	
000450H	ICR16 [R/W] B, H, W ---11111	ICR17 [R/W] B, H, W ---11111	ICR18 [R/W] B, H, W ---11111	ICR19 [R/W] B, H, W ---11111	
000454H	ICR20 [R/W] B, H, W ---11111	ICR21 [R/W] B, H, W ---11111	ICR22 [R/W] B, H, W ---11111	ICR23 [R/W] B, H, W ---11111	
000458H	ICR24 [R/W] B, H, W ---11111	ICR25 [R/W] B, H, W ---11111	ICR26 [R/W] B, H, W ---11111	ICR27 [R/W] B, H, W ---11111	
00045CH	ICR28 [R/W] B, H, W ---11111	ICR29 [R/W] B, H, W ---11111	ICR30 [R/W] B, H, W ---11111	ICR31 [R/W] B, H, W ---11111	
000460H	ICR32 [R/W] B, H, W ---11111	ICR33 [R/W] B, H, W ---11111	ICR34 [R/W] B, H, W ---11111	ICR35 [R/W] B, H, W ---11111	
000464H	ICR36 [R/W] B, H, W ---11111	ICR37 [R/W] B, H, W ---11111	ICR38 [R/W] B, H, W ---11111	ICR39 [R/W] B, H, W ---11111	
000468H	ICR40 [R/W] B, H, W ---11111	ICR41 [R/W] B, H, W ---11111	ICR42 [R/W] B, H, W ---11111	ICR43 [R/W] B, H, W ---11111	

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
00046C$_H$	ICR44 [R/W] B, H, W ---11111	ICR45 [R/W] B, H, W ---11111	ICR46 [R/W] B, H, W ---11111	ICR47 [R/W] B, H, W ---11111	Interrupt Controller
000470$_H$ to 00047C$_H$	—				
000480$_H$	RSRR [R, R/W] B, H, W 10000000 ($\overline{INIT}$) -0-XX-00 (INIT) XXX--X00 (RST)	STCR [R/W] B, H, W 001100-1 ($\overline{INIT}$) 0011XX-1 (INIT) 00X1XX-X (RST)	TBCR [R/W] B, H, W 00XXX-00 (INIT) 00XXX-XX (RST)	CTBR [W] B, H, W XXXXXXXX (INIT) XXXXXXXX (RST)	Clock Control unit
000484$_H$	CLKR [R/W] B, H, W -000-000 (INIT) -XXX-XXX (RST)	WPR [W] B, H, W XXXXXXXX (INIT) XXXXXXXX (RST)	DIVR0 [R/W] B, H, W 00000011 (INIT) XXXXXXXX (RST)	DIVR1 [R/W] B, H, W 0000----(INIT) XXXX----(RST)	
000488$_H$ to 0005FC$_H$	—				Reserved
000600$_H$	DDR0 [R/W] B 00000000	DDR1 [R/W] B 00000000	DDR2 [R/W] B 00000000	—	T-unit Data Direction Register
000604$_H$	—		DDR6 [R/W] B 00000000	—	
000608$_H$	DDR8 [R/W] B 00000000	DDR9 [R/W] B -0000000	DDRA [R/W] B 00000000	DDRB [R/W] B 00000000	
00060C$_H$	—				
000610$_H$	—				T-unit Port Function Register
000614$_H$	—	—	PFR6 [R/W] B 11111111	PFR61 [R/W] B ----0000	
000618$_H$	PFR8 [R/W] B 111--0--	PFR9 [R/W] B -0000111	PFRA1 [R/W] B 11111111	PFRB1 [R/W] B 00000000	
00061C$_H$	PFRB2 [R/W] B 000---00	—	PFRA2 [R/W] B --0-----	—	
000620$_H$	PCR0 [R/W] B 00000000	PCR1 [R/W] B 00000000	PCR2 [R/W] B 00000000	—	T-unit Pull-up Resis-tance Control Register
000624$_H$	—		PCR6 [R/W] B 00000000	—	
000628$_H$	PCR8 [R/W] B 00000000	PCR9 [R/W] B -000--0-	PCRA [R/W] B 00000000	PCRB [R/W] B 00000000	
00062C$_H$	—				

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
000630H to 00063CH	—				Reserved
000640H	ASR0 [R/W] H, W 00000000 00000000		ACR0 [R/W] H, W 1111XX00 00000000		T-unit
000644H	ASR1 [R/W] H, W XXXXXXXX XXXXXXXX		ACR1 [R/W] B, H, W XXXXXXXX XXXXXXXX		
000648H	ASR2 [R/W] H, W XXXXXXXX XXXXXXXX		ACR2 [R/W] B, H, W XXXXXXXX XXXXXXXX		
00064CH	ASR3 [R/W] H, W XXXXXXXX XXXXXXXX		ACR3 [R/W] B, H, W XXXXXXXX XXXXXXXX		
000650H	ASR4 [R/W] H, W XXXXXXXX XXXXXXXX		ACR4 [R/W] B, H, W XXXXXXXX XXXXXXXX		
000654H	ASR5 [R/W] H, W XXXXXXXX XXXXXXXX		ACR5 [R/W] B, H, W XXXXXXXX XXXXXXXX		
000658H	ASR6 [R/W] H, W XXXXXXXX XXXXXXXX		ACR6 [R/W] B, H, W XXXXXXXX XXXXXXXX		
00065CH	ASR7 [R/W] H, W XXXXXXXX XXXXXXXX		ACR7 [R/W] B, H, W XXXXXXXX XXXXXXXX		
000660H	AWR0 [R/W] B, H, W 01111111 11111011		AWR1 [R/W] B, H, W XXXXXXXX XXXXXXXX		
000664H	AWR2 [R/W] B, H, W XXXXXXXX XXXXXXXX		AWR3 [R/W] B, H, W XXXXXXXX XXXXXXXX		
000668H	AWR4 [R/W] B, H, W XXXXXXXX XXXXXXXX		AWR5 [R/W] B, H, W XXXXXXXX XXXXXXXX		
00066CH	AWR6 [R/W] B, H, W XXXXXXXX XXXXXXXX		AWR7 [R/W] B, H, W XXXXXXXX XXXXXXXX		
000670H	MCRA [R/W] B, H, W XXXXXXXX	MCRB [R/W] B, H, W XXXXXXXX	—		
000674H	—				
000678H	IOWR0 [R/W] B, H, W XXXXXXXX	IOWR1 [R/W] B, H, W XXXXXXXX	IOWR2 [R/W] B, H, W XXXXXXXX	—	
00067CH	—				
000680H	CSER [R/W] B, H, W 00000001	CHER [R/W] B, H, W 11111111	—	TCR [R/W] B, H, W 00000000 (INIT) 0000XXXX (RST)	
000684H	RCR [R/W] B, H, W 00XXXXXX XXXX0XXX		—		

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
00068CH to 0007F8H	—				Reserved
0007FCH	—	MODR [W] *2 XXXXXXXX	—		T-unit
000800H to 000AFCH	—				Reserved
000B00H	ESTS0 [R/W] B X0000000	ESTS1 [R/W] B XXXXXXXX	ESTS2 [R] B 1XXXXXXX	—	DSU (Evaluation chip only)
000B04H	ECTL0 [R/W] B 0X000000	ECTL1 [R/W] B 00000000	ECTL2 [W] B 000X0000	ECTL3 [R/W] B 00X00X11	
000B08H	ECNT0 [W] B XXXXXXXX	ECNT1 [W] B XXXXXXXX	EUSA [W] B XXX00000	EDTC [W] B 0000XXXX	
000B0CH	EWPT [R] H 00000000 00000000		ECTL4 [R] ([R/W]) B -0X00000	ECTL5 [R] ([R/W]) B ----000X	
000B10H	EDTR0 [W] H XXXXXXXX XXXXXXXX		EDTR1 [W] H XXXXXXXX XXXXXXXX		
000B14H to 000B1CH	—				
000B20H	EIA0 [W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B24H	EIA1 [W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B28H	EIA2 [W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B2CH	EIA3 [W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B30H	EIA4 [W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B34H	EIA5 [W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B38H	EIA6 [W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B3CH	EIA7 [W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B40H	EDTA [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B44H	EDTM [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
000B48H	EOA0 [W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				DSU (Evaluation chip only)
000B4CH	EOA1 [W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B50H	EPCR [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B54H	EPSR [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B58H	EIAM0 [W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B5CH	EIAM1 [W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B60H	EOAM0/EODM0 [W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B64H	EOAM1/EODM1 [W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B68H	EOD0 [W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B6CH	EOD1 [W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B70H to 000FFCH	—				Reserved
001000H	DMASA0 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				DMAC
001004H	DMADA0 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001008H	DMASA1 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00100CH	DMADA1 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001010H	DMASA2 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001014H	DMADA2 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001018H	DMASA3 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00101CH	DMADA3 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001020H	DMASA4 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

(Continued)

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
001024H	DMADA4 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				DMAC
001028H to 001FFCH	—				Reserved

*1 : Byte access is not permitted for the lower 16 bits of DMAC0 to DMAC4 (DTC15 to DTC0) .

*2 : This register is accessed through mode vector fetch; it cannot be accessed in normal mode.

■ INTERRUPT VECTORS

Interrupt	Interrupt No.		Interrupt level*1	Offset	TBR default address*2	RN
	10	16				
Reset	0	00	—	$3FC_H$	$000FFFFC_H$	—
Mode vector	1	01	—	$3F8_H$	$000FFFF8_H$	—
System reserved	2	02	—	$3F4_H$	$000FFFF4_H$	—
System reserved	3	03	—	$3F0_H$	$000FFFF0_H$	—
System reserved	4	04	—	$3EC_H$	$000FFFEC_H$	—
System reserved	5	05	—	$3E8_H$	$000FFFE8_H$	—
System reserved	6	06	—	$3E4_H$	$000FFFE4_H$	—
Coprocessor absent trap	7	07	—	$3E0_H$	$000FFFE0_H$	—
Coprocessor error trap	8	08	—	$3DC_H$	$000FFFDC_H$	—
INTE instruction	9	09	—	$3D8_H$	$000FFFD8_H$	—
Instruction break exception	10	0A	—	$3D4_H$	$000FFFD4_H$	—
Operand break trap	11	0B	—	$3D0_H$	$000FFFD0_H$	—
Step trace trap	12	0C	—	$3CC_H$	$000FFFCC_H$	—
NMI request (tool)	13	0D	—	$3C8_H$	$000FFFC8_H$	—
Undefined instruction exception	14	0E	—	$3C4_H$	$000FFFC4_H$	—
NMI request	15	0F	15 (F_H) fixed	$3C0_H$	$000FFFC0_H$	—
External interrupt 0	16	10	ICR00	$3BC_H$	$000FFFBC_H$	6
External interrupt 1	17	11	ICR01	$3B8_H$	$000FFFB8_H$	7
External interrupt 2	18	12	ICR02	$3B4_H$	$000FFFB4_H$	11
External interrupt 3	19	13	ICR03	$3B0_H$	$000FFFB0_H$	12
External interrupt 4	20	14	ICR04	$3AC_H$	$000FFFAC_H$	—
External interrupt 5	21	15	ICR05	$3A8_H$	$000FFFA8_H$	—
External interrupt 6	22	16	ICR06	$3A4_H$	$000FFFA4_H$	—
External interrupt 7	23	17	ICR07	$3A0_H$	$000FFFA0_H$	—
Reload timer 0	24	18	ICR08	$39C_H$	$000FFF9C_H$	8
Reload timer 1	25	19	ICR09	398_H	$000FFF98_H$	9
Reload timer 2	26	1A	ICR10	394_H	$000FFF94_H$	10
UART0 (RX completed)	27	1B	ICR11	390_H	$000FFF90_H$	0
UART1 (RX completed)	28	1C	ICR12	$38C_H$	$000FFF8C_H$	1
UART2 (RX completed)	29	1D	ICR13	388_H	$000FFF88_H$	2
UART0 (TX completed)	30	1E	ICR14	384_H	$000FFF84_H$	3
UART1 (TX completed)	31	1F	ICR15	380_H	$000FFF80_H$	4
UART2 (TX completed)	32	20	ICR16	$37C_H$	$000FFF7C_H$	5

(Continued)

Interrupt	Interrupt No.		Interrupt level*1	Offset	TBR default address*2	RN
	10	16				
DMAC0 (end, error)	33	21	ICR17	378H	000FFF78H	—
DMAC1 (end, error)	34	22	ICR18	374H	000FFF74H	—
DMAC2 (end, error)	35	23	ICR19	370H	000FFF70H	—
DMAC3 (end, error)	36	24	ICR20	36CH	000FFF6CH	—
DMAC4 (end, error)	37	25	ICR21	368H	000FFF68H	—
A/D	38	26	ICR22	364H	000FFF64H	15
PPG0	39	27	ICR23	360H	000FFF60H	13
PPG1	40	28	ICR24	35CH	000FFF5CH	14
PPG2	41	29	ICR25	358H	000FFF58H	—
PPG3	42	2A	ICR26	354H	000FFF54H	—
System reserved	43	2B	ICR27	350H	000FFF50H	—
U-TIMER0	44	2C	ICR28	34CH	000FFF4CH	—
U-TIMER1	45	2D	ICR29	348H	000FFF48H	—
U-TIMER2	46	2E	ICR30	344H	000FFF44H	—
Time base timer overflow	47	2F	ICR31	340H	000FFF40H	—
I^2C I/F0	48	30	ICR32	33CH	000FFF3FH	—
I^2C I/F1	49	31	ICR33	338H	000FFF38H	—
System reserved	50	32	ICR34	334H	000FFF34H	—
System reserved	51	33	ICR35	330H	000FFF30H	—
16 bit Free Run Timer	52	34	ICR36	32CH	000FFF2CH	—
ICU0 (load)	53	35	ICR37	328H	000FFF28H	—
ICU1 (load)	54	36	ICR38	324H	000FFF24H	—
ICU2 (load)	55	37	ICR39	320H	000FFF20H	—
ICU3 (load)	56	38	ICR40	31CH	000FFF1CH	—
System reserved	57	39	ICR41	318H	000FFF18H	—
System reserved	58	3A	ICR42	314H	000FFF14H	—
System reserved	59	3B	ICR43	310H	000FFF10H	—
System reserved	60	3C	ICR44	30CH	000FFF0CH	—
System reserved	61	3D	ICR45	308H	000FFF08H	—
System reserved	62	3E	ICR46	304H	000FFF04H	—
Delay interrupt bit	63	3F	ICR47	300H	000FFF00H	—
System reserved (Used by REALOS)	64	40	—	2FCH	000FFEFCH	—
System reserved (Used by REALOS)	65	41	—	2F8H	000FFEF8H	—
System reserved	66	42	—	2F4H	000FFEF4H	—

(Continued)

(Continued)

Interrupt	Interrupt No.		Interrupt level*1	Offset	TBR default address*2	RN
	10	16				
System reserved	67	43	—	$2F0_H$	$000FFEF0_H$	—
System reserved	68	44	—	$2EC_H$	$000FFEEC_H$	—
System reserved	69	45	—	$2E8_H$	$000FFEE8_H$	—
System reserved	70	46	—	$2E4_H$	$000FFEE4_H$	—
System reserved	71	47	—	$2E0_H$	$000FFEE0_H$	—
System reserved	72	48	—	$2DC_H$	$000FFEDC_H$	—
System reserved	73	49	—	$2D8_H$	$000FFED8_H$	—
System reserved	74	4A	—	$2D4_H$	$000FFED4_H$	—
System reserved	75	4B	—	$2D0_H$	$000FFED0_H$	—
System reserved	76	4C	—	$2CC_H$	$000FFECC_H$	—
System reserved	77	4D	—	$2C8_H$	$000FFEC8_H$	—
System reserved	78	4E	—	$2C4_H$	$000FFEC4_H$	—
System reserved	79	4F	—	$2C0_H$	$000FFEC0_H$	—
Used by INT instruction	80 to 255	50 to FF	—	$2BC_H$ to 000_H	$000FFEBC_H$ to $000FFC00_H$	—

*1 : ICRs are registers built in the interrupt controller to set interrupt levels for individual interrupt requests.
The ICRs are provided for the different interrupt levels.

*2 : The TBR is the register holding the start address of the EIT vector table.
The TBR value and the offset value preset for each EIT source are added together to be the vector address.

Note: The 1 Kbyte area from the TBR address is the EIT vector area.
The vector size is 4 bytes and the relationship between vector number and vector address is expressed as follows:

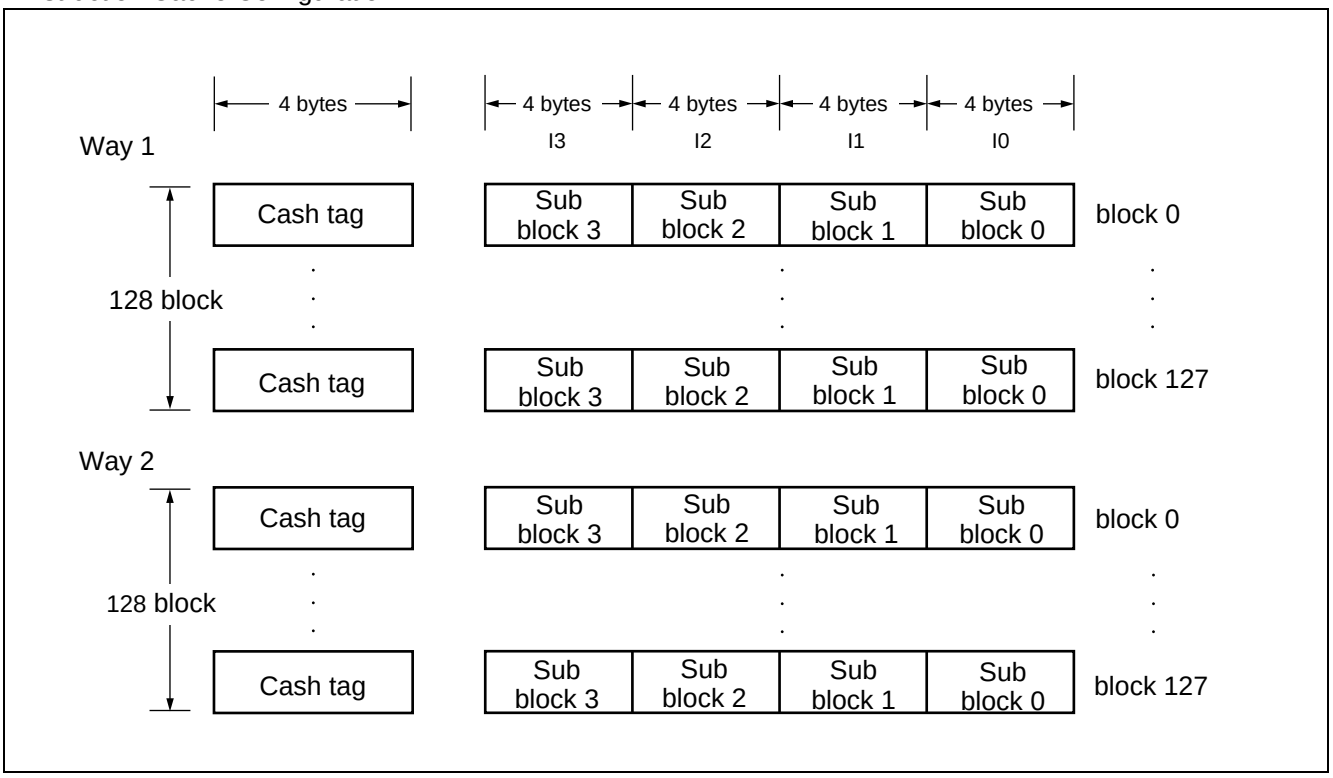
Vctadr = TBR + vctofs
= TBR + $(3FC_H - 4 \times vct)$
vctadr : vector address
vctofs : vector offset
vct : vector number

■ INSTRUCTION CACHE

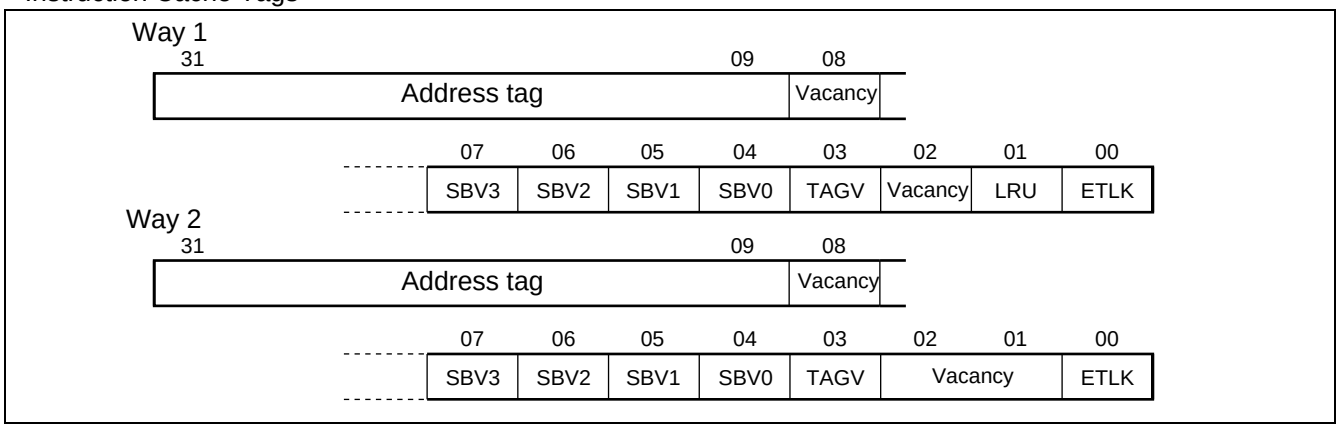
The instruction cache is a fast local memory for temporary storage. Once an instruction code is accessed from external slower memory, the instruction cache holds the instruction code inside to increase the speed of accessing the same code from then on.
By setting the RAM mode, the instruction cache data RAM is made directly read/write-accessible by software.

- Configuration
  - FR family's basic instruction length : Two bytes
  - Block layout : Two-way set associative
  - Blocks : 128 blocks per way
    16 bytes per block (= 4 sub-blocks)
    4 bytes per sub-block (= 1 bus access unit)

- Instruction Cache Configuration



• Instruction Cache Tags



[bit 31 to bit 9] Address tag

The address tag stores the upper 23 bits of the memory address of the instruction cached in the corresponding block.
For example, memory address IA of the instruction data stored in sub-block k in block i is obtained from the following equation:

$IA = \text{address tag} \times 2^9 + i \times 2^4 + k \times 2^2$

The address tag is used to check for a match with the instruction address requested for access by the CPU. The CPU and cache behave as follows depending on the result of the tag check:

- When the requested instruction data exists in the cache (hit), the cache transfers the data to the CPU within the cycle.
- When the requested instruction data does not exist in the cache (miss), the CPU and cache obtain the data loaded by external access at the same time.

[bit 7 to bit4] SBV3 to SBV0 : Sub-block validation

When SBV_n contains "1", the corresponding sub-block holds the current instruction data at the address located by the tag. Each sub-block usually holds two instructions (excluding immediate-value transfer instructions).

[bit 3] TAGV : Tag validation bit

This bit indicates whether the address tag value is valid. When the bit contains "0", the corresponding block is invalid regardless of the settings of the sub-block validation bits. (The bit is set to "0" when the cache is flushed.)

[bit 1] LRU (only in way 1)

This bit exists only in the instruction cache tag in way 1. The bit indicates way 1 or 2 as the way containing the last entry accessed in the selected set. When set to "1", the LRU bit indicates that the entry of the set in way 1 is the last entry accessed. When set to "0", it indicates that the one in way 2 is the last entry accessed.

[bit 0] ETLK : Entry lock

This bit is used to lock all the entries in the block corresponding to the tag in the cache. When the ETLK bit is set to "1", the entries are locked and are not updated when a cache miss occurs. Note, however, that invalid sub-blocks are updated. If a cache miss occurs with both of ways 1 and 2 in the entry lock states, access to external memory takes place after losing one cycle used for evaluating the cache miss.

Control Registers

• Cache Size Register (ISIZE)

Address : 00000307H

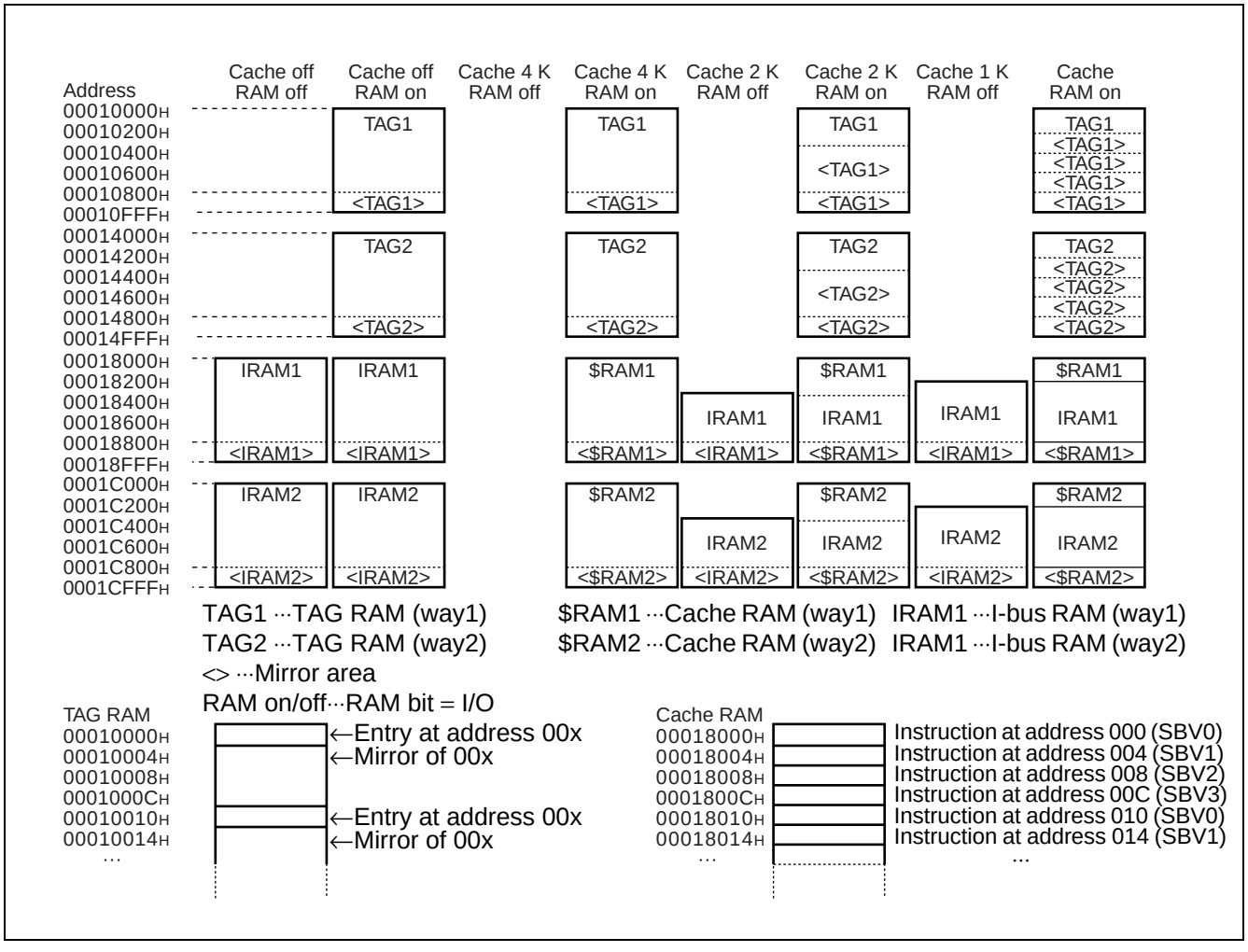
bit	7	6	5	4	3	2	1	0	Initial value
	—	—	—	—	—	—	SIZE1	SIZE0	- - - - - - 10B
	—	—	—	—	—	—	R/W	R/W	

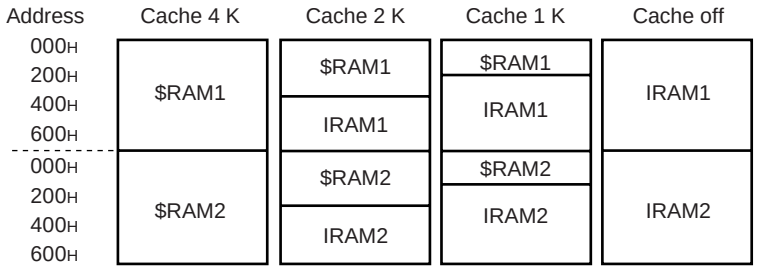
• Instruction Cache Control Register (ICHCR)

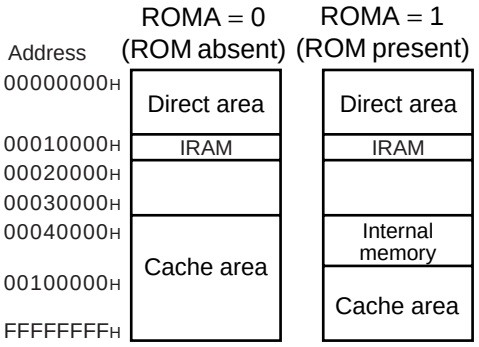
The instruction cache (I-cache) control register (ICHCR) controls the operations of the instruction cache. Writing a value to the ICHCR has no effect on the caching of any instruction fetched within three cycles that follow.

Address : 000003E7H

bit	7	6	5	4	3	2	1	0	Initial value
	RAM	—	GBLK	ALFL	EOLK	ELKR	FLSH	ENAB	0 - 000000B
	R/W	—	R/W	R/W	R/W	R/W	R/W	R/W	







(Even the D-bus RAM area is cashed, when it is transferred to the IA-Bus.)
Internal ROM/RAM area should be cached.

Each chip-select area can be set as a non-cache area.

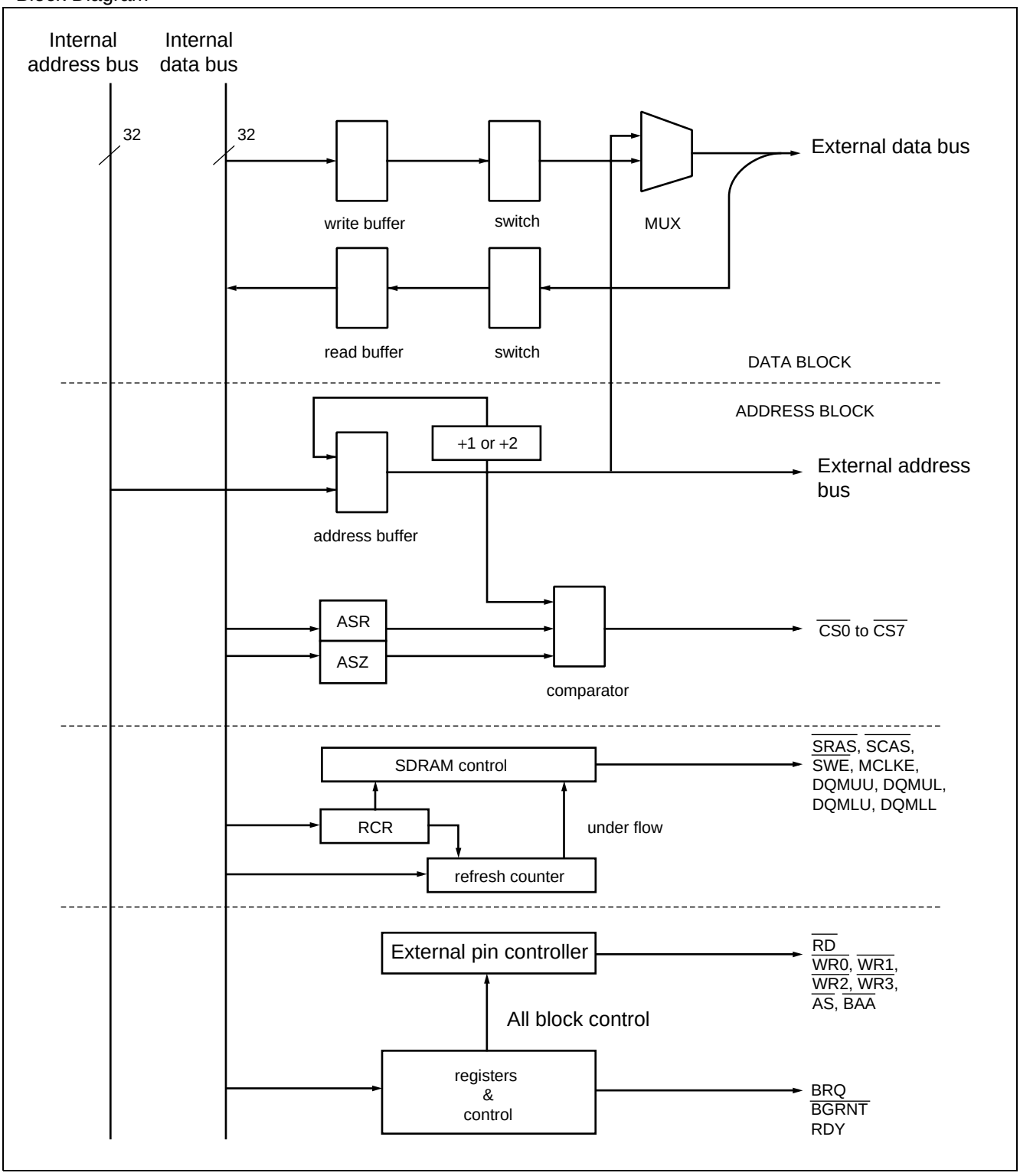
■ PERIPHERAL RESOURCES

1. External Bus Interface Controller

• External Bus Interface Controller Features

- Maximum output address width = 32-bit (4 Gbytes memory space)
- Various different types of external memory (8-bit, 16-bit, or 32-bit devices) can be directly connected and the controller can support multiple devices with different access timings.
  Asynchronous SRAM, asynchronous ROM/FLASH memory (supports multiple write strobe access or byte-enable access)
  Page mode ROM/FLASH memory (2, 4, or 8 page size)
  Burst mode ROM/FLASH memory
  Address/data multiplexed bus (8-bit or 16-bit width only)
  Synchronous memory (built-in ASIC memory, etc.)
  Note: Synchronous SRAM cannot be directly connected.
- Memory can be divided into eight independent banks (chip select areas) with a separate chip select output for each bank.
  The size of each area can be set in 64 Kbytes increments (the size of each chip select area can range from 64 Kbytes to 2 Gbytes)
  Each area can be located anywhere in the physical address space (subject to boundary limitations based on the area size)
- The following functions can be set independently for each chip select area :
  Chip select area enable/disable (Access is not performed to disabled areas)
  Setting of an access timing type to support each type of memory (For SDRAM, only the $\overline{CS6}$ and $\overline{CS7}$ areas can be connected.)
  Detailed access timing settings (wait cycles and similar settings for each access type)
  Data bus width (8-bit, 16-bit, 32-bit)
  Byte-ordering setting (big or little endian)
  Note: The $\overline{CS0}$ area must be big endian.
  Write-prohibit setting (read-only areas)
  Enable or disable loading into built-in cache
  Enable or disable prefetch function
  Maximum burst length setting (1, 2, 4, 8)
- Different detailed timing settings can be set for each timing type
  Even for the same type, different settings can be used for each chip select area.
  Up to 15 auto-wait cycles can be specified. (For asynchronous SRAM, ROM, Flash, and I/O areas)
  The bus cycle can be extended by the external RDY input. (For asynchronous SRAM, ROM, Flash, and I/O areas)
  Fast access wait and page wait settings are supported (For burst/page mode ROM and Flash areas)
  Idle cycles, recovery cycles, setup delays, and similar can be inserted.
  Capable of setting timing values such as the CAS latency and RAS-CAS delay (SDRAM area)
  Capable of controlling the distributed/centralized auto-refresh, self-refresh, and other refresh timings (SDRAM area)
- DMA supports fly-by transfer
  Transfer between memory and I/O can be performed by a single access.
  Memory wait cycles can be synchronized with the I/O wait period during fly-by transfer.
  Hold times can be maintained by extending access to the data source only.
  Separate idle and recovery cycle settings can be specified for use in fly-by transfer.
- Supports external bus arbitration using BRQ and $\overline{BGRNT}$.
- Pins not used by the external interface can be set as general purpose I/O ports.

• Block Diagram



- I/O pin
  External interface pin (Some pins are general purpose pins.)
  The following shows I/O pins of each interface.

  - Normal bus interface
    A23 to A00, D31 to D00 (AD15 to AD00)
    $\overline{CS0}$, $\overline{CS1}$, $\overline{CS2}$, $\overline{CS3}$, $\overline{CS4}$, $\overline{CS5}$, $\overline{CS6}$, $\overline{CS7}$
    $\overline{AS}$, SYSCLK, MCLK,
    $\overline{RD}$
    $\overline{WR}$, $\overline{WR0}$ ($\overline{UUB}$) , $\overline{WR1}$ ($\overline{ULB}$) , $\overline{WR2}$ ($\overline{ULB}$) , $\overline{WR3}$ ($\overline{LLB}$) ,
    RDY, BRQ, $\overline{BGRNT}$
  - Memory interface
    MCLK, MCLKE
    MCLKI (for SDRAM)
    $\overline{LBA}$ (= $\overline{AS}$) , $\overline{BAA}$ (for burst ROM/FLASH)
    $\overline{SRAS}$, $\overline{SCAS}$, $\overline{SWE}$ (= $\overline{WR}$) (for SDRAM)
    DQMUU, DQMUL, DQMLU, DQMLL (for SDRAM (= $\overline{WR0}$, $\overline{WR1}$, $\overline{WR2}$, $\overline{WR3}$))
  - DMA interface
    $\overline{IOWR}$, $\overline{IORD}$
    DACK0, DACK1
    DREQ0, DREQ1
    DEOP0, DEOP1

• Register List

31 24	23 16	15 08	07 00
ASR0		ACR0	
ASR1		ACR1	
ASR2		ACR2	
ASR3		ACR3	
ASR4		ACR4	
ASR5		ACR5	
ASR6		ACR6	
ASR7		ACR7	
AWR0		AWR1	
AWR2		AWR3	
AWR4		AWR5	
AWR6		AWR7	
MCRA	MCRB	Reserved	Reserved
Reserved	Reserved	Reserved	Reserved
IOWR0	IOWR1	Reserved	Reserved
Reserved	Reserved	Reserved	Reserved
CSER	CHER	Reserved	TCR
RCR		Reserved	Reserved
Reserved	Reserved	Reserved	Reserved
Reserved	Reserved	Reserved	Reserved
Reserved	Reserved	Reserved	Reserved
Reserved	Reserved	Reserved	Reserved
Reserved	(MODR)	Reserved	Reserved

Area select registers 0 to 7 (ASR0 to ASR7)
Area configuration registers 0 to 7 (ACR0 to ACR7)

Area weight register (AWR0 to AWR7)

Memory setting register
(For SDRAM/FCRAM auto-precharge OFF mode) (MCRA)

Memory setting register
(For FCRAM auto-precharge ON mode) (MCRB)

DMAC I/O wait registers (IOWR0 and IOWR1)

Chip-select area enable register (CSER)

Cache fetch enable register (CHER)

Terminal and timing control register (TCR)

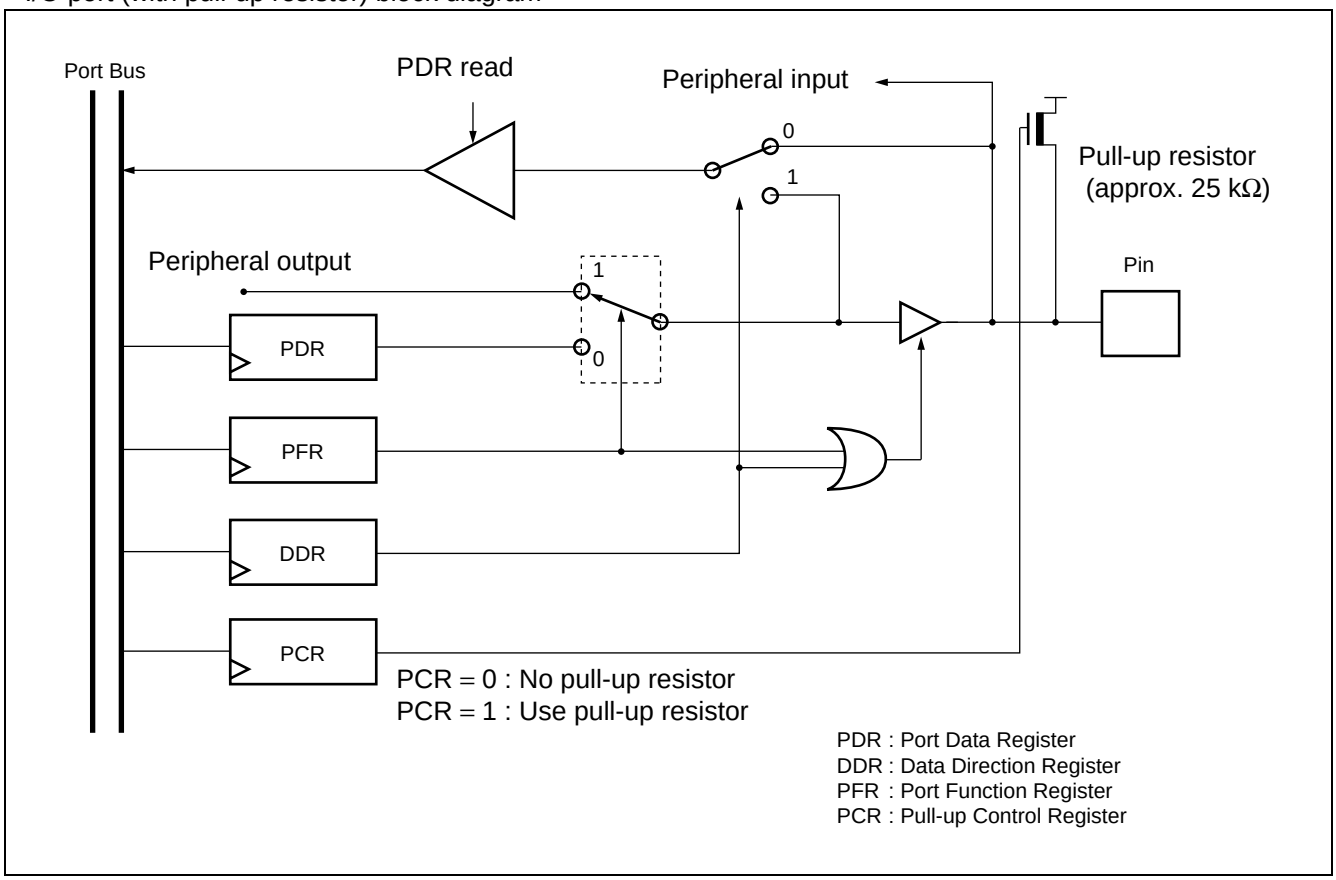
Refresh control register (RCR)

Notes : • Reserved indicates a reserved register. When writing, always set to “0”.
• The MODR register cannot be accessed by the user program.

2. I/O Ports

MB91301 series pins can be used as I/O ports when not set for use by the external bus interface or the various peripheral I/O functions.

• I/O port (with pull-up resistor) block diagram



Note : For port output, the pull-up resistor is disabled irrespective of the setting.

I/O ports with pull-up resistors have the following registers :

- PDR (Port Data Register)
- DDR (Data Direction Register)
- PFR (Port Function Register)
- PCR (Pull-up Control Register)

I/O ports have three following modes

- When port is in input mode (PFR = “0” & DDR = “0”)
  PDR read : Reads the level of the corresponding external pin.
  PDR write : Writes the value to the PDR.
- When port is in output mode (PFR = “0” & DDR = “1”)
  PDR read : Reads the PDR value.
  PDR write : Outputs the PDR value to the corresponding external pin.
- When port is in peripheral output mode (PFR = “1” & DDR = “X”)
  PDR : Reads the value of the corresponding peripheral output.
  PDR write : Writes the value to the PDR.

Notes :
- Use byte access to access ports.
- The external bus function has priority for port 0 to port A when these are used as external bus pins. Accordingly, writing to the DDR has no effect on the pin input/output setting while the pins are operating as external bus pins. The value set in the DDR becomes meaningful when the PFR register is modified to set the pins as general purpose ports.
- In stop mode (HIZ = 0), the pull-up resistor control register setting is used.
- In stop mode (HIZ = 1), the pull-up resistor control register (PCR) setting is ignored during hardware standby.
- Using pull-up resistors is prohibited when these pins are used as external bus pins. In this case, do not write “1” to the corresponding bit in the pull-up resistor control register (PCR).

• Port Data Register (PDR)

		7	6	5	4	3	2	1	0	Initial value
PDR0										
Address :	00000000_H	P07	P06	P05	P04	P03	P02	P01	P00	$XXXXXXXX_B$
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
PDR1										
Address :	00000001_H	P17	P16	P15	P14	P13	P12	P11	P10	$XXXXXXXX_B$
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
PDR2										
Address :	00000002_H	P27	P26	P25	P24	P23	P22	P21	P20	$XXXXXXXX_B$
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
PDR6										
Address :	00000006_H	P67	P66	P65	P64	P63	P62	P61	P60	$XXXXXXXX_B$
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
PDR8										
Address :	00000008_H	P87	P86	P85	P84	P83	P82	P81	P80	$XXXXXXXX_B$
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
PDR9										
Address :	00000009_H	—	P96	P95	P94	P93	P92	P91	P90	$- XXXXXXX_B$
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
PDRA										
Address :	$0000000A_H$	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	$XXXXXXXX_B$
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
PDRB										
Address :	$0000000B_H$	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	$XXXXXXXX_B$
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
PDRG										
Address :	00000010_H	PG7	PG6	PG5	PG4	PG3	PG2	PG1	PG0	$XXXXXXXX_B$
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
PDRH										
Address :	00000011_H	—	—	—	—	—	PH2	PH1	PH0	$- - - - - XXX_B$
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
PDRJ										
Address :	00000013_H	PJ7	PJ6	PJ5	PJ4	PJ3	PJ2	PJ1	PJ0	$XXXXXXXX_B$
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- PDR0 to PDR2, PDR6, PDR8 to PDRB, PDRG, PDRH and PDRJ are the I/O data registers for the I/O pots.
- The corresponding PDR0 to DDRJ and PFR6 to PFRJ registers control input/output.
- P00 to P07, P10 to P17 and P20 to P27 do not have a PFR (port function register).

• Data Direction Register (DDR)

DDR0

Address : 00000600H	7	6	5	4	3	2	1	0	Initial value
	P07	P06	P05	P04	P03	P02	P01	P00	00000000B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

DDR1

Address : 00000601H	7	6	5	4	3	2	1	0	Initial value
	P17	P16	P15	P14	P13	P12	P11	P10	00000000B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

DDR2

Address : 00000602H	7	6	5	4	3	2	1	0	Initial value
	P27	P26	P25	P24	P23	P22	P21	P20	00000000B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

DDR6

Address : 00000606H	7	6	5	4	3	2	1	0	Initial value
	P67	P66	P65	P64	P63	P62	P61	P60	00000000B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

DDR8

Address : 00000608H	7	6	5	4	3	2	1	0	Initial value
	P87	P86	P85	P84	P83	P82	P81	P80	00000000B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

DDR9

Address : 00000609H	7	6	5	4	3	2	1	0	Initial value
	—	P96	P95	P94	P93	P92	P91	P90	- 0000000B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

DDRA

Address : 0000060AH	7	6	5	4	3	2	1	0	Initial value
	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	00000000B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

DDRB

Address : 0000060BH	7	6	5	4	3	2	1	0	Initial value
	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	00000000B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

DDRG

Address : 00000400H	7	6	5	4	3	2	1	0	Initial value
	PG7	PG6	PG5	PG4	PG3	PG2	PG1	PG0	00000000B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

DDRH

Address : 00000401H	7	6	5	4	3	2	1	0	Initial value
	—	—	—	—	—	PH2	PH1	PH0	- - - - - 000B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

DDRJ

Address : 00000403H	7	6	5	4	3	2	1	0	Initial value
	PJ7	PJ6	PJ5	PJ4	PJ3	PJ2	PJ1	PJ0	00000000B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

DDR0 to DDR2, DDR6, DDR8 to DDRB, DDRG, DDRH and DDRJ control the direction (input or output) of each bit in the corresponding port.

When PFR = 0 DDR = 0 : Port input
DDR = 1 : Port output

When PFR = 1 DDR = 0 : Peripheral input
DDR = 1 : Peripheral output

• Pull-up Resistor Control Register (PCR)

		bit	7	6	5	4	3	2	1	0	Initial value
PCR0	Address : 00000620H		P07	P06	P05	P04	P03	P02	P01	P00	00000000B
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
PCR1	Address : 00000621H	bit	7	6	5	4	3	2	1	0	Initial value
			P17	P16	P15	P14	P13	P12	P11	P10	00000000B
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
PCR2	Address : 00000622H	bit	7	6	5	4	3	2	1	0	Initial value
			P27	P26	P25	P24	P23	P22	P21	P20	00000000B
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
PCR6	Address : 00000626H	bit	7	6	5	4	3	2	1	0	Initial value
			P67	P66	P65	P64	P63	P62	P61	P60	00000000B
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
PCR8	Address : 00000628H	bit	7	6	5	4	3	2	1	0	Initial value
			P87	P86	P85	P84	P83	P82	P81	P80	00000000B
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
PCR9	Address : 00000629H	bit	7	6	5	4	3	2	1	0	Initial value
			—	P96	P95	P94	—	—	P91	—	- 000 - - 0 -B
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
PCRA	Address : 0000062AH	bit	7	6	5	4	3	2	1	0	Initial value
			PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	00000000B
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
PCRB	Address : 0000062BH	bit	7	6	5	4	3	2	1	0	Initial value
			PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	00000000B
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
PCRH	Address : 00000421H	bit	7	6	5	4	3	2	1	0	Initial value
			—	—	—	—	—	PH2	PH1	PH0	- - - - - 000B
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

PCR0 to PCR2, PCR6, PCR8 to PCRB, PCRG, PCRH and PCRJ control the pull-up resistors for the corresponding port.

PCR = 0 : No pull-up resistor

PCR = 1 : Use pull-up resistor

• Port Function Register (PFR)

		bit	7	6	5	4	3	2	1	0	Initial value
Address :	PFR6 00000616H		A23E	A22E	A21E	A20E	A19E	A18E	A17E	A16E	11111111B
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Address :	PFR8 00000618H	bit	WR3XE	WR2XE	WR1XE	—	—	BRQE	—	—	111 - - 0 - -B
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Address :	PFR9 00000619H	bit	—	WRXE	BAAE	ASXE	—	MCKE	MCKEE	SYSE	- 0000111B
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Address :	PFRA1 0000061AH	bit	CS7XE	CS6XE	CS5XE	CS4XE	CS3XE	CS2XE	CS1XE	CS0XE	11111111B
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Address :	PFRB1 0000061BH	bit	DES1	AK12	AK11	AK10	DES0	AK02	AK01	AK00	00000000B
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Address :	PFRB2 0000061CH	bit	DRDE	DWRE	PPE1	—	—	—	AKH1	AKH0	000 - - - 00B
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Address :	PFRA2 0000061EH	bit	—	—	PPE2	—	—	—	—	—	-- 0 - - - - -B
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Address :	PFRG 00000410H	bit	SCE2	SOE2	—	—	—	—	—	—	00 - - - - - -B
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Address :	PFRH 00000411H	bit	—	—	—	—	—	—	PPE3	—	- - - - - - 0 -B
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Address :	PFRJ 00000413H	bit	—	PPE0	SCE1	SOE1	—	SCE0	SOE0	—	- 000 - 00 -B
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Address :	PFR61 00000617H	bit	—	—	—	—	TEST1	TEST0	I2CE1	I2CE0	- - - - 0000 B
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

PFR6, PFR8 to PFRB, PFRA2, PFRG, PFRH and PFRJ control the output for the corresponding external bus interface or peripheral output bit.
Always write "0" to unused bits in the PFR.

3. Interrupt Controller

The interrupt controller receives and processes interrupts.

• Hardware Configuration

The interrupt controller consists of the following :

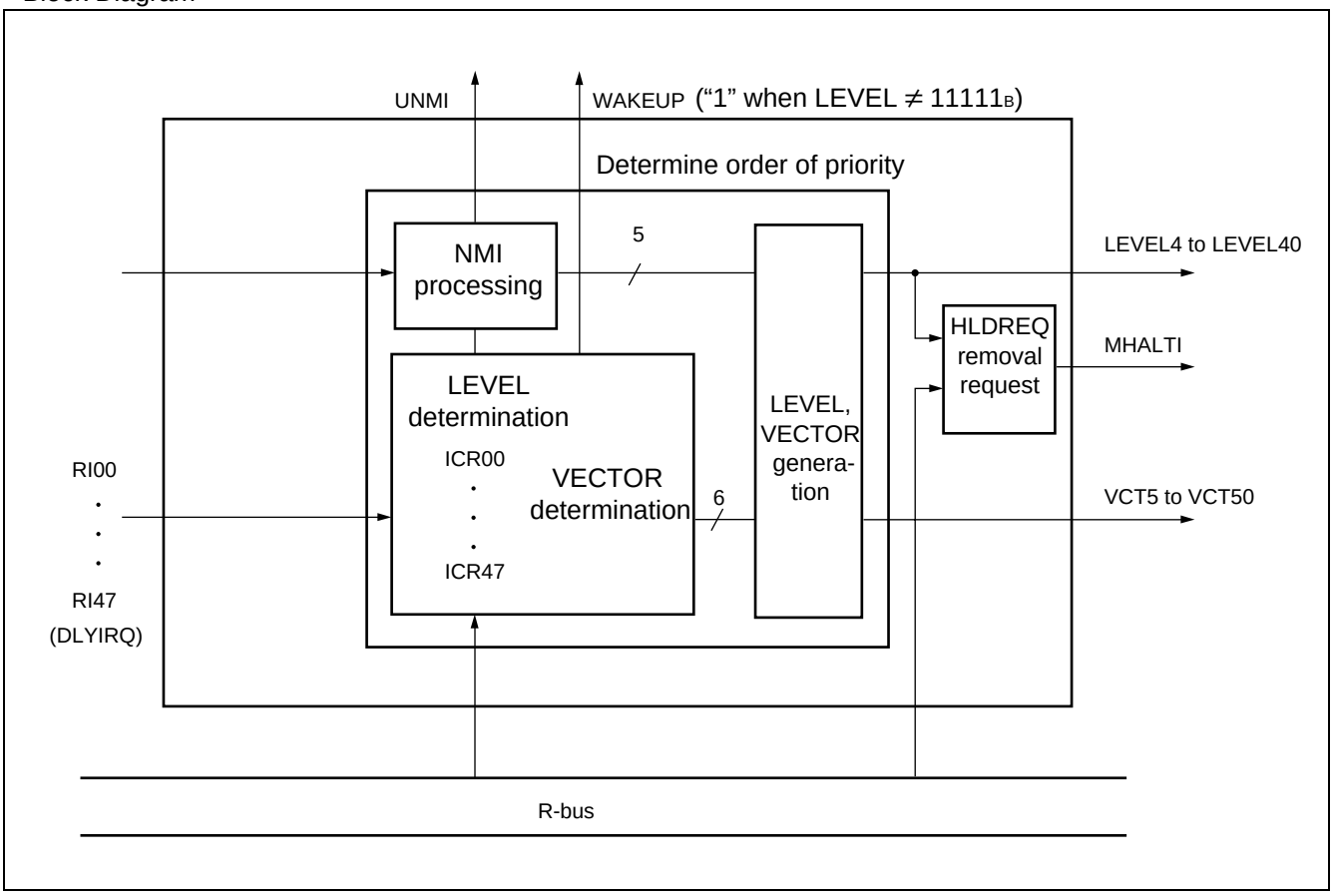
- ICR register
- Interrupt priority determination circuit
- Interrupt level and interrupt number (vector) generator
- Hold request removal request generator

• Principal Functions

The main functions of the interrupt controller are as follows :

- Detect NMI and interrupt requests
- Prioritize interrupts (according to level and number)
- Notify interrupt level of selected interrupt request (to CPU)
- Notify interrupt number of selected interrupt request (to CPU)
  If an NMI or interrupt request with an interrupt level other than "11111_B" occurs, notify recovery from stop mode (to CPU)
- Generate hold request removal requests to the bus master

• Block Diagram



• Register List

	bit 7	6	5	4	3	2	1	0	
Address : 00000440H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR00
Address : 00000441H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR01
Address : 00000442H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR02
Address : 00000443H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR03
Address : 00000444H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR04
Address : 00000445H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR05
Address : 00000446H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR06
Address : 00000447H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR07
Address : 00000448H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR08
Address : 00000449H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR09
Address : 0000044AH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR10
Address : 0000044BH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR11
Address : 0000044CH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR12
Address : 0000044DH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR13
Address : 0000044EH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR14
Address : 0000044FH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR15
Address : 00000450H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR16
Address : 00000451H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR17
Address : 00000452H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR18
Address : 00000453H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR19
Address : 00000454H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR20
Address : 00000455H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR21
Address : 00000456H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR22
Address : 00000457H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR23
Address : 00000458H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR24
Address : 00000459H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR25
Address : 0000045AH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR26
Address : 0000045BH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR27
Address : 0000045CH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR28
Address : 0000045DH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR29
Address : 0000045EH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR30
Address : 0000045FH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR31

(Continued)

(Continued)

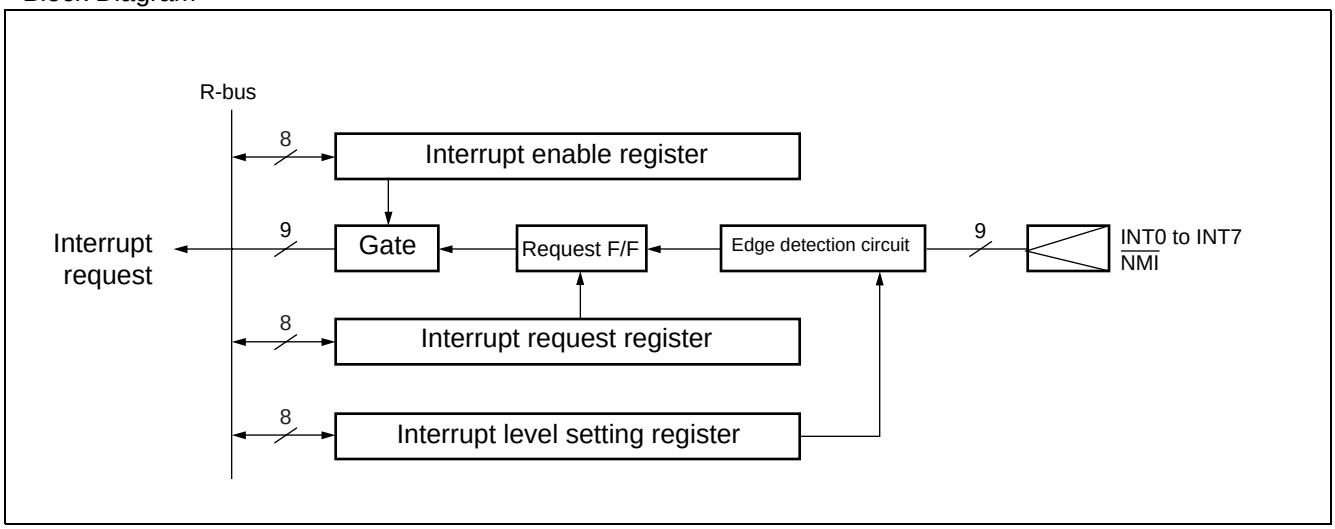
	bit	7	6	5	4	3	2	1	0	
Address: 00000460H		—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR32
Address: 00000461H		—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR33
Address: 00000462H		—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR34
Address: 00000463H		—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR35
Address: 00000464H		—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR36
Address: 00000465H		—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR37
Address: 00000466H		—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR38
Address: 00000467H		—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR39
Address: 00000468H		—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR40
Address: 00000469H		—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR41
Address: 0000046AH		—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR42
Address: 0000046BH		—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR43
Address: 0000046CH		—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR44
Address: 0000046DH		—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR45
Address: 0000046EH		—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR46
Address: 0000046FH		—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR47

Address: 0000045H		MHALTI	—	—	LVL4	LVL3	LVL2	LVL1	LVL0	HRCL

4. External Interrupt/NMI Control Block

The external interrupt control block controls external interrupt requests input to the $\overline{\text{NMI}}$ and INT0 to INT7 pins. The interrupt trigger level can be selected from "H", "L", "rising edge", or "falling edge" (except for NMI).

• Block Diagram



• Register List

External interrupt enable register (ENIR)

bit

7	6	5	4	3	2	1	0
EN7	EN6	EN5	EN4	EN3	EN2	EN1	EN0

External interrupt request register (EIRR)

bit

15	14	13	12	11	10	9	8
ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0

Request level setting register (ELVR)

bit

15	14	13	12	11	10	9	8
LB7	LA7	LB6	LA6	LB5	LA5	LB4	LA4

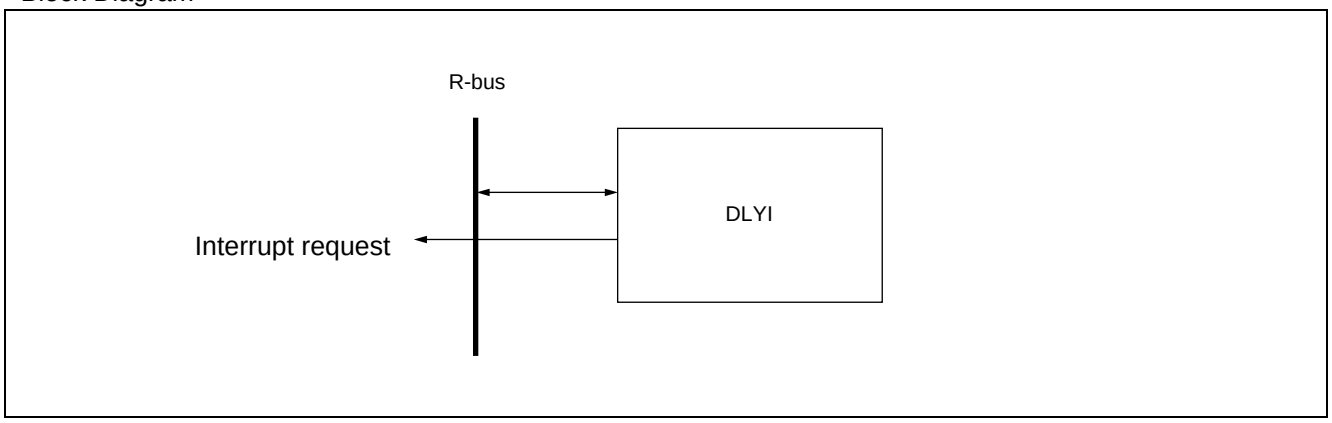
bit

7	6	5	4	3	2	1	0
LB3	LA3	LB2	LA2	LB1	LA1	LB0	LA0

5. Delay Interrupt Module

The delay interrupt module is used to generate interrupts for task switching.
This module can be used to generate and cancel interrupts to the CPU via software.

• Block Diagram



• Register List

Delay interrupt control register (DICR)

bit

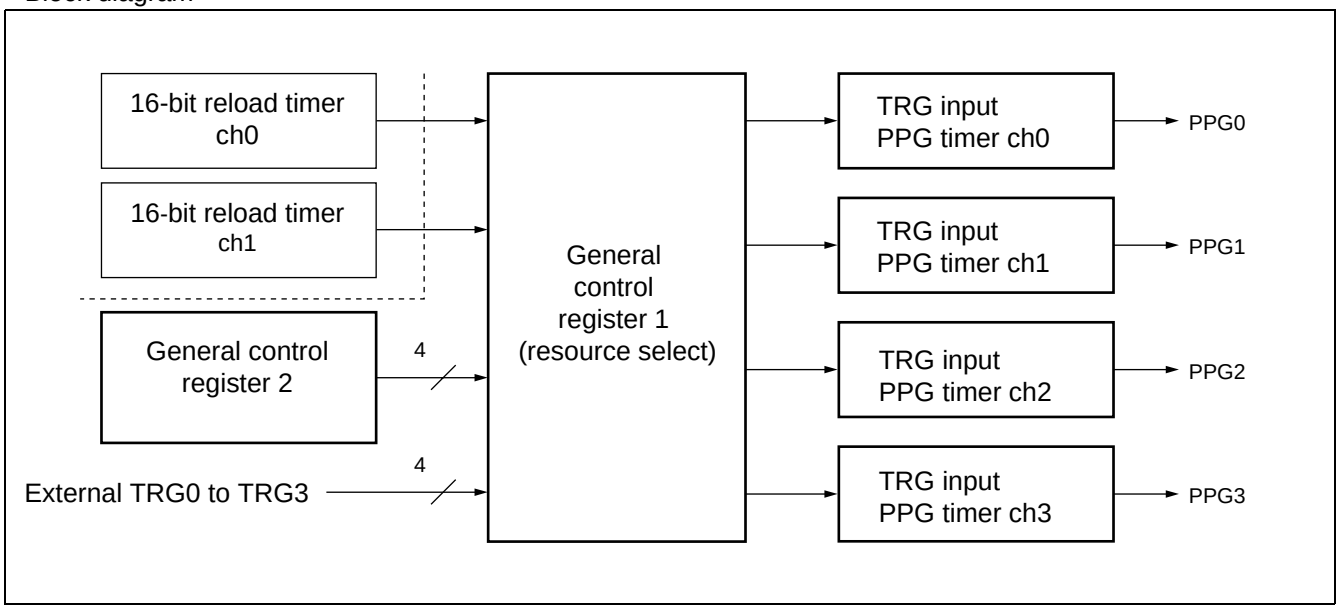
7	6	5	4	3	2	1	0
—	—	—	—	—	—	—	DLYI

6. PPG Timer

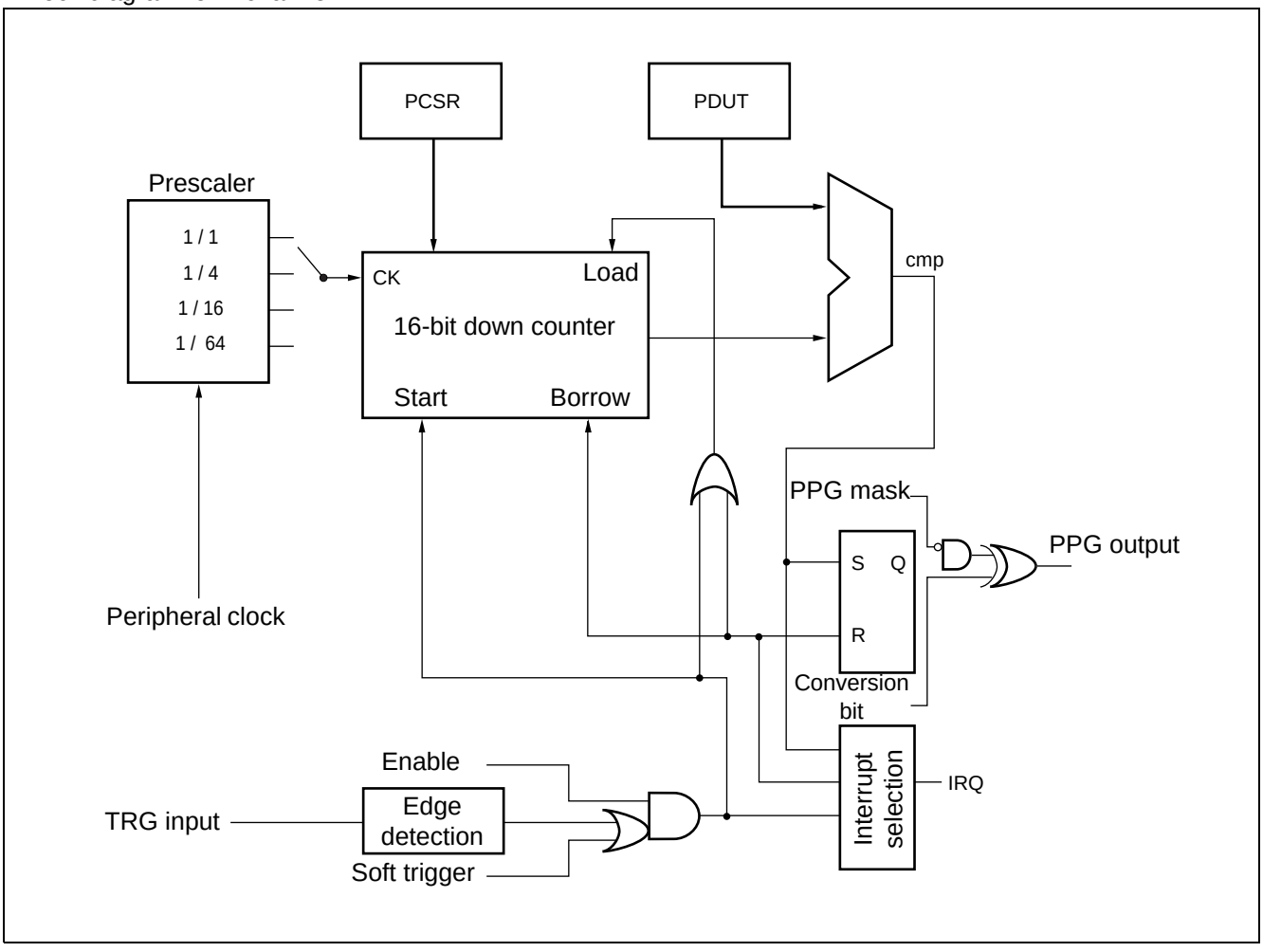
The PPG timer can output highly precise PWM waveforms efficiently.
The MB91301 series contains four channels of PPG timer.

- Features of the PPG Timer
  - Each channel consists of a 16-bit down counter, a 16-bit data register with cycle setting buffer, a 16-bit compare register with duty setting buffer, and pin control section.
  - The count clocks for the 16-bit down counter can be selected from the following four types :
    Internal clock ϕ, ϕ/4, ϕ/16, ϕ/64
  - The counter is initialized to “$FFFF_H$” at a reset or counter borrow.
  - Each channel has a PPG output.
  - Register outline
    Cycle setting register: Reload data register with buffer
    Duty setting register: Compare register with buffer
    Transfer from the buffer takes place upon a counter borrow.
  - Pin control overview
    A duty match sets the pin control section to 1. (Preferential)
    A counter borrow resets it to 0.
    The output value fix mode is available, which can each output all "L" (or "H").
    A polarity can also be specified.
  - An interrupt request can be generated at a combination of the following events :
    Activation of the PPG timer
    Counter borrow (cycle match)
    Duty match
    Counter borrow (cycle match) or duty match
    DMA transfer can be initiated by the above interrupt request.
  - It is possible to set the simultaneous activation of two or more channels by means of software or another interval timer.
    Restarting during operation can also be set.
  - The request level to be detected can be selected from among "rising edge", "falling edge", and "both edges".

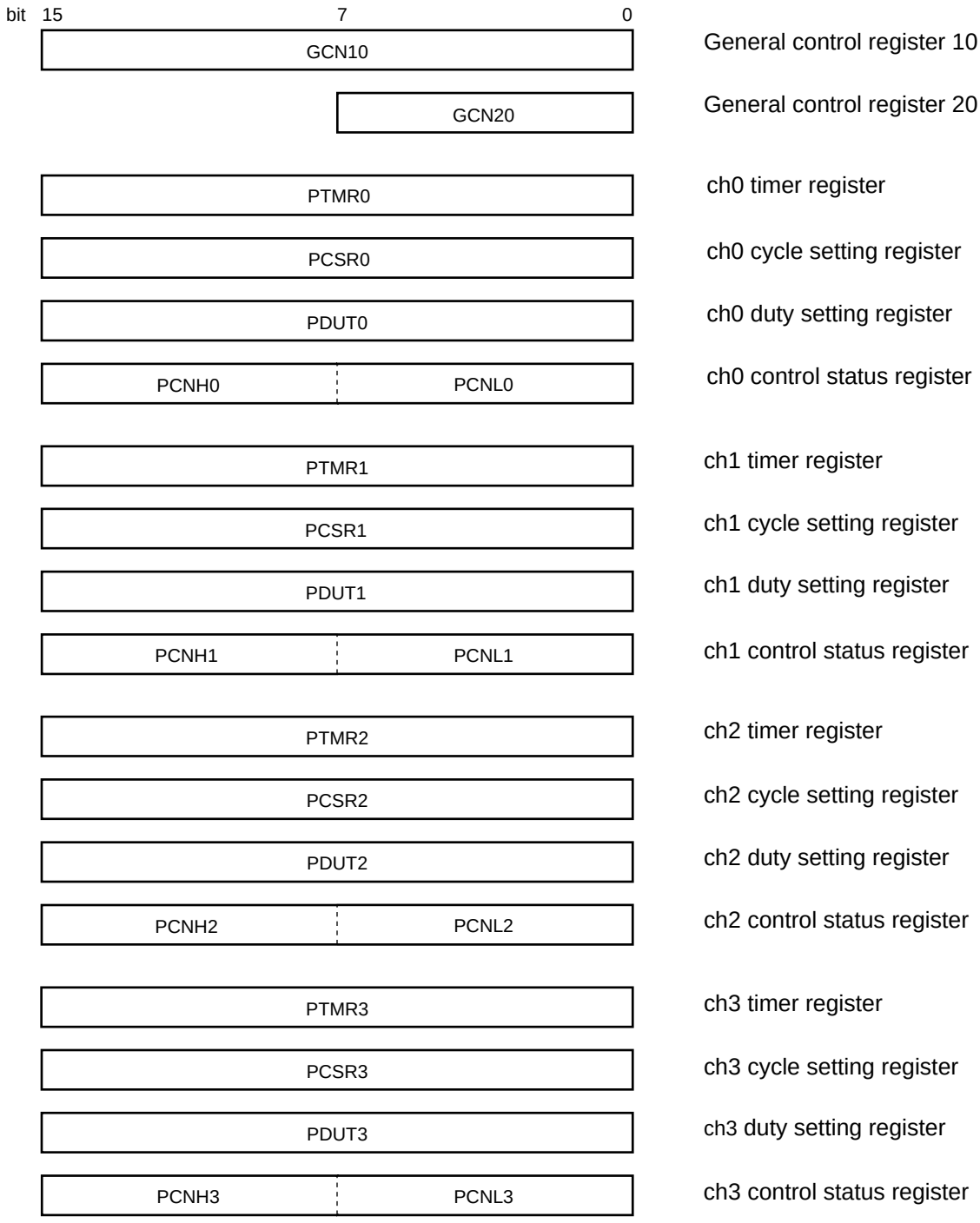
• Block diagram



• Block diagram for 1 channel



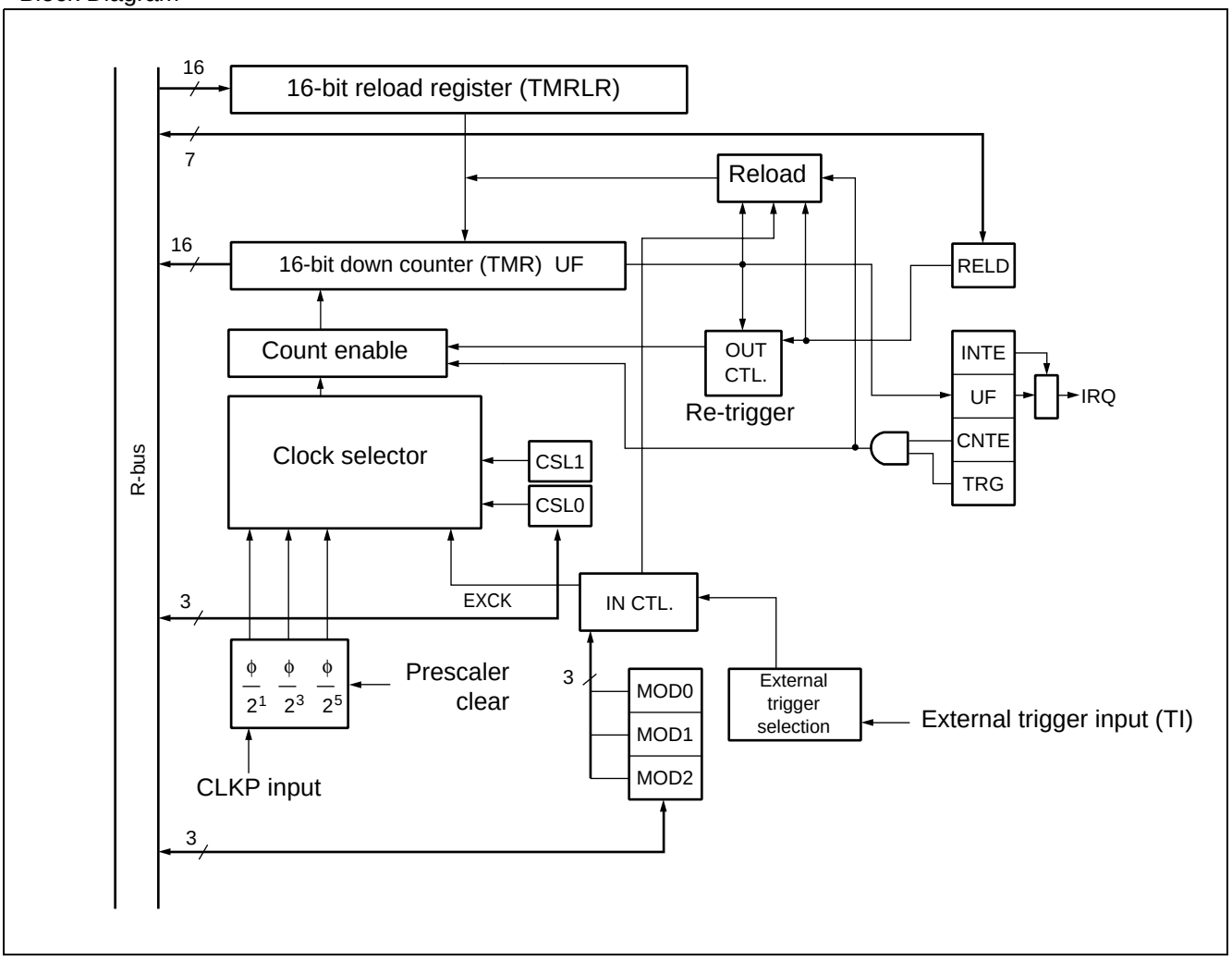
• Register List



7. 16-Bit Reload Timer

The 16-bit timer consists of a 16-bit down-counter, 16-bit reload register, prescaler for generating the internal count clock, and a control register.
The clock source can be selected from three internal clock signals (machine clock divided by 2, 8, or 32) or the external event.
The interrupt can be used to initiate DMA transfer.
The MB91301 series has three 16-bit reload timer channels.

• Block Diagram



• Register List

Control status register (TMCSR)

bit	15	14	13	12	11	10	9	8
	—	—	—	—	CSL1	CSL0	MOD2	MOD1

bit	7	6	5	4	3	2	1	0
	MOD0	—	OUTL	RELD	INTE	UF	CNTE	TRG

16-bit timer register (TMR)

bit	15	0

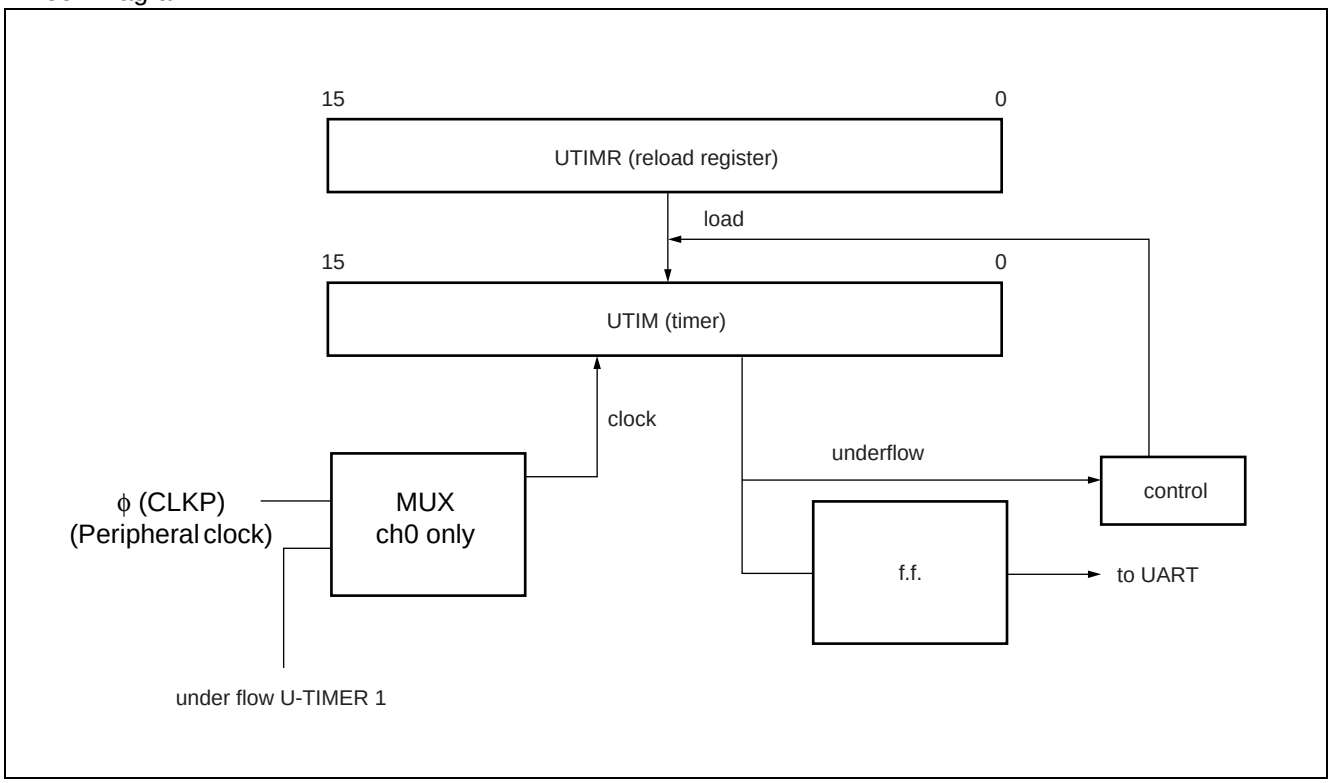
16-bit reload register (TMRLR)

bit	15	0

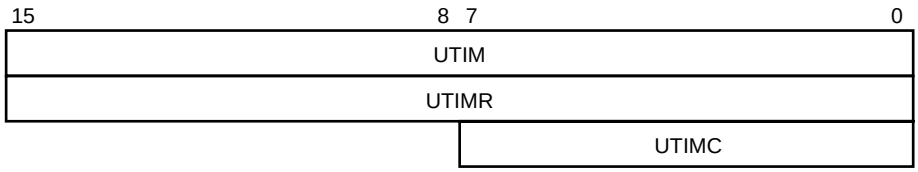
8. U-TIMER (16 bit timer for UART baud rate generation)

The U-TIMER is a 16-bit timer used to generate the baud rate for the UART. Any desired baud rate can be set using the combination of the chip operating frequency and U-TIMER reload value.
The U-TIMER can also be used as an interval timer by generating an interrupt from a count underflow event.
The MB91301 series has three U-TIMER channels. When used as an interval timer, two U-TIMER channels can be connected in cascade for a maximum count interval of up to $2^{32} \times \phi$.
Cascade connection is only available for ch0 and ch1 or ch0 and ch2.

• Block Diagram



• Register List



• U-TIMER (UTIM)

Address	bit	15	14	----------	2	1	0	Initial value
000064H (ch 0)		b15	b14		b2	b1	b0	
00006CH (ch 1)								00000000 00000000B
000074H (ch 2)		R	R		R	R	R	

UTIM contains the timer value. Use a 16-bit transfer instruction to access the register.

Reload register (UTIMR)

Address	bit	15	14	----------	2	1	0	Initial value
000064H (ch 0)		b15	b14		b2	b1	b0	
00006CH (ch 1)								00000000 00000000B
000074H (ch 2)		W	W		W	W	W	

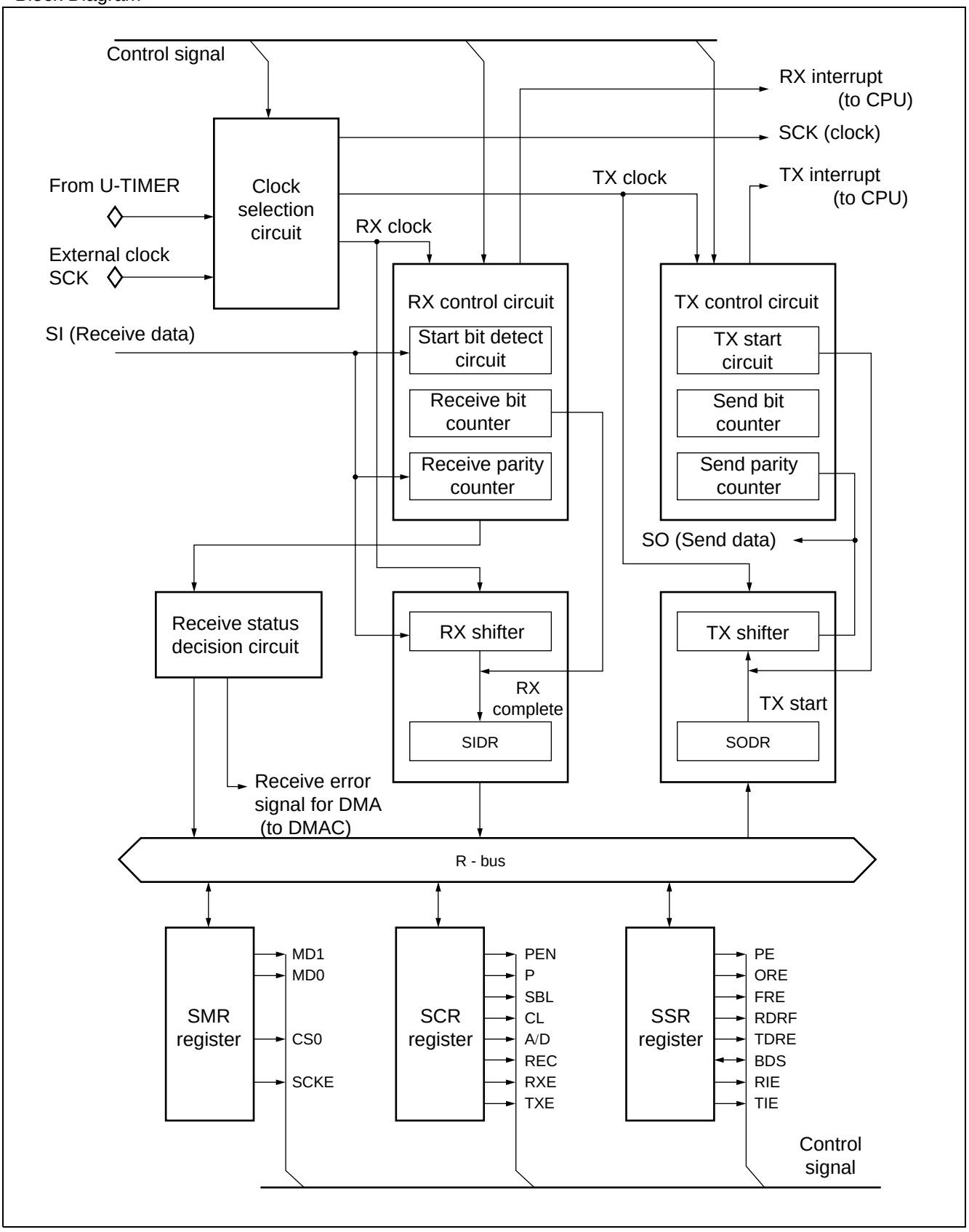
UTIMR is the register that contains the value to be reloaded to UTIM when UTIM causes an underflow. Use a 16-bit transfer instruction to access the register.

9. UART

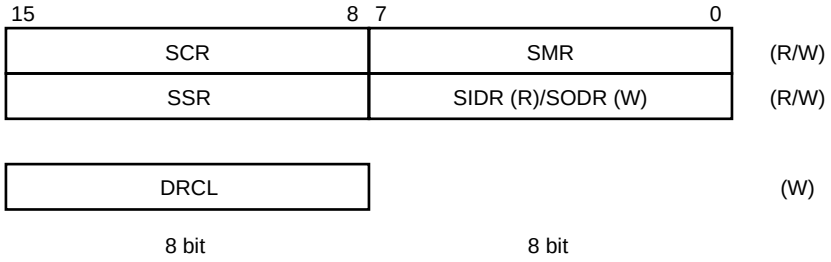
The UART is a serial I/O port for asynchronous (start-stop synchronized) or CLK synchronized transmission. The MB91301 series has three UART channels.

- **UART Features**
  - Full duplex double buffer
  - Asynchronous (start-stop synchronized) or CLK synchronized transmission
  - Supports multi-processor mode
  - Fully programmable baud rate
    The internal timer can be set to any desired baud rate (see “8. U-TIMER” description)
  - Variable baud rate can be input from an external clock.
  - Error detection functions (parity, framing, overrun)
  - Transmission signal format is NRZ
  - The interrupt can be used to initiate DMA transfer.
  - The DMAC interrupt can be cleared by writing to the DRCL register.

• Block Diagram



• Register List



Serial input data register
Serial output data register (SIDR/SODR)

bit	7	6	5	4	3	2	1	0
	D7	D6	D5	D4	D3	D2	D1	D0

Serial status register (SSR)

bit	7	6	5	4	3	2	1	0
	PE	ORE	FRE	RDRF	TDRE	BDS	RIE	TIE

Serial mode register (SMR)

bit	7	6	5	4	3	2	1	0
	MD1	MD0	—	—	CS0	—	SCKE	—

Serial control register (SCR)

bit	7	6	5	4	3	2	1	0
	PEN	P	SBL	CL	A/D	REC	RXE	TXE

DRCL register (DRCL)

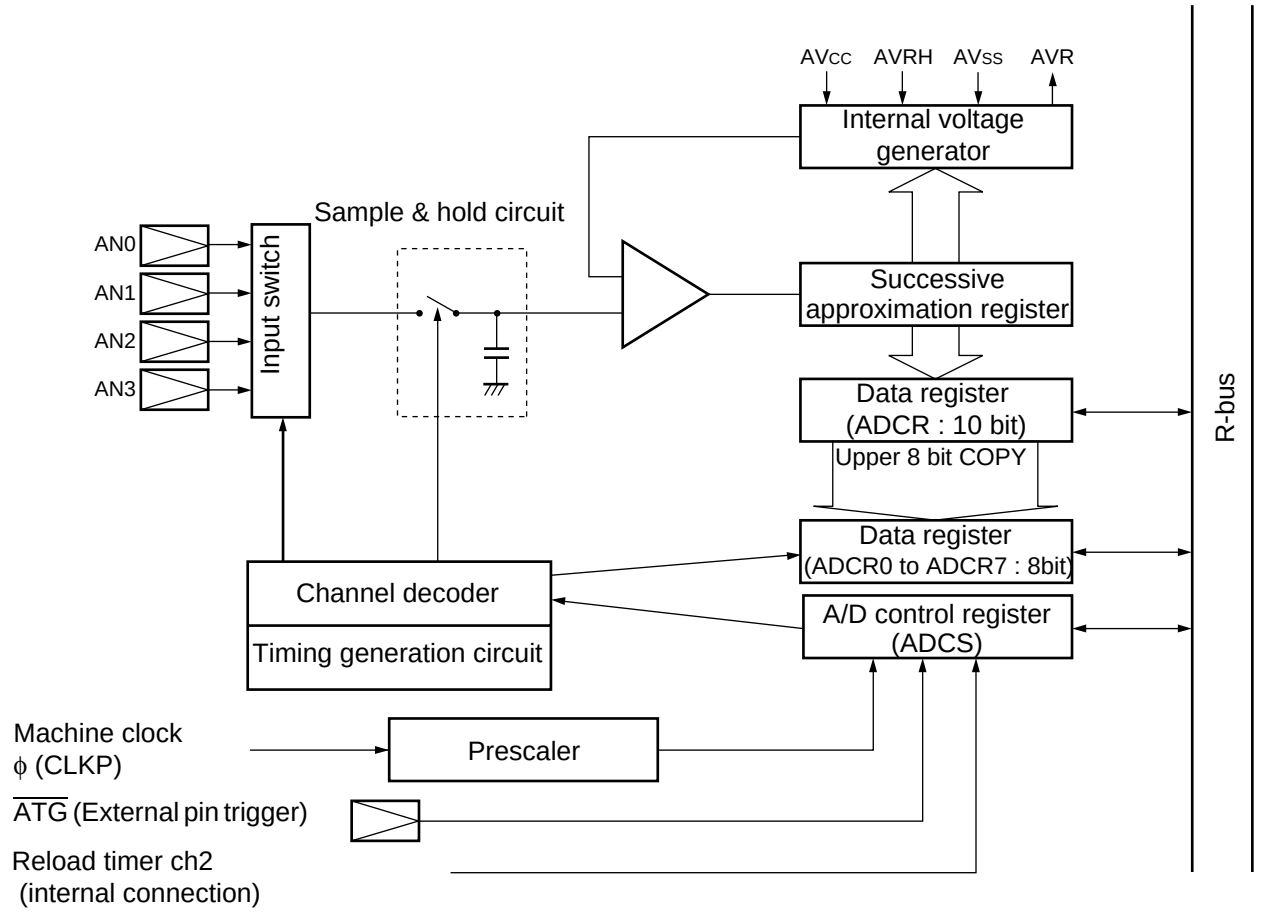
bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—

10. A/D Converter (Successive Approximation Type)

The A/D converter converts analog input voltages to digital values.

- **A/D Converter Features**
  - Peripheral clock (CLKP) 140 clock cycle
  - Minimum conversion time 4.1 µs/ch (for machine clock 34 MHz = CLKP)
  - Built-in sample & hold circuit
  - Resolution = 10-bit
  - 4 channel program-selectable analog inputs
    Single conversion mode : Convert 1 specified channel
    Scan conversion mode : Continuous conversion of multiple channels. Conversion can be specified for up to 4 channels.
  - Single, continuous, and stop conversion operation is supported.
    Single conversion mode : Convert specified channel then stop.
    Continuous conversion mode : Perform continuous conversion for the selected channel.
    Stop conversion mode : Perform conversion for one channel, then wait for the next activation trigger (synchronizes the conversion start timing)
  - DMA transfer can be initiated by an interrupt.
  - Selectable conversion activation trigger: Software, external trigger (falling edge), or reload timer (rising edge)

• Block Diagram



• Register List

Control status register (ADCS)

bit	15	14	13	12	11	10	9	8
	BUSY	INT	INTE	CRF	STS1	STS0	STRT	—

bit	7	6	5	4	3	2	1	0
	MD1	MD0	ANS2	ANS1	ANS0	ANE2	ANE1	ANE0

Data register (ADCR)

bit	15	14	13	12	11	10	9	8
	—	—	—	—	—	—	9	8

bit	7	6	5	4	3	2	1	0
	7	6	5	4	3	2	1	0

Conversion result register (ADCR0 to ADCR3)

bit	7	6	5	4	3	2	1	0
	7	6	5	4	3	2	1	0

11. DMAC (DMA Controller)

The DMA controller is used to perform DMA (direct memory access) transfer on the FR family device.
Using DMA transfer under the control of the DMA controller improves system performance by enabling data to be transferred at high speed independently of the CPU.

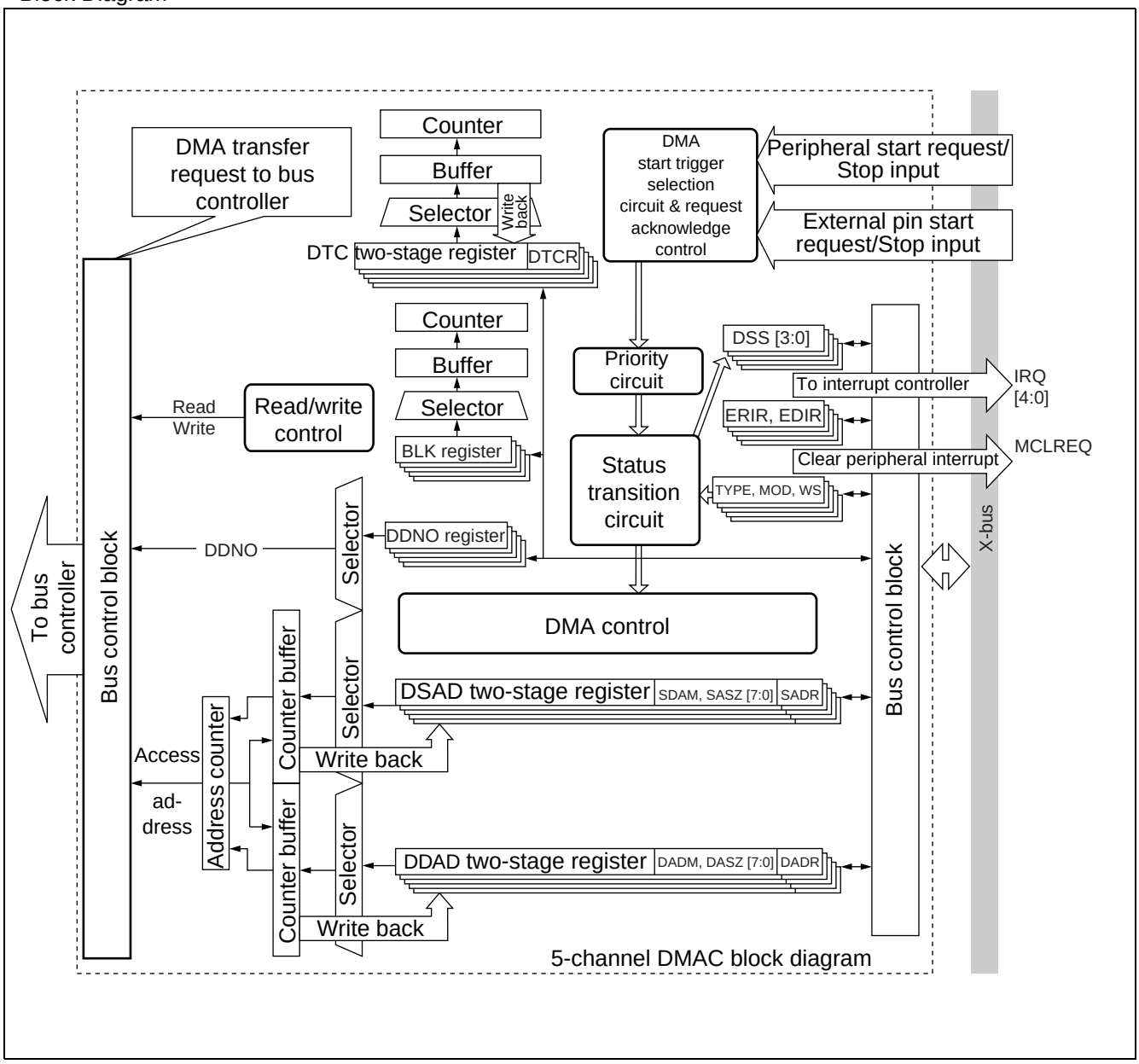
- **Hardware Configuration**
  - Independent DMA channels × 5 channels
  - 5-channel independent access control circuits
  - 32-bit address register (Supports reloading : 2 per channel)
  - 16-bit transfer count register (Supports reloading : 1 per channel)
  - 4-bit block count register (1 per channel)
  - External transfer request input pins : DREQ0, DREQ1 (ch0, ch1 only)
  - External transfer request acknowledge output pins : DACK0, DACK1 (ch0, ch1 only)
  - DMA completion output pins : DEOP0, DEOP1 (ch0, ch1 only)
  - fly-by transfer (memory to I/O , I/O to memory) (ch0, ch1 only)
  - Two-cycle transfer

- **Main Functions of the DMA Controller**
  - Supports independent data transfer for multiple channels (5 channels)

  (1) Priority order (ch 0 > ch 1 > ch 2 > ch 3 > ch 4)
  (2) Order can be reversed for ch 0 and ch 1
  (3) DMAC activation triggers
    - Input from dedicated external pin (edge detection/level detection, ch 0, ch 1 only)
    - Request from built-in peripheral (shared interrupt request, including external interrupts)
    - Software request (register write)

  (4) Transfer modes
    - Demand transfer, burst transfer, step transfer, or block transfer
      Addressing mode: Full 32-bit address (increment/decrement/fixed)
      (address increment can be in the range−255 to +255)
    - Data type : byte/half-word/word
    - Single-shot or reload operation selectable

• Block Diagram



• Register List

			bit 31 24 23 16 15 08 07 00
ch 0 control status	register A	DMACA0 0000200H	
ch 0 control status	register B	DMACB0 0000204H	
ch 1 control status	register A	DMACA1 0000208H	
ch 1 control status	register B	DMACB1 000020CH	
ch 2 control status	register A	DMACA2 0000210H	
ch 2 control status	register B	DMACB2 0000214H	
ch 3 control status	register A	DMACA3 0000218H	
ch 3 control status	register B	DMACB3 000021CH	
ch 4 control status	register A	DMACA4 0000220H	
ch 4 control status	register B	DMACB4 0000224H	

		bit 31 24 23 16 15 08 07 00
Overall control register	DMACR 0000240H	

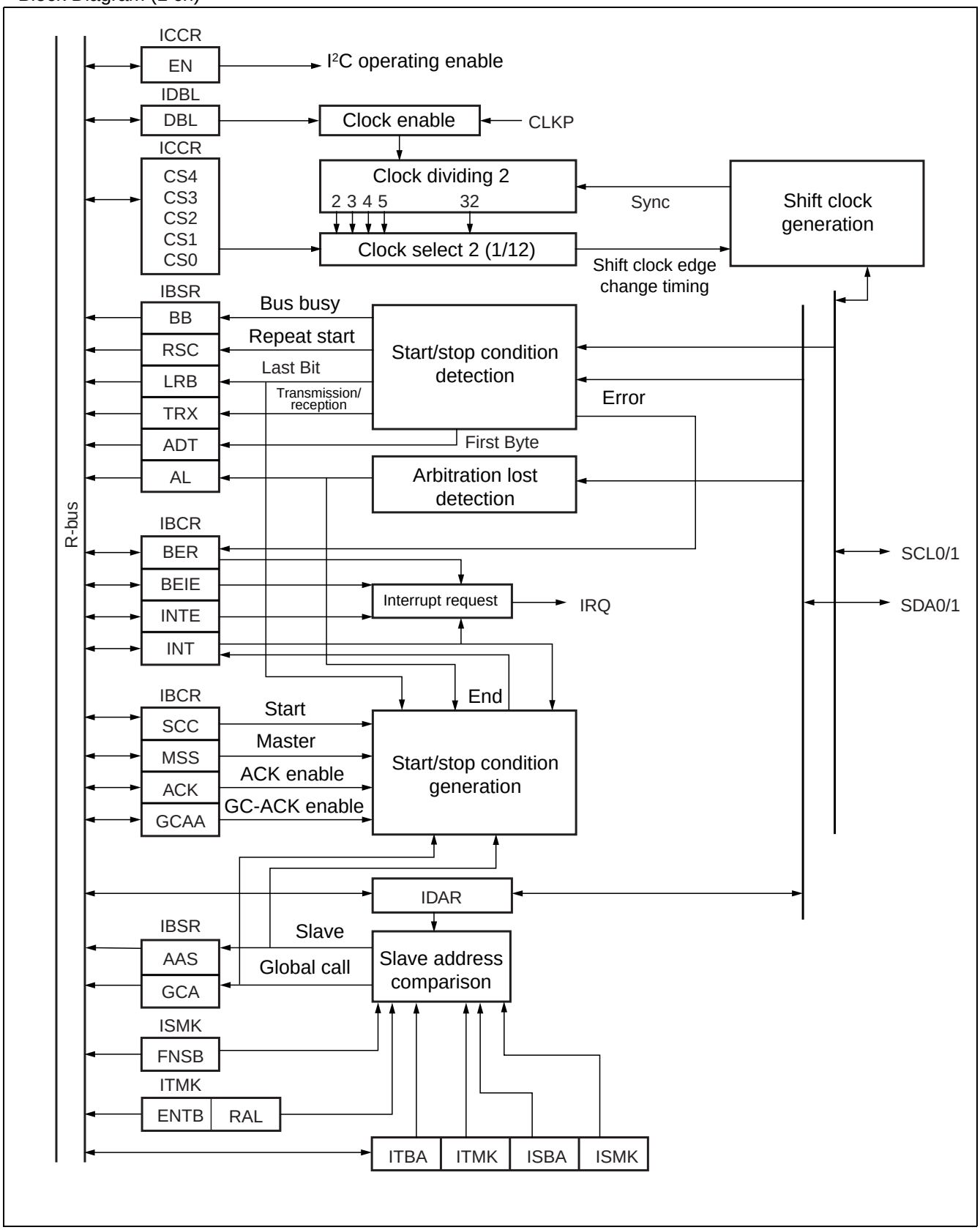
ch 0 transfer source address register	DMASA0 0001000H	
ch 0 transfer destination address register	DMADA0 0001004H	
ch 1 transfer source address register	DMASA1 0001008H	
ch 1 transfer destination address register	DMADA1 000100CH	
ch 2 transfer source address register	DMASA2 0001010H	
ch 2 transfer destination address register	DMADA2 0001014H	
ch 3 transfer source address register	DMASA3 0001018H	
ch 3 transfer destination address register	DMADA3 000101CH	
ch 4 transfer source address register	DMASA4 0001020H	
ch 4 transfer destination address register	DMADA4 0001024H	

12. I²C Interface

I²C interface is the serial I/O port that support INTER IC BUS and functions as the master/slave device on the I²C bus. It has the features below.

- Master/slave transmission and reception
- Arbitration function
- Clock synchronization
- Slave address/general call address detection function
- Forwarding direction detection function
- The function of generating/detecting repeat “START” conditions.
- Bus error detection function
- 10-bit/7-bit slave address
- Control slave address receiving at the master mode
- For support multiple slave address
- Can be interrupt at transmitting or bus mirror
- For normal mode (Max 100 Kbps) /fast mode (Max 400 Kbps)

• Block Diagram (1 ch)



• Register List

• Bus control register (IBCR0/1)

Address : 000094H/0000B4H

	15	14	13	12	11	10	9	8
	BER	BEIE	SCC	MSS	ACK	GCAA	INTE	INT
	R/W	R/W	W	R/W	R/W	R/W	R/W	R/W
Initial value = >	0	0	0	0	0	0	0	0

• Bus status register (IBSR0/1)

Address : 000095H/0000B5H

	7	6	5	4	3	2	1	0
	BB	RSC	AL	LRB	TRX	AAS	GCA	ADT
	R	R	R	R	R	R	R	R
Initial value = >	0	0	0	0	0	0	0	0

• 10-bit slave address register (ITBA0/1)

Address : 000096H/0000B6H

	15	14	13	12	11	10	9	8
	—	—	—	—	—	—	TA9	TA8
	R	R	R	R	R	R	R/W	R/W
Initial value = >	0	0	0	0	0	0	0	0

Address : 000097H/0000B7H

	7	6	5	4	3	2	1	0
	TA7	TA6	TA5	TA4	TA3	TA2	TA1	TA0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value = >	0	0	0	0	0	0	0	0

(Continued)

(Continued)

- 10-bit slave address mask register (ITMK0/1)

Address : 000098H/0000B8H

15	14	13	12	11	10	9	8
ENTB	RAL	—	—	—	—	TM9	TM8
R/W	R	R	R	R	R	R/W	R/W
0	0	1	1	1	1	1	1

Initial value = >

Address : 000099H/0000B9H

7	6	5	4	3	2	1	0
TM7	TM6	TM5	TM4	TM3	TM2	TM1	TM0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

Initial value = >

- 7-bit slave address register (ISBA0/1)

Address : 00009BH/0000BBH

7	6	5	4	3	2	1	0
—	SA6	SA5	SA4	SA3	SA2	SA1	SA0
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Initial value = >

- 7-bit slave address mask register (ISMK0/1)

Address : 00009AH/0000BAH

15	14	13	12	11	10	9	8
ENSB	SM6	SM5	SM4	SM3	SM2	SM1	SM0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	1	1	1	1	1	1	1

Initial value = >

- Data register (IDAR0/1)

Address : 00009DH/0000BDH

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Initial value = >

- Clock control register (ICCR0/1)

Address : 00009EH/0000BEH

15	14	13	12	11	10	9	8
TEST	—	EN	CS4	CS3	CS2	CS1	CS0
W	R	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	1	1	1	1	1

Initial value = >

- Clock disable register (IDBL0/1)

Address : 00009FH/0000BFH

7	6	5	4	3	2	1	0
—	—	—	—	—	—	—	DBL
R	R	R	R	R	R	R	R/W
0	0	0	0	0	0	0	0

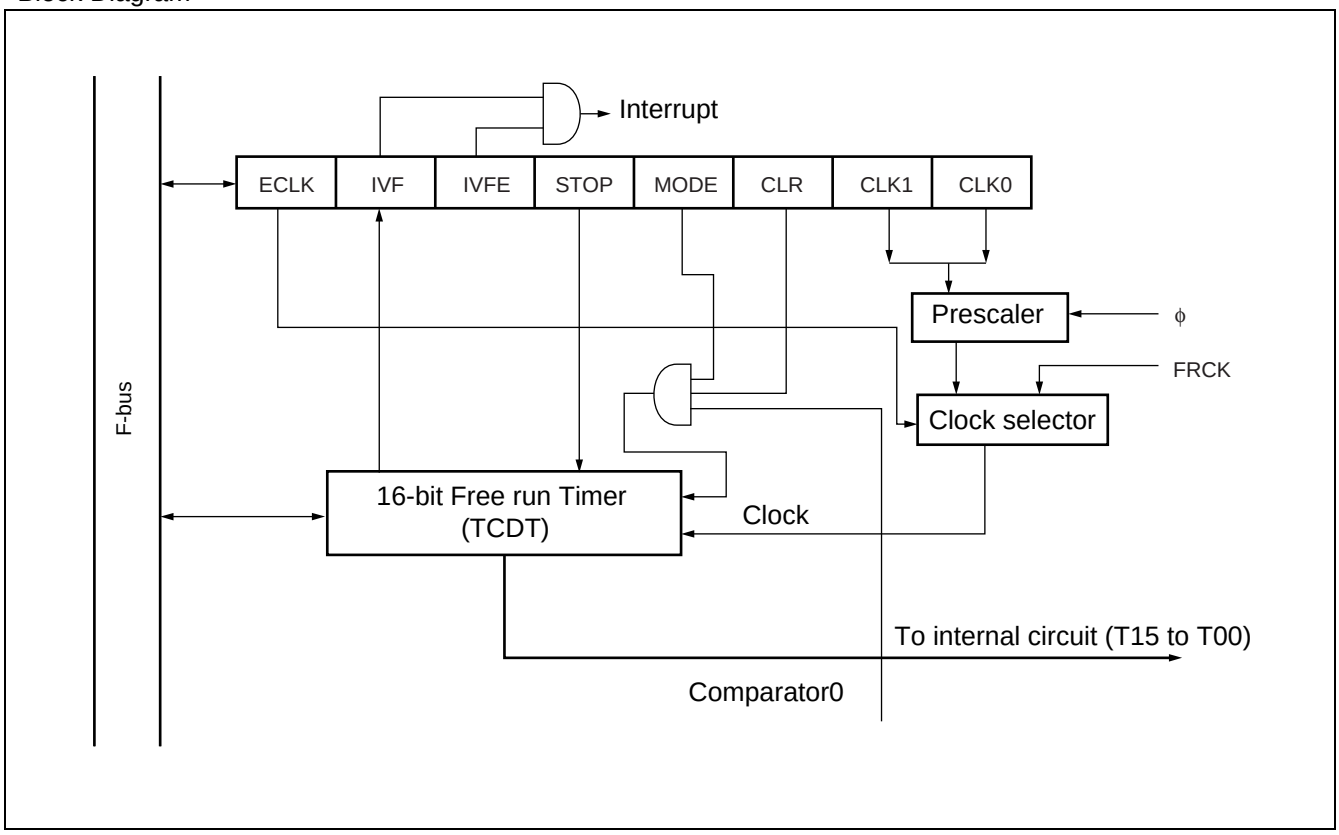
Initial value = >

13. 16 bit Free Run Timer

16-bit free-run timer consists of a 16-bit up counter and a control status register.
The timer count value is used as the base timer of output compare and input capture.

- The count clock can be selected from four different clocks.
- Can be generated the interrupt by the counter over-flow.
- Setting the mode enables initialization of counter through compare-match operation with the value of the compare clear register0 in the output compare.

•Block Diagram



•Register List

15	14	13	12	11	10	9	8
T15	T14	T13	T12	T11	T10	T9	T8

Timer data register (upper)
(TCDT)

7	6	5	4	3	2	1	0
T07	T06	T05	T04	T03	T02	T01	T00

Timer data register (lower)
(TCDT)

7	6	5	4	3	2	1	0
ECLK	IVF	IVFE	STOP	MODE	CLR	CLK1	CLK0

Timer control status register (lower)
(TCCS)

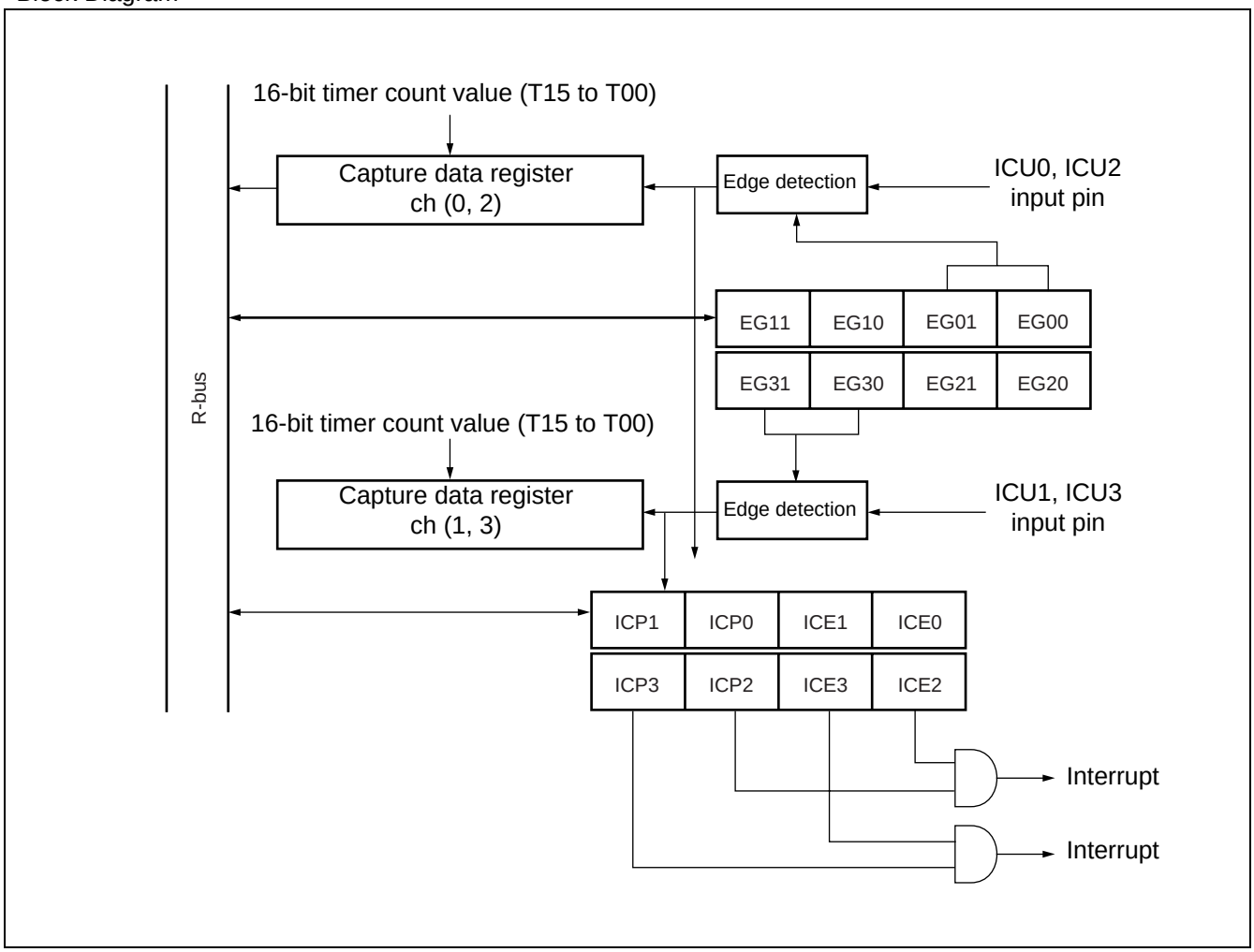
14. Input Capture

This module has a function that detects a rising edge, falling edge or both edges and holds a value of the 16-bit free-run timer in a register at the time of detection. It can also generate an interrupt when detecting an edge.

The input capture consist of input capture and control registers.
Each input capture have the corresponded external input pins.

- The valid edge of the external input can be selected from three types :
  Rising edge
  Falling edge
  Both edges
- It can generate an interrupt when it detects the valid edge of the external input.

•Block Diagram



•Register List

15	14	13	12	11	10	9	8	
CP15	CP14	CP13	CP12	CP11	CP10	CP09	CP08	Input capture data register (upper) (IPCP)

7	6	5	4	3	2	1	0	
CP07	CP06	CP05	CP04	CP03	CP02	CP01	CP00	Input capture data register (lower) (IPCP)

7	6	5	4	3	2	1	0	
ICP3	ICP2	ICE3	ICE2	EG31	EG30	EG21	EG20	Capture control register (ICS23)

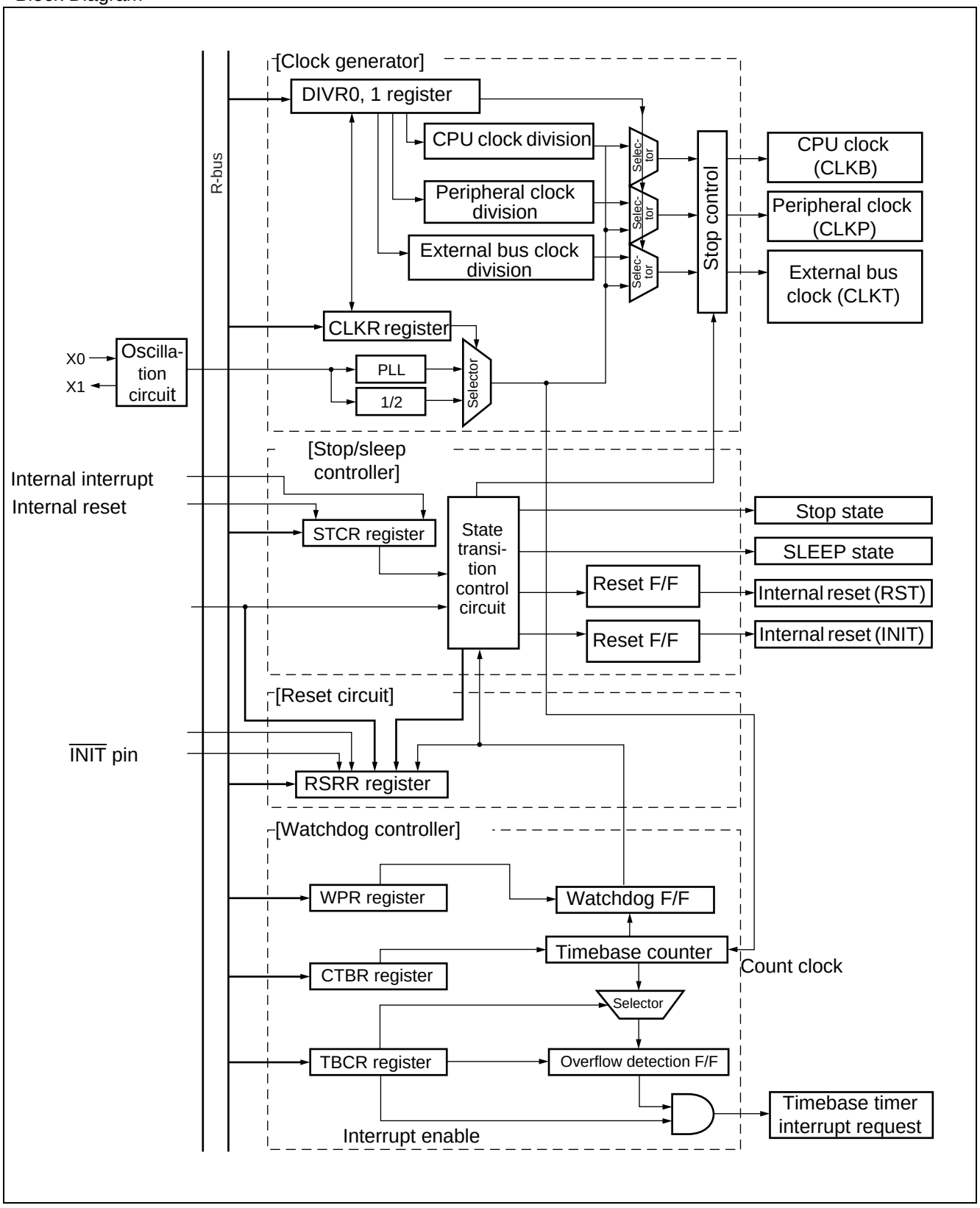
7	6	5	4	3	2	1	0	
ICP1	ICP0	ICE1	ICE0	EG11	EG10	EG01	EG00	Capture control register (ICS01)

15. Clock Generation Control

The internal operating clock is generated as follows in MB91301 series.

- Source clock selection : Selects the clock source.
- Base clock generation : The base clock is generated by dividing the source clock by 2 or using a PLL.
- Generation in each internal block : The base clock is divided to generate the operating clock for each block.

• Block Diagram



• Register List

• RSRR : Reset initiation register/Watchdog timer control register

bit	15	14	13	12	11	10	9	8
Address : 00000480H	INIT	—	WDOG	—	SRST	—	WT1	WT0
	R	R	R	R	R	R	R/W	R/W
Initial value ($\overline{\text{INIT}}$ pin)	1	0	0	0	0	0	0	0
Initial value (INIT)	–	0	–	X	X	–	0	0
Initial value (RST)	X	X	X	–	–	X	0	0

• STCR : Standby control register

bit	7	6	5	4	3	2	1	0
Address : 00000481H	STOP	SLEEP	HIZ	SRST	OS1	OS0	—	OSCD1
	R/W	R/W	R/W	R/W	R/W	R/W	—	R/W
Initial value ($\overline{\text{INIT}}$ pin)	0	0	1	1	0	0	–	1
Initial value (INIT)	0	0	1	1	X	X	–	1
Initial value (RST)	0	0	X	1	X	X	–	X

• TBCR : Timebase counter control register

bit	15	14	13	12	11	10	9	8
Address : 00000482H	TBIF	TBIE	TBC2	TBC1	TBC0	—	SYNCR	SYNCS
	R/W	R/W	R/W	R/W	R/W	—	R/W	R/W
Initial value (INIT)	0	0	X	X	X	–	0	0
Initial value (RST)	0	0	X	X	X	–	X	X

• CTBR : Timebase counter clear register

bit	7	6	5	4	3	2	1	0
Address : 00000483H	D7	D6	D5	D4	D3	D2	D1	D0
	W	W	W	W	W	W	W	W
Initial value (INIT)	X	X	X	X	X	X	X	X
Initial value (RST)	X	X	X	X	X	X	X	X

• CLKR : Clock source control register

bit	15	14	13	12	11	10	9	8
Address : 00000484H	—	PLL1S2	PLL1S1	PLL1S0	—	PLL1EN	CLKS1	CLKS0
	—	R/W	R/W	R/W	—	R/W	R/W	R/W
Initial value (INIT)	–	0	0	0	–	0	0	0
Initial value (RST)	–	X	X	X	–	X	X	X

(Continued)

(Continued)

• WPR : Watchdog reset generation delay register

bit	7	6	5	4	3	2	1	0
Address : 00000485H	D7	D6	D5	D4	D3	D2	D1	D0
	W	W	W	W	W	W	W	W
Initial value (INIT)	X	X	X	X	X	X	X	X
Initial value (RST)	X	X	X	X	X	X	X	X

• DIVR0 : Base clock division setting register 0

bit	15	14	13	12	11	10	9	8
Address : 00000486H	B3	B2	B1	B0	P3	P2	P1	P0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value (INIT)	0	0	0	0	0	0	1	1
Initial value (RST)	X	X	X	X	X	X	X	X

• DIVR1 : Base clock division setting register 1

bit	7	6	5	4	3	2	1	0
Address : 00000487H	T3	T2	T1	T0	—	—	—	—
	R/W	R/W	R/W	R/W	—	—	—	—
Initial value (INIT)	0	0	0	0	–	–	–	–
Initial value (RST)	X	X	X	X	–	–	–	–

– : Changes depending on what triggered the reset.
× : Not initialized

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

(V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Supply voltage	V_{CC}	V_{SS} – 0.5	V_{SS} + 4.0	V	*1
Analog supply voltage	AV_{CC}	V_{SS} – 0.5	V_{SS} + 4.0	V	*2
Analog reference voltage	AVRH, AVRL	V_{SS} – 0.5	AV_{CC}	V	*2
Input voltage	V_I	V_{SS} – 0.3	V_{CC} + 0.3	V	
Analog pin input voltage	V_{IA}	V_{SS} – 0.3	AV_{CC} + 0.3	V	
Output voltage	V_{OH}	V_{SS} – 0.3	V_{CC} + 0.3	V	
“L” level maximum output current	I_{OL}	—	10	mA	*3
“L” level average output current	I_{OLAV}	—	8	mA	*4
“L” level total maximum output current	ΣI_{OL}	—	100	mA	
“L” level total average output current	ΣI_{OLAV}	—	50	mA	*5
“H” level maximum output current	I_{OH}	—	–10	mA	*3
“H” level average output current	I_{OHAV}	—	–4	mA	*4
“H” level total maximum output current	ΣI_{OH}	—	–50	mA	
“H” level total average output current	ΣI_{OHAV}	—	–20	mA	*5
Power consumption	P_D	—	1000	mW	
Operating temperature	Ta	0	+70	°C	
Storage temperature	T_{STG}	–50	+150	°C	

*1 : V_{CC} must not be lower than V_{SS} – 0.3 V.

*2 : AV_{CC}, AVRH and AVRL should not exceed V_{CC}+0.3 V, including at power-on. AVRH and AVRL should not exceed AV_{CC}. Also AVRL should not exceed AVRH.

*3 : The maximum output current is the peak value for a single pin.

*4 : The average output current is the average current for a single pin over a period of 100ms.

*5 : The total average output current is the average current for all pins over a period of 100ms.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

(V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Supply voltage	V_{CC}	3.0	3.6	V	Normal operation
Analog supply voltage	AV_{CC}	V_{SS} + 3	3.6	V	
Analog reference voltage	AVRH	AV_{SS}	AV_{CC}	V	
	AVRL	AV_{SS}	AVRH	V	
Operating temperature	Ta	0	+70	°C	

<Notes on turning the power on>
The maximum power rising slope ($\Delta V/\Delta t$) must be 0.05 V/µs when the 3 V power supply is turned on.
It takes about 100 µs until the 2.5 V power supply becomes stable after the 3 V power supply becomes stable.
Keep $\overline{INIT}$ input during that interval.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

3. DC Characteristics

(V_{CC} = 3.0 V to 3.6 V , V_{SS} = AV_{SS} = 0 V, Ta = 0 °C to +70 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IH}	Non-hysteresis input pin	—	2.0	—	V_{CC} + 0.3	V	
	V_{IHS}	Hysteresis input pin	—	0.8 × V_{CC}	—	V_{CC} + 0.3	V	Hysteresis input
"L" level input voltage	V_{IL}	Non-hysteresis input pin	—	V_{SS}	—	0.8	V	
	V_{ILS}	Hysteresis input pin	—	V_{SS}	—	0.2 × V_{CC}	V	Hysteresis input
"H" level output voltage	V_{OH}	All output pins	V_{CC} = 3.0 V I_{OH} = –4.0 mA	V_{CC} – 0.4	—	V_{CC}	V	
"L" level output voltage	V_{OL}	All output pins	V_{CC} = 3.0 V I_{OL} = 4.0 mA	V_{SS}	—	0.4	V	
Input leak current (Hi-Z output leak current)	I_{LI}	All input pins*	V_{CC} = 3.6 V 0.45 V < V_I < V_{CC}	–5	—	+5	µA	
Pull-up resistance	R_{UP}	With pins Pull-up settings	V_{CC} = 3.6 V V_I = 0.45 V	10	25	120	kΩ	
Power supply current	I_{CC}	V_{CC}	f_C = 17 MHz V_{CC} = 3.6 V	—	120	150	mA	When operating at : CLKB : 68 MHz CLKT : 68 MHz CLKP : 34 MHz (×4 multiplier)
	I_{CCS}		f_C = 17 MHz V_{CC} = 3.6 V	—	50	90	mA	When sleeping at : CLKP : 34 MHz in sleep mode
	I_{CCH}		Ta = +25 °C V_{CC} = 3.6 V	—	200	700	µA	In stop mode
Input capacitance	C_{IN}	Except for V_{CC} V_{SS} AV_{CC} AV_{SS} AVRH AVR	—	—	5	15	pF	

* : Excludes X0, X1, pins with internal pull-up resistor ($\overline{INIT}$, $\overline{TRST}$), and pins with a pull-up resistor set by PCR.

4. AC Characteristics

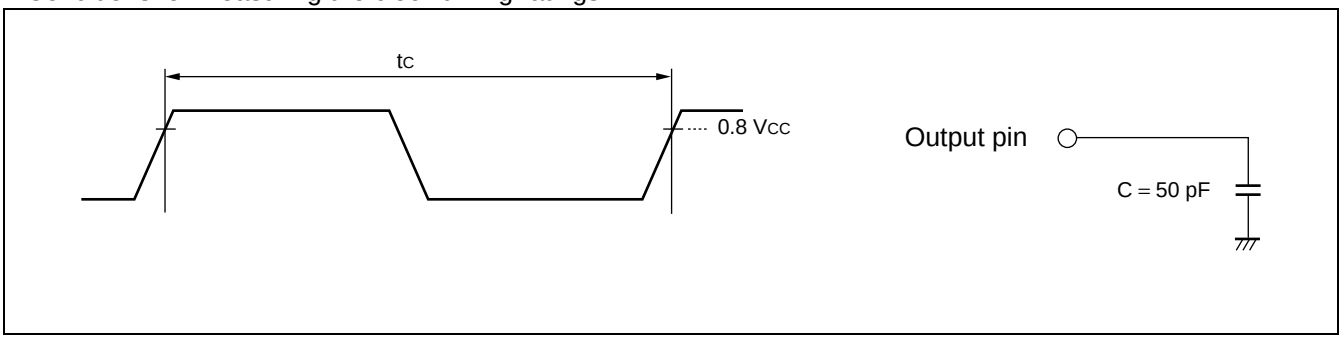
(1) Clock Timing Ratings

(V_{CC} = 3.0 V to 3.6 V , V_{SS} = AV_{SS} = 0 V, Ta = 0 °C to +70 °C)

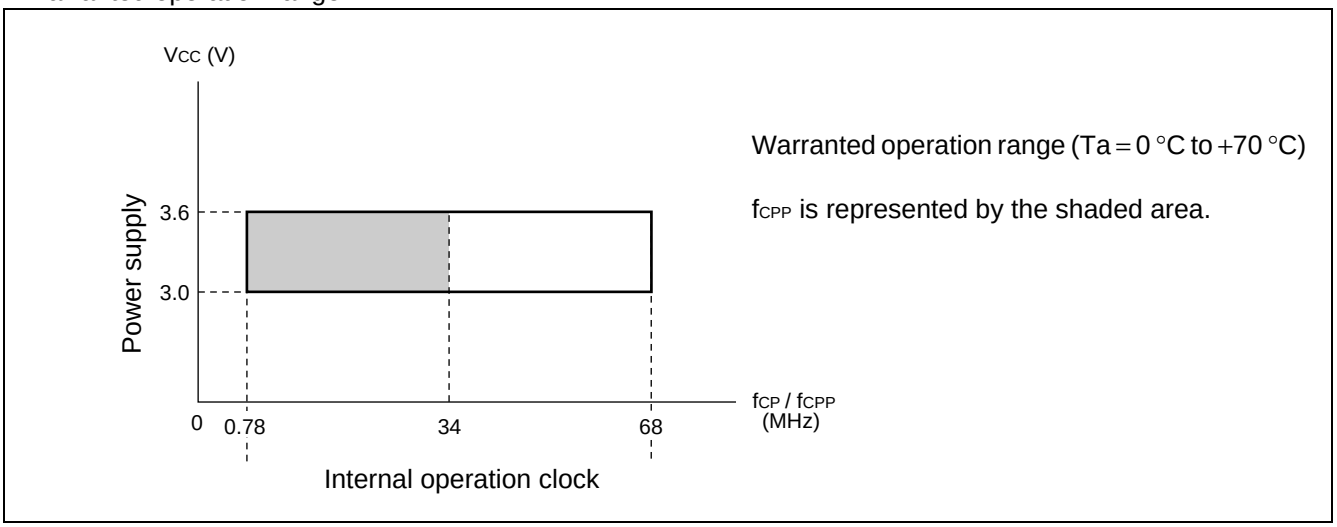
Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Clock frequency (1)	f_C	X0, X1	—	12.5	17	MHz	Using PLL (When operating at max internal frequency (68 MHz) = 17 MHz self-oscillation with ×4 PLL)
Clock cycle time	t_C	X0, X1		—	58.8	ns	
Clock frequency (2)	f_C	X0, X1	—	10	34	MHz	Self-oscillation (1/2 division input)
Internal operation clock frequency	f_{CP}	—	—	0.78*	68	MHz	CPU
	f_{CPP}			0.78*	34	MHz	Peripherals
	f_{CPT}			0.78*	68	MHz	External bus
Internal operation clock cycle time	t_{CP}	—	—	14.7	1280*	ns	CPU
	t_{CPP}			29.4	1280*	ns	Peripherals
	t_{CPT}			14.7	1280*	ns	External bus

* : Values are for minimum clock frequency (12.5 MHz) input to X0, oscillation circuit uses PLL, and gear ratio = 1/16.

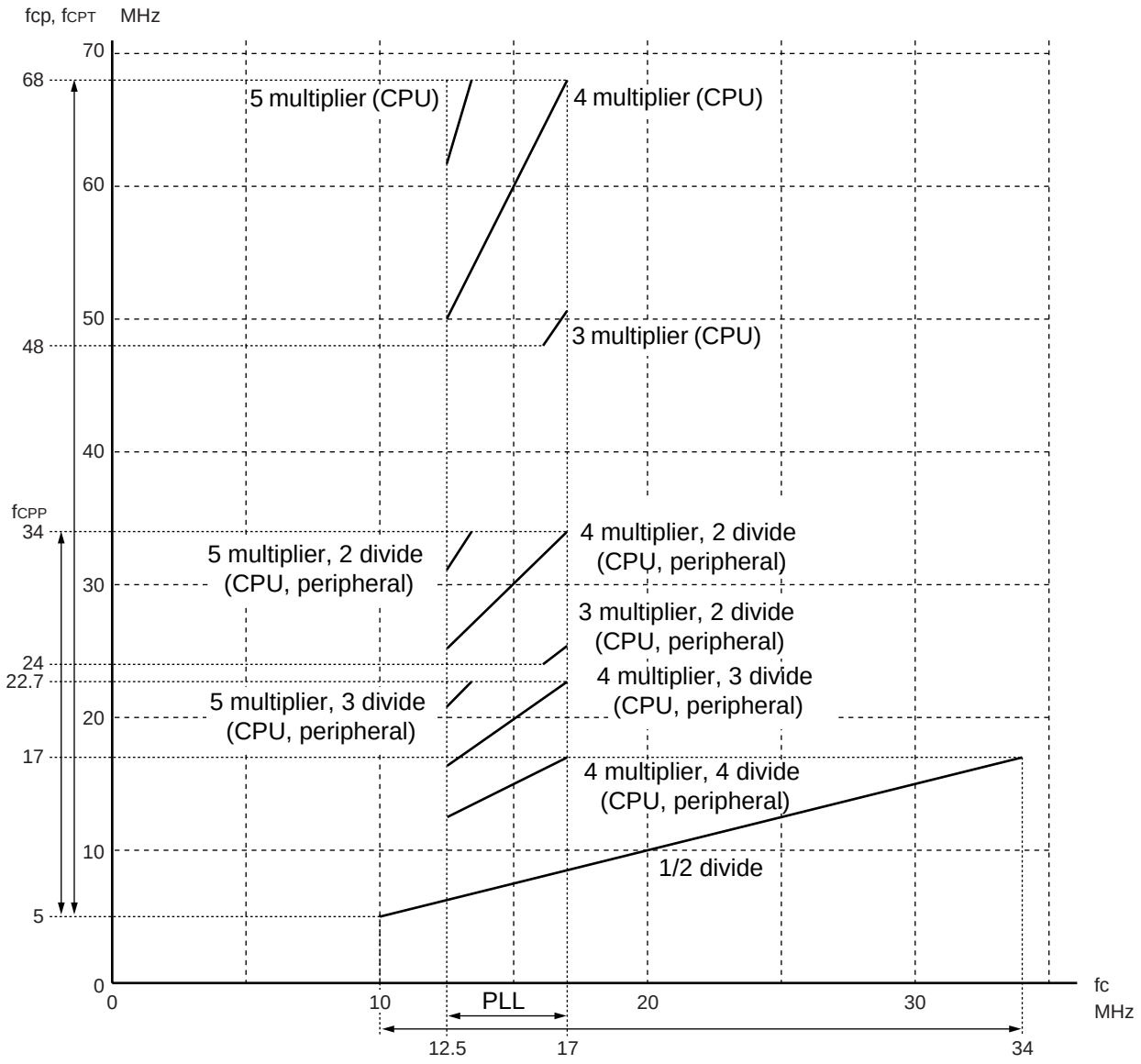
• Conditions for measuring the clock timing ratings



• Warranted operation range



• External/internal clock setting range

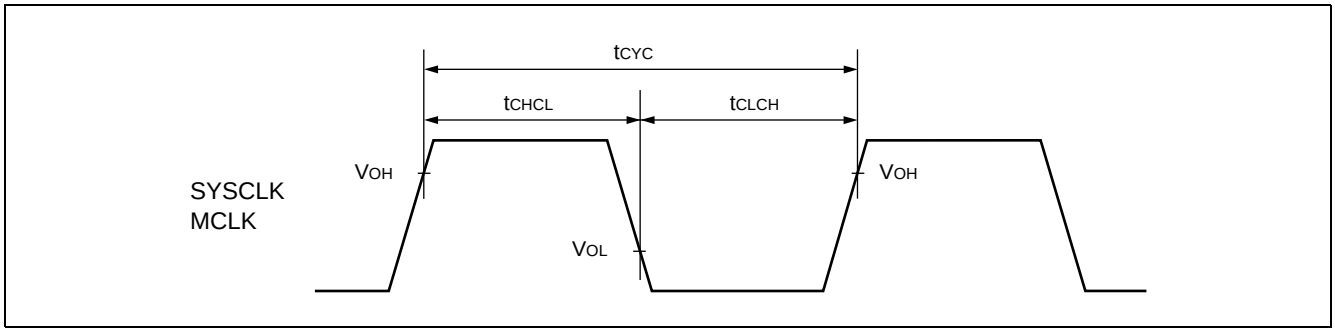


Notes : • If using the PLL, input an external clock in the range 12.5 MHz to 17 MHz.
• Allow a PLL oscillation stabilization time $>$ 300 µs.
• Set the gear ratio for the internal clock to be within the values shown in the “(1) Clock Timing Ratings” table.

(2) Clock Output Timing

(V_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = 0 °C to +70 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Cycle time	t_{CYC}	SYSCLK, MCLK	—	t_{CPT}	—	ns	*1
SYSCLK↑→SYSCLK↓	t_{CHCL}	SYSCLK, MCLK		$\frac{1}{2}t_{CYC}$–2.35	$\frac{1}{2}t_{CYC}$+2.65	ns	*2
SYSCLK↓→SYSCLK↑	t_{CLCH}	SYSCLK, MCLK		$\frac{1}{2}t_{CYC}$–2.35	$\frac{1}{2}t_{CYC}$+2.65	ns	*3



*1 : t_{CYC} is the frequency of one clock cycle after gearing.

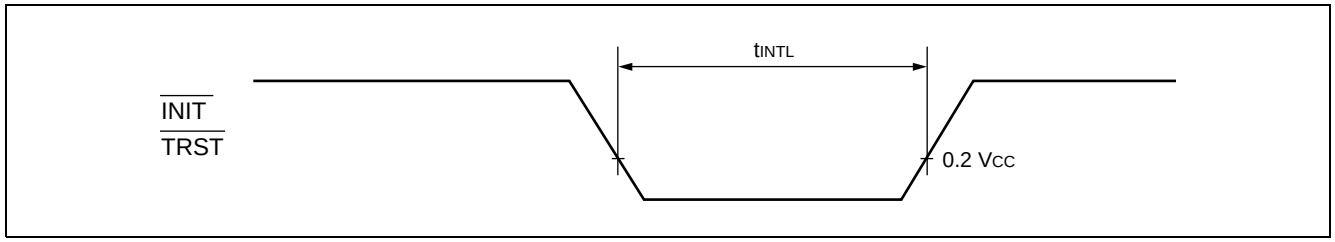
*2 : The following ratings are for the gear ratio set to × 1.
For the ratings when the gear ratio is set to between 1/2, 1/4 and 1/8, substitute 1/2, 1/4 or 1/8 for n in the following equation.
Min : (1 / 2 × 1 / n) × t_{CYC} – 2.35
Max : (1 / 2 × 1 / n) × t_{CYC} + 2.65

*3 : The following rating are for the gear ratio set to × 1.
Min : (1 / 2 × 1 / n) × t_{CYC} – 2.35
Max : (1 / 2 × 1 / n) × t_{CYC} + 2.65

(3) Reset and Tool Reset Input Ratings

(V_{CC} = 3.0 V to 3.6 V , V_{SS} = AV_{SS} = 0 V, Ta = 0 °C to +70 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
$\overline{INIT}$ input time (at power-on)	t_{INTL}	$\overline{INIT}$, $\overline{TRST}$	—	20 + α	—	µs	
$\overline{INIT}$ input time (other than at power-on)				t_{CP} × 5	—	ns	
$\overline{INIT}$ input time (recovery from stop)				20 + α	—	µs	

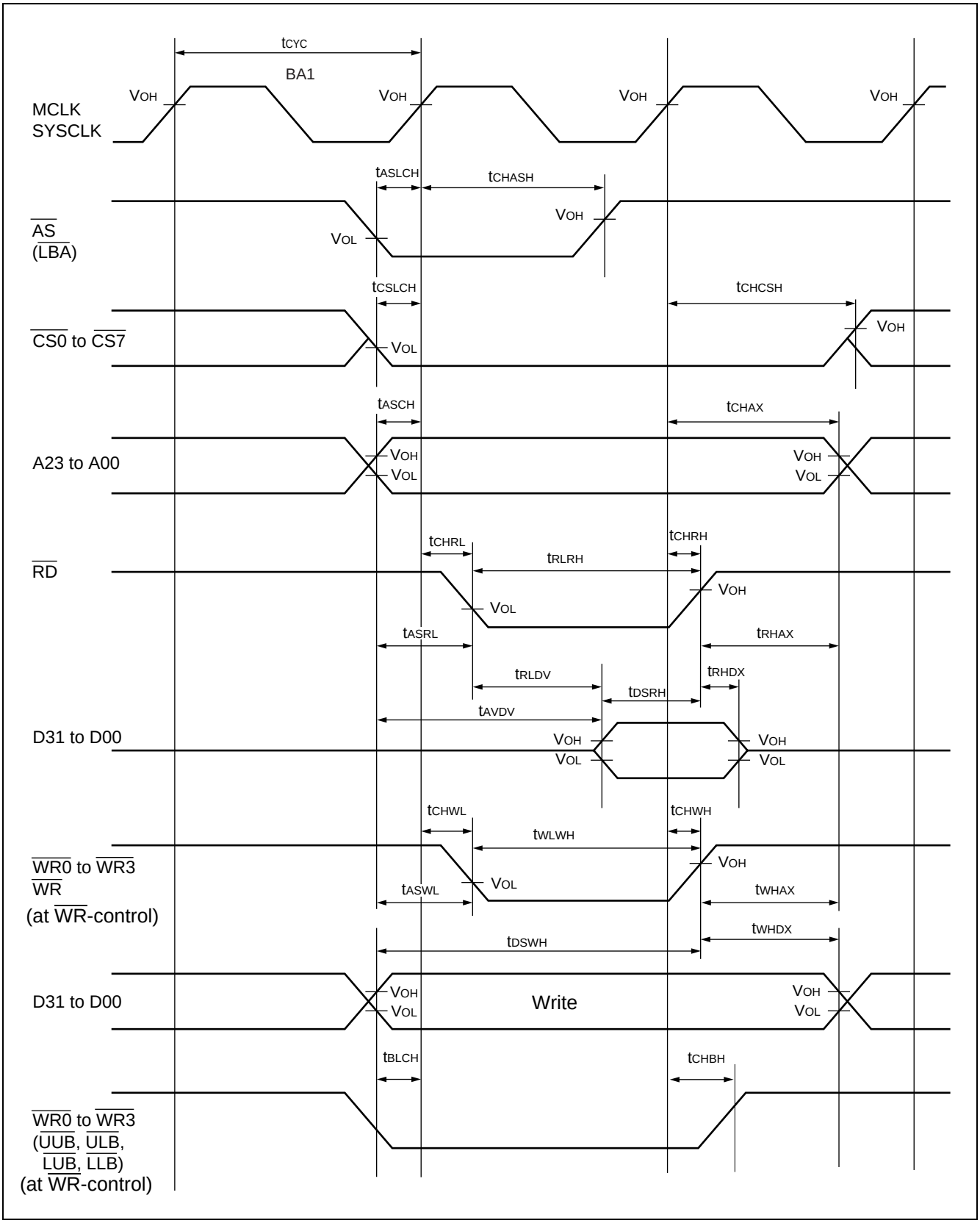


(4) Normal Bus Access Read/Write Operation

(V_{CC} = 3.0 V to 3.6 V , V_{SS} = AV_{SS} = 0 V, Ta = 0 °C to +70 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
$\overline{CS0}$ to $\overline{CS7}$ setup	t_{CSLCH}	SYSCLK, $\overline{CS0}$ to $\overline{CS7}$	—	3	—	ns	
$\overline{CS0}$ to $\overline{CS7}$ hold	t_{CHCSH}			3	t_{CYC} / 2 + 4	ns	
Address setup	t_{ASCH}	SYSCLK, A23 to A00		3	—	ns	
	t_{ASWL}	$\overline{WR0}$ to $\overline{WR3}$, A23 to A00		4	—	ns	
	t_{ASRL}	$\overline{RD}$, $\overline{A23}$ to $\overline{A00}$		5	—	ns	
Address hold	t_{CHAX}	SYSCLK, A23 to A00		3	t_{CYC} / 2 + 4	ns	
	t_{WHAX}	$\overline{WR0}$ to $\overline{WR3}$, A23 to A00		t_{CYC} / 2 – 5	—	ns	
	t_{RHAX}	$\overline{RD}$, A23 to A00		t_{CYC} / 2 – 7	—	ns	
Valid address→ Valid data input time	t_{AVDV}	A23 to A00, D31 to D00		—	3 / 2×t_{CYC} – 11	ns	*
$\overline{WR0}$ to $\overline{WR3}$ delay time	t_{CHWL}	SYSCLK, $\overline{WR}$, $\overline{WR0}$ to $\overline{WR3}$		—	6	ns	
$\overline{WR0}$ to $\overline{WR3}$ delay time	t_{CHWH}			—	6	ns	
$\overline{WR0}$ to $\overline{WR3}$ minimum pulse width	t_{WLWH}	$\overline{WR}$, $\overline{WR0}$ to $\overline{WR3}$		t_{CYC} – 5	—	ns	
Data setup →$\overline{WR}$x↑	t_{DSWH}	$\overline{WR}$, $\overline{WR0}$ to $\overline{WR3}$, D31 to D00		t_{CYC}	—	ns	
$\overline{WR}$x↑→ Data hold time	t_{WHDX}			5	—	ns	
$\overline{RD}$ delay time	t_{CHRL}	SYSCLK, $\overline{RD}$		—	6	ns	
$\overline{RD}$ delay time	t_{CHRH}			—	10	ns	
$\overline{RD}$↓→ Valid data input time	t_{RLDV}	$\overline{RD}$, D31 to D00		—	t_{CYC} – 10	ns	*
Data setup →$\overline{RD}$↑ time	t_{DSRH}			10	—	ns	
$\overline{RD}$↑→ Data hold time	t_{RHDX}			0	—	ns	
$\overline{RD}$ minimum pulse width	t_{RLRH}	$\overline{RD}$		t_{CYC} – 5	—	ns	
$\overline{AS}$ setup	t_{ASLCH}	SYSCLK, $\overline{AS}$		t_{CYC} / 2 – 6	—	ns	
$\overline{AS}$ hold	t_{CHASH}			3	—	ns	
$\overline{UUB}$/$\overline{ULB}$/$\overline{LUB}$/$\overline{LLB}$ set up	t_{BLCH}	SYSCLK, $\overline{UUB}$/ $\overline{ULB}$/$\overline{LUB}$/$\overline{LLB}$		t_{CYC} / 2 – 6	—	ns	
$\overline{UUB}$/$\overline{ULB}$/$\overline{LUB}$/$\overline{LLB}$ hold	t_{CHBH}			3	—	ns	

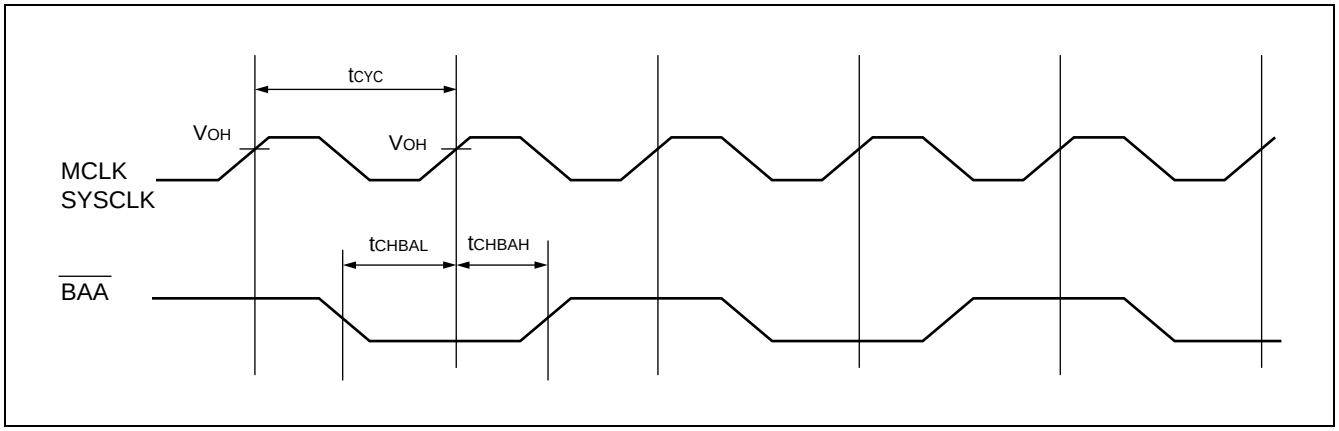
* : When the bus is delayed by automatic wait insertion or RDY input, add (t_{CYC} × number of wait cycles) to the rated values.


tCYC
BA1
MCLK
SYSCLK
VOH
tASLCH
tCHASH
AS
(LBA)
VOL
tCSLCH
tCHCSH
CS0 to CS7
tASCH
tCHAX
A23 to A00
tCHRL
tCHRH
tRLRH
RD
tASRL
tRHAX
tRLDV
tRHDX
tDSRH
tAVDV
D31 to D00
tCHWL
tCHWH
tWLWH
WR0 to WR3
WR
(at WR-control)
tASWL
tWHAX
tWHDX
tDSWH
D31 to D00
Write
tBLCH
tCHBH
WR0 to WR3
(UUB, ULB,
LUB, LLB)
(at WR-control)

(5) $\overline{\text{BAA}}$ Timing

(V_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = 0 °C to +70 °C)

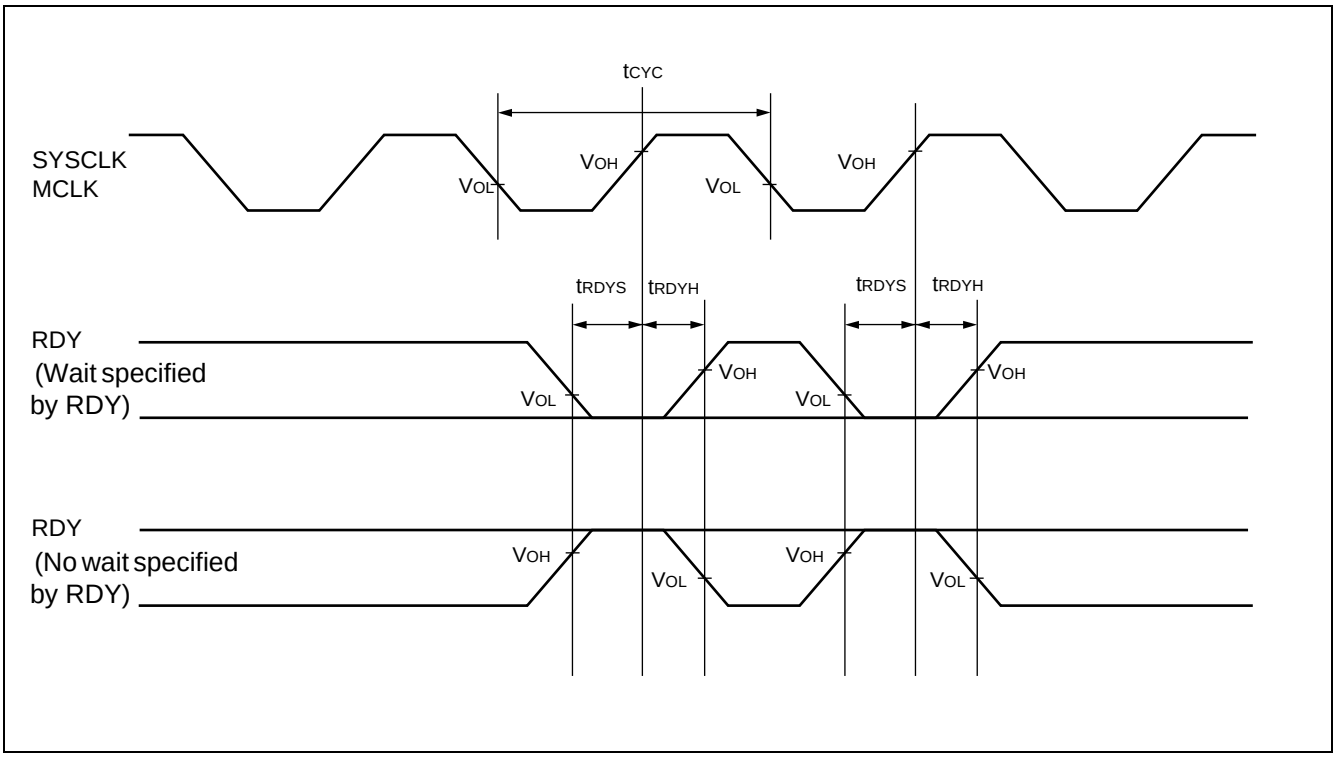
Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
$\overline{\text{BAA}}$ setup	t_{CHBAH}	SYSCLK, $\overline{\text{BAA}}$	—	t_{CYC} / 2 – 6	—	ns	
$\overline{\text{BAA}}$ hold	t_{CHBAL}			3	—	ns	



(6) Ready Input Timings

(V_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = 0 °C to +70 °C)

Parameter	Sym-bol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
RDY setup time →SYSCLK↓	t_{RDYS}	SYSCLK RDY	—	10	—	ns	
SYSCLK↓→ RDY hold time	t_{RDYH}	SYSCLK RDY	—	0	—	ns	

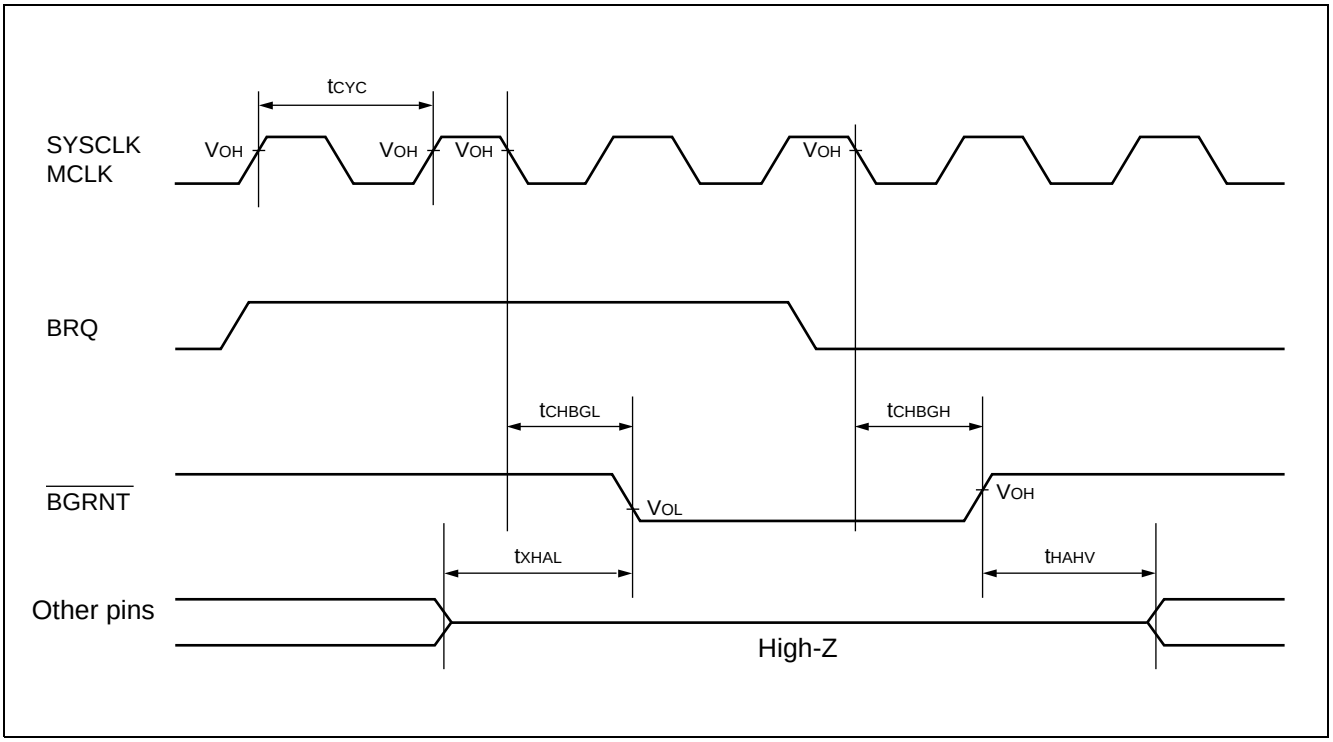


(7) Hold Timing

(V_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = 0 °C to +70 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
$\overline{BGRNT}$ delay time	t_{CHBGL}	SYSCLK, $\overline{BGRNT}$	—	—	6	ns	
$\overline{BGRNT}$ delay time	t_{CHBGH}			—	6	ns	
Pin floating →$\overline{BGRNT}$ ↓time	t_{XHAL}	$\overline{BGRNT}$, each pins		t_{CYC} – 10	t_{CYC} + 10	ns	
$\overline{BGRNT}$ ↑→pin valid time	t_{HAHV}			t_{CYC} – 10	t_{CYC} + 10	ns	

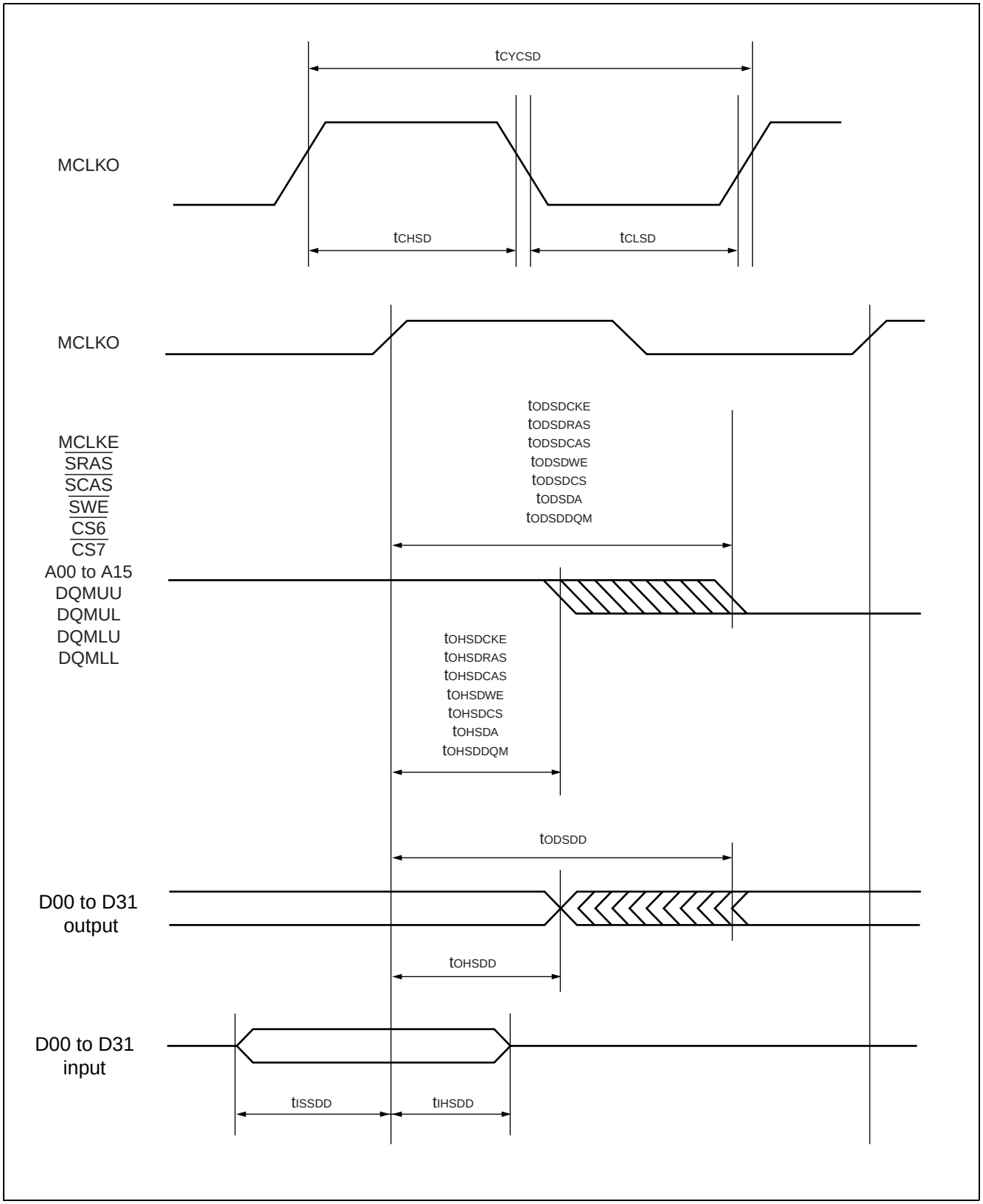
Note : The time from receiving BRQ to $\overline{BGRNT}$ changing is one cycle or more.



(8) SDRAM Timing

(V_{CC} = 3.0 V to 3.6 V , V_{SS} = AV_{SS} = 0 V, Ta = 0 °C to +70 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Output clock cycle time	t_{CYCSD}	MCLK	—	—	68	MHz	
"H" level clock pulse width	t_{CHSD}			5	—	ns	
"L" level clock pulse width	t_{CLSD}			5	—	ns	
MCLKO↑→ output delay time	$t_{ODSDCKE}$	MCLKE	—	—	11	ns	
Output hold time	$t_{OHSDCKE}$			2	—	ns	
MCLKO↑→ output delay time	$t_{ODSDRAS}$	$\overline{SRAS}$		—	11	ns	
Output hold time	$t_{OHSDRAS}$			2	—	ns	
MCLKO↑→ output delay time	$t_{ODSDCAS}$	$\overline{SCAS}$		—	11	ns	
Output hold time	$t_{OHSDCAS}$			2	—	ns	
MCLKO↑→ output delay time	t_{ODSDWE}	$\overline{SWE}$		—	11	ns	
Output hold time	t_{OHSDWE}			2	—	ns	
MCLKO↑→ output delay time	t_{ODSDCS}	$\overline{CS6}$, $\overline{CS7}$		—	11	ns	
Output hold time	t_{OHSDCS}			2	—	ns	
MCLKO↑→ output delay time	t_{ODSDA}	A00 to A15		—	11	ns	
Output hold time	t_{OHSDA}			2	—	ns	
MCLKO↑→ output delay time	$t_{ODSDDQM}$	DQMUU, DQMUL, DQMLU, DQMLL		—	11	ns	
Output hold time	$t_{OHSDDQM}$			2	—	ns	
MCLKO↑→ output delay time	t_{ODSDD}	D00 to D31		—	11	ns	
Output hold time	t_{OHSDD}			2	—	ns	
Data input setup time	t_{ISSDD}	D00 to D31	—	4	—	ns	
Data input hold time	t_{IHSDD}			2	—	ns	


tCYCSD
MCLKO
tCHSD
tCLSD
MCLKO
MCLKE
SRAS
SCAS
SWE
CS6
CS7
A00 to A15
DQMUU
DQMUL
DQMLU
DQMLL
tODSDCKE
tODSDRAS
tODSDCAS
tODSDWE
tODSDCS
tODSDA
tODSDDQM
tOHSDCKE
tOHSDRAS
tOHSDCAS
tOHSDWE
tOHSDCS
tOHSDA
tOHSDDQM
tODSDD
D00 to D31
output
tOHSDD
D00 to D31
input
tISSDD
tIHSDD

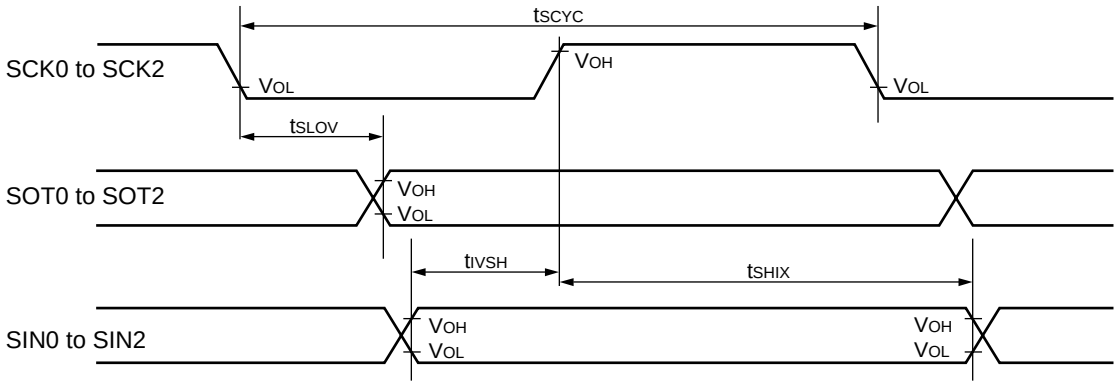
(9) UART Timing

(V_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = 0 °C to +70 °C)

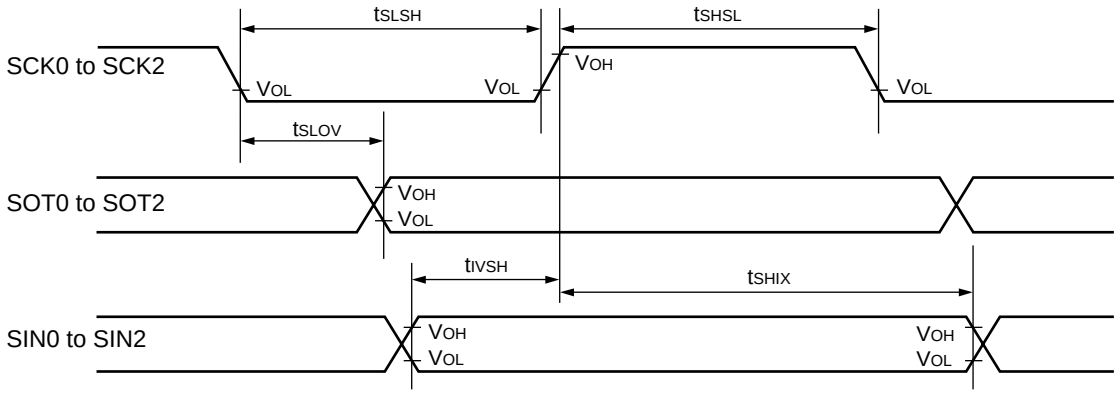
Parameter	Sym-bol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0 to SCK2	Internal shift clock mode	8 t_{CYCP}	—	ns	
SCK↓ →SO delay time	t_{SLOV}	SCK0 to SCK2, SOT0 to SOT2		–80	+80	ns	
Valid SI →SCK↑	t_{IVSH}	SCK0 to SCK2, SIN0 to SIN2		100	—	ns	
SCK↑ → valid SIN hold time	t_{SHIX}	SCK0 to SCK2, SIN0 to SIN2		60	—	ns	
Serial clock “H” pulse width	t_{SHSL}	SCK0 to SCK2	External shift clock mode	4 t_{CYCP}	—	ns	
Serial clock “L” pulse width	t_{SLSH}	SCK0 to SCK2		4 t_{CYCP}	—	ns	
SCK↓ →SOT delay time	t_{SLOV}	SCK0 to SCK2, SOT0 to SOT2		—	150	ns	
Valid SIN→SCK↑	t_{IVSH}	SCK0 to SCK2, SIN0 to SIN2		60	—	ns	
SCK↑→ valid SIN hold time	t_{SHIX}	SCK0 to SCK2, SIN0 to SIN2		60	—	ns	

Notes : • These are the AC ratings for CLK synchronous mode.
• t_{CYCP} is the peripheral clock cycle time.

• Internal shift clock mode



• External shift clock mode

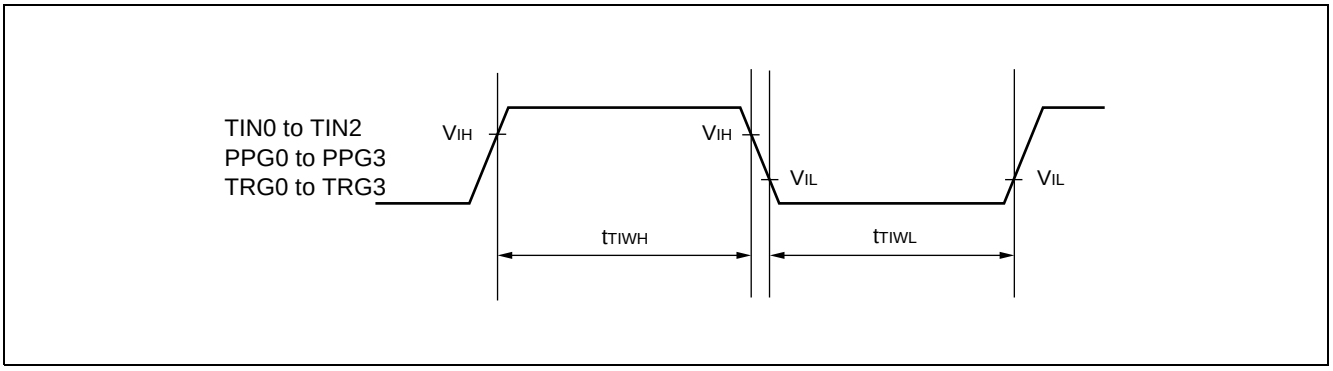


(10) Reload Timer Clock and PPG Timer Input Timings

(V_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = 0 °C to +70 °C)

Parameter	Sym-bol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH} t_{TIWL}	TIN0 to TIN2, PPG0 to PPG3, TRG0 to TRG3	—	2 t_{CYCP}*	—	ns	

* : t_{CYCP} is the peripheral clock cycle time.

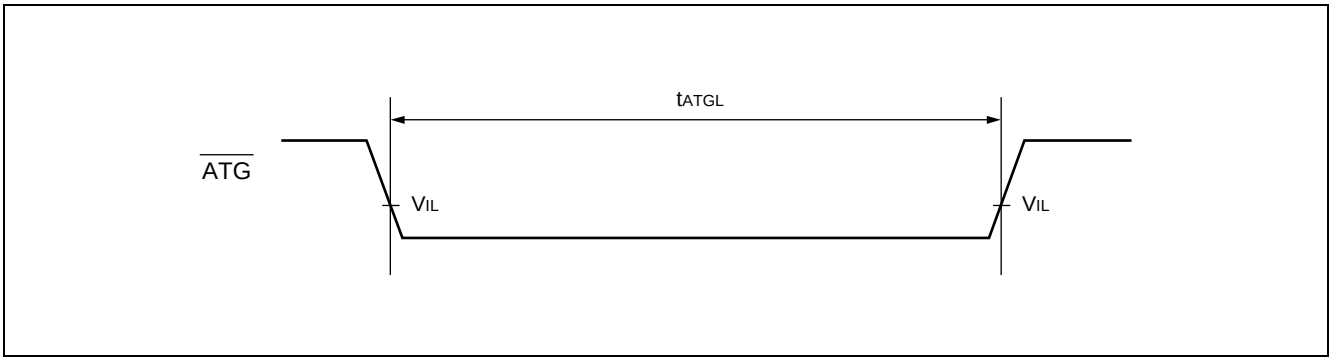


(11) Trigger Input Timing

(V_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = 0 °C to +70 °C)

Parameter	Sym-bol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
A/D activation trigger input time	t_{ATGL}	$\overline{ATG}$	—	5 t_{CYCP}*	—	ns	

* : t_{CYCP} is the peripheral clock cycle time.



(12) DMA Controller Timing

(V_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = 0 °C to +70 °C)

[For edge detection] (Block/step transfer mode, burst transfer mode)

Parameter	Sym-bol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
DREQ input pulse width	t_{DRWL}	DREQ 0, DREQ1	—	2 t_{CYC}	—	ns	

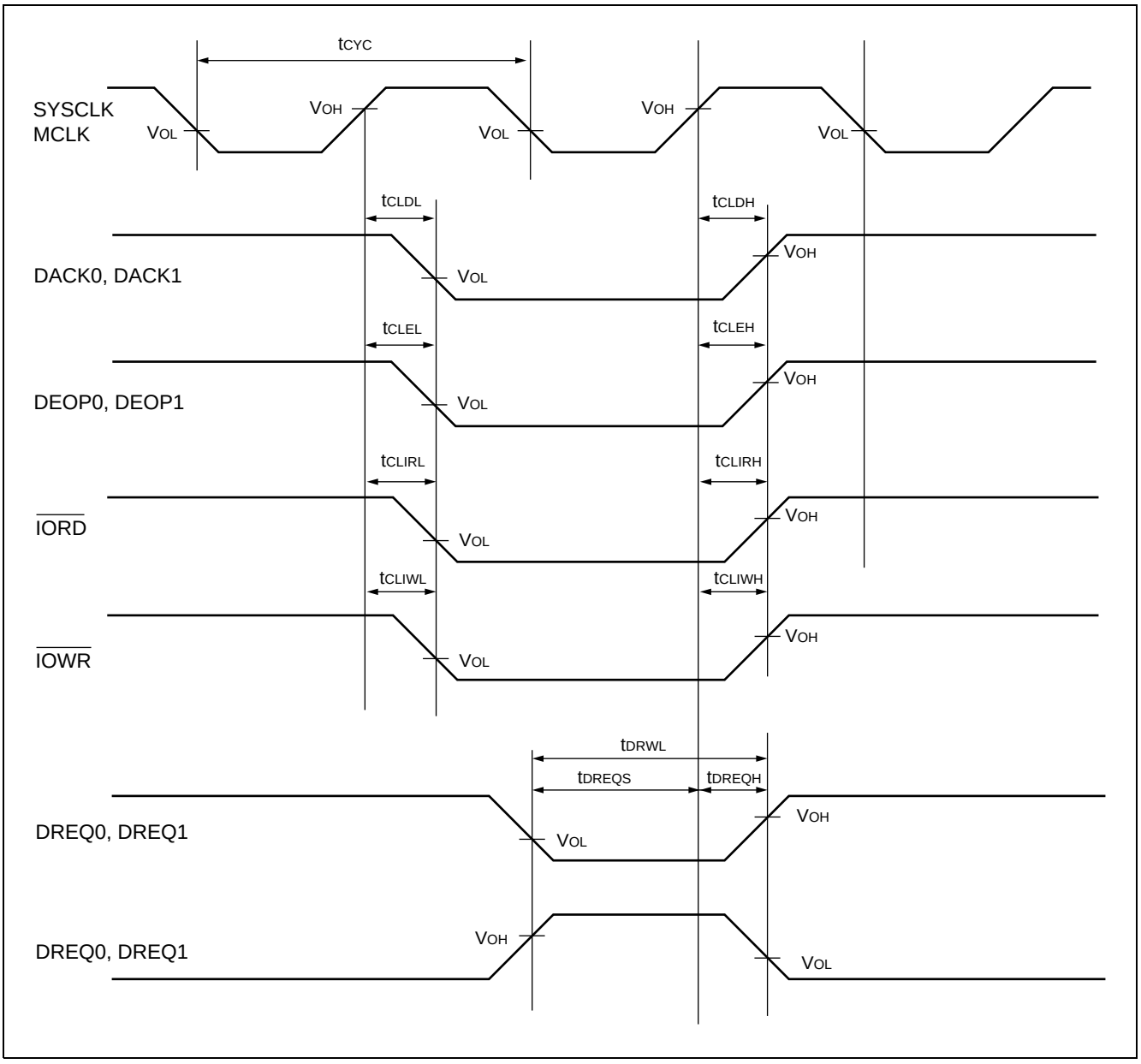
Note : When $f_{CPT} > f_{CP}$, t_{CYC} becomes same as t_{CP}.

[For level detection] (Demand transfer mode)

Parameter	Sym-bol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
DSTP setup time	t_{DREQS}	SYSCLK, DREQ 0, DREQ1	—	10	—	ns	
DSTP hold time	t_{DREQH}	SYSCLK, DREQ 0, DREQ1		0.0	—	ns	

[For all operation modes]

Parameter	Sym-bol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
DACK delay time	t_{CLDL}	SYSCLK, DACK 0, DACK1	—	—	10	ns	
	t_{CLDH}			—	10		
DEOP delay time	t_{CLEL}	SYSCLK, DEOP 0, DEOP1		—	10	ns	
	t_{CLEH}			—	10		
$\overline{IORD}$ delay time	t_{CLIRL}	SYSCLK, $\overline{IORD}$		—	10	ns	
	t_{CLIRH}			—	10		
$\overline{IOWR}$ delay time	t_{CLIWL}	SYSCLK, $\overline{IOWR}$		—	10	ns	
	t_{CLIWH}			—	10		


tCYC
SYSCLK
MCLK
VOH
VOL
VOH
VOL
VOL
tCLDL
tCLDH
DACK0, DACK1
VOH
VOL
tCLEL
tCLEH
DEOP0, DEOP1
VOH
VOL
tCLIRL
tCLIRH
IORD
VOH
VOL
tCLIWL
tCLIWH
IOWR
VOH
VOL
tDRWL
tDREQS
tDREQH
DREQ0, DREQ1
VOH
VOL
DREQ0, DREQ1
VOH
VOL

(13) I²C Timing

- At master mode operation

(A_{VCC} = V_{CC} = 3.3 ± 0.3 V, A_{VSS} = V_{SS} = 0.0 V, Ta = 0 °C to +70 °C)

Parameter	Symbol	Pin	Conditions	Typical mode		Fast mode*3		Unit	Remarks
				Min	Max	Min	Max		
SCL clock frequency	f_{SCL}	SCL0, SCL1	R = 1 kΩ, C = 50 pF*4	0	100	0	400	kHz	
"L" period of SCL clock	t_{LOW}	SCL0, SCL1		4.7	—	1.3	—	µs	
"H" period of SCL clock	t_{HIGH}	SCL0, SCL1		4.0	—	0.6	—	µs	
BUS free time between "STOP condition" and "START condition"	t_{BUS}	SDA0, SDA1		4.7	—	1.3	—	µs	
SCL↓→SDA output delay time	t_{HDDAT}	SCL0, SCL1, SDA0, SDA1		—	5 × M*1	—	5 × M*1	ns	
Setup time of "repeat START condition" SCL↑→SDA↓	t_{SUSTA}	SCL0, SCL1, SDA0, SDA1		4.7	—	0.6	—	µs	
Hold time of "repeat START condition" SDA↓→SCL↓	t_{HDSTA}	SCL0, SCL1, SDA0, SDA1		4.0	—	0.6	—	µs	After that, the first clock pulse is generated.
Setup time of "STOP condition" SCL↑→SDA↑	t_{SUSTO}	SCL0, SCL1, SDA0, SDA1		4.0	—	0.6	—	µs	
SDA data input hold time (vs. SCL↓)	t_{HDDAT}	SDA0, SDA1		2 × M*1	—	2 × M*1	—	µs	
SDA data input setup time (vs. SCL↑)	t_{SUDAT}	SDA0, SDA1		250	—	100*2	—	ns	

*1 : M = resource clock cycle (ns)

*2 : A high-speed mode I²C bus device can be used for a standard mode I²C bus system as long as the device satisfies a requirement of "$t_{SUDAT} \geq 250$ ns".
When a certain device does not extend the "L" period of the SCL signal, the next data must be output to the SDA line within 1250 ns (maximum SDA/SCL rise time + t_{SUDATA}) in which the SCL line is released.

*3 : For use at over 100 kHz, set the resource clock frequency to at least 6 MHz.

*4 : R and C represent the pull-up resistor and load capacitor of the SCL and SDA output lines.

• At slave mode operation

(A_{VCC} = V_{CC} = 3.3 ± 0.3 V, A_{VSS} = V_{SS} = 0.0 V, Ta = 0 °C to +70 °C)

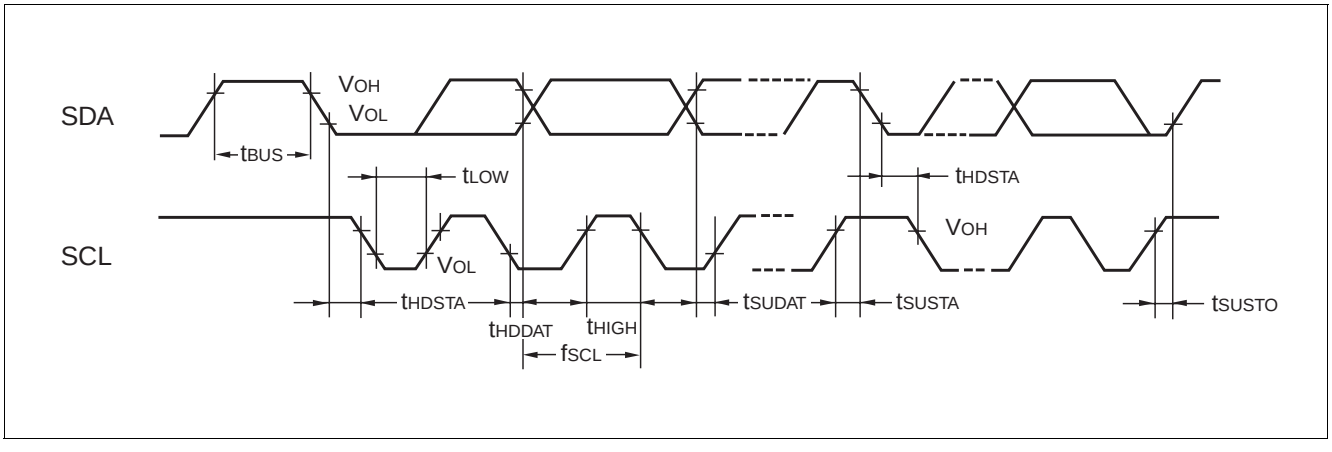
Parameter	Symbol	Pin	Conditions	Typical mode		Fast mode*3		Unit	Remarks
				Min	Max	Min	Max		
SCL clock frequency	f_{SCL}	SCL0, SCL1	R = 1 kΩ, C = 50 pF*4	0	100	0	400	kHz	
"L" period of SCL clock	t_{LOW}	SCL0, SCL1		4.7	—	1.3	—	µs	
"H" period of SCL clock	t_{HIGH}	SCL0, SCL1		4.0	—	0.6	—	µs	
BUS free time between "STOP condition" and "START condition"	t_{BUS}	SDA0, SDA1		4.7	—	1.3	—	µs	
SCL↓→SDA output delay time	t_{HDDAT}	SCL0, SCL1, SDA0, SDA1		—	5 × M*1	—	5 × M*1	ns	
Setup time of "repeat START condition" SCL↑→SDA↓	t_{SUSTA}	SCL0, SCL1, SDA0, SDA1		4.7	—	0.6	—	µs	
Hold time of "repeat START condition" SDA↓→SCL↓	t_{HDSTA}	SCL0, SCL1, SDA0, SDA1		4.0	—	0.6	—	µs	After that, the first clock pulse is generated.
Setup time of "STOP condition" SCL↑→SDA↑	t_{SUSTO}	SCL0, SCL1, SDA0, SDA1		4.0	—	0.6	—	µs	
SDA data input hold time (vs. SCL↓)	t_{HDDAT}	SDA0, SDA1		2 × M*1	—	2 × M*1	—	µs	
SDA data input setup time (vs. SCL↑)	t_{HDSTA}	SDA0, SDA1		250	—	100*2	—	ns	

*1 : M = resource clock cycle (ns)

*2 : A high-speed mode I²C bus device can be used for a standard mode I²C bus system as long as the device satisfies a requirement of "t_{SUDAT} ≥ 250 ns".
When a certain device does not extend the "L" period of the SCL signal, the next data must be output to the SDA line within 1250 ns (maximum SDA/SCL rise time + t_{SUDATA}) in which the SCL line is released.

*3 : For use at over 100 kHz, set the resource clock frequency to at least 6 MHz.

*4 : R and C represent the pull-up resistor and load capacitor of the SCL and SDA output lines.



5. Electrical Characteristics for the A/D Converter

(V_{CC} = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, AVRH = 3.0 V to 3.6 V , Ta = 0 °C to +70 °C)

Parameter	Symbol	Pin name	Value			Unit
			Min	Typ	Max	
Resolution	—	—	—	—	10	BIT
Total error	—	—	−8.5	—	+8.5	LSB
Linearity error	—	—	−3.0	—	+3.0	LSB
Differential linearity error	—	—	−2.5	—	+2.5	LSB
Zero transition error	V_{OT}	AN0 to AN3	−8.0	+0.5	+8.0	LSB
Full-scale transition error	V_{FST}	AN0 to AN3	AVRH − 8.0	AVRH − 1.5	AVRH + 8.0	LSB
Conversion time*1	—	—	4.1 µs machine clock (CLKP) 34 MHz at operating	—	—	µs
Analog port input current	I_{AIN}	AN0 to AN3	—	0.1	10	µA
Analog input voltage	V_{AIN}	AN0 to AN3	AVss	—	AVRH	V
Reference voltage	—	AVRH	AVss	—	AV_{CC}	V
Power supply current	I_A	AV_{CC}	—	0.6	2	mA
	I_{AH}*2		—	—	10	µA
Reference voltage supply current	I_R	AVRH	—	0.6	2	mA
	I_{RH}*2		—	—	10	µA
Variation between channels	—	AN0 to AN3	—	—	5	LSB

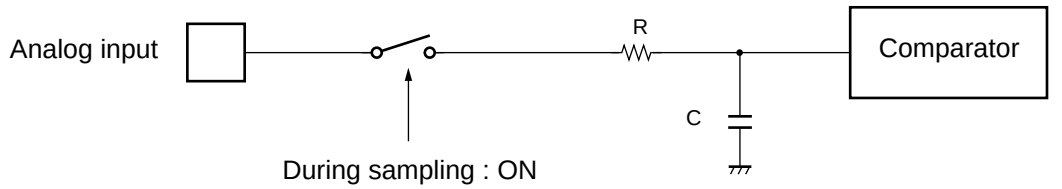
*1 : For V_{CC} = AV_{CC} = 3.0 V to 3.6 V , machine clock = 34 MHz

*2 : Current when A/D converter not operating and CPU in stop mode (V_{CC} = AV_{CC} = AVRH = 3.6 V)

Notes :
- The relative error increases as AVRH becomes smaller.
- Ensure that the output impedance of the external circuit connected to the analog input meets the following condition :
  Output impedance of external circuit < 7 kΩ
  If the output impedance of the external circuit is too high, the analog voltage sampling time may be too short.

- **About the external impedance of the analog input and its sampling time**
  - A/D converter with sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sampling and hold capacitor is insufficient, adversely affecting A/D conversion precision.

- Analog input equivalent circuit



	R	C
MB91302A	8.1 kΩ (Max)	10.0 pF (Max)

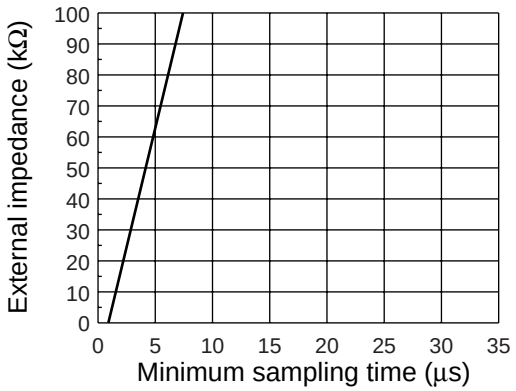
Note : The values are reference.

  - To satisfy the A/D conversion precision standard, consider the relationship between the external impedance and minimum sampling time and either adjust the resistor value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value.

- The relationship between the external impedance and minimum sampling time

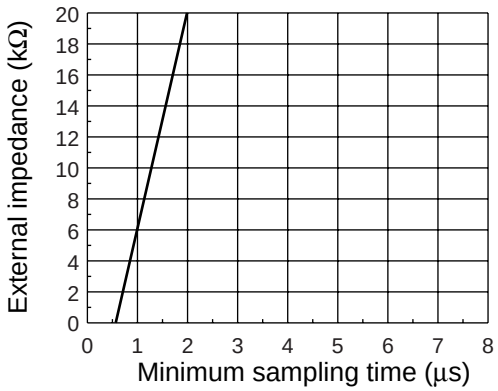
(External impedance = 0 kΩ to 100 kΩ)

MB91302A



(External impedance = 0 kΩ to 20 kΩ)

MB91302A



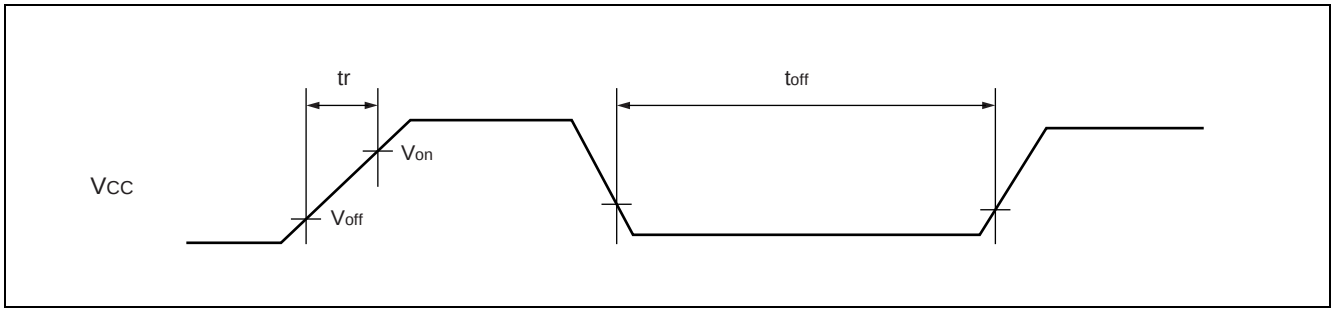
  - If the sampling time cannot be sufficient, connect a capacitor of about 0.1 µF to the analog input pin.

  - About errors

As |AVRH − AVSS| becomes smaller, values of relative errors grow larger.

6. Power-on ratings

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power rise time	tr	—	38	ms	Tilt = 0.05 V / ms
Power start time	Voff	—	0.1	V	
Power end voltage	Von	2.0	—	V	
Power shutdown time	toff	1	—	ms	



■ PIN STATUS IN EACH CPU STATE

• Terms used in the pin status list

- Input ready
  Indicates that the input function can be used.
- Input 0 fixed
  Indicates that the input level has been internally fixed to be 0 to prevent leakage when the input is released.
- Output Hi-Z
  Indicates to put the pin in a high impedance state with the pin driving transistor disabled for driving.
- Output held
  Indicates the output in the output state existing immediately before this mode is established.
  If the device enters this mode with an internal output peripheral operating or while serving as an output port, the output is performed by the internal peripheral or the port output is maintained, respectively.
- Previous state held
  When the device serves for output or input immediately before entering this mode, the device maintains the output or is ready for the input, respectively.

• Pin Status List (External bus : 32 bit bus width)

Pin no.	Port name	Specified function name	Function name	At initialization ($\overline{INIT}$)		Sleep mode	Stop mode		Bus released (BGRNT)	
				Function name	Initial value		HIZ = 0	HIZ = 1	CS shared	CS not shared
			Bus width 32 bit	Bus width 8 bit						
1 to 5	P13 to P17	D11 to D15	D11 to D15	P13 to P17	Output Hi-Z Input ready	P : Previous state held F : Output held or Hi-Z	P : Previous state held F : Output held or Hi-Z	Output Hi-Z/ input 0 fixed	Output Hi-Z	Output Hi-Z
8 to 15	P20 to P27	D16 to D23	D16 to D23	P20 to P27						
18 to 25	P30 to P37	D24 to D31	D24 to D31	D24 to D31						
28	P80	RDY	P80	P80	Output Hi-Z Input ready	P : Previous state held F : RDY input	Previous state held	Output Hi-Z/ input 0 fixed	P : Previous state held F : RDY input	P : Previous state held F : RDY input
29	P81	$\overline{BGRNT}$	P81	P81		P : Previous state held F : H output			L output	L output
30	P82	BRQ	P82	P82		P : Previous state held F : BRQ input invalid			BRQ input	BRQ input
31	P83	$\overline{RD}$	$\overline{RD}$	$\overline{RD}$	H output	P : Previous state held F : H output	Previous state held		Output Hi-Z	Previous state held
32	P84	DQMUU/$\overline{WR0}$	DQMUU/$\overline{WR0}$	DQMUU/$\overline{WR0}$						
33	P85	DQMUL/$\overline{WR1}$	DQMUL/$\overline{WR1}$	P85	F : H output					
34	P86	DQMLU/$\overline{WR2}$	DQMLU/$\overline{WR2}$	P86						
35	P87	DQMLL/$\overline{WR3}$	DQMLL/$\overline{WR3}$	P87						
36	P90	SYSCLK	SYSCLK	SYSCLK	Asserted : L output Negated : CLK output	P : Previous state held F : SYSCLK output	P : Previous state held F : H or L output	Output Hi-Z/ input 0 fixed	F : CLK output	F : CLK output
37	P91	MCLKE	MCLKE	MCLKE	H output	F : L output	F : L output	F : Output Hi-Z	Output Hi-Z	H output
38	P92	MCLK	MCLK	MCLK	Asserted : L output Negated : CLK output	P : Previous state held F : H output	P : Previous state held F : H output	F : Output Hi-Z	Output Hi-Z	F : CLK output
39	P93	—	P93	P93	Output Hi-Z Input ready	Previous state held	Previous state held	Output Hi-Z	Port Function	Port Function
40	P94	$\overline{SRAS}$/$\overline{LBA}$/ $\overline{AS}$	P94	P94	Output Hi-Z Input ready	P : Previous state held F : H output	H output	Output Hi-Z	Output Hi-Z	F : H output
41	P95	$\overline{SCAS}$/$\overline{BAA}$	P95	P95	Output Hi-Z Input ready	P : Previous state held F : H output	H output	Output Hi-Z	Output Hi-Z	H output
42	P96	$\overline{SWE}$/$\overline{WR}$	P96	P96	Output Hi-Z Input ready	P : Previous state held F : $\overline{SWE}$ output	Previous state held	Output Hi-Z/ input 0 fixed	Output Hi-Z	Previous state held
45 to 52	P40 to P47	A00 to A07	A00 to A07	A00 to A07	FF output	P : Previous state held F : Address output	The same as stated left	Output Hi-Z/ input 0 fixed	Output Hi-Z	Output Hi-Z
55 to 62	P50 to P57	A08 to A15	A08 to A15	A08 to A15						
64 to 67	P60 to P63	A16 to A19	A16 to A19	A16 to A19						
68	P64	A20/SDA0	A20	A20						
69	P65	A21/SCL0	A21	A21						
70	P66	A22/SDA1	A22	A22						
71	P67	A23/SCL1	A23	A23						
76 to 79	—	AN3 to AN0	AN3 to AN0	AN3 to AN0	input invalid	Previous state held	input invalid	input invalid	Previous state held	Previous state held
81	PG0	INT0/ICU0	PG0	PG0	Output Hi-Z Input ready	P : Previous state held F : Normal operation	P : Previous state held F : Input ready	P : Output Hi-Z F : Input ready	Normal operation	Normal operation
82	PG1	INT1/ICU1	PG1	PG1						
83	PG2	INT2/ICU2	PG2	PG2						
84	PG3	INT3/ICU3	PG3	PG3						

(Continued)

(Continued)

Pin no.	Port name	Specified function name	Function name	At initialization ($\overline{INIT}$)		Sleep mode	Stop mode		Bus released (BGRNT)	
				Function name	Initial value		HIZ = 0	HIZ = 1		
			Bus width 32 bit	Bus width 8 bit					CS shared	CS not shared
85	PG4	INT4/$\overline{ATG}$/FRCK	PG4	PG4	Output Hi-Z Input ready	P : Previous state held F : Normal operation	P : Previous state held F : Input ready	P : Output Hi-Z F : Input ready	Normal operation	Normal operation
86	PG5	INT5/SIN2	PG5	PG5						
87	PG6	INT6/SOT2	PG6	PG6						
88	PG7	INT7/SCK2	PG7	PG7						
90	PJ0	SIN0	PJ0	PJ0	Output Hi-Z Input ready	P : Previous state held F : Normal operation	Previous state held	Output Hi-Z/input 0 fixed	Normal operation	Normal operation
91	PJ1	SOT0	PJ1	PJ1						
92	PJ2	SCK0	PJ2	PJ2						
93	PJ3	SIN1	PJ3	PJ3						
94	PJ4	SOT1	PJ4	PJ4						
95	PJ5	SCK1	PJ5	PJ5						
96	PJ6	PPG0	PJ6	PJ6						
97	PJ7	TRG0	PJ7	PJ7						
98	PH0	TIN0	PH0	PH0	Output Hi-Z Input ready	P : Previous state held F : Normal operation	Previous state held	Output Hi-Z/input 0 fixed	Normal operation	Normal operation
99	PH1	TIN1/PPG3	PH1	PH1						
100	PH2	TIN2/TRG3	PH2	PH2						
103	PB0	DREQ0	PB0	PB0	Output Hi-Z Input ready	P : Previous state held F : Normal operation	Previous state held	Output Hi-Z/input 0 fixed	Normal operation	Normal operation
104	PB1	DACK0	PB1	PB1						
105	PB2	DEOP0	PB2	PB2						
106	PB3	DREQ1	PB3	PB3						
107	PB4	DACK1/TRG1	PB4	PB4						
108	PB5	DEOP1/PPG1	PB5	PB5						
109	PB6	$\overline{IOWR}$	PB6	PB6						
110	PB7	$\overline{IORD}$	PB7	PB7						
122	PA0	$\overline{CS0}$	$\overline{CS0}$	$\overline{CS0}$	H output	H output	H output	Output Hi-Z	F : SREN = 0 : H output, SREN = 1 : Output Hi-Z	F : SREN = 0 : H output, SREN = 1 : Output Hi-Z
123	PA1	$\overline{CS1}$	$\overline{CS1}$	$\overline{CS1}$						
124	PA2	$\overline{CS2}$	$\overline{CS2}$	$\overline{CS2}$						
125	PA3	$\overline{CS3}$	$\overline{CS3}$	$\overline{CS3}$						
126	PA4	$\overline{CS4}$/TRG2	$\overline{CS4}$	$\overline{CS4}$						
127	PA5	$\overline{CS5}$/PPG2	$\overline{CS5}$	$\overline{CS5}$						
128	PA6	$\overline{CS6}$	$\overline{CS6}$	$\overline{CS6}$						
129	PA7	$\overline{CS7}$	$\overline{CS7}$	$\overline{CS7}$						
132 to 139	P00 to P07	D00 to D07	D00 to D07	P00 to P07	Output Hi-Z Input ready	P : Previous state held F : Output held or Hi-Z	P : Previous state held F : Output held or Hi-Z	Output Hi-Z/input 0 fixed	Output Hi-Z	Output Hi-Z
142 to 144	P10 to P12	D08 to D10	D08 to D10	P10 to P12						

P : General-purpose port selected, F : Specified function selected

Notes :
- The bus width is determined after a mode vector fetch.
- The bus width at initialization time is 8 bits.

• Pin Status List (External bus : 16 bit bus width)

Pin no.	Port name	Specified function name	Function name	At initialization ($\overline{INIT}$)		Sleep mode	Stop mode		Bus released (BGRNT)	
				Function name	Initial value		HIZ = 0	HIZ = 1	CS shared	CS not shared
			Bus width 16 bit	Bus width 8 bit						
1 to 5	P13 to P17	D11 to D15	P13 to P17	P13 to P17	Output Hi-Z Input ready	P : Previous state held F : Output held or Hi-Z	P : Previous state held F : Output held or Hi-Z	Output Hi-Z/input 0 fixed	Output Hi-Z	Output Hi-Z
8 to 15	P20 to P27	D16 to D23	D16 to D23	P20 to P27						
18 to 25	P30 to P37	D24 to D31	D24 to D31	D24 to D31						
28	P80	RDY	P80	P80	Output Hi-Z Input ready	P : Previous state held F : RDY input	Previous state held	Output Hi-Z/input 0 fixed	P : Previous state held F : RDY input	P : Previous state held F : RDY input
29	P81	$\overline{BGRNT}$	P81	P81		P : Previous state held F : H output			L output	L output
30	P82	BRQ	P82	P82		P : Previous state held F : BRQ input invalid			BRQ input	BRQ input
31	P83	$\overline{RD}$	$\overline{RD}$	$\overline{RD}$	H output	P : Previous state held F : H output	Previous state held		Output Hi-Z	Output Hi-Z
32	P84	DQMUU/$\overline{WR0}$	DQMUU/$\overline{WR0}$	DQMUU/$\overline{WR0}$						
33	P85	DQMUL/$\overline{WR1}$	DQMUL/$\overline{WR1}$	P85	F : H output					
34	P86	DQMLU/$\overline{WR2}$	P86	P86						
35	P87	DQMLL/$\overline{WR3}$	P87	P87						
36	P90	SYSCLK	SYSCLK	SYSCLK	Asserted : L output Negated : CLK output	P : Previous state held F : SYSCLK output	P : Previous state held F : H or L output	Output Hi-Z/input 0 fixed	F : CLK output	F : CLK output
37	P91	MCLKE	MCLKE	MCLKE	H output	F : L output	F : L output	F : Output Hi-Z	Output Hi-Z	H output
38	P92	MCLK	MCLK	MCLK	Asserted : L output Negated : CLK output	P : Previous state held F : H output	P : Previous state held F : H output	F : Output Hi-Z	Output Hi-Z	F : CLK output
39	P93	—	P93	P93	Output Hi-Z Input ready	Previous state held	Previous state held	Previous state held	Output Hi-Z	Output Hi-Z
40	P94	$\overline{SRAS}$/$\overline{LBA}$/$\overline{AS}$	P94	P94	Output Hi-Z Input ready	P : Previous state held F : H output	H output	Output Hi-Z	Output Hi-Z	F : H output
41	P95	$\overline{SCAS}$/$\overline{BAA}$	P95	P95	Output Hi-Z Input ready	P : Previous state held F : H output	H output	Output Hi-Z	Output Hi-Z	H output
42	P96	$\overline{SWE}$/$\overline{WR}$	P96	P96	Output Hi-Z Input ready	P : Previous state held F : $\overline{SWE}$ output	Previous state held	Output Hi-Z/input 0 fixed	Output Hi-Z	Previous state held
45 to 52	P40 to P47	A00 to A07	A00 to A07	A00 to A07	FF output	P : Previous state held F : Address output	The same as stated left	Output Hi-Z/input 0 fixed	Output Hi-Z	Output Hi-Z
55 to 62	P50 to P57	A08 to A15	A08 to A15	A08 to A15						
64 to 67	P60 to P63	A16 to A19	A16 to A19	A16 to A19						
68	P64	A20/SDA0	A20	A20						
69	P65	A21/SCL0	A21	A21						
70	P66	A22/SDA1	A22	A22						
71	P67	A23/SCL1	A23	A23						
76 to 79	—	AN3 to AN0	AN3 to AN0	AN3 to AN0	input invalid	Previous state held	input invalid	input invalid	Previous state held	Previous state held

(Continued)

(Continued)

Pin no.	Port name	Specified function name	Function name	At initialization ($\overline{INIT}$)		Sleep mode	Stop mode		Bus released (BGRNT)	
				Function name	Initial value		HIZ = 0	HIZ = 1		
			Bus width 16 bit	Bus width 8 bit					CS shared	CS not shared
81	PG0	INT0/ICU0	PG0	PG0	Output Hi-Z Input ready	P : Previous state held F : Normal operation	P : Previous state held F : Input ready	P : Output Hi-Z F : Input ready	Normal operation	Normal operation
82	PG1	INT1/ICU1	PG1	PG1	Output Hi-Z Input ready	P : Previous state held F : Normal operation	P : Previous state held F : Input ready	P : Output Hi-Z F : Input ready	Normal operation	Normal operation
83	PG2	INT2/ICU2	PG2	PG2						
84	PG3	INT3/ICU3	PG3	PG3						
85	PG4	INT4/$\overline{ATG}$/ FRCK	PG4	PG4						
86	PG5	INT5/SIN2	PG5	PG5						
87	PG6	INT6/SOT2	PG6	PG6						
88	PG7	INT7/SCK2	PG7	PG7						
90	PJ0	SIN0	PJ0	PJ0	Output Hi-Z Input ready	P : Previous state held F : Normal operation	Previous state held	Output Hi-Z/input 0 fixed	Normal operation	Normal operation
91	PJ1	SOT0	PJ1	PJ1						
92	PJ2	SCK0	PJ2	PJ2						
93	PJ3	SIN1	PJ3	PJ3						
94	PJ4	SOT1	PJ4	PJ4						
95	PJ5	SCK1	PJ5	PJ5						
96	PJ6	PPG0	PJ6	PJ6						
97	PJ7	TRG0	PJ7	PJ7						
98	PH0	TIN0	PH0	PH0	Output Hi-Z Input ready	P : Previous state held F : Normal operation	Previous state held	Output Hi-Z/input 0 fixed	Normal operation	Normal operation
99	PH1	TIN1/PPG3	PH1	PH1						
100	PH2	TIN2/TRG3	PH2	PH2						
103	PB0	DREQ0	PB0	PB0	Output Hi-Z Input ready	P : Previous state held F : Normal operation	Previous state held	Output Hi-Z/input 0 fixed	Normal operation	Normal operation
104	PB1	DACK0	PB1	PB1						
105	PB2	DEOP0	PB2	PB2						
106	PB3	DREQ1	PB3	PB3						
107	PB4	DACK1/TRG1	PB4	PB4						
108	PB5	DEOP1/PPG1	PB5	PB5						
109	PB6	$\overline{IOWR}$	PB6	PB6						
110	PB7	$\overline{IORD}$	PB7	PB7						
122	PA0	$\overline{CS0}$	$\overline{CS0}$	$\overline{CS0}$	H output	H output	H output	Output Hi-Z	F : SREN = 0 : H output, SREN = 1 : Output Hi-Z	F : SREN = 0 : H output, SREN = 1 : Output Hi-Z
123	PA1	$\overline{CS1}$	$\overline{CS1}$	$\overline{CS1}$						
124	PA2	$\overline{CS2}$	$\overline{CS2}$	$\overline{CS2}$						
125	PA3	$\overline{CS3}$	$\overline{CS3}$	$\overline{CS3}$						
126	PA4	$\overline{CS4}$/TRG2	$\overline{CS4}$	$\overline{CS4}$						
127	PA5	$\overline{CS5}$/PPG2	$\overline{CS5}$	$\overline{CS5}$						
128	PA6	$\overline{CS6}$	$\overline{CS6}$	$\overline{CS6}$						
129	PA7	$\overline{CS7}$	$\overline{CS7}$	$\overline{CS7}$						
132 to 139	P00 to P07	D00 to D07	P00 to P07	P00 to P07	Output Hi-Z Input ready	P : Previous state held F : Output held or Hi-Z	P : Previous state held F : Output held or Hi-Z	Output Hi-Z/input 0 fixed	Output Hi-Z	Output Hi-Z
142 to 144	P10 to P12	D08 to D10	P10 to P12	P10 to P12						

P : General-purpose port selected, F : Specified function selected

Notes : • The bus width is determined after a mode vector fetch.
• The bus width at initialization time is 8 bits.

• Pin Status List (External bus : 8 bit bus width)

Pin no.	Port name	Specified function name	Function name	At initialization ($\overline{INIT}$)		Sleep mode	Stop mode		Bus released (BGRNT)	
				Function name	Initial value		HIZ = 0	HIZ = 1	CS shared	CS not shared
			Bus width 8 bit	Bus width 8 bit						
1 to 5	P13 to P17	D11 to D15	P13 to P17	P13 to P17	Output Hi-Z Input ready	P : Previous state held F : Output held or Hi-Z	P : Previous state held F : Output held or Hi-Z	Output Hi-Z/input 0 fixed	Output Hi-Z	Output Hi-Z
8 to 15	P20 to P27	D16 to D23	P20 to P27	P20 to P27						
18 to 25	P30 to P37	D24 to D31	D24 to D31	D24 to D31						
28	P80	RDY	P80	P80	Output Hi-Z Input ready	P : Previous state held F : RDY input	Previous state held	Output Hi-Z/input 0 fixed	P : Previous state held F : RDY input	P : Previous state held F : RDY input
29	P81	$\overline{BGRNT}$	P81	P81		P : Previous state held F : H output			L output	L output
30	P82	BRQ	P82	P82		P : Previous state held F : BRQ input invalid			BRQ input	BRQ input
31	P83	$\overline{RD}$	$\overline{RD}$	$\overline{RD}$	H output	P : Previous state held F : H output	Previous state held		Output Hi-Z	Output Hi-Z
32	P84	DQMUU/$\overline{WR0}$	DQMUU/$\overline{WR0}$	DQMUU/$\overline{WR0}$						
33	P85	DQMUL/$\overline{WR1}$	P85	P85	F : H output					
34	P86	DQMLU/$\overline{WR2}$	P86	P86						
35	P87	DQMLL/$\overline{WR3}$	P87	P87						
36	P90	SYSCLK	SYSCLK	SYSCLK	Asserted : L output Negated : CLK output	P : Previous state held F : SYSCLK output	P : Previous state held F : H or L output	Output Hi-Z/input 0 fixed	F : CLK output	F : CLK output
37	P91	MCLKE	MCLKE	MCLKE	H output	F : L output	F : L output	F : Output Hi-Z	Output Hi-Z	H output
38	P92	MCLK	MCLK	MCLK	Asserted : L output Negated : CLK output	P : Previous state held F : H output	P : Previous state held F : H output	F : Output Hi-Z	Output Hi-Z	F : CLK output
39	P93	—	P93	P93	Output Hi-Z Input ready	Previous state held	Previous state held	Previous state held	Output Hi-Z	Output Hi-Z
40	P94	$\overline{SRAS}$/$\overline{LBA}$/$\overline{AS}$	P94	P94	Output Hi-Z Input ready	P : Previous state held F : H output	H output	Output Hi-Z	Output Hi-Z	F : H output
41	P95	$\overline{SCAS}$/$\overline{BAA}$	P95	P95	Output Hi-Z Input ready	P : Previous state held F : H output	H output	Output Hi-Z	Output Hi-Z	H output
42	P96	$\overline{SWE}$/$\overline{WR}$	P96	P96	Output Hi-Z Input ready	P : Previous state held F : $\overline{SWE}$ output	Previous state held	Output Hi-Z/input 0 fixed	Output Hi-Z	Previous state held
45 to 52	P40 to P47	A00 to A07	A00 to A07	A00 to A07	FF output	P : Previous state held F : Address output	The same as stated left	Output Hi-Z/input 0 fixed	Output Hi-Z	Output Hi-Z
55 to 62	P50 to P57	A08 to A15	A08 to A15	A08 to A15						
64 to 67	P60 to P63	A16 to A19	A16 to A19	A16 to A19						
68	P64	A20/SDA0	A20	A20						
69	P65	A21/SCL0	A21	A21						
70	P66	A22/SDA1	A22	A22						
71	P67	A23/SCL1	A23	A23						
76 to 79	—	AN3 to AN0	AN3 to AN0	AN3 to AN0	input invalid	Previous state held	input invalid	input invalid	Previous state held	Previous state held
81	PG0	INT0/ICU0	PG0	PG0	Output Hi-Z Input ready	P : Previous state held F : Normal operation	P : Previous state held F : Input ready	P : Output Hi-Z F : Input ready	Normal operation	Normal operation

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Pin no.	Port name	Specified function name	Function name	At initialization ($\overline{INIT}$)		Sleep mode	Stop mode		Bus released (BGRNT)	
				Function name	Initial value		HIZ = 0	HIZ = 1	CS shared	CS not shared
			Bus width 8 bit	Bus width 8 bit						
82	PG1	INT1/ICU1	PG1	PG1	Output Hi-Z Input ready	P : Previous state held F : Normal operation	P : Previous state held F : Input ready	P : Output Hi-Z F : Input ready	Normal operation	Normal operation
83	PG2	INT2/ICU2	PG2	PG2						
84	PG3	INT3/ICU3	PG3	PG3						
85	PG4	INT4/$\overline{ATG}$/FRCK	PG4	PG4						
86	PG5	INT5/SIN2	PG5	PG5						
87	PG6	INT6/SOT2	PG6	PG6						
88	PG7	INT7/SCK2	PG7	PG7						
90	PJ0	SIN0	PJ0	PJ0	Output Hi-Z Input ready	P : Previous state held F : Normal operation	Previous state held	Output Hi-Z/input 0 fixed	Normal operation	Normal operation
91	PJ1	SOT0	PJ1	PJ1						
92	PJ2	SCK0	PJ2	PJ2						
93	PJ3	SIN1	PJ3	PJ3						
94	PJ4	SOT1	PJ4	PJ4						
95	PJ5	SCK1	PJ5	PJ5						
96	PJ6	PPG0	PJ6	PJ6						
97	PJ7	TRG0	PJ7	PJ7						
98	PH0	TIN0	PH0	PH0	Output Hi-Z Input ready	P : Previous state held F : Normal operation	Previous state held	Output Hi-Z/input 0 fixed	Normal operation	Normal operation
99	PH1	TIN1/PPG3	PH1	PH1						
100	PH2	TIN2/TRG3	PH2	PH2						
103	PB0	DREQ0	PB0	PB0	Output Hi-Z Input ready	P : Previous state held F : Normal operation	Previous state held	Output Hi-Z/input 0 fixed	Normal operation	Normal operation
104	PB1	DACK0	PB1	PB1						
105	PB2	DEOP0	PB2	PB2						
106	PB3	DREQ1	PB3	PB3						
107	PB4	DACK1/TRG1	PB4	PB4						
108	PB5	DEOP1/PPG1	PB5	PB5						
109	PB6	$\overline{IOWR}$	PB6	PB6						
110	PB7	$\overline{IORD}$	PB7	PB7						
122	PA0	$\overline{CS0}$	$\overline{CS0}$	$\overline{CS0}$	H output	H output	H output	Output Hi-Z	F : SREN = 0 : H output, SREN = 1 : Output Hi-Z	F : SREN = 0 : H output, SREN = 1 : Output Hi-Z
123	PA1	$\overline{CS1}$	$\overline{CS1}$	$\overline{CS1}$						
124	PA2	$\overline{CS2}$	$\overline{CS2}$	$\overline{CS2}$						
125	PA3	$\overline{CS3}$	$\overline{CS3}$	$\overline{CS3}$						
126	PA4	$\overline{CS4}$/TRG2	$\overline{CS4}$	$\overline{CS4}$						
127	PA5	$\overline{CS5}$/PPG2	$\overline{CS5}$	$\overline{CS5}$						
128	PA6	$\overline{CS6}$	$\overline{CS6}$	$\overline{CS6}$						
129	PA7	$\overline{CS7}$	$\overline{CS7}$	$\overline{CS7}$						
132 to 139	P00 to P07	D00 to D07	P00 to P07	P00 to P07	Output Hi-Z Input ready	P : Previous state held F : Output held or Hi-Z	P : Previous state held F : Output held or Hi-Z	Output Hi-Z/input 0 fixed	Output Hi-Z	Output Hi-Z
142 to 144	P10 to P12	D08 to D10	P10 to P12	P10 to P12						

P : General-purpose port selected, F : Specified function selected

Notes : • The bus width is determined after a mode vector fetch.
• The bus width at initialization time is 8 bits.

• Pin Status List (Single chip mode)

Pin no.	Port name	Specified function name	At initialization ($\overline{INIT}$)		Sleep mode	Stop mode	
			Function name	Initial value		HIZ = 0	HIZ = 1
			Bus width 8 bit	Internal ROM mode vector (MD2-0 = 000)			
1 to 5	P13 to P17	—	P13 to P17	Output Hi-Z/ Input ready	Previous state held	Previous state held	Output Hi-Z/ input 0 fixed
8 to 15	P20 to P27	—	P20 to P27				
18 to 25	P30 to P37	—	P30 to P37		Output Hi-Z	Output Hi-Z	
28	P80	—	P80		Previous state held	Previous state held	
29	P81	—	P81				
30	P82	—	P82				
31	P83	—	P83				
32	P84	—	P84				
33	P85	—	P85				
34	P86	—	P86				
35	P87	—	P87				
36	P90	—	P90				
37	P91	—	P91				
38	P92	—	P92				
39	P93	—	P93				
40	P94	SRAS	P94				
41	P95	$\overline{SCAS}$/$\overline{BAA}$	P95				
42	P96	$\overline{SWE}$/$\overline{WR}$	P96				
45 to 52	P40 to P47	—	P40 to P47		Output Hi-Z	Output Hi-Z	
55 to 62	P50 to P57	—	P50 to P57				
64 to 67	P60 to P63	—	P60 to P63		Previous state held	Previous state held	
68	P64	SDA0	P64				
69	P65	SCL0	P65				
70	P66	SDA1	P66				
71	P67	SCL1	P67				
76 to 79	—	AN0 to AN3	AN0 to AN3	Input invalid		Input invalid	input invalid
81	PG0	INT0/ICU0	PG0	Output Hi-Z/ Input ready		P : Previous state held F : Input ready Previous state held	P : Output Hi-Z F : Input ready
82	PG1	INT1/ICU1	PG1				
83	PG2	INT2/ICU2	PG2				
84	PG3	INT3/ICU3	PG3				
85	PG4	INT4/$\overline{ATG}$/FRCK	PG4				
86	PG5	INT5/SIN2	PG5				
87	PG6	INT6/SOT2	PG6				
88	PG7	INT7/SCK2	PG7				
90	PJ0	SIN0	PJ0				Output Hi-Z/ input 0 fixed
91	PJ1	SOT0	PJ1				
92	PJ2	SCK0	PJ2				
93	PJ3	SIN1	PJ3				
94	PJ4	SOT1	PJ4				
95	PJ5	SCK1	PJ5				

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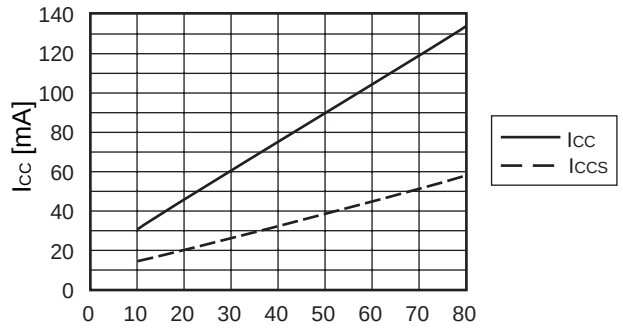
Pin no.	Port name	Specified function name	At initialization ($\overline{INIT}$)		Sleep mode	Stop mode	
			Function name	Initial value			
			Bus width 8 bit	Internal ROM mode vector (MD2-0 = 000)		HIZ = 0	HIZ = 1
96	PJ6	PPG0	PJ6	Output Hi-Z/ Input ready	Previous state held	Previous state held	Output Hi-Z/ input 0 fixed
97	PJ7	TRG0	PJ7				
98	PH0	TIN0	PH0				
99	PH1	TIN1/PPG3	PH1				
100	PH2	TIN2/TRG3	PH2				
103	PB0	—	PB0				
104	PB1	—	PB1				
105	PB2	—	PB2				
106	PB3	—	PB3				
107	PB4	TRG1	PB4				
108	PB5	PPG1	PB5				
109	PB6	—	PB6				
110	PB7	—	PB7				
122	PA0	—	PA0				
123	PA1	—	PA1				
124	PA2	—	PA2				
125	PA3	—	PA3				
126	PA4	TRG2	PA4				
127	PA5	PPG2	PA5				
128	PA6	—	PA6				
129	PA7	—	PA7				
132 to 139	P00 to P07	—	P00 to P07				
142 to 144	P10 to P12	—	P10 to P12				

P : General-purpose port selected, F : Specified function selected

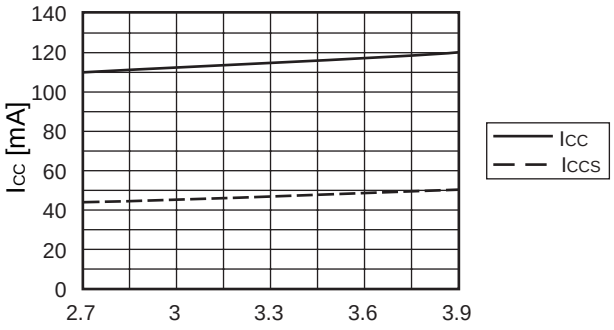
Notes :
- The bus width is determined after a mode vector fetch.
- The bus width at initialization time is 8 bits.

■ EXAMPLE CHARACTERISTICS

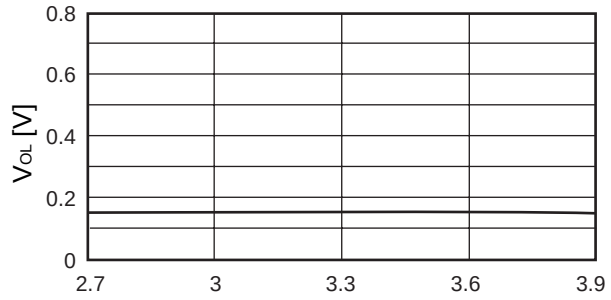
I_{CC} – Internal frequency (PLL On)
External V_{CC} = 3.6 V, Ta = + 25 °C



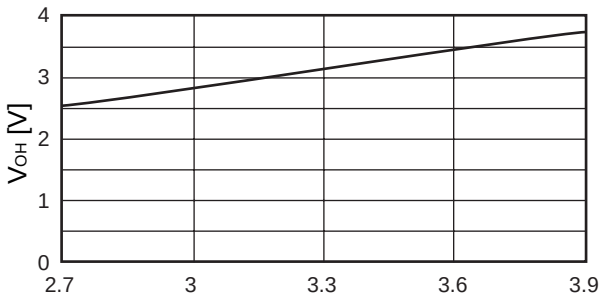
I_{CC} – External V_{CC} (PLL On)
Internal frequency = 68 MHz, Ta = + 25 °C



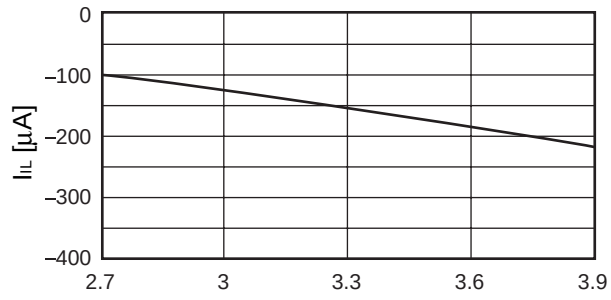
V_{OL} – External V_{CC}
Internal frequency = 68 MHz, Ta = + 25 °C



V_{OH} – External V_{CC}
Internal frequency = 68 MHz, Ta = + 25 °C



I_{IL} – External V_{CC}
Internal frequency = 68 MHz, Ta = + 25 °C



■ ORDERING IMFORMATION

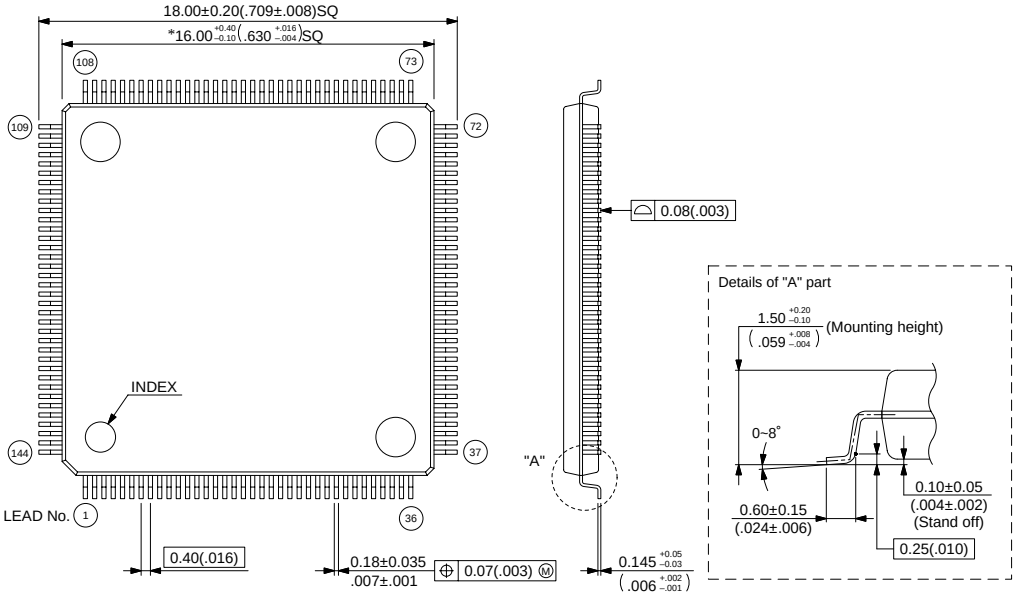
Part No.	Package	Remarks
MB91302APFF-G-001-BNDE1	144-pin Plastic LQFP (FPT-144P-M12)	Without ROM
MB91302APFF-G-010-BNDE1		Optional real time OS internal model
MB91302APFF-G-020-BNDE1		Built-in IPL (Internal Program Loader) version
MB91302APFF-G-XXX-BNDE1		User ROM version
MB91V301A-RDK01*	179-pin Ceramic PGA (PGA-179C-A03)	Development pack for MB91302A real time OS internal model (MB91V301A and CD-ROM for development)
MB91V301A	179-pin Ceramic PGA (PGA-179C-A03)	Evaluation chip

* : In case of buying this product, it is necessary to make a contract with “MB91V301A-RDK01 Fujitsu software product use contract”.

■ PACKAGE DIMENSIONS

144-pin Plastic LQFP
(FPT-144P-M12)

Note 1) * : These dimensions include resin protrusion.
Resin protrusion is +0.25 (.010) Max (each side) .
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches)
Note : The values in parentheses are reference values.

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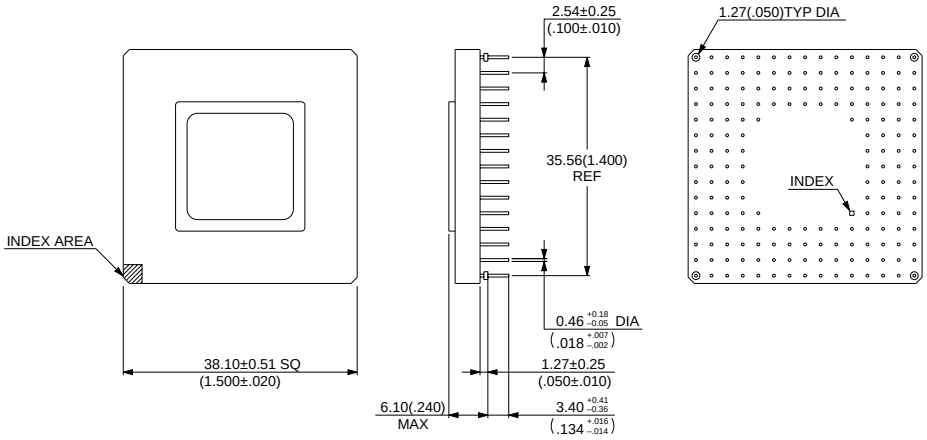
179-pin Ceramic PGA
(PGA-179C-A03)



Dimensions in mm (inches)
Note : The values in parentheses are reference values.

The information for microcontroller supports is shown in the following homepage.
http://www.fujitsu.com/global/services/microelectronics/product/micom/support/index.html

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