

32-bit Microcontroller

CMOS

FR60 MB91305

MB91305

■ DESCRIPTION

MB91305 is a single-chip microcontroller that has a 32-bit high-performance RISC CPU as well as built-in I/O resources for embedded controllers requiring high-performance and high-speed CPU processing.

The FR family is the most suitable for embedded applications, for example, DVD player, printer, TV, and PDP control, that require a high level of CPU processing power.

MB91305 is an FR60 model that is based on the FR30/40 of CPUs. It has enhanced bus access and is optimized for high-speed use.

■ FEATURES

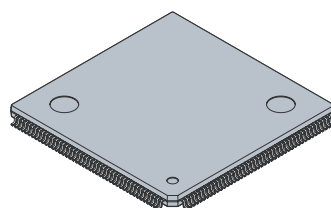
1. FR CPU

- 32-bit RISC, load/store architecture, 5 stages pipeline
- With USB function (MOD = 0000_B) : operating frequency of 64 MHz [original oscillation at 48 MHz] 48 MHz / 3-divided × 4 multiplication

(Continued)

■ PACKAGE

176-pin plastic LQFP



(FPT-176P-M07)

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- With no USB function (MOD = 0010_B) : operating frequency of 64 MHz [original oscillation at 16 MHz] 16 MHz × 4 multiplication
- 16-bit fixed-length instructions (basic instructions) , one instruction per cycle
- Memory-to-memory transfer, bit processing, instructions including barrel shift, etc. : instructions appropriate for embedded applications
- Function entry and exit instructions, multi load/store instructions of register contents : instructions compatible with high-level languages
- Register interlock to facilitate assembly-language coding
- Built-in multiplier/instruction-level support
 - Signed 32-bit multiplication : 5 cycles
 - Signed 16-bit multiplication : 3 cycles
- Interrupts (saving of PC and PS) : 6 cycles, 16 priority levels
- Harvard architecture enabling simultaneous execution of both program access and data access
- 4-word queues in the CPU provided to add an instruction prefetch function
- Instructions compatible with the FR family

2. Bus Interface

This bus interface is used for external bus and internal macro USB function.

- Maximum operating frequency of 32 MHz
- 16-bit data input-output
- Totally independent 8-area chip select outputs that can be defined in the minimum units of 64K bytes. The $\overline{CS2}$ and $\overline{CS3}$ areas are reserved as shown below. $\overline{CS0}$, $\overline{CS1}$, and $\overline{CS4}$ to $\overline{CS7}$ can be used only.
 - $\overline{CS2}$ area : USB function
 - $\overline{CS3}$ area : Unused
- Basic bus cycle (2 cycles)
- Automatic wait cycle generator that can be programmed for each area and can insert waits because $\overline{CS2}$ and $\overline{CS3}$ are reserved, the setting is fixed.
- 24-bit address can be fully outputted
- 8- and 16-bit data I/O
- Prefetch buffer installed
- Unused data and address pins can be used as general-purpose I/O and resource function.
- Support of interfaces for various memory modules
 - Asynchronous SRAM, asynchronous ROM/Flash memory
 - Page-mode ROM/Flash memory (a page-size of 1, 2, 4, or 8 can be selected)
 - Burst-mode ROM/Flash memory (MBM29BL160D/161D/162D etc.)
 - SDRAM (or FCRAM type, CAS Latency1 to Latency8, 2/4 bank product)
 - Address/data multiplexed bus (8-bit/16-bit width only)
- Basic bus cycle : 2 cycles
- Automatic wait cycle generator (Max 15 cycles) that can be programmed for each area
- External wait cycles due to RDY input
- Endian setting of byte ordering (big/little)

Note : $\overline{CS0}$ area is only big endian.

- Write disable setting (read only area)
- Enable/disable set of capturing to the built-in cache
- Enable/disable set of prefetch function
- External bus arbitration using BRQ and \overline{BGRNT} is enabled

3. Built-in Memory

64K bytes RAM of built-in F-bus

4. Instruction Cache Memory

- Instruction cache : 4K bytes
- 2 way set associative
- 128 block/way, 4 entry (4 words) /block
- Lock function allows specific program codes to stay resident in cache.
- Instruction RAM function : A part of the instruction cache not in use can be used as RAM for instruction execution

5. DMAC (DMA Controller)

- 5 channels (channels 1 and 2 are connected to the USB function.)
- 3 transfer sources (internal peripherals, software)
- Addressing mode with 32-bit full address specifications (increase, decrease, fixed)
- Transfer modes (demand transfer, burst transfer, step transfer, block transfer)
- Transfer data size that can be selected from 8, 16, and 32 bits

6. Bit Search Module (Used by REALOS)

Searches for the position of the first bit varying between 1 and 0 in the MSB of a word

7. 16-bit Reload Timer (Including One Channel for REALOS)

- 16-bit timer; 3 channels
- Internal clock that can be selected from those resulting from frequency divided by 2, 8, and 32

8. UART

- Full-duplex double buffer
- 5 channels
- Parity or no parity can be selected.
- Either asynchronous (start-stop synchronization) or CLK synchronous communication can be selected.
- Built-in timer for dedicated baud rates
- An external clock can be used as the transfer clock.
- Plentiful error detection functions (parity, frame, overrun)

9. I²C Interface*

- 4 channels (bridge function and pin function for 5 channels)
- Master/slave transmission and reception
- Clock synchronization function
- Transfer direction detection function
- Bus error detection function
- Supports standard mode (Max 100 Kbps) and high-speed mode (Max 400 Kbps) .
- Built-in FIFO function : each 16-byte sending/receiving
- Arbitration function
- Slave address/general call address detection function
- Start condition repetitious occurrence and detection function
- 10-bit/7-bit slave address

10. Interrupt Controller

- Total of 17 external interrupts (one unmaskable interrupt pin ($\overline{\text{NMI}}$) and 16 regular interrupt pins (INT15 to INT0))
- Interrupts from internal peripherals
- Priority level can be defined as programmable (16 levels) except for the unmaskable interrupt pin.
- Can be used for wake-up during stop.

11. 10-bit A/D Converter

- 10-bit resolution, 10 channels
- Sequential comparison and conversion type (conversion time : about 8.18 μs)
- Conversion modes (single conversion mode and scan conversion mode)
- Causes of startup (software and external triggers)

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12. PPG

- 4 channels
- 16-bit data register with 16-bit down counter and cycle setting buffer
- Internal clock : Frequency-divide-by number selectable from 1, 4, 16, and 64

13. PWC

- 1 channel (1 input)
- 16-bit up counter
- Simple Low-pass digital filter

14. 16-bit Free-run Timer

- 16-bit 1channel
- Input capture 4 channels

15. USB Function (Enabling/Disabling Function Can Be Selected by Mode Pin)

- USB2.0 full-speed, double buffer
- Configuration of FIFO for End point
CONTROL IN/OUT, BULK IN/OUT, and INTERRUPT IN

16. Other Interval Timers

Watchdog timer

17. I/O Ports

Maximum of 98 ports

18. Other Features

- Has a built-in oscillation circuit as a clock source.
- $\overline{\text{INIT}}$ is provided as a reset pin.
- Additionally, a watchdog timer reset and software resets are provided.
- Stop mode and sleep mode supported as low-power consumption modes
- Gear function
- Built-in timebase timer
- Package : LQFP-176, 0.5 mm pitch, and 24 mm × 24 mm
- CMOS technology : 0.18 μm
- Power supply voltage : two sources (0.18 μm) of 3.3 V (−0.3 V to +0.3 V) and 1.8 V (−0.15 V to +0.15 V)

* : LICENSE

Purchase of Fujitsu I²C components conveys a license under the Philips I²C Patent Rights to use, these components in an I²C system provided that the system conforms to the I²C Standard Specification as defined by Philips.

PIN ASSIGNMENT

(TOP VIEW)

	176	D23/P27		132	PA4/INT4
	175	D22/P26		131	PA3/INT3
	174	D21/P25		130	PA2/INT2
	173	D20/P24		129	PA1/INT1
	172	D19/P23		128	PA0/INT0
	171	D18/P22		127	NMI
	170	D17/P21		126	VDDI
	169	D16/P20		125	VSS
	168	VDDI		124	VDDE
	167	VSS		123	P97/SDA4
	166	VDDE		122	P96/SCL4
	165	PE2/DEOP2/TRG3		121	P95/SDA3
	164	PE1/DACK2/TRG2		120	P94/SCL3
	163	PE0/DREQ2/TRG1		119	P93/SDA2
	162	PD5/DEOP1/TIN2		118	P92/SCL2
	161	PD4/DACK1/TIN1		117	P91/SDA1
	160	PD3/DREQ1/TIN0		116	P90/SCL1
	159	PD2/DEOP0		115	P84/SDA0
	158	PD1/DACK0		114	P83/SCL0
	157	PD0/DREQ0		113	P82/SCK4
	156	PC7/RINI/ORD		112	P81/SOUT4
	155	PC6/TOUT2/MWR		111	P80/SIN4
	154	PC5/TOUT1		110	P75/SCK3
	153	PC4/TOUT0/TRG0		109	P74/SOUT3
	152	PC3/PPG3		108	P73/SIN3
	151	PC2/PPG2		107	P72/SCK2
	150	PC1/PPG1		106	P71/SOUT2
	149	PC0/PPG0		105	P70/SIN2
	148	VDDI		104	P65/SCK1
	147	VSS		103	P64/SOUT1
	146	UDM		102	P63/SIN1
	145	UDP		101	P62/SCK0
	144	VDDF		100	P61/SOUT0
	143	PB7/INT15/ICU3		99	P60/SIN0
	142	PB6/INT14/ICU2		98	VDDI
	141	PB5/INT13/ICU1		97	VSS
	140	PB4/INT12/ICU0		96	VDDE
	139	PB3/INT11/FRCK		95	TRST
	138	PB2/INT10/ATRQ		94	ICLK
	137	PB1/INT9		93	IBREAK
	136	PB0/INT8		92	ICD3
	135	PA7/INT7		91	ICD2
	134	PA6/INT6		90	ICD1
	133	PA5/INT5		89	ICD0
VDDE	1			88	ICS2
VSS	2			87	ICS1
VDDI	3			86	ICS0
D24	4			85	AN9/PF7
D25	5			84	AN8/PF6
D26	6			83	AN7/PF5
D27	7			82	AN6/PF4
D28	8			81	AN5/PF3
D29	9			80	AN4/PF2
D30	10			79	AN3/PF1
D31	11			78	AN2/PF0
VDDE	12			77	AN1
VSS	13			76	ANO
VDDI	14			75	AVSS
RD	15			74	AVRH
WR0/DQMUU	16			73	AVCC
WR1/DQMULP30	17			72	MD3
CS0/P31	18			71	MD2
CS1/P32	19			70	MD1
CS4/P33	20			69	MDO
CS5/P34	21			68	INTT
CS6/P35	22			67	VDDI
CS7/P36	23			66	X1
RDY/P37	24			65	VSS
P40/BGRNT	25			64	X0
P41/BRQ	26			63	VDDE
SYSCLK/P42	27			62	A23/P57
MCLK/P43	28			61	A22/P56
MCLK/P44	29			60	A21/P55
P45/SRAS/LBA/AS	30			59	A20/P54
P46/SCAS/BAA	31			58	A19/P53
P47/SWE/WR	32			57	A18/P52
VDDE	33			56	A17/P51
VSS	34			55	A16/P50
VDDI	35			54	VDDI
A0	36			53	VSS
A1	37			52	VDDE
A2	38			51	A15
A3	39			50	A14
A4	40			49	A13
A5	41			48	A12
A6	42			47	A11
A7	43			46	A10
A8	44			45	A9

(FPT-176P-M07)

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■ PIN DESCRIPTION

• Function pins

Pin no.	Pin name	I/O Type*	Function
169 to 176	D16 to D23	C	External data bus bit16 to bit23. It is available in the external bus mode.
	P20 to P27		Can be used as ports in 8-bit external bus mode.
4 to 11	D24 to D31	C	External data bus bit24 to bit31. It is available in the external bus mode.
15	\overline{RD}	H	External bus read strobe output. This pin is enabled at external bus mode.
16	$\overline{WR0}$ /DQMUU	H	External bus write strobe output. This pin is enabled at external bus mode. When \overline{WR} is used as the write strobe, this becomes the byte-enable pin (DQMUU) .
17	$\overline{WR1}$ /DQMUL	D	External bus write strobe output. The pin is enabled when $\overline{WR1}$ output is enabled in the external bus mode. When \overline{WR} is used as the write strobe, this becomes the byte-enable pin (DQMUL) .
	P30		General-purpose input/output port. The pin is enabled when the external bus write-enable output is disabled.
18	$\overline{CS0}$	D	Chip select 0 output. This pin is enabled at external bus mode.
	P31		General-purpose input/output port. This pin is enabled in the single-chip mode.
19	$\overline{CS1}$	D	Chip select 1 output. This function is enabled when chip select 1 output is enabled.
	P32		General-purpose input/output port. This function is enabled when chip select 1 output is disabled.
20	$\overline{CS4}$	D	Chip select 4 output. This function is enabled when chip select 4 output is enabled.
	P33		General-purpose input/output port. This function is enabled when chip select 4 output is disabled.
21	$\overline{CS5}$	D	Chip select 5 output. This function is enabled when chip select 5 output is enabled.
	P34		General-purpose input/output port. This function is enabled when chip select 5 output is disabled.
22	$\overline{CS6}$	D	Chip select 6 output. This function is enabled when chip select 6 output is enabled.
	P35		General-purpose input/output port. This function is enabled when chip select 6 output is disabled.
23	$\overline{CS7}$	D	Chip select 7 output. This function is enabled when chip select 7 output is enabled.
	P36		General-purpose input/output port. This function is enabled when chip select 7 output is disabled.

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Pin no.	Pin name	I/O Type*	Function
24	RDY	D	External ready input. This function is enabled when external ready input is enabled.
	P37		General-purpose input/output port. This function is enabled when external ready input is disabled.
25	$\overline{\text{BGRNT}}$	D	Acceptance output for external bus release. Outputs "L" when the external bus is released. This function is enabled when output is enabled.
	P40		General-purpose input/output port. This function is enabled when external bus release acceptance is disabled.
26	BRQ	D	External bus release request input. Input "1" to request release of the external bus. The function is enabled when input is enabled.
	P41		General-purpose input/output port. This function is enabled when the external bus release request is disabled.
27	SYCLK	D	System clock output. This function is enabled when system clock output is enabled. This outputs the same clock as the external bus operating frequency. (Output halts in stop mode.)
	P42		General-purpose input/output port. This function is enabled when system clock output is disabled.
28	MCLKE	D	Clock enable signal for SDRAM.
	P43		General-purpose input/output port. This function is enabled when memory clock output is disabled.
29	MCLK	D	Memory clock output. This function is enabled when memory clock output is enabled. This outputs the same clock as the external bus operating frequency. (Output halts in sleep mode.)
	P44		General-purpose input/output port. This function is enabled when memory clock output is disabled.
30	$\overline{\text{AS}}$	D	Address strobe output. This function is enabled when address strobe output is enabled.
	$\overline{\text{LBA}}$		Address load output for burst flash memory. This function is enabled when address load output is enabled.
	$\overline{\text{SRAS}}$		RAS strobe single for SDRAM.
	P45		General-purpose input/output port. This function is enabled when address load output is disabled.
31	$\overline{\text{BAA}}$	D	Address advance output for burst flash memory. This function is enabled when address advance output is enabled.
	$\overline{\text{SCAS}}$		CAS strobe signal for SDRAM.
	P46		General-purpose input/output port. This function is enabled when address advance output is disabled.

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Pin no.	Pin name	I/O Type*	Function
32	\overline{WR}	D	Memory write strobe output. This function is enabled when write strobe output is enabled.
	\overline{SWE}		Write output for SDRAM.
	P47		General-purpose input/output port. This function is enabled when write strobe output is disabled.
36 to 51	A0 to A15	H	External address bus bit0 to bit15.
55 to 62	A16 to A23	D	External address bus bit16 to bit23.
	P50 to P57		Can be used as ports when external address bus is not used.
64	X0	A	Clock (oscillation) input.
66	X1		Clock (oscillation) output.
68	\overline{INIT}	B	External reset input (Reset to initialize settings)
69 to 71	MD0 to MD2	I	These pins set the basic operating mode. Connect V_{CC} or V_{SS} .
72	MD3	J	These pins set the basic operating mode. Connect V_{CC} or V_{SS} .
76, 77	AN0, AN1	M	Analog input pin.
78 to 85	AN2 to AN9	F	Analog input pin.
	PF0 to PF7		Can be used as ports when analog input pin is not used.
86 to 88	ICS0 to ICS2	C	Status output pin for development tool.
89 to 92	ICD0 to ICD3	L	Data input/output pin for development tool.
93	IBREAK	J	Break pin for development tool.
94	ICLK	D	Clock pin for development tool.
95	\overline{TRST}	B	Reset pin for development tool.
99	SIN0	D	UART0 data input pin. This input is used continuously when UART0 is performing input. In this case, do not output to this port unless doing so intentionally.
	P60		General-purpose input/output port.
100	SOUT0	D	UART0 data output pin. This function is enabled when UART0 data output is enabled.
	P61		General-purpose input/output port.
101	SCK0	D	UART0 clock input/output pin. This function is enabled when UART0 clock output is enabled.
	P62		General-purpose input/output port.

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Pin no.	Pin name	I/O Type*	Function
102	SIN1	D	UART1 data input pin. This input is used continuously when UART1 is performing input. In this case, do not output to this port unless doing so intentionally.
	P63		General-purpose input/output port.
103	SOUT1	D	UART1 data output pin. This function is enabled when UART1 data output is enabled.
	P64		General-purpose input/output port.
104	SCK1	D	UART1 clock input/output pin. This function is enabled when UART1 clock output is enabled.
	P65		General-purpose input/output port.
105	SIN2	D	UART2 data input pin. This input is used continuously when UART2 is performing input. In this case, do not output to this port unless doing so intentionally.
	P70		General-purpose input/output port.
106	SOUT2	D	UART2 data output pin. This function is enabled when UART2 data output is enabled.
	P71		General-purpose input/output port.
107	SCK2	D	UART2 clock input/output pin. This function is enabled when UART2 clock output is enabled.
	P72		General-purpose input/output port.
108	SIN3	D	UART3 data input pin. This input is used continuously when UART3 is performing input. In this case, do not output to this port unless doing so intentionally.
	P73		General-purpose input/output port.
109	SOUT3	D	UART3 data output pin. This function is enabled when UART3 data output is enabled.
	P74		General-purpose input/output port.
110	SCK3	D	UART3 clock input/output pin. This function is enabled when UART3 clock output is enabled.
	P75		General-purpose input/output port.
111	SIN4	D	UART4 data input pin. This input is used continuously when UART4 is performing input. In this case, do not output to this port unless doing so intentionally.
	P80		General-purpose input/output port.
112	SOUT4	D	UART4 data output pin. This function is enabled when UART4 data output is enabled.
	P81		General-purpose input/output port.

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Pin no.	Pin name	I/O Type*	Function
113	SCK4	D	UART4 clock input/output pin. This function is enabled when UART4 clock output is enabled.
	P82		General-purpose input/output port.
114	SCL0	D	Clock I/O pin for I ² C bus. This function is enabled when typical operation of I ² C is enabled. The port output must remain off unless intentionally turned on. (pseudo open drain output)
	P83		General-purpose input/output port.
115	SDA0	D	Data I/O pin for I ² C bus. This function is enabled when typical operation of I ² C is enabled. The port output must remain off unless intentionally turned on. (pseudo open drain output)
	P84		General-purpose input/output port.
116	SCL1	D	Clock I/O pin for I ² C bus. This function is enabled when typical operation of I ² C is enabled. The port output must remain off unless intentionally turned on. (pseudo open drain output)
	P90		General-purpose input/output port.
117	SDA1	D	Data I/O pin for I ² C bus. This function is enabled when typical operation of I ² C is enabled. The port output must remain off unless intentionally turned on. (pseudo open drain output)
	P91		General-purpose input/output port.
118	SCL2	K	Clock I/O pin for I ² C bus. This function is enabled when typical operation of I ² C is enabled. The port output must remain off unless intentionally turned on. (pseudo open drain output)
	P92		General-purpose input/output port.
119	SDA2	K	Data I/O pin for I ² C bus. This function is enabled when typical operation of I ² C is enabled. The port output must remain off unless intentionally turned on. (pseudo open drain output)
	P93		General-purpose input/output port.
120	SCL3	K	Clock I/O pin for I ² C bus. This function is enabled when typical operation of I ² C is enabled. The port output must remain off unless intentionally turned on. (pseudo open drain output)
	P94		General-purpose input/output port.
121	SDA3	K	Data I/O pin for I ² C bus. This function is enabled when typical operation of I ² C is enabled. The port output must remain off unless intentionally turned on. (pseudo open drain output)
	P95		General-purpose input/output port.
122	SCL4	K	Clock I/O pin for I ² C bus. This function is enabled when typical operation of I ² C is enabled. The port output must remain off unless intentionally turned on. (pseudo open drain output)
	P96		General-purpose input/output port.

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Pin no.	Pin name	I/O Type*	Function
123	SDA4	K	Data I/O pin for I ² C bus. This function is enabled when typical operation of I ² C is enabled. The port output must remain off unless intentionally turned on. (pseudo open drain output)
	P97		General-purpose input/output port.
127	$\overline{\text{NMI}}$	B	NMI (Non Maskable Interrupt) input
128 to 131	INT0 to INT3	G	External interrupt inputs. These inputs are used continuously when the corresponding external interrupt is enabled. In this case, do not output to these ports unless doing so intentionally.
	PA0 to PA3		General-purpose input/output port.
132	INT4	G	External interrupt input. These inputs are used continuously when the corresponding external interrupt is enabled. In this case, do not output to these ports unless doing so intentionally. When USB function is enabled (MD3, MD2, MD1, MD0 = 0000 _B), INT4 function is used only for the USB interrupt. Therefore, it is not possible to use it as an external interrupt pin.
	PA4		General-purpose input/output port.
133 to 135	INT5 to INT7	G	External interrupt input. These inputs are used continuously when the corresponding external interrupt is enabled. In this case, do not output to these ports unless doing so intentionally.
	PA5 to PA7		General-purpose input/output port.
136	INT8	G	External interrupt input. These inputs are used continuously when the corresponding external interrupt is enabled. In this case, do not output to these ports unless doing so intentionally.
	PB0		General-purpose input/output port.
137	INT9	G	External interrupt input. These inputs are used continuously when the corresponding external interrupt is enabled. In this case, do not output to these ports unless doing so intentionally.
	PB1		General-purpose input/output port.
138	INT10	G	External interrupt input. These inputs are used continuously when the corresponding external interrupt is enabled. In this case, do not output to these ports unless doing so intentionally.
	ATR $\overline{\text{G}}$		A/D converter external trigger input. These inputs are used continuously when using as A/D start trigger. In this case, do not output to these ports unless doing so intentionally.
	PB2		General-purpose input/output port.
139	INT11	G	External interrupt input. These inputs are used continuously when the corresponding external interrupt is enabled. In this case, do not output to these ports unless doing so intentionally.
	FRCK		External clock input pin of free-run timer. These inputs are used continuously when using as external clock input pin of free-run timer. In this case, do not output to these ports unless doing so intentionally.
	PB3		General-purpose input/output port.

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Pin no.	Pin name	I/O Type*	Function
140 to 143	INT12 to INT15	G	External interrupt input. These inputs are used continuously when the corresponding external interrupt is enabled. In this case, do not output to these ports unless doing so intentionally.
	ICU0 to ICU3		Input capture input pins. These inputs are used continuously when selected as input capture inputs. In this case, do not output to these ports unless doing so intentionally.
	PB4 to PB7		General-purpose input/output port.
145	UDP	USB	+ pin of USB.
146	UDM		- pin of USB.
149 to 152	PPG0 to PPG3	D	PPG ch.0 to PPG ch.3 timer output.
	PC0 to PC3		General-purpose input/output port.
153	TOUT0	D	Data output of reload timer 0. This function is enabled when data output of reload timer 0 is enabled using port function register.
	TRG0		External trigger input for PPG0 timer. This input is used continuously when the corresponding timer input is enabled. In this case, do not output to this port unless doing so intentionally.
	PC4		General-purpose input/output port.
154	TOUT1	D	Data output of reload timer 1. This function is enabled when data output of reload timer 1 is enabled using port function register.
	PC5		General-purpose input/output port.
155	TOUT2	D	Data output of reload timer 2. This function is enabled when data output of reload timer 2 is enabled using port function register.
	$\overline{\text{IOWR}}$		Write strobe output for DMA fly-by transfer. This function is enabled when outputting a write strobe for DMA fly-by transfer is enabled.
	PC6		General-purpose input/output port.
156	RIN	D	PWC input. These inputs are used continuously when the corresponding external interrupt is enabled. In this case, do not output to these ports unless doing so intentionally.
	$\overline{\text{IORD}}$		Read strobe output for DMA fly-by transfer. This function is enabled when outputting a read strobe for DMA fly-by transfer is enabled.
	PC7		General-purpose input/output port.
157	DREQ0	D	External input for DMA transfer requests. This input is used continuously when the corresponding external input for DMA transfer requests are enabled. In this case, do not output to this port unless doing so intentionally.
	PD0		General-purpose input/output port.

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Pin no.	Pin name	I/O Type*	Function
158	$\overline{\text{DACK0}}$	D	DMA external transfer request acceptance output. This function is enabled when DMA external transfer request acceptance output is enabled.
	PD1		General-purpose input/output port.
159	$\overline{\text{DEOP0}}$	D	Completion output for DMA external transfer. This function is enabled when completion output for DMA external transfer is enabled.
	PD2		General-purpose input/output port.
160	DREQ1	D	External input for DMA transfer requests. This input is used continuously when external input for DMA transfer request is enabled. In this case, do not output to this port unless doing so intentionally. When using USB, this function (DMAC ch.1) cannot be used because it is used as USB data transfer. DREQ2 input is disabled.
	TIN0		Reload timer input. This input is used continuously when the corresponding timer input is enabled. In this case, do not output to this port unless doing so intentionally.
	PD3		General-purpose input/output port.
161	$\overline{\text{DACK1}}$	D	DMA external transfer request acceptance output. This function is enabled when DMA transfer request acceptance output is enabled. When using USB, this function (DMAC ch.1) cannot be used because it is used as USB data transfer. External transfer ACK output of DMA should be disabled.
	TIN1		Reload timer input. This input is used continuously when the corresponding timer input is enabled. In this case, do not output to this port unless doing so intentionally.
	PD4		General-purpose input/output port.
162	$\overline{\text{DEOP1}}$	D	Completion output for DMA external transfer. This function is enabled when completion output for DMA external transfer is enabled. When using USB, this function (DMAC ch.1) cannot be used because it is used as USB data transfer. External transfer EOP output of DMA should be disabled.
	TIN2		Reload timer input. This input is used continuously when the corresponding timer input is enabled. In this case, do not output to this port unless doing so intentionally.
	PD5		General-purpose input/output port.
163	DREQ2	D	External input for DMA transfer requests. This input is used continuously when external input for DMA transfer request is enabled. In this case, do not output to this port unless doing so intentionally. When using USB, this function (DMAC ch.2) cannot be used because it is used as USB data transfer. DREQ2 input is disabled.
	TRG1		External trigger input for PPG1 timer. This input is used continuously when the corresponding timer input is enabled. In this case, do not output to this port unless doing so intentionally.
	PE0		General-purpose input/output port.

(Continued)

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(Continued)

Pin no.	Pin name	I/O Type*	Function
164	$\overline{\text{DACK2}}$	D	DMA external transfer request acceptance output. This function is enabled when DMA transfer request acceptance output is enabled. When using USB, this function (DMAC ch.2) cannot be used because it is used as USB data transfer. External transfer ACK output of DMA should be disabled.
	TRG2		External trigger input for PPG2 timer. This input is used continuously when the corresponding timer input is enabled. In this case, do not output to this port unless doing so intentionally.
	PE1		General-purpose input/output port.
165	$\overline{\text{DEOP2}}$	D	Completion output for DMA external transfer. This function is enabled when completion output for DMA external transfer is enabled. When using USB, this function (DMAC ch.2) cannot be used because it is used as USB data transfer. External transfer EOP output of DMA should be disabled.
	TRG3		External trigger input for PPG3 timer. This input is used continuously when the corresponding timer input is enabled. In this case, do not output to this port unless doing so intentionally.
	PE2		General-purpose input/output port.

* : For I/O circuit type, refer to “■ I/O CIRCUIT TYPES”.

• Power supply and GND pins

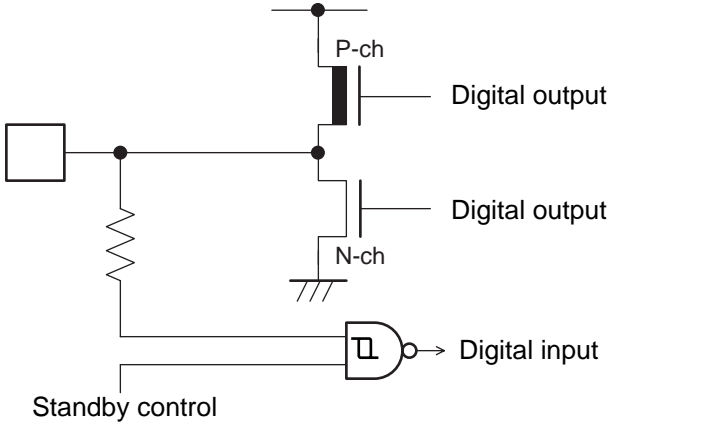
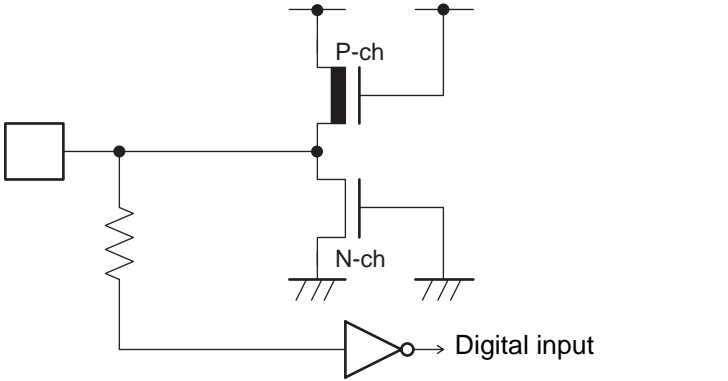
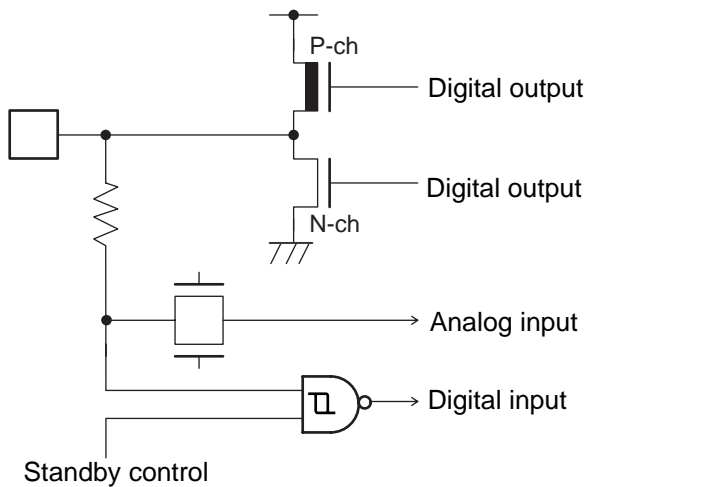
Pin no.	Pin name	Function
2, 13, 34, 53, 65, 97, 125, 147, 167	VSS	GND pins. Connect all pins at the same potential.
3, 14, 35, 54, 67, 98, 126, 148, 168	VDDI	1.8 V power supply pins. Connect all pins at the same potential.
1, 12, 33, 52, 63, 96, 124, 144, 166	VDDE	3.3 V power supply pins. Connect all pins at the same potential.
73	AVCC	Analog power supply pin for A/D converter
74	AVRH	Reference power supply pin for A/D converter
75	AVSS	Analog GND pin for the A/D converter

■ I/O CIRCUIT TYPES

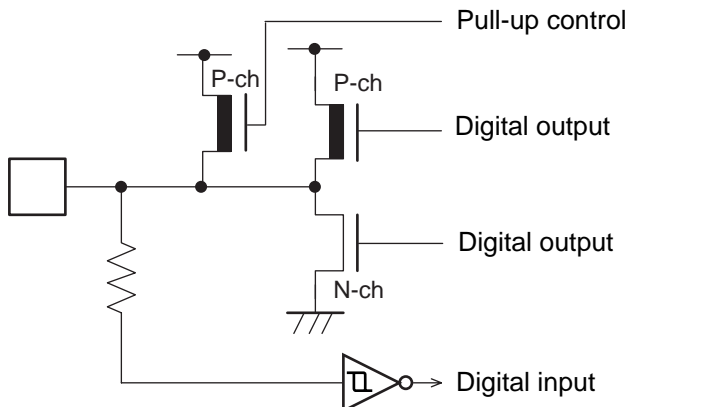
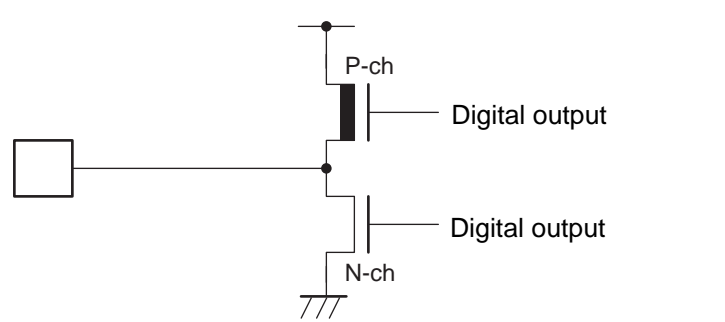
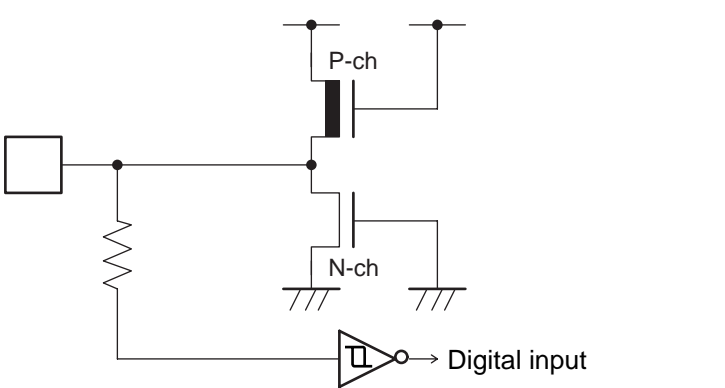
Type	Circuit	Remarks
A		<p>Oscillation feedback resistance approx. $1M\Omega$</p>
B		<ul style="list-style-type: none"> • With pull-up resistor • CMOS level hysteresis input
C		<ul style="list-style-type: none"> • CMOS level I/O • With standby control • $I_{OL} = 4\text{ mA}$

(Continued)

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Type	Circuit	Remarks
D	 <p>Circuit diagram for Type D: A CMOS output stage with a P-channel MOSFET (P-ch) and an N-channel MOSFET (N-ch). The gates are connected to a digital input through an AND gate. A standby control signal is connected to the gates. The output node is connected to a pull-up resistor and a digital output terminal.</p>	<ul style="list-style-type: none"> • CMOS level output • CMOS level hysteresis input • With standby control • $I_{OL} = 4 \text{ mA}$
E	 <p>Circuit diagram for Type E: A CMOS input stage with a P-channel MOSFET (P-ch) and an N-channel MOSFET (N-ch). The gates are connected to a digital input through an inverter. A pull-up resistor is connected to the output node. A standby control signal is connected to the gates.</p>	<ul style="list-style-type: none"> • CMOS level input • No standby control
F	 <p>Circuit diagram for Type F: A CMOS output stage with a P-channel MOSFET (P-ch) and an N-channel MOSFET (N-ch). The gates are connected to a digital input through an AND gate. A standby control signal is connected to the gates. The output node is connected to a pull-up resistor, an analog input terminal, and a digital input terminal.</p>	<ul style="list-style-type: none"> • CMOS level output • CMOS level hysteresis input • With standby control • With analog input • $I_{OL} = 4 \text{ mA}$

(Continued)

Type	Circuit	Remarks
G		<ul style="list-style-type: none"> • With pull-up control • CMOS level output • CMOS level hysteresis input • No standby control • $I_{OL} = 4 \text{ mA}$
H		<p>CMOS level output</p>
I		<ul style="list-style-type: none"> • CMOS level hysteresis input • No standby control

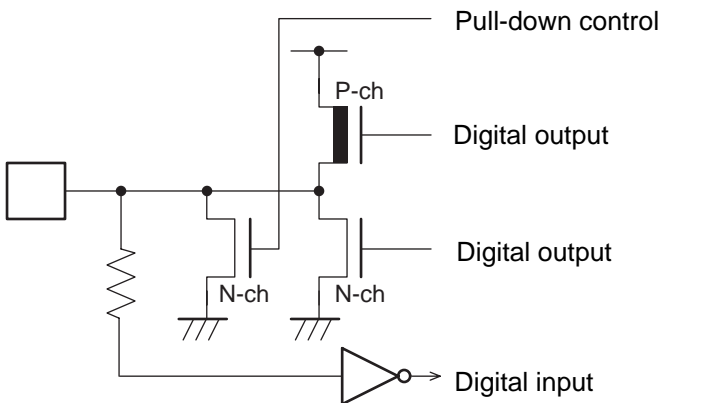
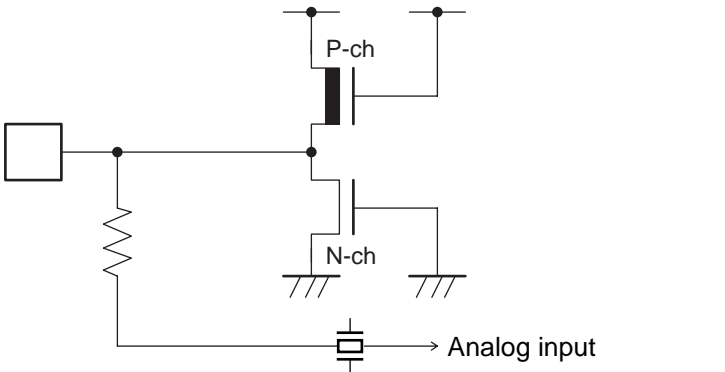
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Type	Circuit	Remarks
J	<p>The circuit for Type J consists of a pull-down resistor connected to ground. The other end of the resistor is connected to the gate of an N-channel MOSFET. The drain of this N-channel MOSFET is connected to the gate of a P-channel MOSFET. The source of the P-channel MOSFET is connected to ground. The drain of the P-channel MOSFET is connected to the input of a digital input buffer. The output of the buffer is labeled "Digital input".</p>	<ul style="list-style-type: none"> • CMOS level hysteresis input • With pull-down resistor
K	<p>The circuit for Type K shows two identical channels. Each channel includes a pull-down resistor connected to ground. The other end of the resistor is connected to the gate of an N-channel MOSFET. The drain of this N-channel MOSFET is connected to the gate of a P-channel MOSFET. The source of the P-channel MOSFET is connected to ground. The drain of the P-channel MOSFET is connected to the input of a digital input buffer. The output of the buffer is labeled "Digital input". The drain of the N-channel MOSFET is also connected to the output of a digital output buffer, labeled "Digital output". The gate of the P-channel MOSFET is also connected to the output of an open-drain control buffer, labeled "Open-drain control".</p>	<ul style="list-style-type: none"> • 3 ports for I²C • CMOS level hysteresis input • CMOS level output • With stop control

(Continued)

(Continued)

Type	Circuit	Remarks
L		<ul style="list-style-type: none"> • CMOS I/O • With pull-down control
M		Analog pin

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■ HANDLING DEVICES

• Preventing a Latch-up

A latch-up can occur on a CMOS IC under following conditions. A latch-up, if it occurs, significantly increases the power supply current and may cause thermal destruction of an element. When you use a CMOS IC, be very careful not to exceed the maximum rating.

- When a voltage higher than VDDE or VDDI or a voltage lower than VSS is applied to an input or output pin.
- When a voltage higher than the rating is applied between VDDE or VDDI and VSS.

• Handling of Unused Input Pins

Do not leave an unused input pin open since it may cause a malfunction. Handle by, for example, using a pull-up or pull-down resistor.

• Power Supply Pins

If more than one VDDE or VDDI or VSS pin exists, those that must be kept at the same potential are designed to be connected to one other inside the device to prevent malfunctions such as latch-up. Be sure to connect the pins to a power supply and ground external to the device to minimize undesired electromagnetic radiation, prevent strobe signal malfunctions due to an increase in ground level, and conform to the total output current rating. Given consideration to connecting the current supply source to VDDE or VDDI and VSS pin of the device at the lowest impedance possible.

It is also recommended that a ceramic capacitor of around 0.1 μ F be connected between VDDE or VDDI and VSS pin at circuit points close to the device as a bypass capacitor.

• Quartz Oscillation Circuit

Noise near the X0 or X1 pin may cause the device to malfunction. Design printed circuit boards so that X0, X1, the quartz oscillator (or ceramic oscillator), and the bypass capacitor to ground are located as near to one another as possible.

It is strongly recommended that printed circuit board artwork that surrounds the X0 and X1 pins with ground be used to increase the expectation of stable operation.

Please ask the Oscillation maker to evaluate the oscillational characteristics of the crystal and this device.

• Mode Pins (MD0 to MD3)

In order to prevent mistakes due to noise, and sending them into test mode, connect these pins as close to VDDE and VSS pins, and at as low an impedance as possible.

• Tool Reset Pins ($\overline{\text{TRST}}$)

Be sure to input the same signal as the $\overline{\text{INIT}}$ when this pin is not used for the tool. The same processing is executed for the mass product.

• Power-on

Immediately after power-on, be sure to apply setting initialization reset (INIT) with $\overline{\text{INIT}}$ pin.

Also immediately after power-on, keep the $\overline{\text{INIT}}$ pin at the "L" level until the oscillator has reached the required oscillation stabilization wait time. (For initialization by INIT from the $\overline{\text{INIT}}$ pin, the oscillation stabilization wait time is set to the minimum value.)

• Source Oscillation Input at Power-on

At power-on, be sure to input a source clock until the oscillation stabilization wait time is reached.

• Precautions at Power-On/Power-Off

- Precautions when turning on and off VDDI pin and VDDE pin

To ensure the reliability of LSI devices, do not continuously apply only VDDE pin for about a minute when VDDI is off.

When VDDE pin is changed from off to on, the power noise may make it impossible to retain the internal state of the circuit.

Power-on : Supply voltage of VDDI pin → analog → Supply voltage of VDDE pin → signal

Power-off : Signal → Supply voltage of VDDE pin → analog → Supply voltage of VDDI pin

- Indeterminate Output when the Power is Turned On

When turning on the power, the output pin may remain indeterminate until internal power supply becomes stable.

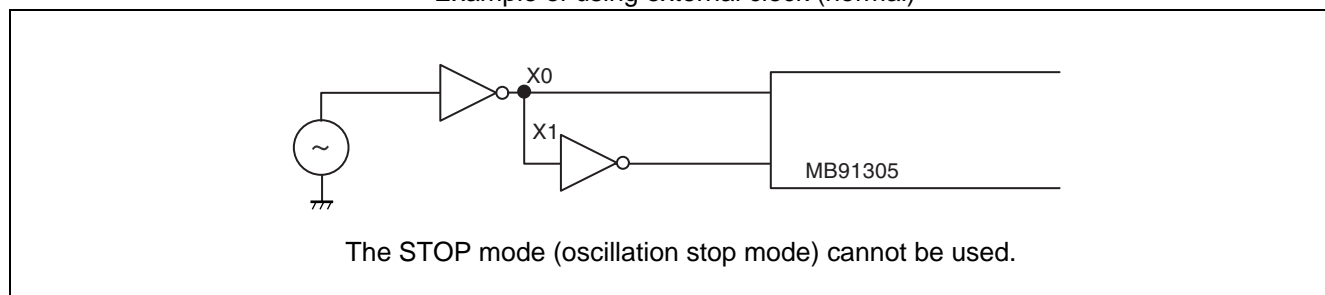
• Clocks

- Notes on using external clock

When the external clock is used, in principle, supply a clock signal to the X0 pin and an opposite-phase clock signal to the X1 pin at the same time. However, in this case the STOP mode (oscillation stop mode) must not be used (This is because, in the STOP mode, the X1 pin stops at "H" output).

Example of using an external clock is illustrated in the following figure.

Example of using external clock (normal)



• Limitations

- Clock controller

Secure the stabilization wait time while "L" is input to $\overline{\text{INIT}}$ pin.

- Bit search module

Only word access is permitted for data register for detection 0 (BSD0), data register for detection 1 (BSD1), and data register for change point detection (BSDC) .

- I/O port

Only byte access is permitted for ports.

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- Low-power Consumption Mode

To switch to standby mode, use synchronous standby mode (set by the SYNCS bit, that is bit8 of the TBCR, timebase counter control register) and be sure to use the following sequence :

```
(LD1  #value_of_stanby, R0)
(LD1  #_STCR, R12)
STB   R0, @R12  : Writing into the standby control register (STCR)
LDUB  @R12, R0  : STCR read for synchronous standby
LDUB  @R12, R0  : Dummy re-read of STCR
NOP                               : NOP × 5 for timing adjustment
NOP
NOP
NOP
NOP
```

- When using the monitor debugger, do not :
 - Set a break point within the above sequence of instructions.
 - Step of the instructions within the above sequence of instructions.

- Prefetch

When allowing prefetch in the little endian area, only word access (32-bit) should be used to access the area. Byte access and halfword access are not working properly.

- Notes on using PS register

PS register is processed by some instructions in advance so that exception operations as stated below may cause breaks during interruption handling routine when using debugger and may cause updates to the display contents of PS flags.

In either case, this device is designed to carry out reprocessing properly after returning from such EIT events. The operations before and after EIT events are performed as prescribed in the specification.

1. The following operations may be performed when the instruction immediately followed by a DIVOV/DIVOS instruction is acceptance of a user interrupt/NMI, single-stepped, or breaks in response to an emulator menu.
 - (1) D0 and D1 flags are updated in advance.
 - (2) EIT handling routine (user interrupt/NMI, or emulator) is executed.
 - (3) After returning from the EIT, a DIVOU/DIVOS instruction is executed and the D0 and D1 flags are updated to the same values as in (1) .
2. The following operations are performed if each instruction from ORCCR, STILM, MOV Ri, and PS is executed to allow an interruption while user interrupt/NMI trigger exists.
 - (1) PS register is updated in advance.
 - (2) EIT handling routine (user interrupt/NMI) is executed.
 - (3) After returning from the EIT, the above instructions are executed and the PS register is updated to the same value as in (1) .

- Watchdog Timer Function

The watchdog timer equipped in this model operates to monitor programs to ensure that they execute reset defer function within a certain period of time, and to reset the CPU if the reset defer function is not executed due to the program runaway. For that reason, once the watchdog timer function is enabled, it keeps its operation until it is reset.

By way of exception, the watchdog timer automatically defers a reset under the condition where the CPU program executions are stopped. For more detail, refer to the description section of the watchdog timer function in "Hardware Manual".

If the system gets out of control and the situation becomes as mentioned above, watchdog reset may not be generated. In that case, please reset (INIT) from the external $\overline{\text{INIT}}$ pin.

- Note on using A/D

The MB91305 has a built-in A/D converter. Do not supply a voltage higher than VDDE to the AVCC.

- Software reset in synchronous mode

When software reset in the synchronous mode is used, the following two conditions must be satisfied before setting the SRST bit of the STCR (standby control register) to 0.

- Set the interrupt enable flag (I-Flag) to the interrupt disabled (I-Flag = 0).
- Do not use NMI.

- Simultaneous occurrences of software break and user interrupt/NMI

If software break and user interrupt/NMI occur together, emulator debugger may:

- Stop at a point other than the programmed break points.
- Not reexecute properly after halting.

If such failures occur, use hardware break instead of software break. When using monitor debugger, do not set any break points within the corresponding instructions.

- Stepping of the RETI Instruction

In the environment where interruptions occur frequently during stepping, the RETI is executed repeatedly for the corresponding interrupt process routines after the stepping. As the result of it, the main routine and low interrupt-level programs are not executed. To avoid this situation, do not step the RETI instruction. Otherwise, perform debugging by disabling the interruptions when the debug on the corresponding interrupt routines becomes unnecessary.

- Operand Break

Do not set the access to the areas containing the address of stack pointer as a target of data event break.

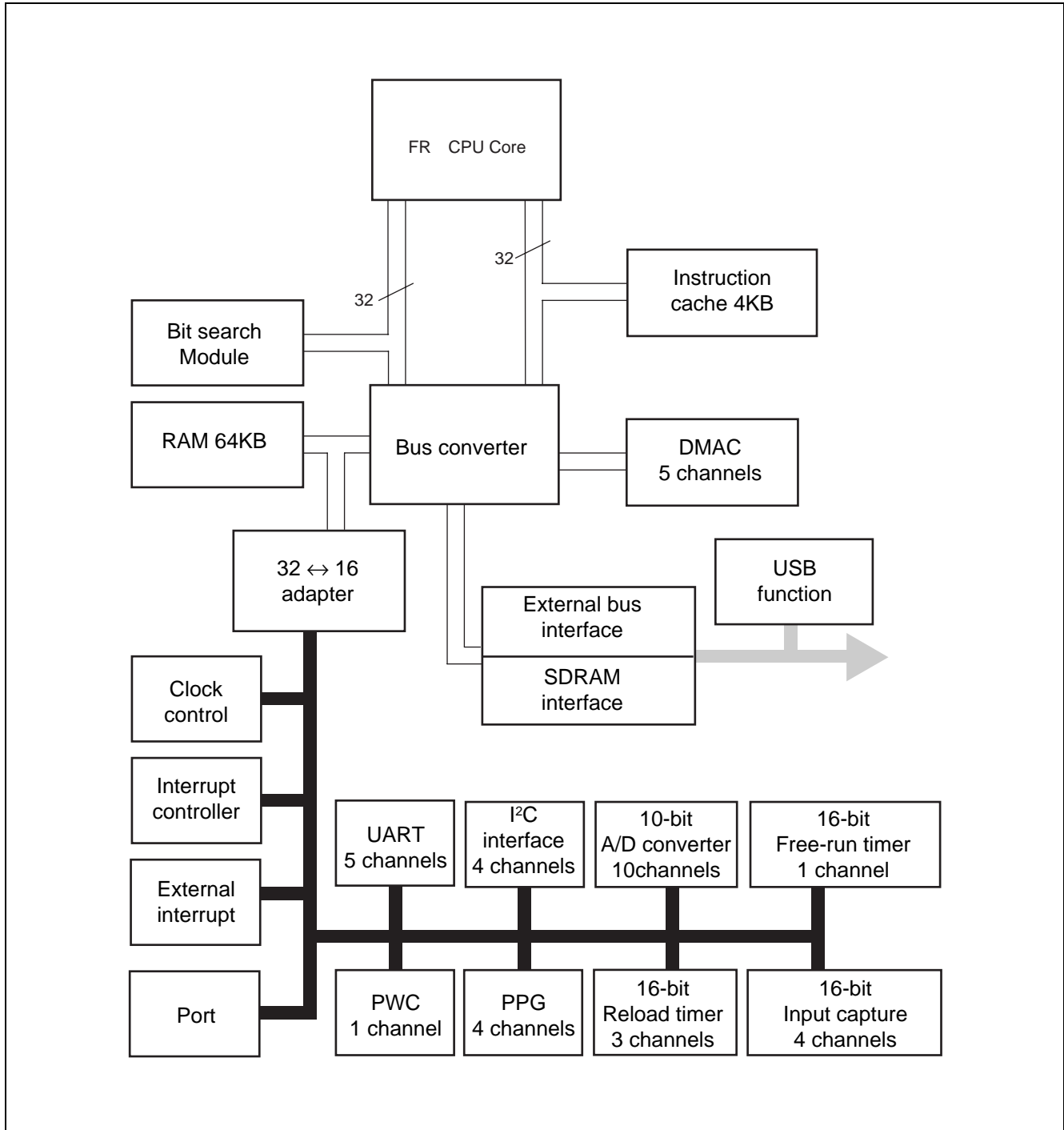
- Sample Batch File for Configuration

When a program is downloaded to internal RAM to execute debug, be sure to execute the following batch file after reset.

```
#-----
# Set MODR (0x7fd) = Enable In memory + 16-bit External Bus
set mem/byte 0x7fd = 0x5
#-----
```

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■ BLOCK DIAGRAM



■ CPU AND CONTROL UNIT

Internal Architecture

The FR family is a high-performance core based on RISC architecture and advanced instructions for embedded applications.

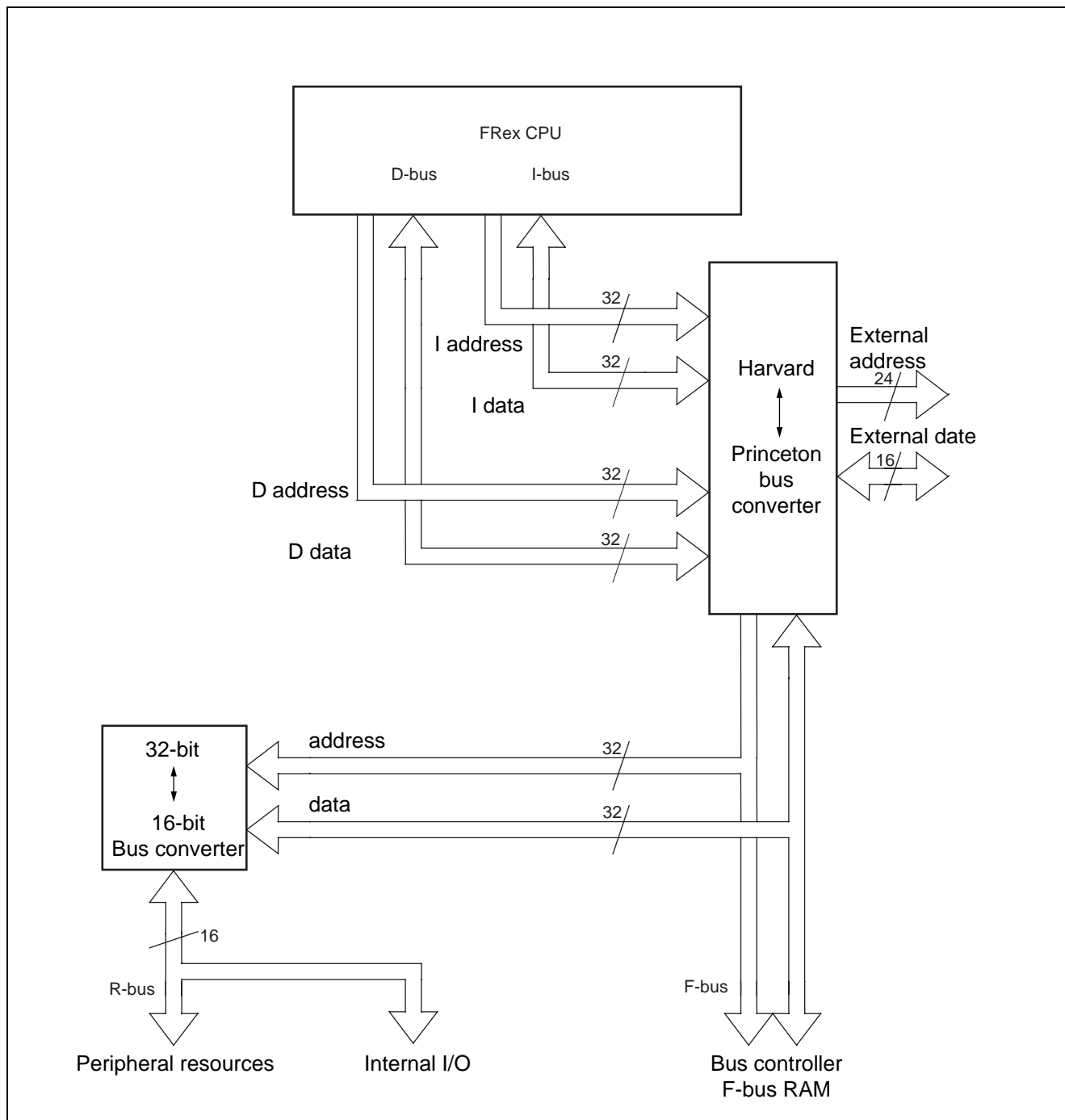
1. Features

- RISC architecture used
Basic instruction : One instruction per cycle
- 32-bit architecture
General-purpose register : 32 bits × 16
- 4G bytes linear memory space
- Multiplier installed
32-bit by 32-bit multiplication : 5 cycles
16-bit by 16-bit multiplication : 3 cycles
- Enhanced interrupt processing function
Quick response speed : 6 cycles
Support of multiple interrupts
Level mask function : 16 levels
- Enhanced instructions for I/O operations
Memory-to-memory transfer instruction
Bit-processing instructions
- Efficient code
Basic instruction word length : 16 bits
- Low-power consumption
Sleep and stop modes
- Gear function

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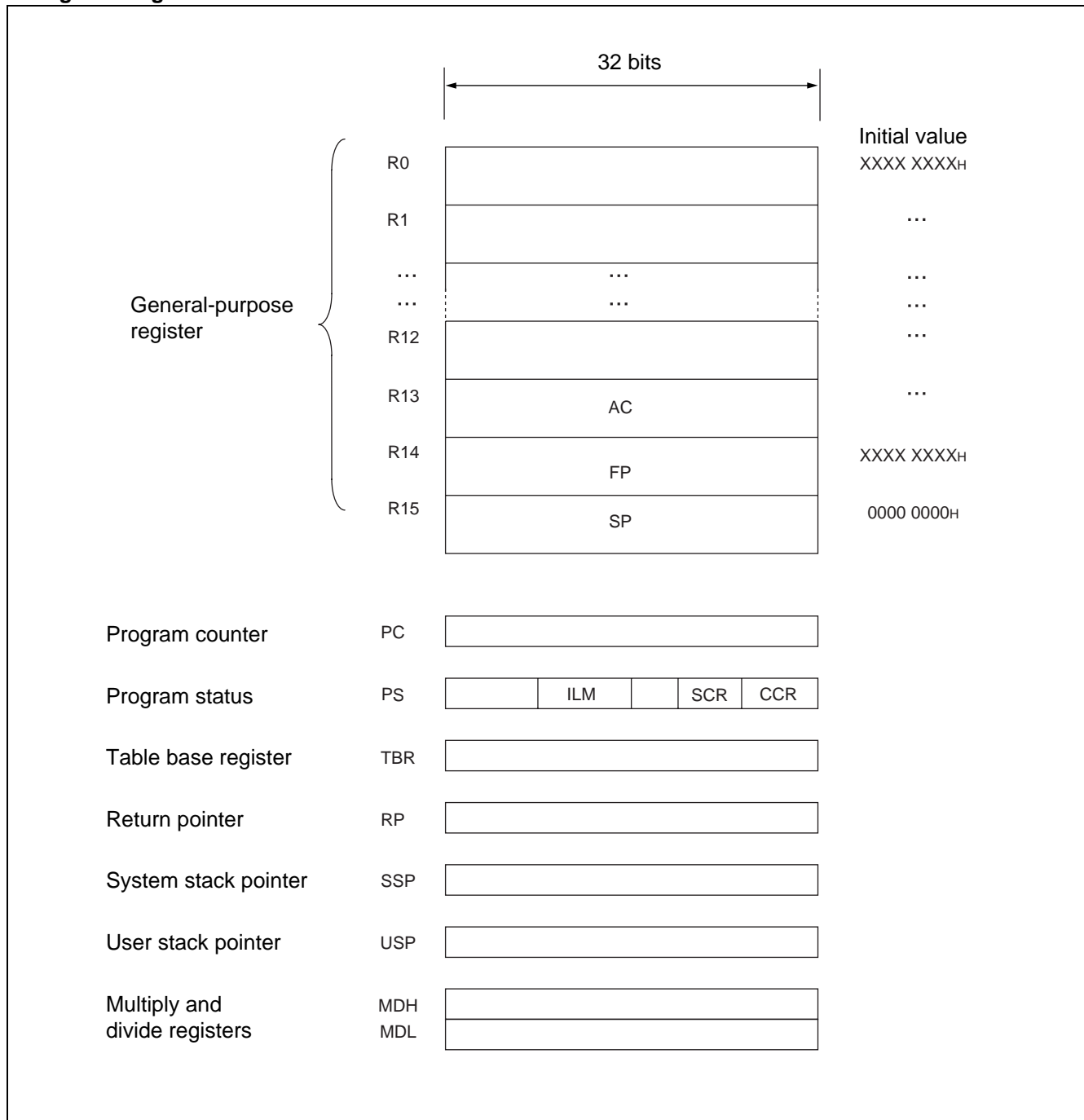
2. Internal Architecture

The FR family CPU uses the Harvard architecture, which has separate buses for instructions and data. A 32-bit↔16-bit bus converter is connected to the 32-bit bus (F-bus), providing an interface between the CPU and peripheral resources. A Harvard↔Princeton bus converter is connected to both the I-bus and D-bus, providing an interface between the CPU and bus controllers.



3. Programming Model

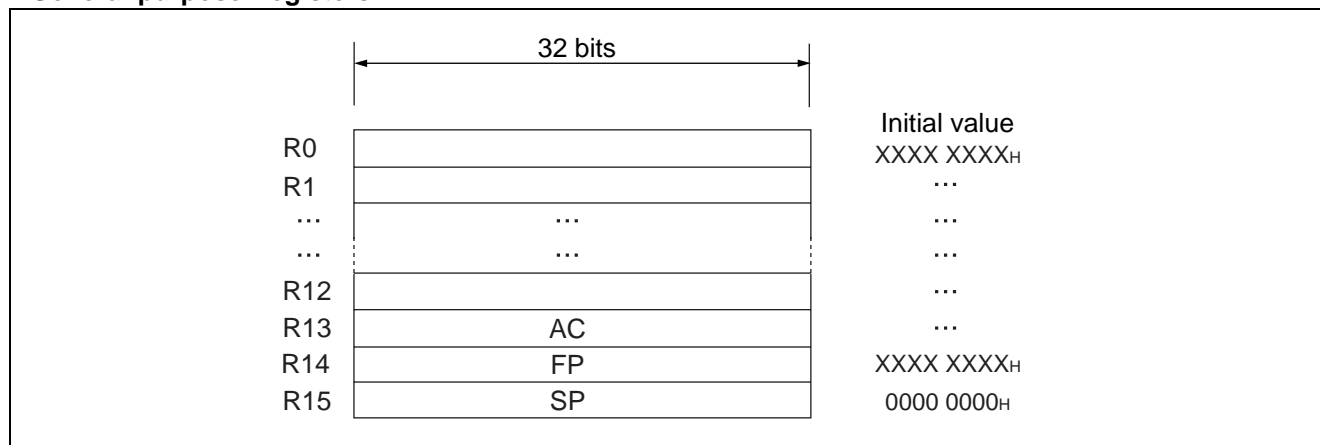
• Programming Model



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4. Registers

• General-purpose Registers



Registers R0 to R15 are general-purpose registers. These registers are used as an accumulator in an operation or a pointer in a memory access.

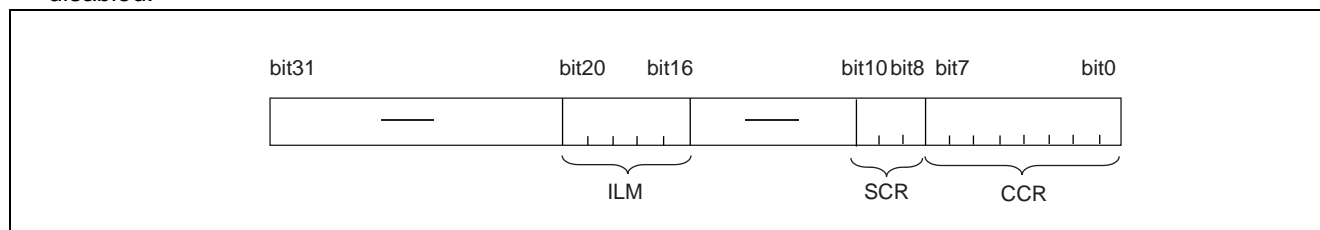
Of these 16 registers, the following are intended for special applications and therefore enhanced instructions are provided for them :

- R13 :
Virtual accumulator (AC)
- R14 :
Frame pointer (FP)
- R15 :
Stack pointer (SP)

The initial value upon reset is undefined for R0 through R14 and is "00000000H" (SSP value) for R15.

- PS (Program Status)

The program status register (PS : Program Status) holds the program status. The PS register consists of three parts : ILM, SCR, and CCR. All undefined bits are reserved. During reading, "0" is always read. Writing is disabled.



• CCR (Condition Code Register)

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
—	—	S	I	N	Z	V	C	--00XXXX _B

S : Stack flag

- This bit is cleared to “0” by a reset.
- Set this bit to “0” when the RETI instruction is executed.

I : Interrupt enable flag

This bit is cleared to “0” by a reset.

N : Negative flag

The initial state of this bit upon reset is undefined.

Z : Zero flag

The initial state of this bit upon reset is undefined.

V : Overflow flag

The initial state of this bit upon reset is undefined.

C : Carry flag

The initial state of this bit upon reset is undefined.

• SCR (System Condition code Register)

bit10	bit9	bit8	Initial value
D1	D0	T	XX0 _B

D1, D0 : Step division flag

These bits hold the intermediate data obtained when step division is executed.

T : Step trace trap flag

This bit specifies whether the step trace trap is to be enabled.

The step trace trap function is used by an emulator. When an emulator is used, this function cannot be used in a user program.

• ILM (Interrupt Level Mask Register)

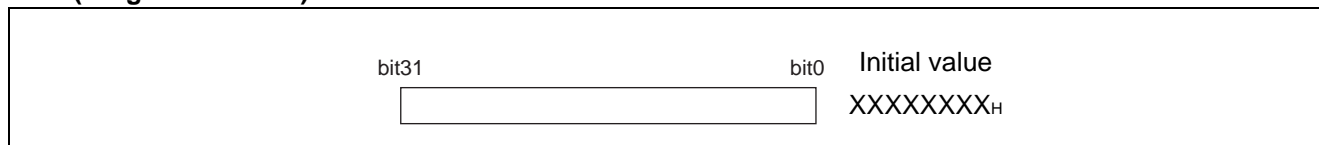
bit20	bit19	bit18	bit17	bit16	Initial value
ILM4	ILM3	ILM2	ILM1	ILM0	01111 _B

The interrupt level mask (ILM) register holds an interrupt level mask value. The value held in ILM register is used as a level mask.

This register is initialized to 15 (01111_B) by a reset.

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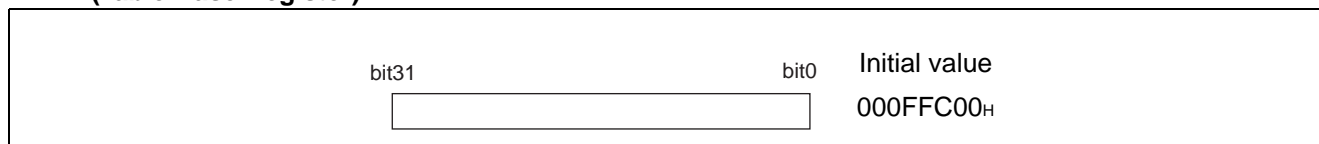
• PC (Program Counter)



The program counter indicates the address of the instruction being executed.

The initial value upon reset is undefined.

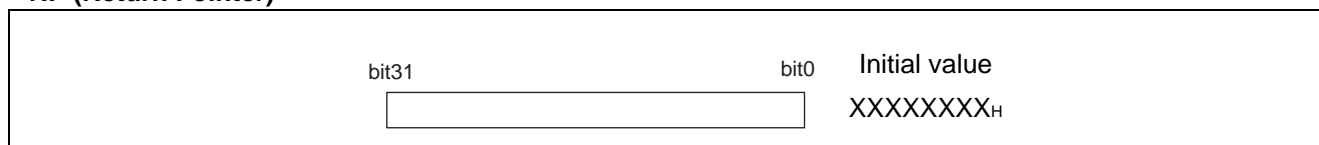
• TBR (Table Base Register)



The table base register holds the first address of the vector table to be used during EIT processing.

The initial value upon reset is "000FFC00H".

• RP (Return Pointer)



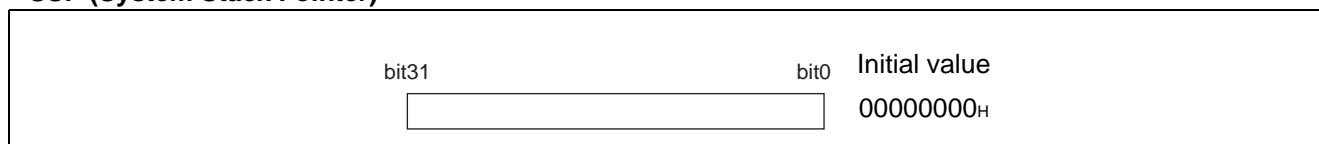
The return pointer holds the return address from a subroutine.

When the CALL instruction is executed, the value of the PC is transferred to the RP.

When the RET instruction is executed, the contents of the RP are transferred to the PC.

The initial value upon reset is undefined.

• SSP (System Stack Pointer)



The SSP is the system stack pointer.

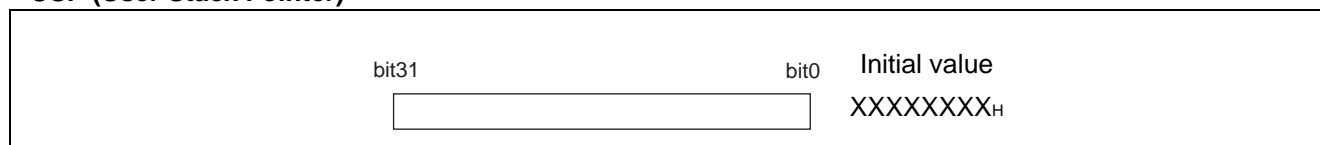
This register is used as an R15 general-purpose register if the S flag of the condition code register (CCR) is "0".

The SSP can also be specified explicitly.

This register is also used as a stack pointer that specifies a stack on which the contents of the PS and PC are to be saved if an EIT occurs.

The initial value upon reset is "00000000H".

• USP (User Stack Pointer)



The USP is the user stack pointer.

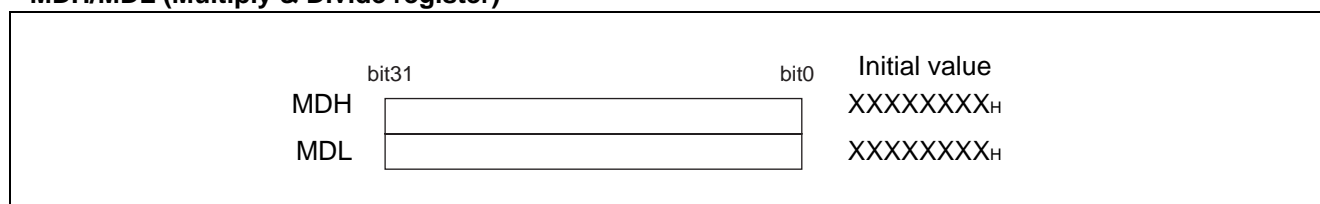
This register is used as an R15 general-purpose register if the S flag of the condition code register (CCR) is “1”.

The USP can also be specified explicitly.

The initial value upon reset is undefined.

This register cannot be used by the RETI instruction.

• MDH/MDL (Multiply & Divide register)



MDH and MDL are the multiply and divide registers. Each register is 32 bits long.

The initial value upon reset is undefined.

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■ MODE SETTINGS

For the FR family, set the operating mode using the mode pins (MD3, MD2, MD1 and MD0) and the mode register (MODR) .

1. Mode pins

Use the four mode pins (MD3, MD2, MD1, and MD0) to specify mode vector fetch.

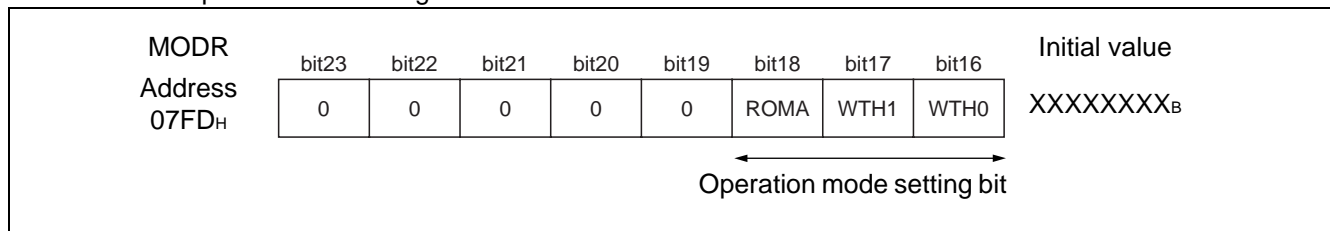
shows the specification related to the mode vector fetch.

Mode pin				Mode name	Reset vector access area	Remarks
MD3	MD2	MD1	MD0			
0	0	0	0	External ROM mode vector	External	With USB. Used at 48 MHz source oscillation.
0	0	1	0	External ROM mode vector	External	Without USB. Used at 16 MHz source oscillation.

Note : The setting other than that shown is prohibited. The single-chip mode is not supported.

2. Mode Register (MODR)

- Detailed explanation of the register

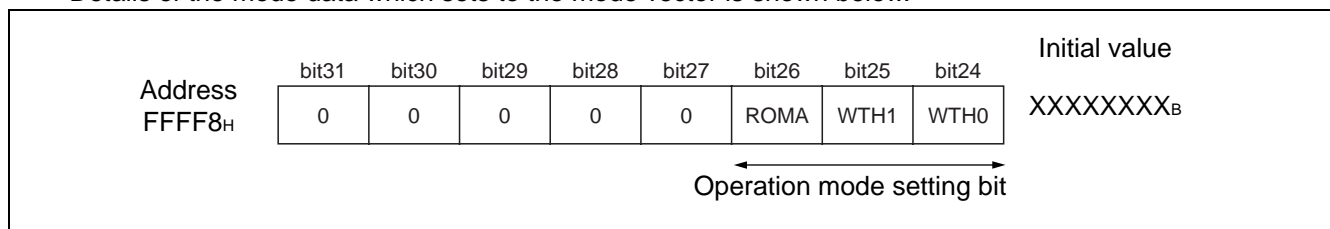


Mode data is data written to the mode register by a mode vector fetch.

After setting to the mode register (MODR) is completed, perform with the operation mode according to this register.

The mode register is set by all reset sources. Accordingly, user program cannot write data to the mode register.

- Detailed explanation of the mode data.
- In the save way of the reset vector, set the mode vector in the vector area.
- Details of the mode data which sets to the mode vector is shown below.



[bit31 to bit27] Reserved bits

Be sure to set "00000_B" to these bits.

Operation when value other than "00000_B" is set cannot guarantee.

[bit26] ROMA (Internal ROM enable bit)

This bit sets whether to enable internal ROM areas.

ROMA	Function	Remarks
0	External ROM mode *	Internal F-bus region (40000 _H to 100000 _H) becomes an external region.
1	Internal ROM mode	Internal F-bus region (40000 _H to 100000 _H) becomes access prohibited (setting disabled) .

* : MB91305 does not contain internal ROM. Use as external ROM mode (setting ROMA = 0) .

[bit25, bit24] WTH1, WTH0 (Bus width specification bit)

Set the bus width specification in external bus mode.

This value is set by DBW1 and DBW0 bits of ACR0 (CS0 area) in the external bus mode.

WTH1	WTH0	Function	Remarks
0	0	8-bit bus width	External bus mode
0	1	16-bit bus width	External bus mode
1	0	32-bit bus width	External bus mode (setting disabled)
1	1	Single-chip mode *	Single-chip mode (setting disabled)

* : not supported.

Note : Mode data set in mode vector must be allocated to “0x000FFFF8_H” as a byte data. In the FR family, since big endian is used as byte endian, the data must be allocated to the most significant byte in bit31 to bit24 as shown below.

Address	bit31	bit24	bit23	bit16	bit15	bit8	bit7	bit0
0x000FFFF8 _H	Mode Data	XXXXXXXX		XXXXXXXX		XXXXXXXX		XXXXXXXX
0x000FFFFC _H	Reset Vector							

MB91305

■ MEMORY SPACE

1. Memory Space

The FR family has a logical address space of 4G bytes (2^{32} addresses) , which the CPU accesses linearly.

• Direct addressing area

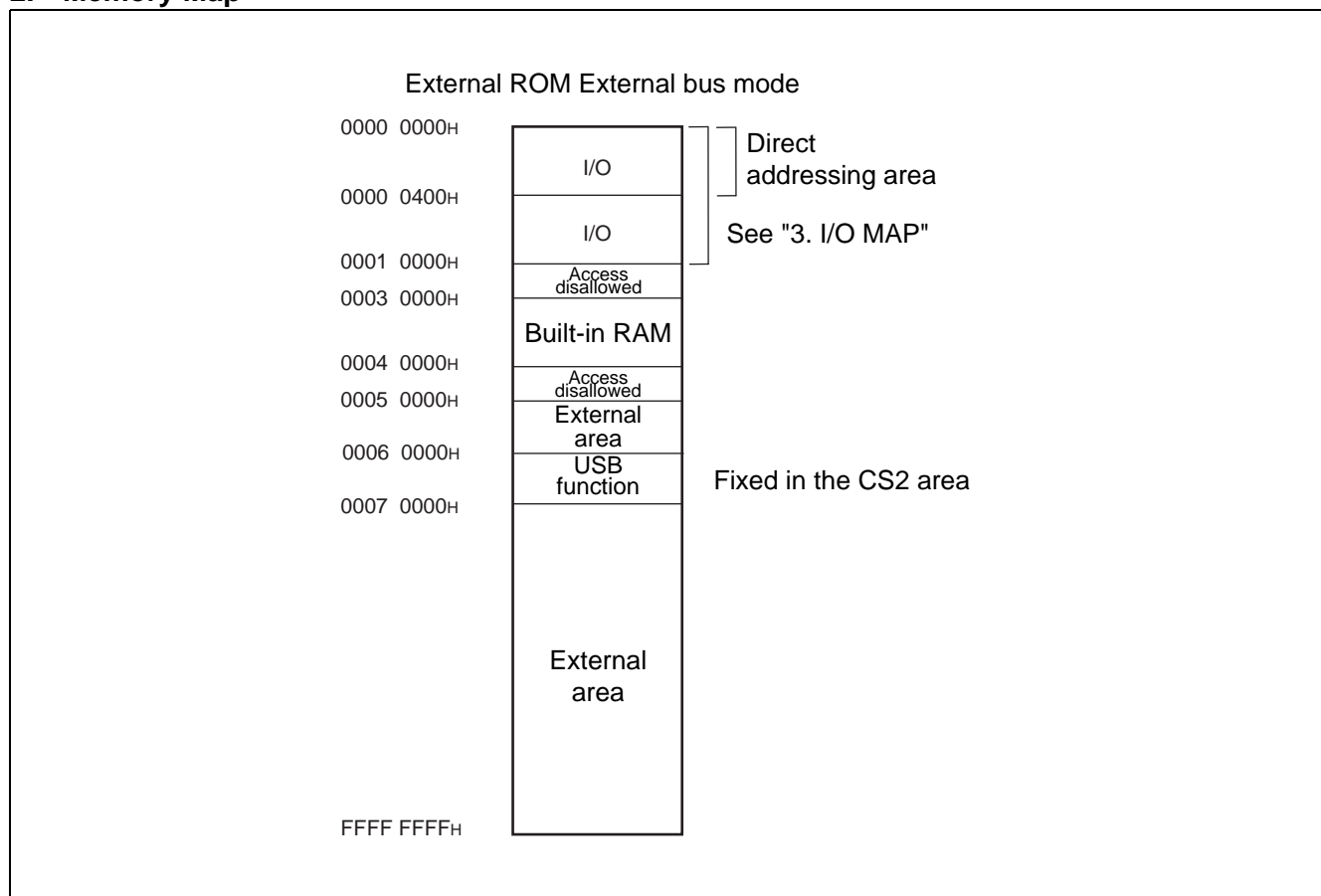
The areas in the address space listed below are used for input-output.

These areas are called the direct addressing area. The address of an operand can be directly specified in an instruction.

The size of the direct addressing area varies according to the size of data to be accessed :

- Byte data access : 000_H to 0FF_H
- Halfword data access : 000_H to 1FF_H
- Word data access : 000_H to 3FF_H

2. Memory Map



Note : Internal RAM area of the MB91305 is "0003 0000_H" to "0003 FFFF_H".

■ I/O MAP

Shows the correspondence between the memory space area and the peripheral resource registers.

Reading the table

Address	Register				Block
	+0	+1	+2	+3	
000000 _H	PDR0 [R/W] X*XXXXX*X	PDR1 [R/W] XXXXXXXX	PDR2 [R/W] XXXXXXXX	PDR3 [R/W] XXXXXXXX	T-unit Port Data Register

Read/write attribute

Initial value of register after reset

Register name (column 1 of the register is at address 4n, column 2 is at address 4n + 2...)

Leftmost register address (For word-length access, column 1 of the register becomes the MSB of the data.)

Note : The initial value of bits in a register are indicated as follows :

“1” : Initial value “1”

“0” : Initial value “0”

“X” : Initial value “X”

“-” : A physical register does not exist at the location.

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Address	Register				Block
	+0	+1	+2	+3	
000000 _H to 00000F _H	—	—	—	—	Reserved
000010 _H	PDR0[R/W] XXXXXXXX	PDR1[R/W] XXXXXXXX	PDR2[R/W] XXXXXXXX	PDR3[R/W] XXXXXXXX	R-bus Port Data Register
000014 _H	PDR4[R/W] XXXXXXXX	PDR5[R/W] XXXXXXXX	PDR6[R/W] --XXXXXX	PDR7[R/W] --XXXXXX	
000018 _H	PDR8[R/W] XXXXXXXX	PDR9[R/W] XXXXXXXX	PDRA[R/W] ----XXX	PDRB[R/W] XXXXXXXX	
00001C _H	PDRC[R/W] XXXXXXXX	PDRD[R/W] --XXXXXX	PDRE[R/W] ----XXX	PDRF[R/W] XXXXXXXX	
000020 _H	ADCTH[R/W] XXXXXXXX00	ADCTL[R/W] 0000X00	ADCH[R/W] 00000000 00000000		10-bit A/D converter
000024 _H	ADAT0[R] XXXXXXXX00 00000000		ADAT1[R] XXXXXXXX00 00000000		
000028 _H	ADAT2[R] XXXXXXXX00 00000000		ADAT3[R] XXXXXXXX00 00000000		
00002C _H	ADAT4[R] XXXXXXXX00 00000000		ADAT5[R] XXXXXXXX00 00000000		
000030 _H	ADAT6[R] XXXXXXXX00 00000000		ADAT7[R] XXXXXXXX00 00000000		
000034 _H	ADAT8[R] XXXXXXXX00 00000000		ADAT9[R] XXXXXXXX00 00000000		
000038 _H	TEST [R/W] 00000000	—	—	—	
00003C _H	—	—	—	—	
000040 _H	HEIRR0 [R/W] 00000000	ENIR0 [R/W] 00000000	ELVR0 [R/W] 00000000		External interrupt
000044 _H	DICR [R/W] -----0	HRCL [R/W] 0--11111	—		DLYI/I-unit
000048 _H	TMRLR0 [W] XXXXXXXXXX XXXXXXXXX		TMR0 [R] XXXXXXXXXX XXXXXXXXX		16-bit Reload Timer 0
00004C _H	—		TMCSR0 [R/W] ---0000 00000000		
000050 _H	TMRLR1 [W] XXXXXXXXXX XXXXXXXXX		TMR1 [R] XXXXXXXXXX XXXXXXXXX		16-bit Reload Timer 1
000054 _H	—		TMCSR1 [R/W] ---0000 00000000		

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
000058 _H	TMRLR2 [W] XXXXXXXX XXXXXXXX		TMR2 [R] XXXXXXXX XXXXXXXX		16-bit Reload Timer 2
00005C _H	—		TMCSR2 [R/W] ----0000 00000000		
000060 _H	SSR0 [R/W] 00001000	SIDR0 [R]/ SODR0 [W] XXXXXXXX	SCR0 [R/W] 00000100	SMR0 [R/W] 00--0-0-	UART0
000064 _H	UTIM0 [R] (UTIMR0 [W]) 00000000 00000000		DRCL0 [W] -----	UTIMC0 [R/W] 0--00001	U-TIMER 0
000068 _H	SSR1 [R/W] 00001000	SIDR1 [R]/ SODR1 [W] XXXXXXXX	SCR1 [R/W] 00000100	SMR1 [R/W] 00--0-0-	UART1
00006C _H	UTIM1 [R] (UTIMR1 [W]) 00000000 00000000		DRCL1 [W] -----	UTIMC1 [R/W] 0--00001	U-TIMER 1
000070 _H	SSR2 [R/W] 00001000	SIDR2 [R]/ SODR2 [W] XXXXXXXX	SCR2 [R/W] 00000100	SMR2 [R/W] 00--0-0-	UART2
000074 _H	UTIM2 [R] (UTIMR2 [W]) 00000000 00000000		DRCL2 [W] -----	UTIMC2 [R/W] 0--00001	U-TIMER 2
000078 _H	SSR3 [R/W] 00001000	SIDR3 [R]/ SODR3 [W] XXXXXXXX	SCR3 [R/W] 00000100	SMR3 [R/W] 00--0-0-	UART3
00007C _H	UTIM3 [R] (UTIMR3 [W]) 00000000 00000000		DRCL3 [W] -----	UTIMC3 [R/W] 0--00001	U-TIMER 3
000080 _H	SSR4 [R/W] 00001000	SIDR4 [R]/ SODR4 [W] XXXXXXXX	SCR4 [R/W] 00000100	SMR4 [R/W] 00--0-0-	UART4
000084 _H	UTIM4 [R] (UTIMR4 [W]) 00000000 00000000		DRCL4 [W] -----	UTIMC4 [R/W] 0--00001	U-TIMER 4
000088 _H	—		—		Reserved
00008C _H	—		—		
000090 _H	PWCCL[R/W] 0000--00	PWCCH[R/W] 00-00000	—		PWC
000094 _H	PWCD[R] XXXXXXXX XXXXXXXX		—		
000098 _H	PWCC2[R/W] 000-----	Reserved	—		
00009C _H	PWCUD[R] XXXXXXXX XXXXXXXX		—		

(Continued)

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Address	Register				Block
	+0	+1	+2	+3	
0000A0 _H	—		—		Reserved
0000A4 _H	—		—		
0000A8 _H	—		—		
0000AC _H	—		—		
0000B0 _H	IFN0 [R] 00000000	IFRN0 [R/W] 00000000	IFCR0 [R/W] 00-00000	IFDR0 [R/W] 00000000	I ² C interface ch.0
0000B4 _H	IBCR0 [R/W] 00000000	IBSR0 [R] 00000000	ITBA0 [R, R/W] 00000000 00000000		
0000B8 _H	ITMK0 [R/W] 00111111 11111111		ISMK0 [R/W] 01111111	ISBA0 [R/W] 00000000	
0000BC _H	—	IDAR0 [R/W] 00000000	ICCR0 [R/W] 00011111	—	
0000C0 _H	IFN1 [R] 00000000	IFRN1 [R/W] 00000000	IFCR1 [R/W] 00-00000	IFDR1 [R/W] 00000000	I ² C interface ch.1
0000C4 _H	IBCR1 [R/W] 00000000	IBSR1 [R] 00000000	ITBA1 [R, R/W] 00000000 00000000		
0000C8 _H	ITMK1 [R/W] 00111111 11111111		ISMK1 [R/W] 01111111	ISBA1 [R/W] 00000000	
0000CC _H	—	IDAR1 [R/W] 00000000	ICCR1 [R/W] 00011111	—	
0000D0 _H	IFN2 [R] 00000000	IFRN2 [R/W] 00000000	IFCR2 [R/W] 00-00000	IFDR2 [R/W] 00000000	I ² C interface ch.2
0000D4 _H	IBCR2 [R/W] 00000000	IBSR2 [R] 00000000	ITBA2 [R, R/W] 00000000 00000000		
0000D8 _H	ITMK2 [R/W] 00111111 11111111		ISMK2 [R/W] 01111111	ISBA2 [R/W] 00000000	
0000DC _H	—	IDA2R [R/W] 00000000	ICCR2 [R/W] 00011111	—	
0000E0 _H	IFN3 [R] 00000000	IFRN3 [R/W] 00000000	IFCR3 [R/W] 00-00000	IFDR3 [R/W] 00000000	I ² C interface ch.3
0000E4 _H	IBCR3 [R/W] 00000000	IBSR3 [R] 00000000	ITBA3 [R, R/W] 00000000 00000000		
0000E8 _H	ITMK3 [R/W] 00111111 11111111		ISMK3 [R/W] 01111111	ISBA3 [R/W] 00000000	
0000EC _H	—	IDAR3 [R/W] 00000000	ICCR3 [R/W] 00011111	—	
0000F0 _H	—	—	—	—	Reserved
0000F4 _H	TCDT [R/W] 00000000 00000000		—	TCCS [R/W] 00000000	16-bit free-run timer

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
0000F8 _H	IPCP1 [R] XXXXXXXX XXXXXXXX		IPCP0 [R] XXXXXXXX XXXXXXXX		16-bit input capture
0000FC _H	IPCP3 [R] XXXXXXXX XXXXXXXX		IPCP2 [R] XXXXXXXX XXXXXXXX		
000100 _H	—	ICS23 [R/W] 00000000	—	ICS01 [R/W] 00000000	Reserved
000104 _H	—	—	—	—	
000108 _H	—	—	—	—	
00010C _H	—	—	—	—	
000110 _H	EIRR1 [R/W] 00000000	ENIR1 [R/W] 00000000	ELVR1 [R/W] 00000000 00000000		External interrupt
000114 _H to 00011F _H	—		—		Reserved
000120 _H	PTMR0 [R] 11111111 11111111		PCSR0 [W] XXXXXXXX XXXXXXXX		PPG0
000124 _H	PDUT0 [W] XXXXXXXX XXXXXXXX		PCNH0 [R/W] 00000000	PCNL0 [R/W] 00000000	
000128 _H	PTMR1 [R] 11111111 11111111		PCSR1 [W] XXXXXXXX XXXXXXXX		PPG1
00012C _H	PDUT1 [W] XXXXXXXX XXXXXXXX		PCNH1 [R/W] 00000000	PCNL1 [R/W] 00000000	
000130 _H	PTMR2 [R] 11111111 11111111		PCSR2 [W] XXXXXXXX XXXXXXXX		PPG2
000134 _H	PDUT2 [W] XXXXXXXX XXXXXXXX		PCNH2 [R/W] 00000000	PCNL2 [R/W] 00000000	
000138 _H	PTMR3 [R] 11111111 11111111		PCSR3[W] XXXXXXXX XXXXXXXX		PPG3
00013C _H	PDUT3 [W] XXXXXXXX XXXXXXXX		PCNH3 [R/W] 00000000	PCNL3 [R/W] 00000000	
000140 _H to 0001FC _H	—				Reserved
000200 _H	DMACA0 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				DMAC
000204 _H	DMACB0 [R/W] 00000000 00000000 00000000 00000000				

(Continued)

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Address	Register				Block
	+0	+1	+2	+3	
000208 _H	DMACA1 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				DMAC
00020C _H	DMACB1 [R/W] 00000000 00000000 00000000 00000000				
000210 _H	DMACA2 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
000214 _H	DMACB2 [R/W] 00000000 00000000 00000000 00000000				
000218 _H	DMACA3 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
00021C _H	DMACB3 [R/W] 00000000 00000000 00000000 00000000				
000220 _H	DMACA4 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
000224 _H	DMACB4 [R/W] 00000000 00000000 00000000 00000000				
000228 _H	—				
00022C _H to 00023C _H	—				
000240 _H	DMACR [R/W] 0XX00000 XXXXXXXX XXXXXXXX XXXXXXXX				
000244 _H to 0002FC _H	—				Reserved
000304 _H	—	—	—	ISIZE[R/W] -----10	I-Cache
000308 _H to 0003E0 _H	—	—	—	—	Reserved
0003E4 _H	—	—	—	ICHCR[R/W] 0-000000	I-Cache
0003E8 _H to 0003EC _H	—	—	—	—	Reserved

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
0003F0 _H	BSD0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Bit Search Module
0003F4 _H	BSD1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0003F8 _H	BSDC [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0003FC _H	BSRR [R] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000400 _H	—	—	DDR2 [R/W] 00000000	DDR3 [R/W] ---0000	R-bus Port Direction Register
000404 _H	DDR4 [R/W] 00000000	DDR5 [R/W] 00000000	DDR6 [R/W] --000000	DDR7 [R/W] --000000	
000408 _H	DDR8 [R/W] ---00000	DDR9 [R/W] 00000000	DDRA [R/W] 00000000	DDRB [R/W] 00000000	
00040C _H	DDRC [R/W] 00000000	DDRD [R/W] --000000	DDRE [R/W] -----00	DDRF [R/W] 00000000	
000410 _H	PFR0 [R/W] 0--00000	PFR1 [R/W] 00000000	PFR2 [R/W] 000---00	PFR3 [R/W] ---0000	R-bus Port Function Register
000414 _H	PFR4 [R/W] ----000	PFR5 [R/W] 11111111	PFR6 [R/W] 00000000	PFR7 [R/W] ----000	
000418 _H	—	PFR9 [R/W] 11111111	—	PFRB [R/W] 00011-0-	
00041C _H	PFRC [R/W] 1111--11	PFRD [R/W] ---101--	PCRA [R/W] 00000000	PCRB [R/W] 00000000	
000420 _H to 00043C _H	—				Reserved
000440 _H	ICR00 [R/W] ---11111	ICR01 [R/W] ---11111	ICR02 [R/W] ---11111	ICR03 [R/W] ---11111	Interrupt Controller
000444 _H	ICR04 [R/W] ---11111	ICR05 [R/W] ---11111	ICR06 [R/W] ---11111	ICR07 [R/W] ---11111	
000448 _H	ICR08 [R/W] ---11111	ICR09 [R/W] ---11111	ICR10 [R/W] ---11111	ICR11 [R/W] ---11111	
00044C _H	ICR12 [R/W] ---11111	ICR13 [R/W] ---11111	ICR14 [R/W] ---11111	ICR15 [R/W] ---11111	
000450 _H	ICR16 [R/W] ---11111	ICR17 [R/W] ---11111	ICR18 [R/W] ---11111	ICR19 [R/W] ---11111	
000454 _H	ICR20 [R/W] ---11111	ICR21 [R/W] ---11111	ICR22 [R/W] ---11111	ICR23 [R/W] ---11111	
000458 _H	ICR24 [R/W] ---11111	ICR25 [R/W] ---11111	ICR26 [R/W] ---11111	ICR27 [R/W] ---11111	

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Address	Register				Block
	+0	+1	+2	+3	
00045C _H	ICR28 [R/W] ---11111	ICR29 [R/W] ---11111	ICR30 [R/W] ---11111	ICR31 [R/W] ---11111	Interrupt Controller
000460 _H	ICR32 [R/W] ---11111	ICR33 [R/W] ---11111	ICR34 [R/W] ---11111	ICR35 [R/W] ---11111	
000464 _H	ICR36 [R/W] ---11111	ICR37 [R/W] ---11111	ICR38 [R/W] ---11111	ICR39 [R/W] ---11111	
000468 _H	ICR40 [R/W] ---11111	ICR41 [R/W] ---11111	ICR42 [R/W] ---11111	ICR43 [R/W] ---11111	
00046C _H	ICR44 [R/W] ---11111	ICR45 [R/W] ---11111	ICR46 [R/W] ---11111	ICR47 [R/W] ---11111	
000470 _H to 00047C _H	—				Reserved
000480 _H	RSRR [R/W] 10000000 * ²	STCR [R/W] 00110011 * ²	TBCR [R/W] 00XXXX00 * ¹	CTBR [W] XXXXXXXX	Clock Control
000484 _H	CLKR [R/W] 00000000 * ¹	WPR [W] XXXXXXXX	DIVR0 [R/W] 00000011 * ¹	DIVR1[R/W] 00000000 * ¹	
000488 _H	—	—	—	—	Reserved
00048C _H	—	—	—	—	
000490 _H	—	—	—	—	
000494 _H to 0005FC _H	—				
000600 _H to 00063F _H	—				
000640 _H	ASR0 [R/W] 00000000 00000000 * ¹		ACR0 [R/W] 1111XX00 00000000 * ¹		T-unit
000644 _H	ASR1 [R/W] XXXXXXXX XXXXXXXX * ¹		ACR1 [R/W] XXXXXXXX XXXXXXXX * ¹		
000648 _H	ASR2 [R/W] XXXXXXXX XXXXXXXX * ¹		ACR2 [R/W] XXXXXXXX XXXXXXXX * ¹		
00064C _H	ASR3 [R/W] XXXXXXXX XXXXXXXX * ¹		ACR3 [R/W] XXXXXXXX XXXXXXXX * ¹		
000650 _H	ASR4 [R/W] XXXXXXXX XXXXXXXX * ¹		ACR4 [R/W] XXXXXXXX XXXXXXXX * ¹		
000654 _H	ASR5 [R/W] XXXXXXXX XXXXXXXX * ¹		ACR5 [R/W] XXXXXXXX XXXXXXXX * ¹		
000658 _H	ASR6 [R/W] XXXXXXXX XXXXXXXX * ¹		ACR6 [R/W] XXXXXXXX XXXXXXXX * ¹		

(Continued)

Address	Register				Block	
	+0	+1	+2	+3		
00065C _H	ASR7 [R/W] XXXXXXXX XXXXXXXX *1		ACR7 [R/W] XXXXXXXX XXXXXXXX *1		T-unit	
000660 _H	AWR0 [R/W] 01111111 11111111 *1		AWR1 [R/W] XXXXXXXX XXXXXXXX *1			
000664 _H	AWR2 [R/W] XXXXXXXX XXXXXXXX *1		AWR3 [R/W] XXXXXXXX XXXXXXXX *1			
000668 _H	AWR4 [R/W] XXXXXXXX XXXXXXXX *1		AWR5 [R/W] XXXXXXXX XXXXXXXX *1			
00066C _H	AWR6 [R/W] XXXXXXXX XXXXXXXX *1		AWR7 [R/W] XXXXXXXX XXXXXXXX *1			
000670 _H	MCRA [R/W] XXXXXXXX	MCRB [R/W] XXXXXXXX	—	—		
000674 _H	—					
000678 _H	IOWR0 [R/W] XXXXXXXX	IOWR1 [R/W] XXXXXXXX	IOWR2 [R/W] XXXXXXXX	—		
00067C _H	—					
000680 _H	CSER [R/W] 00000001	CHER [R/W] 11111111	—	TCR [R/W] 00000000		
000684 _H	RCR [R/W] 00XXXXXXXX XXXX0XXX		—	—		
000688 _H to 0007F8 _H	—					Reserved
0007FC _H	—	MODR [W] XXXXXXXX	—	—		—
000800 _H to 000AFC _H	—					Reserved
000B00 _H	ESTS0 [R/W] X0000000	ESTS1 [R/W] XXXXXXXX	ESTS2 [R] 1XXXXXXXX	—	DSU	
000B04 _H	ECTL0 [R/W] 0X000000	ECTL1 [R/W] 00000000	ECTL2 [W] 000X0000	ECTL3 [R/W] 00X00X11		
000B08 _H	ECNT0 [W] XXXXXXXX	ECNT1 [W] XXXXXXXX	EUSA [W] XXX00000	EDTC [W] 0000XXXX		
000B0C _H	EWP1 [R] 00000000 00000000		—			
000B10 _H	EDTR0 [W] XXXXXXXX XXXXXXXX		EDTR1 [W] XXXXXXXX XXXXXXXX			

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Address	Register				Block
	+0	+1	+2	+3	
000B14 _H to 000B1C _H	—				DSU
000B20 _H	EIA0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B24 _H	EIA1 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B28 _H	EIA2 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B2C _H	EIA3 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B30 _H	EIA4 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B34 _H	EIA5 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B38 _H	EIA6 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B3C _H	EIA7 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B40 _H	EDTA [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B44 _H	EDTM [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B48 _H	EOA0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B4C _H	EOA1 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B50 _H	EPCR [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B54 _H	EPSR [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B58 _H	EIAM0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B5C _H	EIAM1 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B60 _H	EOAM0/EODM0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B64 _H	EOAM1/EODM1 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

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Address	Register				Block	
	+0	+1	+2	+3		
000B68 _H	EOD0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				DSU	
000B6C _H	EOD1 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
000B70 _H to 000FFC _H	—				Reserved	
001000 _H	DMASA0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				DMAC	
001004 _H	DMADA0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
001008 _H	DMASA1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
00100C _H	DMADA1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
001010 _H	DMASA2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
001014 _H	DMADA2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
001018 _H	DMASA3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
00101C _H	DMADA3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
001020 _H	DMASA4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
001024 _H	DMADA4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
001028 _H to 007104 _H	—					Reserved

*1 : Register whose initial value depends on the reset level. The registers at the INIT level are indicated.

*2 : Register whose initial value depends on the reset level. The registers at the INIT level due to the $\overline{\text{INIT}}$ pin are indicated.

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Address	Register				Block
	+0	+1	+2	+3	
00060000 _H	FIFO0o [R] XXXXXXXX XXXXXXXX		FIFO0i [W] XXXXXXXX XXXXXXXX		USB Function
00060004 _H	FIFO1 [R] XXXXXXXX XXXXXXXX		FIFO2 [W] XXXXXXXX XXXXXXXX		
00060008 _H	FIFO3 [R] XXXXXXXX XXXXXXXX		—		
0006000C _H to 0006001F _H	—				
00060020 _H	—		CONT1 [R/W] 000XX0XX XXX00000		
00060024 _H	CONT2 [R/W] XXXXXXXX XXX00000		CONT3 [R/W] XXXXXXXX XXX00000		
00060028 _H	CONT4 [R/W] XXXXXXXX XXX00000		CONT5 [R/W] XXXXXXXX XXXX00XX		
0006002C _H	CONT6 [R/W] XXXXXXXX XXXX00XX		CONT7 [R/W] XXXXXXXX XXX00000		
00060030 _H	CONT8 [R/W] XXXXXXXX XXX00000		CONT9 [R/W] 0XX0XXX 0XXX0000		
00060034 _H	CONT10 [R/W] 00000000 X00000XX		TTSIZE [R/W] 00010001 00010001		
00060038 _H	TRSIZE [R/W] 00010001 00010001		—		
0006003C _H	—				
00060040 _H	RSIZE0 [R] XXXXXXXX XXXX0000		—		
00060044 _H	RSIZE1 [R] XXXXXXXX X0000000		—		
00060048 _H to 0006005F _H	—				
00060060 _H	—		ST1 [R/W] XXXXXX00 00000000		
00060064 _H	—				
00060068 _H	ST2 [R] XXXXXXXX XXX00000		ST3 [R/W] XXXXXXXX XXX00000		
0006006C _H	ST4 [R/W] XXXXX000 00000000		ST5 [R/W] XXXX0XXX XX000000		

(Continued)

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
00060070 _H to 0006007F _H	—				USB Function
00060080 _H to 0006FFFB _H	—				Reserved
0006FFFC _H	—	—	USBRST -0-----	—	USB reset

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■ INTERRUPT SOURCE TABLE

Interrupt source	Interrupt number		Interrupt level	Offset	Address of TBR default	Resource number
	Decimal	Hexa-decimal				
Reset	0	00	—	3FC _H	000FFFFC _H	—
Mode vector	1	01	—	3F8 _H	000FFFF8 _H	—
Reserved for system	2	02	—	3F4 _H	000FFFF4 _H	—
Reserved for system	3	03	—	3F0 _H	000FFFF0 _H	—
Reserved for system	4	04	—	3EC _H	000FFFE _C	—
Reserved for system	5	05	—	3E8 _H	000FFFE8 _H	—
Reserved for system	6	06	—	3E4 _H	000FFFE4 _H	—
No-coprocessor trap	7	07	—	3E0 _H	000FFFE0 _H	—
Coprocessor error trap	8	08	—	3DC _H	000FFFD _C	—
INTE instruction	9	09	—	3D8 _H	000FFFD8 _H	—
Instruction break exception	10	0A	—	3D4 _H	000FFFD4 _H	—
Operand break trap	11	0B	—	3D0 _H	000FFFD0 _H	—
Step trace trap	12	0C	—	3CC _H	000FFFC _C	—
NMI request (tool)	13	0D	—	3C8 _H	000FFFC8 _H	—
Undefined instruction exception	14	0E	—	3C4 _H	000FFFC4 _H	—
NMI request	15	0F	15 (F _H) fixed	3C0 _H	000FFFC0 _H	—
External interrupt 0	16	10	ICR00	3BC _H	000FFFB _C	—
External interrupt 1	17	11	ICR01	3B8 _H	000FFFB8 _H	—
External interrupt 2	18	12	ICR02	3B4 _H	000FFFB4 _H	—
External interrupt 3	19	13	ICR03	3B0 _H	000FFFB0 _H	—
External interrupt 4 (USB-function)	20	14	ICR04	3AC _H	000FFFA _C	—
External interrupt 5	21	15	ICR05	3A8 _H	000FFFA8 _H	—
External interrupt 6	22	16	ICR06	3A4 _H	000FFFA4 _H	—
External interrupt 7	23	17	ICR07	3A0 _H	000FFFA0 _H	—
Reload timer 0	24	18	ICR08	39C _H	000FFF9 _C	8
Reload timer 1	25	19	ICR09	398 _H	000FFF98 _H	9
Reload timer 2	26	1A	ICR10	394 _H	000FFF94 _H	10
UART0 (Reception completed)	27	1B	ICR11	390 _H	000FFF90 _H	0
UART1 (Reception completed)	28	1C	ICR12	38C _H	000FFF8 _C	1
UART2 (Reception completed)	29	1D	ICR13	388 _H	000FFF88 _H	2
UART0 (Transmission completed)	30	1E	ICR14	384 _H	000FFF84 _H	3
UART1 (Transmission completed)	31	1F	ICR15	380 _H	000FFF80 _H	4

(Continued)

Interrupt source	Interrupt number		Interrupt level	Offset	Address of TBR default	Resource number
	Decimal	Hexa-decimal				
UART2 (Transmission completed)	32	20	ICR16	37C _H	000FFF7C _H	5
DMAC0 (end or error)	33	21	ICR17	378 _H	000FFF78 _H	—
DMAC1 (end or error)	34	22	ICR18	374 _H	000FFF74 _H	—
DMAC2 (end or error)	35	23	ICR19	370 _H	000FFF70 _H	—
DMAC3 (end or error)	36	24	ICR20	36C _H	000FFF6C _H	—
DMAC4 (end or error)	37	25	ICR21	368 _H	000FFF68 _H	—
A/D	38	26	ICR22	364 _H	000FFF64 _H	—
PPG0	39	27	ICR23	360 _H	000FFF60 _H	—
PPG1	40	28	ICR24	35C _H	000FFF5C _H	—
PPG2	41	29	ICR25	358 _H	000FFF58 _H	—
PPG3	42	2A	ICR26	354 _H	000FFF54 _H	—
PWC	43	2B	ICR27	350 _H	000FFF50 _H	—
External interrupt 8/U-TIMER0	44	2C	ICR28	34C _H	000FFF4C _H	—
External interrupt 9/U-TIMER1	45	2D	ICR29	348 _H	000FFF48 _H	—
External interrupt 10/U-TIMER2	46	2E	ICR30	344 _H	000FFF44 _H	—
Timebase timer overflow / U-TIMER3	47	2F	ICR31	340 _H	000FFF40 _H	—
External interrupt 11/U-TIMER4	48	30	ICR32	33C _H	000FFF3C _H	—
16-bit free-run timer	49	31	ICR33	338 _H	000FFF38 _H	—
I ² C ch.0	50	32	ICR34	334 _H	000FFF34 _H	—
I ² C ch.1	51	33	ICR35	330 _H	000FFF30 _H	—
I ² C ch.2	52	34	ICR36	32C _H	000FFF2C _H	—
I ² C ch.3	53	35	ICR37	328 _H	000FFF28 _H	—
UART3 (Reception completed)	54	36	ICR38	324 _H	000FFF24 _H	—
UART4 (Reception completed)	55	37	ICR39	320 _H	000FFF20 _H	—
UART3 (Transmission completed)	56	38	ICR40	31C _H	000FFF1C _H	—
UART4 (Transmission completed)	57	39	ICR41	318 _H	000FFF18 _H	—
External interrupt 12/Input capture 0	58	3A	ICR42	314 _H	000FFF14 _H	—
External interrupt 13/Input capture 1	59	3B	ICR43	310 _H	000FFF10 _H	—
External interrupt 14/Input capture 2	60	3C	ICR44	30C _H	000FFF0C _H	—
External interrupt 15/Input capture 3	61	3D	ICR45	308 _H	000FFF08 _H	—
Reserved for system	62	3E	ICR46	304 _H	000FFF04 _H	—
Delayed interrupt source bit	63	3F	ICR47	300 _H	000FFF00 _H	—

(Continued)

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(Continued)

Interrupt source	Interrupt number		Interrupt level	Offset	Address of TBR default	Resource number
	Decimal	Hexa-decimal				
Reserved for system (used by REALOS)	64	40	—	2FC _H	000FFEFC _H	—
Reserved for system (used by REALOS)	65	41	—	2F8 _H	000FFE8 _H	—
Reserved for system	66	42	—	2F4 _H	000FFE4 _H	—
Reserved for system	67	43	—	2F0 _H	000FEF0 _H	—
Reserved for system	68	44	-	2EC _H	000FEEC _H	—
Reserved for system	69	45	—	2E8 _H	000FEE8 _H	—
Reserved for system	70	46	—	2E4 _H	000FEE4 _H	—
Reserved for system	71	47	—	2E0 _H	000FEE0 _H	—
Reserved for system	72	48	—	2DC _H	000FEDC _H	—
Reserved for system	73	49	—	2D8 _H	000FED8 _H	—
Reserved for system	74	4A	—	2D4 _H	000FED4 _H	—
Reserved for system	75	4B	—	2D0 _H	000FED0 _H	—
Reserved for system	76	4C	—	2CC _H	000FECC _H	—
Reserved for system	77	4D	—	2C8 _H	000FEC8 _H	—
Reserved for system	78	4E	—	2C4 _H	000FEC4 _H	—
Reserved for system	79	4F	—	2C0 _H	000FEC0 _H	—
Used in INT instruction	80 to 255	50 to FF	—	2BC _H to 000 _H	000FEBC _H to 000FC00 _H	—

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Rating

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V _{DDE}	V _{SS} - 0.5	V _{SS} + 4.0	V	*2
Power supply voltage (Internal) *1	V _{DDI}	V _{SS} - 0.5	V _{SS} + 2.2	V	*2
Analog power supply voltage*1	AV _{CC}	V _{SS} - 0.5	V _{SS} + 4.0	V	*3
Analog reference voltage*1	AV _{RH}	V _{SS} - 0.5	V _{SS} + 4.0	V	*3
Input voltage*1	V _I	V _{SS} - 0.3	V _{DDE} + 0.3	V	
Analog pin input voltage*1	V _{IA}	V _{SS} - 0.3	AV _{CC} + 0.3	V	
Output voltage*1	V _O	V _{SS} - 0.3	AV _{CC} + 0.3	V	
"L" level maximum output current	I _{OL}	—	10	mA	*4
"L" level average output current	I _{OLAV}	—	4	mA	*5
"L" level total maximum output current	ΣI _{OL}	—	100	mA	
"L" level total average output current	ΣI _{OLAV}	—	50	mA	*6
"H" level maximum output current	I _{OH}	—	-10	mA	*4
"H" level average output current	I _{OHAV}	—	-4	mA	*5
"H" level total maximum output current	ΣI _{OH}	—	-50	mA	
"H" level total average output current	ΣI _{OHAV}	—	-20	mA	*6
Power consumption	P _D	—	750	mW	
Operating temperature	T _a	-10	+70	°C	
Storage temperature	T _{STG}	—	+150	°C	

*1 : This parameter is based on AV_{SS} = V_{SS} = 0.0 V.

*2 : V_{DDE} must not be lower than V_{SS} - 0.3 V.

*3 : Be careful not to exceed V_{DDE} + 0.3 V, for example, when power is turned on.

*4 : Maximum output current determines the peak value of any one of corresponding pins.

*5 : Average output current is defined as the value of the average current flowing over 100 ms at any one of the corresponding pins.

*6 : Average total output current is defined as the value of the average current flowing over 100 ms at all of the corresponding pins.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

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2. Recommended Operating Conditions

($V_{SS} = AV_{SS} = 0\text{ V}$)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power supply voltage	V_{DDE}	3.0	3.6	V	
	V_{DDI}	1.65	1.95	V	
Analog power supply voltage	AV_{CC}	$V_{SS} - 0.3$	$V_{SS} + 3.6$	V	
Analog reference voltage	AV_{RH}	AV_{SS}	AV_{CC}	V	
Operating temperature	T_a	-10	+70	°C	

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

3. DC Characteristics

(1) CPU

($V_{DDI} = 1.8 \text{ V} \pm 0.15 \text{ V}$, $V_{DDE} = AV_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$, $V_{SS} = AV_{SS} = 0 \text{ V}$, $T_a = -10 \text{ }^\circ\text{C}$ to $+70 \text{ }^\circ\text{C}$)

Parameter	Symbol	Pin	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
“H” level input voltage	V_{IH}	D31 to D16	—	$0.7 \times V_{DDE}$	—	$V_{DDE} + 0.3$	V	
	V_{HIS}	Input ports except for D31 to D16	—	$0.8 \times V_{DDE}$	—	$V_{DDE} + 0.3$	V	Hysteresis input
“L” level input voltage	V_{IL}	D31 to D16	—	V_{SS}	—	$0.25 \times V_{DDE}$	V	
	V_{ILS}	Input ports except for D31 to D16	—	V_{SS}	—	$0.2 \times V_{DDE}$	V	Hysteresis input
“H” level output voltage	V_{OH}	All output pins	$V_{DDE} = 3.0 \text{ V}$ $I_{OH} = -4.0 \text{ mA}$	$V_{DDE} - 0.5$	—	V_{DDE}	V	
“L” level output voltage	V_{OL}	All output pins	$V_{DDE} = 3.0 \text{ V}$ $I_{OL} = 4.0 \text{ mA}$	V_{SS}	—	0.4	V	
Input leak current (High-Z output Leakage current)	I_{LI}	All input pins	$V_{DDE} = 3.6 \text{ V}$ $0.45 \text{ V} < V_I < V_{DDE}$	-5	—	+5	μA	
Pull-up resistance	R_{UP}	*1	$V_{DDE} = 3.6 \text{ V}$ $V_I = 0.45 \text{ V}$	12	25	100	$\text{k}\Omega$	
Pull-down resistance	R_{DOWN}	*2	$V_{DDE} = 3.6 \text{ V}$ $V_I = 3.3 \text{ V}$	12	25	100	$\text{k}\Omega$	
Power supply current	I_{CC}	VDDE, VDDI	$f_C = 16.5 \text{ MHz}$ $V_{DDE} = 3.3 \text{ V}$ $V_{DDI} = 1.8 \text{ V}$	—	120	180	mA	(Multiply by 4) When operating at 66 MHz
	I_{CCS}		$f_C = 16.5 \text{ MHz}$ $V_{DDE} = 3.3 \text{ V}$ $V_{DDI} = 1.8 \text{ V}$	—	60	90	mA	at sleep
	I_{CCH}		$T_a = +25 \text{ }^\circ\text{C}$ $V_{DDE} = 3.3 \text{ V}$ $V_{DDI} = 1.8 \text{ V}$	—	200	1000	μA	at stop
Input capacitance	C_{IH}	Other than VDDE, VSS AVCC and AVSS	—	—	10	—	pF	

*1 : Pins that the I/O circuit type is B and G

*2 : Pins that the I/O circuit type is J

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(2) USB

[1] DC characteristics

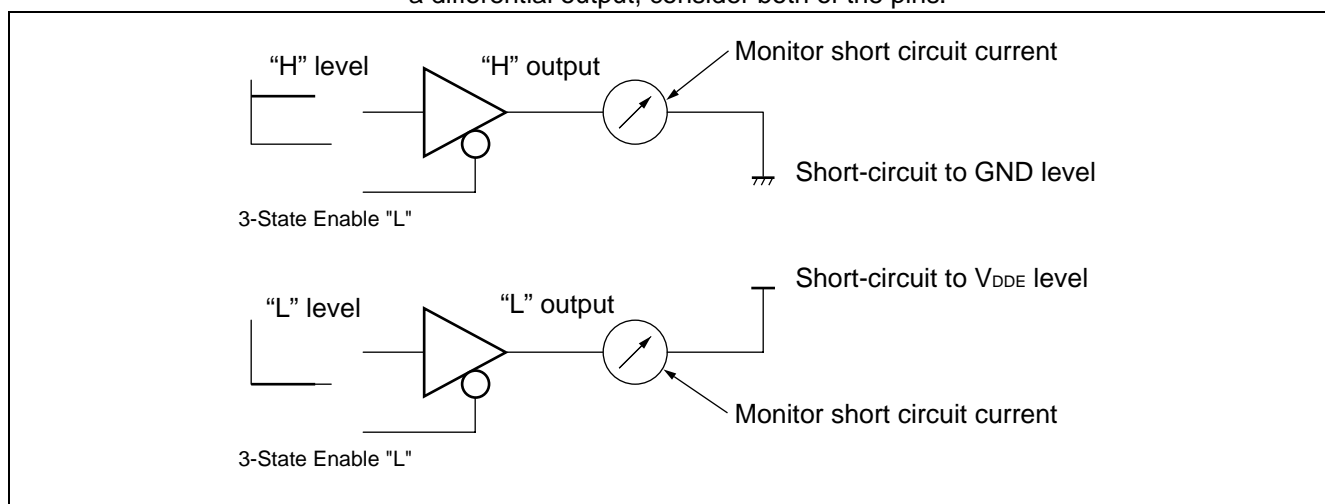
($V_{DDI} = 1.8 \text{ V} \pm 0.15 \text{ V}$, $V_{DDE} = AV_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$, $V_{SS} = AV_{SS} = 0 \text{ V}$, $T_a = -10 \text{ }^\circ\text{C}$ to $+70 \text{ }^\circ\text{C}$)

Parameter	Symbol	Pin	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level output voltage	V_{OH}	—	$I_{OH} = -100 \mu\text{A}$	$V_{DDE} - 0.2$	—	V_{DDE}	V	
"L" level output voltage	V_{OL}	—	$I_{OL} = 100 \mu\text{A}$	0	—	0.2	V	
"H" level output voltage	I_{OH}	—	Full Speed $V_{OH} = V_{DDE} - 0.4 \text{ V}$	-20	—	—	mA	
		—	Low Speed $V_{OH} = V_{DDE} - 0.4 \text{ V}$	-6	—	—		
"L" level output voltage	I_{OL}	—	Full Speed $V_{OL} = 0.4 \text{ V}$	20	—	—	mA	
		—	Low Speed $V_{OL} = 0.4 \text{ V}$	6	—	—		
Output Short-Circuit Current	I_{OS}	—	—	—	—	300	mA	*1
Input leak current	I_{LZ}	—	—	—	—	± 5	μA	*2

*1 : < Output Short Circuit Current I_{OS} >

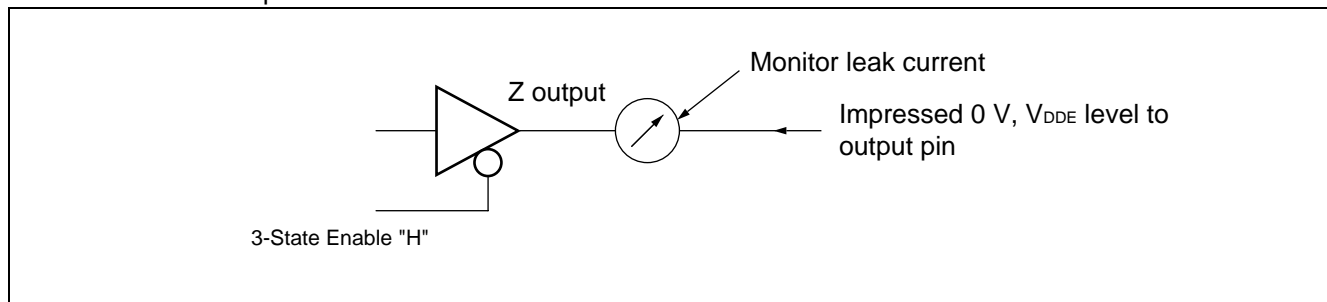
The output short circuit current I_{OS} is the maximum current that flows when the output pin is connected to V_{DDE} or V_{SS} pin (within the maximum rating) .

Output Short Circuit Current : The output short circuit current's value is the short-circuit current value of one terminal in one side of the differential output terminal. As this USB I/O buffer is a differential output, consider both of the pins.



*2 : < Z leak current I_{LZ} measurement >

The leak current when V_{DDE} or V_{SS} potential is impressed to bi-directional pin at high-impedance state of USB I/O buffer is the input leak current I_{LZ} .



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[2] DC Characteristics

Conform to USB Specification Revision 1.1

($V_{DDI} = 1.8 \text{ V} \pm 0.15 \text{ V}$, $V_{DDE} = AV_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$, $V_{SS} = AV_{SS} = 0 \text{ V}$, $T_a = -10 \text{ }^\circ\text{C}$ to $+70 \text{ }^\circ\text{C}$)

Parameter		Symbol	Value		Unit	Remarks
			Min	Max		
Input Levels	High (driven)	V_{IH}	2.0	—	V	*1
	Low	V_{IL}	—	0.8	V	*1
	Differential Input Sensitivity	V_{DI}	0.2	—	V	*2
	Common Mode Range	V_{CM}	0.8	2.5	V	*2
Output Levels	Low	V_{OL}	0.0	0.3	V	*3
	High (driven)	V_{OH}	2.8	3.6	V	*3
	Differential Output Signal Voltage	V_{CRS}	1.3	2.0	V	*4
Terminations	Bus Pull-Up Resistor on Upstream Port	R_{PU}	1.425	1.575	k Ω	$1.5 \text{ k}\Omega \pm 5\%$
	Bus Pull-Down Resistor on Downstream Port	R_{PD}	1.425	1.575	k Ω	$1.5 \text{ k}\Omega \pm 5\%$
	Termination Voltage for Upstream Port Pull-Up	V_{TERM}	3.0	3.6	V	*5

*1 : < Input Levels V_{IH} and V_{IL} >

The switching-threshold voltage of the single-end-receiver in USB I/O buffer is set within the following range; V_{IL} (Max) = 0.8 V, V_{IH} (Min) = 2.0 V (TTL input standard).

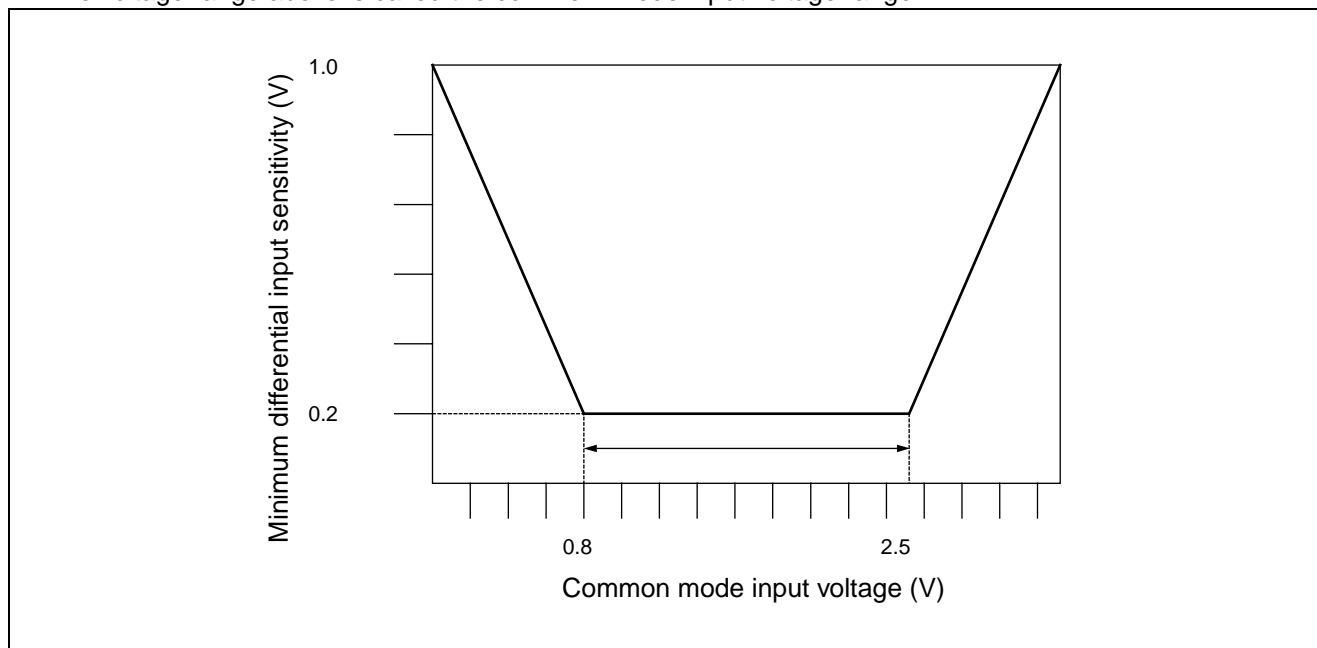
And, to fall the noise sensitivity, a little hysteresis is set.

*2 : < Input Levels V_{DI} and V_{CM} >

Reception of the USB differential data signal uses the differential-receiver.

The differential input sensitivity of the differential-receiver is 200 mV, when the difference voltage between the differential data input and local ground reference level is the following ranges; 0.8 V to 2.5 V.

The voltage range above is called the common² mode input voltage range.

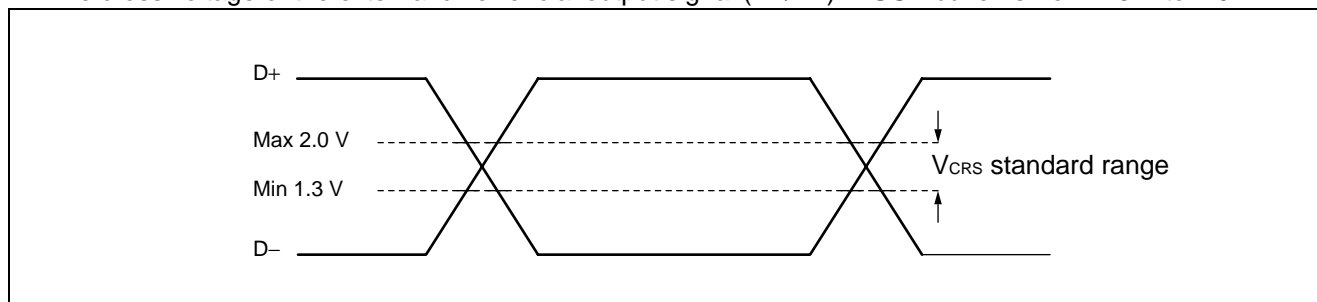
*3 : < Output Levels V_{OL} and V_{OH} >

The driver's output driving ability is set to following;

- at low state (V_{OL}) : less than 0.3 V (vs. 3.6 V, 1.5 k Ω load)
- at high state (V_{OH}) : more than 2.8 V (vs. ground, 1.5 k Ω load)

*4 : < Output Levels V_{CRS} >

The cross voltage of the external differential output signal ($D+/D-$) in USB buffer is from 1.3 V to 2.0 V.

*5 : < Terminations V_{TERM} >

Pull-up voltage for the upstream port is shown.

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4. AC Characteristics

(1) Clock timing ratings

($V_{DDI} = 1.8\text{ V} \pm 0.15\text{ V}$, $V_{DDE} = AV_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_{SS} = AV_{SS} = 0\text{ V}$, $T_a = -10\text{ }^\circ\text{C}$ to $+70\text{ }^\circ\text{C}$)

Parameter	Symbol	Pin	Condi- tions	Value		Unit	Remarks
				Min	Max		
Clock frequency (1)	f _c	X0 X1	—	37.5	48	MHz	Using PLL*1
				12.5	16	MHz	
Clock cycle time	t _c	X0 X1	—	—	20.8	ns	
				—	62.5	ns	
Clock frequency (2)	f _c	X0 X1	—	10	50	MHz	Self-oscillation (1/2 division input)
Clock frequency (3)	f _c	X0 X1		10	50	MHz	At external clock
Clock cycle time	t _c	X0 X1		40	100	ns	
Input clock pulse width	P _{WH} P _{WL}	X0 X1		16	—	ns	
Input clock rise time and fall time	t _{CR} t _{CF}	X0 X1		—	8	ns	
Internal operating clock frequency	f _{CP}	—		—	3.125*2	64	MHz
	f _{CPP}		3.125*2		32	MHz	Peripheral
	f _{CPT}		3.125*2		32	MHz	External bus
Internal operating clock cycle time	t _{CP}	—	—	15.6	1280*2	ns	CPU
	t _{CPP}			31.2	1280*2	ns	Peripheral
	t _{CPT}			31.2	1280*2	ns	External bus

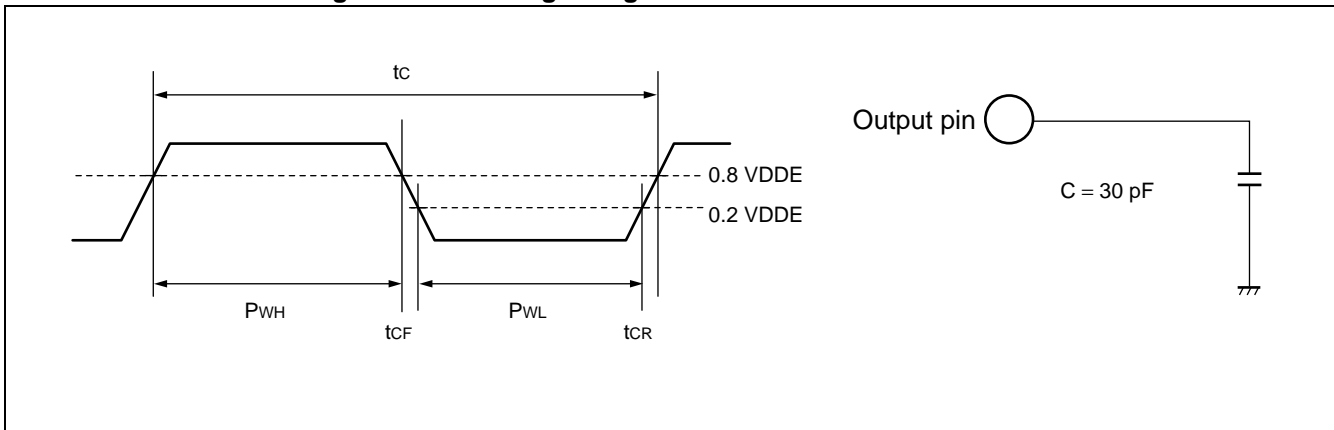
*1 : This value is as follows;

- With USB function (MD pin = 0000_B) : 37.5 MHz to 48 MHz And using USB: fixed to 48 MHz
(operation at a maximum internal speed of 64 MHz by
quadrupling a self-oscillation frequency of 48 MHz via PLL of
divided by 3.)
- Without USB function (MD pin = 0010_B) : 12.5 MHz to 16 MHz
(operation at a maximum internal speed of 64 MHz by
quadrupling a self-oscillation frequency of 16 MHz via PLL.)

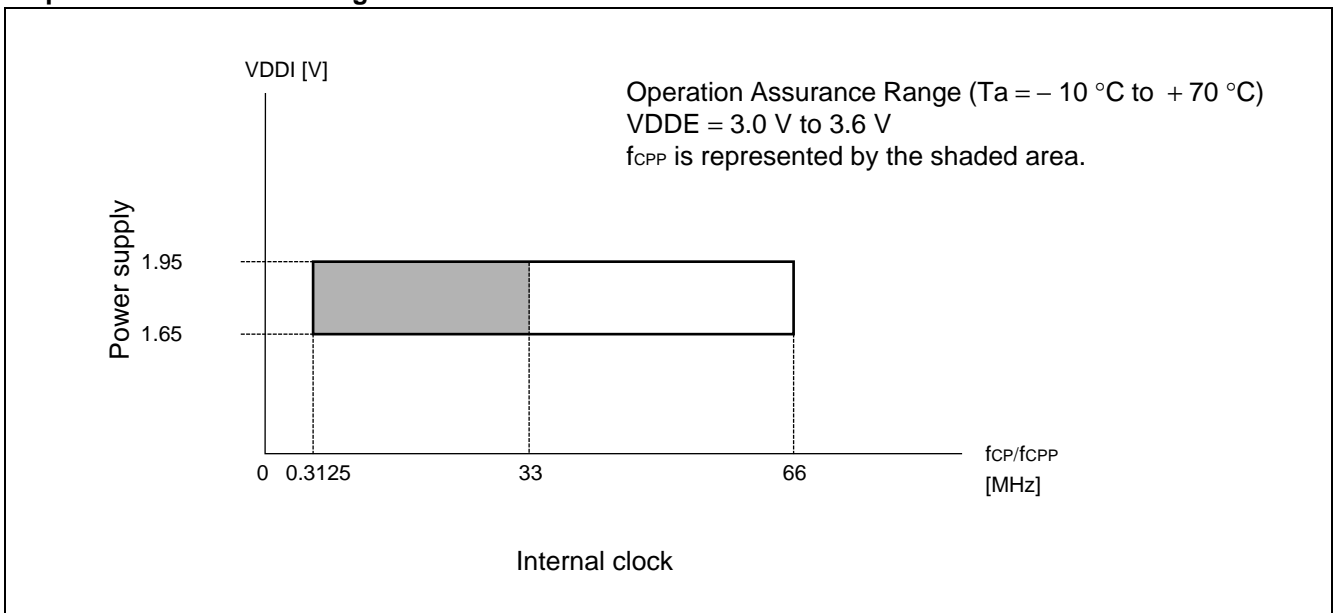
*2 : The values shown represent a minimum clock frequency of 12.5 MHz input at the X0 pin, using the oscillation circuit PLL and a gear ratio of 1/16.

$$12.5\text{ [MHz]} \times 4\text{ (multiply)} \times 1/16\text{ (gear 1/16)} = 3.125\text{ [MHz]}$$

• **Conditions for measuring the clock timing ratings**

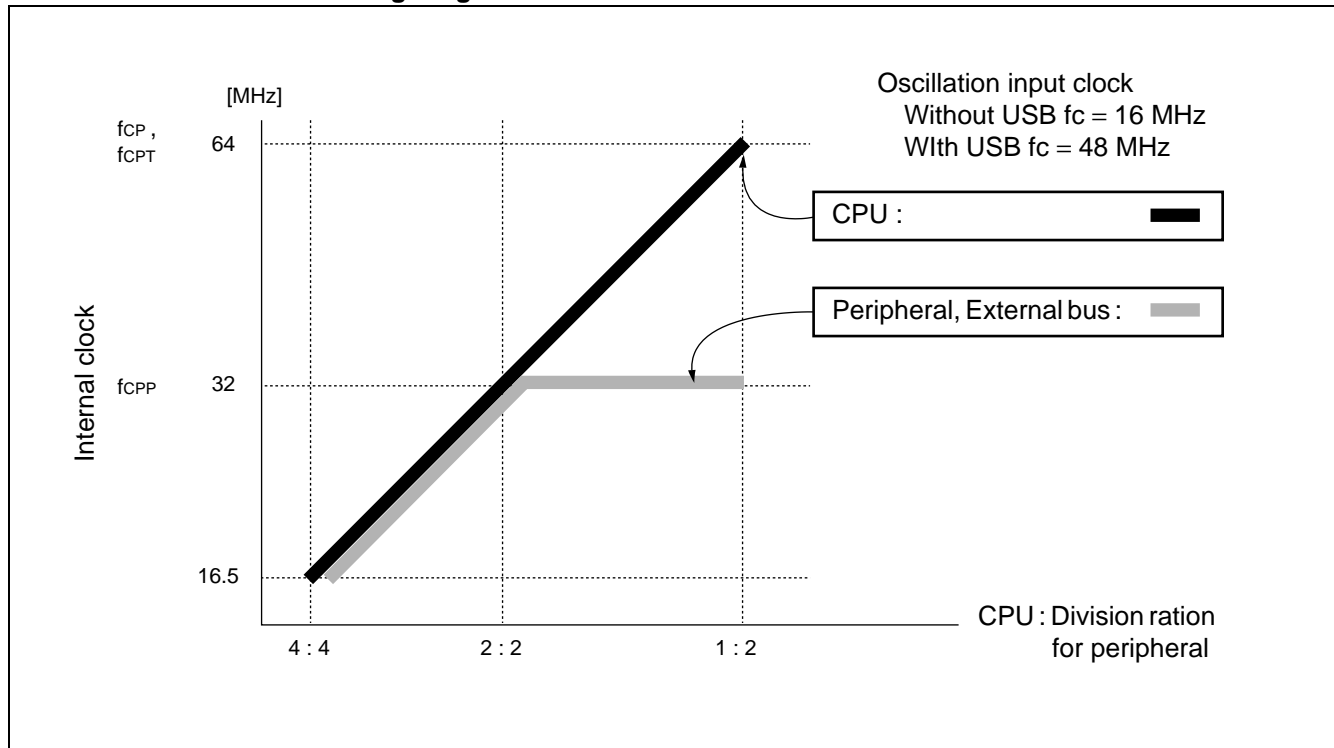


• **Operation Assurance Range**



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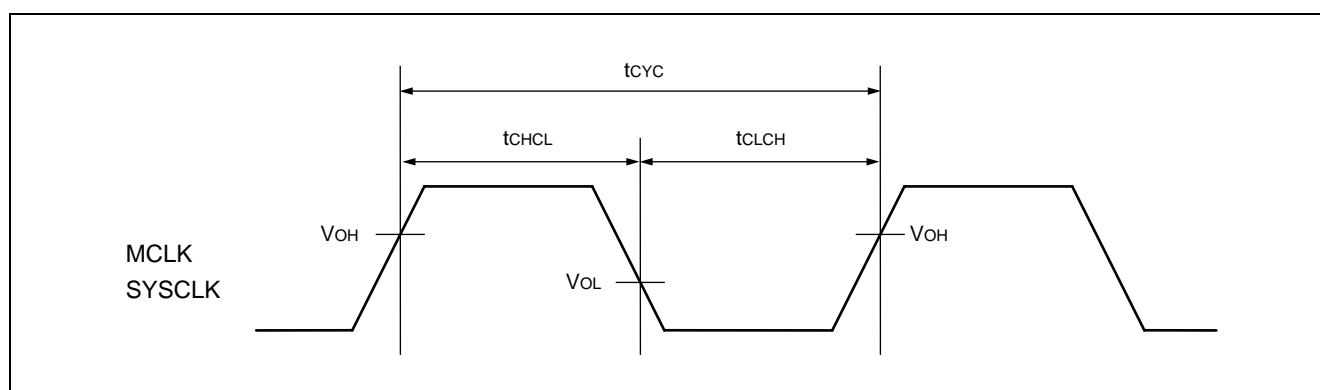
• External/internal clock setting range



- Notes :
- When the PLL is used, the external clock input must fall between 12.5 MHz and 16.5 MHz.
 - Set the PLL oscillation stabilization wait time longer than 500 μ s.
 - The internal clock gear setting should not exceed the relevant value in the table in (1) "Clock timing ratings".

(2) Clock output timing(V_{DDI} = 1.8 V ± 0.15 V, V_{DDE} = AV_{CC} = 3.3 V ± 0.3 V, V_{SS} = AV_{SS} = 0 V, Ta = -10 °C to +70 °C)

Parameter	Symbol	Pin	Condi- tions	Value		Unit	Remarks
				Min	Max		
Cycle time	t _{CYC}	MCLK SYSCLK	—	t _{CPT}	—	ns	*1
MCLK (SYSCLK) ↑ → MCLK (SYSCLK) ↓	t _{CHCL}	MCLK SYSCLK		1/2 × t _{CYC} - 3	1/2 × t _{CYC} + 3	ns	*2
MCLK (SYSCLK) ↓ → MCLK (SYSCLK) ↑	t _{CLCL}	MCLK SYSCLK		1/2 × t _{CYC} - 3	1/2 × t _{CYC} + 3	ns	*3

*1 : t_{CYC} is the frequency of one clock cycle after gearing.

*2 : The following ratings are for the gear ratio set to 1.

For the ratings when the gear ratio is set to between 1/2, 1/4 and 1/8, substitute 1/2, 1/4 or 1/8 for n in the following equation.

$$t_{CHCL} = (1/2 \times 1/n) \times t_{CYC} - 10$$

*3 : The following rating are for the gear ratio set to 1.

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(3) Reset and hardware standby input ratings

($V_{DDI} = 1.8 \text{ V} \pm 0.15 \text{ V}$, $V_{DDE} = AV_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$, $V_{SS} = AV_{SS} = 0 \text{ V}$, $T_a = -10 \text{ }^\circ\text{C}$ to $+70 \text{ }^\circ\text{C}$)

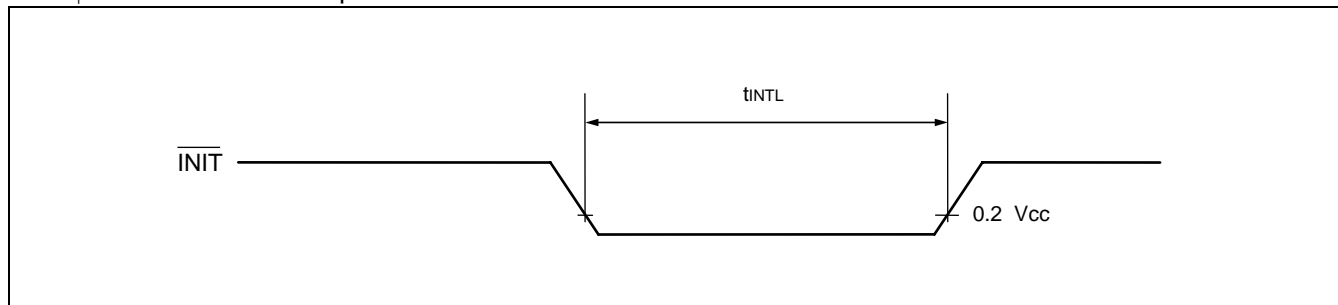
Parameter	Symbol	Pin	Condi- tions	Value		Unit	Remarks
				Min	Max		
$\overline{\text{INIT}}$ input time (at power-on)	t_{INTL}	$\overline{\text{INIT}}$	—	*	—	ns	
$\overline{\text{INIT}}$ input time (other than at power-on)				$t_{\text{CP}} \times 5$	—	ns	

* : $\overline{\text{INIT}}$ input time (at power-on)

FAR resonator, ceramic oscillator : $\phi \times 2^{15}$ or greater recommended

Crystal : $\phi \times 2^{21}$ or greater recommended

ϕ : Power on \rightarrow X0/X1 period $\times 2$



(4-1) Normal bus access read/write operation(V_{DDI} = 1.8 V ± 0.15 V, V_{DDE} = AV_{CC} = 3.3 V ± 0.3 V, V_{SS} = AV_{SS} = 0 V, Ta = -10 °C to +70 °C)

Parameter	Symbol	Pin	Condi- tions	Value		Unit	Remarks
				Min	Max		
$\overline{CS0}/\overline{CS1}/\overline{CS4}/\overline{CS5}/\overline{CS6}/\overline{CS7}$ setup	t _{CSLCH}	MCLK/SYSCLK $\overline{CS0}$ to $\overline{CS7}$	—	3	—	ns	
$\overline{CS0}/\overline{CS1}/\overline{CS4}/\overline{CS5}/\overline{CS6}/\overline{CS7}$ hold	t _{CSHCH}			3	t _{cyc} / 2 + 6	ns	
Address setup	t _{ASCH}	MCLK/SYSCLK A23 to A0	—	3	—	ns	
Address hold	t _{CHAX}			3	t _{cyc} / 2 + 6	ns	
Valid address → Valid data input time	t _{AVDV}	A23 to A0 D31 to D16	—	—	3/2 × t _{cyc} - 15	ns	*1 *2
$\overline{WR0}$, $\overline{WR1}$ delay time	t _{CHWL}	MCLK/SYSCLK $\overline{WR0}$, $\overline{WR1}$		—	6	ns	
$\overline{WR0}$, $\overline{WR1}$ delay time	t _{CHWH}		—	6	ns		
$\overline{WR0}$, $\overline{WR1}$ minimum pulse width	t _{WLWH}	$\overline{WR0}$, $\overline{WR1}$	t _{cyc} - 3	—	ns		
Data setup → \overline{WRx} ↑	t _{DSWH}	$\overline{WR0}$, $\overline{WR1}$ D31 to D16	—	t _{cyc}	—	ns	
\overline{WRx} ↑ → Data hold time	t _{WHDX}			5	—	ns	
\overline{RD} delay time	t _{CHRL}	MCLK/SYSCLK \overline{RD}	—	—	6	ns	
\overline{RD} delay time	t _{CHRH}			—	6	ns	
\overline{RD} ↓ → Valid data input time	t _{RLDV}	\overline{RD} D31 to D16	—	—	t _{cyc} - 15	ns	*1
Data setup → \overline{RD} ↑ Time	t _{DSRH}			15	—	ns	
\overline{RD} ↑ → Data hold time	t _{RHDX}			0	—	ns	
\overline{RD} minimum pulse width	t _{RLRH}			t _{cyc} - 3	—	ns	
\overline{AS} setup	t _{ASLCH}	MCLK/SYSCLK \overline{AS}	—	3	—	ns	
\overline{AS} hold	t _{ASHCH}			3	—	ns	

*1 : When the bus timing is delayed by automatic wait insertion or RDY input, add the time (t_{cyc} × the number of cycles added for the delay) to this rating.

*2 : The following ratings are for the gear ratio set to 1.

For the ratings when the gear ratio is set to between 1/2, 1/4 and 1/8, substitute 1/2, 1/4 and 1/8 for n in the following equation.

$$t_{AVDV} : 3 / (2n) \times t_{cyc} - 15$$

(4-2) Multiplex bus access read/write operation(V_{DDI} = 1.8 V ± 0.15 V, V_{DDE} = AV_{CC} = 3.3 V ± 0.3 V, V_{SS} = AV_{SS} = 0 V, Ta = -10 °C to +70 °C)

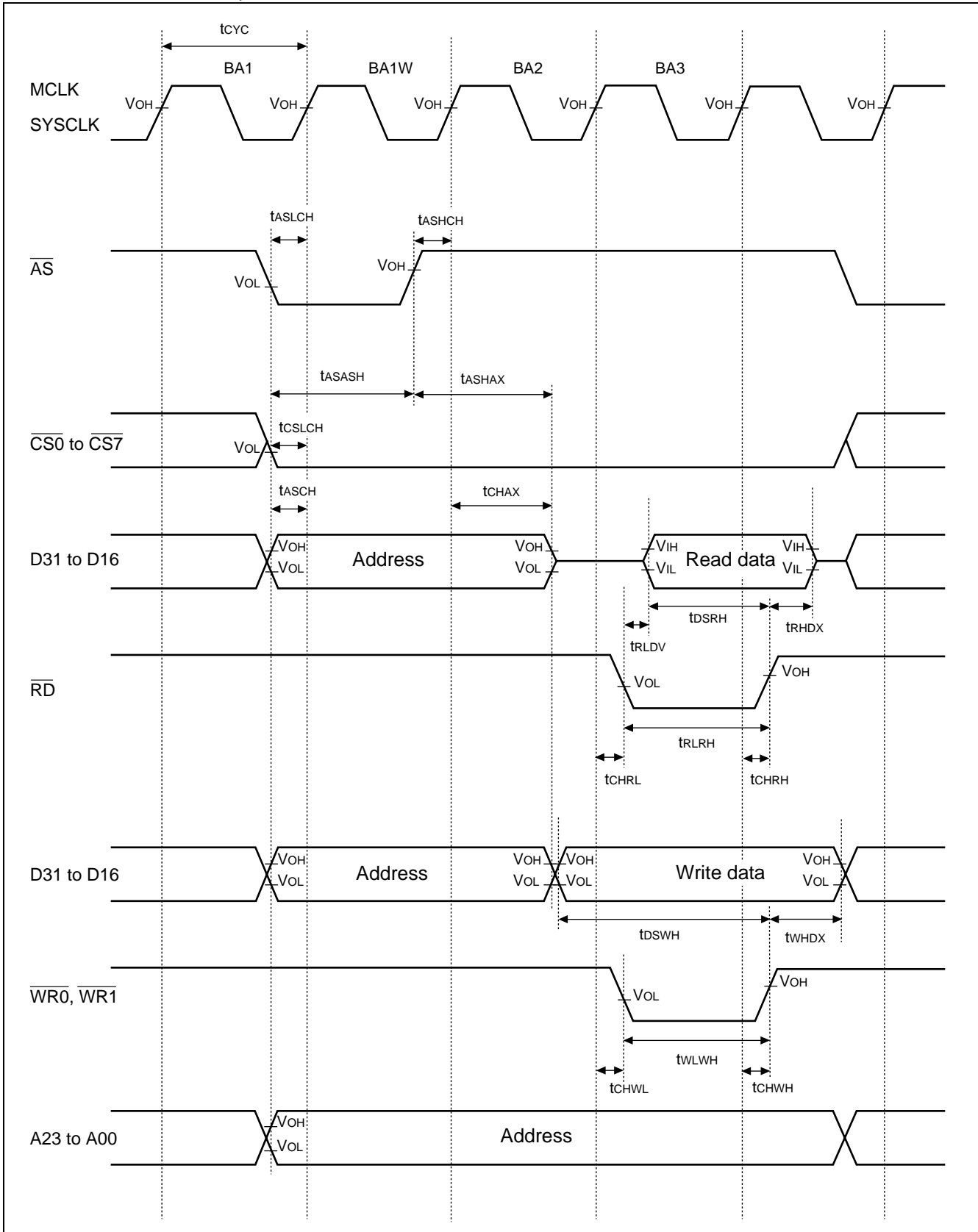
Parameter	Symbol	Pin	Condi- tions	Value		Unit	Remarks
				Min	Max		
D31 to D16 address setup time → MCLK (SYSCLK) ↑	t _{ASCH}	MCLK/SYSCLK D31 to D16 (address)	—	3	—	ns	
MCLK (SYSCLK) ↑ → D31 to D16 address hold time	t _{CHAX}			3	t _{CYC} / 2 + 6	ns	
D31 to D16 address setup time → \overline{AS} ↑	t _{ASASH}	\overline{AS} D31 to D16 (address)		12	—	ns	*
\overline{AS} ↑ → D31 to D16 address hold time	t _{ASHAX}			t _{CYC} - 3	t _{CYC} + 3	ns	*

* : At $\overline{CS} \rightarrow \overline{RD}/\overline{WR}$ setup extension = 1

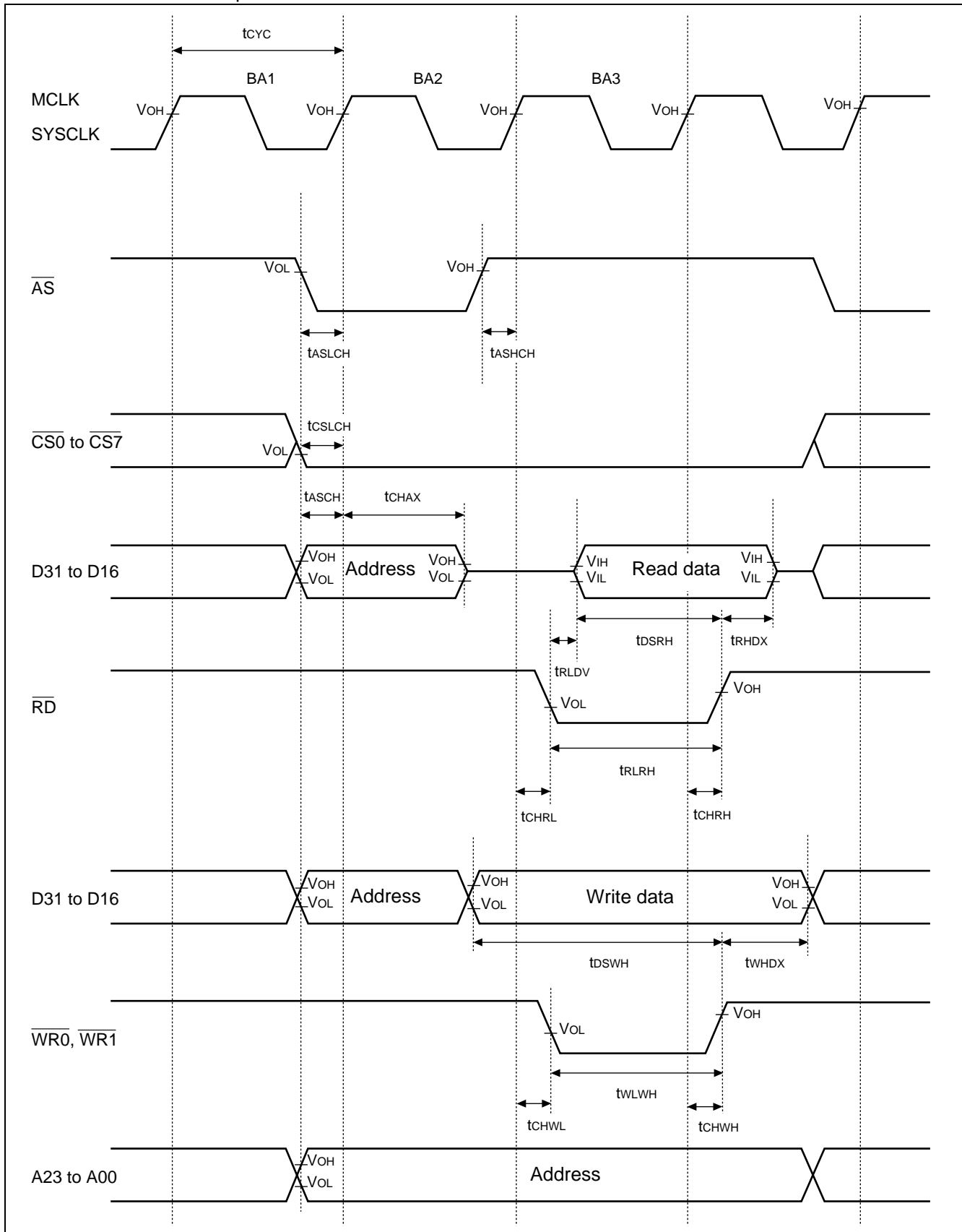
Note : Use the same rating as normal bus interface except for this rating.

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- At $\overline{CS} \rightarrow \overline{RD}/\overline{WR}$ setup extension = 1



- At $\overline{CS} \rightarrow \overline{RD}/\overline{WR}$ setup extension = 0

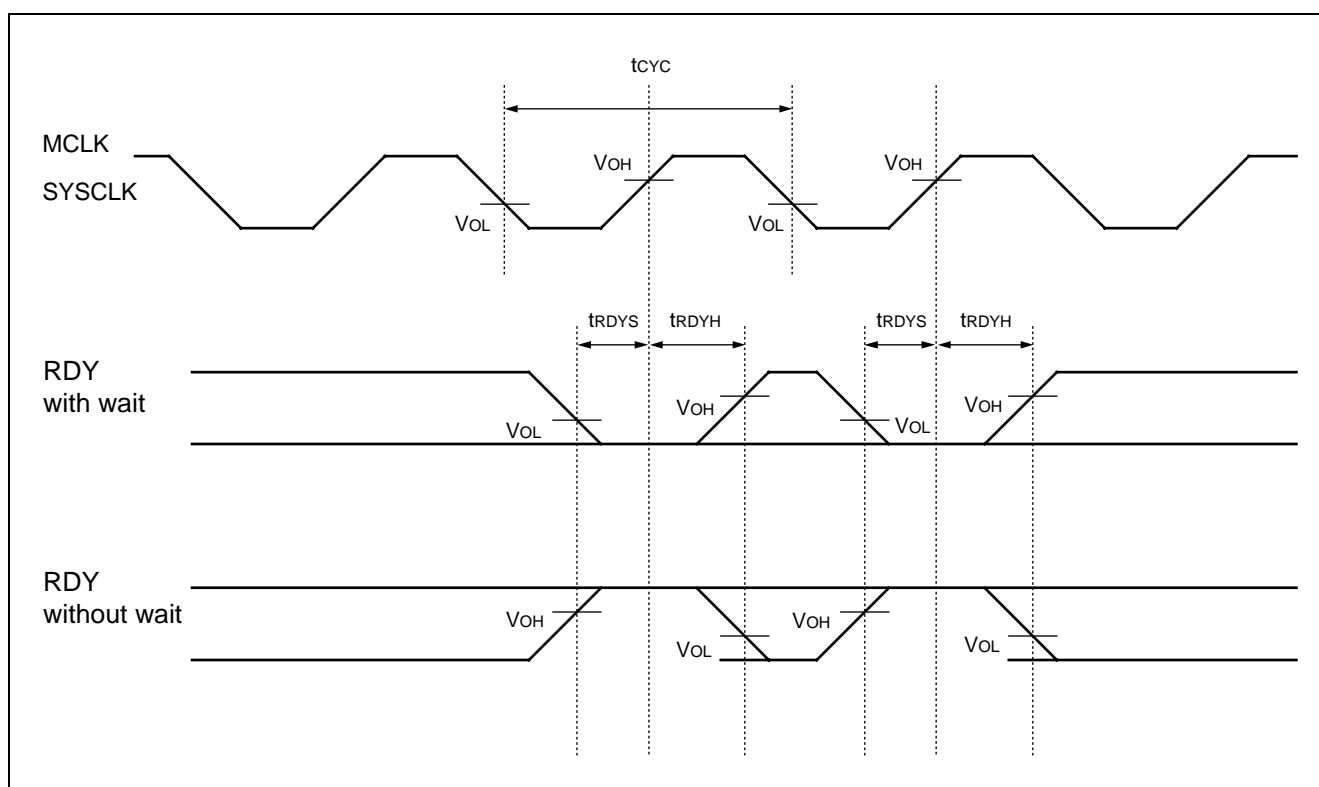


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(5) Ready input timings

($V_{DDI} = 1.8 \text{ V} \pm 0.15 \text{ V}$, $V_{DDE} = AV_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$, $V_{SS} = AV_{SS} = 0 \text{ V}$, $T_a = -10 \text{ }^\circ\text{C to } +70 \text{ }^\circ\text{C}$)

Parameter	Symbol	Pin	Condi- tions	Value		Unit	Remarks
				Min	Max		
RDY setup time → MCLK (SYSCLK) ↓	t_{RDYS}	MCLK SYSCLK RDY	—	10	—	ns	
MCLK (SYSCLK) ↓ → RDY hold time	t_{RDYH}	MCLK SYSCLK RDY	—	0	—	ns	

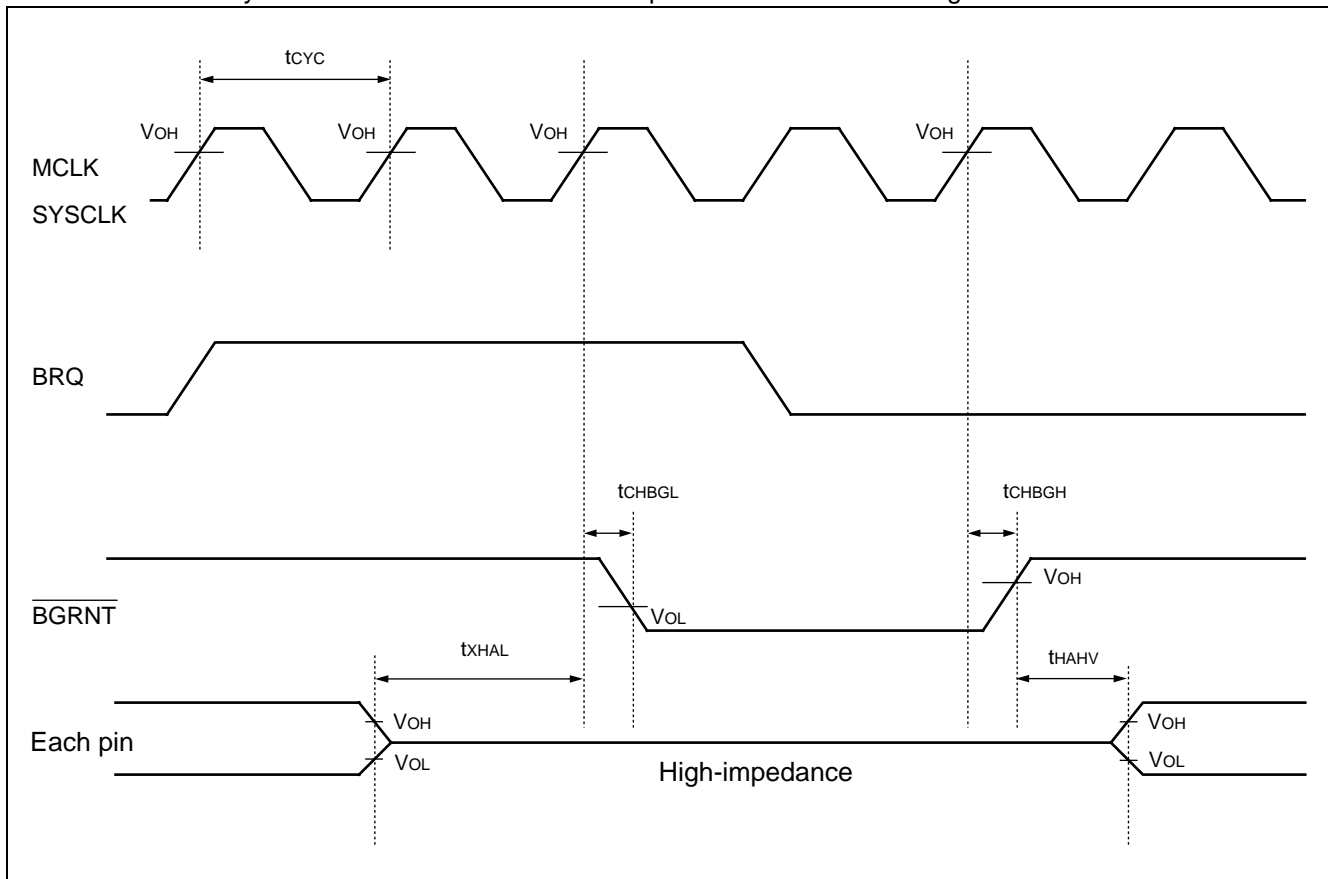


(6) Hold timing

($V_{DDI} = 1.8\text{ V} \pm 0.15\text{ V}$, $V_{DDE} = AV_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_{SS} = AV_{SS} = 0\text{ V}$, $T_a = -10\text{ }^\circ\text{C}$ to $+70\text{ }^\circ\text{C}$)

Parameter	Symbol	Pin	Condi-tions	Value		Unit	Remarks
				Min	Max		
$\overline{\text{BGRNT}}$ delay time	t_{CHBGL}	MCLK SYSCLK $\overline{\text{BGRNT}}$	—	$t_{\text{CYC}} / 2 - 6$	$t_{\text{CYC}} / 2 + 6$	ns	
$\overline{\text{BGRNT}}$ delay time	t_{CHBGH}			$t_{\text{CYC}} / 2 - 6$	$t_{\text{CYC}} / 2 + 6$	ns	
Pin floating → $\overline{\text{BGRNT}}$ ↓ time	t_{XHAL}	$\overline{\text{BGRNT}}$		$t_{\text{CYC}} - 10$	$t_{\text{CYC}} + 10$	ns	
$\overline{\text{BGRNT}}$ ↑ → Pin valid time	t_{HAHV}			$t_{\text{CYC}} - 10$	$t_{\text{CYC}} + 10$	ns	

Note : It takes one cycle or more from when BRQ is captured until $\overline{\text{BGRNT}}$ changes.



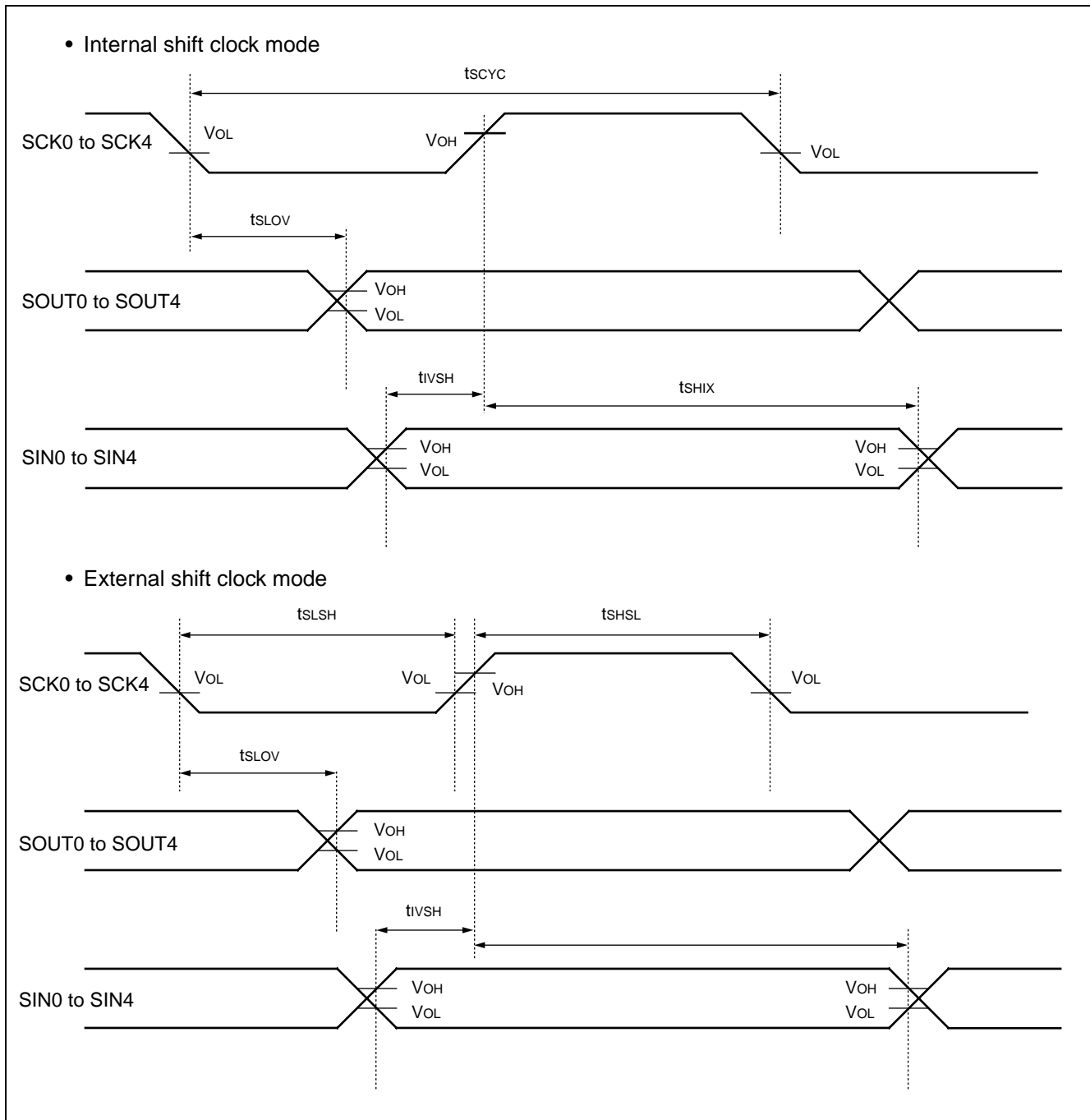
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(7) UART timing

($V_{DDI} = 1.8\text{ V} \pm 0.15\text{ V}$, $V_{DDE} = AV_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_{SS} = AV_{SS} = 0\text{ V}$, $T_a = -10\text{ }^{\circ}\text{C}$ to $+70\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0 to SCK4	Internal shift clock mode	$8 t_{CYCP}$	—	ns	
SCLK $\downarrow \rightarrow$ SOUT delay time	t_{SLOV}	SCK0 to SCK4 SOUT0 to SOUT4		-80	+80	ns	
Valid SIN \rightarrow SCLK \uparrow	t_{IVSH}	SCK0 to SCK4 SIN0 to SIN4		100	—	ns	
SCLK $\uparrow \rightarrow$ valid SIN hold time	t_{SHIX}	SCK0 to SCK4 SIN0 to SIN4		60	—	ns	
Serial clock "H" Pulse Width	t_{SHSL}	SCK0 to SCK4	External shift clock mode	$4 t_{CYCP}$	—	ns	
Serial clock "L" Pulse Width	t_{SLSH}	SCK0 to SCK4		$4 t_{CYCP}$	—	ns	
SCLK $\downarrow \rightarrow$ SOUT delay time	t_{SLOV}	SCK0 to SCK4 SOUT0 to SOUT4		—	150	ns	
Valid SIN \rightarrow SCLK \uparrow	t_{IVSH}	SCK0 to SCK4 SIN0 to SIN4		60	—	ns	
SCLK $\uparrow \rightarrow$ valid SIN hold time	t_{SHIX}	SCK0 to SCK4 SIN0 to SIN4		60	—	ns	

- Notes : • Above rating is for CLK synchronous mode.
• t_{CYCP} indicates the peripheral clock cycle time.



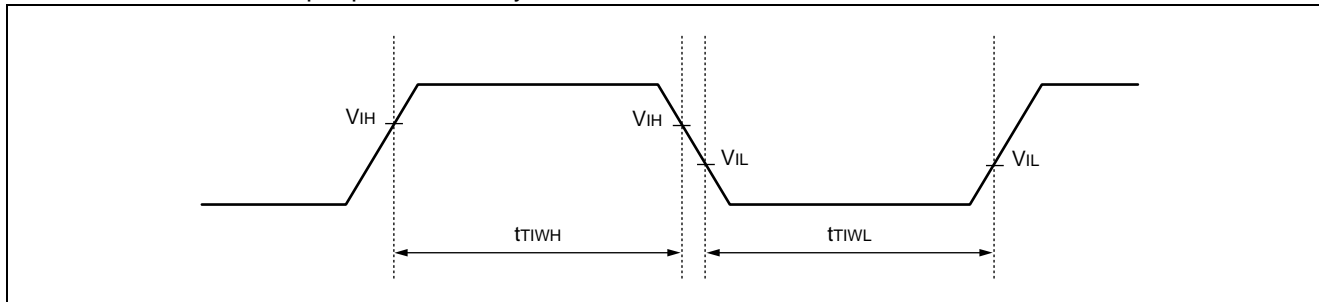
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(8) Timer clock Input Timing

($V_{DDI} = 1.8\text{ V} \pm 0.15\text{ V}$, $V_{DDE} = AV_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_{SS} = AV_{SS} = 0\text{ V}$, $T_a = -10\text{ }^{\circ}\text{C}$ to $+70\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH} t_{TIWL}	TIN0 to TIN2	—	$2 t_{CYCP}$	—	ns	

Note : t_{CYCP} indicates the peripheral clock cycle time.

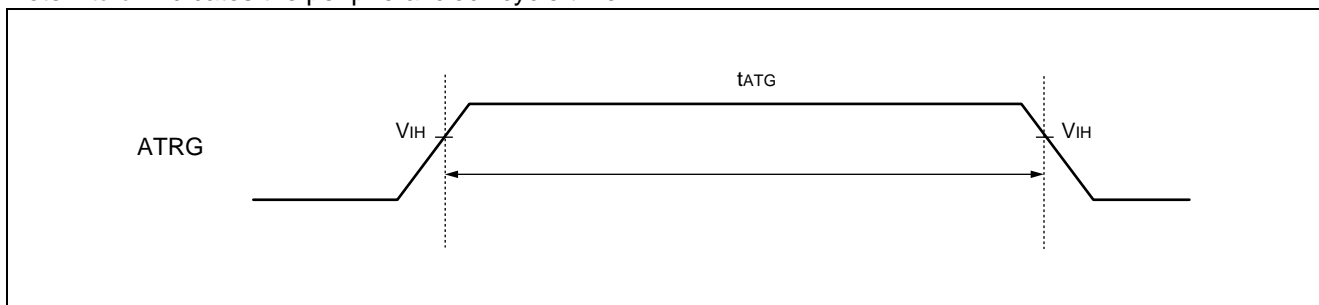


(9) Trigger Input Timing

($V_{DDI} = 1.8\text{ V} \pm 0.15\text{ V}$, $V_{DDE} = AV_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_{SS} = AV_{SS} = 0\text{ V}$, $T_a = -10\text{ }^{\circ}\text{C}$ to $+70\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
A/D activation trigger input time	t_{ATG}	ATRG	—	$5 t_{CYCP}$	—	ns	

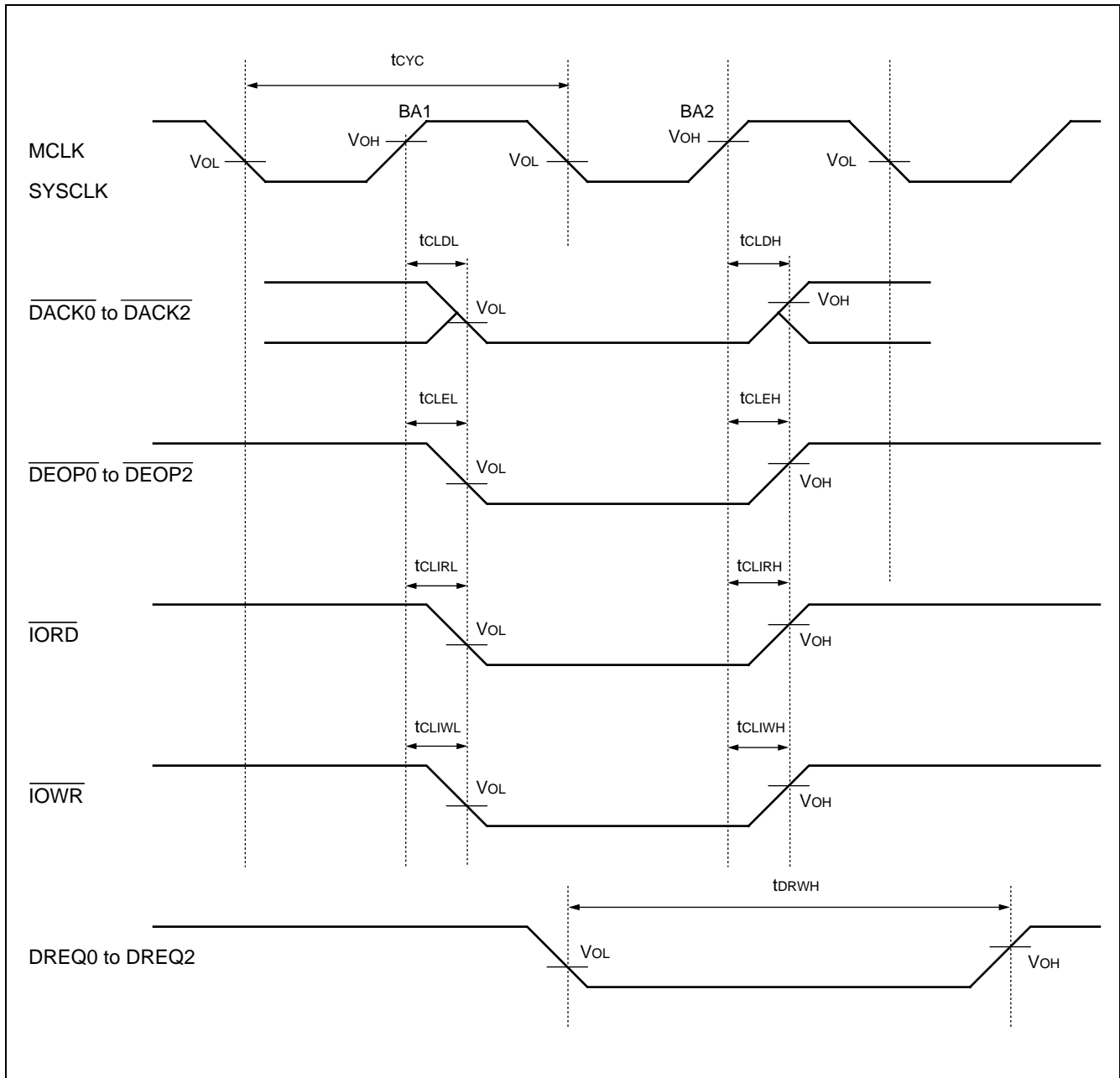
Note : t_{CYCP} indicates the peripheral clock cycle time.



(10) DMA controller timing(V_{DDI} = 1.8 V ± 0.15 V, V_{DDE} = AV_{CC} = 3.3 V ± 0.3 V, V_{SS} = AV_{SS} = 0 V, Ta = -10 °C to +70 °C)

Parameter	Symbol	Pin	Condi- tions	Value		Unit	Remarks
				Min	Max		
DREQ Input pulse width	t _{DRWH}	DREQ0 to DREQ2	—	5 t _{cyc}	—	ns	
$\overline{\text{DACK}}$ delay time	t _{CLDL}	MCLK/SYSCLK		—	6	ns	
	t _{CLDH}	$\overline{\text{DACK0}}$ to $\overline{\text{DACK2}}$		—	6		
$\overline{\text{DEOP}}$ delay time	t _{CLEL}	MCLK/SYSCLK		—	6	ns	
	t _{CLEH}	$\overline{\text{DEOP0}}$ to $\overline{\text{DEOP2}}$		—	6		
$\overline{\text{IORD}}$ delay time	t _{CLIRL}	MCLK/SYSCLK		—	6	ns	
	t _{CLIRH}			—	6		
$\overline{\text{IOWR}}$ delay time	t _{CLIWL}	MCLK/SYSCLK		—	6	ns	
	t _{CLIWH}			—	6		

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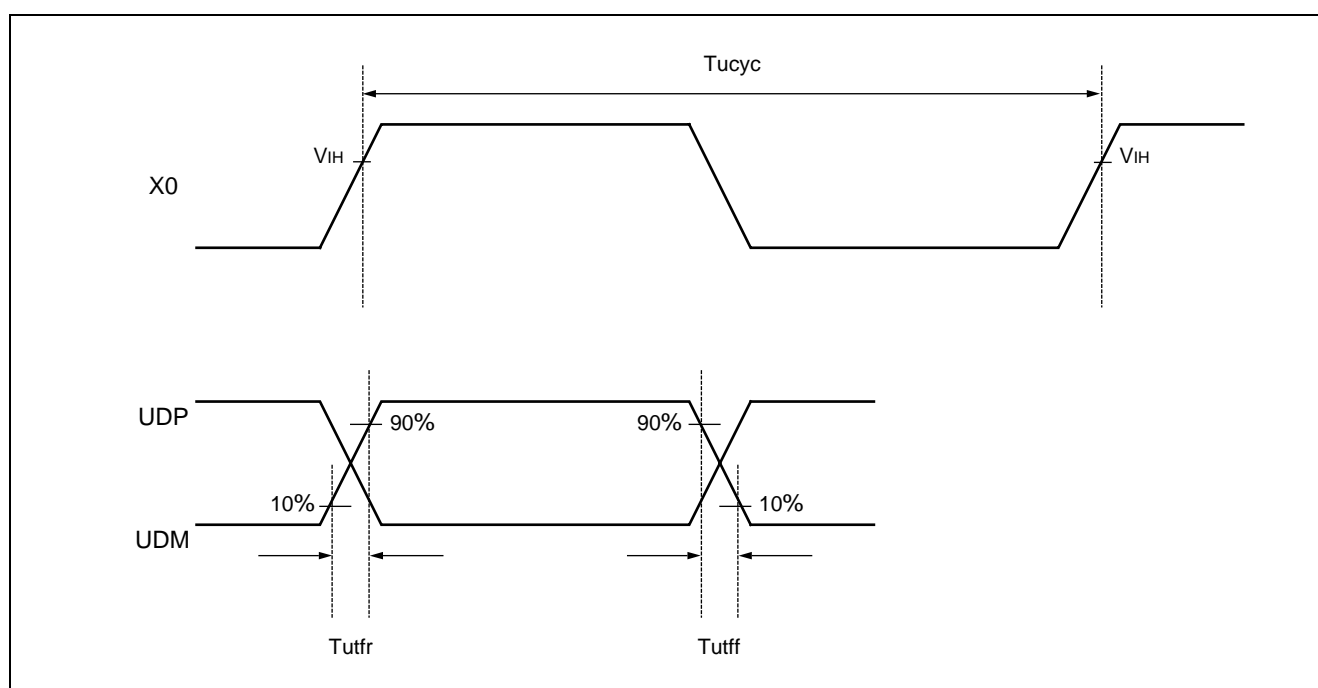
Note : The waveform of \overline{DACKx} and \overline{DEOPx} is the waveforms when the PFR register is set to FR30 compatible timing.

When the setting is chip selection timing, The delay starts from the falling edge of MCLK/SYSCLK.

(11) USB interface

($V_{DDI} = 1.8\text{ V} \pm 0.15\text{ V}$, $V_{DDE} = AV_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_{SS} = AV_{SS} = 0\text{ V}$, $T_a = -10\text{ }^\circ\text{C}$ to $+70\text{ }^\circ\text{C}$)

Parameter	Symbol	Pin	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input clock	Tucyc	X0 X1	—	—	48*1	—	MHz	Self oscillation 2500 ppm accuracy*1
		X0	—					External input 2500 ppm accuracy*1
Rise Time	Tutfr	UDP/ UDM	Full Speed	4	—	20	ns	*2
Fall Time	Tutff	UDP/ UDM	Full Speed	4	—	20	ns	*2
Differential Rise and Fall Timing Matching	Tutfrfm	UDP/ UDM	Full Speed	90	—	111.11	%	*2
Driver Output Resistance	Tuzdrv	UDP UDM	—	28	—	44	Ω	*3



*1 : AC characteristics for USB interface conform to USB Specification Revision 1.1.

*2 : < Driver Characteristics T_{utfr} , T_{utff} and T_{utfrfm} >

These are regulations of the rising / falling time of the differential data signal.

This time is defined at the time between 10% to 90% of the output signal voltage.

For full-speed buffer, T_{utfr}/T_{utff} is specified such that the T_{utfr}/T_{utff} ratio falls within $\pm 10\%$ to minimize RFI radiation.

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*3 : < Driver Characteristics ZDRV >

The USB Full-speed connection is done by $90 \Omega \pm 15\%$ of characteristic impedance (Z_0).

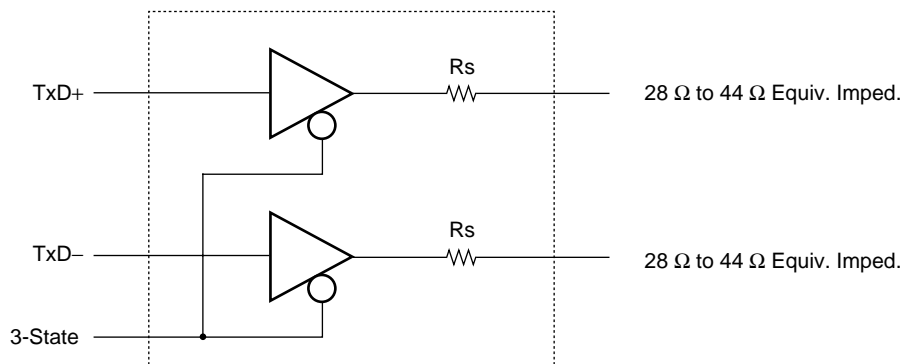
It is connected through the shielded twist 2-pair cable.

In this USB standard, both following conditions must be satisfied.

- The output impedance of USB Driver is from 28Ω to 44Ω .
- To balance, discrete series resistor (R_s) is added.

The output impedance of USB I/O Buffer of this LSI is about 3Ω to 19Ω .

Therefore, it is necessary to add the series resistance R_s of 25Ω to 30Ω (recommended value 27Ω).



Driver output impedance 3Ω to 19Ω

R_s series resistance 25Ω to 30Ω

Resistance R_s of recommended value 27Ω should be added.

(12) I²C Timing

In the master mode operation

($V_{DDI} = 1.8\text{ V} \pm 0.15\text{ V}$, $V_{DDE} = AV_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_{SS} = AV_{SS} = 0\text{ V}$, $T_a = -10\text{ }^{\circ}\text{C to } +70\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Condition	Standard-mode		Fast-mode* ³		Unit	Remarks
			Min	Max	Min	Max		
SCL clock frequency	f _{SCL}	R = 1 kΩ, C = 50 pF* ⁴	0	100	0	400	kHz	
"L" width of the SCL clock	t _{LOW}		4.7	—	1.3	—	μs	
"H" width of the SCL clock	t _{HIGH}		4.0	—	0.6	—	μs	
Bus free time between a STOP and START condition	t _{BUS}		4.7	—	1.3	—	μs	
SCL ↓ → SDA output delay time	t _{DLDAT}		—	5 × M* ¹	—	5 × M* ¹	ns	
Set-up time for a repeated START condition SCL ↑ → SDA ↓	t _{SUSTA}		4.7	—	0.6	—	μs	
Hold time (repeated) START condition SDA ↓ → SCL ↓	t _{HDSTA}		4.0	—	0.6	—	μs	The first clock pulse is generated afterword.
Set-up time for STOP condition SCL ↑ → SDA ↑	t _{SUSTO}		4.0	—	0.6	—	μs	
Data input hold time (vs.SCL ↓)	t _{HDDAT}		2 × M* ¹	—	2 × M* ¹	—	μs	
Data input set-up time (vs.SCL ↑)	t _{SUDAT}		250	—	100* ²	—	ns	

*1 : M = Resource clock cycle (ns)

*2 : To use high-speed mode I²C bus device for standard mode I²C bus system, it must satisfy the request condition (t_{SUDAT} = 250 ns). If a device does not extend "L" period of the SCL signal, the following data must be output to the SDA line before 1250 ns (SCL line is opened, equal to SDA, SCL rise Max time + t_{SUDATA}).

*3 : To use it exceeding 100kHz, the resource clock is set to 6MHz or more.

*4 : R and C is the pull-up resistor and the load capacity for SCL and SDA output lines respectively.

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In the slave mode operation

($V_{DDI} = 1.8\text{ V} \pm 0.15\text{ V}$, $V_{DDE} = AV_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_{SS} = AV_{SS} = 0\text{ V}$, $T_a = -10\text{ }^\circ\text{C}$ to $+70\text{ }^\circ\text{C}$)

Parameter	Symbol	Condition	Standard-mode		Fast-mode*3		Unit	Remarks
			Min	Max	Min	Max		
SCL clock frequency	f _{SCL}	R = 1 kΩ, C = 50 pF*4	0	100	0	400	kHz	
"L" width of the SCL clock	t _{LOW}		4.7	—	1.3	—	μs	
"H" width of the SCL clock	t _{HIGH}		4.0	—	0.6	—	μs	
SCL ↓ → SDA output delay time	t _{DLDAT}		—	5 × M*1	—	5 × M*1	ns	
Bus free time between a STOP and START condition	t _{BUS}		4.7	—	1.3	—	μs	
Data input hold time (vs.SCL↓)	t _{HDDAT}		2 × M*1	—	2 × M*1	—	μs	
Data input set-up time (vs.SCL↑)	t _{SUDAT}		250	—	100*2	—	ns	
Set-up time for a repeated START condition SCL↑ → SDA↓	t _{SUSTA}		4.7	—	0.6	—	μs	
Hold time for a repeated START condition SDA↓ → SCL↓	t _{HDSTA}		4.0	—	0.6	—	μs	The first clock pulse is generated afterword.
Set-up time for STOP condition SCL↑ → SDA↑	t _{SUSTO}		4.0	—	0.6	—	μs	

*1 : M = Resource clock cycle (ns)

*2 : To use high-speed mode I²C bus device for standard mode I²C bus system, it must satisfy the request condition (t_{SUDAT} = 250 ns). If a device does not extend "L" period of the SCL signal, the following data must be output to the SDA line before 1250 ns (SCL line is opened, equal to SDA, SCL rise Max time + t_{SUDATA}).

*3 : To use it exceeding 100kHz, the resource clock is set to 6MHz or more.

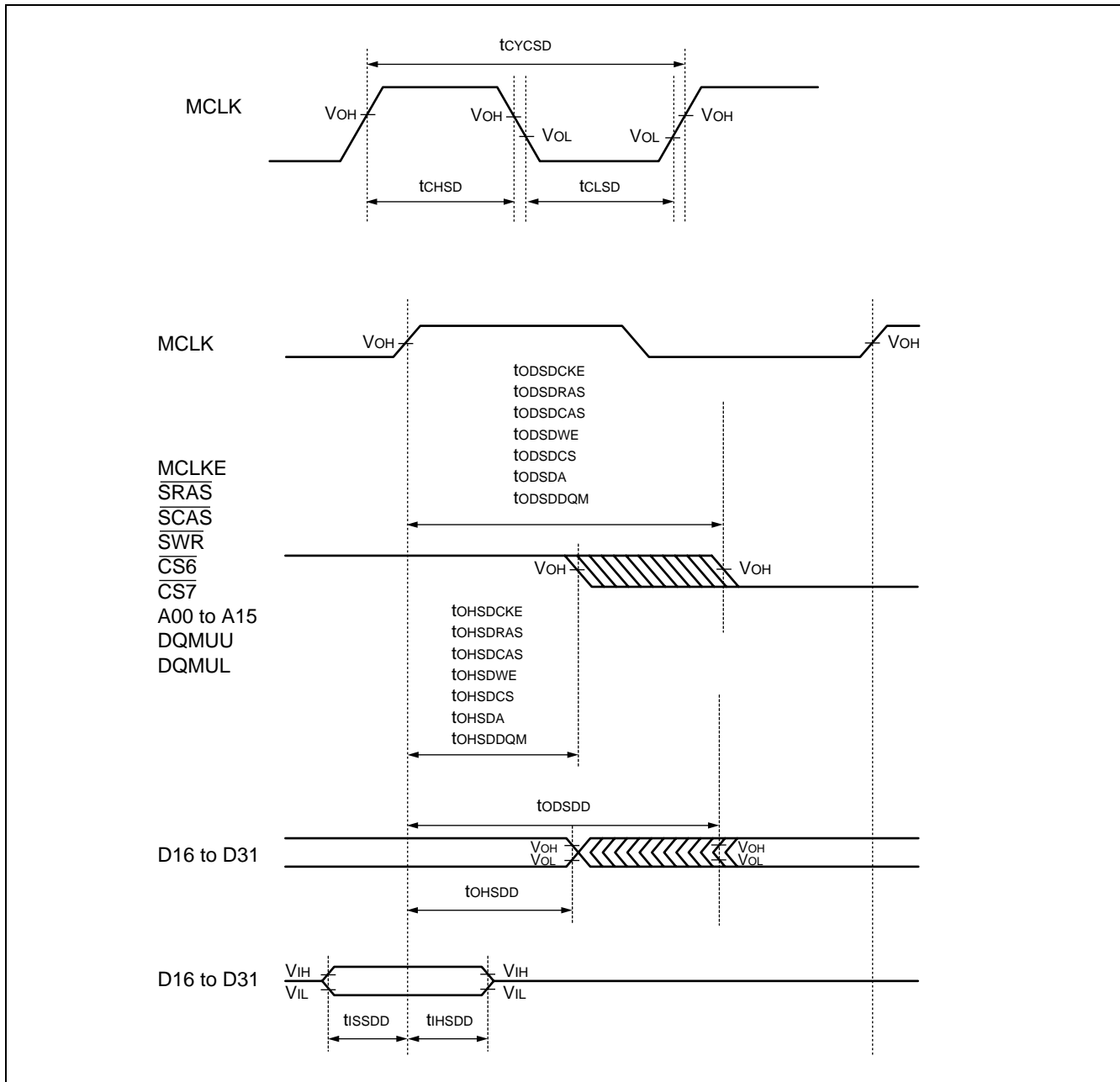
*4 : R and C is the pull-up resistor and the load capacity for SCL and SDA output lines respectively.

(13) SDRAM Timing

(V_{DDI} = 1.8 V ± 0.15 V, V_{DDE} = AV_{CC} = 3.3 V ± 0.3 V, V_{SS} = AV_{SS} = 0 V, Ta = -10 °C to +70 °C)

Parameter	Symbol	Pin	Condi- tions	Value		Unit	Remarks
				Min	Max		
Output clock cycle time	t _{CYCSD}	MCLK	—	—	32	MHz	
“H” level clock pulse width	t _{CHSD}			12	—	ns	
“L” level clock pulse width	t _{CLSD}			12	—	ns	
MCLK ↑ → output delay time	t _{ODSDCKE}	MCLKE	—	—	15	ns	
Output hold time	t _{OHSDCKE}			2	—	ns	
MCLK ↑ → output delay time	t _{ODSDRAS}	$\overline{\text{SRAS}}$	—	—	15	ns	
Output hold time	t _{OHSDRAS}			2	—	ns	
MCLK ↑ → output delay time	t _{ODSDCAS}	$\overline{\text{SCAS}}$	—	—	15	ns	
Output hold time	t _{OHSDCAS}			2	—	ns	
MCLK ↑ → output delay time	t _{ODSDWE}	$\overline{\text{SWR}}$	—	—	15	ns	
Output hold time	t _{OHSDWE}			2	—	ns	
MCLK ↑ → output delay time	t _{ODSDCS}	$\overline{\text{CS6}}$ $\overline{\text{CS7}}$	—	—	15	ns	
Output hold time	t _{OHSDCS}			2	—	ns	
MCLK ↑ → output delay time	t _{ODSDA}	A00 to A15	—	—	15	ns	
Output hold time	t _{OHSDA}			2	—	ns	
MCLK ↑ → output delay time	t _{ODSDDQM}	DQMUU DQMUL	—	—	15	ns	
Output hold time	t _{OHSDDQM}			2	—	ns	
MCLK ↑ → output delay time	t _{ODSDD}	D16 to D31	—	—	15	ns	
Output hold time	t _{OHSDD}			2	—	ns	
Data input setup time	t _{ISSDD}	D16 to D31	—	15	—	ns	
Data input hold time	t _{IHSDD}			2	—	ns	

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5. Electrical Characteristics for the A/D Converter

($V_{DDI} = 1.8 \text{ V} \pm 0.15 \text{ V}$, $V_{DDE} = AV_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$, $V_{SS} = AV_{SS} = 0 \text{ V}$, $T_a = -10 \text{ }^\circ\text{C}$ to $+70 \text{ }^\circ\text{C}$)

Parameter	Symbol	Pin	Value			Unit
			Min	Typ	Max	
Resolution	—	—	—	—	10	BIT
Total error	—	—	—	—	± 5.5	LSB
Nonlinear error	—	—	—	—	± 3.5	LSB
Differential linear error	—	—	—	—	± 2.0	LSB
Zero transition voltage	V_{OT}	AN0 to AN9	-4.0	—	+6.0	LSB
Full-transition voltage	V_{FST}	AN0 to AN9	$AVRH - 5.5$	—	$AVRH + 3.0$	LSB
Conversion time	—	—	8.18*1	—	—	μs
Analog port input current	I_{AIN}	AN0 to AN9	—	0.1	10	μA
Analog input voltage	V_{AIN}	AN0 to AN9	$AVSS$	—	$AVRH$	V
Reference voltage	—	$AVRH$	$AVSS$	—	$AVCC$	V
Power supply current	I_A	$AVCC$	—	3.6	—	mA
	I_{AH}		—	—	10^{*2}	μA
Reference voltage supply current	I_R	$AVRH$	—	600	—	μA
	I_{RH}		—	—	10^{*2}	μA
Variation between channels	—	AN0 to AN9	—	—	5	LSB

*1 : For $V_{DDI} = 1.8 \text{ V} \pm 0.15 \text{ V}$, $V_{DDE} = AV_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$, machine clock = 32 MHz

*2 : Current when A/D converter not operating ($V_{DDE} = AV_{CC} = AVRH = 3.6 \text{ V}$, $V_{DDI} = 1.95 \text{ V}$)

- Notes :
- The relative error increases as $AVRH$ becomes smaller.
 - If the output impedance of the external circuit is too high, the analog voltage sampling time may be too short.

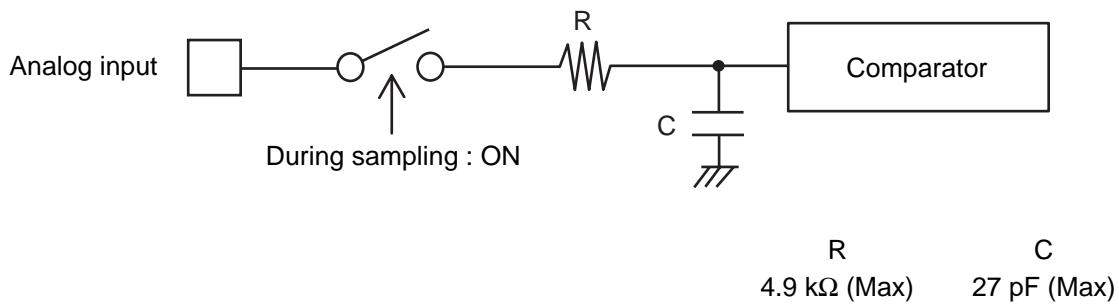
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- **About the external impedance of the analog input and its sampling time**

- A/D converter with sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting A/D conversion precision. Therefore, to satisfy the A/D conversion precision standard, consider the relationship between the external impedance and minimum sampling time and either adjust the operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value.

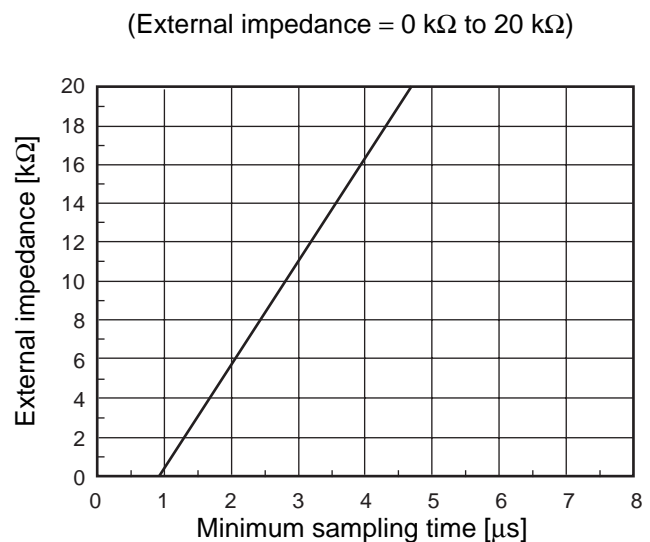
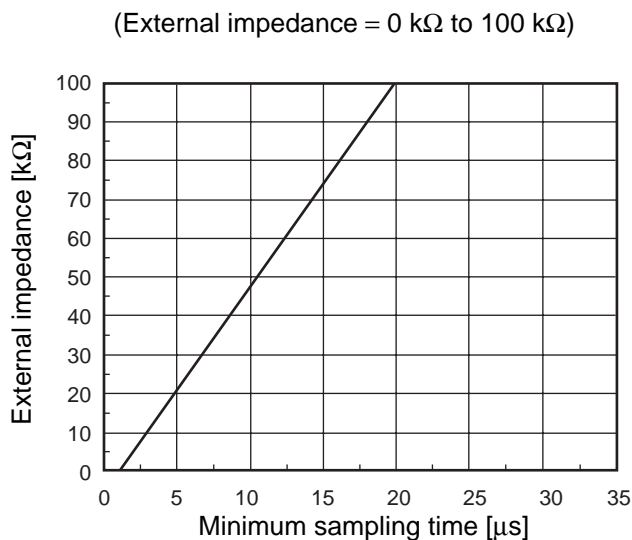
And if the sampling time cannot be sufficient, connect a capacitor of about 0.1 μF to the analog input pin.

- Analog input circuit model



Note : The values are reference values.

- The relationship between the external impedance and minimum sampling time



- About the error

The accuracy gets worse as $|AVRH - AV_{SS}|$ becomes smaller.

• Definition of A/D Converter Terms

- Resolution

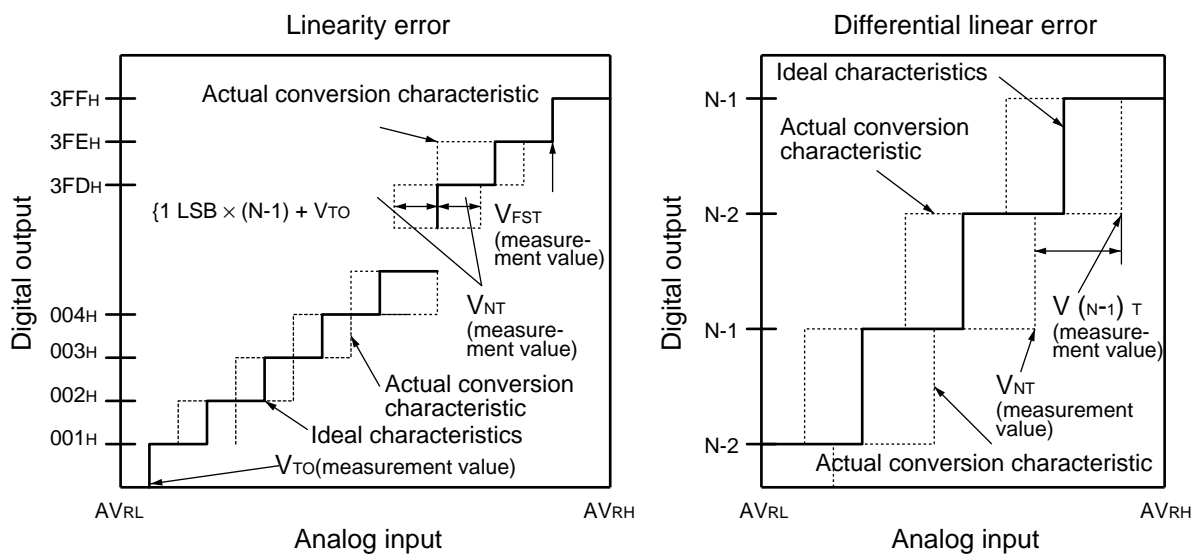
Analog variation that is recognized by an A/D converter.

- Linearity error

The deviation between the actual conversion characteristics and a straight line connecting the device's zero transition point ("000000000" ←→ "000000001") and full scale transition point ("111111110" ←→ "111111111").

- Differential linear error

Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value.



$$\text{Linear error in digital output } N = \frac{V_{NT} - \{1\text{LSB} \times (N - 1) + V_{OT}\}}{1\text{LSB}} \quad [\text{LSB}]$$

$$\text{Differential linear error in digital output } N = \frac{V_{(N+1)T} - V_{NT}}{1\text{LSB}} \quad [\text{LSB}]$$

$$1\text{LSB} = \frac{V_{FST} - V_{OT}}{1022} \quad [\text{V}]$$

$$1\text{LSB}' = \frac{AV_{RH} - AV_{RL}}{1024} \quad [\text{V}] \quad (\text{Ideal value})$$

N : A/D converter digital output value

V_{OT} : A voltage at which digital output transitions from (000)_H to (001)_H.

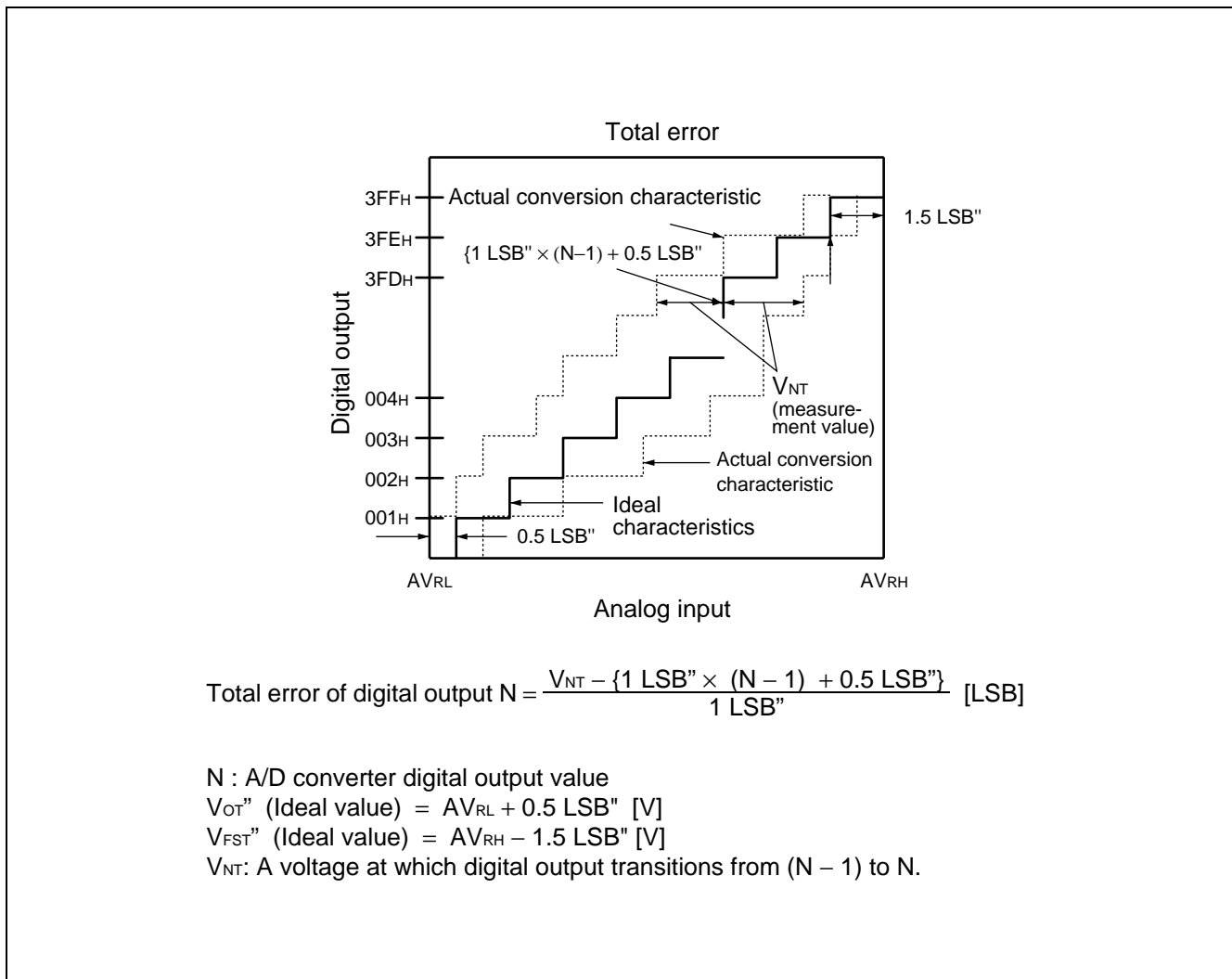
V_{FST} : A voltage at which digital output transitions from (3FE)_H to (3FF)_H.

V_{NT} : A voltage at which digital output transitions from (N - 1) to N.

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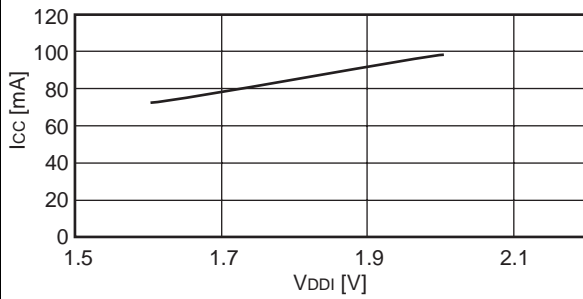
- Total error

This error indicates the difference between actual and ideal values, including the zero transition error/full-scale transition error/linearity error.

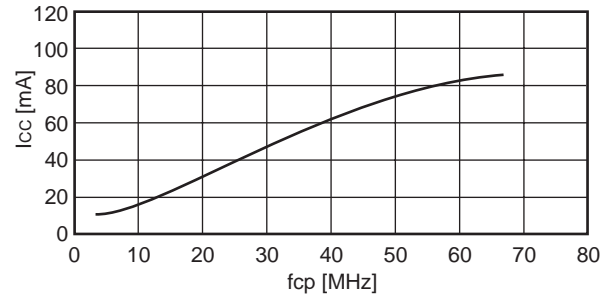


EXAMPLE CHARACTERISTICS

I_{CC} - V_{DDI} example characteristics
 $T_a = +25\text{ }^\circ\text{C}$, $f_{cp} = 68\text{ MHz}$
 $f_{cpp} = 34\text{ MHz}$, $f_{cpt} = 34\text{ MHz}$

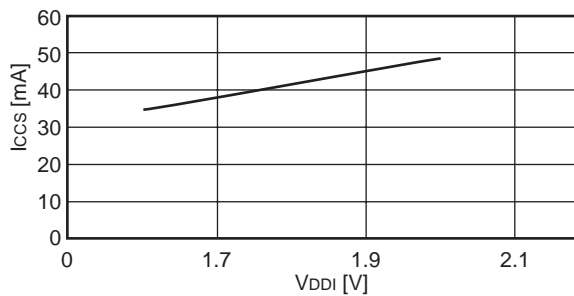


I_{CC} - f_{CP} example characteristics
 $T_a = +25\text{ }^\circ\text{C}$, $V_{DDE} = 3.3\text{ V}$
 $V_{DDI} = 1.8\text{ V}$

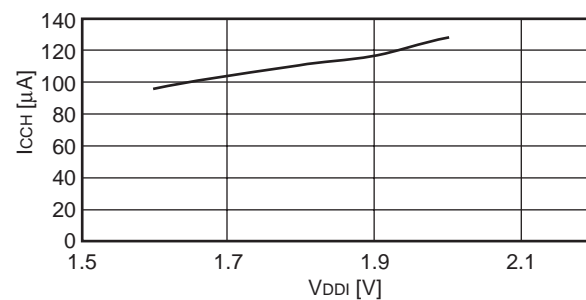


($f_{cp} : f_{cpp} : f_{cpt} = 2 : 1 : 1$, PLL 4 multiplication)

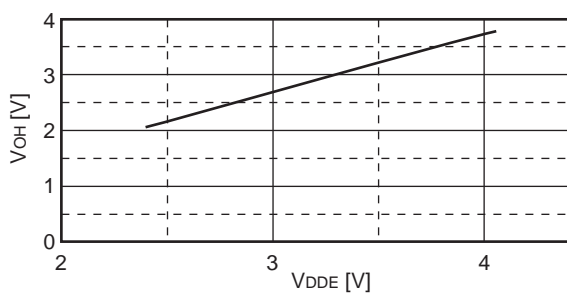
I_{CCS} - V_{DDI} example characteristics
 $T_a = +25\text{ }^\circ\text{C}$



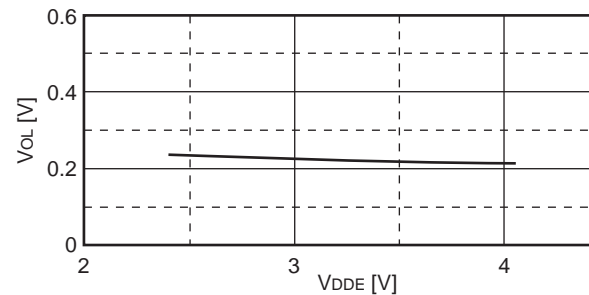
I_{CCH} - V_{DDI} example characteristics
 $T_a = +25\text{ }^\circ\text{C}$



V_{OH} - V_{DDE} example characteristics
 $T_a = +25\text{ }^\circ\text{C}$



V_{OL} - V_{DDE} example characteristics
 $T_a = +25\text{ }^\circ\text{C}$

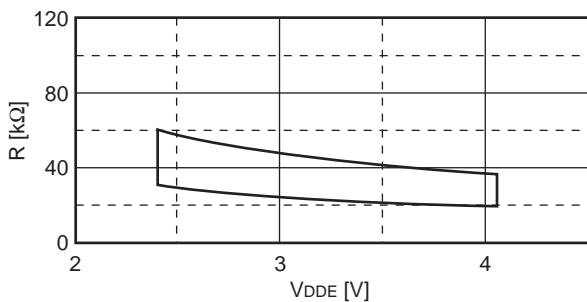


Note : Not including USB I/O

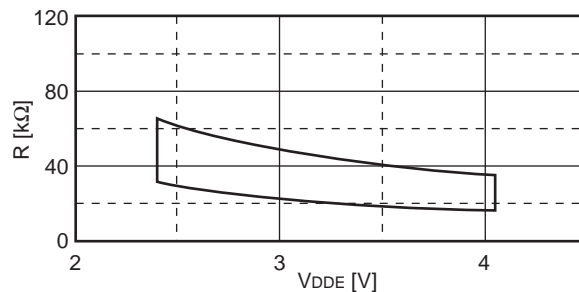
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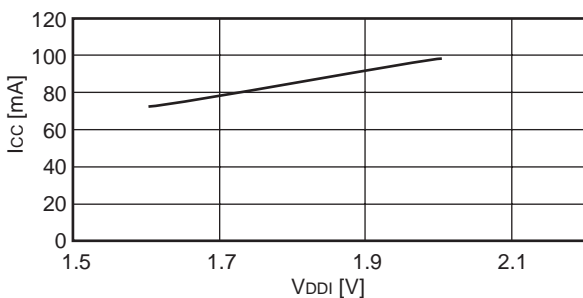
Pull-up resistor example characteristics
Ta = + 25 °C



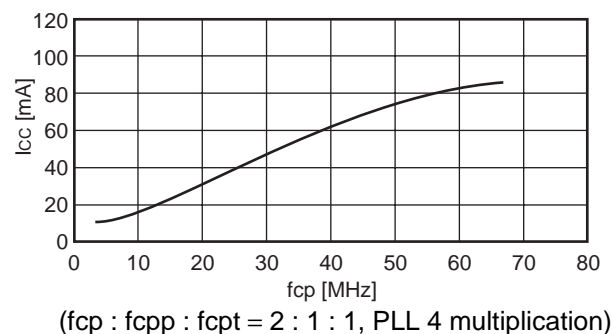
Pull-down resistor example characteristics
Ta = + 25 °C



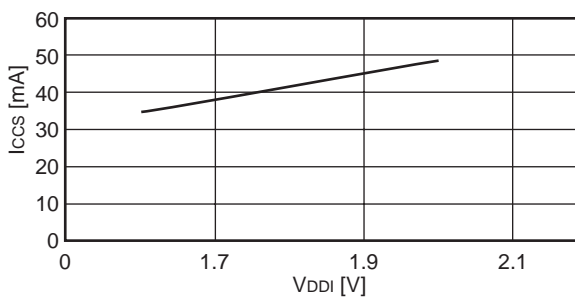
I_{CC}-V_{DDI} example characteristics
Ta = + 25 °C, f_{CP} = 68 MHz
f_{CPp} = 34 MHz, f_{CPt} = 34 MHz



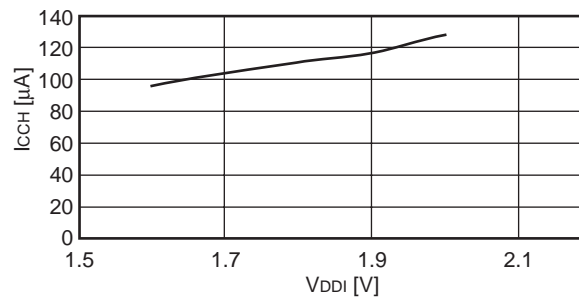
I_{CC}-f_{CP} example characteristics
Ta = + 25 °C, V_{DD E} = 3.3 V
V_{DDI} = 1.8 V



I_{CCS}-V_{DDI} example characteristics
Ta = + 25 °C



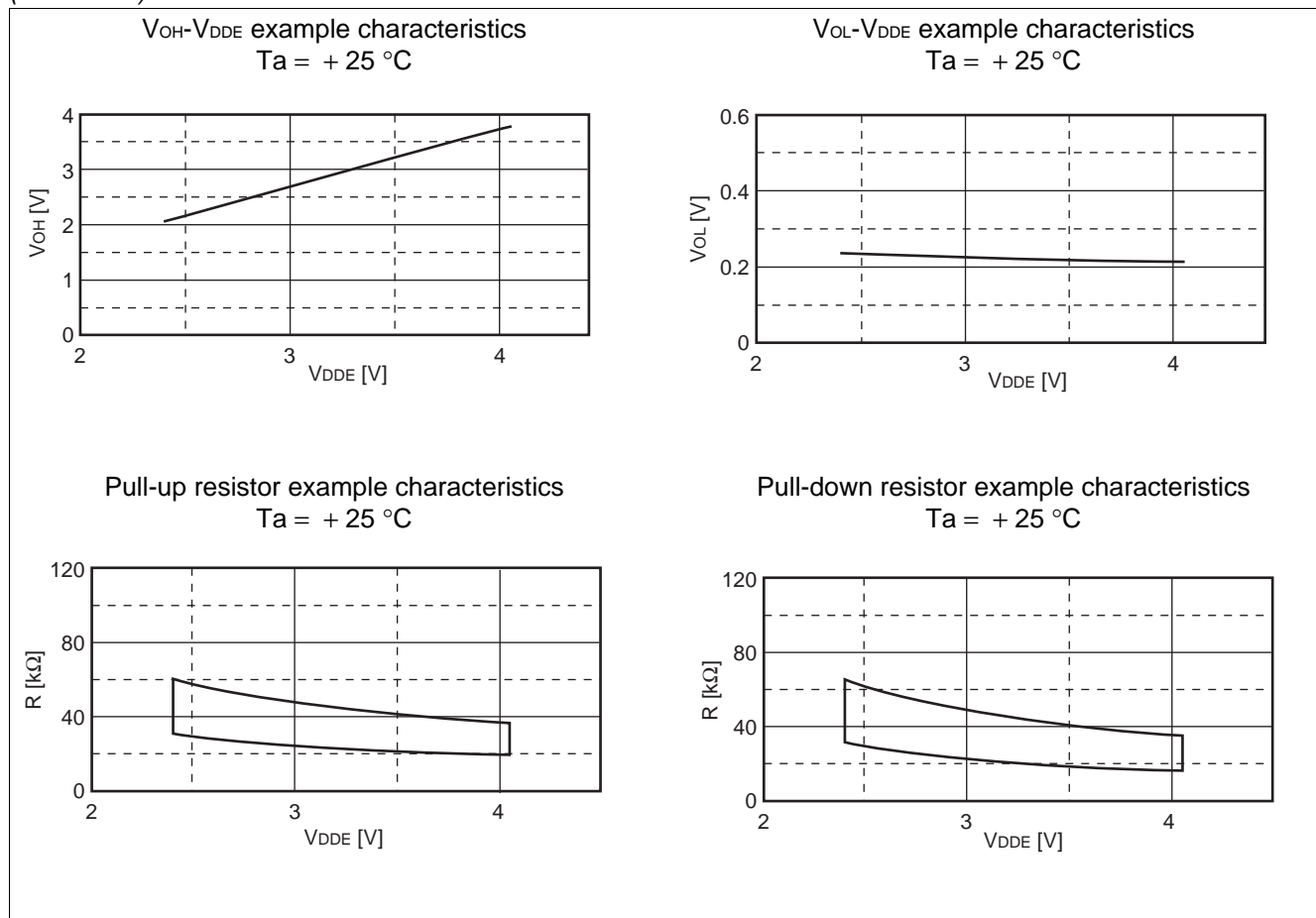
I_{CC H}-V_{DDI} example characteristics
Ta = + 25 °C



Note : Not including USB I/O

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Note : Not including USB I/O

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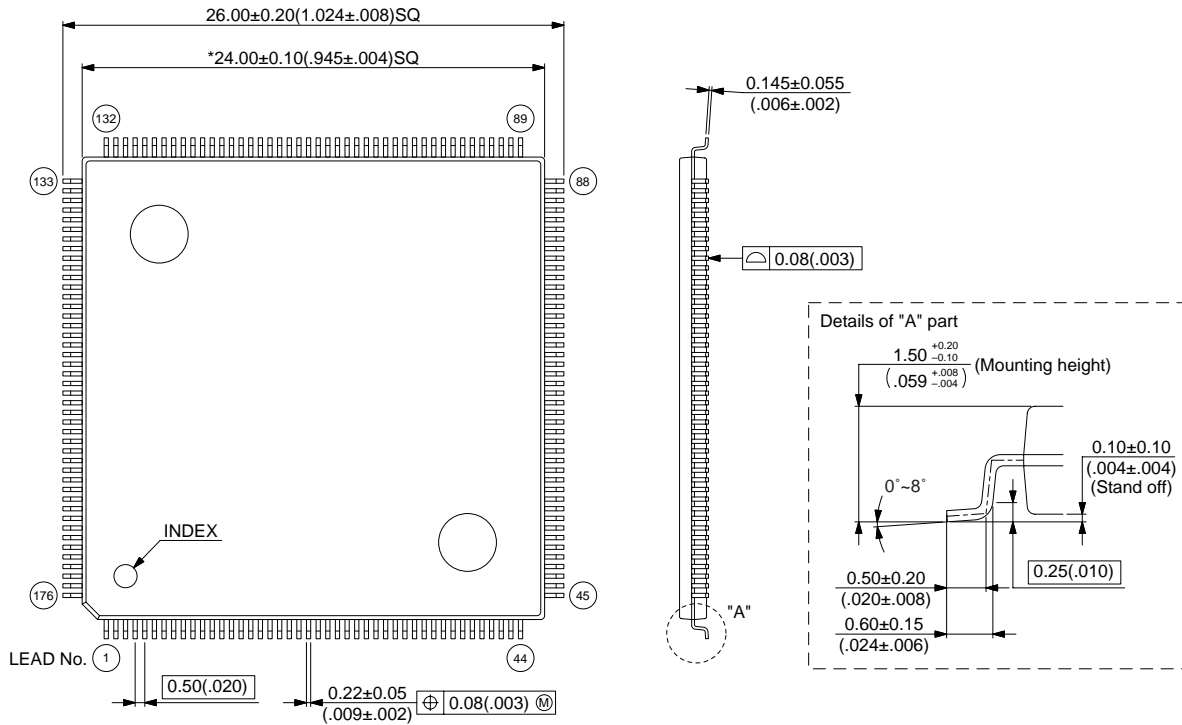
■ ORDERING INFORMATION

Part number	Package	Remarks
MB91305PMC	176-pin plastic LQFP (FPT-176P-M07)	

■ PACKAGE DIMENSION

176-pin plastic LQFP
(FPT-176P-M07)

- Note 1) * : Values do not include resin protrusion.
Resin protrusion is +0.25 (.010) Max (each side) .
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



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Dimensions in mm (inches).
Note: The values in parentheses are reference values.

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The information for microcontroller supports is shown in the following homepage.

<http://www.fujitsu.com/global/services/microelectronics/product/micom/support/index.html>

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