FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-16401-2E

32-bit RISC Microcontroller

CMOS

FR50 Family MB91360G Series

MB91FV360GA/F361GA/F362GA

■ DESCRIPTION

The Fujitsu MB91360G series is a standard microcontroller containing a wide range of I/O peripherals and bus control functions. The MB91360G series features a 32-bit RISC CPU (FR50 series) core and is suitable for embedded control applications requiring high-performance and high-speed CPU processing. The MB91360G series also contains up to 4 Kbyte instruction cache memory and other internal memories to improve the execution speed of the CPU.

■ FEATURES

- **Execution time : down to 15.6 ns (64 MHz)**
- **FR50 series CPU : RISC architecture**
  The CPU has a general-purpose register architecture with improved numeric implementation whereby a wide range of delayed branch instructions reduces losses in execution time due to pipeline breaks.
  Bit manipulation instructions and memory access instructions have been enhanced resulting in improved code efficiency and execution speed for control implementation.
  - A five-stage pipeline structure provides high-speed processing (one instruction per cycle)
  - 32-bit linear address space : 4 Gbytes
  - Fixed 16-bit instruction size (basic instructions)
  - High-speed multiplication/step division
  - High-speed interrupt processing (6 cycles)
  - General-purpose registers : 16 × 32 bits

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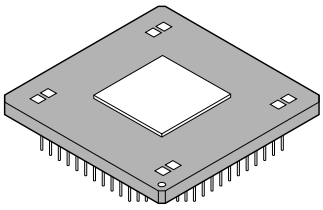
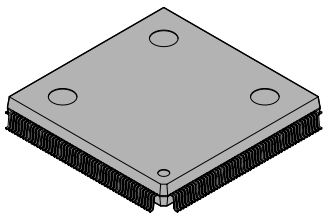
■ PACKAGE

401-pin Ceramics PGA



(PGA-401C-A02)

208-pin plastic QFP



(FPT-208P-M04)

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- **External bus interface unit with a wide range of functions**
  Divides the external memory space into a maximum of eight areas. Chip select signal setting, data bus width selection (8, 16, 32-bit) , and area size can be specified for each area.
  - Address bus up to 32 bit wide
  - Programmable auto-wait function
- **Internal instruction cache**
  The MB91360G series contains up to 4-Kbyte instruction cache to improve the execution speed of external programs.
  - Two-way set associative caching
- **DMAC**
  Direct memory access (DMA) can be used to perform various types of data transfer without going via the CPU. This improves system performance.
  - Eight channels (including up to 3 external channels)
  - Three transfer modes supported : single/block, burst, continuous transfer
- **Power consumption control mechanisms**
  The MB91360G series contains a number of functions for controlling the operating clock to reduce power consumption.
  - Software control : Sleep and stop/real time clock functions
  - Hardware control : Hardware standby function
  - Gear (divider) function : The CPU and peripheral clock frequencies can be set independently.
- **Contains a range of peripheral functions**
  - UART, U-timer
  - Real Time Clock (with optional subclock operation and subclock calibration module)
  - Stepper Motor Control
  - Sound Generator
  - Serial IO (SIO) , SIO-Prescaler
  - Power Down Reset
  - Alarm Comparator
  - IO-Timer
  - I^2C Interface
  - 10 Bit D/A Converter
  - CAN Interface
  - 10-bit A/D converter
  - 16-bit reload timer
  - 16-bit PWM timer
  - Watchdog timer
  - Bit search module
  - Interrupt controller
  - External interrupt inputs
  - I/O port function
- **Interrupt levels**
  “16 maskable interrupt levels”
- **Other**
  - Power supply voltage
  - 5 V power supply used, the internal regulator creates internal supply of 3.3 V
  - Package : MB91FV360GA uses a PGA401 package, MB91F361GA and MB91F362GA are delivered in a QFP208 package.

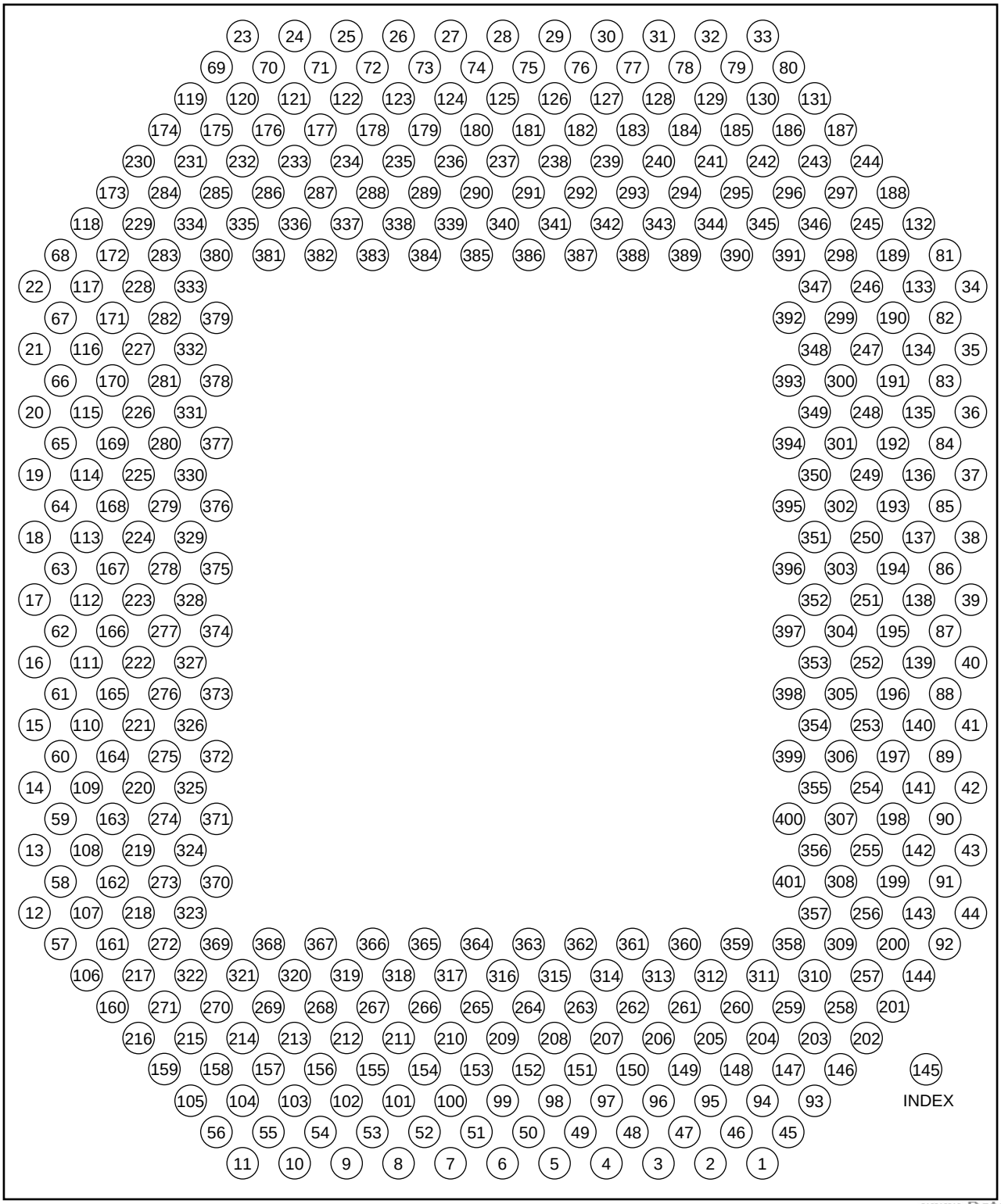
■ PRODUCT LINEUP

Resource Channels Memory Size	MB91FV360GA	MB91F361GA	MB91F362GA
Cache/Instruction RAM	4 KB / 4 KB	1 KB / 1 KB	- / 4 KB
D-bus RAM	16 KB	12 KB	12 KB
F-bus RAM	16 KB	4 KB	4 KB
Flash/ROM	512 KB on F-bus	512 KB on ext. bus	512 KB on F-bus
Boot ROM	2 KB	2 KB	2 KB
CAN	4 ch	3 ch	3 ch
Stepper Motor Control	4 ch	4 ch	4 ch
Sound Generator	1 ch	1 ch	1 ch
PPG	8 ch	8 ch	8 ch
Input Capture	4 ch	4 ch	4 ch
Output Compare	4 ch	4 ch	4 ch
Free Running Timer	2 ch	2 ch	2 ch
D/A Converter	2 ch	2 ch	2 ch
A/D Converter	16 ch	16 ch	16 ch
I^2C 100 kHz I^2C 400 kHz	1 ch	1 ch	1 ch
Alarm Comparator	1 ch	1 ch	1 ch
SIO/SIO prescaler	2 ch	2 ch	2 ch
UART/U-Timer	3 ch	3 ch	3 ch
16-bit Reload Timer	6 ch	6 ch	6 ch
Ext. Interrupt	8 ch	8 ch	8 ch
Non maskable Interrupt	1	—	—
Real Time Clock	1	1	1
32 kHz subclock option for RTC	yes	no	no
subclock calibration	yes	no	no
LED port	8 bit	8 bit	8 bit
Power down Reset	1	1	1
Bit search Module	1	1	1
Watchdog timer	1	1	1
Ext. Address Bus	32 bit	21 bit	21 bit
Ext. Data Bus	32 bit	32 bit	32 bit
Ext. DMA	3 ch	1 ch	1 ch
Max. operating frequency	64 MHz	64 MHz	64 MHz

■ PIN ASSIGNMENTS

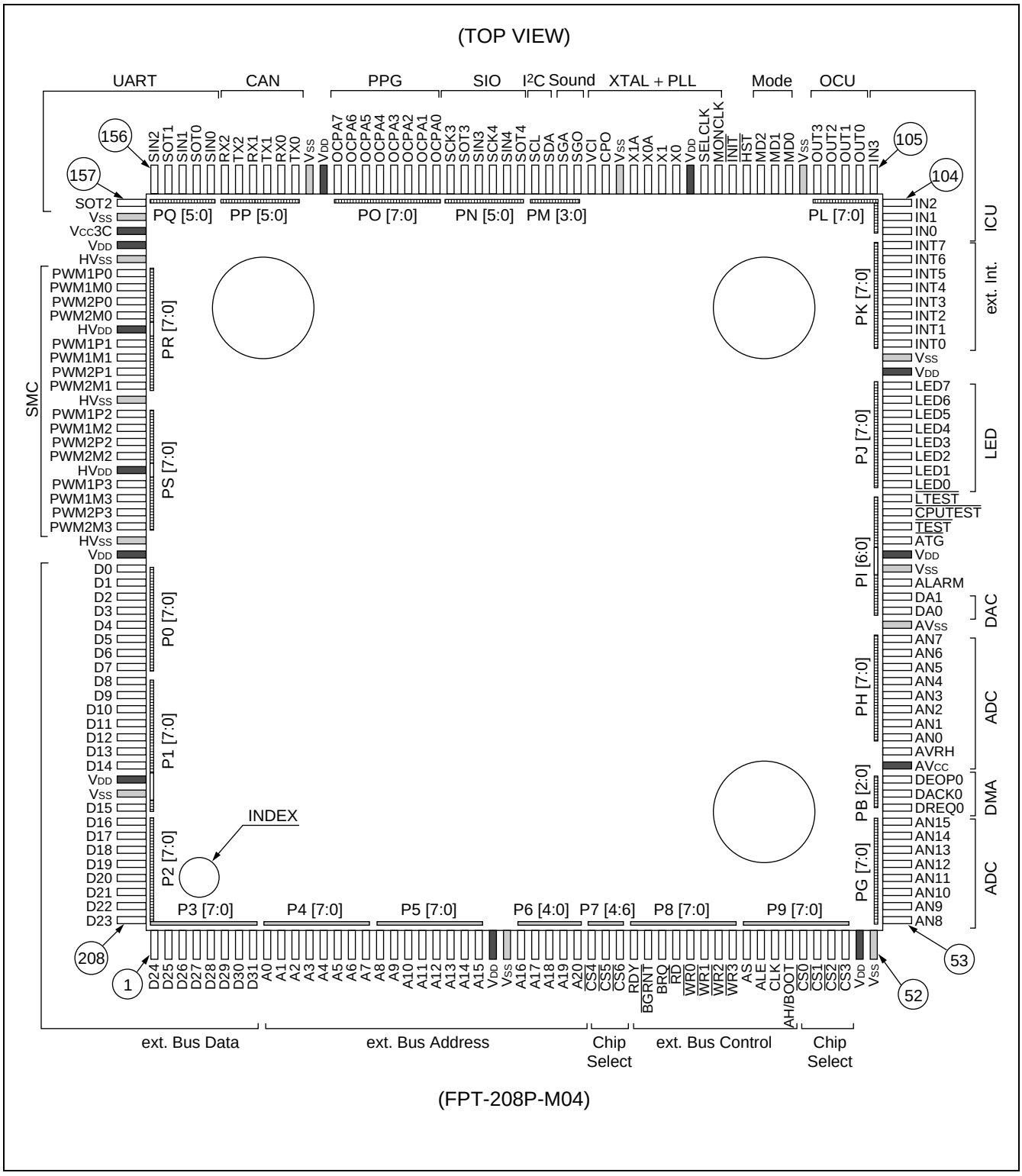
• MB91FV360GA

(BOTTOM VIEW)



(PGA-401C-A02)

- **MB91F361GA/F362GA**



(FPT-208P-M04)

■ PIN DESCRIPTIONS

Pin No. QFP208	Pin No. PGA401	Pin Name	I/O	General Purpose IO Port	Circuit Type FV360GA	Circuit Type F361GA F362GA	Function
9	202	A0	I/O	—	Q	Q	Ext. Bus Address Bit 0
10	310	A1	I/O	—	Q	Q	Ext. Bus Address Bit 1
11	201	A2	I/O	—	Q	Q	Ext. Bus Address Bit 2
12	357	A3	I/O	—	Q	Q	Ext. Bus Address Bit 3
26	358	V_{SS}	—	—	—	—	—
25	401	V_{DD}	—	—	—	—	—
13	257	A4	I/O	—	Q	Q	Ext. Bus Address Bit 4
14	144	A5	I/O	—	Q	Q	Ext. Bus Address Bit 5
15	309	A6	I/O	—	Q	Q	Ext. Bus Address Bit 6
16	256	A7	I/O	—	Q	Q	Ext. Bus Address Bit 7
17	200	A8	I/O	—	Q	Q	Ext. Bus Address Bit 8
18	356	A9	I/O	—	Q	Q	Ext. Bus Address Bit 9
19	308	A10	I/O	—	Q	Q	Ext. Bus Address Bit 10
20	92	A11	I/O	—	Q	Q	Ext. Bus Address Bit 11
—	400	V_{SS}	—	—	—	—	—
21	44	A12	I/O	—	Q	Q	Ext. Bus Address Bit 12
22	255	A13	I/O	—	Q	Q	Ext. Bus Address Bit 13
23	143	A14	I/O	—	Q	Q	Ext. Bus Address Bit 14
24	199	A15	I/O	—	Q	Q	Ext. Bus Address Bit 15
27	307	A16	I/O	—	Q	Q	Ext. Bus Address Bit 16
—	355	not connected					
28	91	A17	I/O	—	Q	Q	Ext. Bus Address Bit 17
29	142	A18	I/O	—	Q	Q	Ext. Bus Address Bit 18
30	254	A19	I/O	—	Q	Q	Ext. Bus Address Bit 19
—	399	V_{SS}	—	—	—	—	—
31	43	A20	I/O	—	Q	Q	Ext. Bus Address Bit 20
—	198	A21	I/O	—	Q	—	Ext. Bus Address Bit 21
—	141	A22	I/O	—	Q	—	Ext. Bus Address Bit 22
—	90	A23	I/O	—	Q	—	Ext. Bus Address Bit 23
—	197	A24	I/O	P70	Q	—	Ext. Bus Address Bit 24
—	306	A25	I/O	P71	Q	—	Ext. Bus Address Bit 25
—	42	A26	I/O	P72	Q	—	Ext. Bus Address Bit 26
—	253	DREQ2	I/O	P73	A	—	DMA Request 2

(Continued)

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Pin No. QFP208	Pin No. PGA401	Pin Name	I/O	General Purpose IO Port	Circuit Type FV360GA	Circuit Type F361GA F362GA	Function
32	140	$\overline{CS4}$	I/O	P74	A	A	Chip Select 4
—	398	V_{SS}	—	—	—	—	—
—	354	V_{DD}	—	—	—	—	—
33	196	$\overline{CS5}$	I/O	P75	A	A	Chip Select 5
34	89	$\overline{CS6}$	I/O	P76	A	A	Chip Select 6
—	41	$\overline{CS7}$	I/O	P77	A	—	Chip Select 7 (CANs)
35	305	RDY	I/O	—	S	S	Ext. Bus Control
36	139	$\overline{BGRNT}$	I/O	P81	A	A	Ext. Bus Control
37	88	BRQ	I/O	P82	A	A	Ext. Bus Control
38	40	$\overline{RD}$	I/O	—	S	S	Ext. Bus Control
39	304	$\overline{WR0}$	I/O	—	S	S	Ext. Bus Control
—	353	V_{SS}	—	—	—	—	—
40	39	$\overline{WR1}$	I/O	—	S	S	Ext. Bus Control
41	252	$\overline{WR2}$	I/O	—	S	S	Ext. Bus Control
42	251	$\overline{WR3}$	I/O	—	S	S	Ext. Bus Control
43	87	AS	I/O	P90	A	A	Ext. Bus Control
44	38	ALE	I/O	P91	A	A	(Ext. Bus Control, not yet implemented)
—	397	not connected					
45	194	CLK	I/O	—	A	A	Ext. Bus Clk
46	195	AH/BOOT	I/O	P93	A	A	Test Signal/Boot Signal
47	137	$\overline{CS0}$	I/O	P94	A	A	Chip select 0
52	352	V_{SS}	—	—	—	—	—
48	250	$\overline{CS1}$	I/O	P95	A	A	Chip Select 1
49	351	$\overline{CS2}$	I/O	P96	A	A	Chip Select 2
50	138	$\overline{CS3}$	I/O	P97	A	A	Chip Select 3
53	37	AN8	I/O	PG0	B	B	ADC Input 8
54	86	AN9	I/O	PG1	B	B	ADC Input 9
55	136	AN10	I/O	PG2	B	B	ADC Input 10
56	303	AN11	I/O	PG3	B	B	ADC Input 11
57	302	AN12	I/O	PG4	B	B	ADC Input 12
58	36	AN13	I/O	PG5	B	B	ADC Input 13
—	396	V_{SS}	—	—	—	—	—
51	350	V_{DD}	—	—	—	—	—

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Pin No. QFP208	Pin No. PGA401	Pin Name	I/O	General Purpose IO Port	Circuit Type FV360GA	Circuit Type F361GA F362GA	Function
59	85	AN14	I/O	PG6	B	B	ADC Input 14
60	249	AN15	I/O	PG7	B	B	ADC Input 15
61	193	DREQ0	I/O	PB0	A	A	DMA Request 0
62	135	DACK0	I/O	PB1	A	A	DMA Acknowledge 0
63	84	DEOP0	I/O	PB2	A	A	DMA EOP 0
—	301	DREQ1	I/O	PB3	A	—	DMA Request 1
—	192	DACK1	I/O	PB4	A	—	DMA Acknowledge 1
—	191	DEOP1	I/O	PB5	A	—	DMA EOP 1
—	395	V_{SS}	—	—	—	—	—
—	35	DACK2	I/O	PB6	A	—	DMA Acknowledge 2
—	349	DEOP2	I/O	PB7	A	—	DMA EOP 2
64	83	AV_{CC}	—	—	—	—	Analog V_{CC}
65	300	AVRH	—	—	R	R	Analog Reference High
66	248	AN0	I/O	PH0	B	B	ADC Input 0
—	393	not connected					
67	82	AN1	I/O	PH1	B	B	ADC Input 1
68	134	AN2	I/O	PH2	B	B	ADC Input 2
69	34	AN3	I/O	PH3	B	B	ADC Input 3
—	394	V_{SS}	—	—	—	—	—
70	190	AN4	I/O	PH4	B	B	ADC Input 4
71	247	AN5	I/O	PH5	B	B	ADC Input 5
72	81	AN6	I/O	PH6	B	B	ADC Input 6
73	133	AN7	I/O	PH7	B	B	ADC Input 7
—	299	AVRL	—	—	R	—	Analog Reference Low
74	348	AV_{SS}	—	—	—	—	Analog V_{SS}
75	246	DA0	O	—	C	C	DAC Output
76	189	DA1	O	—	C	C	DAC Output
77	132	ALARM	I	—	D	D	Alarm Comparator Input
78	392	V_{SS}	—	—	—	—	—
79	347	V_{DD}	—	—	—	—	—
80	298	$\overline{ATG}$	I/O	PI3	A	A	ADC Trigger Input
81	245	$\overline{TEST}$	I	—	E	E	Test Input
82	188	$\overline{CPUTEST}$	I	—	E	E	Test Input
83	297	$\overline{LTEST}$	I	—	E	E	Test Input

(Continued)

(Continued)

Pin No. QFP208	Pin No. PGA401	Pin Name	I/O	General Purpose IO Port	Circuit Type FV360GA	Circuit Type F361GA F362GA	Function
—	244	not connected					
84	346	LED0	I/O	PJ0	J	J	LED Port 0
85	187	LED1	I/O	PJ1	J	J	LED Port 1
86	345	LED2	I/O	PJ2	J	J	LED Port 2
—	391	V_{SS}	—	—	—	—	—
—	390	not connected					
87	243	LED3	I/O	PJ3	J	J	LED Port 3
88	131	LED4	I/O	PJ4	J	J	LED Port 4
89	296	LED5	I/O	PJ5	J	J	LED Port 5
90	242	LED6	I/O	PJ6	J	J	LED Port 6
91	186	LED7	I/O	PJ7	J	J	LED Port 7
94	344	INT0	I/O	PK0	A	A	Ext. Interrupt 0
95	295	INT1	I/O	PK1	A	A	Ext. Interrupt 1
96	80	INT2	I/O	PK2	A	A	Ext. Interrupt 2
93	389	V_{SS}	—	—	—	—	—
97	33	INT3	I/O	PK3	A	A	Ext. Interrupt 3
98	241	INT4	I/O	PK4	A	A	Ext. Interrupt 4
99	130	INT5	I/O	PK5	A	A	Ext. Interrupt 5
100	185	INT6	I/O	PK6	A	A	Ext. Interrupt 6
101	294	INT7	I/O	PK7	A	A	Ext. Interrupt 7
92	343	V_{DD}	—	—	—	—	—
102	79	IN0	I/O	PL0	A	A	ICU Input 0
103	129	IN1	I/O	PL1	A	A	ICU Input 1
104	240	IN2	I/O	PL2	A	A	ICU Input 2
110	388	V_{SS}	—	—	—	—	—
105	32	IN3	I/O	PL3	A	A	ICU Input 3
106	184	OUT0	I/O	PL4	A	A	OCU Output 0
107	128	OUT1	I/O	PL5	A	A	OCU Output 1
108	78	OUT2	I/O	PL6	A	A	OCU Output 2
109	183	OUT3	I/O	PL7	A	A	OCU Output 3
111	293	MD0	I	—	T	T	Mode Pin 0
112	31	MD1	I	—	T	T	Mode Pin 1
113	239	MD2	I	—	T	T	Mode Pin 2
—	127	$\overline{NMI}$	I	—	E	—	Non maskable Interrupt

(Continued)

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Pin No. QFP208	Pin No. PGA401	Pin Name	I/O	General Purpose IO Port	Circuit Type FV360GA	Circuit Type F361GA F362GA	Function
—	387	V_{SS}	—	—	—	—	—
—	342	not connected					
114	182	$\overline{HST}$	I	—	E	E	Hardware Standby
—	77	$\overline{RST}$	I	—	E	—	Reset Pin
115	30	$\overline{INIT}$	I	—	U	U	Initial Pin
116	292	MONCLK	O	—	G	G	System Clock Output
117	126	SELCLK	I	—	F	F	Clock Selection
118	76	V_{DD}	—	—	—	—	—
119	29	X0	—	—	H	H	4 MHz Oscillator Pin
120	291	X1	—	—	H	H	4 MHz Oscillator Pin
—	341	V_{SS}	—	—	—	—	—
—	28	ICLK	IO	—	L	—	ICE CLK
—	238	ICS0	O	—	G	—	ICE Status
—	237	ICS1	O	—	G	—	ICE Status
—	75	ICS2	O	—	G	—	ICE Status
—	27	ICD0	I/O	—	N	—	ICE Data
—	386	V_{DD}	—	—	—	—	—
—	180	ICD1	I/O	—	N	—	ICE Data
—	181	ICD2	I/O	—	N	—	ICE Data
—	124	ICD3	I/O	—	N	—	ICE Data
—	340	V_{SS}	—	—	—	—	—
—	236	BREAK	I	—	O	—	ICE Break
—	339	TDT0	I/O	—	W	—	Trace Data
—	125	TDT1	I/O	—	W	—	Trace Data
—	26	TDT2	I/O	—	W	—	Trace Data
—	74	TDT3	I/O	—	W	—	Trace Data
—	123	TDT4	I/O	—	W	—	Trace Data
—	290	TDT5	I/O	—	W	—	Trace Data
—	289	TDT6	I/O	—	W	—	Trace Data
—	25	TDT7	I/O	—	W	—	Trace Data
—	385	$V_{SS}3$	—	—	—	—	—
—	338	$V_{DD}3$	—	—	—	—	—
—	73	TDT8	I/O	—	W	—	Trace Data
—	235	TDT9	I/O	—	W	—	Trace Data

(Continued)

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Pin No. QFP208	Pin No. PGA401	Pin Name	I/O	General Purpose IO Port	Circuit Type FV360GA	Circuit Type F361GA F362GA	Function
—	179	TDT10	I/O	—	W	—	Trace Data
—	122	TDT11	I/O	—	W	—	Trace Data
—	72	TDT12	I/O	—	W	—	Trace Data
—	288	TDT13	I/O	—	W	—	Trace Data
—	178	TDT14	I/O	—	W	—	Trace Data
—	177	TDT15	I/O	—	W	—	Trace Data
—	384	$V_{SS}3$	—	—	—	—	—
—	24	TDT16	I/O	—	W	—	Trace Data
—	337	TDT17	I/O	—	W	—	Trace Data
—	71	TDT18	I/O	—	W	—	Trace Data
—	287	TDT19	I/O	—	W	—	Trace Data
—	234	TDT20	I/O	—	W	—	Trace Data
—	382	not connected					
—	70	TDT21	I/O	—	W	—	Trace Data
—	121	TDT22	I/O	—	W	—	Trace Data
—	23	TDT23	I/O	—	W	—	Trace Data
—	383	$V_{SS}3$	—	—	—	—	—
—	176	TDT24	I/O	—	W	—	Trace Data
—	233	TDT25	I/O	—	W	—	Trace Data
—	69	TDT26	I/O	—	W	—	Trace Data
—	120	TDT27	I/O	—	W	—	Trace Data
—	286	TDT28	I/O	—	W	—	Trace Data
—	336	TDT29	I/O	—	W	—	Trace Data
—	232	TDT30	I/O	—	W	—	Trace Data
—	175	TDT31	I/O	—	W	—	Trace Data
—	119	TDT32	I/O	—	W	—	Trace Data
—	381	$V_{SS}3$	—	—	—	—	—
—	335	$V_{DD}3$	—	—	—	—	—
—	285	TDT33	I/O	—	W	—	Trace Data
—	231	TDT34	I/O	—	W	—	Trace Data
—	174	TDT35	I/O	—	W	—	Trace Data
—	284	TDT36	I/O	—	W	—	Trace Data
—	230	TDT37	I/O	—	W	—	Trace Data
—	334	TDT38	I/O	—	W	—	Trace Data

(Continued)

(Continued)

Pin No. QFP208	Pin No. PGA401	Pin Name	I/O	General Purpose IO Port	Circuit Type FV360GA	Circuit Type F361GA F362GA	Function
—	173	TDT39	I/O	—	W	—	Trace Data
—	333	TDT40	I/O	—	W	—	Trace Data
—	380	$V_{SS}3$	—	—	—	—	—
—	379	not connected					
—	229	TDT41	I/O	—	W	—	Trace Data
—	118	TDT42	I/O	—	W	—	Trace Data
—	283	TDT43	I/O	—	W	—	Trace Data
—	228	TDT44	I/O	—	W	—	Trace Data
—	172	TDT45	I/O	—	W	—	Trace Data
—	332	TDT46	I/O	—	W	—	Trace Data
—	282	TDT47	I/O	—	W	—	Trace Data
—	68	TDT48	I/O	—	W	—	Trace Data
—	378	$V_{SS}3$	—	—	—	—	—
—	22	TDT49	I/O	—	W	—	Trace Data
—	227	TDT50	I/O	—	W	—	Trace Data
—	117	TDT51	I/O	—	W	—	Trace Data
—	171	TDT52	I/O	—	W	—	Trace Data
—	281	TDT53	I/O	—	W	—	Trace Data
—	331	$V_{DD}3$	—	—	—	—	—
—	67	TDT54	I/O	—	W	—	Trace Data
—	116	TDT55	I/O	—	W	—	Trace Data
—	226	TDT56	I/O	—	W	—	Trace Data
—	377	$V_{SS}3$	—	—	—	—	—
—	21	TDT57	I/O	—	W	—	Trace Data
—	170	TDT58	I/O	—	W	—	Trace Data
—	115	TDT59	I/O	—	W	—	Trace Data
—	66	TDT60	I/O	—	W	—	Trace Data
—	169	TDT61	I/O	—	W	—	Trace Data
—	280	TDT62	I/O	—	W	—	Trace Data
—	20	TDT63	I/O	—	W	—	Trace Data
—	225	TDT64	I/O	—	W	—	Trace Data
—	114	TDT65	I/O	—	W	—	Trace Data
—	376	$V_{SS}3$	—	—	—	—	—
—	330	not connected					

(Continued)

(Continued)

Pin No. QFP208	Pin No. PGA401	Pin Name	I/O	General Purpose IO Port	Circuit Type FV360GA	Circuit Type F361GA F362GA	Function
—	168	TDT66	I/O	—	W	—	Trace Data
—	65	TDT67	I/O	—	W	—	Trace Data
—	19	TDT68	I/O	—	W	—	Trace Data
—	279	TAD0	O	—	X	—	Trace Address
—	113	TAD1	O	—	X	—	Trace Address
—	64	TAD2	O	—	X	—	Trace Address
—	18	TAD3	O	—	X	—	Trace Address
—	278	TAD4	O	—	X	—	Trace Address
—	329	$V_{SS}3$	—	—	—	—	—
—	17	TAD5	O	—	X	—	Trace Address
—	224	TAD6	O	—	X	—	Trace Address
—	223	TAD7	O	—	X	—	Trace Address
—	63	TAD8	O	—	X	—	Trace Address
—	16	TAD9	O	—	X	—	Trace Address
—	375	$V_{DD}3$	—	—	—	—	—
—	166	TAD10	O	—	X	—	Trace Address
—	167	TAD11	O	—	X	—	Trace Address
—	111	TAD12	O	—	X	—	Trace Address
—	328	$V_{SS}3$	—	—	—	—	—
—	222	TAD13	O	—	X	—	Trace Address
—	327	TAD14	O	—	X	—	Trace Address
—	112	TAD15	O	—	X	—	Trace Address
—	15	$\overline{TWR}$	O	—	X	—	Trace Control
—	62	$\overline{TOE}$	O	—	X	—	Trace Control
—	110	TCLK	I/O	—	W	—	Trace Control
—	277	$\overline{TCE1}$	O	—	X	—	Trace Control
—	276	$\overline{TADSC}$	O	—	X	—	Trace Control
—	14	EXRAM	I	—	P	—	Trace Control
—	374	V_{SS}	—	—	—	—	—
—	326	V_{DD}	—	—	—	—	—
126	61	SGO	I/O	PM0	A	A	Sound Generator SGO
127	221	SGA	I/O	PM1	A	A	Sound Generator SGA
128	165	SDA	I/O	PM2	Y	Y	I^2C SDA
129	109	SCL	I/O	PM3	Y	Y	I^2C SCL

(Continued)

(Continued)

Pin No. QFP208	Pin No. PGA401	Pin Name	I/O	General Purpose IO Port	Circuit Type FV360GA	Circuit Type F361GA F362GA	Function
—	60	not connected					
—	275	V_{DD}	—	—	—	—	—
121	164	X0A	I	—	I	reserved should be connected to be V_{SS}	32 kHz Oscillator Pin
122	163	X1A	O	—	I	reserved should be left open	32 kHz Oscillator Pin
123	373	V_{SS}	—	—	—	—	—
—	13	V_{DD}	—	—	—	—	—
124	325	CPO	not connected			reserved should be left open	—
125	59	VCI	not connected			reserved should be connected to be V_{SS}	—
—	274	not connected					
—	220	V_{SS}	—	—	—	—	—
—	371	not connected					
130	58	SOT4	I/O	PN0	A	A	SIO Output
131	108	SIN4	I/O	PN1	A	A	SIO Input
132	12	SCK4	I/O	PN2	A	A	SIO Clock
—	372	V_{SS}	—	—	—	—	—
—	162	V_{DD}	—	—	—	—	—
133	219	SIN3	I/O	PN3	A	A	SIO Input
134	57	SOT3	I/O	PN4	A	A	SIO Output
135	107	SCK3	I/O	PN5	A	A	SIO Clock
—	273	V_{SS}	—	—	—	—	—
—	324	V_{DD}	—	—	—	—	—
136	218	OCPA0	I/O	PO0	A	A	PPG Output
137	161	OCPA1	I/O	PO1	A	A	PPG Output
138	106	OCPA2	I/O	PO2	A	A	PPG Output
—	370	V_{SS}	—	—	—	—	—
—	323	V_{DD}	—	—	—	—	—
139	272	OCPA3	I/O	PO3	A	A	PPG Output

(Continued)

(Continued)

Pin No. QFP208	Pin No. PGA401	Pin Name	I/O	General Purpose IO Port	Circuit Type FV360GA	Circuit Type F361GA F362GA	Function
140	217	OCPA4	I/O	PO4	A	A	PPG Output
141	160	OCPA5	I/O	PO5	A	A	PPG Output
—	271	V_{SS}	—	—	—	—	—
144	216	V_{DD}	—	—	—	—	—
142	322	OCPA6	I/O	PO6	A	A	PPG Output
143	159	OCPA7	I/O	PO7	A	A	PPG Output
146	321	TX0	I/O	PP0	Q	Q	CAN 0 TX
145	369	V_{SS}	—	—	—	—	—
—	368	not connected					
147	215	RX0	I/O	PP1	Q	Q	CAN 0 RX
148	105	TX1	I/O	PP2	Q	Q	CAN 1 TX
149	270	RX1	I/O	PP3	Q	Q	CAN 1 RX
—	214	V_{SS}	—	—	—	—	—
—	158	V_{DD}	—	—	—	—	—
150	320	TX2	I/O	PP4	Q	Q	CAN 2 TX
151	269	RX2	I/O	PP5	Q	Q	CAN 2 RX
—	56	TX3	I/O	PP6	Q	—	CAN 3 TX
—	367	V_{SS}	—	—	—	—	—
—	11	V_{DD}	—	—	—	—	—
—	213	RX3	I/O	PP7	Q	—	CAN 3 RX
152	104	SIN0	I/O	PQ0	A	A	UART 0 Input
153	157	SOT0	I/O	PQ1	A	A	UART 0 Output
—	268	V_{SS}	—	—	—	—	—
—	319	V_{DD}	—	—	—	—	—
154	55	SIN1	I/O	PQ2	A	A	UART 1 Input
155	103	SOT1	I/O	PQ3	A	A	UART 1 Output
156	212	SIN2	I/O	PQ4	A	A	UART 2 Input
—	366	V_{SS}	—	—	—	—	—
160	10	V_{DD}	—	—	—	—	V_{DD}
157	156	SOT2	I/O	PQ5	A	A	UART 2 Output
159	102	V_{CC}3C	—	—	C	C	Bypass Capacitor Pin
—	54	not connected					
158	155	V_{SS}	—	—	—	—	—
—	267	not connected					

(Continued)

(Continued)

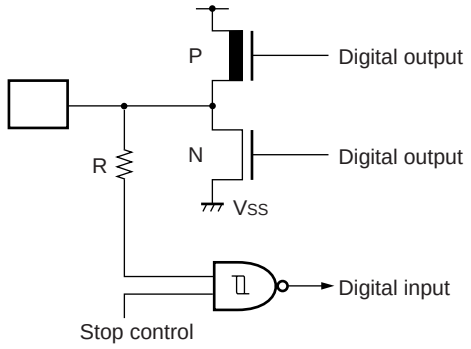
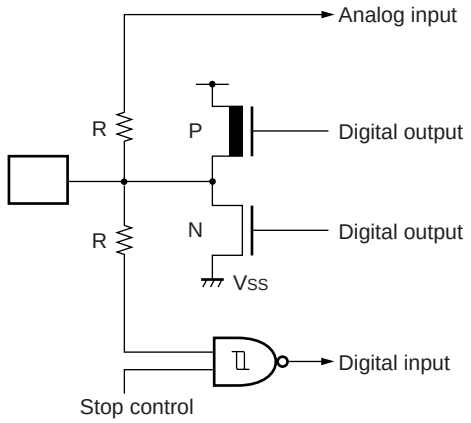
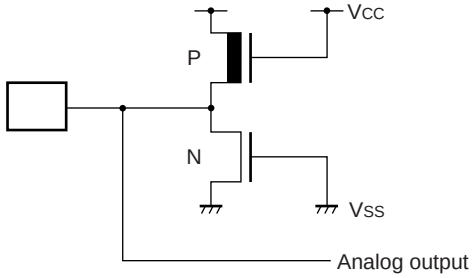
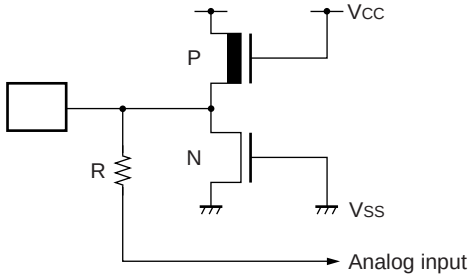
Pin No. QFP208	Pin No. PGA401	Pin Name	I/O	General Purpose IO Port	Circuit Type FV360GA	Circuit Type F361GA F362GA	Function
162	9	PWM1P0	I/O	PR0	K	K	SMC 0
163	211	PWM1M0	I/O	PR1	K	K	SMC 0
164	101	PWM2P0	I/O	PR2	K	K	SMC 0
161	365	HV_{SS}	—	—	—	—	—
—	318	not connected					
165	154	PWM2M0	I/O	PR3	M	M	SMC 0
167	53	PWM1P1	I/O	PR4	K	K	SMC 1
168	8	PWM1M1	I/O	PR5	K	K	SMC 1
—	266	HV_{SS}	—	—	—	—	—
166	100	HV_{DD}	—	—	—	—	—
169	52	PWM2P1	I/O	PR6	K	K	SMC 1
170	7	PWM2M1	I/O	PR7	M	M	SMC 1
—	265	not connected					
171	317	HV_{SS}	—	—	—	—	—
—	6	HV_{DD}	—	—	—	—	—
172	210	PWM1P2	I/O	PS0	K	K	SMC 2
173	209	PWM1M2	I/O	PS1	K	K	SMC 2
174	51	PWM2P2	I/O	PS2	K	K	SMC 2
—	5	HV_{SS}	—	—	—	—	—
—	364	not connected					
175	152	PWM2M2	I/O	PS3	M	M	SMC 2
177	153	PWM1P3	I/O	PS4	K	K	SMC 3
178	98	PWM1M3	I/O	PS5	K	K	SMC 3
181	316	HV_{SS}	—	—	—	—	—
176	208	HV_{DD}	—	—	—	—	—
179	315	PWM2P3	I/O	PS6	K	K	SMC 3
180	99	PWM2M3	I/O	PS7	M	M	SMC 3
—	4	not connected					
—	50	V_{SS}	—	—	—	—	—
182	97	V_{DD}	—	—	—	—	—
183	264	D0	I/O	—	Q	Q	Ext. Bus Data Bit 0
184	263	D1	I/O	—	Q	Q	Ext. Bus Data Bit 1
185	3	D2	I/O	—	Q	Q	Ext. Bus Data Bit 2
—	363	V_{SS}	—	—	—	—	—

(Continued)

(Continued)

Pin No. QFP208	Pin No. PGA401	Pin Name	I/O	General Purpose IO Port	Circuit Type FV360GA	Circuit Type F361GA F362GA	Function
—	314	not connected					
186	49	D3	I/O	—	Q	Q	Ext. Bus Data Bit 3
187	207	D4	I/O	—	Q	Q	Ext. Bus Data Bit 4
188	151	D5	I/O	—	Q	Q	Ext. Bus Data Bit 5
189	96	D6	I/O	—	Q	Q	Ext. Bus Data Bit 6
190	48	D7	I/O	—	Q	Q	Ext. Bus Data Bit 7
191	262	D8	I/O	—	Q	Q	Ext. Bus Data Bit 8
192	150	D9	I/O	—	Q	Q	Ext. Bus Data Bit 9
193	149	D10	I/O	—	Q	Q	Ext. Bus Data Bit 10
—	362	V_{SS}	—	—	—	—	—
194	2	D11	I/O	—	Q	Q	Ext. Bus Data Bit 11
195	313	D12	I/O	—	Q	Q	Ext. Bus Data Bit 12
196	47	D13	I/O	—	Q	Q	Ext. Bus Data Bit 13
197	261	D14	I/O	—	Q	Q	Ext. Bus Data Bit 14
200	206	D15	I/O	—	Q	Q	Ext. Bus Data Bit 15
198	360	V_{DD}	—	—	—	—	—
201	46	D16	I/O	—	Q	Q	Ext. Bus Data Bit 16
202	95	D17	I/O	—	Q	Q	Ext. Bus Data Bit 17
203	1	D18	I/O	—	Q	Q	Ext. Bus Data Bit 18
199	361	V_{SS}	—	—	—	—	—
204	148	D19	I/O	—	Q	Q	Ext. Bus Data Bit 19
205	205	D20	I/O	—	Q	Q	Ext. Bus Data Bit 20
206	45	D21	I/O	—	Q	Q	Ext. Bus Data Bit 21
207	94	D22	I/O	—	Q	Q	Ext. Bus Data Bit 22
208	260	D23	I/O	—	Q	Q	Ext. Bus Data Bit 23
1	312	D24	I/O	—	Q	Q	Ext. Bus Data Bit 24
2	204	D25	I/O	—	Q	Q	Ext. Bus Data Bit 25
3	147	D26	I/O	—	Q	Q	Ext. Bus Data Bit 26
4	93	D27	I/O	—	Q	Q	Ext. Bus Data Bit 27
—	359	V_{SS}	—	—	—	—	—
—	311	not connected					
5	259	D28	I/O	—	Q	Q	Ext. Bus Data Bit 28
6	203	D29	I/O	—	Q	Q	Ext. Bus Data Bit 29
7	146	D30	I/O	—	Q	Q	Ext. Bus Data Bit 30
8	258	D31	I/O	—	Q	Q	Ext. Bus Data Bit 31

■ I/O CIRCUIT TYPE

Type	Circuit type	Remarks
A		• I/O, CMOS Automotive Schmitt-Trigger Input, STOP control, I_{OH} = 4 mA, I_{OL} = 4 mA
B		• I/O, CMOS Automotive Schmitt-Trigger Input, Analog Input, STOP control, I_{OH} = 4 mA, I_{OL} = 4 mA
C		• Analog output
D		• Analog Input

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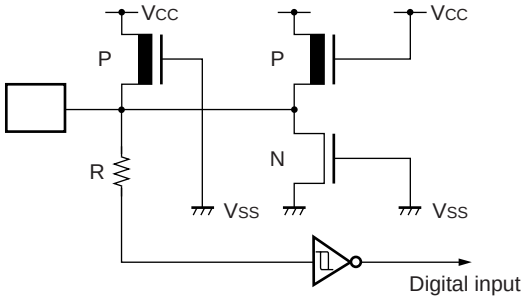
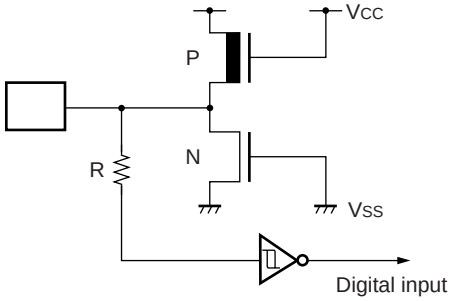
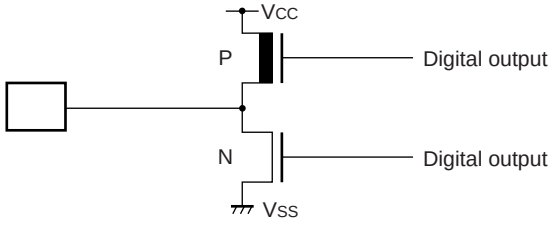
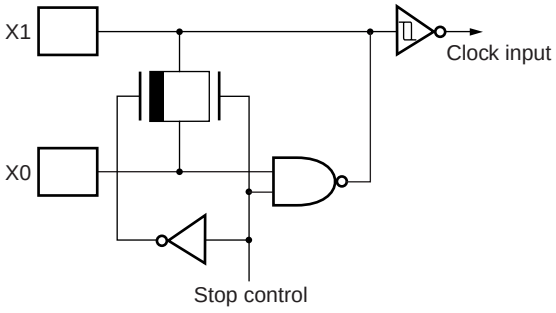
Type	Circuit type	Remarks
E		• CMOS Schmitt-Trigger Input, Pullup Resistor: 50 kΩ
F		• CMOS Schmitt-Trigger Input
G		• Tristate Output, I_{OH} = 4 mA, I_{OL} = 4 mA
H		• 4 MHz Oscillator Pin

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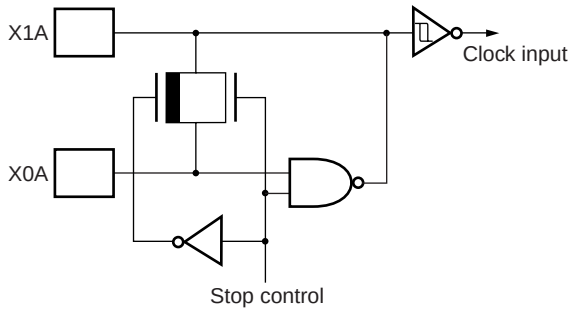
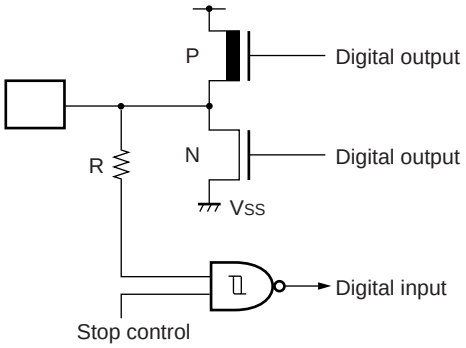
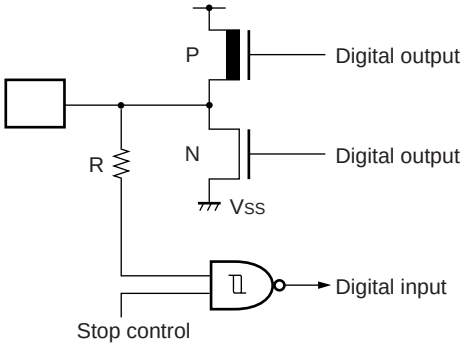
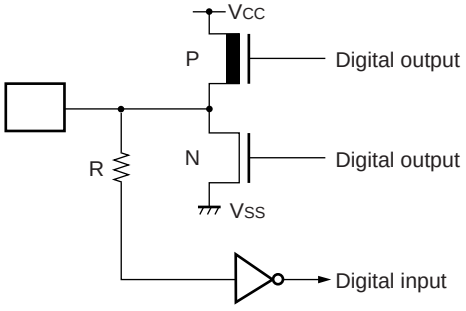
Type	Circuit type	Remarks
I		• 32 kHz Oscillator Pin
J		• I/O, CMOS Automotive Schmitt-Trigger Input, STOP control (LED) , I_{OH} = 14 mA, I_{OL} = 24 mA
K		• I/O, CMOS Automotive Schmitt-Trigger Input, STOP control (SMC) , I_{OH} = 30 mA, I_{OL} = 30 mA • Typ. slew rate of 40 ns
L		• I/O, CMOS Input; 5 V or 3 V input, I_{OH} = 4 mA, I_{OL} = 4 mA

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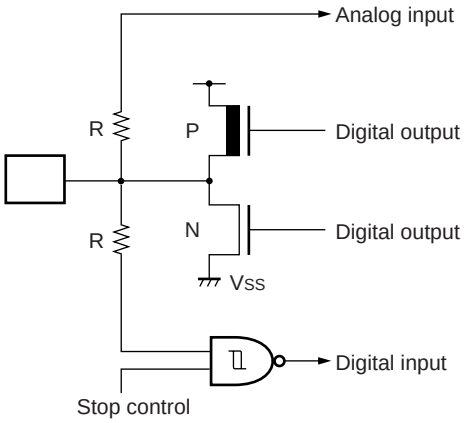
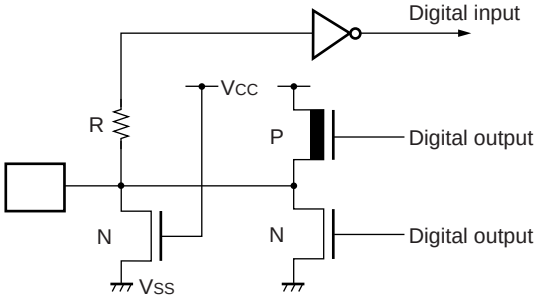
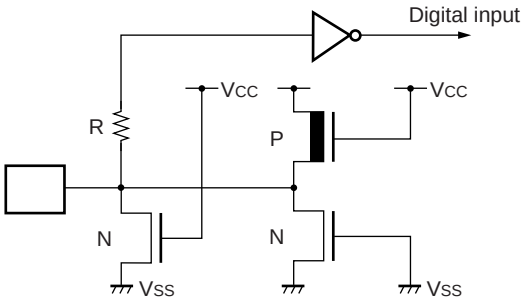
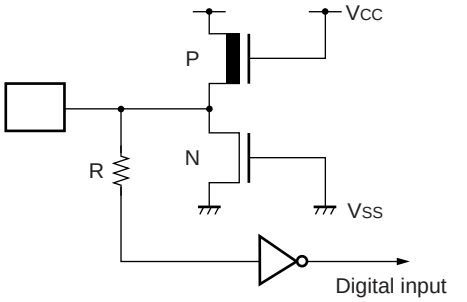
Type	Circuit type	Remarks
M		• I/O, CMOS Automotive Schmitt-Trigger Input, Analog Input, STOP control (SMC) , I_{OH} = 30 mA, I_{OL} = 30 mA • Typ. slew rate of 40 ns
N		• I/O, CMOS Input, Pulldown Resistor: 50 kΩ, 5 V or 3 V input, I_{OH} = 4 mA, I_{OL} = 4 mA
O		• CMOS Input, Pulldown Resistor: 50 kΩ, 5 V or 3 V input
P		• CMOS Input; 3 V input

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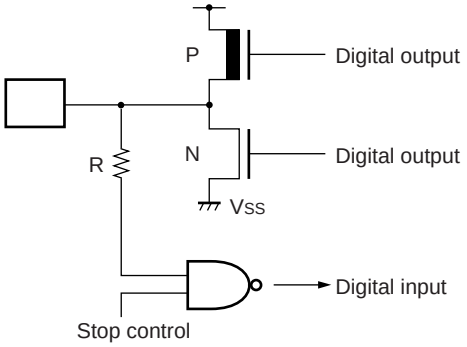
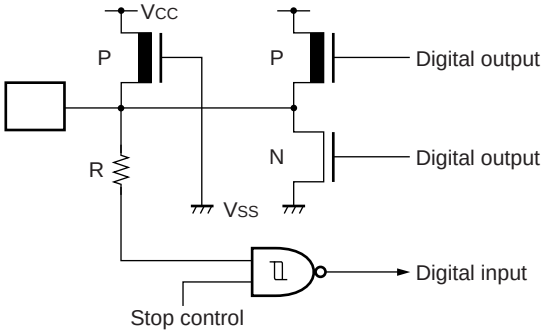
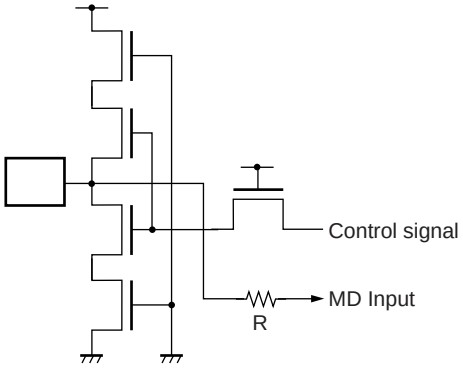
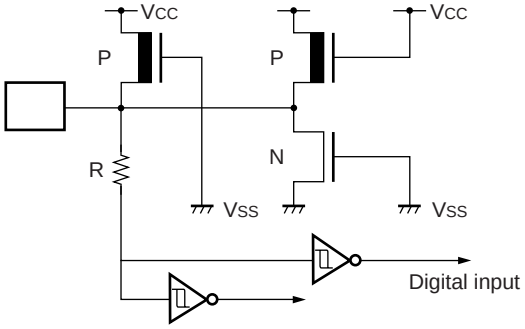
Type	Circuit type	Remarks
Q		• I/O CMOS Input, STOP control, I_{OH} = 4 mA, I_{OL} = 4 mA
S		• I/O, CMOS Schmitt-Trigger Input, STOP control, Pullup Resistor : 10 kΩ, I_{OH} = 4 mA, I_{OL} = 4 mA
T		• CMOS Input • can withstand high V_{ID} for flash programming
U		• CMOS Schmitt-Trigger Input, Pullup Resistor: 50 kΩ, 3 V and 5 V input to the core

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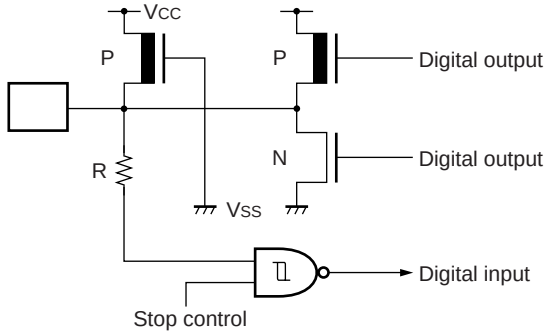
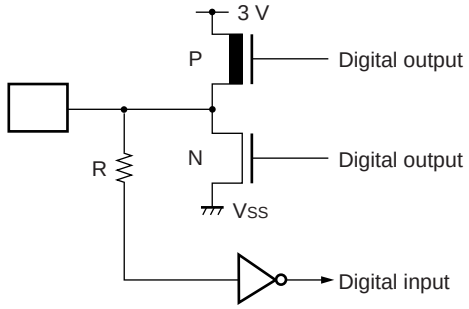
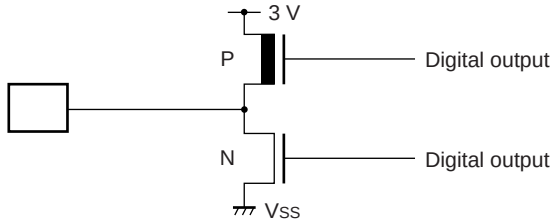
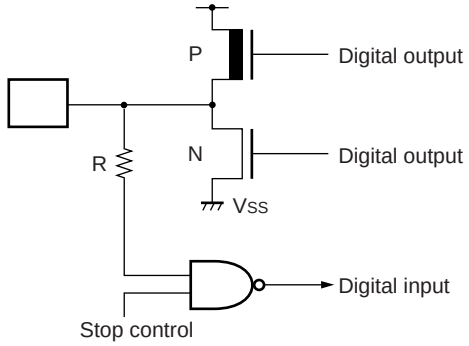
Type	Circuit type	Remarks
V		• I/O, CMOS Schmitt-Trigger Input, STOP control, Pullup Resistor: 50 kΩ,, I_{OH} = 4 mA, I_{OL} = 4 mA
W		• I/O, CMOS Input; 3 V input
X		• Tristate Output, 3 V
Y		• I/O CMOS Input, STOP control, I_{OH} = 3 mA, I_{OL} = 3 mA, in I^2C mode operating as open drain outputs

Note : Symbols used in circuit types (Common to all circuit diagrams)
P : P channel transistor
N : N channel transistor
R : Diffusion resistor

Circuit Type	Description
A	I/O, I_{OH} = 4 mA / I_{OL} = 4 mA, CMOS Automotive Schmitt-Trigger Input, STOP control
B	I/O, I_{OH} = 4 mA / I_{OL} = 4 mA, CMOS Automotive Schmitt-Trigger Input, Analog Input, STOP control
C	Analog Output
D	Analog Input
E	CMOS Schmitt-Trigger Input, Pull-up Resistor: 50 kΩ,
F	CMOS Schmitt-Trigger Input
G	Tristate Output, I_{OH} = 4 mA / I_{OL} = 4 mA
H	4 MHz Oscillator Pin
I	32 kHz Oscillator pin
J	I/O, I_{OH} = 14 mA / I_{OL} = 24 mA, CMOS Automotive Schmitt-Trigger Input, STOP control (LED)
K	I/O, I_{OH} = 30 mA / I_{OL} = 30 mA, CMOS Automotive Schmitt-Trigger Input, STOP control, slew rate improved for EMC (SMC)
L	I/O, I_{OH} = 4 mA / I_{OL} = 4 mA, CMOS Input; 5 V or 3 V input
M	I/O, I_{OH} = 30 mA / I_{OL} = 30 mA, CMOS Automotive Schmitt-Trigger Input, Analog Input, STOP control, slew rate improved for EMC (SMC)
N	I/O, I_{OH} = 4 mA / I_{OL} = 4 mA, CMOS Input, Pulldown Resistor: 50 kΩ,; 5 V or 3 V input
O	CMOS Input, Pulldown Resistor: 50 kΩ,; 5 V or 3 V input
P	CMOS Input; 3 V input
Q	I/O, I_{OH} = 4 mA / I_{OL} = 4 mA, CMOS Input, STOP control
R	AVRL / AVRH Input
S	I/O, I_{OH} = 4 mA / I_{OL} = 4 mA, CMOS Input, STOP control, Pull-up Resistor: 10 kΩ,
T	CMOS Input, can withstand V_{ID} for flash programming
U	CMOS Schmitt-Trigger Input, Pull-up Resistor: 50 kΩ,, 3.3 V and 5 V inputs to core
W	I/O, I_{OH} = 4 mA / I_{OL} = 4 mA, CMOS Input; 3 V input
X	Tristate Output, I_{OH} = 4 mA / I_{OL} = 4 mA, 3 V
Y	I/O, I_{OH} = 3 mA / I_{OL} = 3 mA (I^2C) , CMOS Input, STOP control

■ HANDLING DEVICES

1. Preventing latch-up

Latch-up may occur in a CMOS IC if a voltage greater than V_{DD} or less than V_{SS} is applied to an input or output pin or if the voltage applied between V_{DD} and V_{SS} exceeds the rating. If latch-up occurs, the power supply current increases rapidly resulting in thermal damage to circuit elements. Therefore, ensure that maximum ratings are not exceeded in circuit operation.

2. Connecting unused pins

Leaving unused input pins open may result in misbehavior or latch up and possible permanent damage of the device. Therefore they must be tied to V_{DD} or V_{SS} through resistors. In this case those resistors should be more than 2 KOhm.

Unused bidirectional pins should be set to the output state and can be left open, or the input state with the above described connection.

The resistor of more than 2 KOhm is used to limit currents through the protection diodes. In case of voltages at the not used pin of 0.3 V or more below V_{SS} or 0.3 V or more above V_{DD} currents which could cause latch-up will flow through those diodes.

3. External reset input

When inputting an “L” level to the $\overline{INIT}$ pin, hold this low level at the $\overline{INIT}$ pin long enough so that after release of the low level at $\overline{INIT}$ and the passing of the built in waiting time stable oscillation of the oscillation circuit is achieved. $\overline{INIT}$ must be pulled low for at least 8 cycles of the 4 MHz oscillation clock.

4. Power supply pins

All V_{DD} pins should be connected to the same potential (exception can be the external bus interface on F361GA and F362GA) . The analogue supply voltage (AV_{CC}) must not be turned on before the digital supply voltage. If the external bus interface is supplied with 3.3 V this voltage also must not be turned on before the 5 V digital voltage has been switched on. If the supply voltage to the external bus interface is switched off (it may not be tristate but should be pulled low) it must be made sure that all related signals do not have a voltage higher than this pulled down supply.

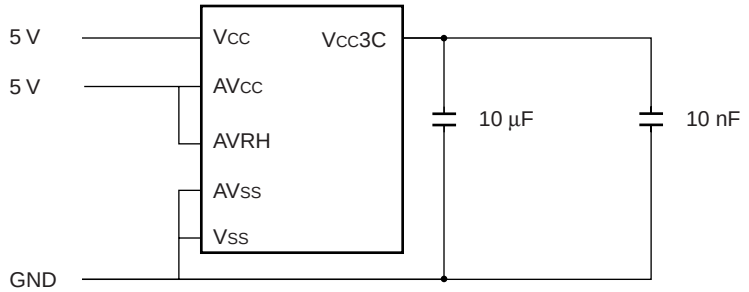
When multiple V_{DD} and V_{SS} pins are provided, be sure to connect all V_{DD} and V_{SS} pins to the power supply or ground externally. Although pins at the same potential are connected together in the internal device design so as to prevent malfunctions such as latch-up, connecting all V_{DD} and V_{SS} pins appropriately minimizes unwanted radiation, prevents malfunction of strobe signals due to increases in the ground level, and keeps the overall output current rating.

Also, take care to connect V_{DD} and V_{SS} to current source in the lowest possible impedance.

Connection of a ceramic bypass capacitor of approximately 0.1 µF between V_{DD} and V_{SS} close to the device is recommended.

The MB91360G series contains a regulator. To use the device with the 5-V power supply, supply 5-V power to the V_{CC} pins and be sure to connect a bypass capacitor of 10 µF parallel to 10 nF to the $V_{CC}3C$ pin for the regulator.

[Use with 5-V power supply]



5. Crystal oscillator circuit

Noise in the vicinity of the X0 and X1 pins can be a cause of device malfunction. Design the circuit board so that X0, X1, the crystal oscillator (or ceramic oscillator) , and the bypass capacitor to ground are located as close to the device as possible.

A printed circuit board design that surrounds the X0 and X1 pins with ground provides for stable operation and is strongly recommended.

6. Mode pins

Connect the mode pins (MD0 to MD2) directly to V_{DD} or V_{SS}.

To prevent the device unintentionally entering test mode due to noise, lay out the printed circuit board so as to minimize the distance from the mode pins to V_{DD} or V_{SS} and to provide a low-impedance connection.

7. Turning the power supply on

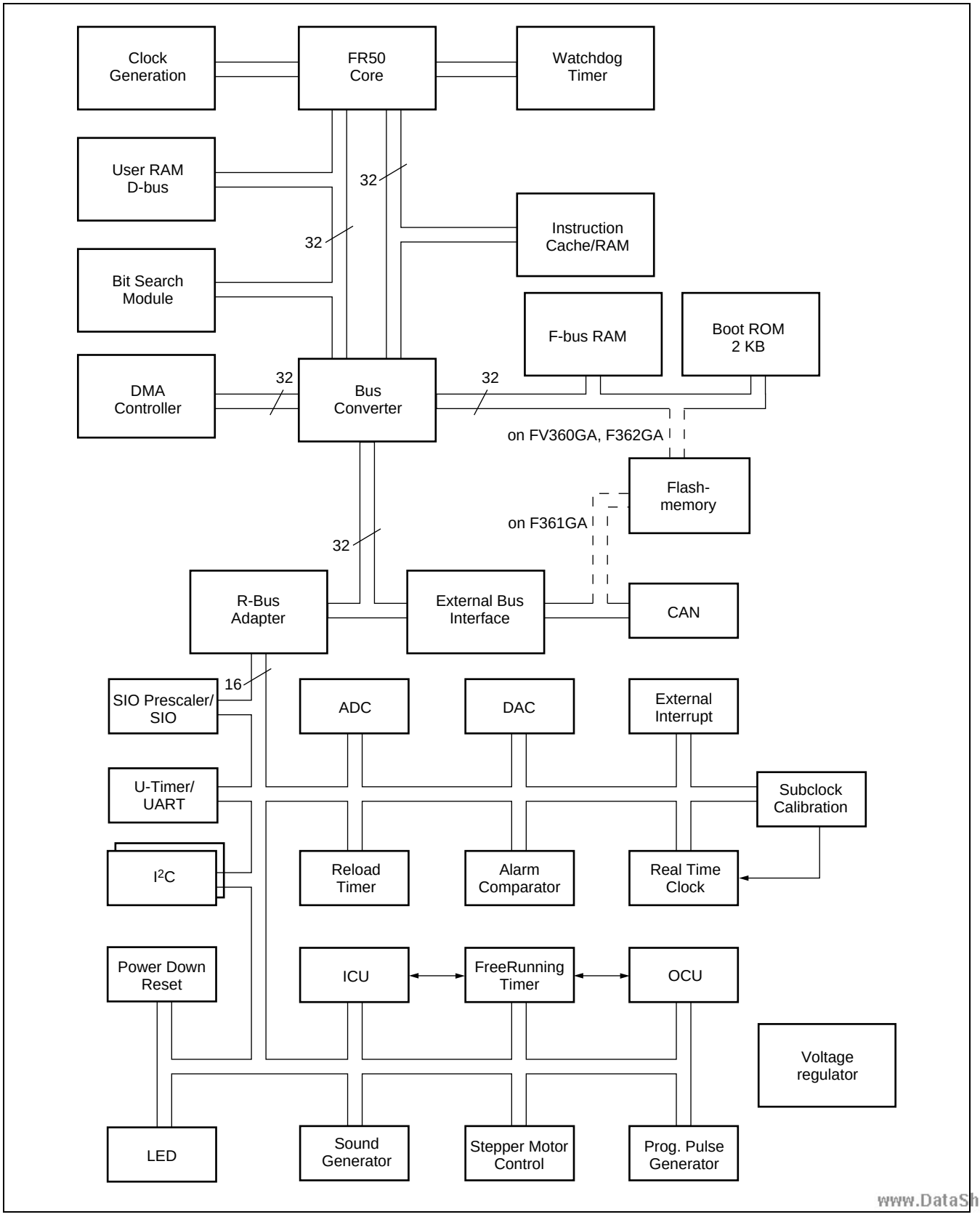
Immediately after power on always execute INIT at the $\overline{INIT}$ pin (start with a low level at the $\overline{INIT}$ pin) . Hold this low level at the $\overline{INIT}$ pin long enough so that after release of the low level at $\overline{INIT}$ and the passing of the built in waiting time stable oscillation of the oscillation circuit is achieved. $\overline{INIT}$ must be pulled low for at least 8 cycles of the 4 MHz oscillation clock.

The analogue supply voltage (AV_{CC}) must not be turned on before the digital supply voltage. If the external bus interface is supplied with 3.3 V this voltage also must not be turned on before the 5 V digital voltage has been switched on.

8. A state in turning power on

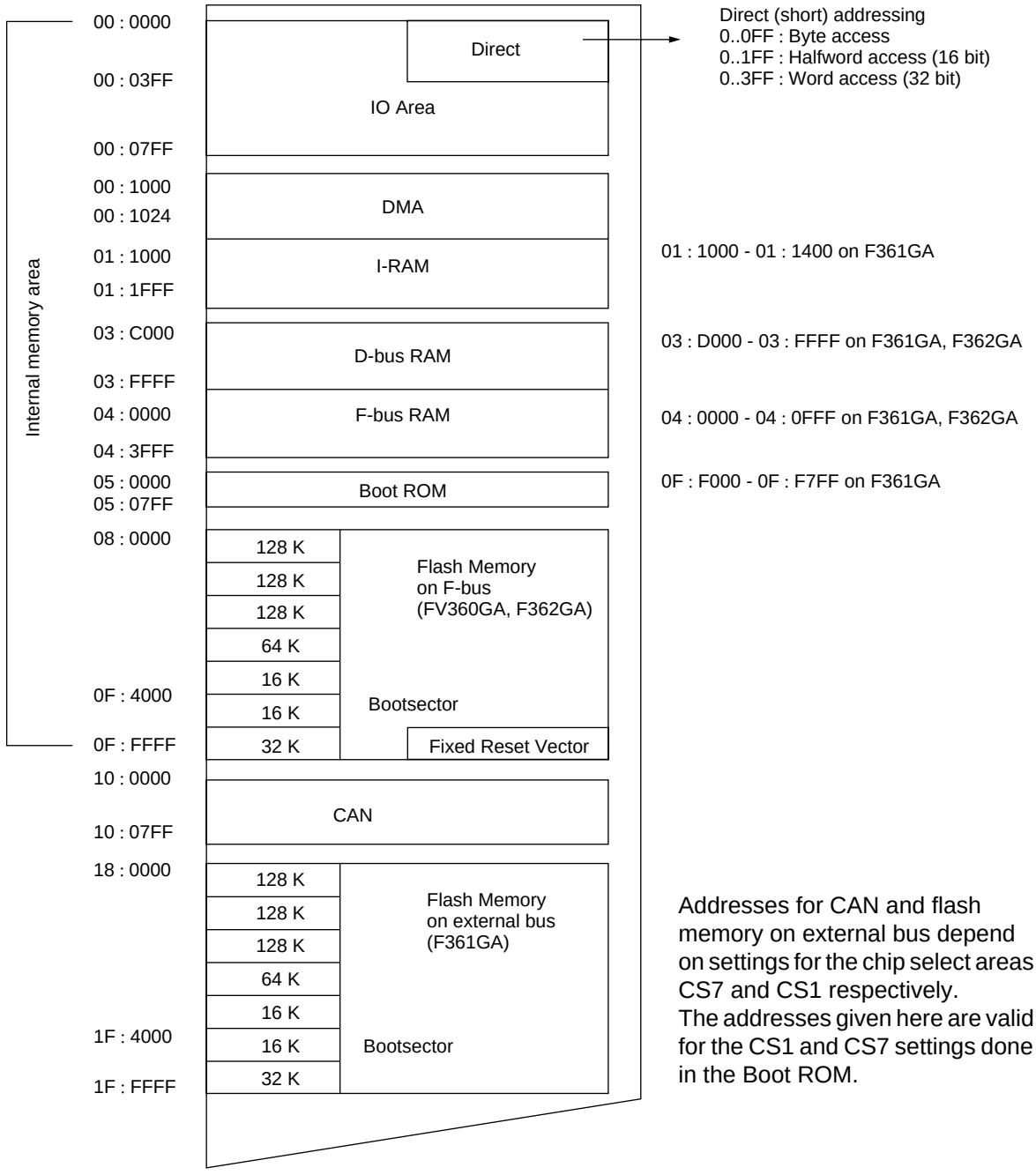
Output pin level is not guranteed while supply voltage does not reach minimum operation voltage in turning power on.

■ BLOCK DIAGRAM



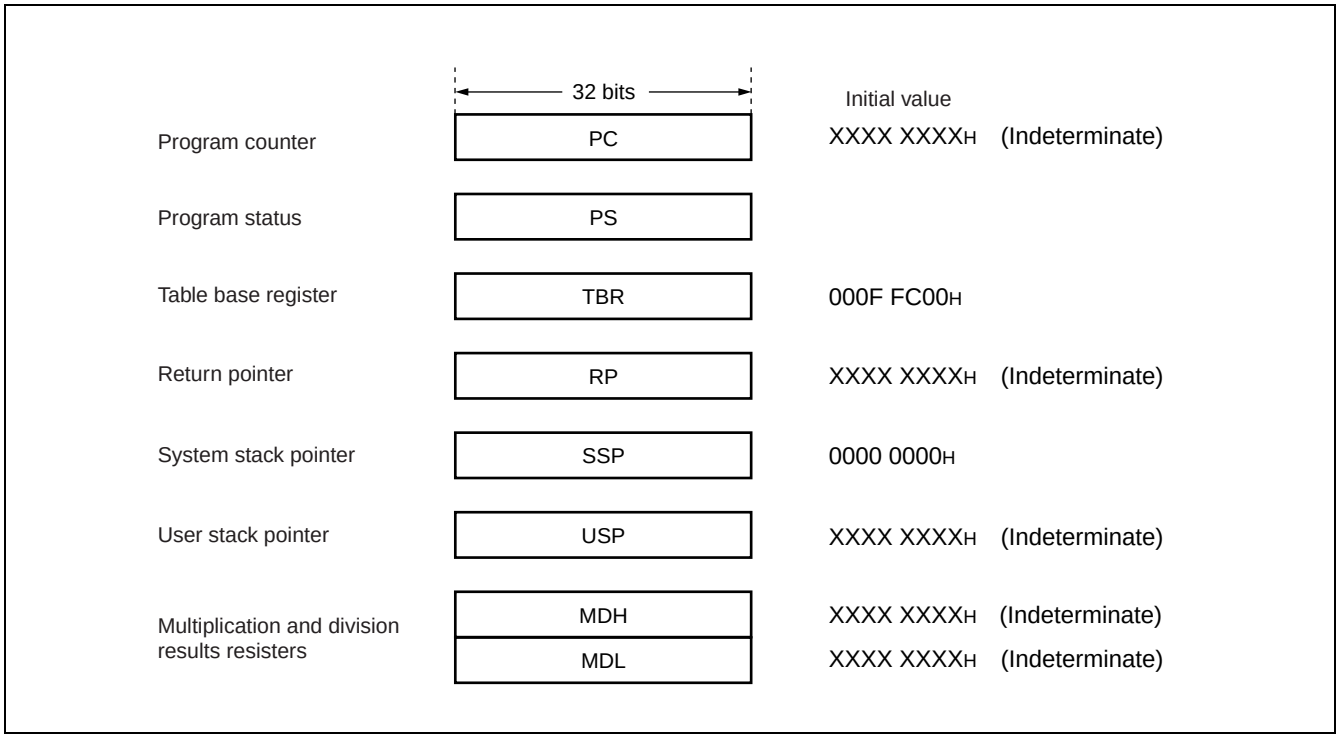
■ CPU CORE

1. Memory Space

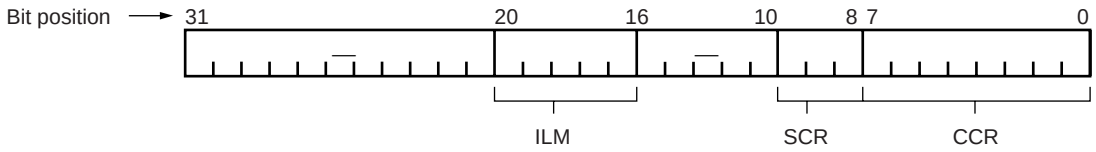


2. Dedicated Registers

Each of the dedicated registers is used for a particular purpose. The dedicated registers consist of the program counter (PC) , program status (PS) , table base register (TBR) , return pointer (RP) , system stack pointer (SSP) , user stack pointer (USP) , and multiplication and division result registers (MDH/MDL) .

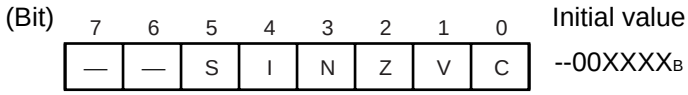


(1) Program status (PS)

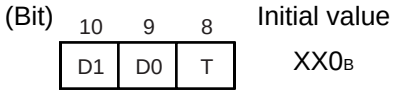


CCR : Condition Code Register
SCR : System Condition Code Register
ILM : Interrupt Level Mask

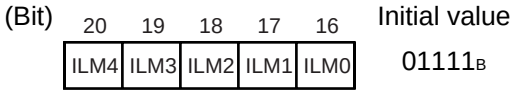
(2) Condition Code Register (CCR)



(3) System Condition Code Register (SCR)



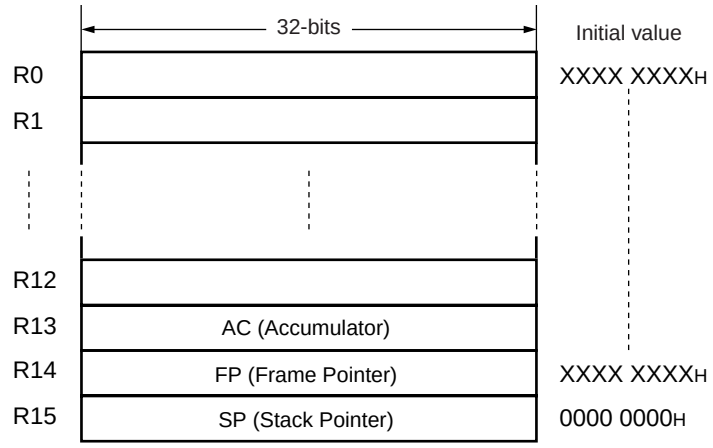
(4) Interrupt Level Mask Register (ILM)



3. General-Purpose Registers

The general-purpose registers are CPU registers R0 to R15. The register are used as the accumulator for operations and as pointers (a field indicating an address) for memory access. The user can specify the purpose for which the general-purpose registers are used.

Register bank structure



Among 16 general-purpose registers, the following registers assume a special purpose. This enhances some instructions.

- R13 : Virtual accumulator (AC)
- R14 : Frame pointer (FP)
- R15 : Stack pointer (SP)

The initial value of R0 to R14 after a reset is indeterminate. The initial value of R15 is 00000000_H (SSP value) .

■ MODE SETTING

The FR50 series of devices uses mode pins (MD2 to MD0) and a mode register (MODR) to set the operation mode.

(1) Mode Pins

Three mode pins (MD2 to MD0) are used to specify the reset mode vector access area.

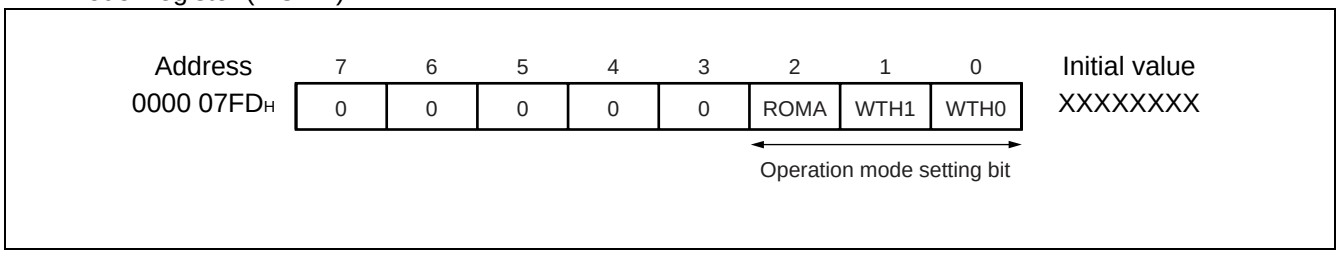
Mode Pins			Mode name	Reset vector access area	Remarks
MD2	MD1	MD0			
0	0	0	Internal ROM mode vector	Internal	
0	0	1	External ROM mode vector	External	The mode register is used to set the bus width.
remaining settings			—	—	Reserved

(2) Mode Register (MODR)

The data to be written to 0000_7FDH using mode vector fetch is called mode data.

MODR is located at 0000_07FDH. After an operation mode has been set in MODR, the device operates in this operation mode. MODR is set only when a reset factor (INIT level) occurs. User programs cannot write data to MODR.

< Mode Register (MODR) >



[Bits 7 to 3] : (Reserved bits)

Always set 00000 at bits 7 to 3. Operation is not guaranteed when other values are set.

[Bit 2] : ROMA (internal ROM enable bit)

The ROMA bit is used to set whether to validate the internal ROM area (Fbus memory area) .

ROMA	Function	Remarks
0	External ROM mode	Access to the Fbus area is external.
1	Internal ROM mode	

[Bits 1 and 0] : WTH1 and WTH0 (bus width/single chip mode specifying bits)

The WTH1 and WTH0 bits are used to set the bus width (valid when operation mode is external bus mode) and the single chip mode. When the operation mode is the external bus mode, this value is set at the BW1 and BW0 bits of AMD0 (CS0 area) .

WTH1	WTH0	Function	Remarks
0	0	8-bit bus width	External bus mode
0	1	16-bit bus width	External bus mode
1	0	32-bit bus width	External bus mode
1	1	Single chip mode	

(3) Fixed Vector

If MB91360 series devices are started in mode MD[2 : 0] = 000, the internal fixed mode vector (FMV = 0x06) and the fixed reset vector are used. The fixed reset vector points to the start address of the internal Boot ROM.

This enables access to the F-bus area, to the internal CAN modules and the internal flash memory.

See also section Boot ROM.

■ I/O MAP

Address	Register				Block
	+0	+1	+2	+3	
000000H	reserved	reserved	reserved	reserved	T-unit Port Data Register
000004H	reserved	reserved	reserved	PDR7 [R/W] -111 - - - -	
000008H	PDR8 [R/W] - - - - - XX -	PDR9 [R/W] XXXXXXX1	—	PDRB [R/W] - - - - - XXX	
00000CH	—				
000010H	PDRG [R/W] XXXXXXXX	PDRH [R/W] XXXXXXXX	PDRI [R/W] X - - - X - - -	PDRJ [R/W] XXXXXXXX	R-bus Port Data Register
000014H	PDRK [R/W] XXXXXXXX	PDRL [R/W] XXXXXXXX	PDRM [R/W] - - - - XXXX	PDRN [R/W] - - XXXXXX	
000018H	PDRO [R/W] XXXXXXXX	PDRP [R/W] - - XXXXX	PDRQ [R/W] - - XXXXX	PDRR [R/W] XXXXXXXX	
00001CH	PDRS [R/W] XXXXXXXX	—	—	—	
000020H to 00003CH	—				Reserved
000040H	EIRR [R/W] 00000000	ENIR [R/W] 00000000	ELVR [R/W] 00000000 00000000		Ext int/NMI
000044H	DICR [R/W] - - - - - - - 0	HRCL [R/W] 0 - - 11111	CLKR2 [R/W] - - - - - 000	reserved	DLYI/I-unit RTC
000048H	TMRLR0 [W] XXXXXXXX XXXXXXXX		TMR0 [R] XXXXXXXX XXXXXXXX		Reload Timer 0
00004CH	—		TMCSR0 [R/W] - - - - 0000 - - - 00000		
000050H	TMRLR1 [W] XXXXXXXX XXXXXXXX		TMR1 [R] XXXXXXXX XXXXXXXX		Reload Timer 1
000054H	—		TMCSR1 [R/W] - - - - 0000 - - - 00000		
000058H	TMRLR2 [W] XXXXXXXX XXXXXXXX		TMR2 [R] XXXXXXXX XXXXXXXX		Reload Timer 2
00005CH	—		TMCSR2 [R/W] - - - - 0000 - - - 00000		
000060H	SSR0 [R/W] 00001 - 00	SIDR0 [R/W] XXXXXXXX	SCR0 [R/W] 00000100	SMR0 [R/W] 00 - - 0 - 0 -	UART0
000064H	ULS0 [R/W] - - - - 0000	—	—	—	

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Address	Register				Block
	+0	+1	+2	+3	
000068H	UTIM0/UTIMR0 [R/W] 00000000 00000000		DRCL0 [W] - - - - - - - -	UTIMC0 [R/W] 0 - - - 0 - 01	U-TIMER 0
00006CH	SSR1 [R/W] 00001 - 00	SIDR1 [R/W] XXXXXXXX	SCR1 [R/W] 00000100	SMR1 [R/W] 00 - - 0 - 0 -	UART1
000070H	ULS1 [R/W] - - - - 0000	—	—	—	
000074H	UTIM1/UTIMR1 [R/W] 00000000 00000000		DRCL1 [W] - - - - - - - -	UTIMC1 [R/W] 0 - - - - - 01	U-TIMER 1
000078H	SSR2 [R/W] 00001 - 00	SIDR2 [R/W] XXXXXXXX	SCR2 [R/W] 00000100	SMR2 [R/W] 00 - - 0 - 0 -	UART2
00007CH	ULS2 [R/W] - - - - 0000	—	—	—	
000080H	UTIM2/UTIMR2 [R/W] 00000000 00000000		DRCL2 [W] - - - - - - - -	UTIMC2 [R/W] 0 - - - 0 - 01	U-TIMER2
000084H	SMCS0 [R/W] 00000010 - - - - 00-0		SES0 [R/W] - - - - - - 00	SDR0 [R/W] 00000000	SIO 0
000088H	SMCS1 [R/W] 00000010 - - - - 00 - 0		SES1 [R/W] - - - - - - 00	SDR1 [R/W] 00000000	SIO 1
00008CH	CDCR0 [R/W] 0 - - - 1111	Reserved	CDCR1 [R/W] 0 - - - 1111	Reserved	SIO 0/1 Prescaler
000090H	—				Reserved
000094H	IBCR [R/W] 00000000	IBSR [R] 00000000	IADR [R/W] -XXXXXXX	ICCR [R/W] - - 0XXXXX	I²C (old) → new I²C from addr 0x184
000098H	—	IDAR [R/W] XXXXXXXX	—	IDBL [R/W] - - - - - - - 0	
00009CH	ADMD [R/W, W] - - - X0000	ADCH [R/W] 00000000	—	ADCS [R/W, W] 0000 - - 00	A/D Converter
0000A0H	ADCD [R/W] 000000XX XXXXXXXX		—	ADBL [R/W] - - - - - - - 0	
0000A4H	—	DACR [R/W] - - - - - 000	DADR0 [R/W] - - - - - - XX XXXXXXXX		DAC
0000A8H	DADR1 [R/W] - - - - - - XX XXXXXXXX		—	DDBL [R/W] - - - - - - - 0	
0000ACH	IOTDBL0 [R/W] - - - - - 000	ICS01 [R/W] 00000000	IOTDBL1 [R/W] - - - - - 000	ICS23 [R/W] 00000000	Input Capture 0, 1, 2, 3
0000B0H	IPCP0 [R] XXXXXXXX XXXXXXXX		IPCP1 [R] XXXXXXXX XXXXXXXX		
0000B4H	IPCP2 [R] XXXXXXXX XXXXXXXX		IPCP3 [R] XXXXXXXX XXXXXXXX		

(Continued)

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Address	Register				Block
	+0	+1	+2	+3	
0000B8H	OCS0/1 [R/W] - - - 0 - - 00	0000 - - 00	reserved		Output Compare 0, 1, 2.3
0000BCH	OCCP0 [R/W] XXXXXXXX	XXXXXXXX	OCCP1 [R/W] XXXXXXXX	XXXXXXXX	
0000C0H	OCCP2 [R/W] XXXXXXXX	XXXXXXXX	OCCP3 [R/W] XXXXXXXX	XXXXXXXX	
0000C4H	—				Reserved
0000C8H	TCDT0 [R/W] XXXXXXXX	XXXXXXXX	—	TCCS0 [R/W] - 0000000	Free Running Counter 0 for ICU/OCU
0000CCH	TCDT1 [R/W] XXXXXXXX	XXXXXXXX	—	TCCS1 [R/W] - 0000000	Free Running Counter 1 for ICU/OCU
0000D0H	ZPD0 [R/W] 00000010	PWC0 [R/W] - - 000 - - 0	ZPD1 [R/W] 00000010	PWC1 [R/W] 00000 - - 0	SMC 0, 1
0000D4H	ZPD2 [R/W] 00000010	PWC2 [R/W] - - 000 - - 0	ZPD3 [R/W] 00000010	PWC3 [R/W] 00000 - - 0	SMC 2, 3
0000D8H	PWC20 [R/W] XXXXXXXX	PWC10 [R/W] XXXXXXXX	PWS20 [R/W] - 0000000	PWS10 [R/W] - - 000000	SMC 0
0000DCH	PWC21 [R/W] XXXXXXXX	PWC11 [R/W] XXXXXXXX	PWS21 [R/W] - 0000000	PWS11 [R/W] - - 000000	SMC 1
0000E0H	PWC22 [R/W] XXXXXXXX	PWC12 [R/W] XXXXXXXX	PWS22 [R/W] - 0000000	PWS12 [R/W] - - 000000	SMC 2
0000E4H	PWC23 [R/W] XXXXXXXX	PWC13 [R/W] XXXXXXXX	PWS23 [R/W] - 0000000	PWS13 [R/W] - - 000000	SMC 3
0000E8H	SMDBL0 [R/W] - - - - - - - 0	SMDBL1 [R/W] - - - - - - 0	SMDBL2 [R/W] - - - - - - - 0	SMDBL3 [R/W] - - - - - - - 0	SMC 0, 1, 2, 3
0000ECH	—	SGDBL [R/W] - - - - - - - 0	SGCR [R, R/W] 0 - - - - - 00	000 - - 000	Sound generator
0000F0H	SGAR [R/W] 00000000	SGFR [R/W] XXXXXXXX	SGTR [R/W] XXXXXXXX	SGDR [R/W] XXXXXXXX	
0000F4H	—	WTDBL [R/W] - - - - - - - 0	WTCR [R, R/W] 00000000	000 - 0000	Real Time Clock (WatchTimer)
0000F8H	—	WTBR [R/W] - - XXXXXX	XXXXXXXX	XXXXXXXX	
0000FCH	WTHR [R/W] - - - 00000	WTMR [R/W] - - 000000	WTSR [R/W] - - 000000	—	
000100H	TMRLR3 [W] XXXXXXXX XXXXXXXX		TMR3 [R] XXXXXXXX XXXXXXXX		Reload Timer 3
000104H	—		TMCSR3 [R/W] - - - - XX - -	- - - XXXXX	

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Address	Register				Block
	+0	+1	+2	+3	
000108H	TMRLR4 [W] XXXXXXXX XXXXXXXX		TMR4 [R] XXXXXXXX XXXXXXXX		Reload Timer 4
00010CH	—		TMCSR4 [R/W] - - - - XX - - - - - XXXXX		
000110H	TMRLR5 [W] XXXXXXXX XXXXXXXX		TMR5 [R] XXXXXXXX XXXXXXXX		Reload Timer 5
000114H	—		TMCSR5 [R/W] - - - - XX - - - - - XXXXX		
000118H	GCN10 [R/W] 00110010 00010000		PDBL0 [R/W] - - - 00000	GCN20 [R/W] - - - - 0000	PWM Control 0
00011CH	GCN11 [R/W] 00110010 00010000		PDBL1 [R/W] - - - 00000	GCN21 [R/W] - - - - 0000	PWM Control 1
000120H	PTMR0 [R] 11111111 11111111		PCSR0 [W] XXXXXXXX XXXXXXXX		PWM0
000124H	PDUT0 [W] XXXXXXXX XXXXXXXX		PCNH0 [R/W] 0000000 -	PCNL0 [R/W] 000000 - 0	
000128H	PTMR1 [R] 11111111 11111111		PCSR1 [W] XXXXXXXX XXXXXXXX		PWM1
00012CH	PDUT1 [W] XXXXXXXX XXXXXXXX		PCNH1 [R/W] 0000000 -	PCNL1 [R/W] 000000 - 0	
000130H	PTMR2 [R] 11111111 11111111		PCSR2 [W] XXXXXXXX XXXXXXXX		PWM2
000134H	PDUT2 [W] XXXXXXXX XXXXXXXX		PCNH2 [R/W] 0000000 -	PCNL2 [R/W] 000000 - 0	
000138H	PTMR3 [R] 11111111 11111111		PCSR3 [W] XXXXXXXX XXXXXXXX		PWM3
00013CH	PDUT3 [W] XXXXXXXX XXXXXXXX		PCNH3 [R/W] 0000000 -	PCNL3 [R/W] 000000 - 0	
000140H	PTMR4 [R] 11111111 11111111		PCSR4 [W] XXXXXXXX XXXXXXXX		PWM4
000144H	PDUT4 [W] XXXXXXXX XXXXXXXX		PCNH4 [R/W] 0000000 -	PCNL4 [R/W] 000000 - 0	
000148H	PTMR5 [R] 11111111 11111111		PCSR5 [W] XXXXXXXX XXXXXXXX		PWM5
00014CH	PDUT5 [W] XXXXXXXX XXXXXXXX		PCNH5 [R/W] 0000000 -	PCNL5 [R/W] 000000 - 0	
000150H	PTMR6 [R] 11111111 11111111		PCSR6 [W] XXXXXXXX XXXXXXXX		PWM6
000154H	PDUT 6 [W] XXXXXXXX XXXXXXXX		PCNH6 [R/W] 0000000 -	PCNL6 [R/W] 000000 - 0	

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Address	Register				Block
	+0	+1	+2	+3	
000158H	PTMR7 [R] 11111111 11111111		PCSR7 [W] XXXXXXXX XXXXXXXX		PWM7
00015CH	PDUT7 [W] XXXXXXXX XXXXXXXX		PCNH7 [R/W] 0000000 -	PCNL7 [R/W] 000000 - 0	
000160H	—				Reserved
000164H	CMCR [R/W] 11111111 0000000		CMPR [R/W] - - - -1001 1 - - -0001		Clock Modulation
000168H	CMLS0 [R/W] 01110111 1111111		CMLS1 [R/W] 01110111 1111111		
00016CH	CMLS2 [R/W] 01110111 1111111		CMLS3 [R/W] 01110111 1111111		
000170H	CMLT0 [R/W] - - - - -100 00000010		CMLT1 [R/W] 11110100 00000010		
000174H	CMLT2 [R/W] - - - - -100 00000010		CMLT3 [R/W] - - - - -100 00000010		
000178H	CMAC [R/W] 11111111 1111111		CMTS [R/W] - -000001 01111111		
00017CH	—	PDRCR [R/W] - - - - - 000	—	—	Power down reset
000180H	ACCDBL[R/W] - - - - - - - 0	ACSR [R, R/W] - - - XXX00	—	—	Alarm comparator
000184H	IBCR2 [R/W, W] 00000000	IBSR2 [R] 00000000	ITBAH [R/W] - - - - - - 00	ITBAL [R/W] 00000000	I²C (new)
000188H	ITMKH [R/W, W] 00 - - - - 11	ITMKL [R/W] 11111111	ISMK [R/W] 01111111	ISBA [R/W] - 0000000	
00018CH	IDARH [-] 00000000	IDAR2 [R/W] 00000000	ICCR2 [R/W] - 0011111	IDBL2 (*) [R/W] - - - - - - - 0	
000190H	CUCR [R, R/W] - - - - - - - - - - - - 0 - -00		CUTD [R/W] 10000000 00000000		Calibration Unit of 32 kHz oscillator
000194H	CUTR1 [R] - - - - - - - - 00000000		CUTR2 [R] 00000000 00000000		
000198H to 0001F8H	—				Reserved
0001FCH	—	—	F362MD [R/W] 00000000	—	F362GA Mode Register
000200H	DMACA0 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				DMAC
000204H	DMACB0 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				

* : Old and new I²C share this bit.

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Address	Register				Block
	+0	+1	+2	+3	
000208H	DMACA1 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				DMAC
00020CH	DMACB1 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000210H	DMACA2 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
000214H	DMACB2 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000218H	DMACA3 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
00021CH	DMACB3 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000220H	DMACA4 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
000224H	DMACB4 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000228H to 00023CH	—				
000240H	DMACR [R/W] 00 - - 0000 -				
000244H to 0002FCH	—				Reserved
000300H	IRBS 00000000 00000001 00100000 - - - - - - - -				Instruction Cache
000304H	—			ISIZE [R/W] - - - - - -11	
000308H to 0003E0H	—				Reserved
0003E4H	—			ICHRC 0-000000	Instruction Cache
0003E8H to 0003ECH	—				Reserved

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Address	Register				Block
	+0	+1	+2	+3	
0003F0H	BSD0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Bit Search Module
0003F4H	BSD1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0003F8H	BSDC [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0003FCH	BSRR [R] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000400H	DDRG [R/W] 00000000	DDRH [R/W] 00000000	DDRI [R/W] - - - -0- - -	DDRJ [R/W] 00000000	R-bus Port Direction Register
000404H	DDRK [R/W] 00000000	DDRL [R/W] 00000000	DDRM [R/W] - - - -0000	DDRN [R/W] - -000000	
000408H	DDRO [R/W] 00000000	DDRP [R/W] - - - -0000	DDRQ [R/W] - -000000	DDRR [R/W] 00000000	
00040CH	DDRS [R/W] 00000000	—	—	—	
000410H	PFRG [R/W] 00000000	PFRH [R/W] 00000000	PFRI [R/W] - - - -0- - -	PFRJ [R/W] 00000000	R-bus Port Function Register
000414H	PFRK [R/W] 00000000	PFRL [R/W] 00000000	PFRM [R/W] - - - -0000	PFRN [R/W] - -000000	
000418H	PFRO [R/W] 00000000	PFRP [R/W] 00000000	PFRQ [R/W] - -000000	PFRR [R/W] 00000000	
00041CH	PFRS [R/W] 00000000	—	—	—	
000420H to 00043CH	—				Reserved
000440H	ICR00 [R, R/W] - - -11111	ICR01 [R, R/W] - - -11111	ICR02 [R, R/W] - - -11111	ICR03 [R, R/W] - - -11111	Interrupt Control unit
000444H	ICR04 [R, R/W] - - -11111	ICR05 [R, R/W] - - -11111	ICR06 [R, R/W] - - -11111	ICR07 [R, R/W] - - -11111	
000448H	ICR08 [R, R/W] - - -11111	ICR09 [R, R/W] - - -11111	ICR10 [R, R/W] - - -11111	ICR11 [R, R/W] - - -11111	
00044CH	ICR12 [R, R/W] - - -11111	ICR13 [R, R/W] - - -11111	ICR14 [R, R/W] - - -11111	ICR15 [R, R/W] - - -11111	
000450H	ICR16 [R, R/W] - - -11111	ICR17 [R, R/W] - - -11111	ICR18 [R, R/W] - - -11111	ICR19 [R, R/W] - - -11111	
000454H	ICR20 [R, R/W] - - -11111	ICR21 [R, R/W] - - -11111	ICR22 [R, R/W] - - -11111	ICR23 [R, R/W] - - -11111	
000458H	ICR24 [R, R/W] - - -11111	ICR25 [R, R/W] - - -11111	ICR26 [R, R/W] - - -11111	ICR27 [R, R/W] - - -11111	

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Address	Register				Block
	+0	+1	+2	+3	
00045C$_H$	ICR28 [R, R/W] - - -11111	ICR29 [R, R/W] - - -11111	ICR30 [R, R/W] - - -11111	ICR31 [R, R/W] - - -11111	Interrupt Control unit
000460$_H$	ICR32 [R, R/W] - - -11111	ICR33 [R, R/W] - - -11111	ICR34 [R, R/W] - - -11111	ICR35 [R, R/W] - - -11111	
000464$_H$	ICR36 [R, R/W] - - -11111	ICR37 [R, R/W] - - -11111	ICR38 [R, R/W] - - -11111	ICR39 [R, R/W] - - -11111	
000468$_H$	ICR40 [R, R/W] - - -11111	ICR41 [R, R/W] - - -11111	ICR42 [R, R/W] - - -11111	ICR43 [R, R/W] - - -11111	
00046C$_H$	ICR44 [R, R/W] - - -11111	ICR45 [R, R/W] - - -11111	ICR46 [R, R/W] - - -11111	ICR47 [R, R/W] - - -11111	
000470$_H$ to 00047C$_H$	—				Reserved
000480$_H$	RSRR [R/W] 10000000	STCR [R/W] 00110011	TBCR [R/W] X0000X00	CTBR [W] XXXXXXXX	Clock Control unit
000484$_H$	CLKR [R/W] 00000000	WPR [W] XXXXXXXX	DIVR0 [R/W] 00000011	DIVR1 [R/W] 00000000	
000488$_H$ to 0005FC$_H$	—				Reserved
000600$_H$	—	—	—	—	T-unit Port Direction Register
000604$_H$	—	—	—	DDR7 [R/W] 00000000	
000608$_H$	DDR8 [R/W] 00000000	DDR9 [R/W] 00000000	—	DDRB [R/W] 00000000	
00060C$_H$	—				
000610$_H$	—	—	—	—	T-unit Port Function Register
000614$_H$	—	—	—	PFR7 [R/W] 00001111	
000618$_H$	PFR8 [R/W] 111110-0	PFR9 [R/W] 11110101	—	PFRB [R/W] 00000000	
00061C$_H$	—				
000620$_H$	—				
000624$_H$	—			PFR27 [R/W] 1111-00-	
000628$_H$ to 00063F$_H$	—				Reserved

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Address	Register				Block
	+0	+1	+2	+3	
000640H	ASR0 [W] 00000000 00000000		AMR0 [W] 11111000 11111111		T-unit
000644H	ASR1 [W] 00000000 00000000		AMR1 [W] 00000000 00000000		
000648H	ASR2 [W] 00000000 00000000		AMR2 [W] 00000000 00000000		
00064CH	ASR3 [W] 00000000 00000000		AMR3 [W] 00000000 00000000		
000650H	ASR4 [W] 00000000 00000000		AMR4 [W] 00000000 00000000		
000654H	ASR5 [W] 00000000 00000000		AMR5 [W] 00000000 00000000		
000658H	ASR6 [W] 00000000 00000000		AMR6 [W] 00000000 00000000		
00065CH	ASR7 [W] 00000000 00000000		AMR7 [W] 00000000 00000000		
000660H	AMD0 [R/W] -00XX111	AMD1 [R/W] -XXXXXXX	AMD2 [R/W] --XXXXXX	AMD3 [R/W] --XXXXXX	
000664H	AMD4 [R/W] --XXXXXX	AMD5 [R/W] --XXXXXX	AMD6 [R/W] -XXXXXXX	AMD7 [R/W] -XXXXXXX	
000668H	CSE [R/W] 11000011	—	—	—	
00066CH	—		—		
000670H	CHE [R/W] 11111111	—	—		
000674H to 0007F8H	—				Reserved
0007FCH	—	MODR [W] XXXXXXXX	—	—	Mode Register
000800H to 000AFCH	—				Reserved
000B00H	ESTS0 X0000000	ESTS1 XXXXXXXX	ESTS2 XXXXXXXX	—	DSU
000B04H	ECTL0 0X000000	ECTL1 00000000	ECTL2 000X0000	ECTL3 00000X11	
000B08H	ECNT0 XXXXXXXX	ECNT1 XXXXXXXX	EUSA XXX0000X	EDTC 0000XXXX	

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Address	Register				Block
	+0	+1	+2	+3	
000B0C$_H$	EWPT XXXXXXXX XXXXXXXX		—		DSU
000B10$_H$	EDTR0 XXXXXXXX XXXXXXXX		EDTR1 XXXXXXXX XXXXXXXX		
000B14$_H$ to 000B1C$_H$	—				
000B20$_H$	EIA0 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B24$_H$	EIA1 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B28$_H$	EIA2 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B2C$_H$	EIA3 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B30$_H$	EIA4 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B34$_H$	EIA5 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B38$_H$	EIA6 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B3C$_H$	EIA7 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B40$_H$	EDTA XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B44$_H$	EDTM XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B48$_H$	EOA0 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B4C$_H$	EOA1 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B50$_H$	EPCR XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B54$_H$	EPSR XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B58$_H$	EIAM0 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B5C$_H$	EIAM1 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B60$_H$	EOAM0/EODM0 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

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Address	Register				Block
	+0	+1	+2	+3	
000B64H	EOAM1/EODM1 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				DSU
000B68H	EOD0 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B6CH	EOD1 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001000H	DMASA0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				DMAC
001004H	DMADA0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001008H	DMASA1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00100CH	DMADA1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001010H	DMASA2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001014H	DMADA2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001018H	DMASA3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00101CH	DMADA3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001020H	DMASA4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001024H	DMADA4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001028H to 003FFCH	—				Reserved
004000H to 006FFFH	—				Reserved
007000H	FMCS [R/W] 1110X000	—	—	—	Flash Memory Control Register on F362GA/ FV360GA
007004H	FMWT [R/W] - -000011	—	—	—	
007008H to 00FFFCH	—				Reserved

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Address	Register				Block
	+0	+1	+2	+3	
010000H to 010FFCH	(for exact address range see "■ PERIPHERAL RESOURCES 1. INSTRUCTION CACHE") on F361GA only 1 K Cache is available, on F362GA no cache, but 4 K I-RAM are available				I-Cache 4 KB
011000H to 011FFCH	—				Reserved
012000H to 01FFFCH	—				Reserved
020000H to 03BFFCH	—				Reserved
03C000H to 03FFFCH	Only first 12 KB are available on F362GA and F361GA				User RAM 16 KB (D-Bus)
040000H to 043FFCH	Only first 4 K are available on F362GA and F361GA				Fast RAM 16 KB (F-Bus)
044000H to 0FEFFC	—				Reserved
050000H to 0507FCH	—				Boot ROM 2 KB (F-Bus)
050800H to 07FFF4H	—				reserved
080000H to 09FFFCH	Sector 0 64 KB		Sector 7 64 KB		Flash Memory 512 K on F-Bus on FV360GA and F362GA
0A0000H to 0BFFFC	Sector 1 64 KB		Sector 8 64 KB		
0C0000H to 0DFFFC	Sector 2 64 KB		Sector 9 64 KB		
0E0000H to 0EFFFC	Sector 3 32 KB		Sector 10 32 KB		
0F0000H to 0F3FFCH	Sector 4 8 KB		Sector 11 8 KB		

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Address	Register				Block
	+0	+1	+2	+3	
0F4000H to 0F7FFCH	Sector 5 8 KB		Sector 12 8 KB		Flash Memory 512 K on F-Bus on FV360GA and F362GA
0F8000H to 0FFFF4H	Sector 6 16 KB		Sector 13 16 KB		
0FFFF8H	FMV [R] 06 00 00 00H				Fixed Reset/Mode Vector
0FFFFCH	FRV [R] 00 05 00 00H on FV360GA/F362GA / 00 FF 00 00 on F361GA				
Write operations to address 0FFFF8H and 0FFFFCH are not possible. When reading these addresses, the values shown above will be read.					

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Address	Register				Block
	+0	+1	+2	+3	
100000H	BVALR0 [R/W] 00000000 00000000		TREQR0 [R/W] 00000000 00000000		CAN 0 Remark : Address range for CAN 0 to CAN 3 depends on chip select range. Mentioned addresses are default values, determined by boot ROM contents.
100004H	TCANR0 [W] 00000000 00000000		TCR0 [R/W] 00000000 00000000		
100008H	RCR0 [R/W] 00000000 00000000		RRTRR0 [R/W] 00000000 00000000		
10000CH	ROVRR0 [R/W] 00000000 00000000		RIER0 [R/W] 00000000 00000000		
100010H	CSR0 [R/W, R] 00000000 00000001		—	LEIR0 [R/W] 000-0000	
100014H	RTEC0 [R] 00000000 00000000		BTR0 [R/W] -1111111 11111111		
100018H	IDER0 [R/W] XXXXXXXX XXXXXXXX		TRTRR0 [R/W] 00000000 00000000		
10001CH	RFWTR0 [R/W] XXXXXXXX XXXXXXXX		TIER0 [R/W] 00000000 00000000		
100020H	AMSR0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
100024H	AMR00 [R/W] XXXXXXXX XXXXXXXX XXXXX - - - XXXXXXXX				
100028H	AMR10 [R/W] XXXXXXXX XXXXXXXX XXXXX - - - XXXXXXXX				
10002CH to 10004BH	GENERAL PURPOSE RAM [R/W]				
10004CH	IDR00 [R/W] XXXXXXXX XXXXXXXX XXXXX - - - XXXXXXXX				
100050H	IDR10 [R/W] XXXXXXXX XXXXXXXX XXXXX - - - XXXXXXXX				
100054H	IDR20 [R/W] XXXXXXXX XXXXXXXX XXXXX - - - XXXXXXXX				
100058H	IDR30 [R/W] XXXXXXXX XXXXXXXX XXXXX - - - XXXXXXXX				
10005CH	IDR40 [R/W] XXXXXXXX XXXXXXXX XXXXX - - - XXXXXXXX				
100060H	IDR50 [R/W] XXXXXXXX XXXXXXXX XXXXX - - - XXXXXXXX				
100064H	IDR60 [R/W] XXXXXXXX XXXXXXXX XXXXX - - - XXXXXXXX				
100068H	IDR70 [R/W] XXXXXXXX XXXXXXXX XXXXX - - - XXXXXXXX				

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Address	Register				Block
	+0	+1	+2	+3	
10006C$_H$	IDR80 [R/W] XXXXXXXX XXXXXXXX XXXXX - - - XXXXXXXX				CAN 0
100070$_H$	IDR90 [R/W] XXXXXXXX XXXXXXXX XXXXX - - - XXXXXXXX				
100074$_H$	IDR100 [R/W] XXXXXXXX XXXXXXXX XXXXX - - - XXXXXXXX				
100078$_H$	IDR110 [R/W] XXXXXXXX XXXXXXXX XXXXX - - - XXXXXXXX				
10007C$_H$	IDR120 [R/W] XXXXXXXX XXXXXXXX XXXXX - - - XXXXXXXX				
100080$_H$	IDR130 [R/W] XXXXXXXX XXXXXXXX XXXXX - - - XXXXXXXX				
100084$_H$	IDR140 [R/W] XXXXXXXX XXXXXXXX XXXXX - - - XXXXXXXX				
100088$_H$	IDR150 [R/W] XXXXXXXX XXXXXXXX XXXXX - - - XXXXXXXX				
10008C$_H$	DLCR00 [R/W] - - - - - - - - - - - - XXXX		DLCR10 [R/W] - - - - - - - - - - - - XXXX		
100090$_H$	DLCR20 [R/W] - - - - - - - - - - - - XXXX		DLCR30 [R/W] - - - - - - - - - - - - XXXX		
100094$_H$	DLCR40 [R/W] - - - - - - - - - - - - XXXX		DLCR50 [R/W] - - - - - - - - - - - - XXXX		
100098$_H$	DLCR60 [R/W] - - - - - - - - - - - - XXXX		DLCR70 [R/W] - - - - - - - - - - - - XXXX		
10009C$_H$	DLCR80 [R/W] - - - - - - - - - - - - XXXX		DLCR90 [R/W] - - - - - - - - - - - - XXXX		
1000A0$_H$	DLCR100 [R/W] - - - - - - - - - - - - XXXX		DLCR110 [R/W] - - - - - - - - - - - - XXXX		
1000A4$_H$	DLCR120 [R/W] - - - - - - - - - - - - XXXX		DLCR130 [R/W] - - - - - - - - - - - - XXXX		
1000A8$_H$	DLCR140 [R/W] - - - - - - - - - - - - XXXX		DLCR150 [R/W] - - - - - - - - - - - - XXXX		
1000AC$_H$	DTR00 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1000B4$_H$	DTR10 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1000BC$_H$	DTR20 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

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Address	Register				Block
	+0	+1	+2	+3	
1000C4H	DTR30 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				CAN 0
1000CCH	DTR40 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1000D4H	DTR50 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1000DCH	DTR60 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1000E4H	DTR70 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1000ECH	DTR80 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1000F4H	DTR90 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1000FCH	DTR100 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
100104H	DTR110 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
10010CH	DTR120 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
100114H	DTR130 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
10011CH	DTR140 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
100124H	DTR150 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
10012CH	CREG0 [R/W] 00000000 00000110		—		

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Address	Register				Block
	+0	+1	+2	+3	
100180H	FMCS [R/W] 1 - - 0X000	----------			Flash Memory control for F361GA
100200H	BVALR1 [R/W] 00000000 00000000		TREQR1 [R/W] 00000000 00000000		CAN 1 Remark : Address range for CAN 0 to CAN 3 depends on chip select range. Mentioned addresses are default values, determined by boot ROM contents.
100204H	TCANR1 [W] 00000000 00000000		TCR1 [R/W] 00000000 00000000		
100208H	RCR1 [R/W] 00000000 00000000		RRTRR1 [R/W] 00000000 00000000		
10020CH	ROVRR1 [R/W] 00000000 00000000		RIER1 [R/W] 00000000 00000000		
100210H	CSR1 [R/W] 00000000 00000001		—	LEIR1 [R/W] 000-0000	
100214H	RTEC1 [R] 00000000 00000000		BTR1 [R/W] -1111111 11111111		
100218H	IDER1 [R/W] XXXXXXXX XXXXXXXX		TRTRR1 [R/W] 00000000 00000000		
10021CH	RFWTR1 [R/W] XXXXXXXX XXXXXXXX		TIER1 [R/W] 00000000 00000000		
100220H	AMSR1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
100224H	AMR01 [R/W] XXXXXXXX XXXXXXXX XXXXX - - - XXXXXXXX				
100228H	AMR11 [R/W] XXXXXXXX XXXXXXXX XXXXX - - - XXXXXXXX				
10022CH to 100248H	GENERAL PURPOSE RAM [R/W]				
10024CH	IDR01 [R/W] XXXXXXXX XXXXXXXX XXXXX - - - XXXXXXXX				
100250H	IDR11 [R/W] XXXXXXXX XXXXXXXX XXXXX - - - XXXXXXXX				
100254H	IDR21[R/W] XXXXXXXX XXXXXXXX XXXXX - - - XXXXXXXX				
100258H	IDR31 [R/W] XXXXXXXX XXXXXXXX XXXXX - - - XXXXXXXX-				
10025CH	IDR41 [R/W] XXXXXXXX XXXXXXXX XXXXX - - - XXXXXXXX				
100260H	IDR51 [R/W] XXXXXXXX XXXXXXXX XXXXX - - - XXXXXXXX				

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Address	Register				Block
	+0	+1	+2	+3	
100264H	IDR61 [R/W] XXXXXXXX XXXXXXXX XXXXX - - - XXXXXXXX				CAN 1
100268H	IDR71 [R/W] XXXXXXXX XXXXXXXX XXXXX - - - XXXXXXXX				
10026CH	IDR81 [R/W] XXXXXXXX XXXXXXXX XXXXX - - - XXXXXXXX				
100270H	IDR91 [R/W] XXXXXXXX XXXXXXXX XXXXX - - - XXXXXXXX				
100274H	IDR101 [R/W] XXXXXXXX XXXXXXXX XXXXX - - - XXXXXXXX				
100278H	IDR111 [R/W] XXXXXXXX XXXXXXXX XXXXX - - - XXXXXXXX				
10027CH	IDR121 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXX - - -				
100280H	IDR131 [R/W] XXXXXXXX XXXXXXXX XXXXX - - - XXXXXXXX				
100284H	IDR141 [R/W] XXXXXXXX XXXXXXXX XXXXX - - - XXXXXXXX				
100288H	IDR151 [R/W] XXXXXXXX XXXXXXXX XXXXX - - - XXXXXXXX				
10028CH	DLCR01 [R/W] - - - - - - - - - - - - XXXX		DLCR11 [R/W] - - - - - - - - - - - - XXXX		
100290H	DLCR21 [R/W] - - - - - - - - - - - - XXXX		DLCR31 [R/W] - - - - - - - - - - - - XXXX		
100294H	DLCR41 [R/W] - - - - - - - - - - - - XXXX		DLCR51 [R/W] - - - - - - - - - - - - XXXX		
100298H	DLCR61 [R/W] - - - - - - - - - - - - XXXX		DLCR71 [R/W] - - - - - - - - - - - - XXXX		
10029CH	DLCR81[R/W] - - - - - - - - - - - - XXXX		DLCR91 [R/W] - - - - - - - - - - - - XXXX		
1002A0H	DLCR101 [R/W] - - - - - - - - - - - - XXXX		DLCR111 [R/W] - - - - - - - - - - - - XXXX		
1002A4H	DLCR121 [R/W] - - - - - - - - - - - - XXXX		DLCR131 [R/W] - - - - - - - - - - - - XXXX		
1002A8H	DLCR141 [R/W] - - - - - - - - - - - - XXXX		DLCR151 [R/W] - - - - - - - - - - - - XXXX		
1002ACH	DTR01 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

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Address	Register				Block
	+0	+1	+2	+3	
1002B4H	DTR11 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				CAN 1
1002BCH	DTR21 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1002C4H	DTR31 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1002CCH	DTR41 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1002D4H	DTR51 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1002DCH	DTR61 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1002E4H	DTR71 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1002ECH	DTR81 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1002F4H	DTR91 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1002FCH	DTR101 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
100304H	DTR111 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
10030CH	DTR121 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
100314H	DTR131 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
10031CH	DTR141 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

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Address	Register				Block
	+0	+1	+2	+3	
100324H	DTR151 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				CAN 1
10032CH	CREG1 [R/W] 00000000 00000110		—		
100400H	BVALR2 [R/W] 00000000 00000000		TREQR2 [R/W] 00000000 00000000		CAN 2 Remark : Address range for CAN 0 to CAN 3 depends on chip select range. Mentioned addresses are default values, determined by boot ROM contents.
100404H	TCANR2 [W] 00000000 00000000		TCR2 [R/W] 00000000 00000000		
100408H	RCR2 [R/W] 00000000 00000000		RRTRR1 [R/W] 00000000 00000000		
10040CH	ROVRR2 [R/W] 00000000 00000000		RIER2 [R/W] 00000000 00000000		
100410H	CSR2 [R/W] 00000000 00000001		—	LEIR2 [R/W] 000-0000	
100414H	RTEC2 [R] 00000000 00000000		BTR2 [R/W] -1111111 11111111		
100418H	IDER2 [R/W] XXXXXXXX XXXXXXXX		TRTRR2 [R/W] 00000000 00000000		
10041CH	RFWTR2 [R/W] XXXXXXXX XXXXXXXX		TIER2 [R/W] 00000000 00000000		
100420H	AMSR2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
100424H	AMR02 [R/W] XXXXXXXX XXXXXXXX XXXXX - - - XXXXXXXX				
100428H	AMR12 [R/W] XXXXXXXX XXXXXXXX XXXXX - - - XXXXXXXX				
10042CH to 100448H	GENERAL PURPOSE RAM [R/W]				
10044CH	IDR02 [R/W] XXXXXXXX XXXXXXXX XXXXX - - - XXXXXXXX				
100450H	IDR12 [R/W] XXXXXXXX XXXXXXXX XXXXX - - - XXXXXXXX				
100454H	IDR22[R/W] XXXXXXXX XXXXXXXX XXXXX - - - XXXXXXXX				
100458H	IDR32 [R/W] XXXXXXXX XXXXXXXX XXXXX - - - XXXXXXXX-				
10045CH	IDR42 [R/W] XXXXXXXX XXXXXXXX XXXXX - - - XXXXXXXX				

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Address	Register				Block
	+0	+1	+2	+3	
100460H	IDR52 [R/W] XXXXXXXX XXXXXXXX XXXXX - - - XXXXXXXX				CAN 2
100464H	IDR62 [R/W] XXXXXXXX XXXXXXXX XXXXX - - - XXXXXXXX				
100468H	IDR72 [R/W] XXXXXXXX XXXXXXXX XXXXX - - - XXXXXXXX				
10046CH	IDR82 [R/W] XXXXXXXX XXXXXXXX XXXXX - - - XXXXXXXX				
100470H	IDR92 [R/W] XXXXXXXX XXXXXXXX XXXXX - - - XXXXXXXX				
100474H	IDR102 [R/W] XXXXXXXX XXXXXXXX XXXXX - - - XXXXXXXX				
100478H	IDR112 [R/W] XXXXXXXX XXXXXXXX XXXXX - - - XXXXXXXX				
10047CH	IDR122 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXX - - -				
100480H	IDR132 [R/W] XXXXXXXX XXXXXXXX XXXXX - - - XXXXXXXX				
100484H	IDR142 [R/W] XXXXXXXX XXXXXXXX XXXXX - - - XXXXXXXX				
100488H	IDR152 [R/W] XXXXXXXX XXXXXXXX XXXXX - - - XXXXXXXX				
10048CH	DLCR02 [R/W] - - - - - - - - - - - - XXXX		DLCR12 [R/W] - - - - - - - - - - - - XXXX		
100490H	DLCR22 [R/W] - - - - - - - - - - - - XXXX		DLCR32 [R/W] - - - - - - - - - - - - XXXX		
100494H	DLCR42 [R/W] - - - - - - - - - - - - XXXX		DLCR52 [R/W] - - - - - - - - - - - - XXXX		
100498H	DLCR62 [R/W] - - - - - - - - - - - - XXXX		DLCR72 [R/W] - - - - - - - - - - - - XXXX		
10049CH	DLCR82[R/W] - - - - - - - - - - - - XXXX		DLCR92 [R/W] - - - - - - - - - - - - XXXX		
1004A0H	DLCR102 [R/W] - - - - - - - - - - - - XXXX		DLCR112 [R/W] - - - - - - - - - - - - XXXX		
1004A4H	DLCR122 [R/W] - - - - - - - - - - - - XXXX		DLCR132 [R/W] - - - - - - - - - - - - XXXX		
1004A8H	DLCR142 [R/W] - - - - - - - - - - - - XXXX		DLCR152 [R/W] - - - - - - - - - - - - XXXX		
1004ACH	DTR02 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

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Address	Register				Block
	+0	+1	+2	+3	
1004AC$_H$	DTR02 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				CAN 2
1004B4$_H$	DTR12 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1004BC$_H$	DTR22 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1004C4$_H$	DTR32 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1004CC$_H$	DTR42 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1004D4$_H$	DTR52 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1004DC$_H$	DTR62 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1004E4$_H$	DTR72 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1004EC$_H$	DTR82 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1004F4$_H$	DTR92 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1004FC$_H$	DTR102 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
100504$_H$	DTR112 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
10050C$_H$	DTR122 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
100514$_H$	DTR132 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

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Address	Register				Block
	+0	+1	+2	+3	
10051C$_H$	DTR142 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				CAN 2
100524$_H$	DTR152 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
10052C$_H$	CREG2 [R/W] 00000000 00000110		—		
100600$_H$	BVALR3 [R/W] 00000000 00000000		TREQR3 [R/W] 00000000 00000000		CAN 3 Remark : Address range for CAN 0 to CAN 3 depends on chip select range. Mentioned addresses are default values, determined by boot ROM contents.
100604$_H$	TCANR3 [W] 00000000 00000000		TCR3 [R/W] 00000000 00000000		
100608$_H$	RCR3 [R/W] 00000000 00000000		RRTRR31 [R/W] 00000000 00000000		
10060C$_H$	ROVRR3 [R/W] 00000000 00000000		RIER3 [R/W] 00000000 00000000		
100610$_H$	CSR3 [R/W] 00000000 00000001		—	LEIR3 [R/W] 000-0000	
100614$_H$	RTEC3 [R] 00000000 00000000		BTR3 [R/W] -1111111 11111111		
100618$_H$	IDER3 [R/W] XXXXXXXX XXXXXXXX		TRTRR3 [R/W] 00000000 00000000		
10061C$_H$	RFWTR3 [R/W] XXXXXXXX XXXXXXXX		TIER3 [R/W] 00000000 00000000		
100620$_H$	AMSR3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
100624$_H$	AMR03 [R/W] XXXXXXXX XXXXXXXX XXXXX - - - XXXXXXXX				
100628$_H$	AMR13 [R/W] XXXXXXXX XXXXXXXX XXXXX - - - XXXXXXXX				
10062C$_H$ to 100648$_H$	GENERAL PURPOSE RAM [R/W]				
10064C$_H$	IDR03 [R/W] XXXXXXXX XXXXXXXX XXXXX - - - XXXXXXXX				
100650$_H$	IDR13 [R/W] XXXXXXXX XXXXXXXX XXXXX - - - XXXXXXXX				
100654$_H$	IDR23[R/W] XXXXXXXX XXXXXXXX XXXXX - - - XXXXXXXX				
100658$_H$	IDR33 [R/W] XXXXXXXX XXXXXXXX XXXXX - - - XXXXXXXX-				

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Address	Register				Block
	+0	+1	+2	+3	
10065CH	IDR43 [R/W] XXXXXXXX XXXXXXXX XXXXX - - - XXXXXXXX				CAN 3
100660H	IDR53 [R/W] XXXXXXXX XXXXXXXX XXXXX - - - XXXXXXXX				
100664H	IDR63 [R/W] XXXXXXXX XXXXXXXX XXXXX - - - XXXXXXXX				
100668H	IDR73 [R/W] XXXXXXXX XXXXXXXX XXXXX - - - XXXXXXXX				
10066CH	IDR83 [R/W] XXXXXXXX XXXXXXXX XXXXX - - - XXXXXXXX				
100670H	IDR93 [R/W] XXXXXXXX XXXXXXXX XXXXX - - - XXXXXXXX				
100674H	IDR103 [R/W] XXXXXXXX XXXXXXXX XXXXX - - - XXXXXXXX				
100678H	IDR113 [R/W] XXXXXXXX XXXXXXXX XXXXX - - - XXXXXXXX				
10067CH	IDR123 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXX - - -				
100680H	IDR133 [R/W] XXXXXXXX XXXXXXXX XXXXX - - - XXXXXXXX				
100684H	IDR143 [R/W] XXXXXXXX XXXXXXXX XXXXX - - - XXXXXXXX				
100688H	IDR153 [R/W] XXXXXXXX XXXXXXXX XXXXX - - - XXXXXXXX				
10068CH	DLCR032 [R/W] - - - - - - - - - - - - XXXX		DLCR13 [R/W] - - - - - - - - - - - - XXXX		
100690H	DLCR232 [R/W] - - - - - - - - - - - - XXXX		DLCR33 [R/W] - - - - - - - - - - - - XXXX		
100694H	DLCR43 [R/W] - - - - - - - - - - - - XXXX		DLCR53 [R/W] - - - - - - - - - - - - XXXX		
100698H	DLCR63 [R/W] - - - - - - - - - - - - XXXX		DLCR733 [R/W] - - - - - - - - - - - - XXXX		
10069CH	DLCR83[R/W] - - - - - - - - - - - - XXXX		DLCR93 [R/W] - - - - - - - - - - - - XXXX		
1006A0H	DLCR103 [R/W] - - - - - - - - - - - - XXXX		DLCR113 [R/W] - - - - - - - - - - - - XXXX		
1006A4H	DLCR123 [R/W] - - - - - - - - - - - - XXXX		DLCR133 [R/W] - - - - - - - - - - - - XXXX		
1006A8H	DLCR143 [R/W] - - - - - - - - - - - - XXXX		DLCR153 [R/W] - - - - - - - - - - - - XXXX		

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Address	Register				Block
	+0	+1	+2	+3	
1006AC$_H$	DTR03 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				CAN 3
1006B4$_H$	DTR13 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1006BC$_H$	DTR23 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1006C4$_H$	DTR33 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1006CC$_H$	DTR43 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1006D4$_H$	DTR53 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1006DC$_H$	DTR63 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1006E4$_H$	DTR73 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1006EC$_H$	DTR83 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1006F4$_H$	DTR93 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1006FC$_H$	DTR103 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
100704$_H$	DTR113 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
10070C$_H$	DTR123 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
100714$_H$	DTR133 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

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Address	Register				Block
	+0	+1	+2	+3	
10071C$_H$	DTR143 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				CAN 3
100724$_H$	DTR153 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
10072C$_H$	CREG3 [R/W] 00000000 00000110		—		
180000$_H$ to 19FFFC$_H$	Sector 0 64 KB		Sector 7 64 KB		Flash Memory 512 K on F361GA - addresses depending on settings for ship select area $\overline{CS1}$
1A0000$_H$ to 1BFFFC	Sector 1 64 KB		Sector 8 64 KB		
1C0000$_H$ to 1DFFFC	Sector 2 64 KB		Sector 9 64 KB		
1E0000$_H$ to 1 EFFFC$_H$	Sector 3 32 KB		Sector 10 32 KB		
1F0000$_H$ to 1F3FFC$_H$	Sector 4 8 KB		Sector 11 8 KB		
1F4000$_H$ to 1F7FFC$_H$	Sector 5 8 KB		Sector 12 8 KB		
1F8000$_H$ to 1FFFFC$_H$	Sector 6 16 KB		Sector 13 16 KB		

Note: The data in reserved areas and areas marked “—” is indeterminate. Do not use those areas!

■ INTERRUPT CAUSES, INTERRUPT VECTORS, AND INTERRUPT CONTROL REGISTER

Interrupt	Interrupt number		Interrupt level *1		Interrupt vector *2		RN
	Decimal	Hexa-decimal	Setting Register	Register address	Offset	Default Vector address	
Reset	0	00	—	—	0x3FC	0x000FFFFC	—
Mode vector	1	01	—	—	0x3F8	0x000FFFF8	—
System reserved	2	02	—	—	0x3F4	0x000FFFF4	—
System reserved	3	03	—	—	0x3F0	0x000FFFF0	—
System reserved	4	04	—	—	0x3EC	0x000FFFEC	—
System reserved	5	05	—	—	0x3E8	0x000FFFE8	—
System reserved	6	06	—	—	0x3E4	0x000FFFE4	—
Co-processor fault trap *4	7	07	—	—	0x3E0	0x000FFFE0	—
Co-processor error trap *4	8	08	—	—	0x3DC	0x000FFFDC	—
INTE instruction *4	9	09	—	—	0x3D8	0x000FFFD8	—
Instruction break exception *4	10	0A	—	—	0x3D4	0x000FFFD4	—
Operand break trap *4	11	0B	—	—	0x3D0	0x000FFFD0	—
Step trace trap *4	12	0C	—	—	0x3CC	0x000FFFCC	—
NMI interrupt (tool) *4	13	0D	—	—	0x3C8	0x000FFFC8	—
Undefined instruction exception	14	0E	—	—	0x3C4	0x000FFFC4	—
NMI request	15	0F	F_H fixed		0x3C0	0x000FFFC0	—
External Interrupt 0	16	10	ICR00	0x440	0x3BC	0x000FFFBC	4
External Interrupt 1	17	11	ICR01	0x441	0x3B8	0x000FFFB8	5
External Interrupt 2	18	12	ICR02	0x442	0x3B4	0x000FFFB4	8
External Interrupt 3	19	13	ICR03	0x443	0x3B0	0x000FFFB0	9
External Interrupt 4	20	14	ICR04	0x444	0x3AC	0x000FFFAC	—
External Interrupt 5	21	15	ICR05	0x445	0x3A8	0x000FFFA8	—
External Interrupt 6	22	16	ICR06	0x446	0x3A4	0x000FFFA4	—
External Interrupt 7	23	17	ICR07	0x447	0x3A0	0x000FFFA0	—
Reload Timer 0	24	18	ICR08	0x448	0x39C	0x000FFF9C	6
Reload Timer 1	25	19	ICR09	0x449	0x398	0x000FFF98	7
Reload Timer 2	26	1A	ICR10	0x44A	0x394	0x000FFF94	—
CAN 0 RX	27	1B	ICR11	0x44B	0x390	0x000FFF90	—
CAN 0 TX/NS	28	1C	ICR12	0x44C	0x38C	0x000FFF8C	—
CAN 1 RX	29	1D	ICR13	0x44D	0x388	0x000FFF88	—
CAN 1 TX/NS	30	1E	ICR14	0x44E	0x384	0x000FFF84	—

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Interrupt	Interrupt number		Interrupt level *1		Interrupt vector *2		RN
	Decimal	Hexa-decimal	Setting Register	Register address	Offset	Default Vector address	
CAN 2 RX	31	1F	ICR15	0x44F	0x380	0x000FFF80	—
CAN 2 TX/NS	32	20	ICR16	0x450	0x37C	0x000FFF7C	—
CAN 3 RX *5	33	21	ICR17	0x451	0x378	0x000FFF78	—
CAN 3 TX/NS *5	34	22	ICR18	0x452	0x374	0x000FFF74	—
PPG 0/1	35	23	ICR19	0x453	0x370	0x000FFF70	—
PPG 2/3	36	24	ICR20	0x454	0x36C	0x000FFF6C	—
PPG 4/5	37	25	ICR21	0x455	0x368	0x000FFF68	—
PPG 6/7	38	26	ICR22	0x456	0x364	0x000FFF64	—
Reload Timer 3	39	27	ICR23	0x457	0x360	0x000FFF60	—
Reload Timer 4	40	28	ICR24	0x458	0x35C	0x000FFF5C	—
Reload Timer 5	41	29	ICR25	0x459	0x358	0x000FFF58	—
ICU 0/1	42	2A	ICR26	0x45A	0x354	0x000FFF54	—
OCU 0/1	43	2B	ICR27	0x45B	0x350	0x000FFF50	—
ICU 2/3	44	2C	ICR28	0x45C	0x34C	0x000FFF4C	—
OCU 2/3	45	2D	ICR29	0x45D	0x348	0x000FFF48	—
ADC	46	2E	ICR30	0x45E	0x344	0x000FFF44	14
Timebase Overflow	47	2F	ICR31	0x45F	0x340	0x000FFF40	—
Free Running Counter 0	48	30	ICR32	0x460	0x33C	0x000FFF3C	—
Free Running Counter 1	49	31	ICR33	0x461	0x338	0x000FFF38	—
SIO 0 *6	50	32	ICR34	0x462	0x334	0x000FFF34	(12)
SIO 1 *6	51	33	ICR35	0x463	0x330	0x000FFF30	(15)
Sound Generator	52	34	ICR36	0x464	0x32C	0x000FFF2C	—
UART 0 RX	53	35	ICR37	0x465	0x328	0x000FFF28	0
UART 0 TX	54	36	ICR38	0x466	0x324	0x000FFF24	1
UART 1 RX	55	37	ICR39	0x467	0x320	0x000FFF20	2
UART 1 TX	56	38	ICR40	0x468	0x31C	0x000FFF1C	3
UART 2 RX	57	39	ICR41	0x469	0x318	0x000FFF18	10
UART 2 TX	58	3A	ICR42	0x46A	0x314	0x000FFF14	11
I^2C	59	3B	ICR43	0x46B	0x310	0x000FFF10	13
Alarm Comparator	60	3C	ICR44	0x46C	0x30C	0x000FFF0C	—
RTC (Watchtimer) / Calibration Unit	61	3D	ICR45	0x46D	0x308	0x000FFF08	—
DMA	62	3E	ICR46	0x46E	0x304	0x000FFF04	—

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Interrupt	Interrupt number		Interrupt level *1		Interrupt vector *2		RN
	Decimal	Hexa-decimal	Setting Register	Register address	Offset	Default Vector address	
Delayed interrupt activation bit	63	3F	ICR47	0x46F	0x300	0x000FFF00	— —
System reserved *3	64	40	—	—	0x2FC	0x000FFEFC	—
System reserved *3	65	41	—	—	0x2F8	0x000FFEF8	—
Security vector	66	42	—	—	0x2F4	0x000FFEF4	—
System reserved	67	43	(ICR51)	0x473	0x2F0	0x000FFEF0	—
System reserved	68	44	(ICR52)	0x474	0x2EC	0x000FFEEC	—
System reserved	69	45	(ICR53)	0x475	0x2E8	0x000FFEE8	—
System reserved	70	46	(ICR54)	0x476	0x2E4	0x000FFEE4	—
System reserved	71	47	(ICR55)	0x477	0x2E0	0x000FFEE0	—
System reserved	72	48	(ICR56)	0x478	0x2DC	0x000FFEDC	—
System reserved	73	49	(ICR57)	0x479	0x2D8	0x000FFED8	—
System reserved	74	4A	(ICR58)	0x47A	0x2D4	0x000FFED4	—
System reserved	75	4B	(ICR59)	0x47B	0x2D0	0x000FFED0	—
System reserved	76	4C	(ICR60)	0x47C	0x2CC	0x000FFECC	—
System reserved	77	4D	(ICR61)	0x47D	0x2C8	0x000FFEC8	—
System reserved	78	4E	(ICR62)	0x47E	0x2C4	0x000FFEC4	—
System reserved	79	4F	(ICR63)	0x47F	0x2C0	0x000FFEC0	—
Used by the INT instruction.	80 to 255	50 to FF	—	—	0x2BC to 0x000	0x000FFEBC to 0x000FFC00	— — —

*1 : The ICRs are located in the interrupt controller and set the interrupt level for each interrupt request. An ICR is provided for each interrupt request.

*2 : The vector address for each EIT (exception, interrupt or trap) is calculated by adding the listed offset to the table base register value (TBR) . The TBR specifies the top of the EIT vector table. The addresses listed in the table are for the default TBR value (0x000FFC00) . The TBR is initialized to this value by a reset.After execution of the internal boot ROM TBR is set to 0x00FFC00.

*3 : Used by REALOS

*4 : System reserved

*5 : Only available on MB91FV360GA

*6 : DMA to/from SIO is not yet implemented.

■ PERIPHERAL RESOURCES

1. INSTRUCTION CACHE

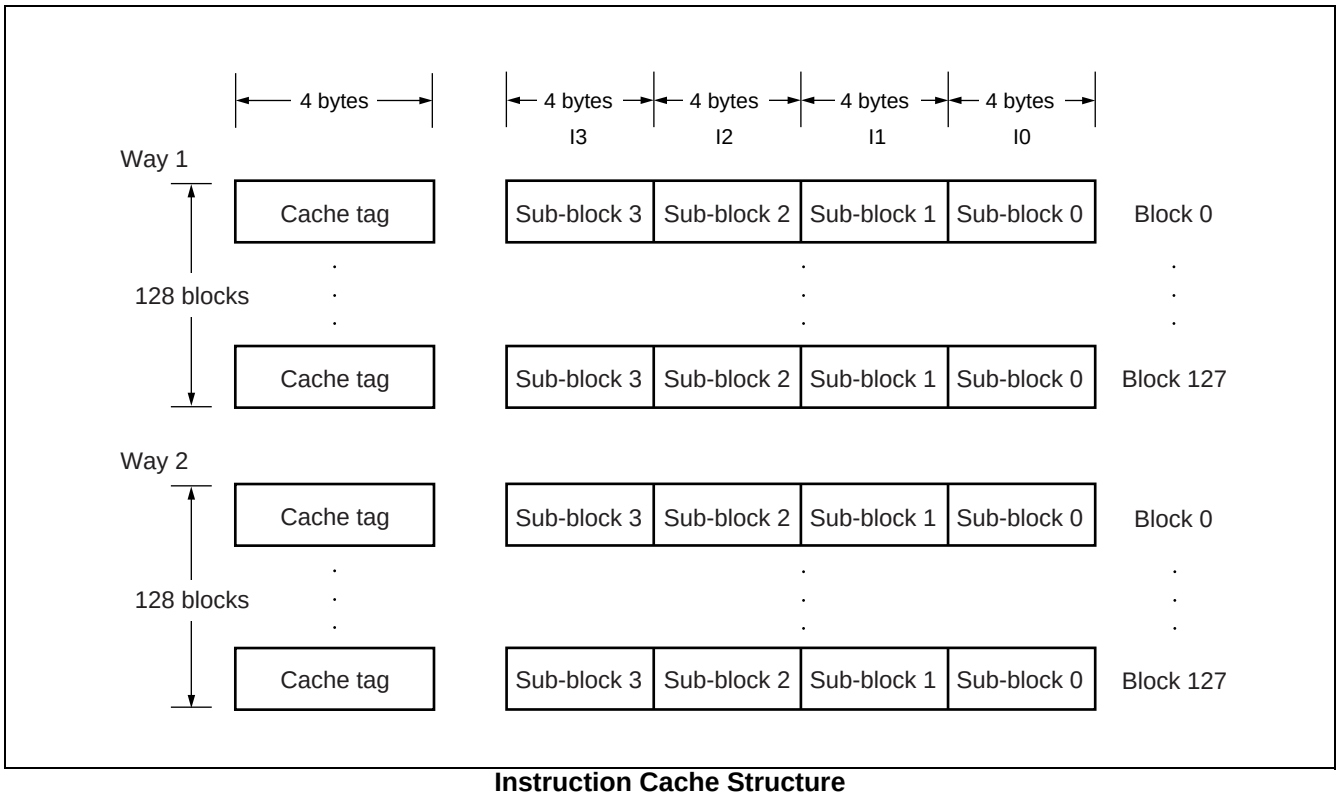
This section describes the instruction cache memory included in FR50 Family members and it operation. This only applies to MB91FV360GA and MB91F361GA.

(1) General Description

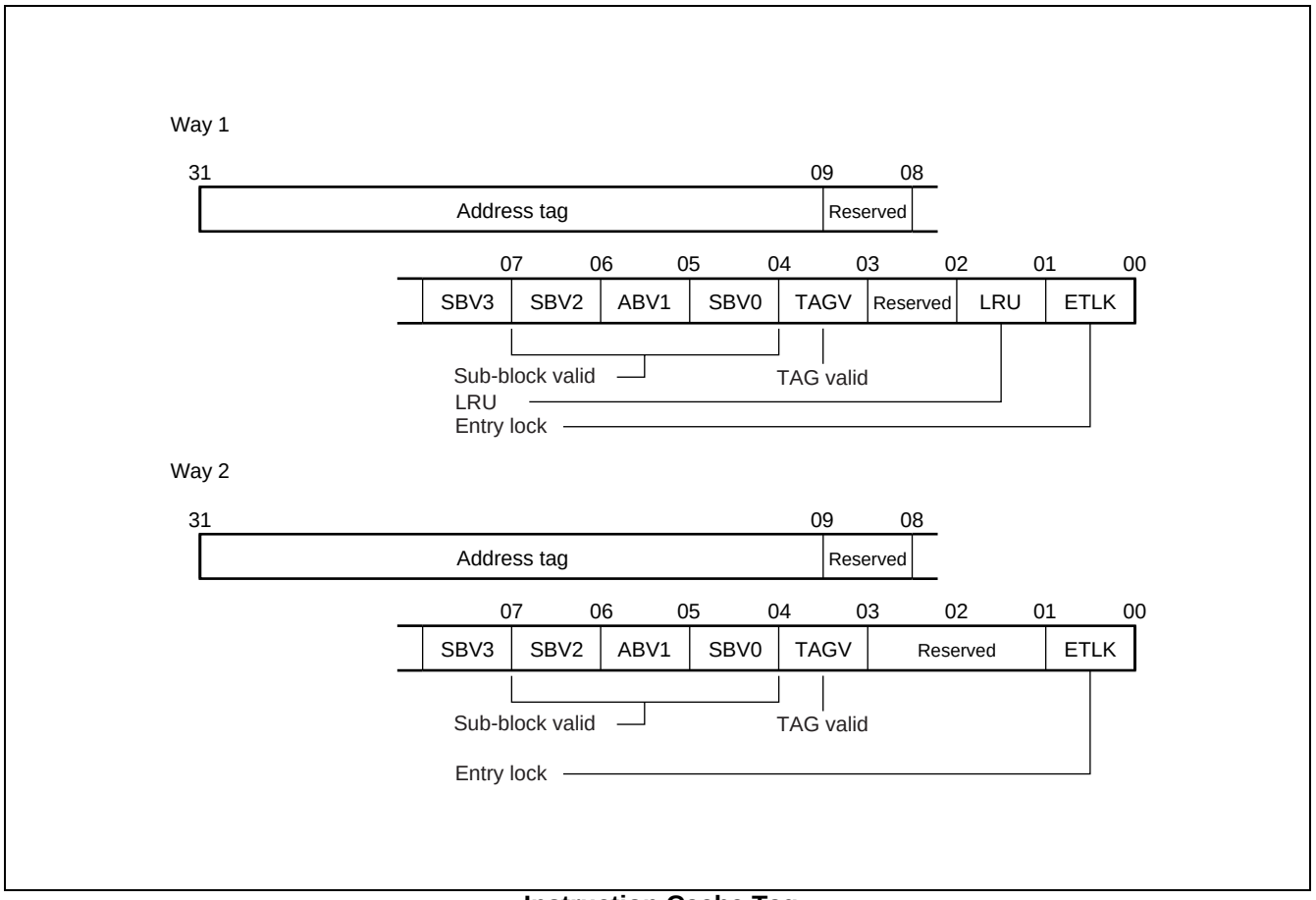
The instruction cache is temporary memory. When an external low-speed memory accesses an instruction code, the instruction cache stores the single-accessed code to increase the second and subsequent access speeds.Setting this memory to the RAM mode enables software to directly read and write instruction cache data RAM and tag RAM.

(2) Main Body Structure

- FR basic instruction length : 2 bytes
- Block arrangement system : 2-way set associative system
- Block
  One way consists of 128 blocks.
  One block consists of 16 bytes (= 4 sub-blocks) .
  One sub-block consists of 4 bytes (= 1 bus access unit) .



Instruction Cache Structure



Instruction Cache Tag

(3) Control Register Structure

IRBS (32 bits)
Address : 00000300H

31	30	29	28	27	26	25	24	Initial value
0	0	0	0	0	0	0	0	00000000B
R	R	R	R	R	R	R	R	

23	22	21	20	19	18	17	16	Initial value
0	0	0	0	0	0	0	1	00000001B
R	R	R	R	R	R	R	R	ICR26

Address : 00000302H

15	14	13	12	11	10	9	8	Initial value
IRBS	IRBS	IRBS	IRBS	—	—	—	—	0010 - - - -B
R/W	R/W	R/W	R/W	—	—	—	—	

7	6	5	4	3	2	1	0	Initial value
—	—	—	—	—	—	—	—	- - - - - - - - B
—	—	—	—	—	—	—	—	

IRBS [bits 15 to 12] These bits are used to set the base address of cache RAM at access in the RAM mode. Align cache RAM in units of 4 K bytes. These bits are initialized by INIT. The initial value is the 00012000H address.

ISIZE (8 bits)

00000307H

7	6	5	4	3	2	1	0	Initial value
—	—	—	—	—	—	SIZE1	SIZE0	- - - - - - 11B
—	—	—	—	—	—	R/W	R/W	

The ICHCR (I-CacHe Control Register) controls the instruction cache operations.
Writing to the ICHCR does not affect caching of instructions fetched within three subsequent cycles.

ICHCR (8 bits)

000003E7H

7	6	5	4	3	2	1	0	Initial value
RAM	—	GBLK	ALFL	EOLK	ELKR	FLSH	ENAB	0 - 000000B
R/W	—	R/W	R/W	R/W	R/W	R/W	R/W	

2. BOOT ROM

The Boot ROM is a fixed start-up routine which is located at FF000 (Reset entry) and will therefore be executed after every RST or INIT. The purpose of this ROM is to configure the device after a reset and to provide a simple serial bootloader for programming the embedded Flash memories.

The Boot ROM contains three logical parts :

(1) Chip Initializations

Immediately after each reset, the following settings will be made :

CS0 : 200000…2FFFFF, 32 Bit Bus, 1 wait-state (default external access)

CS1 : 180000…1FFFFF, 32 Bit Bus, 1 wait-state (Flash Area only on F361GA)

CS7 : 100000…10FFFF, 16 Bit Bus, 1 wait-state (CAN)

In addition, the Table-Base Register will be initialized to 1FFC00 (F361GA only) and the synchronous reset (see TBCR) will be enabled.

(2) Check for Bootcondition

After the chip initialization, the “Security-Vector” will be checked (Vector #66) . The purpose of this feature is to disable the bootstraploader due to security reasons.

The RSRR (reset cause register) will be read and saved. If no power-on reset (external $\overline{\text{INIT}}$ input, RSRR = 0x80) is indicated, a branch to the user application will be initiated (Branch to 1F4000) .

If $\overline{\text{INIT}}$ was detected and the “Security-Vector” check okay, the following conditions must be met in order to start the Bootstraploader :

Within a certain time, the start-up character “V” must be received via UART0 (9600, 8N1) . The time-out is set to 200 ms.

(3) Bootstraploader

If the Bootcondition was met, an acknowledge character “F” will be transmitted via UART0 to indicate that the Bootloader is ready to accept commands. 4 different commands are possible :

Receive and write to a specified memory block
Dump the contents of a specified memory block
Initiate a “CALL” to a certain location
Re-dump a calculated checksum for verification

(4) Configuration Register (Mode Register F362MD)

This register is used to control which pins of the external bus interface are active, where the pins for the external DMA channel are located and which I^2C module is used.

address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
000001FE$_H$	—	ASYMCLKT	HIZ_D_A	HIZ_ECLK	HIZ_D_23_16	HIZ_D_15_0	DMASWP	IICSEL
access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value		0	0	0	0	0	0	0

3. CLOCK MODULATOR

An important property of MCUs and other electronic devices is their electromagnetic compatibility - EMC. Besides a low susceptibility against external interferences, a low radiated emission is desired to avoid interference of adjacent devices.

Particularly the system clock and derived signals such as data- and address busses contribute significantly to the radiated emission. The purpose of the clock modulator is to spread the energy of these signals over a wide range of frequencies and thus reducing the amplitudes of the fundamental and harmonic frequencies.

With the use of an advanced frequency modulation algorithm, the Fujitsu built in clock modulator can achieve an attenuation of up to 20-25 dB compared to non modulated clock operation. Since the modulator is highly configurable, it can be optimally adjusted to the actual application in order to achieve minimal electromagnetic interference.

By default, the modulator is disabled and the MCU is running with unmodulated clock.

If you plan to use this feature, please contact Fujitsu.

4. I/O PORTS

There are 3 types of I/O port register structure; port data register (PDR7 to PDR5) , data direction register (DDR7 to DDR5) , and portfunction registers (PFR7 to PRF5) , where bits PDR7 to PDR5, bits DDR7 to DDR5, and bits PFR7 to PRF5 correspond respectively. Each bit on the register corresponds to an external pin. The PFR settings define whether a pin is used as a functional I/O (e.g. UART output) or as general purpose pin.

- For input (DDR = “0”) setting;
  PDR reading operation : reads level of corresponding external pin.
  PDR writing operation : writes set value to PDR.

- For output (DDR = “1”) setting;
  PDR reading operation : reads PDR value.
  PDR writing operation : outputs PDR value to corresponding external pin.

(1) Register configuration

Port Data Register

		bit 7	bit 0	Initial value	Access
Address :	00000007H	PDR7		111XXXXXB	R/W
	00000008H	PDR8		XXXXXXXXB	R/W
	00000009H	PDR9		XXXXXXX1B	R/W
	0000000BH	PDRB		XXXXXXXXB	R/W
	00000010H	PDRG		XXXXXXXXB	R/W
	00000011H	PDRH		XXXXXXXXB	R/W
	00000012H	PDRI		X - - - X - - -B	R/W
	00000013H	PDRJ		XXXXXXXXB	R/W
	00000014H	PDRK		XXXXXXXXB	R/W
	00000015H	PDRL		XXXXXXXXB	R/W
	00000016H	PDRM		- - - - XXXXB	R/W
	00000017H	PDRN		- -XXXXXXB	R/W
	00000018H	PDRO		XXXXXXXXB	R/W
	00000019H	PDRP		XXXXXXXXB	R/W
	0000001AH	PDRQ		--XXXXXXB	R/W
	0000001BH	PDRR		XXXXXXXXB	R/W
	0000001CH	PDRS		XXXXXXXXB	R/W

Data directon Register

		bit 7	bit 0	Initial value	Access
Address :	00000607H	DDR7		00000000B	R/W
	00000608H	DDR8		00000000B	R/W
	00000609H	DDR9		00000000B	R/W
	0000060BH	DDRB		00000000B	R/W
	00000400H	DDRG		00000000B	R/W
	00000401H	DDRH		00000000B	R/W
	00000402H	DDRI		- - - - 0 - - -B	R/W
	00000403H	DDRJ		00000000B	R/W
	00000404H	DDRK		00000000B	R/W
	00000405H	DDRL		00000000B	R/W
	00000406H	DDRM		- - - - 0000B	R/W
	00000407H	DDRN		- - 000000B	R/W
	00000408H	DDRO		00000000B	R/W
	00000409H	DDRP		00000000B	R/W
	0000040AH	DDRQ		- - 000000B	R/W
	0000040BH	DDRR		00000000B	R/W
	0000040CH	DDRS		00000000B	R/W

Port function registers (PFR)

	7	6	5	4	3	2	1	0	Initial value	Access
PFR7 Address : 00000617H	P77	P76	P75	P74	P73	P72	P71	P70	00001111B	R/W
PFR8 Address : 00000618H	P87	P86	P85	P84	P83	P82	—	—	111110 - -B	R/W
PFR9 Address : 00000619H	P97	P96	P95	P94	P93	P92	P91	P90	11110101B	R/W
PFRB Address : 0000061BH	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	00000000B	R/W
PFR27 Address : 00000627H	P277	P276	P275	P274	P273	P272	P271	P270	1111 - 00 -B	R/W
PFRG Address : 00000410H	PG7	PG6	PG5	PG4	PG3	PG2	PG1	PG0	00000000B	R/W
PFRH Address : 00000411H	PH7	PH6	PH5	PH4	PH3	PH2	PH1	PH0	00000000B	R/W
PFRI Address : 00000412H	—	—	—	—	PI3	—	—	—	- - - - 0 - - -B	R/W
PFRJ Address : 00000413H	PJ7	PJ6	PJ5	PJ4	PJ3	PJ2	PJ1	PJ0	00000000B	R/W
PFRK Address : 00000414H	PK7	PK6	PK5	PK4	PK3	PK2	PK1	PK0	00000000B	R/W
PFRL Address : 00000415H	PL7	PL6	PL5	PL4	PL3	PL2	PL1	PL0	00000000B	R/W
PFRM Address : 00000416H	—	—	—	—	PM3	PM2	PM1	PM0	- - - - 0000B	R/W
PFRN Address : 00000417H	—	—	PN5	PN4	PN3	PN2	PN1	PN0	- - 000000B	R/W

(Continued)

(Continued)

PFRO

Address : 00000418H

7	6	5	4	3	2	1	0	Initial value	Access
PO7	PO6	PO5	PO4	PO3	PO2	PO1	PO0	00000000B	R/W

PFRP

Address : 00000419H

7	6	5	4	3	2	1	0	Initial value	Access
PP7	PP6	PP5	PP4	PP3	PP2	PP1	PP0	00000000B	R/W

PFRQ

Address : 0000041AH

7	6	5	4	3	2	1	0	Initial value	Access
—	—	PQ5	PQ4	PQ3	PQ2	PQ1	PQ0	- - 000000B	R/W

PFRR

Address : 0000041BH

7	6	5	4	3	2	1	0	Initial value	Access
PR7	PR6	PR5	PR4	PR3	PR2	PR1	PR0	00000000B	R/W

PFRS

Address : 0000041CH

7	6	5	4	3	2	1	0	Initial value	Access
PS7	PS6	PS5	PS4	PS3	PS2	PS1	PS0	00000000B	R/W

5. DMA CONTROLLER (DMAC)

The DMAC module is used to implement direct memory access (DMA) transfer in FR50 series devices.

In a DMA transfer controlled by this module, various types of data can be transferred at high speed without involving the CPU, thus increasing system performance.

(1) Hardware Configuration

The following are the main components of the DMAC module :

- Five independent DMA channels
- 5-channel independent access control circuit
- 32-bit address registers (Reload can be specified : Two registers for each channel.)
- 16-bit transfer count registers (Reload can be specified : One register for each channel.)
- 4-bit block count registers (One register for each channel)
- External transfer request input pins DREQ0, DREQ1, and DREQ2 (only channels 0, 1, and 2)
- External transfer request acceptance output pins DACK0, DACK1, and DACK2 (only channels 0, 1, and 2)
- DMA termination output pins DEOP0, DEOP1, and DEOP2 (only channels 0, 1, and 2)
- Two-cycle transfer

(2) Main Functions

The following are the main functions of data transfer performed by the module :

- Independent data transfer in multiple channels is enabled (5 channels) .

  a : Priority (channel 0 > channel 1 > channel 2 > channel 3 > channel 4)
  b : Priority can be alternated between channel 0 and channel 1.
  c : DMAC start cause
  - External-only pin input (edge detection/level detection channels 0 to 2 only)
  - Internal peripheral request (interrupt request is shared, including external interrupts)
  - Software request (register write)

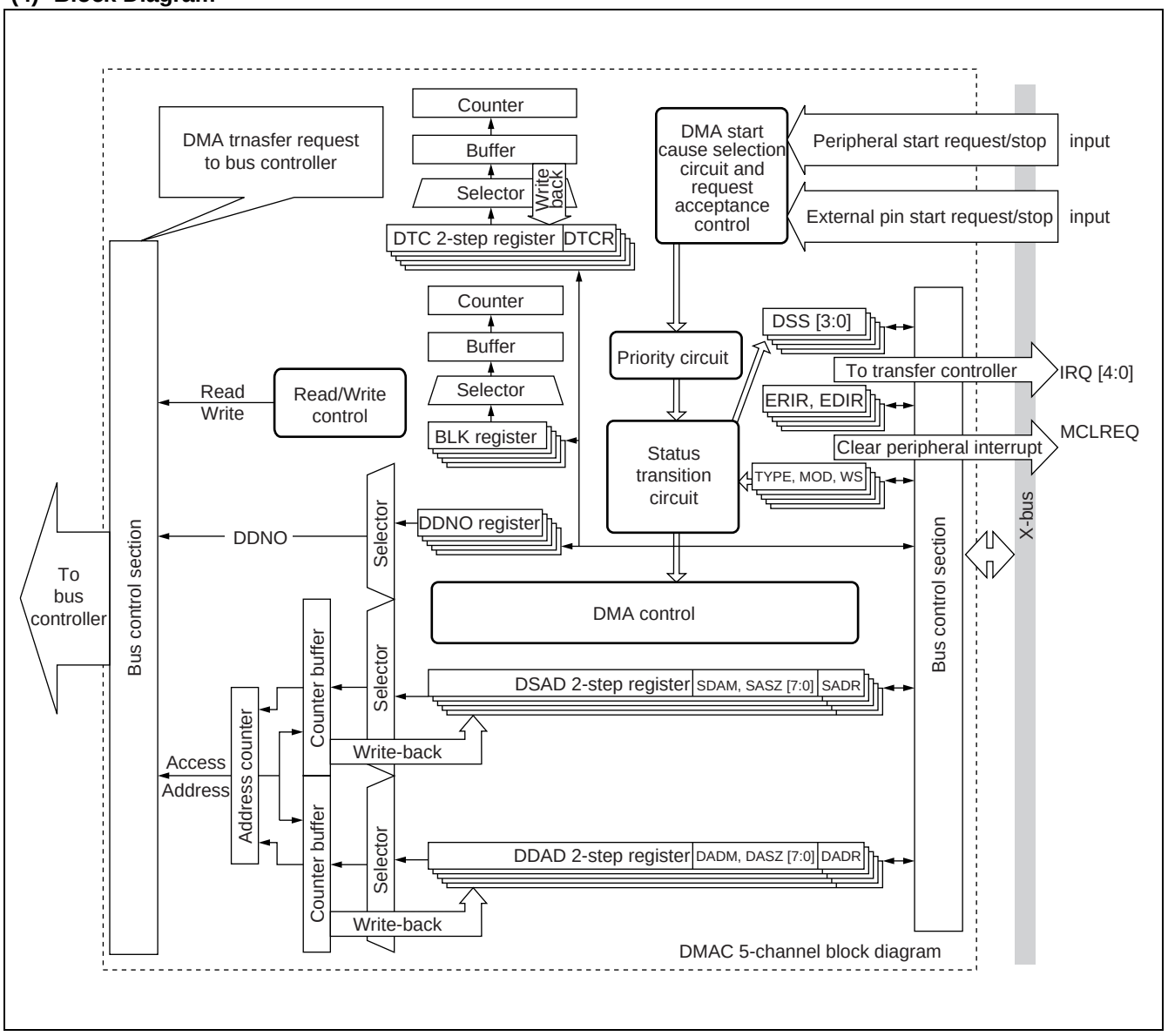
  d : Transfer mode
  - Demand transfer, burst transfer, step transfer, block transfer
  - Addressing mode 32-bit full address specification (increase, decrease, fixed)
    (An address increment/decrement size of –255 to +255 can be specified.)
  - Data types of byte, halfword, and word lengths
  - Single-shot/reload selectable

(3) Registers Configuration

Channel 0 control/status register A	DMACA0 0000200H
Channel 0 control/status register B	DMACB0 0000204H
Channel 1 control/status register A	DMACA1 0000208H
Channel 1 control/status register B	DMACB1 000020CH
Channel 2 control/status register A	DMACA2 0000210H
Channel 2 control/status register B	DMACB2 0000214H
Channel 3 control/status register A	DMACA3 0000218H
Channel 3 control/status register B	DMACB3 000021CH
Channel 4 control/status register A	DMACA4 0000220H
Channel 4 control/status register B	DMACB4 0000224H
Overall control register	DMACR 0000240H

Channel 0 transfer source address register	DMASA0 0001000H
Channel 0 transfer destination address register	DMADA0 0001004H
Channel 1 transfer source address register	DMASA1 0001008H
Channel 1 transfer destination address register	DMADA1 000100CH
Channel 2 transfer source address register	DMASA2 0001010H
Channel 2 transfer destination address register	DMADA2 0001014H
Channel 3 transfer source address register	DMASA3 0001018H
Channel 3 transfer destination address register	DMADA3 000101CH
Channel 4 transfer source address register	DMASA4 0001020H
Channel 4 transfer destination address register	DMADA4 0001028H

(4) Block Diagram



6. UART

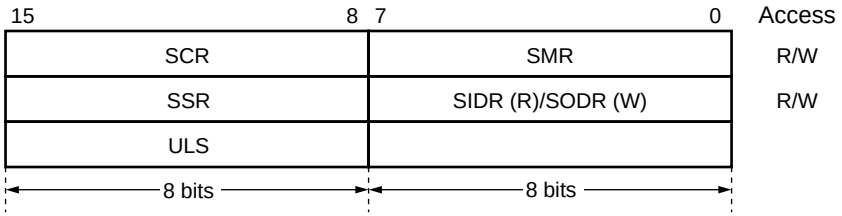
The UART is a serial I/O port for performing asynchronous (stop-start synchronization) communications. The MB91360G series contains three UART channels.

(1) Features

- Full-duplex, double buffering
- Supports asynchronous (stop-start synchronization) communications
- Supports multi-processor mode
- Fully programmable baud rate
  The baud rate can be set using an internal timer. (See the U-TIMER section.)
- Supports flexible baud rate setting using an external clock
- Error detection function (parity, framing, overrun)
- Non return to zero (NRZ) transfer signal
- Supports DMA transfer activation using an interrupt

(2) Register Configuration

Register structure



Serial input register (SIDR)

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Serial output register (SODR)

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Serial status register (SSR)

7	6	5	4	3	2	1	0
PE	ORE	FRE	RDRF	TDRE	—	RIE	TIE

Serial mode register (SMR)

7	6	5	4	3	2	1	0
MD1	MD0	—	—	CS0	—	SCKE	—

Serial control register (SCR)

7	6	5	4	3	2	1	0
PEN	P	SBL	CL	A/D	REC	RXE	TXE

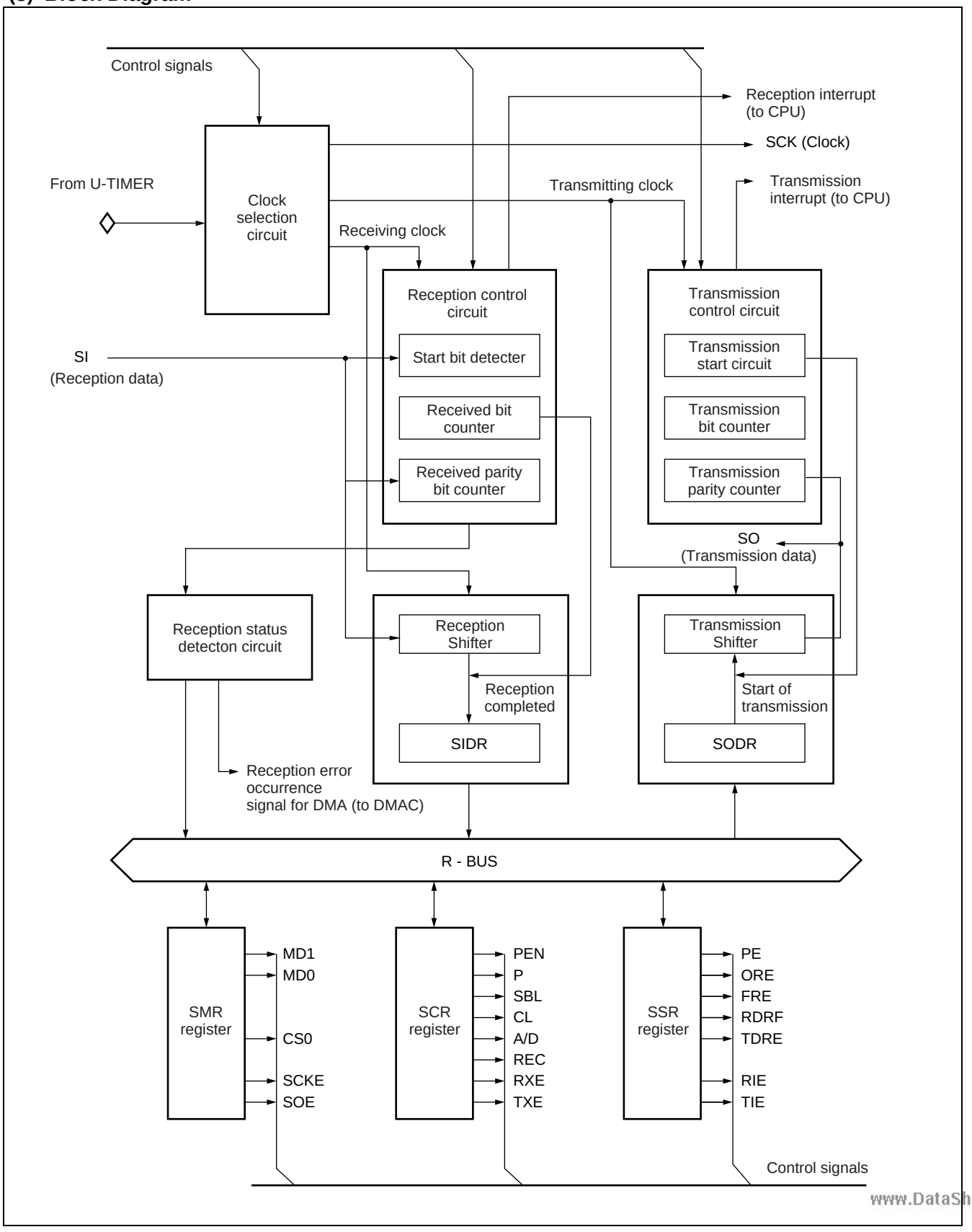
UART level select register (ULS)

7	6	5	4	3	2	1	0
—	—	—	—	NSDO	NSDI	UTDBL	UDBL

	Address	Bits	7	6	5	4	3	2	1	0	Initial value
SMR	0000 0063$_H$ 0000 006F$_H$ 0000 007B$_H$		MD1	MD2	Reserved	Reserved	CS0	Reserved	Reserved	Reserved	00--0-00$_B$
			R/W	R/W			W				← Access

	Address	Bits	7	6	5	4	3	2	1	0	Initial value
SCR	0000 0062$_H$ 0000 006E$_H$ 0000 007A$_H$		PEN	P	SBL	CL	A/D	REC	RXE	TXE	00000100$_B$
			R/W	R/W	R/W	R/W	R/W	W	R/W	R/W	← Access

(3) Block Diagram

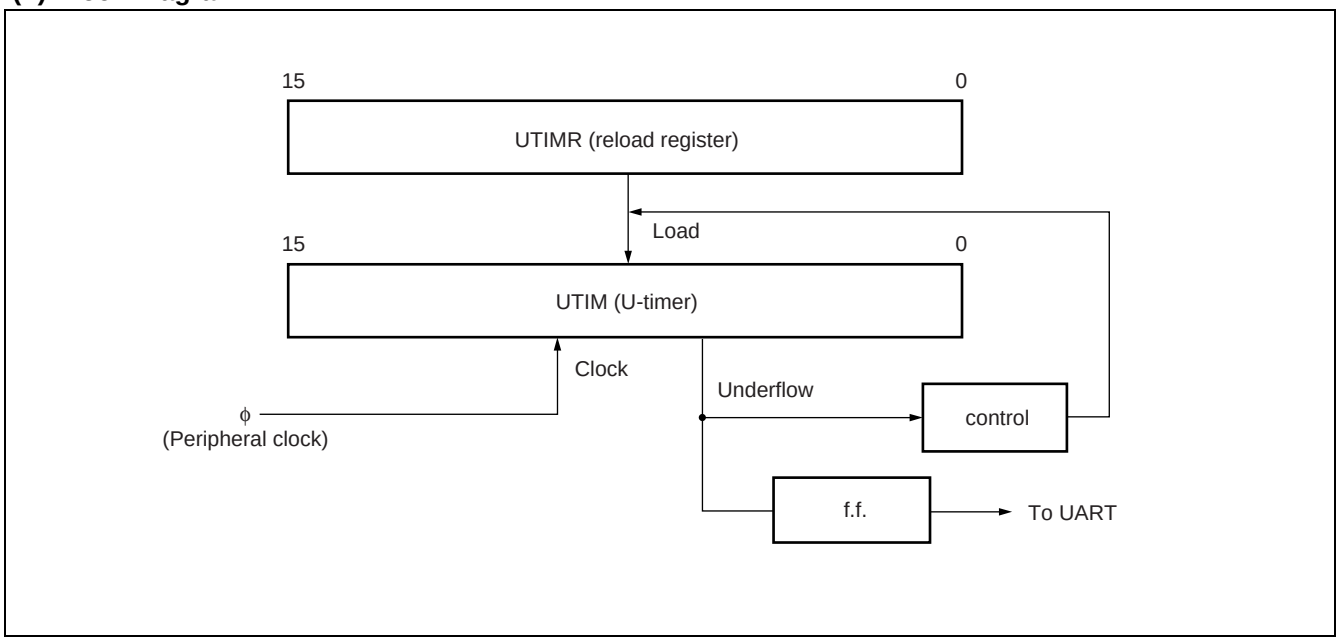


7. U-TIMER (16-bit Timer for UART Baud Rate Generation)

The U-timer (U-TIMER) is a 16-bit timer used to generate the baud rate for the UART. The operating frequency of the chip and the U-TIMER reload value can be combined to set a user-defined baud rate.

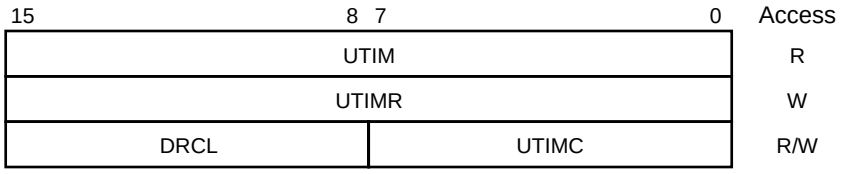
The MB91360G series contains three U-TIMER channels. The intervaltimers can count for a maximum of 216 × ϕ.

(1) Block Diagram



(2) Register Configuration

Register structure



R : Read,
W : Write

UTIM	Address	Bits	15	14	----------	2	1	0	Initial value	Access
0-ch	00000068H		b15	b14		b2	b1	b0	0	R
1-ch	00000074H									
2-ch	00000080H									

UTIMR Reload Register

UTIMR	Address	Bits	15	14	----------	2	1	0	Initial value	Access
0-ch	00000068H		b15	b14		b2	b1	b0	0	W
1-ch	00000074H									
2-ch	00000080H									

UTIMC U Timer Control Register

UTIMC	Address	7	6	5	4	3	2	1	0	Initial value	Access
0-ch	0000006BH	UCC1	—	—	—	UNDR	Reserved	UTST	UTCR	0---0001	R/W
1-ch	00000077H										
2-ch	00000083H										

8. PWM TIMER

The PWM (Pulse Width Modulation) timer can output high-precision pulse waves at an arbitrary cycle and pulse width (duty ratio) .

The MB91360G series contains eight PWM timer channels. Each of the channels consists of a 16-bit down-counter, cycle setting register, duty setting register, and pin controller.

The control status register for each channel is used to indicate the operation status of the PWM timer. General control registers 1 and 2 are common registers shared by four channels, serving for input and software triggering.

(1) Features

- The count clock for the 16-bit down-counter can be selected from among the following four types :
  Internal clocks : ϕ, ϕ/4, ϕ/16, ϕ/64 (ϕ : Machine clock for peripherals)
- The counter can be initialized to "$FFFF_H$" by a reset or underflow.
  The 16-bit down-counter causes an underflow when it changes from "0000_H" to "$FFFF_H$".
- Each channel has PWM outputs.
- Eight channels : Eight output pins
- Registers
- Cycle setting register : Data reload register with buffer
- Data transfer from the buffer is performed either when an activation trigger is detected or when the down-counter causes an underflow (cycle match) . The output is inverted at a cycle match.
- Duty setting register : Compare register with buffer.
- The value set in this register is compared to the counter value. The output is inverted when the values match (duty match) .
- Pin control
- A duty match causes a reset to "1" (given priority) .
- An underflow causes a reset to "0".
- The output value fix mode enables output of all "L" or all "H".
- The polarity can also be specified.
- Interrupt requests can be generated by selecting the following interrupt sources :
- Activation of the PWM timer (software trigger or trigger input)
- Occurrence of an underflow (cycle match)
- Occurrence of a duty match
- Occurrence of an underflow (cycle match) or duty match
- You can set simultaneous activation of two or more channels using software or another interval timer. You can also set restarting the PWM timer during operation.

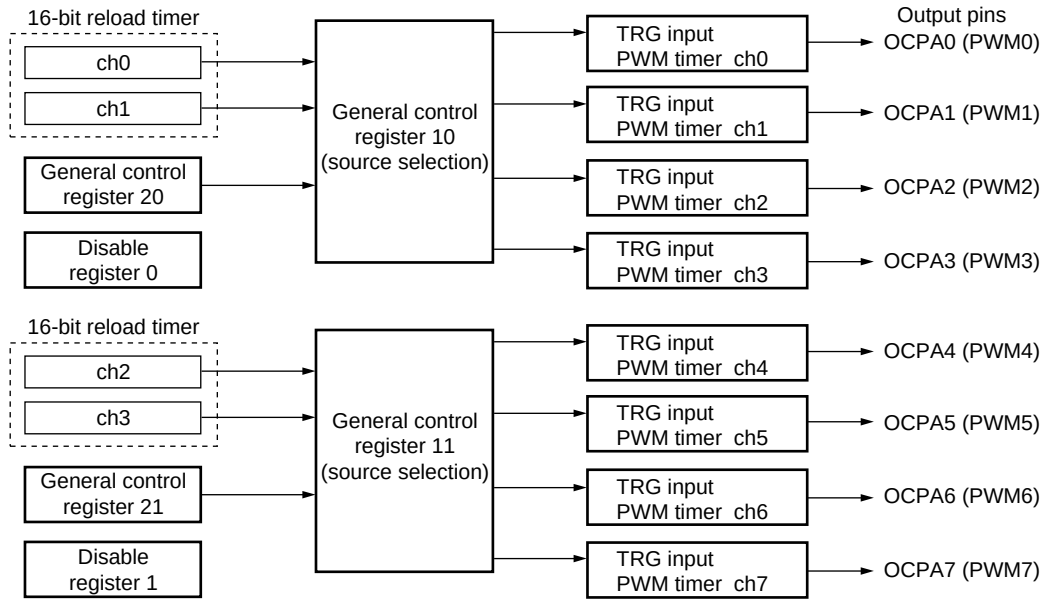
(2) Register Configuration for Channels 1 to 3

Address	Bits 15 8 7 0	Access	Register name
00000118H	GCN10	R/W	General control register 10
0000011AH	PDBL0 / GCN20	R/W	Disable/General control register 20
PWM timer ch 0			
00000120H	PTMR	R	ch0 timer register
00000122H	PCSR	W	ch0 cycle setting register
00000124H	PDUT	W	ch0 duty setting register
00000126H	PCNH / PCNL	R/W	ch0 control status registers
PWM timer ch 1			
00000128H	PTMR	R	ch1 timer register
0000012AH	PCSR	W	ch1 cycle setting register
0000012CH	PDUT	W	ch1 duty setting register
0000012EH	PCNH / PCNL	R/W	ch1 control status registers
PWM timer ch 2			
00000130H	PTMR	R	ch2 timer register
00000132H	PCSR	W	ch2 cycle setting register
00000134H	PDUT	W	ch2 duty setting register
00000136H	PCNH / PCNL	R/W	ch2 control status registers
PWM timer ch 3			
00000138H	PTMR	R	ch3 timer register
0000013AH	PCSR	W	ch3 cycle setting register
0000013CH	PDUT	W	ch3 duty setting register
0000013EH	PCNH / PCNL	R/W	ch3 control status registers

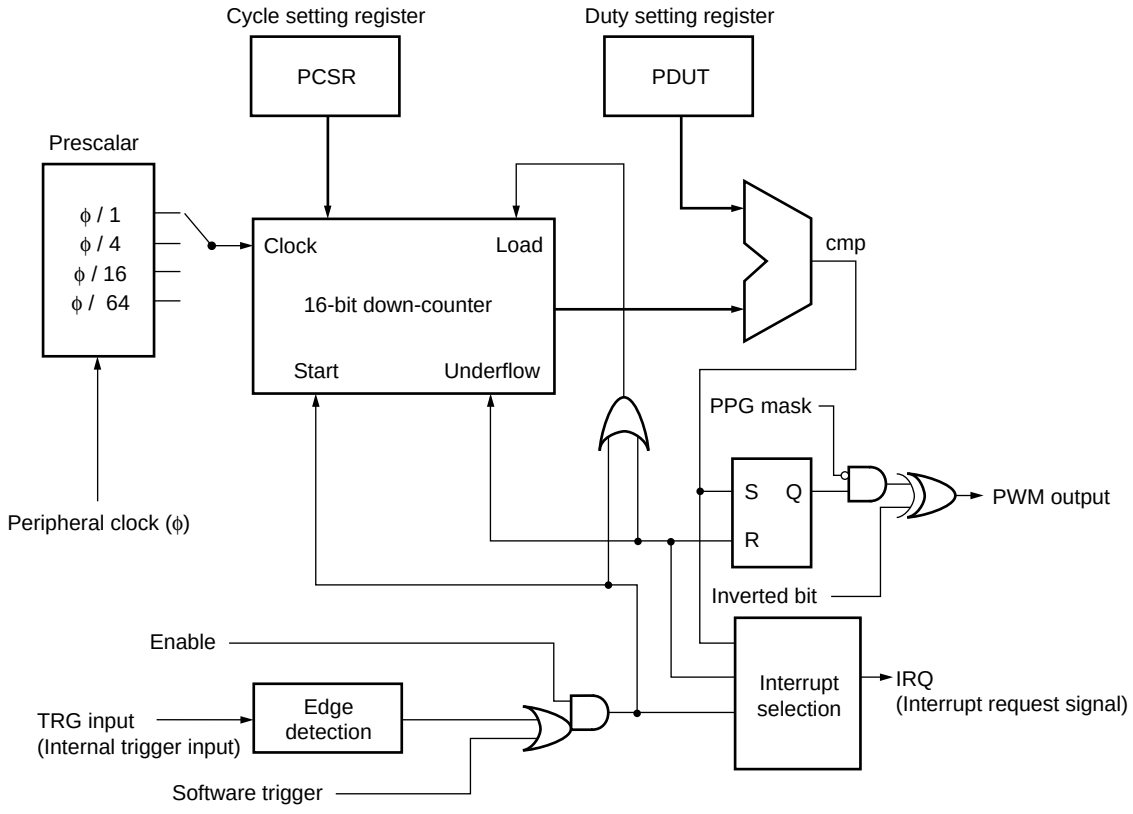
(3) PWM Timer Registers for Channels 4 to 7

Address	Bits 15 – 8	Bits 7 – 0	Access	Register name
0000011CH	GCN11		R/W	General control register 11
0000011EH	PDBL1	GCN21	R/W	Disable/General control register 21
PWM timer ch 4				
00000140H	PTMR		R	ch4 timer register
00000142H	PCSR		W	ch4 cycle setting register
00000144H	PDUT		W	ch4 duty setting register
00000146H	PCNH	PCNL	R/W	ch4 control status registers
PWM timer ch 5				
00000148H	PTMR		R	ch5 timer register
0000014AH	PCSR		W	ch5 cycle setting register
0000014CH	PDUT		W	ch5 duty setting register
0000014EH	PCNH	PCNL	R/W	ch5 control status registers
PWM timer ch 6				
00000150H	PTMR		R	ch6 timer register
00000152H	PCSR		W	ch6 cycle setting register
00000154H	PDUT		W	ch6 duty setting register
00000156H	PCNH	PCNL	R/W	ch6 control status registers
PWM timer ch 7				
00000158H	PTMR		R	ch7 timer register
0000015AH	PCSR		W	ch7 cycle setting register
0000015CH	PDUT		W	ch7 duty setting register
0000015EH	PCNH	PCNL	R/W	ch7 control status registers

(4) Configuration Diagram of the Entire PWM Timer



(5) Configuration Diagram of PWM Timer 1 ch



9. 16-BIT RELOAD TIMER

Each 16-bit reload timer consists of a 16-bit down-counter, a 16-bit reload register, a prescaler for generating the internal count clock, and a control register.

The 16-bit reload timer can also activate DMA transfer using interrupts.

The MB91360G series contains six 16-bit reload timer channels.

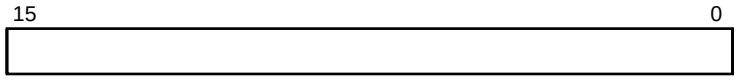
(1) 16 bit Reloard Timer Register Configuration

Control status register (TMCSR)

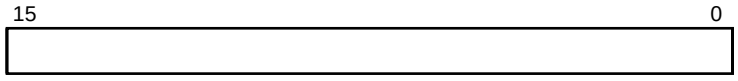
15	14	13	12	11	10	9	8
—	—	—	—	CSL1	CSL0	—	—

7	6	5	4	3	2	1	0
—	—	—	RELD	INTE	UF	CNTE	TRG

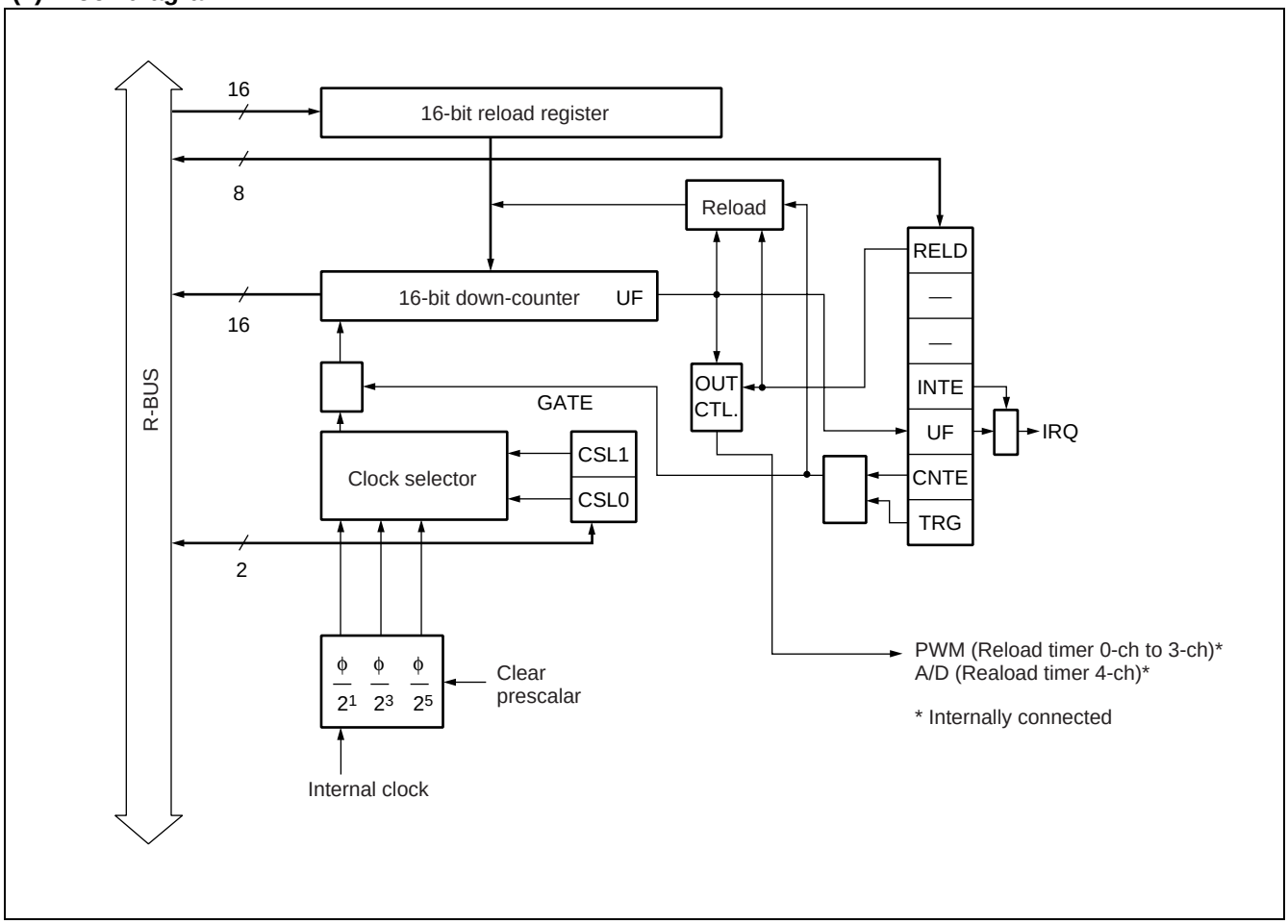
16-bit timer register (TMR)



16-bit reload register (TMRLR)



(2) Block diagram



10. BIT SEARCH MODULE

The bit search module searches for a “0”, “1”, or change-point in the data written to the input register and returns the position of the detected bit.

This section describes the data register for detecting zeros (BSD0) , data register for detecting ones (BSD1) , data register for detecting change-points (BSDC) , and detection result register (BSRR) .

a : **Data register for detecting zeros (BSD0)**

Address	31 Register structure 0	Initial value	Access
0000 03F0H		Indeterminate	W

b : **Date register for detecting ones (BSD1)**

Address	31 Register structure 0	Initial value	Access
0000 03F4H		Indeterminate	R/W

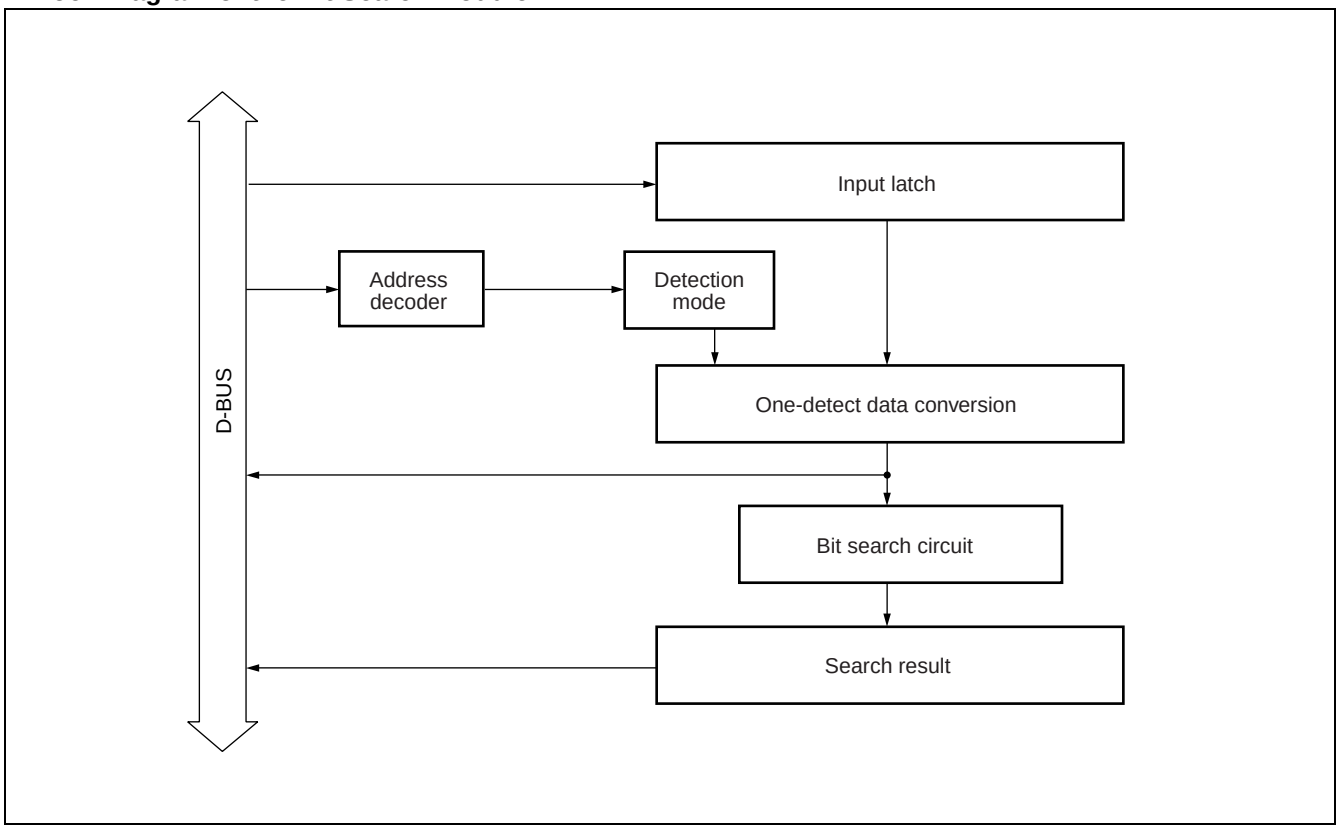
c : **Data register for detecting change points (BSDC)**

Address	31 Register structure 0	Initial value	Access
0000 03F8H		Indeterminate	W

d : **Detection Result Register** (**BSRR**)

Address	31 Register structure 0	Initial value	Access
0000 03FCH		Indeterminate	R

• **Block Diagram of the Bit Search Module**



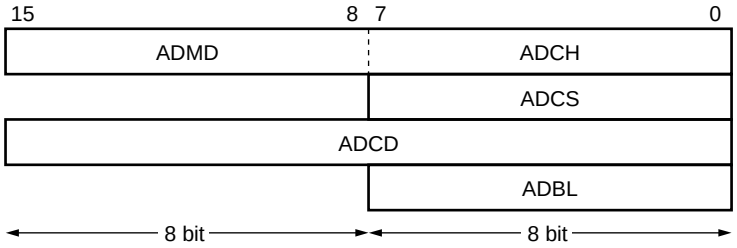
11. 10-BIT A/D CONVERTER (Successive Approximation Conversion Type)

This section provides an overview of the A/D converter, describes the register structure and functions, and describes the operation of the A/D converter.

A/D Converter converts analog input voltage into digital values, and provides the following features.

- Conversion time : minimum 178 cycles (32 MHz : 5.6 µs, 24 MHz : 7.4 µs, 16 MHz : 11.2 µs) per channel
- RC type successive approximation conversion with sample & hold circuit
- 10-bit resolution
- Program selection analog input from 16 channels
- Single conversion mode : conversion of one selected channel
- Scan conversion mode : continuous conversion of multiple channels, programmable for up to 16 channels
- Single conversion mode : Convert the specified channel once only.
- Continuous mode : Repeatedly convert the specified channels.
- Stop mode : Convert one channel then temporarily halt until the next activation.
  (Enables synchronization of the conversion start timing.)
  A/D conversion can be followed by an A/D conversion interrupt request to CPU. This interrupt, an option that is ideal for continuous processing can be used to start a DMA transfer of the results of A/D conversion to memory.

- Startup may be by software, external trigger (falling edge) or timer (rising edge)



Channel setting register (ADCH)

bit	7	6	5	4	3	2	1	0
Address : 00009D$_H$	ANS3	ANS2	ANS1	ANS0	ANE3	ANE2	ANE1	ANE0

Mode register (ADMD)

bit	15	14	13	12	11	10	9	8
Address : 00009C$_H$	—	—	—	—	MOD1	MOD0	STS1	STS0

Control status register (ADCS)

bit	7	6	5	4	3	2	1	0
Address : 00009F$_H$	BUSY	INT	INTE	PAUS	—	—	STRT	Reserved

Data register (ADCD)

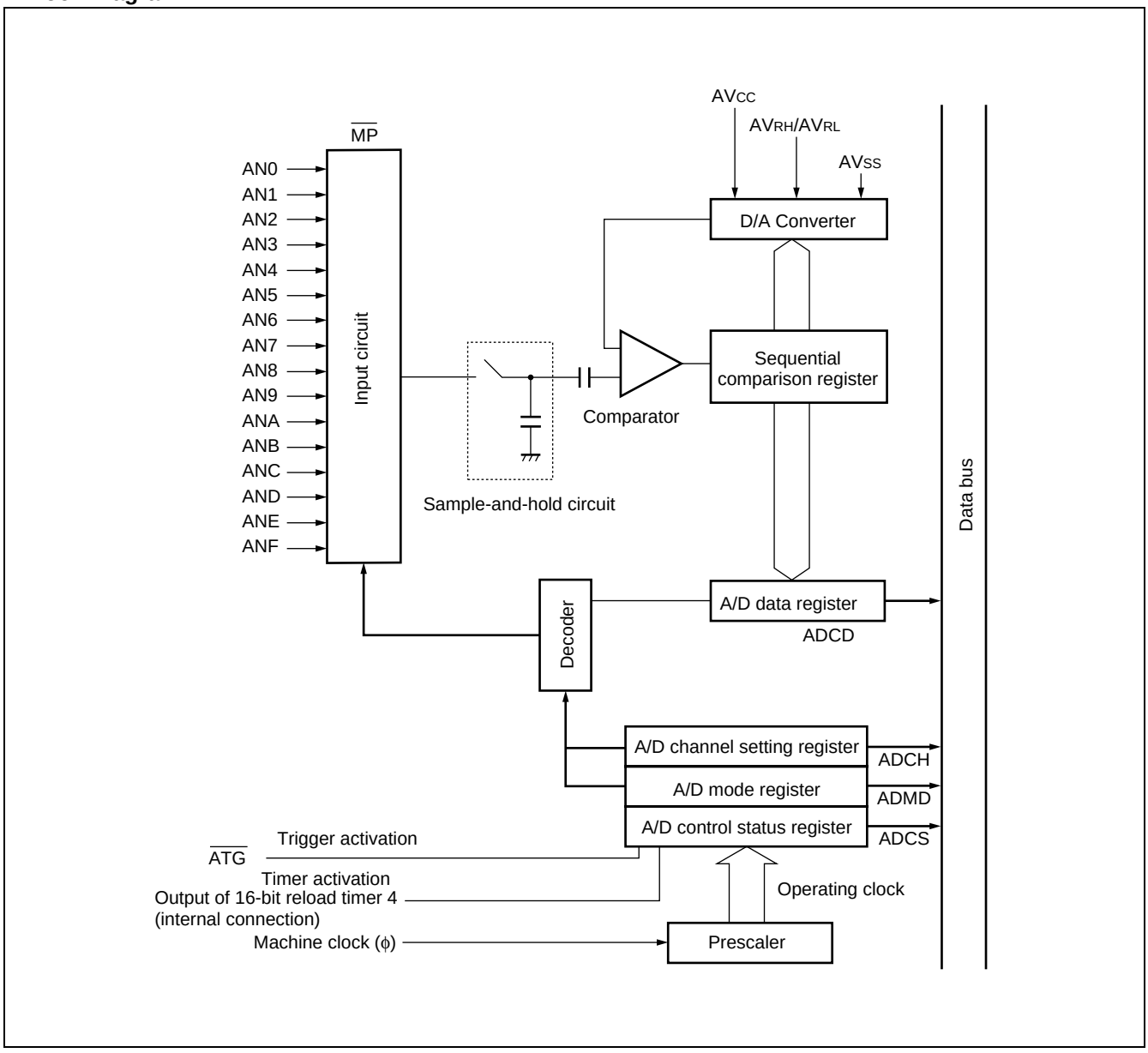
bit	7	6	5	4	3	2	1	0
Address : 0000A1$_H$	D7	D6	D5	D4	D3	D2	D1	D0

bit	15	14	13	12	11	10	9	8
Address : 0000A0$_H$	—	—	—	—	—	—	D9	D8

Disable register (ADBL)

bit	15	14	13	12	11	10	9	8
Address : 0000A3$_H$	—	—	—	—	—	—	—	DBL

• **Block Diagram**



12. INTERRUPT CONTROLLER

An interrupt controller controls interrupt acceptance and arbitration processing.

Hardware configuration

This module consists of the following :

- ICR register
- Interrupt priority evaluation circuit
- Interrupt level and interrupt number (vector) generator
- Hold request cancel request generator

Major functions

This module has the following major functions :

- Detecting an NMI request or interrupt request
- Priority evaluation (using the level or number)
- Transferring the level of the interrupt cause in the evaluation result (to the CPU)
- Transferring the number of the interrupt cause in the evaluation result (to the CPU)
- Instructing recovery from stop mode due to an NMI or interrupt level other than 11111 (to the CPU)
- Generating a hold request cancel request for the bus master

(1) Register Configuration

	bit 7	6	5	4	3	2	1	0	
Address : 00000440H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR00
Address : 00000441H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR01
Address : 00000442H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR02
Address : 00000443H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR03
Address : 00000444H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR04
Address : 00000445H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR05
Address : 00000446H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR06
Address : 00000447H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR07
Address : 00000448H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR08
Address : 00000449H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR09
Address : 0000044AH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR10
Address : 0000044BH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR11
Address : 0000044CH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR12
Address : 0000044DH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR13
Address : 0000044EH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR14
Address : 0000044FH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR15
Address : 00000450H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR16
Address : 00000451H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR17
Address : 00000452H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR18
Address : 00000453H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR19
Address : 00000454H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR20
Address : 00000455H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR21
Address : 00000456H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR22
Address : 00000457H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR23
Address : 00000458H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR24
Address : 00000459H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR25
Address : 0000045AH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR26
Address : 0000045BH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR27
Address : 0000045CH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR28
Address : 0000045DH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR29
Address : 0000045EH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR30
Address : 0000045FH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR31
				R	R/W	R/W	R/W	R/W	

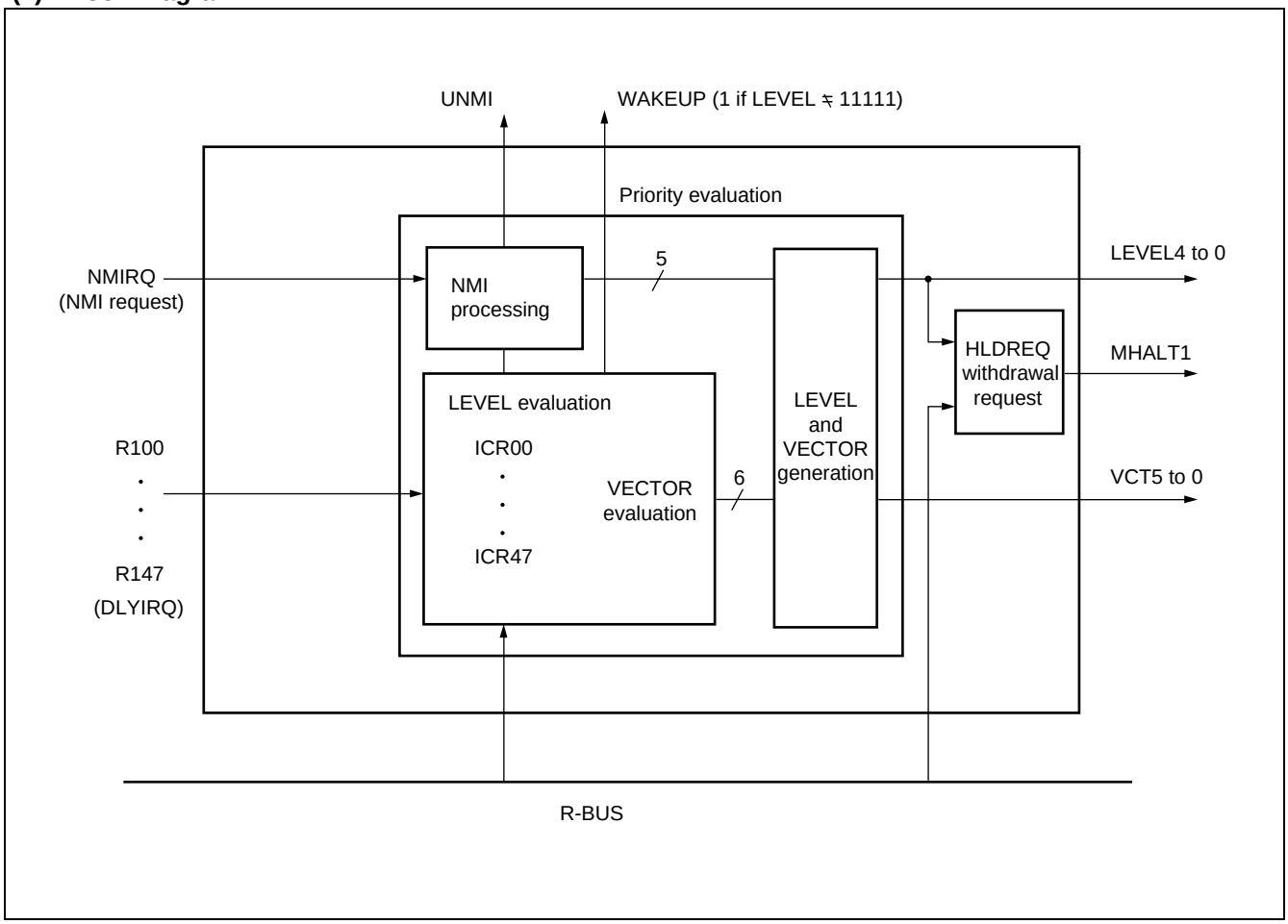
(Continued)

(Continued)

	bit 7	6	5	4	3	2	1	0	
Address : 00000460H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR32
Address : 00000461H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR33
Address : 00000462H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR34
Address : 00000463H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR35
Address : 00000464H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR36
Address : 00000465H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR37
Address : 00000466H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR38
Address : 00000467H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR39
Address : 00000468H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR40
Address : 00000469H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR41
Address : 0000046AH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR42
Address : 0000046BH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR43
Address : 0000046CH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR44
Address : 0000046DH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR45
Address : 0000046EH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR46
Address : 0000046FH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR47
				R	R/W	R/W	R/W	R/W	

Address : 00000045H	MHALTI	—	—	LVL4	LVL3	LVL2	LVL1	LVL0	HRCL
	R/W			R	R/W	R/W	R/W	R/W	

(2) Block Diagram



13. EXTERNAL INTERRUPT/NMI CONTROL BLOCK

The external interrupt/NMI controller controls external interrupt requests input from the NMI and INT0 to INT7 pins.

Detection of “H” levels, “L” levels, rising edges, or falling edges can be selected (except for the NMI) .

The external interrupt/NMI controller can also be used for DMA requests.

This section lists the registers of the controller and provides its block diagram.

(1) Register configuration of the External Interrupt NMI Controller

External interruption permission register (ENIR)

Bit	7	6	5	4	3	2	1	0
	EN7	EN6	EN5	EN4	EN3	EN2	EN1	EN0

External interruption factors register (EIRR)

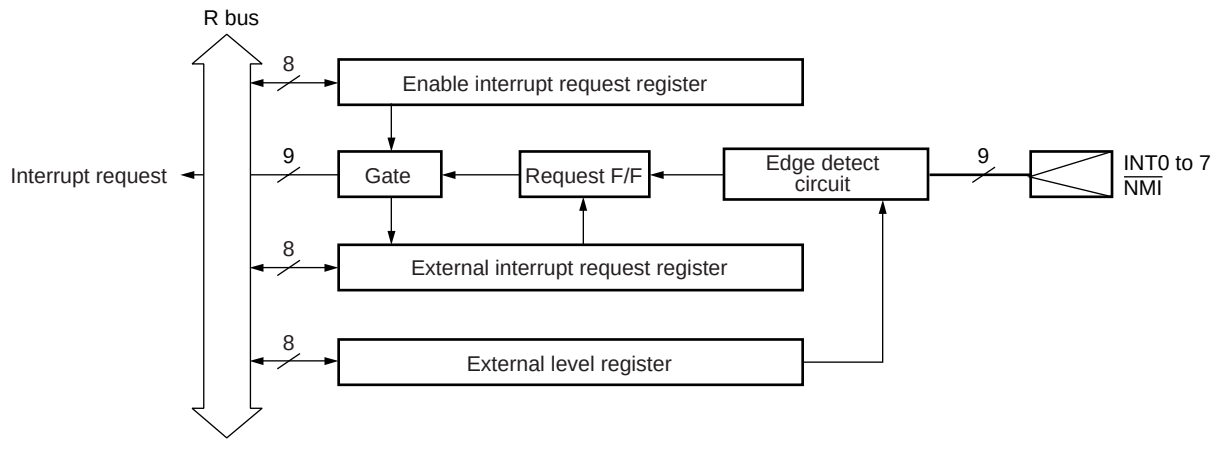
Bit	15	14	13	12	11	10	9	8
	ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0

Request level setting register (ELVR)

Bit	15	14	13	12	11	10	9	8
	LB7	LA7	LB6	LA6	LB5	LA5	LB4	LA4

Bit	7	6	5	4	3	2	1	0
	LB3	LA3	LB2	LA2	LB1	LA1	LB0	LA0

(2) Block diagram



14. DELAYED INTERRUPT

Delayed Interrupt Control Register (DICR)

The delayed interrupt control register (DICR) is a delayed interrupt generator register and is used to generate the task switching interrupt.

Structure of the DICR

Address	Bits	7	6	5	4	3	2	1	0	Initial value
00000044H		—	—	—	—	—	—	—	DLYI	- - - - - - - 0
									R/W	← Access

15. CLOCK GENERATION

The MB91V360 generates internal operating clocks as follows :

- Base clock generation : Device scales clock source input by 2 (X clock) or oscillates base clock with PLL to generate basic clock (PLL clock)
- Generation of each internal clock : Device scales base clock to generate clocks supplied to each block

Generation and control of each clock are explained below.

Some devices allow the operation of the RTC module based on a separate 32 kHz subclock. See the section about subclock operation for more details.

(1) Register Configuration

RSRR : **Reset Source Register**, **Watchdog Timer Control Register**

bit	15	14	13	12	11	10	9	8
address : 00000480H	INIT	HSTB	WDOG	ERST	SRST	—	WT1	WT0
access	R	R	R	R	R	—	R/W	R/W
Initial Value ($\overline{INIT}$)	1	0	0	0	0	—	0	0
Initial Value (INIT)	*	*	*	X	X	—	0	0
Initial Value (RST)	X	X	X	*	*	—	0	0
After Boot ROM **	0	0	0	0	0	0	0	0

* : varies with reset factor
x : not initialized

** : After execution of the program in the internal boot ROM the reset source is visible

STCR : **Standby Control Register**

bit	7	6	5	4	3	2	1	0
address : 00000481H	STOP	SLEEP	HIZ	SRST	OS1	OS0	OSCD2	OSCD1
access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value ($\overline{INIT}$)	0	0	1	1	0	0	1	1
Initial Value ($\overline{HST}$) *	0	0	1	1	1	1	1	1
Initial Value (INIT)	0	0	1	1	X	X	1	1
Initial Value (RST)	0	0	X	1	X	X	X	X

* : Valid only when this initialization is performed simultaneously with initialization by $\overline{INIT}$: others same as INIT.

(Continued)

TBCR : Time-based counter control register

bit	15	14	13	12	11	10	9	8
address : 00000482H	TBIF	TBIE	TBC2	TBC1	TBC0	—	SYNCR	SYNCS
Initial Value (INIT)	0	0	X	X	X	X	0	0
Initial Value (RST)	0	0	X	X	X	X	X	X
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

CTBR : Time-based counter clear register

bit	7	6	5	4	3	2	1	0
address : 00000483H	D7	D6	D5	D4	D3	D2	D1	D0
Initial Value (INIT)	X	X	X	X	X	X	X	X
Initial Value (RST)	X	X	X	X	X	X	X	X
	W	W	W	W	W	W	W	W

CLKR : Clock source control register

bit	15	14	13	12	11	10	9	8
address : 00000484H	PLL2S0	PLL1S2	PLL1S1	PLL1S0	PLL2EN	PLL1EN	CLKS1	CLKS0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value (INIT)	0	0	0	0	0	0	0	0
Initial Value (RST)	X	X	X	X	X	X	X	X

WPR Watchdog reset generation postponement register

bit	7	6	5	4	3	2	1	0
address : 00000485H	D7	D6	D5	D4	D3	D2	D1	D0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value (INIT)	X	X	X	X	X	X	X	X
Initial Value (RST)	X	X	X	X	X	X	X	X

DIVR0 : Base clock division setting register 0

bit	7	6	5	4	3	2	1	0
address : 00000486H	B3	B2	B1	B0	P3	P2	P1	P0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value (INIT)	0	0	0	0	0	0	1	1
Initial Value (RST)	X	X	X	X	X	X	X	X

DIVR1 : Base clock division setting register 1

bit	7	6	5	4	3	2	1	0
address : 00000487H	T3	T2	T1	T0	S3	S2	S1	S0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value (INIT)	0	0	0	0	0	0	0	0
Initial Value (RST)	X	X	X	X	X	X	X	X

(Continued)

(Continued)

CMCR : Clock Control for CAN Modules

address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	initial
0164H	PRE7	PRE6	PRE5	PRE4	PRE3	PRE2	PRE1	PRE0	11111111

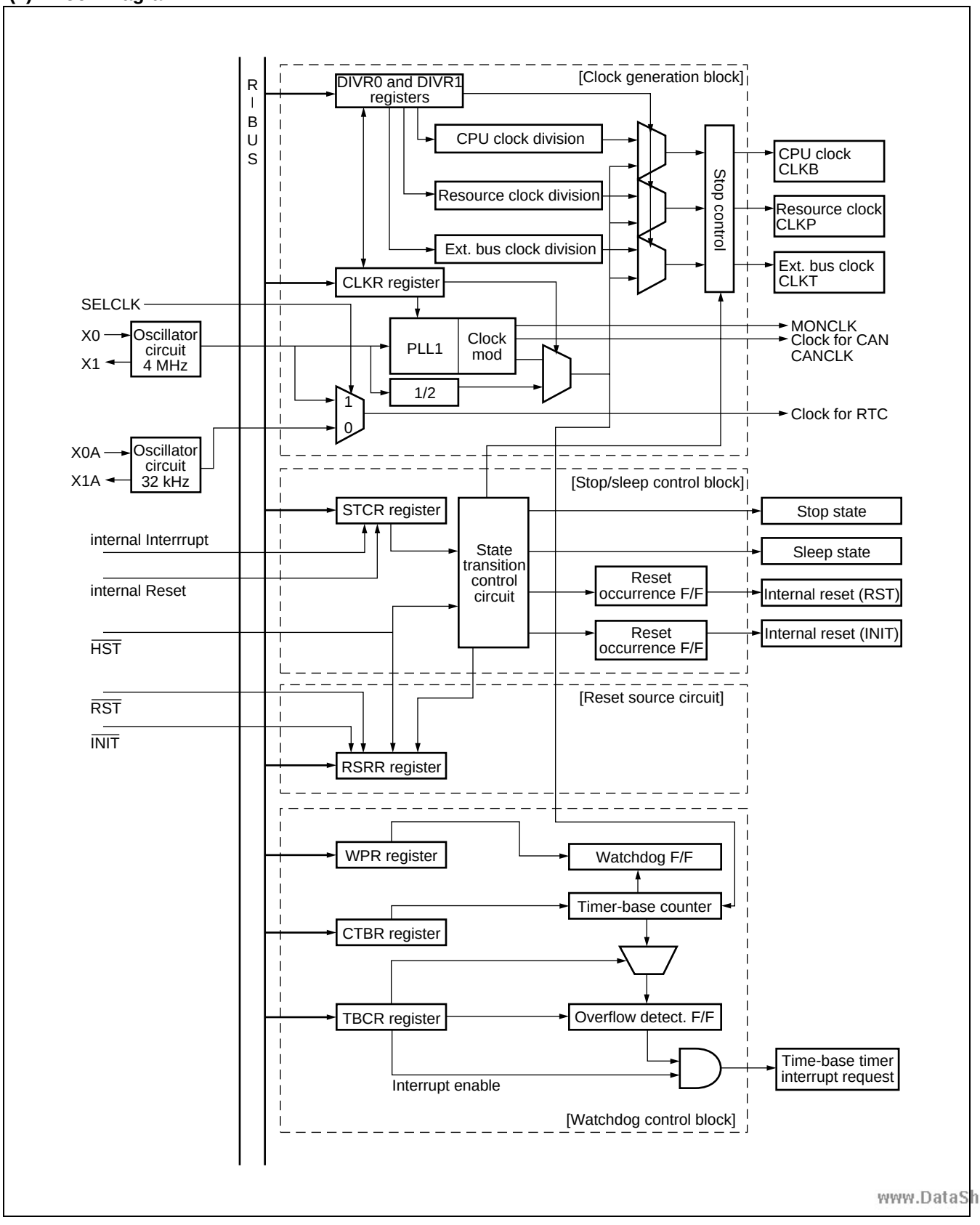
address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	initial
0165H	PRES	—	—	—	—	—	—	—	00000000

Subclock RTC32 (CLKR2)

This register is used to control the RTC32 mode bit for use in subclock system.

address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
000046H	—	—	—	—	—	—	—	RTC32
access						R/W	R/W	R/W
initial value						0	0	0

(2) Block Diagram



16. BUS INTERFACE

The external bus interface controls the interfaces with the external memory and external I/Os.

- Up to 32-bit (4 GB) address output.
- Up to eight independent banks provided by chip-select function
  The banks can be set in 64-KB (minimum) at any position in the logic address space.
  Can be set to no area
- 32/16/8 bit bus width setup can be performed for each chip-select area.
- Programmable automatic memory wait (up to 7 cycles) insertion

Note : Chip Select Areas CS7 and CS1 are used for the internal CAN modules and Flash module (F361GA only) respectively. The necessary register settings are done by an internal boot routine. Take care not to overwrite register bits related to those CS areas.
If the CAN macros and the flash memory which are connected internally to the external bus (also called User Logic Bus) are used, a certain number of data, address and control ports of the external bus interface cannot be configured as general purpose IO ports.

(1) Register Configuration

Area select Registers (ASR0 to ASR7)

	bit 7 ... bit 0		R/W
00000640H	ASR0	00000000B	W
00000644H	ASR1	0000XXXXB	W
00000648H	ASR2	0000XXXXB	W
0000064CH	ASR3	0000XXXXB	W
00000650H	ASR4	0000XXXXB	W
00000654H	ASR5	0000XXXXB	W
00000658H	ASR6	0000XXXXB	W
0000065CH	ASR7	00000000B	W

After execution of the code internal boot ROM ASR0 is set to “0x20”, ASR1 to “0x1C”, and ASR7 to “0x10” (F361GA only)

(Continued)

(Continued)

Area Mask Register (AMR0 to AMR7)

AMR0	00000642H	AM R0	FFFFFFFFH	W
AMR1	00000646H	AMR1	0000XXXXH	W
AMR2	0000064AH	AMR2	0000XXXXH	W
AMR3	0000064EH	AMR3	0000XXXXH	W
AMR4	0000652H	AMR4	0000XXXXH	W
AMR5	00000656H	AMR5	0000XXXXH	W
AMR6	0000065AH	AMR6	0000XXXXH	W
AMR7	0000065CH	AMR7	00000000H	W

Area Mode Registers (AMD0 to AMD7)

00000660H

—	—	RDYE	BW1	BW0	WTC2	WTC1	WTC0

00000111B R / W

CHE (CacHe Enable register)

00000670H

CHE7	CHE6	CHE5	CHE4	CHE3	CHE2	CHE1	CHE0

11111111B R / W

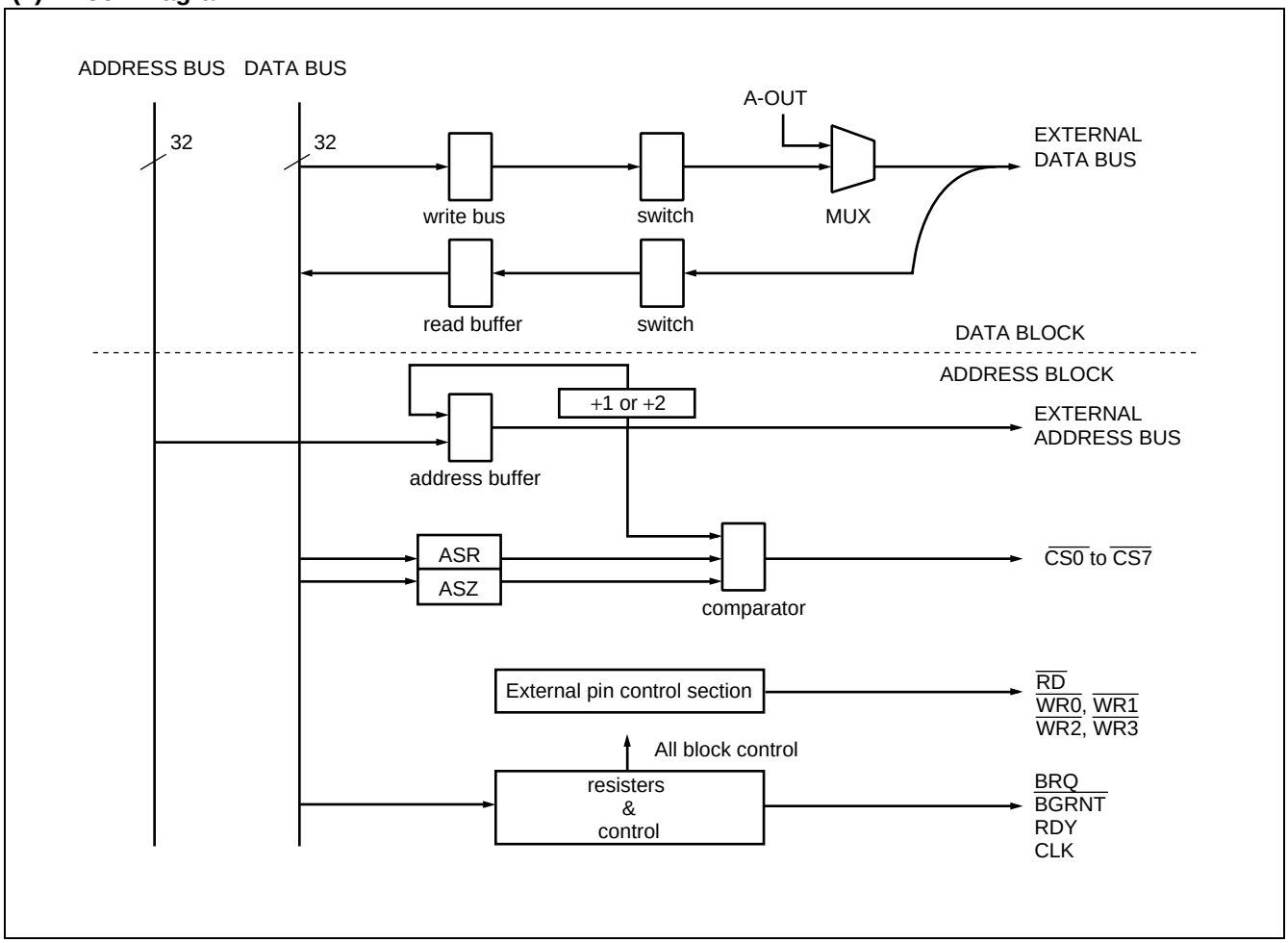
CSE (Chip Select Enable register)

00000668H

CSE7	CSE6	CSE5	CSE4	CSE3	CSE2	CSE1	CSE0

00000001B R / W

(2) Block Diagram



17. CAN CONTROLLER

This section provides an overview of the CAN Interface, describes the register structure and functions, and describes the operation of the CAN Interface.

The CAN controller is a module built into a MB91360G series. The CAN (Controller Area Network) is the standard protocol for serial communication between automobile controllers and is widely used in industrial applications.

The CAN controller has the following features :

- Conforms to CAN Specification Version 2.0 Part A and B
  - Supports transmission/reception in standard frame and extended frame formats
- Supports transmitting of data frames by receiving remote frames
- 16 transmitting/receiving message buffers
  - 29-bit ID and 8-byte data
  - Multi-level message buffer configuration
- Supports full-bit comparison, full-bit mask and partial bit mask filtering.
  - Two acceptance mask registers in either standard frame format or extended frame formats
- Bit rate programmable from 10 Kbits/s to 1 Mbits/s (when input clock is at 16 MHz)

The following sections only describe CAN 0. For the addresses of the registers of the other CAN channels see the IO-Map.

(1) List of Control Registers

List of Control Registers (1)

Address CAN0	Register	Abbreviation	Access	Initial Value
100000H	Message buffer valid register	BVALR0	R/W	00000000 00000000
100001H				
100002H	Transmit request register	TREQR0	R/W	00000000 00000000
100003H				
100004H	Transmit cancel register	TCANR0	W	00000000 00000000
100005H				
100006H	Transmit complete register	TCR0	R/W	00000000 00000000
100007H				
100008H	Receive complete register	RCR0	R/W	00000000 00000000
100009H				
10000AH	Remote request receiving register	RRTRR0	R/W	00000000 00000000
10000BH				
10000CH	Receive overrun register	ROVRR0	R/W	00000000 00000000
10000DH				
10000EH	Receive interrupt enable register	RIER0	R/W	00000000 00000000
10000FH				
100010H	Control status register	CSR0	R/W, R	00---000 0----0-1
100011H				
100012H	Last event indicator register	LEIR0	R/W	-------- 000-0000
100013H				
100014H	Receive/transmit error counter	RTEC0	R	00000000 00000000
100015H				
100016H	Bit timing register	BTR0	R/W	-1111111 11111111
100017H				
100018H	IDE register	IDER0	R/W	XXXXXXXX XXXXXXXX
100019H				

List of Control Registers (2)

Address CAN0	Register	Abbreviation	Access	Initial Value
10001AH	Transmit RTR register	TRTRR0	R/W	00000000 00000000
10001BH				
10001CH	Remote frame receive waiting register	RFWTR0	R/W	XXXXXXXX XXXXXXXX
10001DH				
10001EH	Transmit interrupt enable register	TIER0	R/W	00000000 00000000
10001FH				
100020H	Acceptance mask select register	AMSR0	R/W	XXXXXXXX XXXXXXXX
100021H				
100022H				XXXXXXXX XXXXXXXX
100023H				
100024H	Acceptance mask register 0	AMR00	R/W	XXXXXXXX XXXXXXXX
100025H				
100026H				XXXXX - - - XXXXXXXX
100027H				
100028H	Acceptance mask register 1	AMR10	R/W	XXXXXXXX XXXXXXXX
100029H				
10002AH				XXXXX - - - XXXXXXXX
10002BH				

(2) Message Buffers

List of Message Buffers (ID Registers) (1)

Address CAN0	Register	Abbreviation	Access	Initial Value
10002CH to 10004BH	General-purpose RAM	—	R/W	XXXXXXXX to XXXXXXXX
10004CH	ID register 0	IDR00	R/W	XXXXXXXX XXXXXXXX
10004DH				
10004EH				XXXXX - - - XXXXXXXX
10004FH				
100050H	ID register 1	IDR10	R/W	XXXXXXXX XXXXXXXX
100051H				
100052H				XXXXX - - - XXXXXXXX
100053H				
100054H	ID register 2	IDR20	R/W	XXXXXXXX XXXXXXXX
100055H				
100056H				XXXXX - - - XXXXXXXX
100057H				
100058H	ID register 3	IDR30	R/W	XXXXXXXX XXXXXXXX
100059H				
10005AH				XXXXX - - - XXXXXXXX
10005BH				
10005CH	ID register 4	IDR40	R/W	XXXXXXXX XXXXXXXX
10005DH				
10005EH				XXXXX - - - XXXXXXXX
10005FH				
100060H	ID register 5	IDR50	R/W	XXXXXXXX XXXXXXXX
100061H				
100062H				XXXXX - - - XXXXXXXX
100063H				
100064H	ID register 6	IDR60	R/W	XXXXXXXX XXXXXXXX
100065H				
100066H				XXXXX - - - XXXXXXXX
100067H				

List of Message Buffers (ID Registers) (2)

Address CAN0	Register	Abbreviation	Access	Initial Value
100068H	ID register 7	IDR70	R/W	XXXXXXXX XXXXXXXX
100069H				
10006AH				XXXXX - - - XXXXXXXX
10006BH				
10006CH	ID register 8	IDR80	R/W	XXXXXXXX XXXXXXXX
10006DH				
10006EH				XXXXX - - - XXXXXXXX
10006FH				
100070H	ID register 9	IDR90	R/W	XXXXXXXX XXXXXXXX
100071H				
100072H				XXXXX - - - XXXXXXXX
100073H				
100074H	ID register 10	IDR10	R/W	XXXXXXXX XXXXXXXX
100075H				
100076H				XXXXX - - - XXXXXXXX
100077H				
100078H	ID register 11	IDR11	R/W	XXXXXXXX XXXXXXXX
100079H				
10007AH				XXXXX - - - XXXXXXXX
10007BH				
10007CH	ID register 12	IDR12	R/W	XXXXXXXX XXXXXXXX
10007DH				
10007EH				XXXXX - - - XXXXXXXX
10007FH				
100080H	ID register 13	IDR13	R/W	XXXXXXXX XXXXXXXX
100081H				
100082H				XXXXX - - - XXXXXXXX
100083H				
100084H	ID register 14	IDR14	R/W	XXXXXXXX XXXXXXXX
100085H				
100086H				XXXXX - - - XXXXXXXX
100087H				

List of Message Buffers (ID Registers) (3)

Address CAN0	Register	Abbreviation	Access	Initial Value
100088H	ID register 15	IDR15	R/W	XXXXXXXX XXXXXXXX
100089H				
10008AH				XXXXX--- XXXXXXXX
10008BH				

List of Message Buffers (DLC Registers and Data Registers) (1)

Address CAN0	Register	Abbreviation	Access	Initial Value
10008CH	DLC register 0	DLCR00	R/W	----XXXX
10008DH				
10008EH	DLC register 1	DLCR10	R/W	----XXXX
10008FH				
100090H	DLC register 2	DLCR20	R/W	----XXXX
100091H				
100092H	DLC register 3	DLCR30	R/W	----XXXX
100093H				
100094H	DLC register 4	DLCR40	R/W	----XXXX
100095H				
100096H	DLC register 5	DLCR50	R/W	----XXXX
100097H				
100098H	DLC register 6	DLCR60	R/W	----XXXX
100099H				
10009AH	DLC register 7	DLCR70	R/W	----XXXX
10009BH				
10009CH	DLC register 8	DLCR80	R/W	----XXXX
10009DH				
10009EH	DLC register 9	DLCR90	R/W	----XXXX
10009FH				
1000A0H	DLC register 10	DLCR100	R/W	----XXXX
1000A1H				

List of Message Buffers (DLC Registers and Data Registers) (2)

Address CAN0	Register	Abbreviation	Access	Initial Value
1000A2H	DLC register 11	DLCR110	R/W	----XXXX
1000A3H				
1000A4H	DLC register 12	DLCR120	R/W	----XXXX
1000A5H				
1000A6H	DLC register 13	DLCR130	R/W	----XXXX
1000A7H				
1000A8H	DLC register 14	DLCR140	R/W	----XXXX
1000A9H				
1000AAH	DLC register 15	DLCR150	R/W	----XXXX
1000ABH				
1000ACH to 1000B3H	Data register 0 (8 bytes)	DTR00	R/W	XXXXXXXX to XXXXXXXX
1000B4H to 1000BBH	Data register 1 (8 bytes)	DTR10	R/W	XXXXXXXX to XXXXXXXX
1000BCH to 1000C3H	Data register 2 (8 bytes)	DTR20	R/W	XXXXXXXX to XXXXXXXX
1000C4H to 1000CBH	Data register 3 (8 bytes)	DTR30	R/W	XXXXXXXX to XXXXXXXX
1000CCH to 1000D3H	Data register 4 (8 bytes)	DTR40	R/W	XXXXXXXX to XXXXXXXX
1000D4H to 1000DBH	Data register 5 (8 bytes)	DTR50	R/W	XXXXXXXX to XXXXXXXX
1000DCH to 1000E3H	Data register 6 (8 bytes)	DTR60	R/W	XXXXXXXX to XXXXXXXX
1000E4H to 1000EBH	Data register 7 (8 bytes)	DTR70	R/W	XXXXXXXX to XXXXXXXX
1000ECH to 1000F3H	Data register 8 (8 bytes)	DTR80	R/W	XXXXXXXX to XXXXXXXX
1000F4H to 1000FBH	Data register 9 (8 bytes)	DTR90	R/W	XXXXXXXX to XXXXXXXX

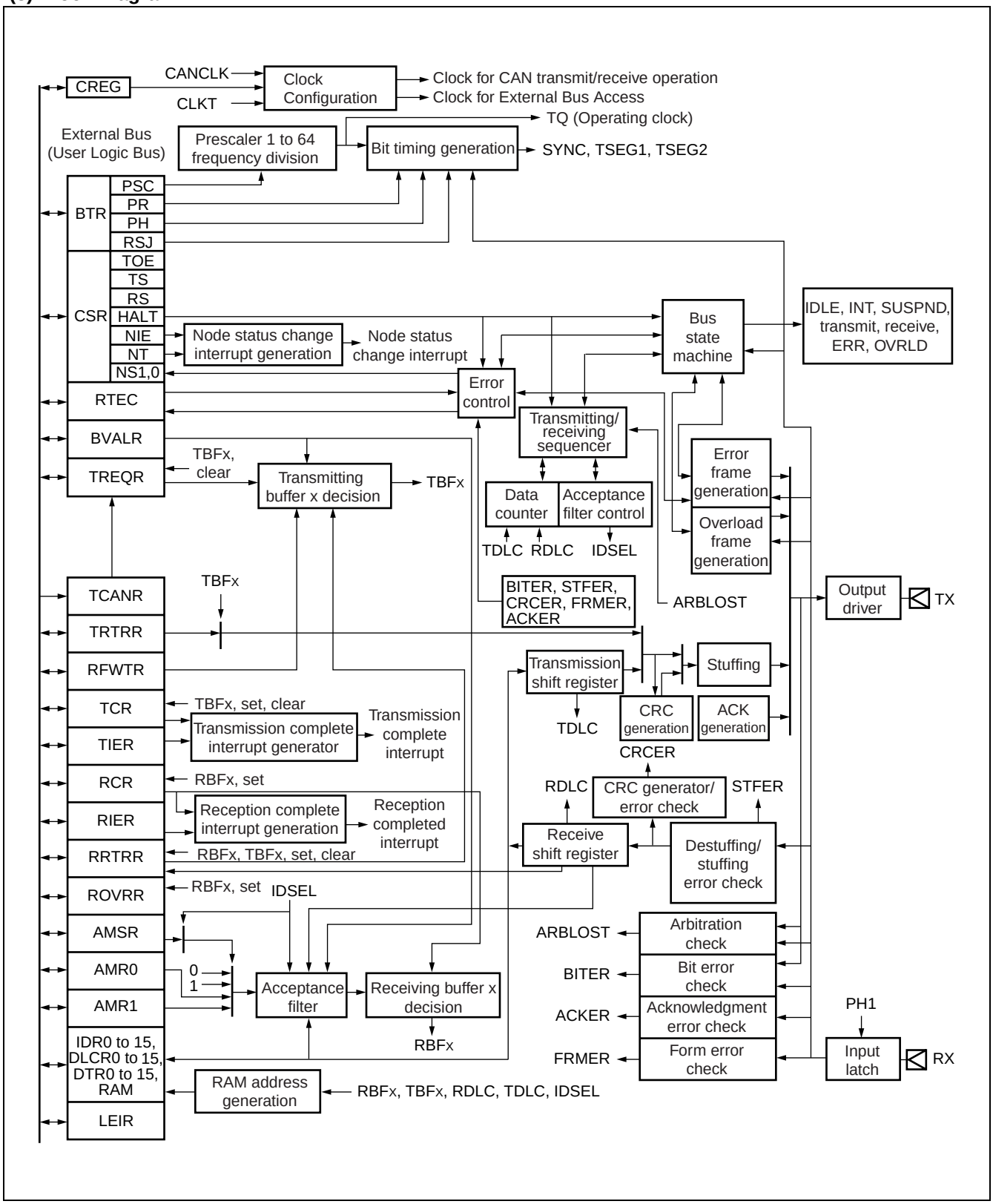
List of Message Buffers (DLC Registers and Data Registers) (3)

Address CAN0	Register	Abbreviation	Access	Initial Value
1000FC$_H$ to 100103$_H$	Data register 10 (8 bytes)	DTR100	R/W	XXXXXXXX to XXXXXXXX
100104$_H$ to 10010B$_H$	Data register 11 (8 bytes)	DTR110	R/W	XXXXXXXX to XXXXXXXX
10010C$_H$ to 100113$_H$	Data register 12 (8 bytes)	DTR120	R/W	XXXXXXXX to XXXXXXXX
100114$_H$ to 10011B$_H$	Data register 13 (8 bytes)	DTR130	R/W	XXXXXXXX to XXXXXXXX
10011C$_H$ to 100123$_H$	Data register 14 (8 bytes)	DTR140	R/W	XXXXXXXX to XXXXXXXX
100124$_H$ to 10012B$_H$	Data register 15 (8 bytes)	DTR150	R/W	XXXXXXXX to XXXXXXXX

Configuration Register (CREG)

Address CAN0	Register	Abbreviation	Access	Initial Value
10012C$_H$ 10012D$_H$	Configuration register	CREG0	R/W	00000000 00000110

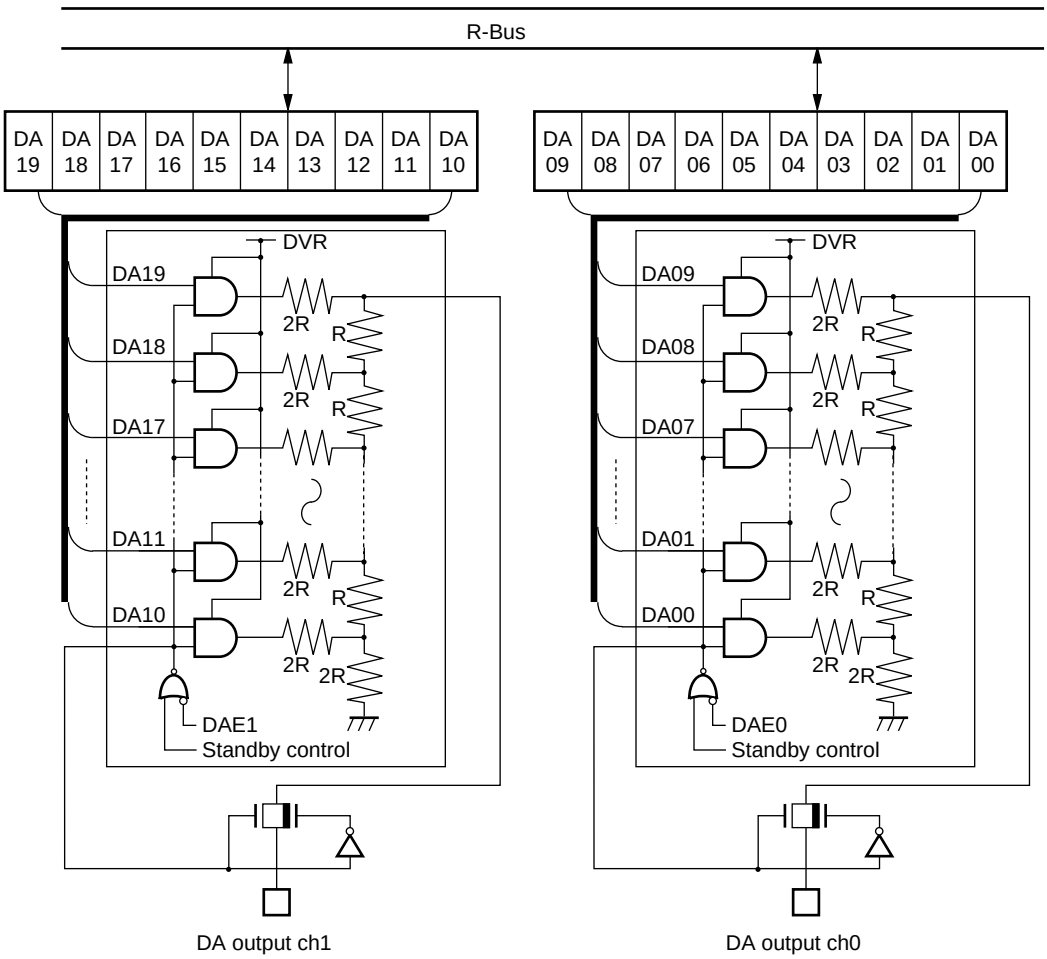
(3) Block Diagram



18. D/A CONVERTER

This section provides an overview of the D/A converter, describes the register structure and functions, and describes the operarton of D/A converter.This block is an R-2R format D/A converter, having ten-bit resolution. The D/A converter has two channels.Output control can be performed independently for the two channels using the D/A control register.

(1) Block Diagram



(2) Registers

D/A control register (DACR)

bit	7	6	5	4	3	2	1	0
Address : 0000A5H	—	—	—	—	—	MODE	DAE1	DAE0

D/A converter data register (ch 0) (DADR0)

bit	15	14	13	12	11	10	9	8
Address : 0000A6H	—	—	—	—	—	—	DA09	DA08

bit	7	6	5	4	3	2	1	0
Address : 0000A7H	DA07	DA06	DA05	DA04	DA03	DA02	DA01	DA00

D/A converter data register (ch 1) (DADR1)

bit	15	14	13	12	11	10	9	8
Address : 0000A8H	—	—	—	—	—	—	DA19	DA18

bit	7	6	5	4	3	2	1	0
Address : 0000A9H	DA17	DA16	DA15	DA14	DA13	DA12	DA11	DA10

D/A clock control (DDBL)

bit	7	6	5	4	3	2	1	0
Address : 0000ABH	—	—	—	—	—	—	—	DBL

19. 100 kHz I²C INTERFACE

This section describes the functions and operation of the MB91360G series basic I²C interface. This interface allows operation up to 100 kHz and 8-bit-addressing.

The I²C interface is a serial I/O port supporting the Inter IC bus, operating as a master/slave device on the I²C bus.

(1) I²C Interface Features

The MB91360G series microcontroller includes a built-in one-channel I²C interface. The I²C interface has the following features.

- Master/slave sending and receiving functions
- Arbitration function
- Clock synchronization function
- Slave address/general call address detection function
- Transfer direction detection function
- Repeated start condition generation and detection function
- Bus error detection function

(2) I²C Interface Registers

a : Bus Status Register (IBSR)

Bit no.	7	6	5	4	3	2	1	0
Address: 000095H	BB	RSC	AL	LRB	TRX	AAS	GCA	FBT
Read/write ⇨	(R)	(R)	(R)	(R)	(R)	(R)	(R)	(R)
Default value ⇨	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

b : Bus Control Register (IBCR)

Bit no.	15	14	13	12	11	10	9	8
Address: 000094H	BER	BEIE	SCC	MSS	ACK	GCAA	INTE	INT
Read/write ⇨	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
Default value ⇨	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

c : Clock control register (ICCR)

Bit no.	7	6	5	4	3	2	1	0
Address: 000097H	—	—	EN	CS4	CS3	CS2	CS1	CS0
Read/write ⇨	(—)	(—)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
Default value ⇨	(—)	(—)	(0)	(X)	(X)	(X)	(X)	(X)

d : Address Register (IADR)

Bit no.	15	14	13	12	11	10	9	8
Address: 000096H	—	A6	A5	A4	A3	A2	A1	A0
Read/write ⇨	(—)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
Default value ⇨	(—)	(X)	(X)	(X)	(X)	(X)	(X)	(X)

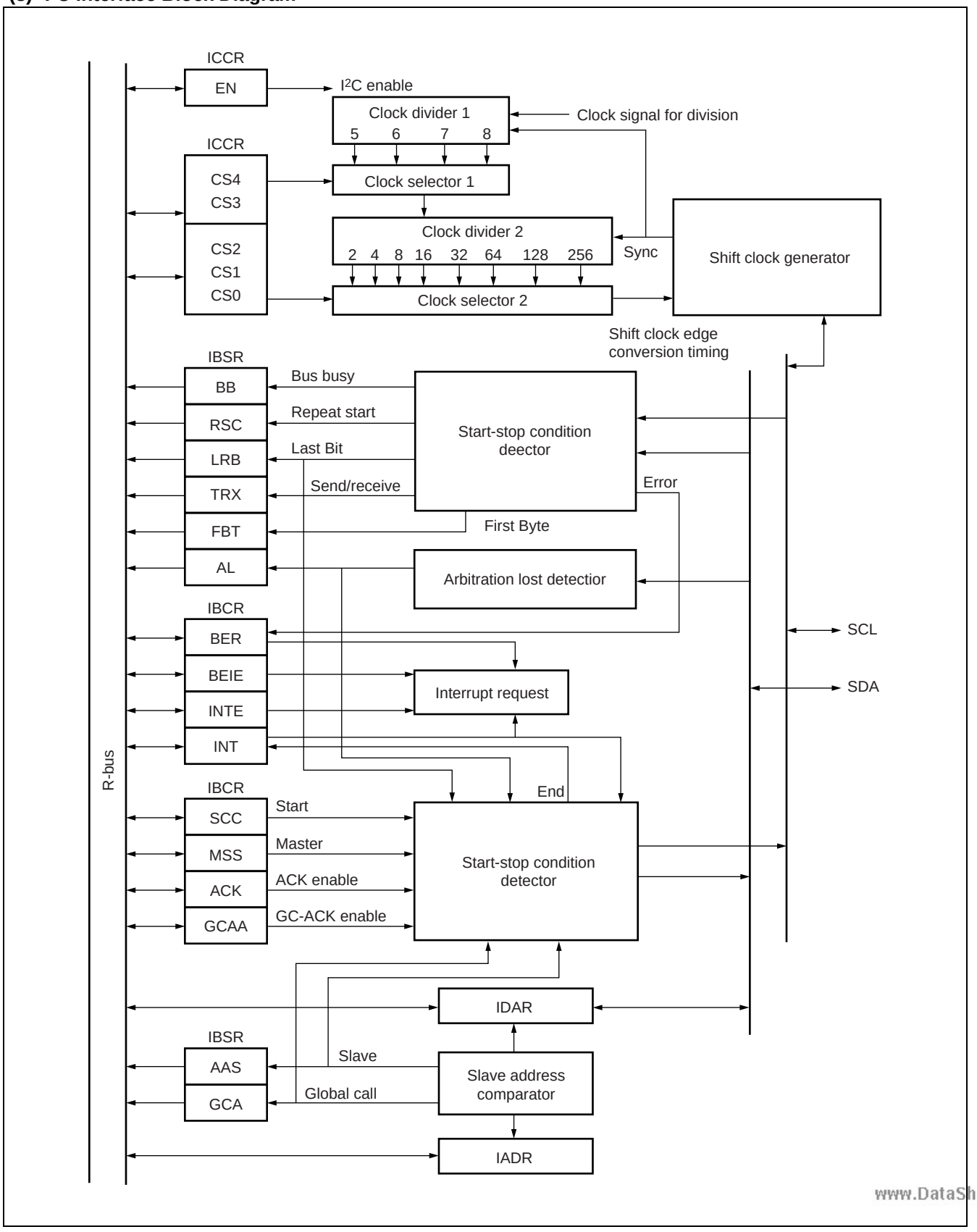
e : Data Register (IDAR)

Bit no.	7	6	5	4	3	2	1	0
Address: 000099H	D7	D6	D5	D4	D3	D2	D1	D0
Read/write ⇨	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
Default value ⇨	(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)

f : Clock Disable Register (IDBL)

Bit no.	7	6	5	4	3	2	1	0
Address: 00009BH	—	—	—	—	—	—	—	DBL
Read/write ⇨	(—)	(—)	(—)	(—)	(—)	(—)	(—)	(R/W)
Default value ⇨	(—)	(—)	(—)	(—)	(—)	(—)	(—)	(0)

(3) I²C Interface Block Diagram



20. 400 kHz I²C INTERFACE

This section describes the functions and operation of the fast I²C interface.

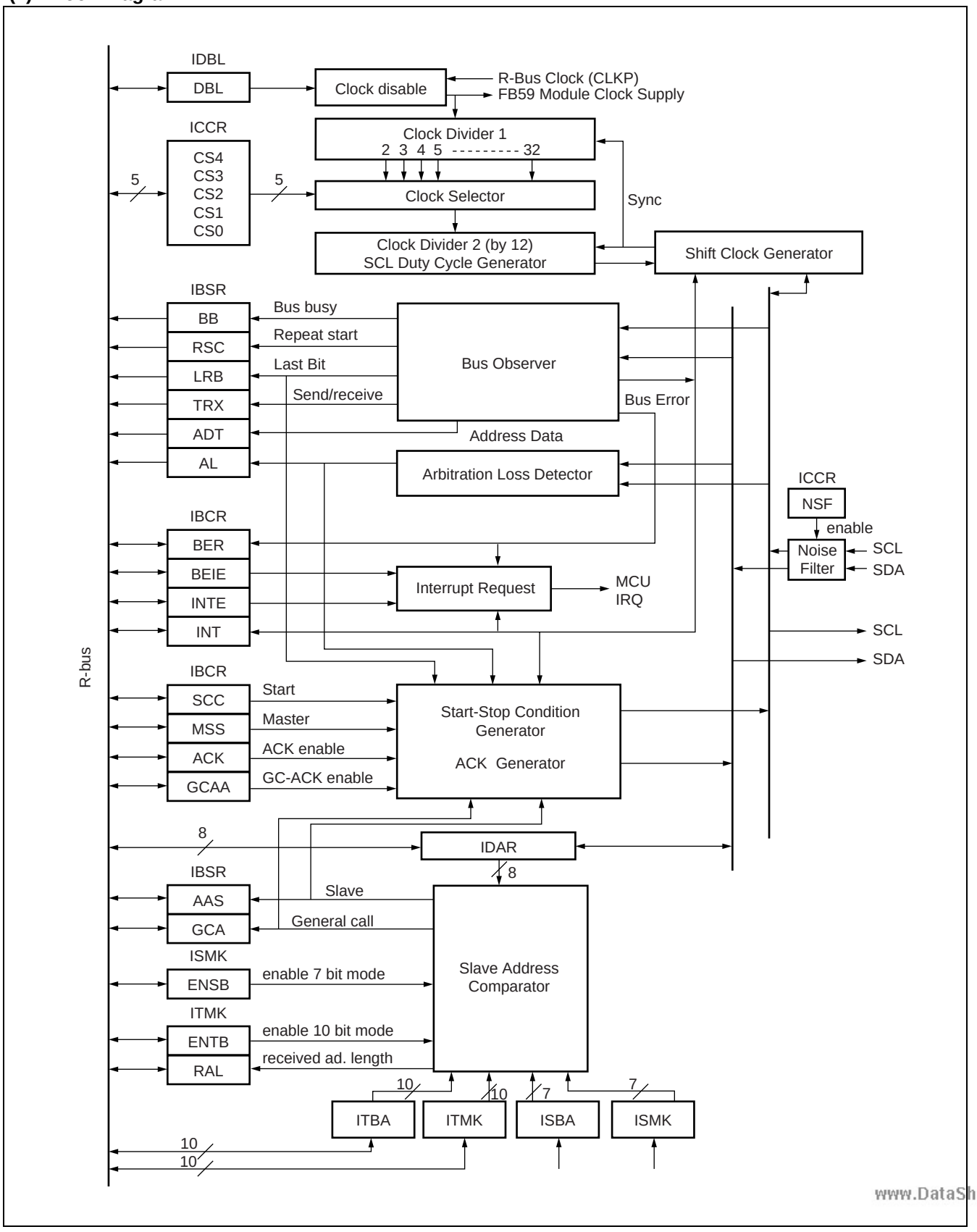
The I²C interface is a serial I/O port supporting the Inter IC bus, operating as a master/slave device on the I²C bus.

(1) Features

- Master/slave transmitting and receiving functions
- Arbitration function
- Clock synchronization function
- General call addressing support
- Transfer direction detection function
- Repeated start condition generation and detection function
- Bus error detection function
- 7 bit addressing as master and slave
- 10 bit addressing as master and slave
- Possibility to give the interface a seven and a ten bit slave address
- Acknowledging upon slave address reception can be disabled (Master-only operation)
- Address masking to give interface several slave addresses (in 7 and 10 bit mode)
- Up to 400 KBit transfer rate
- Possibility to use built-in noise filters for SDA and SCL
- Can receive data at 400 KBit if R-Bus-Clock is higher than 6 MHz regardless of prescaler setting
- Can generate MCU interrupts on transmission and bus error events
- Supports being slowed down by a slave on bit and byte level

The I²C interface does not support SCL clock stretching on bit level since it can receive the full 400 KBit datarate if the R-Bus-Clock (CLKP) is higher than 6 MHz regardless of the prescaler setting. However, clock stretching on byte level is performed since SCL is pulled low during an interrupt (INT = “1” in IBCR register) .

(2) Block Diagram



(3) I²C Interface Registers

a : Bus Control Register (IBCR2)

	15	14	13	12	11	10	9	8	⇦ Bit no.
Address: 000184H	BER	BEIE	SCC	MSS	ACK	GCAA	INTE	INT	
Read/write ⇨	(R/W)	(R/W)	(W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Default value ⇨	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	

b : Bus Status Register (IBSR2)

	7	6	5	4	3	2	1	0	⇦ Bit no.
Address: 000185H	BB	RSC	AL	LRB	TRX	AAS	GCA	FBT	
Read/write ⇨	(R)	(R)	(R)	(R)	(R)	(R)	(R)	(R)	
Default value ⇨	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	

c : Ten Bit slave Address register (ITBAH, ITBAL)

Ten Bit Address high byte

	15	14	13	12	11	10	9	8	⇦ Bit no.
Address: 000186H	—	—	—	—	—	—	TA9	TA8	
Read/write ⇨	(—)	(—)	(—)	(—)	(—)	(—)	(R/W)	(R/W)	
Default value ⇨	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	

Ten Bit Address low byte

	7	6	5	4	3	2	1	0	⇦ Bit no.
Address: 000187H	TA7	TA6	TA5	TA4	TA3	TA2	TA1	TA0	
Read/write ⇨	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Default value ⇨	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	

d : Ten bit slave address Mask register (ITMKH, ITMKL)

Ten Bit Address Mask high byte

	15	14	13	12	11	10	9	8	⇦ Bit no.
Address: 000188H	ENTB	RAL	—	—	—	—	TM9	TM8	
Read/write ⇨	(R/W)	(R)	(—)	(—)	(—)	(—)	(R/W)	(R/W)	
Default value ⇨	(0)	(0)	(1)	(1)	(1)	(1)	(1)	(1)	

Ten Bit Address Mask low byte

	7	6	5	4	3	2	1	0	⇦ Bit no.
Address: 000189H	TM7	TM6	TM5	TM4	TM3	TM2	TM1	TM0	
Read/write ⇨	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Default value ⇨	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)	

e : Seven Bit slave Address register (ISBA)

	7	6	5	4	3	2	1	0	⇦ Bit no.
Address: 00018BH	—	SA6	SA5	SA4	SA3	SA2	SA1	SA0	
Read/write ⇨	(—)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Default value ⇨	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	

(Continued)

(Continued)

f : Seven bit slave address Mask register (ISMK)

	15	14	13	12	11	10	9	8	⇦ Bit no.
Address : 00018A$_H$	ENSB	SM6	SM5	SM4	SM3	SM2	SM1	SM0	
Read/write ⇨	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Default value ⇨	(0)	(1)	(1)	(1)	(1)	(1)	(1)	(1)	

g : Data Register (IDARH, IDAR2)

Data register high byte

	15	14	13	12	11	10	9	8	⇦ Bit no.
Address : 00018C$_H$	—	—	—	—	—	—	—	—	
Read/write ⇨	(—)	(—)	(—)	(—)	(—)	(—)	(—)	(—)	
Default value ⇨	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	

Data register

	7	6	5	4	3	2	1	0	⇦ Bit no.
Address : 00018D$_H$	D7	D6	D5	D4	D3	D2	D1	D0	
Read/write ⇨	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Default value ⇨	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	

h : Clock control register (ICCR2)

	15	14	13	12	11	10	9	8	⇦ Bit no.
Address : 00018E$_H$	—	NSF	EN	CS4	CS3	CS2	CS1	CS0	
Read/write ⇨	(—)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Default value ⇨	(0)	(0)	(0)	(1)	(1)	(1)	(1)	(1)	

i : Clock Disable Register (IDBL2)

	7	6	5	4	3	2	1	0	⇦ Bit no.
Address : 00018F$_H$	—	—	—	—	—	—	—	DBL	
Read/write ⇨	(—)	(—)	(—)	(—)	(—)	(—)	(—)	(R/W)	
Default value ⇨	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	

21. 16-BIT I/O TIMER

The MB91360G Series contains two 16-bit free-running timer modules, two output compare modules, and two input capture modules and supports four input channels and four output channels. The following sections only describes the 16-bit free-running timer, Output Compare 0/1 and Input Capture 0/1.
The remaining modules have the identical functions and the register addresses should be found in the I/O map.

(1) Function Overview

a : 16-bit free-running timer

The 16-bit free-run timer consists of a 16-bit up counter, control register, and prescaler. The values output from this timer counter are used as the base timer for input capture and output compare.

- Four counter clocks are available.
  Internal clock : ϕ/4, ϕ/16, ϕ/32, ϕ/64
- An interrupt can be generated upon a counter overflow or a match with compare register 0.
- The counter value can be initialized to “0000H” upon a reset, software clear, or match with compare register 0.

b : Output compare (2 channels per one module)

The output compare module consists of two 16-bit compare registers, compare output latch, and control register.

When the 16-bit free-running timer value matches the compare register value, the output level is reversed and an interrupt is issued.

- The two compare registers can be used independently.
  Output pins and interrupt flags corresponding to compare registers
- Output pins can be controlled based on pairs of the two compare registers.
  Output pins can be reversed by using the two compare registers.
- Initial values for output pins can be set.
- Interrupts can be generated upon a compare match.

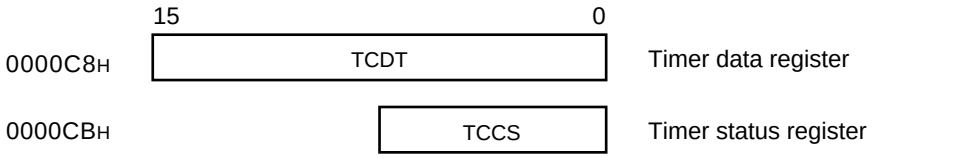
c : Input capture (2 channels per one module)

The input capture module consists of two 16-bit capture registers and control registers corresponding to two independent external input pins. The 16-bit free-running timer value can be stored in the capture register and an interrupt is issued simultaneously upon detection of an edge of a signal input from an external input pin.

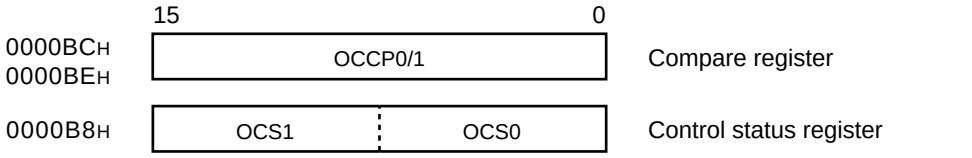
- The detection edge of an external input signal can be specified.
  Rising, falling, or both edges
- Two input channels can operate independently.
- An interrupt can be issued upon a valid edge of an external input signal.

(2) Registers

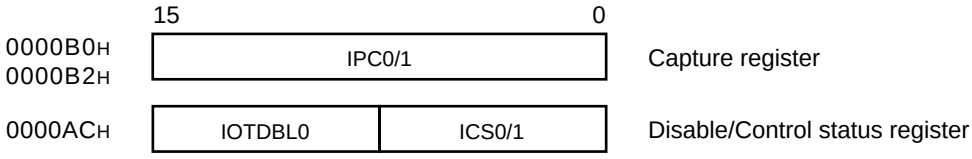
a : 16-bit free-running timer



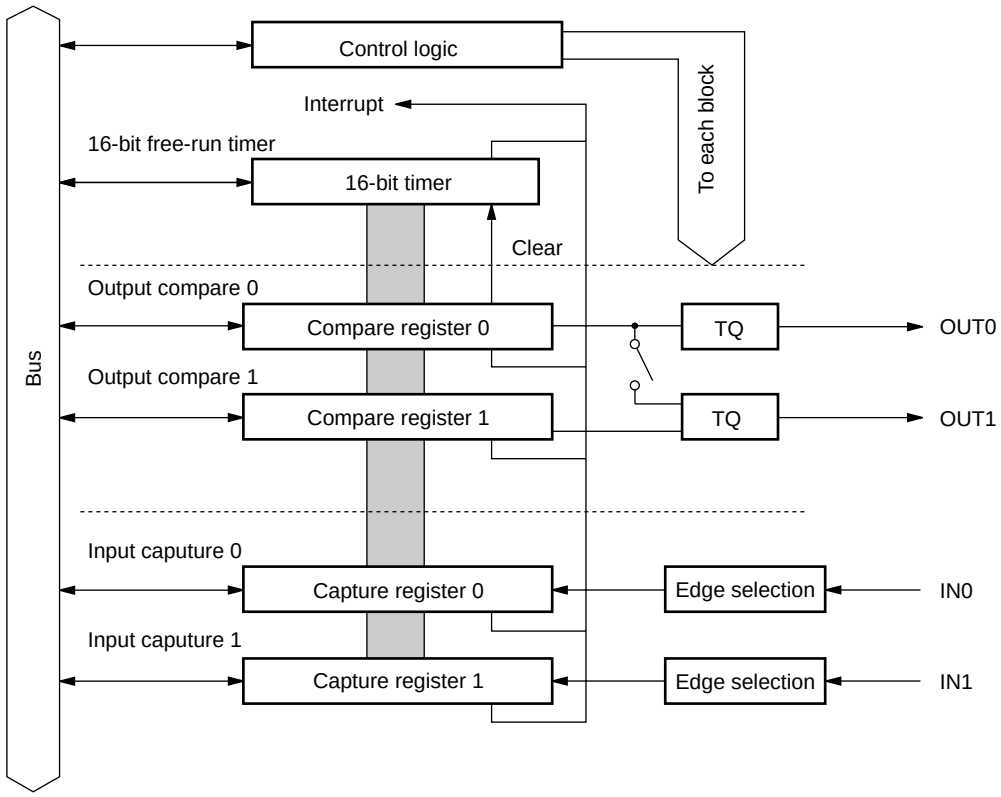
b : 16-bit output compare



c : 16-bit input capture



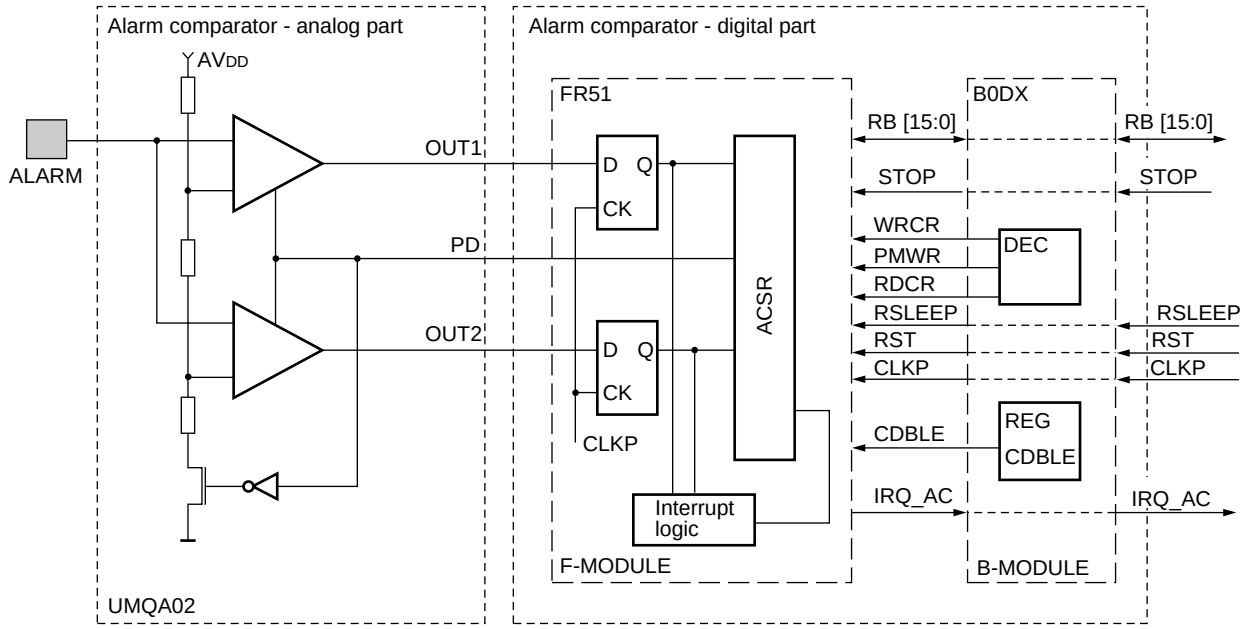
(3) Block Diagram



22. ALARM COMPARATOR

This section provides an overview of the Alarm Comparator (Also called Under/Overvoltage Detection) , describes the register structure and functions, and describes the operation of the Alarm Comparator.

(1) Block Diagram



(2) Registers

Alarm Comparator Clock Disable Register (ACCDBL)

Address	Bits	7	6	5	4	3	2	1	0	Initial value
00000180H		—	—	—	—	—	—	—	CDBLE	- - - - - - - 0B
									R/W	← Access

Alarm Comparator Status Disable Register (ACSR)

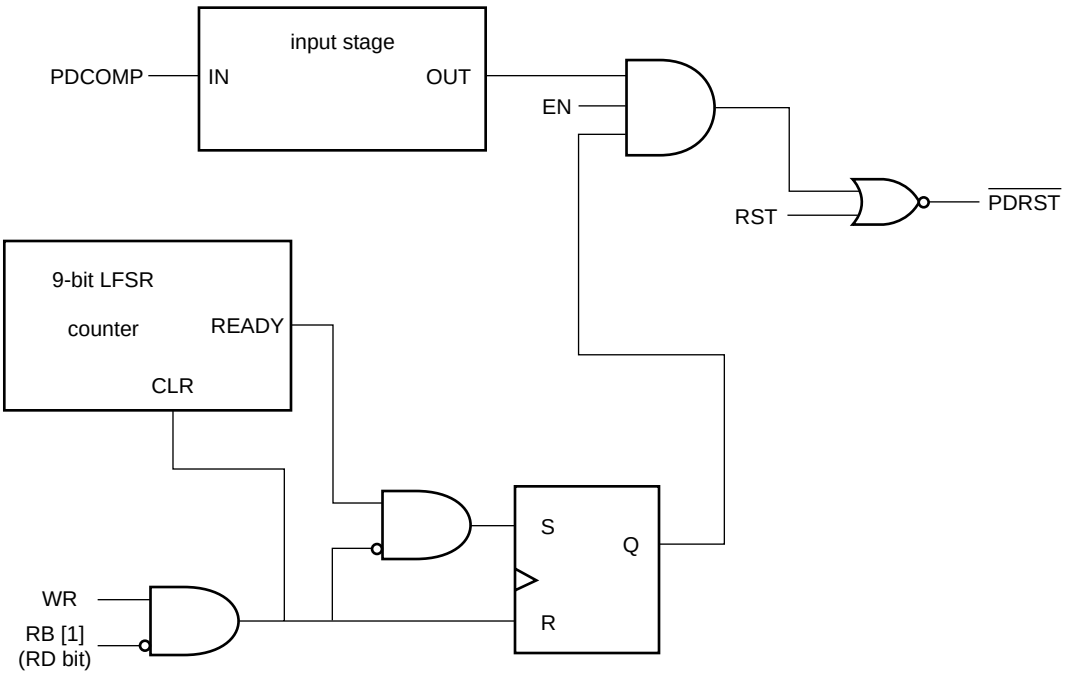
Address	Bits	7	6	5	4	3	2	1	0	Initial value
00000181H		—	OV_EN	UV-EN	OUT2	OUT1	IRQ	IEN	PD	-11xxx00B
			R/W	R/W	R	R	R/W	R/W	R/W	← Access

23. POWER DOWN RESET

This section provides an overview of the Power Down Reset, describes the register structure and functions, and describes the operation of the Power Down Reset Module.

The power down reset module performs a system reset when V_{CC} goes below a threshold voltage. The reset signal is be disabled and enabled by setting the power down reset control register PDRCR. For low power applications the digital and the analog part of the power down reset control circuit can be disabled.

(1) Block Diagram



(2) Register

	7	6	5	4	3	2	1	0
PDRCR	—	—	—	—	—	CDSBLE	PD	EN
access	—	—	—	—	—	R/W	R/W	R/W
initial value (INIT)	—	—	—	—	—	0	0	0
initial value (RST)	X	X	X	X	X	X	X	X

24. SERIAL I/O INTERFACE (SIO)

This section provides an overview of the Serial I/O Interface (SIO) , describes the register structure and functions, and describes the operation of the SIO.

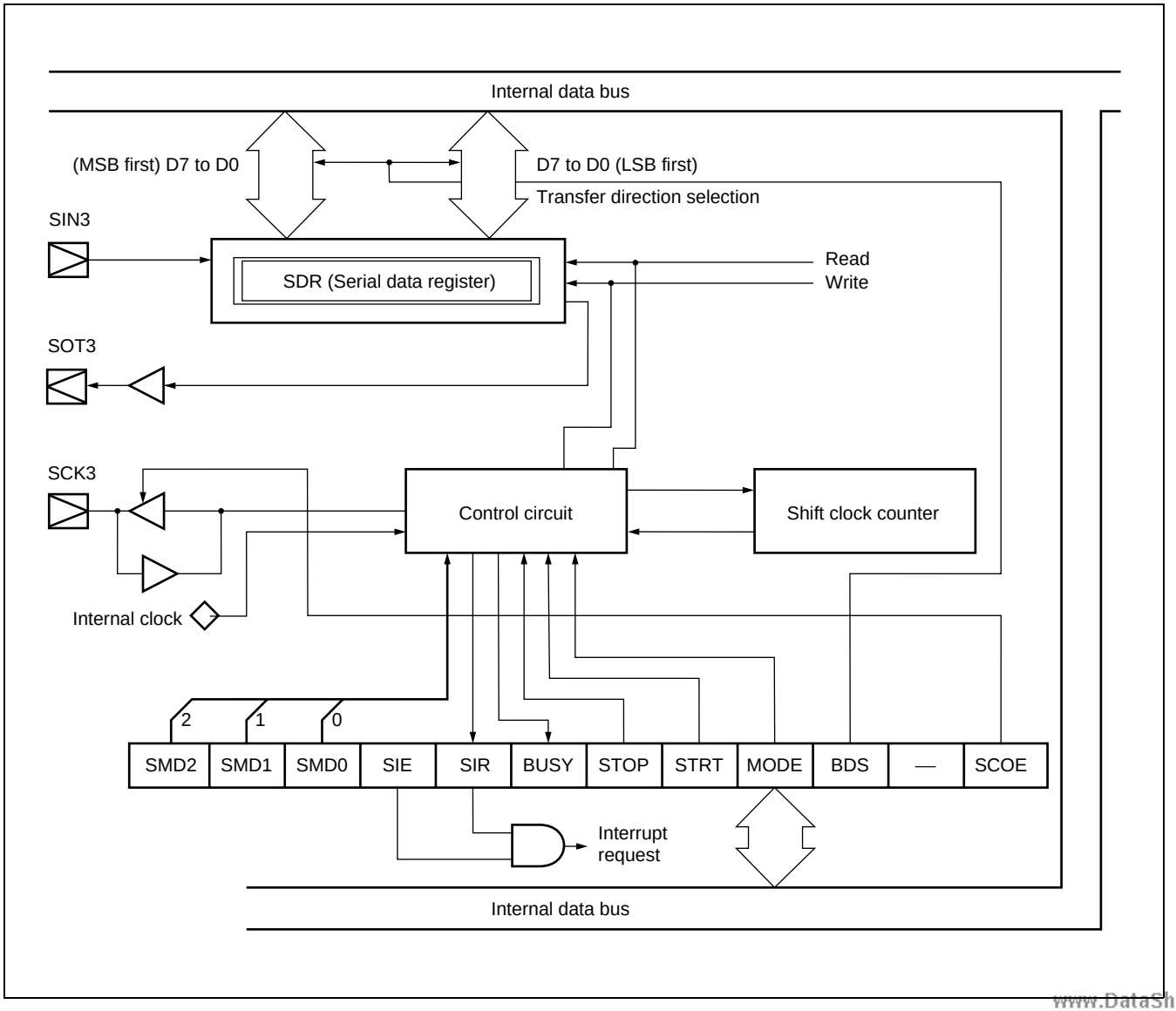
(1) Block Diagram

This block is a serial I/O interface that allows data transfer using clock synchronization. The interface consists of a single eight-bit channel. Data can be transferred from the LSB or MSB.

MB91360G series contains two Serial I/O units SIO0 and SIO1. This section only describes SIO0. Please see the IO-Map for the register addresses of SIO1.

The serial I/O interface operates in two modes :

- Internal shift clock mode : Data is transferred in synchronization with the internal clock.
- External shift clock mode : Data is transferred in synchronization with the clock supplied via the external pin (SCK) . By manipulating the general-purpose port sharing the external pin (SCK) , data can also be transferred by a CPU instruc tion in this mode.



(2) Registers

Serial mode control status register (SMCS)

Address : 000084H

15	14	13	12	11	10	9	8
SMD2	SMD1	SMD0	SIE	SIR	BUSY	STOP	STRT

Address : 000085H

7	6	5	4	3	2	1	0
—	—	—	—	MODE	BDS	—	SCOE

SIO edge selection/clock disable register (SES)

Address : 000086H

15	14	13	12	11	10	9	8
—	—	—	—	—	—	DBL	NEG

Serial data register (SDR)

Address : 000087H

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

25. SOUND GENERATOR

This section provides an overview of the Sound Generator, describes the register structure and functions, and describe the operation of the Sound Generator.

The Sound Generator consists of the Sound Control register, Frequency Data register, Amplitude Data register, Decrement Grade register, Tone Count register, Sound Disable register, PWM pulse generator, Frequency counter, Decrement counter and Tone Pulse counter.

(1) Registers

Sound Control register (SGCR)

	7	6	5	4	3	2	1	0	⇦ Bit no.
Address: 0000EF$_H$	S1	S0	TONE	—	—	INTE	INT	ST	
Read/write ⇨	(R/W)	(R/W)	(R/W)	(—)	(—)	(R/W)	(R/W)	(R/W)	
Default value ⇨	(0)	(0)	(0)	(—)	(—)	(0)	(0)	(0)	

	15	14	13	12	11	10	9	8	⇦ Bit no.
Address: 0000EE$_H$	TST	—	—	—	—	—	BUSY	DEC	
Read/write ⇨	(R/W)	(—)	(—)	(—)	(—)	(—)	(R)	(R/W)	
Default value ⇨	(0)	(—)	(—)	(—)	(—)	(—)	(0)	(0)	

Frequency Data register (SGFR)

	7	6	5	4	3	2	1	0	⇦ Bit no.
Address: 0000F1$_H$	D7	D6	D5	D4	D3	D2	D1	D0	
Read/write ⇨	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Default value ⇨	(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)	

Amplitude Data register (SGAR)

	15	14	13	12	11	10	9	8	⇦ Bit no.
Address: 0000F0$_H$	D7	D6	D5	D4	D3	D2	D1	D0	
Read/write ⇨	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Default value ⇨	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	

Decrement Grade register (SGDR)

	7	6	5	4	3	2	1	0	⇦ Bit no.
Address: 0000F3$_H$	D7	D6	D5	D4	D3	D2	D1	D0	
Read/write ⇨	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Default value ⇨	(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)	

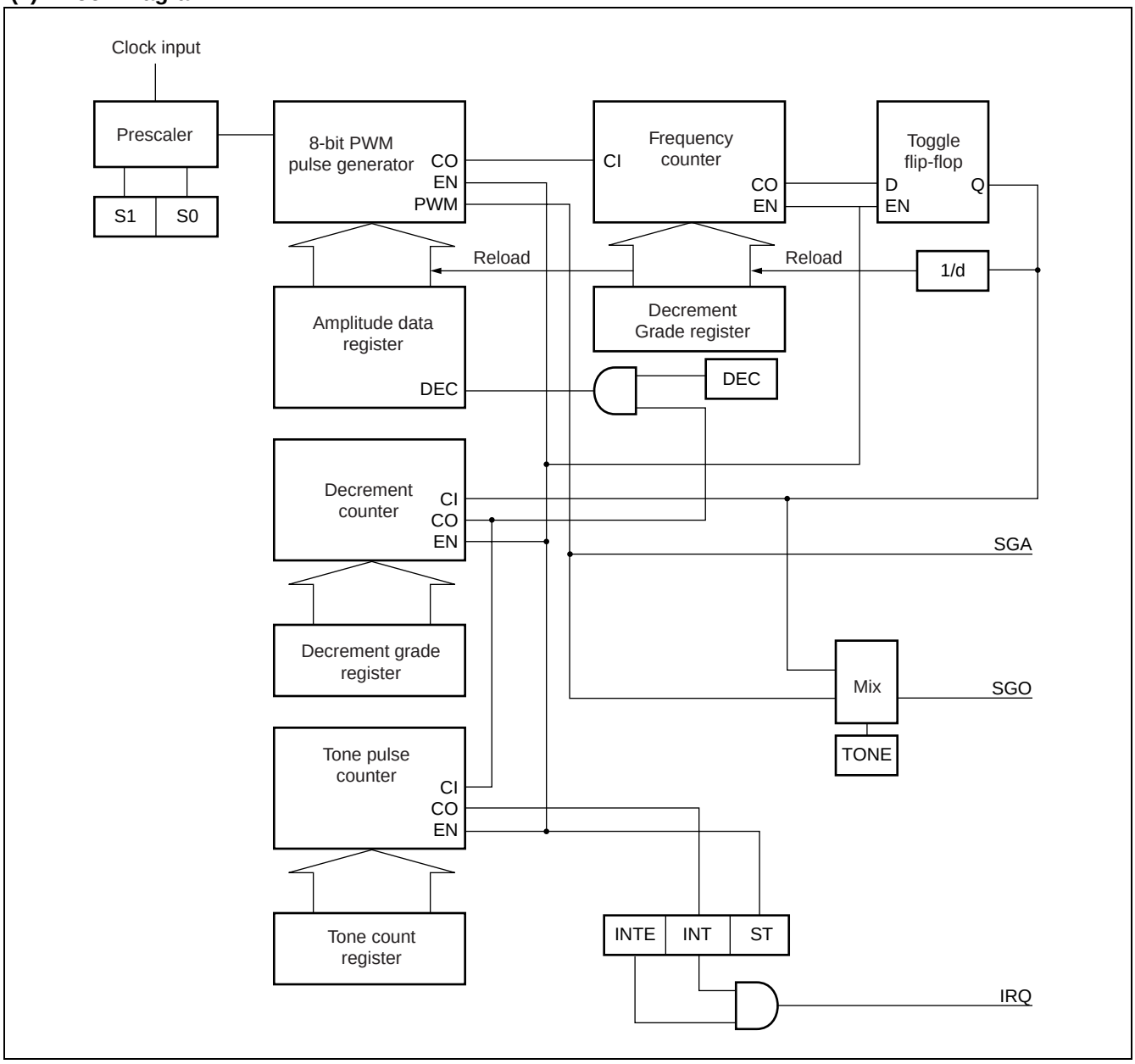
Tone Count register (SGTR)

	15	14	13	12	11	10	9	8	⇦ Bit no.
Address: 0000F2$_H$	D7	D6	D5	D4	D3	D2	D1	D0	
Read/write ⇨	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Default value ⇨	(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)	

Sound Disable register (SGDBL)

	7	6	5	4	3	2	1	0	⇦ Bit no.
Address: 0000ED$_H$	—	—	—	—	—	—	—	DBL	
Read/write ⇨	(—)	(—)	(—)	(—)	(—)	(—)	(—)	(R/W)	
Default value ⇨	(—)	(—)	(—)	(—)	(—)	(—)	(—)	(0)	

(2) Block Diagram



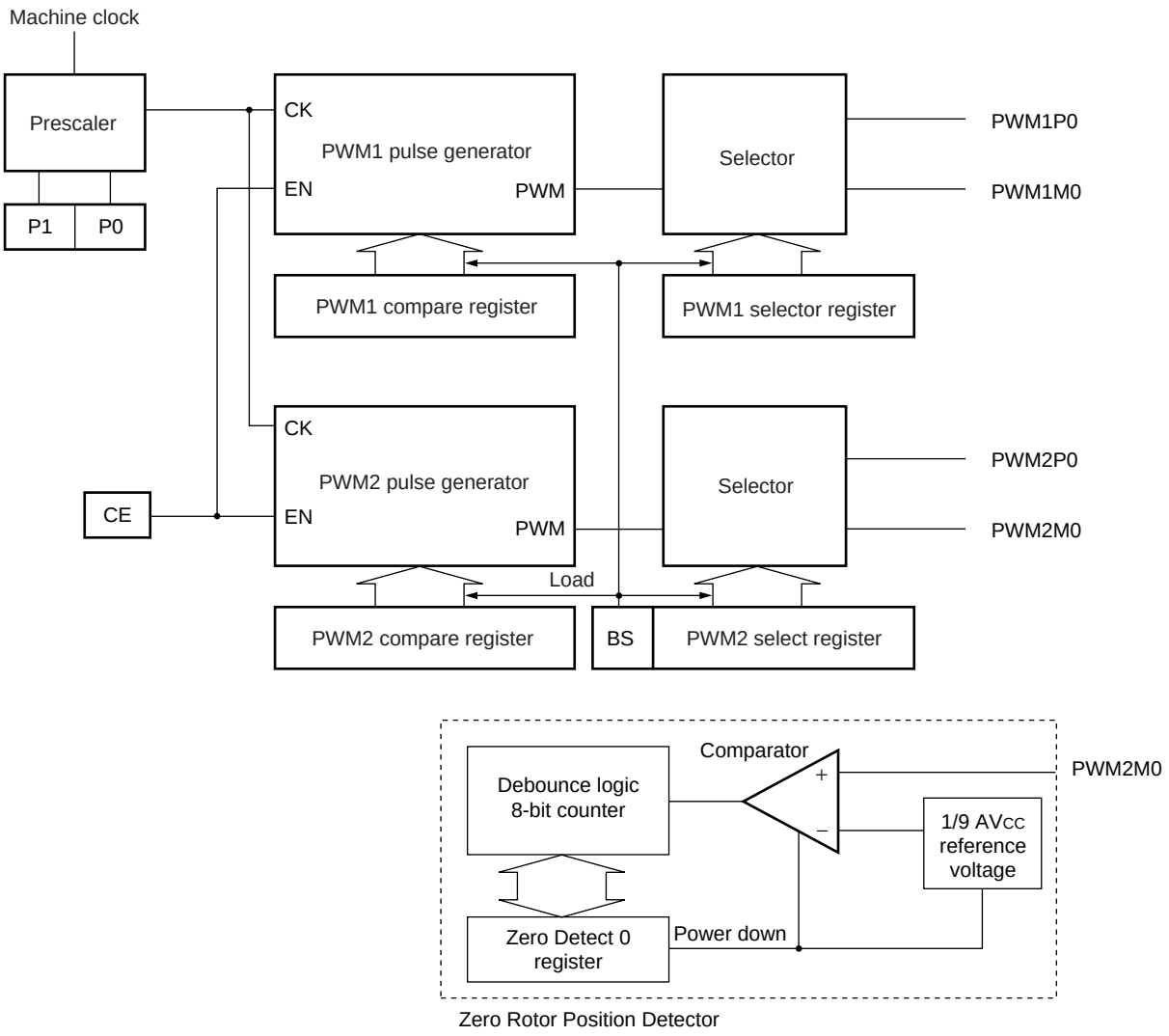
26. STEPPER MOTOR CONTROLLER

This section provides an overview of the Stepper Motor Control Module, describe the register structure and functions, and described the operation of the Stepper Motor Control Module.

The Stepping Motor Controller consists of two PWM Pulse Generators, four motor drivers, Selector Logic and the Zero Rotor Position Detector. The four motor drivers have high output drive capabilities and they can be directly connected to the four ends of two motor coils. The combination of the PWM Pulse Generators and Selector Logic is designed to control the rotation of the motor. A Synchronization mechanism assures the synchronous operations of the two PWMs. The Zero Rotor Position Detector helps CPU obtain feed back information of the rotor movements. The following sections describe the Stepping Motor Controller 0 only. The other controllers have the same functions. The register addresses are found in the I/O map.

Note : The Rotor Zero Position Detection capability is protected by a patent from Mannesmann VDO and may only be used with VDO's prior approval.

(1) Block Diagram



(2) Registers

PWM Control 0 register (PWC0)

	7	6	5	4	3	2	1	0	⇦ Bit no.
Address: 0000D1H	—	—	P1	P0	CE	—	—	TST	
Read/write ⇨	(—)	(—)	(R/W)	(R/W)	(R/W)	(—)	(—)	(R/W)	
Default value ⇨	(—)	(—)	(0)	(0)	(0)	(—)	(—)	(0)	

Zero Detect 0 register (ZPD0)

	15	14	13	12	11	10	9	8	⇦ Bit no.
Address: 0000D0H	S1	S0	TS	T2	T1	T0	PD	RS	
Read/write ⇨	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Default value ⇨	(0)	(0)	(0)	(0)	(0)	(0)	(1)	(0)	

PWM1 Compare 0 register (PWC10)

	7	6	5	4	3	2	1	0	⇦ Bit no.
Address: 0000D9H	D7	D6	D5	D4	D3	D2	D1	D0	
Read/write ⇨	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Default value ⇨	(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)	

PWM2 Compare 0 register (PWC20)

	15	14	13	12	11	10	9	8	⇦ Bit no.
Address: 0000D8H	D7	D6	D5	D4	D3	D2	D1	D0	
Read/write ⇨	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Default value ⇨	(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)	

PWM1 Select register (PWS10)

	7	6	5	4	3	2	1	0	⇦ Bit no.
Address: 0000DBH	—	—	P2	P1	P0	M2	M1	M0	
Read/write ⇨	(—)	(—)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Default value ⇨	(—)	(—)	(0)	(0)	(0)	(0)	(0)	(0)	

PWM2 Select register (PWS20)

	15	14	13	12	11	10	9	8	⇦ Bit no.
Address: 0000DAH	—	BS	P2	P1	P0	M2	M1	M0	
Read/write ⇨	(—)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Default value ⇨	(—)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	

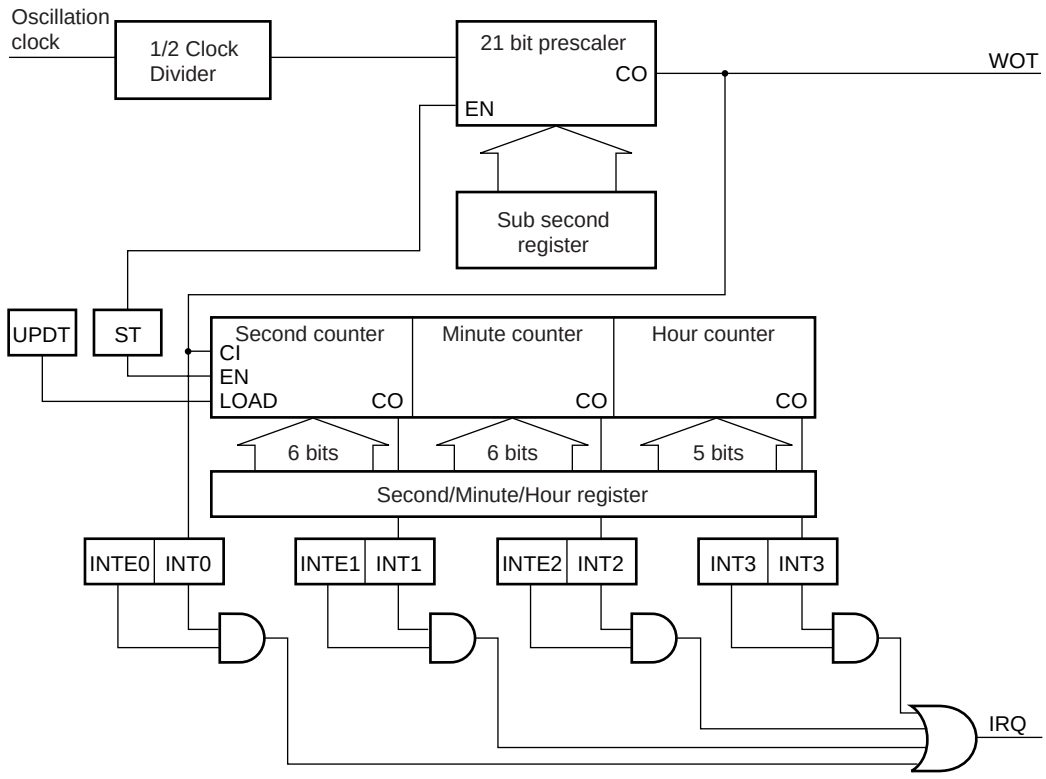
PWM Clock Disable register (SMDBL0)

	7	6	5	4	3	2	1	0	⇦ Bit no.
Address: 0000E8H	—	—	—	—	—	—	—	DBL	
Read/write ⇨	(—)	(—)	(—)	(—)	(—)	(—)	(—)	(R/W)	
Default value ⇨	(—)	(—)	(—)	(—)	(—)	(—)	(—)	(0)	

27. REAL TIME CLOCK

This section provides an overview of the Real Time Clock (also called Watchtimer) , describes the register structure and functions, and describes the operation of RTC module.The Real Time Clock (Watch Timer) consists of the Timer Control register, Sub-second register, Second/Minute/Hour registers, 1/2 clock divider, 21bit prescaler and Second/Minute/Hour counters. The Real Time Clock operates as the real-world timer and provides the real-world time information.

(1) Block Diagram



(2) Registers

Timer disable register (WTDBL)

	7	6	5	4	3	2	1	0	⇦ Bit no.
Address: 0000F5H	—	—	—	—	—	—	—	DBL	
Read/write ⇨	(—)	(—)	(—)	(—)	(—)	(—)	(—)	(R/W)	
Default value ⇨	(—)	(—)	(—)	(—)	(—)	(—)	(—)	(0)	

Timer control register (WTCR)

	7	6	5	4	3	2	1	0	⇦ Bit no.
Address: 0000F7H	TST2	TST1	TST0	—	RUN	UPDT	—	ST	
Read/write ⇨	(R/W)	(R/W)	(R/W)	(—)	(R)	(R/W)	(—)	(R/W)	
Default value ⇨	(0)	(0)	(0)	(—)	(0)	(0)	(—)	(0)	

	15	14	13	12	11	10	9	8	⇦ Bit no.
Address: 0000F6H	INTE3	INT3	INTE2	INT2	INTE1	INT1	INTE0	INT0	
Read/write ⇨	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Default value ⇨	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	

Sub-second register (WTBR)

	7	6	5	4	3	2	1	0	⇦ Bit no.
Address: 0000FBH	D7	D6	D5	D4	D3	D2	D1	D0	
Read/write ⇨	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Default value ⇨	(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)	

	15	14	13	12	11	10	9	8	⇦ Bit no.
Address: 0000FAH	D15	D14	D13	D12	D11	D10	D9	D8	
Read/write ⇨	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Default value ⇨	(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)	

	7	6	5	4	3	2	1	0	⇦ Bit no.
Address: 0000F9H	—	—	—	D20	D19	D18	D17	D16	
Read/write ⇨	(—)	(—)	(—)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Default value ⇨	(—)	(—)	(—)	(X)	(X)	(X)	(X)	(X)	

Second register (WTSR)

	15	14	13	12	11	10	9	8	⇦ Bit no.
Address: 0000FEH	—	—	S5	S4	S3	S2	S1	S0	
Read/write ⇨	(—)	(—)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Default value ⇨	(—)	(—)	(X)	(X)	(X)	(X)	(X)	(X)	

(Continued)

(Continued)

Minute register (WTMR)

	7	6	5	4	3	2	1	0	⇦ Bit no.
Address: 0000FD$_H$	—	—	M5	M4	M3	M2	M1	M0	
Read/write ⇨	(—)	(—)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Default value ⇨	(—)	(—)	(X)	(X)	(X)	(X)	(X)	(X)	

Hour register (WTHR)

	15	14	13	12	11	10	9	8	⇦ Bit no.
Address: 0000FC$_H$	—	—	—	H4	H3	H2	H1	H0	
Read/write ⇨	(—)	(—)	(—)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Default value ⇨	(—)	(—)	(—)	(X)	(X)	(X)	(X)	(X)	

28. SUBCLOCK

The Subclock System provides various power saving modes. The key of the concept is to supply the 32 kHz clock signal only to the Real Time Clock RTC) Module, while the rest of the MCU is provided with 4 MHz clock signal in order to achieve lower power supply current in the RTC32K mode.

This behavior can be altered by the configuration input, SELCLK pin to switch the RTC module to operate with the 4 MHz clock. The following sections describe the operation with SELCLK connected to “0” and SELCLK connected to “1” respectively.

Note : On MB91F361GA and MB91F362GA SELCLK should always be connected to “1”, subclock operation is not implemented on those devices.

(1) Operation of Subclock (SELCLK = 0)

The next table summarizes the operation states of the components related to the Subclock System.To simplify this table SLEEP modes are not listed but the operation is the same as for RUN modes except that the CPU is stopped.

Mode	Power dissipation	Operation of components				
		4 M Osc.	32 K Osc.	RTC	CPU & Peripheral	PLL
RUN	High	Run	Run	Run	Run	Stop/Run
RTC4M32K	Medium Low	Run	Run	Run	Stop	Stop
RTC32K	Low	Stop	Run	Run	Stop	Stop
STOP	Lowest	Stop	Stop	Stop	Stop	Stop

The following table summarizes those operation modes and necessary software settings.

Mode	Software Setting					
	STOP	PLL1EN	PLL2EN	OSCD1	OSCD2	RTC32
RUN	0	0 or 1	1	Don’t Care	Don’t Care	Don’t Care
RTC4M32K	1	Don’t Care	1	0	0	Don’t Care
RTC32K	1	Don’t Care	1	1	0	1
STOP	1	Don’t Care	Don’t Care	1	1	Don’t Care

It is recommended that PLL2EN is set to “1” after the initialization to start the 32 kHz oscillation and this bit should be kept at “1” during the operation. Otherwise the 32 kHz oscillator does not start. Also bits 9 and 10 of the CLKR register (address 0046H) should always be set to “0” during operation.

(2) 4 MHz Real Time Clock Configuration (SELCLK = 1)

When the SELCLK pad is connected logic level 1, the 32 kHz oscillation is disabled regardless of the software setting. In this configuration, the Real Time Clock Module is supplied with the 4 MHz oscillation clock signal.

The following table summaries the modes available in this configuration.

Mode	Power dissipation	Operation of components				
		4 M Osc.	32 K Osc.	RTC	CPU & Peripheral	PLL
RUN	High	Run	Stop	Run	Run	Stop/Run
RTC4M	Medium Low	Run	Stop	Run	Stop	Stop
STOP	Lowest	Stop	Stop	Stop	Stop	Stop

Mode	Software Setting					
	STOP	PLL1EN	PLL2EN	OSCD1	OSCD2	RTC32
RUN	0	0 or 1	Don’t Care	Don’t Care	Don’t Care	Don’t Care
RTC4M	1	Don’t Care	Don’t Care	0	Don’t Care	Don’t Care
STOP	1	Don’t Care	Don’t Care	1	Don’t Care	Don’t Care

(3) Use of Real Time Clock Module

There is some additional consideration needed to operate the RTC module to achieve the desired functionality.

Because the RTC module is directly connected to the 32 kHz oscillation clock, the oscillation stabilization time has to be taken care of by the software.This can be achieved by using another timer (e.g the Time Base Timer) to trigger the software to start the RTC module (Setting of ST bit to “1”) .

It is also important to stop the RTC module before entering the STOP mode. Otherwise, the reactivation from STOP mode results in unpredictable operation of the RTC module.

After the reactivation, the oscillation stabilization time has to be measured again by the software, then the RTC module can be restarted.

29. 32 kHz CLOCK CALIBRATION UNIT

The 32 kHz Clock Calibration Module provides possibilities to calibrate the 32 kHz oscillation clock with respect to the 4 MHz oscillation clock.

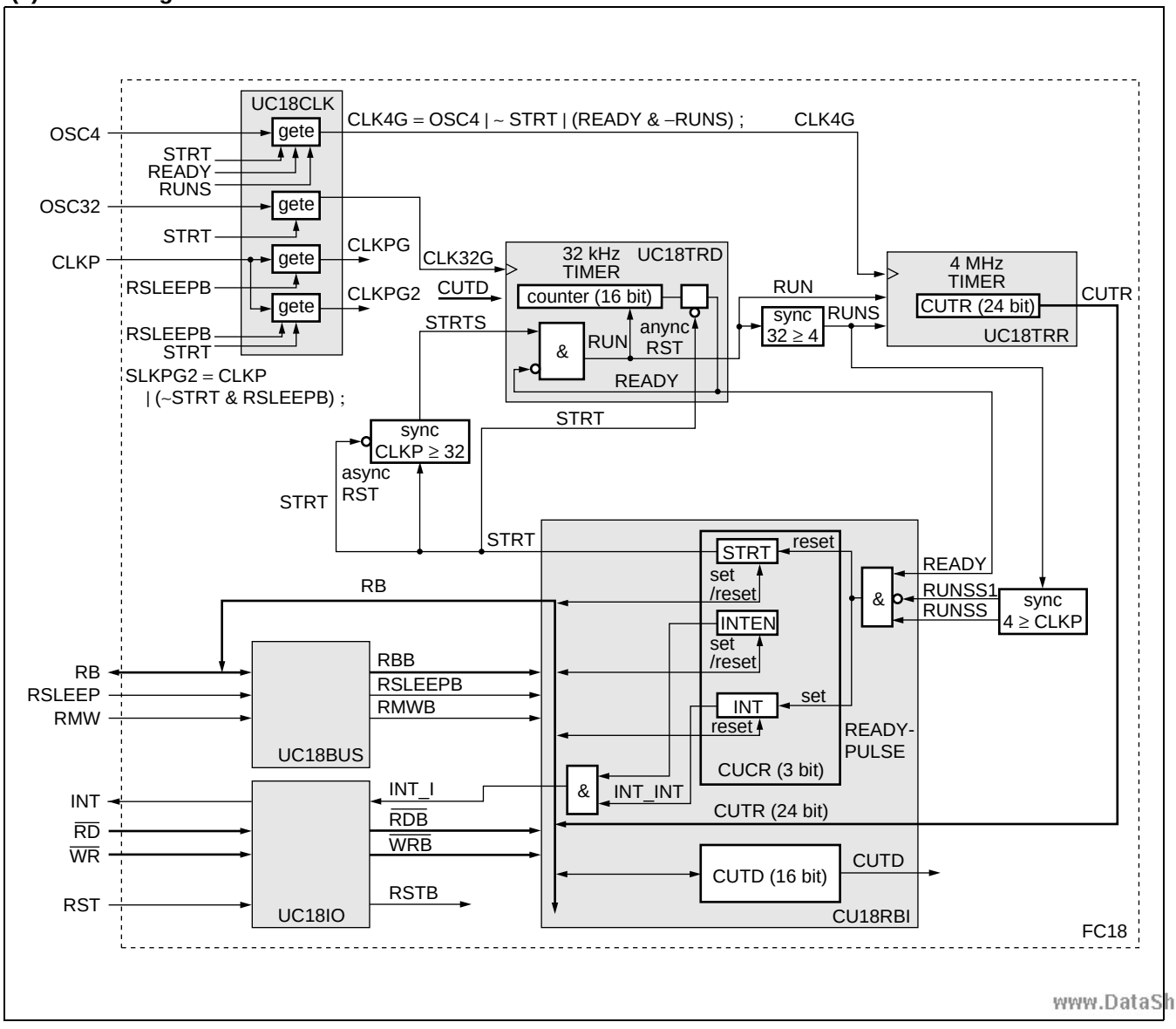
(1) Description

This hardware allows the software to measure time generated by the 32 kHz clock with the 4 MHz clock.

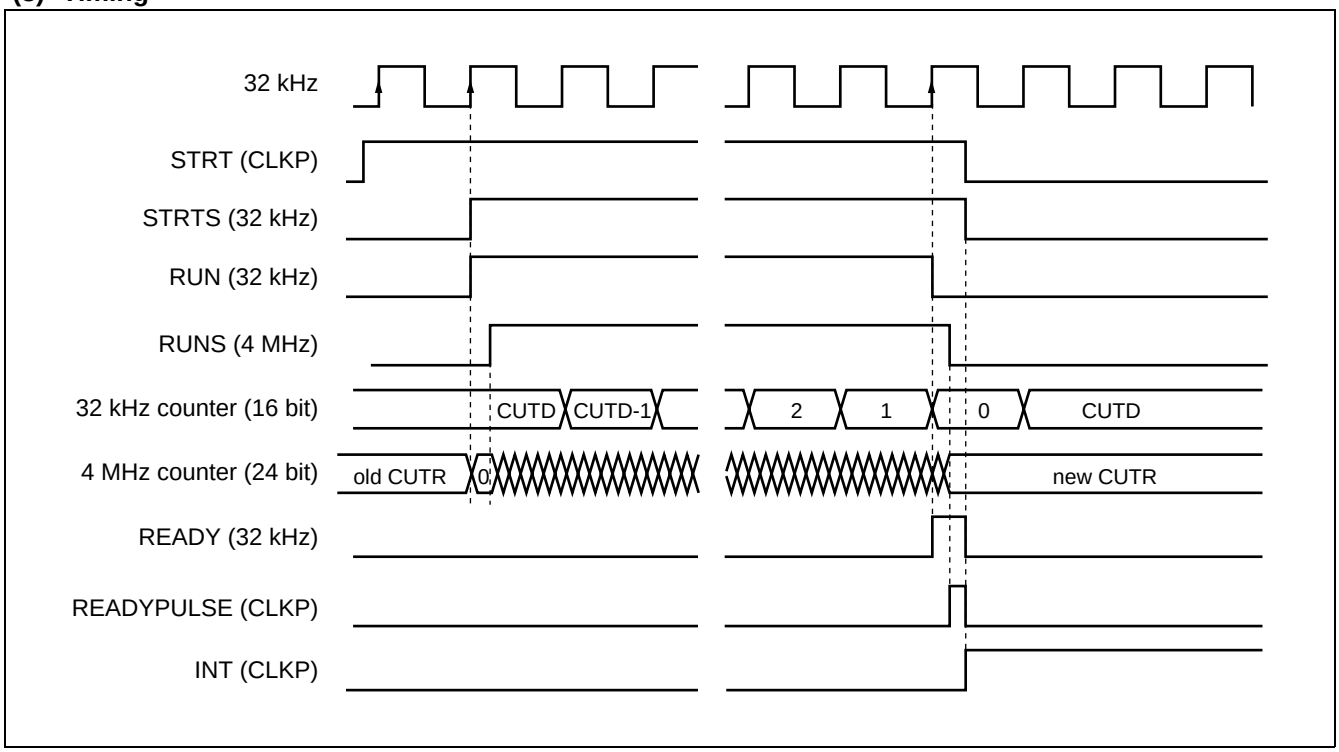
By utilizing this hardware in conjunction with software processing, the accuracy of the 32 kHz clock can come closer to that of the 4 MHz clock. The measurement result from the 32 kHz Clock Calibration Module can be processed by the software and the setting required for the Real Time Clock Module can be obtained.

This module consists of two timers, one operating with the 32 kHz clock and the other operating with the 4 MHz clock. The 32 kHz timer triggers the 4 MHz timer and resulting 4 MHz timer value is stored in a register. The value stored in this register can be used for the subsequent software processing to calculate the desired Real Time Clock module's setting.

(2) Block Diagram



(3) Timing



(4) Clocks

The module operates with 3 different clocks : The 4 MHz clock OSC4, the 32 kHz clock OSC32 and the Rbus clock CLKP. Synchronization circuits adapt the different domains.

All 3 clocks are gated. The 32 kHz and the 4 MHz clock are switched off if STRT is 0. CLKPG is gated by RSLEEP and CLKPG2 by RSLEEP and STRT for the 2 bits, which are set/reset by hardware.

The clock frequencies have to fulfill the following requirements :

1.) Clock ratio

$T_{OSC32} > 2 \times T_{OSC4} + 3 \times T_{CLKP}$

$T_{OSC4} < 1 / 2 \times T_{OSC32} - 3 / 2 \times T_{CLKP}$

$T_{CLKP} < 1 / 3 \times T_{OSC32} - 2 / 3 \times T_{OSC4}$

2.) The input frequencies must not exceed the values given in next table.

Maximum operation frequencies

	CLKP		OSC32		OSC4	
maximum	32 MHz	31.25 ns	4 MHz	250 ns	13 MHz	76.9 ns

Examples of valid clock ratios which fulfill requirements 1 and 2

	OSC32		OSC4		CLKP	
maximum operation speed	4 MHz	250 ns	13 MHz	76.9 ns	32 MHz	31.25 ns
standard TDIR mode	500 kHz	2000 ns	4 MHz	250 ns	4 MHz	250 ns
normal operation	32 kHz	31.25 us	4 MHz	250 ns	> 2 MHz	500 ns

(5) Register Description

a : Calibration Unit Control Register (CUCR)

Control Register low byte (CUCRL)

	7	6	5	4	3	2	1	0	⇦ Bit no.
Address: 000191H	—	—	—	STRT	—	—	INT	INTEN	
Read/write ⇨	(R)	(R)	(R)	(R/W)	(R)	(R/W)	(R/W)	(R/W)	
Default value ⇨	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	

b : **32 kHz Timer Data Register** (**CUTD**)

32 kHz Timer Data Register high byte (CUTDH)

	15	14	13	12	11	10	9	8	⇦ Bit no.
Address: 000192H	TDD15	TDD14	TDD13	TDD12	TDD11	TDD10	TDD9	TDD8	
Read/write ⇨	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Default value ⇨	(1)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	

32 kHz Timer Data Register low byte (CUTDL)

	7	6	5	4	3	2	1	0	⇦ Bit no.
Address: 000193H	TDD7	TDD6	TDD5	TDD4	TDD3	TDD2	TDD1	TDD0	
Read/write ⇨	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Default value ⇨	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	

c : 4 MHz Timer Data Register (CUTR)

4 MHz Timer Data Register1 high byte (CUTR1H)

	15	14	13	12	11	10	9	8	⇦ Bit no.
Address: 000194H	—	—	—	—	—	—	—	—	
Read/write ⇨	(R)	(R)	(R)	(R)	(R)	(R)	(R)	(R)	
Default value ⇨	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	

4 MHz Timer Data Register1 low byte (CUTR1L)

	7	6	5	4	3	2	1	0	⇦ Bit no.
Address: 000195H	TDR23	TDR22	TDR21	TDR20	TD19	TDR18	TDR17	TDR16	
Read/write ⇨	(R)	(R)	(R)	(R)	(R)	(R)	(R)	(R)	
Default value ⇨	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	

4 MHz Timer Data Register2 high byte (CUTR2H)

	15	14	13	12	11	10	9	8	⇦ Bit no.
Address: 000196H	TDR15	TDR14	TDR13	TDR12	TDR11	TDR10	TDR9	TDR8	
Read/write ⇨	(R)	(R)	(R)	(R)	(R)	(R)	(R)	(R)	
Default value ⇨	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	

4 MHz Timer Data Register2 low byte (CUTR2L)

	7	6	5	4	3	2	1	0	⇦ Bit no.
Address: 000197H	TDR7	TDR6	TDR5	TDR4	TD3	TDR2	TDR1	TDR0	
Read/write ⇨	(R)	(R)	(R)	(R)	(R)	(R)	(R)	(R)	
Default value ⇨	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	

30. FLASH MEMORY

MB91360G series devices feature 512 K of embedded flash memory. On MB91F361GA it is connected to the external bus, on the other devices to the F-bus.

(1) Out Line of Flash Memory

The Flash Memory consists of a flash memory unit derived from the MBM29LV400C and a flash memory interface circuit.

Flash Memory :

- 512 Kword × 8 bit/256 Kword × 16 bit/128 Kword × 32 bit
  (64 Kbyte×3 + 32 Kbyte + 8 Kbyte×2 + 16 Kbyte) sectors
- Uses automatic program algorithm (Embedded Algorithm™)
- Erase pause/restart function
- Detects completion of writing/erasing using data polling or toggle bit functions
- Detects completion of writing/erasing by RY/BY pin
- Compatible with JEDEC standard commands
- Performs minimum of 10,000 write/erase operations
- Sector erase function (any combination of sectors)
- Sector protect function
- Temporary sector protect cancellation function
- Allows flash memory interface circuit to write to/erase flash memory both under control of external pin by writer and under control of internal bus by CPU.

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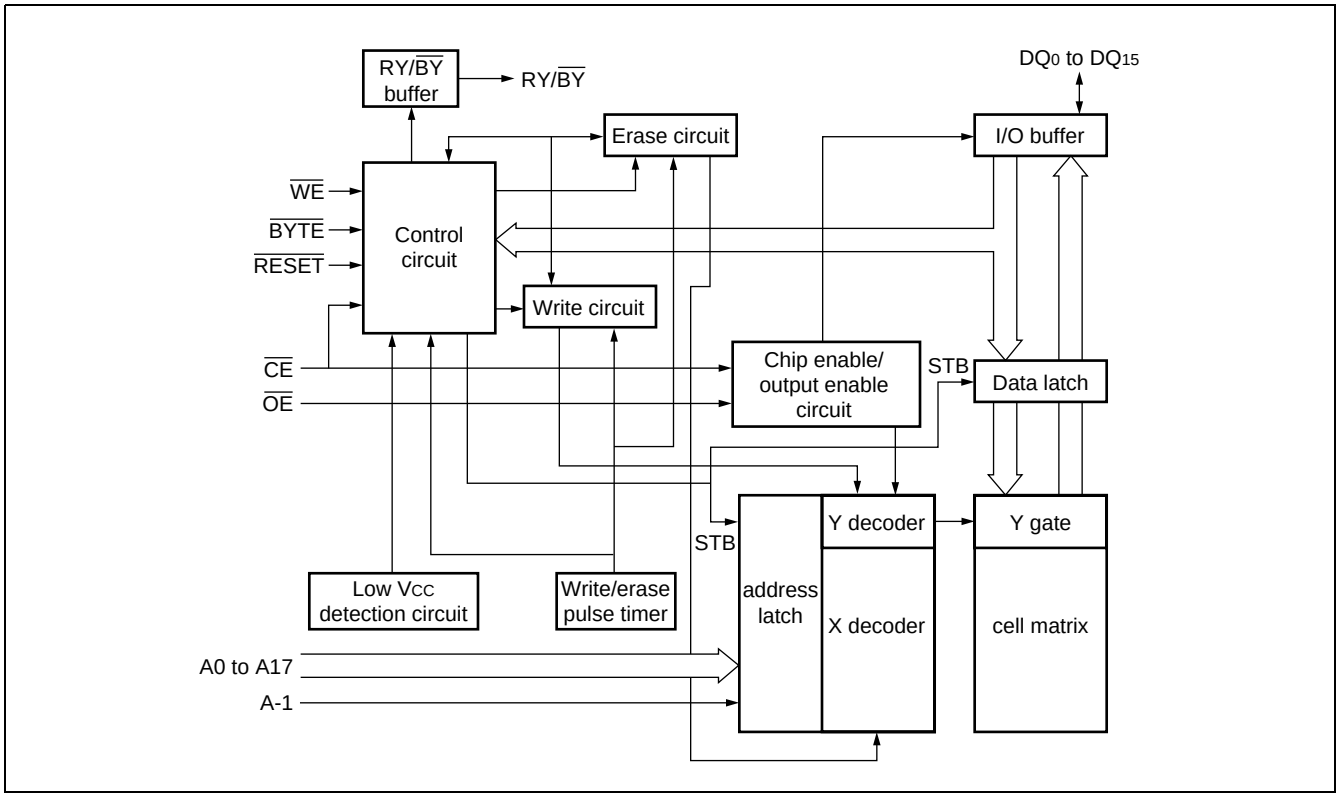
(2) Block diagrams of Flash Memory

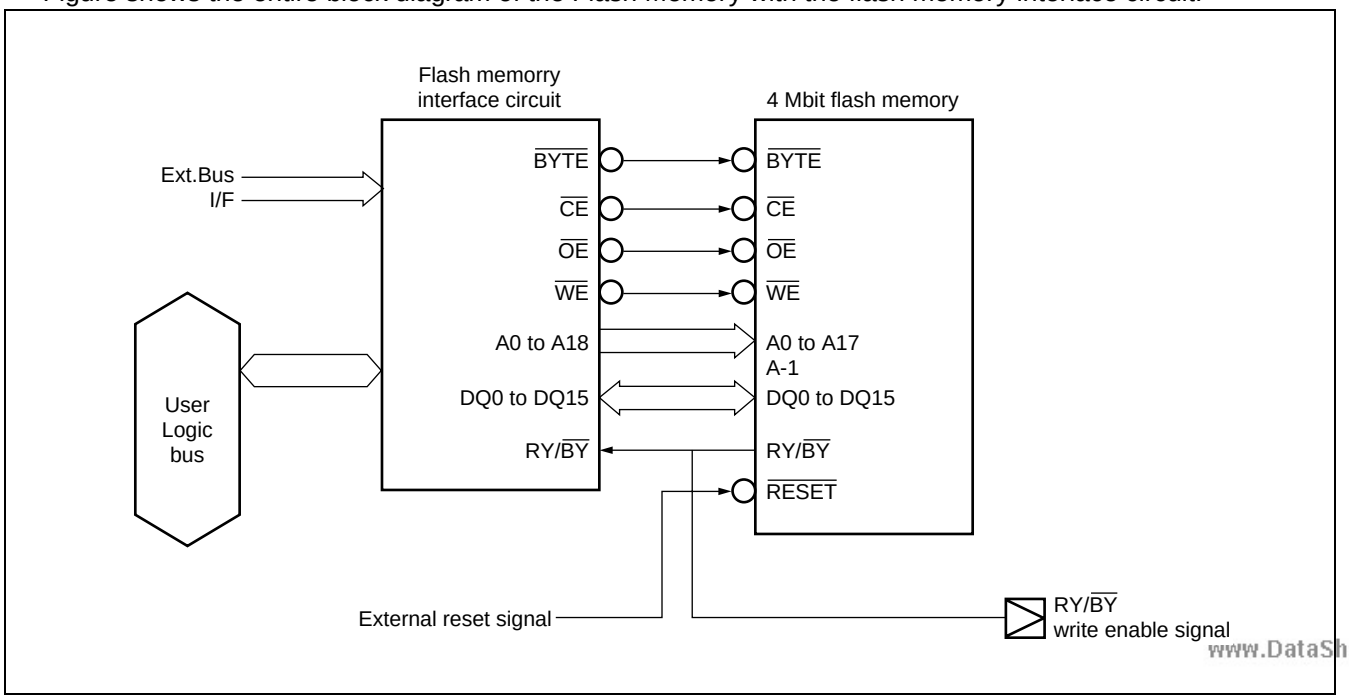
a : Block diagram of Flash Memory

Figure shows the block diagram of the flash memory unit, which has almost the same configuration as the MBM29FLV400C.



b : Entire block diagram of Flash Memory

Figure shows the entire block diagram of the Flash Memory with the flash memory interface circuit.



c : Sector configuration

i) write, byte read, half word read

		Flash Memory mode	Other modes F361GA	Other modes other devices
8 bit × 2		$7FFFF_H$	1FFFFF	FFFFF
Sector 13	16 KB	$7C000_H$	1FC000	FC000
Sector 12	8 KB	$7A000_H$	1FA000	FA000
Sector 11	8 KB	78000_H	1F8000	F8000
Sector 10	32 KB	70000_H	1F0000	F0000
Sector 9	64 KB	60000_H	1E0000	E0000
Sector 8	64 KB	50000_H	1D0000	D0000
Sector 7	64 KB	40000_H	1C0000	C0000
Sector 6	16 KB	$3C000_H$	1BC000	BC000
Sector 5	8 KB	$3A000_H$	1BA000	BA000
Sector4	8 KB	38000_H	1B8000	B8000
Sector 3	32 KB	30000_H	1B0000	B0000
Sector 2	64 KB	20000_H	1A0000	A0000
Sector 1	64 KB	10000_H	190000	90000
Sector 0	64 KB	00000_H	180000	80000

ii) long word read

MSB		LSB		Flash Memory mode	Other modes F361GA	Other modes other devices
8 bit × 2		8 bit × 2		7FFFF	$1FFFFF_H$	FFFFF
Sector 13	16 KB	Sector 6	16 KB	78000_H	$1F8000_H$	F8000
Sector 12	8 KB	Sector 5	8 KB	74000_H	$1F4000_H$	F4000
Sector 11	8 KB	Sector 4	8 KB	70000_H	$1F0000_H$	F0000
Sector 10	32 KB	Sector 3	32 KB	60000_H	$1E0000_H$	E0000
Sector 9	64 KB	Sector 2	64 KB	40000_H	$1C0000_H$	C0000
Sector 8	64 KB	Sector 1	64 KB	20000_H	$1A0000_H$	A0000
Sector 7	64 KB	Sector 0	64 KB	00000_H	180000_H	80000

(3) Write/Erase Modes

The flash memory can be accessed in two different ways; the flash memory mode allowing write/erase directly from the external pins, and the other modes allowing write/erase from the CPU via the internal bus. These modes are selected by the external mode pins.

a : **Flash Memory mode**

The CPU stops when the mode pins are set to 111 while the $\overline{INIT}$ signal is asserted. The flash memory interface circuit is directly connected to the external bus interface, allowing direct control by the external pins. This mode makes the MCU seem like a standard flash memory at the external pins, and write/erase can be performed using a flash memory programmer.

In the flash memory mode all the operations supported by the flash memory automatic algorithm can be used.

b : **Other modes**

The flash memory is located in the $\overline{CS1}$ area of the CPU memory space and like ordinary mask ROM can be read-accessed and program-accessed from the CPU through the flash memory interface circuit. After execution of the internal Boot ROM the area for CS1 is set from 180000 to FFFFF (F361GA only) .

Writing/erasing the flash memory is performed by instructions from the CPU via the flash memory interface circuit. Therefore, this mode allows rewriting even when the MCU is soldered on the target board.

The sector protect operations can not be performed in these modes.

c : **Control signals of flash memory**

Next table lists the flash memory control signals in the flash memory mode.

There is almost a one-to-one correspondence between the flash memory control signals and the external pins of the MBM29LV400C. The V_{ID} (12 V) pins required by the sector protect operations are MD0, MD1 and MD2 instead of A9, $\overline{RESET}$ and $\overline{OE}$ for the MBM29LV400C.

In the flash memory mode, the width of the external data bus can be 8 or 16 bit.

Flash Control Signals

MB91F361GA/MB91F362GA			MBM29LV400C
Pin number	**Normal function**	**Flash Memory mode**	
1 to 8	D24 to D31	D24 to D31	DQ8 to DQ15
9	A0	A0	A-1
10 to 24	A1 to A15	A1 to A15	A0 to A14
27 to 30	A16 to A18	A16 to A18	A15 to A17
32	$\overline{CS4}$	$\overline{CS4}$	WE
33	$\overline{CS5}$	$\overline{CS5}$	BYTE
35	RDY	RDY	OE
36	$\overline{BGRNT}$	$\overline{BGRNT}$	CE
37	BRQ	BRQ	RY/$\overline{BY}$
111	MD0	VDA9	A9 (V_{ID})
112	MD1	VDRS	$\overline{RESET}$ (V_{ID})
113	MD2	VDOE	OE (V_{ID})
115	$\overline{INIT}$	$\overline{INIT}$	RESET
201 to 208	D16 to D23	D16 to D23	DQ0 to DQ7

A19, A20 should be pulled up, $\overline{INIT}$ must be low during power on for at least 500 ns.

MB91FV360GA			MBM29LV400C
Pin number	Normal function	Flash Memory mode	
202	A0	A0	A-1
310	A1	A1	A0
201	A2	A2	A1
357	A3	A3	A2
257	A4	A4	A3
144	A5	A5	A4
309	A6	A6	A5
256	A7	A7	A6
200	A8	A8	A7
356	A9	A9	A8
308	A10	A10	A9
92	A11	A11	A10
44	A12	A12	A11
255	A13	A13	A12
143	A14	A14	A13
199	A15	A15	A14
307	A16	A16	A15
91	A17	A17	A16
142	A18	A18	A17
140	$\overline{CS4}$	$\overline{CS4}$	$\overline{WE}$
196	$\overline{CS5}$	$\overline{CS5}$	$\overline{BYTE}$
89	$\overline{CS6}$	$\overline{TMOD}$	—
305	RDY	RDY	$\overline{OE}$
139	$\overline{BGRNT}$	$\overline{BGRNT}$	$\overline{CE}$
88	BRQ	BRQ	RY/$\overline{BY}$
293	MD0	VDA9	A9 (V_{ID})
31	MD1	VDRS	$\overline{RESET}$ (V_{ID})
239	MD2	VDOE	$\overline{OE}$ (V_{ID})
30	$\overline{INIT}$	$\overline{INIT}$	$\overline{RESET}$
46	D16	D16	DQ0
95	D17	D17	DQ1
1	D18	D18	DQ2
148	D19	D19	DQ3
205	D20	D20	DQ4

(Continued)

(Continued)

MB91FV360GA			MBM29LV400C
Pin number	**Normal function**	**Flash Memory mode**	
45	D21	D21	DQ5
94	D22	D22	DQ6
260	D23	D23	DQ7
312	D24	D24	DQ8
204	D25	D25	DQ9
147	D26	D26	DQ10
93	D27	D27	DQ11
259	D28	D28	DQ12
203	D29	D29	DQ13
146	D30	D30	DQ14
258	D31	D31	DQ15

(4) Flash Control Status Register (FMCS)

Flash Memory Macros used in devices :
Normal Flash Macro used in : MB91F361GA, MB91F362GA
Fast Flash Macro used in : MB91FV360GA

	address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
FV360GA, F362GA :	00007000_H	FACCEN	—	—	RDYEG*	RDY	RDYI	WE	LPM
F361GA :	00100180_H								
	access	R/W	R/W	R/W	R	R	R/W	R/W	R/W
	initial value	1	1	1	0	X	0	0	0
	value after Boot ROM	0	1	1	0	X	0	0	0

* : It is not allowed to use RDYEG.

(5) Read/Write Access

In the flash memory mode, read/write access to the flash memory must be under control of the external pins. However, with the CPU access, there are no special timing constraints on read/write access because the flash memory is controlled by the flash memory interface circuit.

In this section, “write access” does not directly mean “program flash memory”. It implies “activation of the flash commands”.

a : Read/write access in flash memory mode

Next table gives the setting of pins for read/write access in the Flash Memory mode. There is no special problem with control of these pins if connected to a flash memory writer. However, in other cases, timing specifications must be met.

Setting Conditions of Pins for Read/Write Access in Flash Memory Mode

Operations	BGRNTX ($\overline{CE}$)	RDY ($\overline{OE}$)	CS4X ($\overline{WE}$)	A0 to A18	D16 to D31	$\overline{INIT}$
Read	L	L	H	Read address	D_{OUT}	H
Write	L	H	L	Write address	D_{IN}	H
Output disable	L	H	H	x	High-Z	H
Standby	H	x	x	x	High-Z	H
Hardware reset	x	x	x	x	High-Z	L

b : Read/write access with CPU on F361GA

The access timing to the flash memory unit is controlled by the flash memory interface circuit. Depending on the setting for CLKT the read operation can be completed in two or more cycles of CLKT.

External Bus clear	Wait cycles
32 MHz	1
24 MHz	1
≤ 16 MHz	0

c : Read access with CPU on other devices

Flash Wait Control Register (FMWT) *

address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
00007004_H	—	—	FAC1	FAC0	EQINH	WTC2	WTC1	WTC0
access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
initial value		0	0	0	0	0	1	1
value after Boot ROM Normal Flash Macro		0	0	0	0	0	1	1
value after Boot ROM Fast Flash Macro		0	0	1	0	0	1	1

* : FMWT register is not available on MB91F361GA (Flash on external bus)

Normal Flash Macro : **Recommended settings**

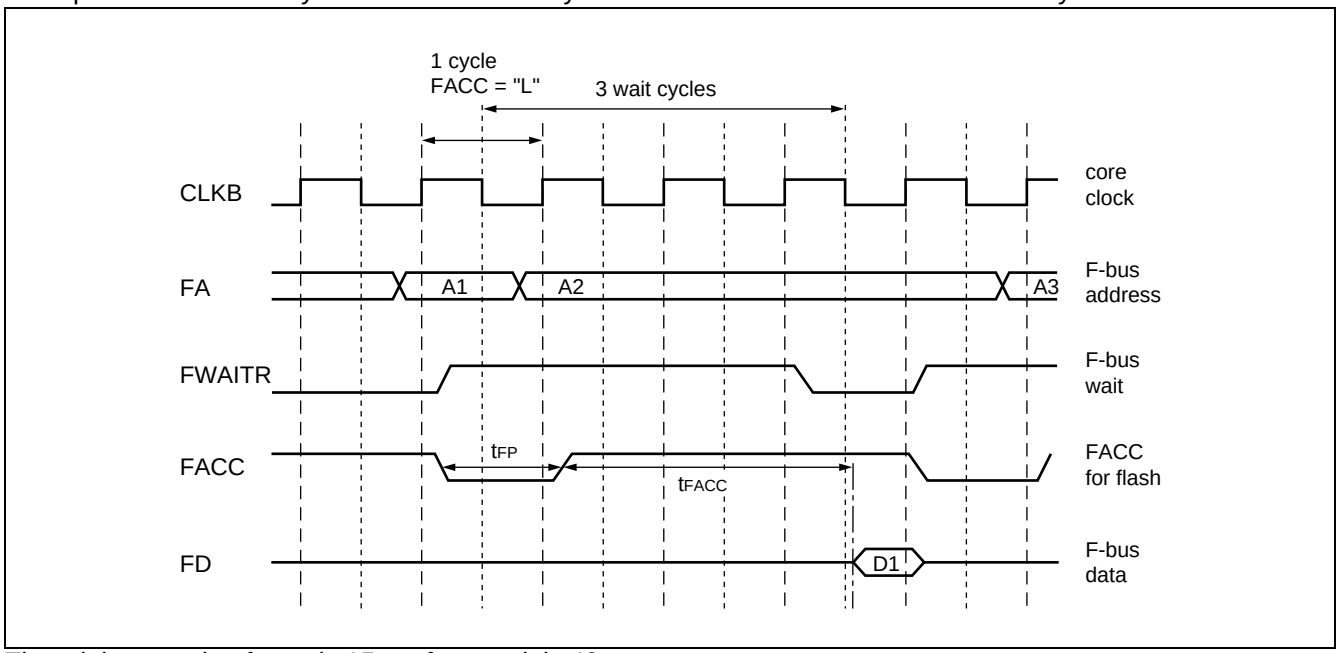
Without applying clock modulation

CLKB unmodulated core clock frequency [MHz]	FAC1	FAC0	EQINH	WTC2	WTC1	WTC0	FACC low cycles/wait cycles	FMWT
64	0	1	0	0	1	1	1 / 3	13H
48	0	1	0	0	1	1	1 / 3	13H
40	0	1	0	0	1	0	1 / 2	12H
32	0	0	0	0	1	0	0.5 / 2	02H
24	0	0	0	0	0	1	0.5 / 1	01H
16	0	0	0	0	0	1	0.5 / 1	01H

When applying clock modulation

CLKB core clock frequency [MHz]	Peak Max. frequency	FAC1	FAC0	EQINH	WTC2	WTC1	WTC0	FACC low cycles/wait cycles	FMWT
48	64	0	1	0	0	1	1	1 / 3	13H
32	48	0	1	0	0	1	1	1 / 3	13H
24	40	0	1	0	0	1	0	1 / 2	12H
24	32	0	0	0	0	1	0	0.5 / 2	02H
16	24	0	0	0	0	0	1	0.5 / 1	01H

Example for flash memory read access with 1 cycle for the low time of FACC and 3 wait cycles



The minimum value for t_{FP} is 15 ns, for t_{FACC} it is 40 ns.

Fast Flash Macro : **Recommended settings**

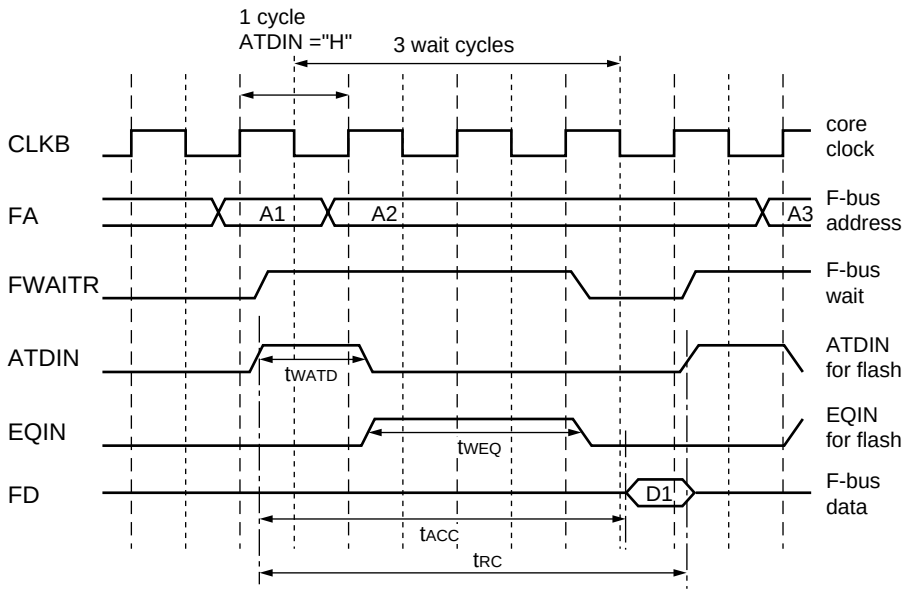
Without applying clock modulation

CLKB unmodulated core clock frequency [MHz]	FAC1	FAC0	EQINH	WTC2	WTC1	WTC0	ATDIN high cycles/wait cycles	FMWT
64	0	1	0	0	1	1	1 / 3	13H
48	0	0	0	0	1	0	0.5 / 2	02H
40	0	0	0	0	1	0	0.5 / 2	02H
32	0	0	1	0	0	1	0.5 / 1	09H
24	0	0	0	0	0	1	0.5 / 1	01H
16	0	0	0	0	0	1	0.5 / 1	01H

When applying clock modulation

CLKB core clock frequency [MHz]	Peak Max. frequency	FAC1	FAC0	EQINH	WTC2	WTC1	WTC0	ATDIN high cycles/wait cycles	FMWT
48	64	0	1	0	0	1	1	1 / 3	13H
32	48	0	0	0	0	1	0	0.5 / 2	02H
24	40	0	0	0	0	1	0	0.5 / 2	12H
24	32	0	0	1	0	0	1	0.5 / 1	09H
16	24	0	0	0	0	0	1	0.5 / 1	01H

Example for flash memory read access with 1 cycle for the high time of ATDIN and 3 wait cycles



The minimum value for t_{WATD} is 10 ns, the minimum value for t_{WEQ} is 20 ns.
The minimum value for t_{RC} is 40 ns.
The maximum value for t_{ACC} is $t_{WATD} + t_{WEQ} + 5$ ns.

d : Write access with CPU on other devices

Recommended settings for WTC2 to WTC0 for write access to the flash memory, FACCEN of FMCS should be set to 1 for writing, so FAC1, FAC0, EQINH register settings then have no meaning for the write operation

Without applying clock modulation

CLKB unmodulated core clock frequency [MHz]	WTC2	WTC1	WTC0	Wait cycles	FMWT
64	setting not allowed for writing				
48	1	0	0	4	X4H
40	1	0	0	4	X4H
32	0	1	0	2	X2H
24	0	1	0	2	X2H
16	0	0	1	1	X1H

When applying clock modulation

CLKB core clock frequency [MHz]	Peak Max. frequency	WTC2	WTC1	WTC0	Wait cycles	FMWT
48	64	setting not allowed for writing				
32	48	1	0	0	4	X4H
24	40	1	0	0	4	X4H
24	32	0	1	0	2	X2H
16	24	0	1	0	2	X2H

(6) Automatic Write/Erase

Irrespective of the Flash Memory mode or other modes, writing to/erasing the flash memory unit is performed by starting the flash memory automatic algorithm.

To start the automatic algorithm, various sequences of write accesses are executed in 1 to 6 cycles. They are called Flash commands.

a : Flash Commands

There are four commands for starting the automatic algorithm of the Flash Memory unit; Read/Reset, Write, Chip Erase, and Sector Erase. There are also Erase Suspend and Erase Resume commands for the sector erase operation.

Next tables give the command sequence lists in the flash memory and other modes.

b : Command sequence

Command Sequence List (CPU access)

Command Sequence	Write Cycle of Bus	First Write Cycle of Bus		Second Write Cycle of Bus		Third Write Cycle of Bus		Fourth Read/ Write Cycle of Bus		Fifth Write Cycle of Bus		Sixth Write Cycle of Bus	
		Address	Data	Address	Data	Address	Data	Address	Data	Address	Data	Address	Data
Read/ Reset*1	1	*2xxxx	xxF0	—	—	—	—	—	—	—	—	—	—
Read/ Reset*1	4	*25554	xxAA	*2aaa8	xx55	*25554	xxF0	RA	RD	—	—	—	—
Write	4	*25554	xxAA	*2aaa8	xx55	*25554	xxA0	PA (even)	PD (word)	—	—	—	—
Chip Erase	6	*25554	xxAA	*2aaa8	xx55	*25554	xx80	*25554	xxAA	*2aaa8	xx55	*25554	xx10
Sector Erase	6	*25554	xxAA	*2aaa8	xx55	*25554	xx80	*25554	xxAA	*2aaa8	xx55	SA (even)	xx30
Sector Erase Suspend		Input of address *2xxxx or data ($xxB0_H$) suspends sector erasing.											
Sector Erase Resume		Input of address *2xxxx or data ($xx30_H$) suspends and resumes sector erasing.											

Addresses in the table are the values in the CPU memory space. All addresses and data are hexadecimal values, where x is any value and *2 may be 08 to 0F on F362GA/FV360GA, 18 to 1F on F361GA.

*1 : Read/Reset command reset Flash memory to read mode.

Command Sequence List (Flash Memory Mode)

Command Sequence	Write Cycle of Bus	First Write Cycle of Bus		Second Write Cycle of Bus		Third Write Cycle of Bus		Fourth Read/ Write Cycle of Bus		Fifth Write Cycle of Bus		Sixth Write Cycle of Bus	
		Address	Data	Address	Data	Address	Data	Address	Data	Address	Data	Address	Data
Read/ Reset*	1	*xxxx	F0	—	—	—	—	—	—	—	—	—	—
Read/ Reset*	4	*aaaa	AA	*5554	55	*aaaa	F0	RA	RD	—	—	—	—
Write	4	*aaaa	AA	*5554	55	*aaaa	A0	PA (even)	PD (word)	—	—	—	—
Chip Erase	6	*aaaa	AA	*5554	55	*aaaa	80	*aaaa	AA	*5554	55	*aaaa	10
Sector Erase	6	*aaaa	AA	*5554	55	*aaaa	80	*aaaa	AA	*5554	55	SA (even)	30
Sector Erase Suspend		Input of address *xxxx or data ($B0_H$) suspends sector erasing.											
Sector Erase Resume		Input of address *xxxx or data (30_H) suspends and resumes sector erasing.											

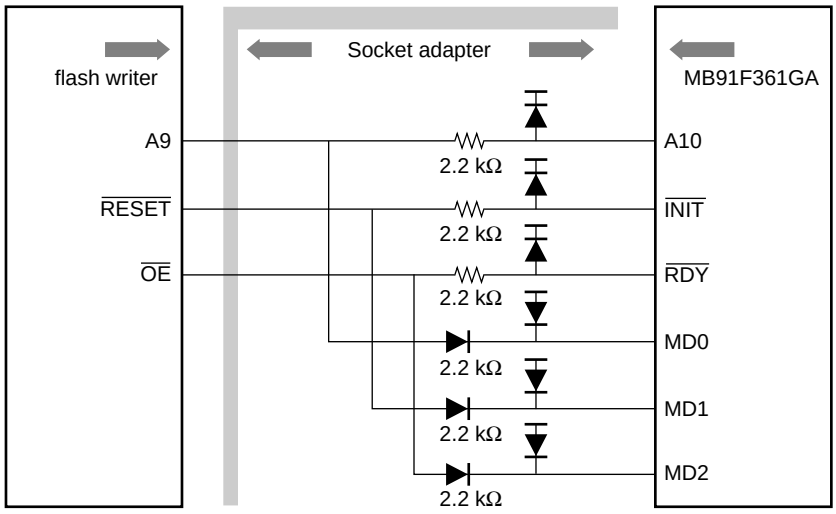
Addresses in the table are values for writer addresses. All addresses and data are hexadecimal values, where x is any value and * may be 0 to 7.
RA : Read address
PA : Write address. Only even addresses can be specified.
SA : Sector address (See next table) . Only even addresses can be specified.
RD : Read data
PD : Write data. Only word data can be specified.

Sector Address for half word mode

Sector	A18	A17	A16	A15	A14	A13	Address range
SA13	1	1	1	1	1	—	7C000H to 7FFFFH
SA12	1	1	1	1	0	1	7A000H to 7BFFFH
SA11	1	1	1	1	0	0	78000H to 79FFF
SA10	1	1	1	0	—	—	70000H to 77FFFH
SA9	1	1	0	—	—	—	60000H to 6FFFFH
SA8	1	0	1	—	—	—	50000H to 5FFFFH
SA7	1	0	0	—	—	—	40000H to 4FFFFH
SA6	0	1	1	1	1	—	3C000H to 3FFFFH
SA5	0	1	1	1	0	1	3A000H to 3BFFFH
SA4	0	1	1	1	0	0	38000H to 39FFFH
SA3	0	1	1	0	—	—	30000H to 37FFFH
SA2	0	1	0	—	—	—	20000H to 2FFFFH
SA1	0	0	1	—	—	—	10000H to 1FFFFH
SA0	0	0	0	—	—	—	00000H to 0FFFFH

(7) Connection to Flash Memory

The Flash Memory mode of the MB91F361GA is intended mainly for external connection to a flash memory writer. As indicated in Table Flash Control Signals, there is a slight difference between the external pins of the MB91F361GA and the MBM29LV400C (4 Mbit flash memory) . Connection to an MBM29LV400C writer requires the socket adapter.



(8) Notes to Use of Flash Memory

Notes on the Flash Memory in MB91360G series devices are given below.

a : **Input of hardware reset ($\overline{\text{INIT}}$)**

To input a hardware reset when the automatic algorithm is not started, where reading is in progress, a minimum of 500 ns should be taken at a low-level width. In this case, a maximum of 500 ns is required until data can be read from the flash memory after a hardware reset has been activated.

Similarly, to input a hardware reset when the automatic algorithm is activated, where writing/erasing is in progress, a minimum of 50 ns should be taken in a low-level width. In this case, 20 µs are required until data can be read after the executing operation has been terminated to initialize the flash memory.

A hardware reset during writing undefined data being written. A hardware reset during erasing may make the sector being erased unusable.

b : **Canceling software reset**, **watchdog timer reset**, **and hardware standby**

When writing/erasing the flash memory with the CPU access and if reset conditions occur while the automatic algorithm is active, the CPU may run away. This occurs because these reset conditions cause the automatic algorithm to continue without initializing the flash memory unit, possibly preventing the flash memory unit from entering the read state when the CPU starts the sequence after the reset has been deasserted. These reset conditions should be inhibited during writing/erasing the Flash Memory.

c : **Program access to Flash Memory**

When the automatic algorithm is operating, read access to the flash memory is disabled. With the memory access mode of the CPU set to the internal ROM mode, writing/erasing should be started after switching the program area to another area such as RAM.

In this case, when sectors containing interrupt vectors are erased, interrupt processing cannot be executed.

For the same reason, all interrupt sources should be disabled while the automatic algorithm is operating.

d : **Hold function**

When the CPU accepts a hold request, the Write signal $\overline{\text{WE}}$ of the flash memory unit may be skewed and many cause erroneous writing/erasing. When the acceptance of a hold request is enabled, ensure that the WE bit of the control status register (FMCS) is 0.

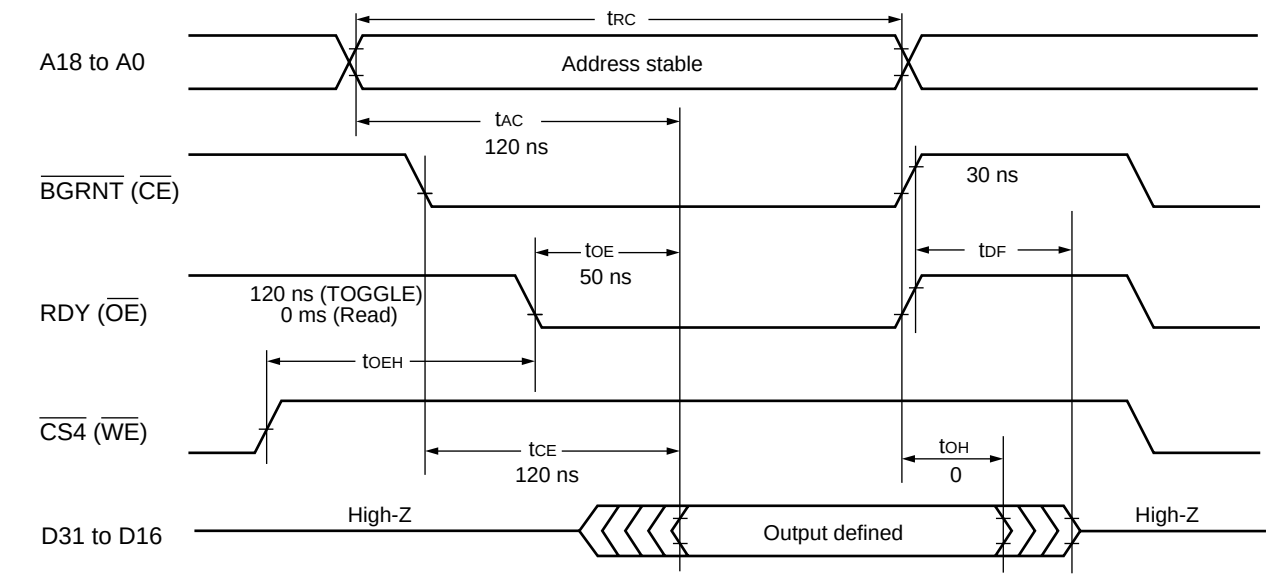
e : **Applying V_{ID}**

Applying V_{ID} required for the sector protect operation should always be started and terminated when the supply voltage is on.

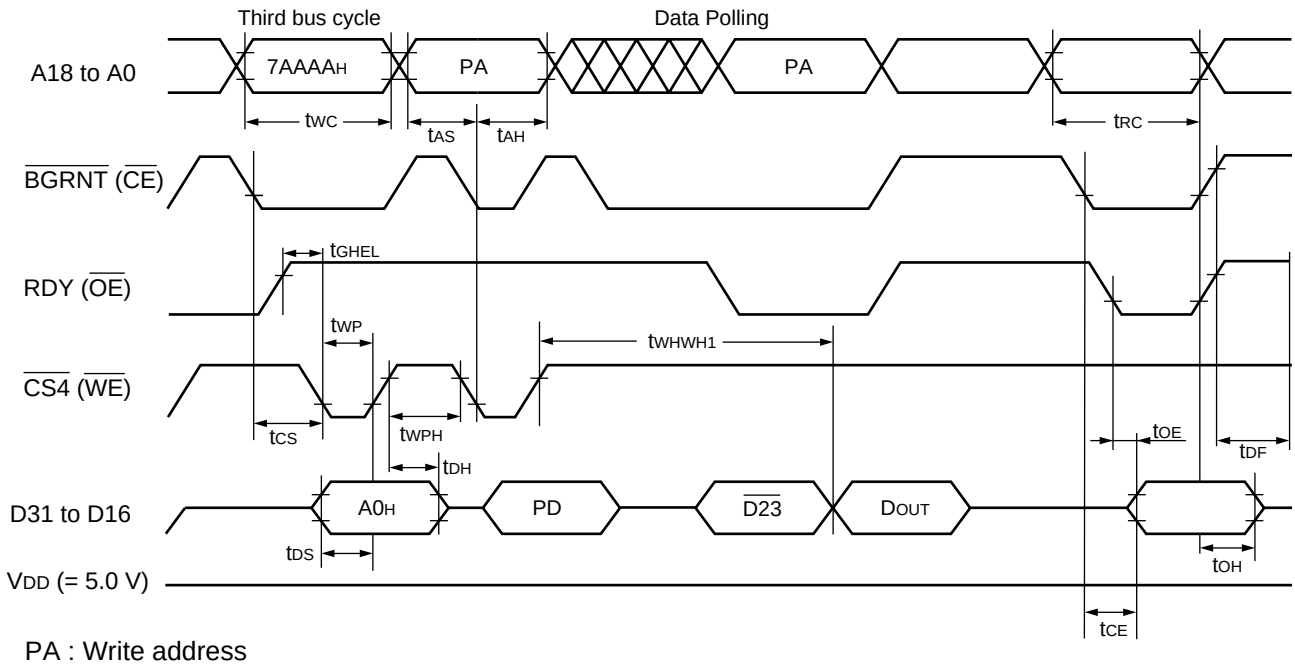
(9) Timing Diagrams in Flash Mode

Each timing diagram for the external pins of the MB91F361 in the Flash Memory mode is shown below.

a : Data read by read access



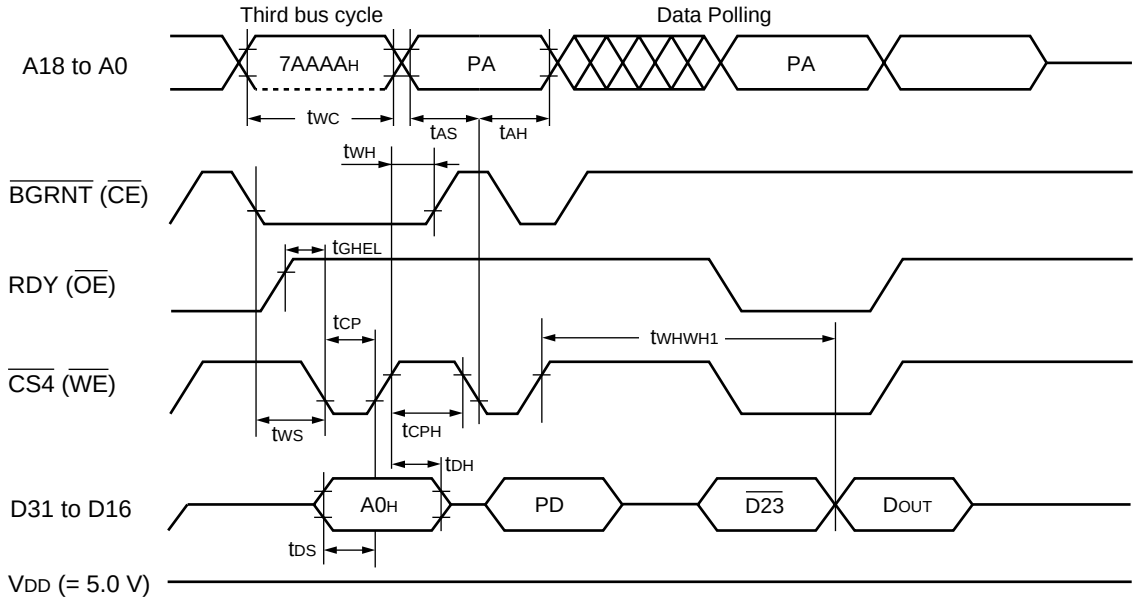
b : **Write Data polling Read (WE control)**



PA : Write address
PD : Write data
D23 : Reverse output of write data
DOUT : Output of write data

Note : The last two bus cycle sequences out of the four are described.

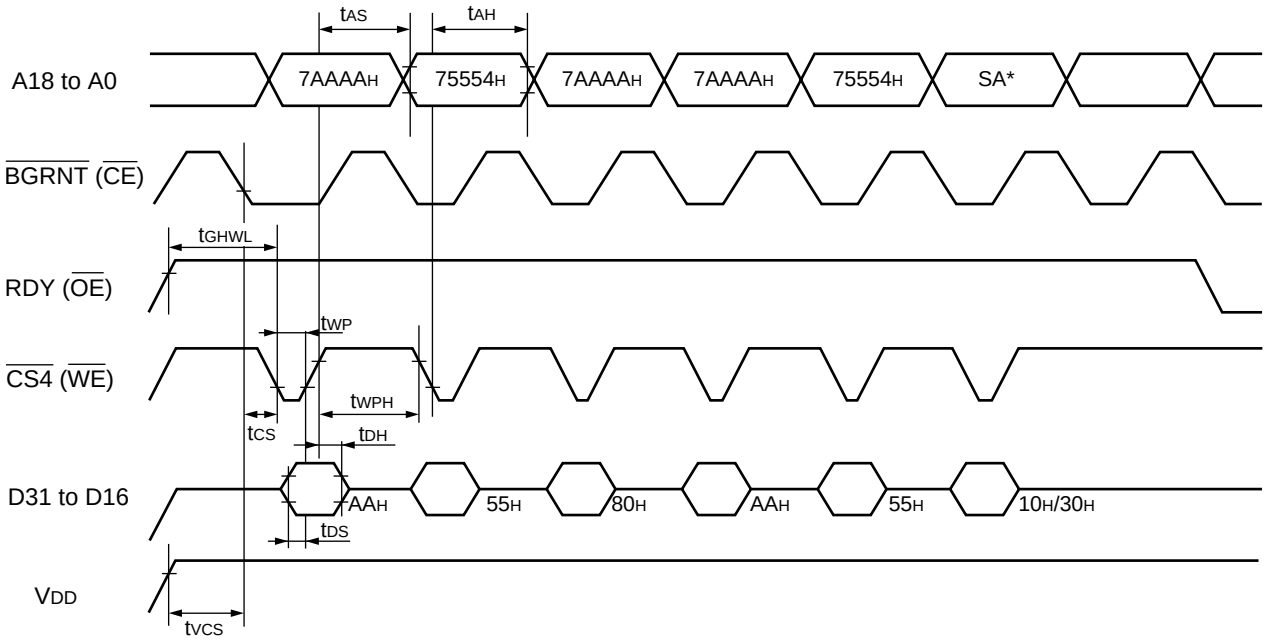
c : Write Data polling Read ($\overline{CE}$ control)



PA : Write address
PD : Write data
$\overline{D23}$: Reverse output of write data
D_{OUT} : Output of write data

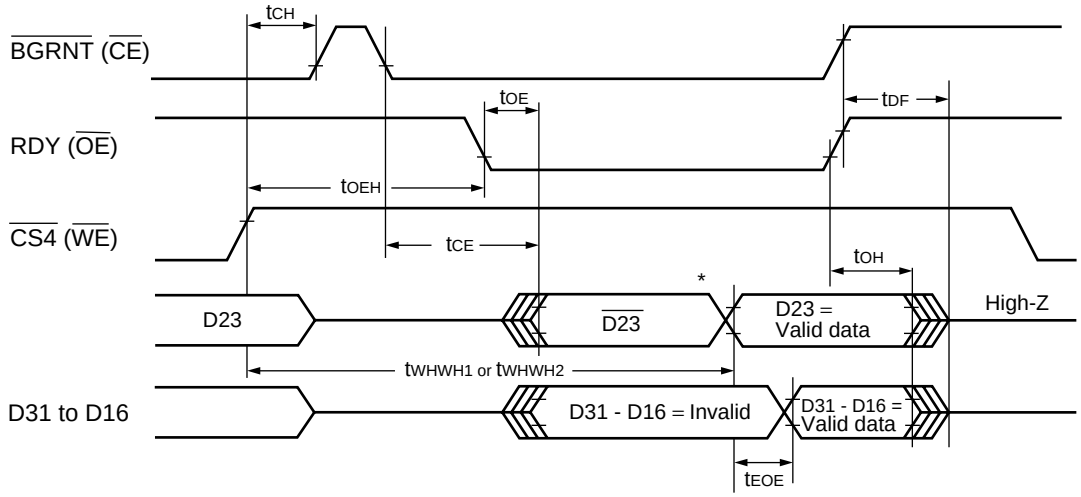
Note : The last two bus cycle sequences out of the four are described.

d : Chip erase/sector erase command sequence



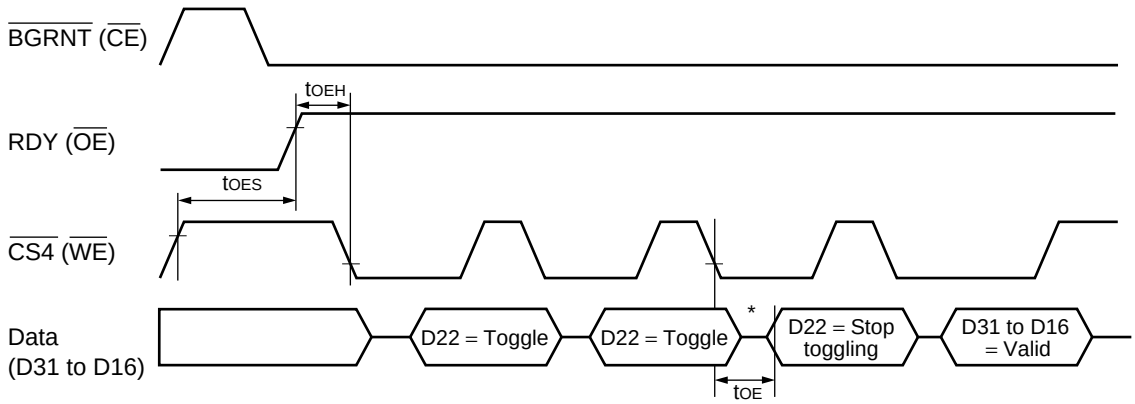
Note : SA is the sector address at sector erasing. 7AAAAH (or 6AAAAH) is the address at chip erasing.

e : **Data polling**



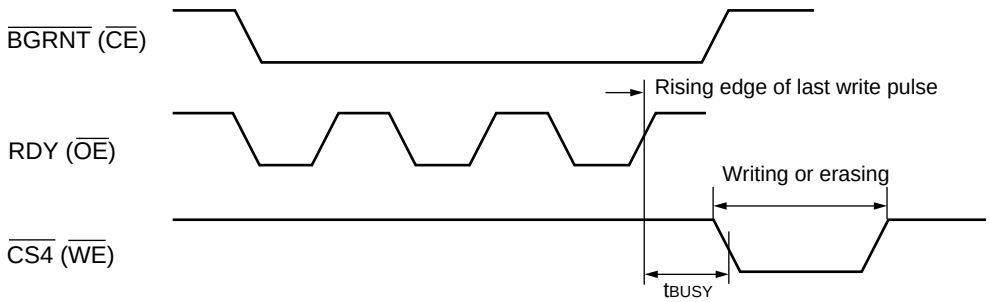
* : DQ7 is valid data (The device terminates automatic operation) .

f : **Toggle bit**

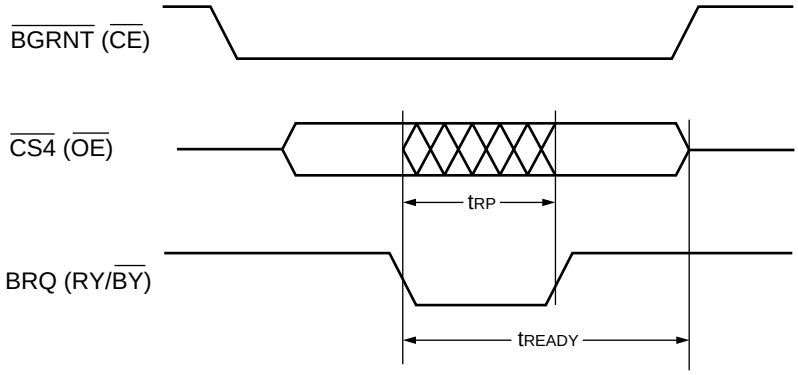


* : DQ6 stops toggling (The device terminates automatic operation) .

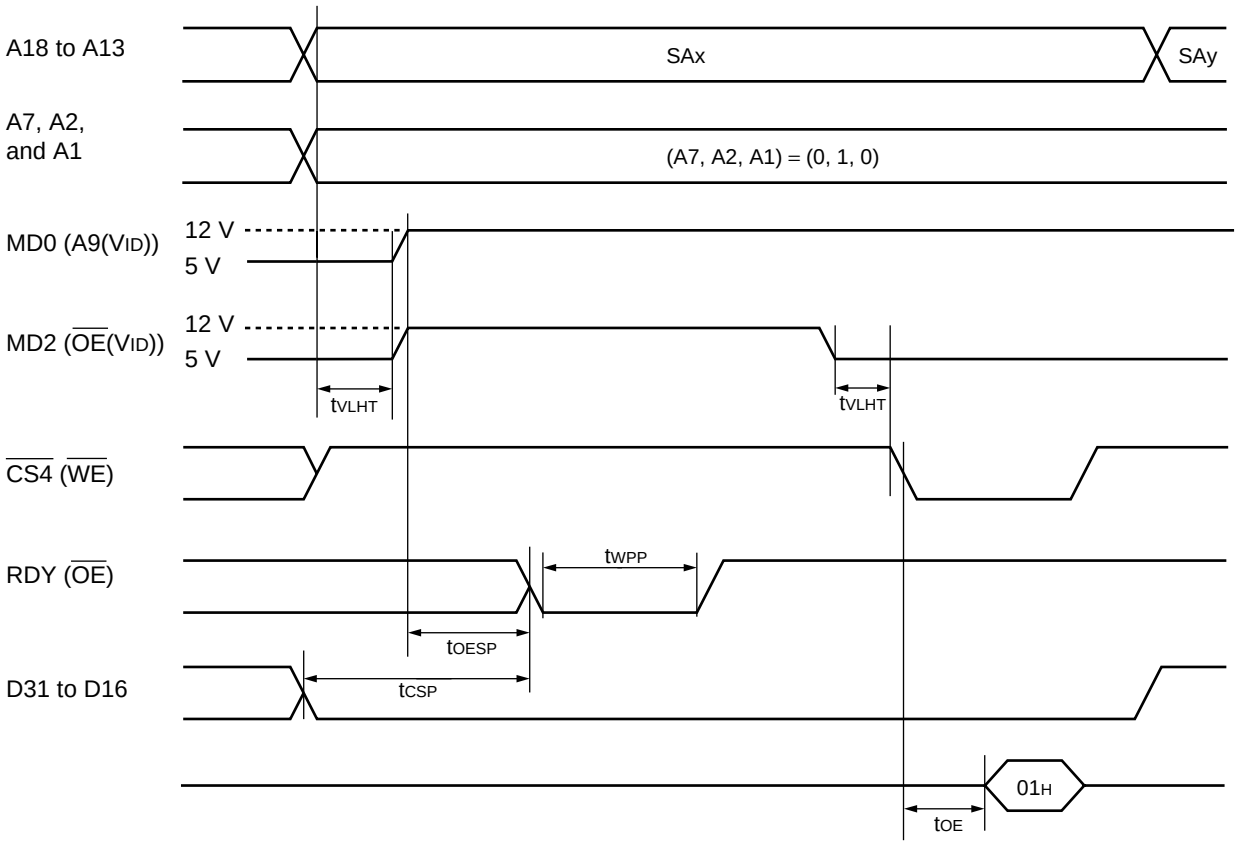
g : **RY/$\overline{BY}$ timing during writing/erasing**



h : **$\overline{\text{INIT}}$ and RY/$\overline{\text{BY}}$ timing**

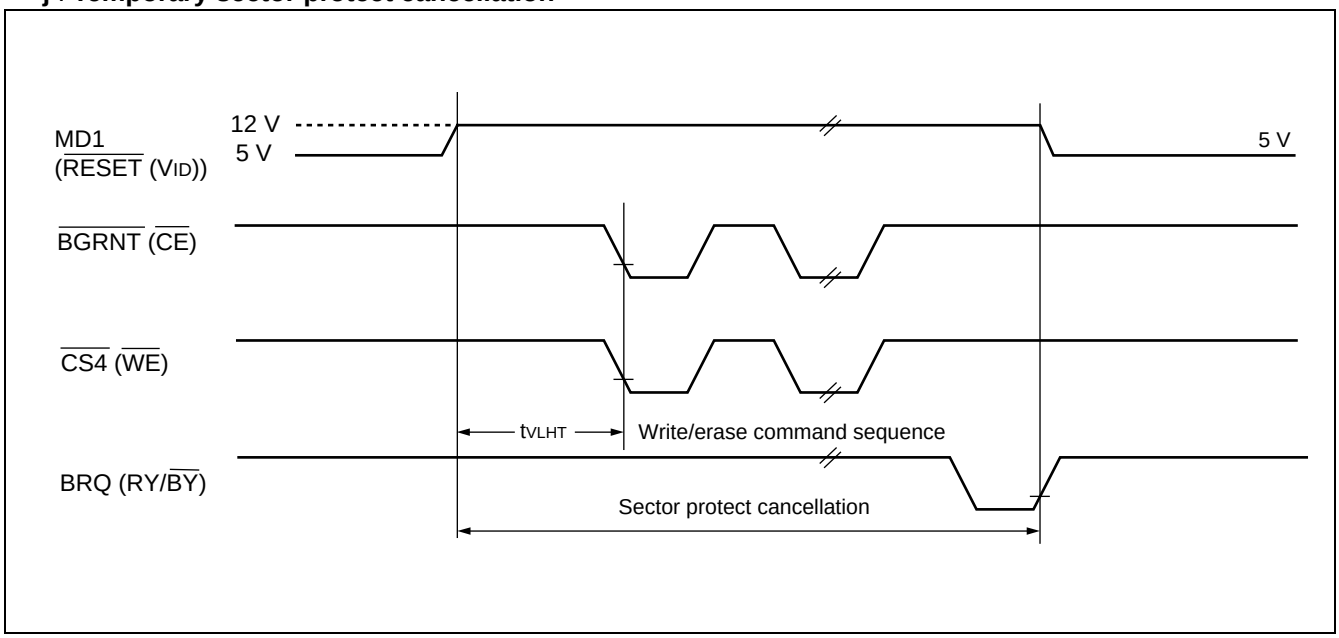


i : **Enable sector protect/verify sector protect**



SA_x : First sector address
SA_y : Next sector address

j : **Temporary sector protect cancellation**



(10) AC Characteristics in Flash Memory Mode

The AC specifications for the external pins of the MB91F361 in the Flash Memory mode are shown below. They apply to the case where the user performs read/write access in the Flash Memory mode. They are not needed for access in the normal mode and for use of a flash memory writer.

The values are subject to change without prior notice.

a : **Read access**

AC Characteristics for Read Access

(Under recommended conditions)

Parameter	Symbol	Test Condi-tions	Value			Unit
			Min.	Typ.	Max.	
Read cycle time	t_{RC}	—	120	—	—	ns
Address access time	t_{ACC}	$\overline{CE}$ = VIL $\overline{OE}$ = VIL	—	—	120	ns
$\overline{CE}$ to data output	t_{CE}	$\overline{OE}$ = VIL	—	—	120	ns
$\overline{OE}$ to data output	t_{OE}	—	—	—	50	ns
$\overline{CE}$ to output floating	t_{DF}	—	—	—	30	ns
$\overline{OE}$ to output floating	t_{DF}	—	—	—	30	ns
Previous cycle data output hold time	t_{OH}	—	0	—	—	ns
$\overline{INITI}$ pin to return to read mode	t_{Ready}	—	—	—	20	µs

b : **Write [write/erase command] access ($\overline{WE}$ control)**

AC Characteristics for Write Access ($\overline{WE}$ Control)

(Under recommended conditions)

Parameter		Symbol	Value			Unit
			Min.	Typ.	Max.	
Write cycle time		t_{WC}	120	—	—	ns
Address setup time		t_{AS}	0	—	—	ns
Address hold time		t_{AH}	50	—	—	ns
Data setup time		t_{DS}	50	—	—	ns
Data hold time		t_{DH}	0	—	—	ns
Output enable setup time		t_{OES}	0	—	—	ns
Output enable hold time	Read	t_{OEH}	0	—	—	ns
	Toggle and data polling		10	—	—	ns
Read recovery time before write		t_{GHWL}	0	—	—	ns
$\overline{CE}$ setup time		t_{CS}	0	—	—	ns
$\overline{CE}$ hold time		t_{CH}	0	—	—	ns
Write pulse width		t_{WP}	50	—	—	ns
Write pulse width High level		t_{WPH}	20	—	—	ns
Write continuation time		t_{WHWH1}	—	16	—	µs
Sector erase continuation time*1		t_{WHWH2}	—	1.5	30	s
V_{CC} setup time		t_{VCS}	50	—	—	µs
Voltage transition time*2		t_{VLHL}	4	—	—	µs
Write pulse width*2		t_{WPP}	100	—	—	µs
OE setup time for validating $\overline{WE}$*2		t_{OESP}	4	—	—	µs
CE setup time for validating $\overline{WE}$*2		t_{CSP}	4	—	—	µs
$\overline{INIT}$ pulse width		t_{RP}	500	—	—	ns
RY/$\overline{BY}$ delay until write/erase is enabled		t_{BUSY}	50	—	—	ns

*1 : The internal preprogramming time before erasing is not included.

*2 : Applies only to sector protection

c : **Write [write/erase command] access ($\overline{CE}$ control)**

AC Characteristics for Write Access ($\overline{CE}$ Control)

(Under recommended conditions)

Parameter		Symbol	Value			Unit
			Min.	Typ.	Max.	
Write cycle time		t_{WC}	120	—	—	ns
Address setup time		t_{AS}	0	—	—	ns
Address hold time		t_{AH}	50	—	—	ns
Data setup time		t_{DS}	50	—	—	ns
Data hold time		t_{DH}	0	—	—	ns
Output enable setup time		t_{OES}	0	—	—	ns
Output enable hold time	Read	t_{OEH}	0	—	—	ns
	Toggle and data polling		10	—	—	ns
Read recovery time before write		t_{GHWL}	0	—	—	ns
$\overline{WE}$ setup time		t_{WS}	0	—	—	ns
$\overline{WE}$ hold time		t_{WH}	0	—	—	ns
$\overline{CE}$ pulse width		t_{CP}	50	—	—	ns
$\overline{CE}$ pulse width High level		t_{CPH}	20	—	—	ns
Write continuation time		t_{WHWH1}	—	16	—	µs
Sector erase continuation time*		t_{WHWH2}	—	1.5	30	s
V_{CC} setup time		t_{VCS}	50	—	—	µs
$\overline{INIT}$ pulse width		t_{RP}	500	—	—	ns
RY/$\overline{BY}$ delay until write/erase is enabled		t_{BUSY}	50	—	—	ns

* : The internal preprogramming time before erasing is not included.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Condition
		Min.	Max.		
Digital supply voltage	V_{DD}-V_{SS}	–0.3	6.0	V	
Stepper motor control supply voltage	HV_{DD}-HV_{SS}	–0.3	6.5	V	
Storage temperature	Tstg	–55	+125	°C	
Power consumption	P_{TOT}	—	*1	mW	T_A = +25°C
Digital input voltage	V_{IDIG}	–0.3*2	5.8	V	V_{SS} = 0 V, V_{DD} = 5 V
Analog input voltage	V_{IA}	–0.3	5.8	V	V_{SSA} = 0 V, V_{DDA} = 5 V
Analog supply voltage	V_{DDA}-V_{SSA}	–0.3	5.8	V	V_{SSA} = 0 V
Analog reference voltage	$V_{REFH/L}$-V_{SSA}	–0.3	5.8	V	V_{SSA} = 0 V
Static DC current into digital I/O	$I_{I/ODC}$	–2	2	mA	$\Sigma I_{I/ODC} < I_{SRUN}$

*1 : The value differs in each kind of the product.

*2 : Making full use of the allowed static DC correct into digital I/O will lead to lower values for V_{IDIG} Min.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

Parameter		Symbol	Value			Unit	Condition
			Min.	Typ.	Max.		
Operating temperature		T_A	–40		+85	°C	
Supply voltage (Internal voltage regulator)	Digital supply	V_{DD} - V_{SS}	4.25*	5	5.25	V	V_{DDCORE} = 3.3 V
	Stepper motor control supply	HV_{DD} - HV_{SS}	4.75	5	5.25	V	HV_{SS} = 0 V
	Analog supply	V_{DDA} - V_{SSA}	4.9	5	5.1	V	V_{SSA} = 0 V
RAM data retention voltage		V_{DD} - V_{SS}	3.0	—	—	V	

*: This is only valid if the integrated power-down reset circuit is switched-off, else a reset can be triggered at voltages less or equal than 4.5 V (see "■ PERIPHERAL RESOURCES 23. POWER DOWN RESET") .

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

3. DC Characteristics

Parameter			Symbol	Value			Unit	Condition
				Min.	Typ.	Max.		
Current consumption	Run mode		I_{srun}	—	—	*1	mA	T_A = 25 °C
	RTC mode		I_{sRTC}	—	0.5 —	1.25 500	mA µA	f_{clk} = 4 MHz at T_A = 25 °C f_{clk} = 32 kHz at T_A = 25 °C
	Stop mode		I_{sstop}	—	10	200	µA	f_{clk} = 0 at T_A = 25 °C
Stepper motor control	H-port output voltage		V_{OHH}	HV_{DD} – 500	—	HV_{DD} – 125	mV	I_{ol} = ±30 mA, T_C = 25 °C
			V_{OHL}	HV_{SS} + 125	—	HV_{SS} + 500	mV	I_{ol} = ±30 mA, T_C = 25 °C
			V_{OHH}	HV_{DD} – 500	—	HV_{DD} – 125	mV	I_{ol} = ±27 mA, T_C = 85 °C
			V_{OHL}	HV_{SS} + 125	—	HV_{SS} + 500	mV	I_{ol} = ±27 mA, T_C = 85 °C
			V_{OHH}	HV_{DD} – 500	—	HV_{DD} – 125	mV	I_{ol} = ±30 mA, T_C = –40 °C
			V_{OHL}	HV_{SS} + 125	—	HV_{SS} + 500	mV	I_{ol} = ±30 mA, T_C = –40 °C
	SMC comparator threshold voltage		V_{THcomp}	HV_{DD} / 9 – 70	HV_{DD} / 9	HV_{DD} / 9 + 70	mV	
	Slew rate		—	—	40	—	ns	Cload = 0 pF
Alarm comparator	Threshold voltage	Over-voltage	V_{TAH}	$^4/_5$ V_{DDA} – 5%	$^4/_5$ V_{DDA}	$^4/_5$ V_{DDA} + 5%	V	(external 4 : 1 divider)
		Under-voltage	V_{TAL}	$^2/_5$ V_{DDA} – 5%	$^2/_5$ V_{DDA}	$^2/_5$ V_{DDA} + 5%	V	
	Switching hysteresis		V_{TAHYS}	12.5	25	50	mV	
	Alarm sense time		t_{AS}	—	—	10	µs	
	Input resistance		R_{in}	5	—	—	MΩ	at V_{TAH}, V_{TAL}
Power down Reset	Threshold voltage		V_{TPOR}	3.5	4.0	4.5	V	
	Switching hysteresis		$V_{TPORHYS}$	20	50	80	mV	
	Reset sense time		t_{RS}	—	—	10	µs	
Digital outputs	Output “H” voltage		V_{OH}	V_{DD} – 0.5	—	V_{DD}	V	I_{load} = 4mA
	Output “L” voltage		V_{OL}	V_{SS}	—	V_{SS} + 0.4	V	I_{load} = –4mA

*1 : See “4. Run Mode Current/Power Consumption”.

(Continued)

Parameter			Symbol	Value			Unit	Condition
				Min.	Typ.	Max.		
Digital Inputs*2	CMOS (Type : Q, S, Y, T)	High voltage range	V_{IH}	$0.65 \times V_{DD}$	—	V_{DD}	V	
		Low voltage range	V_{IL}	V_{SS}	—	$0.25 \times V_{DD}$	V	
	CMOS Schmitt-Trigger (Types : E, F, U)	High voltage range	V_{IH}	$0.8 \times V_{DD}$	—	V_{DD}	V	
		Low voltage range	V_{IL}	V_{SS}	—	$0.2 \times V_{DD}$	V	
	CMOS Automotive Schmitt-Trigger (Types : A, B, K1, M1, J)	High voltage range	V_{IH}	$0.8 \times V_{DD}$	—	V_{DD}	V	
		Low voltage range	V_{IL}	V_{SS}	—	$0.5 \times V_{DD}$ $0.6 \times V_{DD}$	V V	V_{DD}min = 4.25 V V_{DD}min = 4.75 V
		hysteresis voltage	—	—	0.5	—	V	
	CMOS 3/5 V (Type : L, N, O)	High voltage range	V_{IH}	$0.65 \times V_{DD}$	—	V_{DD}	V	
		Low voltage range	V_{IL}	V_{SS}	—	$0.25 \times V_{DD}$	V	
	CMOS 3 V (Type : P, W)	High voltage range	V_{IH}	$0.65 \times V_{DD}$	—	V_{DD}	V	
		Low voltage range	V_{IL}	V_{SS}	—	$0.25 \times V_{DD}$	V	
		Input capacitance	C_{IN}	—	—	16	pF	
		Input leakage current	I_{IL}	–1	—	+1	µA	T_A = 25 °C
		Pull up resistor	R_{up1} R_{up2}	—	50 10	—	kΩ kΩ	Types : E, U Type : S

(Continued)

*2 : valid for bidirectional tristate I/O PAD cell

(Continued)

Parameter		Symbol	Value			Unit	Condition
			Min.	Typ.	Max.		
ADC inputs	Reference voltage input	V_{REFH} V_{REFL}	V_{REFL} + 3 V_{SSA}	—	V_{DDA} V_{REFH} − 3	V V	
	Input voltage range	V_{imax} V_{imin}	V_{REFL} —	—	V_{REFH} —	V V	
	Input resistance	R_I	—	—	3.6	kΩ	
	Input capacitance	C_I	—	—	30	pF	
	Input leakage current	I_{IL}	–5	—	5	µA	T_A = 25 °C
	Impedance of external output driving the ADC input	—	—	—	4.0	kΩ	at sampling time of 1.6 µs
DAC analog outputs	Output voltage	V_{out}	V_{SSA}	—	V_{DDA}	V	
	Output impedance	R_{out}	—	2.9	—	kΩ	external voltage follower required
	Output capacitance	C_{out}	—	—	20	pF	
Sound generator	Output voltage	$V_{outHIGH}$ V_{outLOW}	V_{DD} − 0.5 V_{SS}	—	V_{DD} V_{SS} + 0.4	V V	
	Output current	I_{out}	4	—	—	mA	
PPG	Output voltage	$V_{outHIGH}$ V_{outLOW}	V_{DD} − 0.5 V_{SS}	—	V_{DD} V_{SS} + 0.4	V V	
	Output current	I_{out}	4	—	—	mA	
LED	Output voltage	$V_{outHIGH}$ V_{outLOW}	V_{DD} − 0.8 —	—	— V_{SS} + 0.8	V V	$I_{outHIGH}$ = 14 mA I_{outLOW} = 24 mA
I^2C Bus Interface (Open Drain Output)	Output voltage	$V_{outHIGH}$ V_{outLOW}	— V_{SS}	—	V_{DD} V_{SS} + 0.4	V V	
	Output current	I_{out}	3	—	—	mA	I_{outLOW} = 3 mA
Lock-up time PLL1 (4 MHz →16 MHz to 64 MHz)		—	—	—	0.1	1	ms	
ESD Protection (Human body model MIL883-B compliant)		V_{surge}	2	—	—	kV	$R_{discharge}$ = 1.5 kΩ $C_{discharge}$ = 100 pF

4. Run Mode Current/Power Consumption

The power dissipation during normal operation is determined by the total power dissipation of the internal logic P_C, the dissipation from analog modules P_A and the power dissipation P_{IO} of the I/O buffers. Among the I/O buffers the dissipation caused by the stepper motor drivers P_{SMC} should be taken into special consideration.

So the overall power consumption P_D will be calculated as a sum of $Pc + P_A + P_{SMC} + P_{IO}$.

(1) Logic Power Consumption

The following formula can be used to calculate the maximum core current consumption when the PLL is used depending on the frequency settings for the internal clocks :

$I_{CC} = 3.45\ [mA/MHz] \times CLKB\ [MHz] + 2.52\ [mA/MHz] \times CLKP[MHz] + 0.72\ [mA/MHz] \times CLKT\ [MHz] + 35.5\ mA.$

If clock modulation is used the following value must be added to this result : $0.24\ [mA/MHz] \times CLKB\ [MHz]$.

This results in the following values (higher clock settings are not allowed) :

Clock frequencies [MHz]			Maximum Core Current Consumption [mA]	Logic Power Consumption P_C at 5.25 V [mW]	Remarks
CLKB	CLKP	CLKT			
64	16	16	308	1.70	no clock modulation possible
48	24	24	290	1.52	
48	16	16	264	1.40	
32	32	32	257	1.35	
32	16	16	205	1.08	
24	24	24	202	1.06	
24	12	12	163	0.86	
16	16	16	146	0.77	
2	2	2	40	0.21	no PLL, no clock modulation
0.125	0.125	0.125	30	0.16	no PLL, no clock modulation

In addition to this power consumption of the MCU core logic the following contributions to the overall power consumption have to be considered :

(2) Analog Power Consumption

Module	Maximum Current Consumption	Remarks
DAC	1 mA / channel	
ADC	7 mA	
Power down reset	0.5 mA	
Alarm Comparator	0.5 mA	

To calculate the analog power consumption P_A, the current contributions of the active modules have to be multiplied by the maximum analog supply voltage of 5.1 V.

(3) I/O and SMC Power Consumption

SMC drivers :
The average current consumption per SMC channel is 38.2 mA, for four channels this results in 152.8 mA. At 2 × 0.5 V this results in 153 mW power consumption P_{SMC} for four channels of stepper motor drivers.

Other I/O Buffers :
The power dissipation (P_{IO}) (at 5.25 V) of the I/O buffers is represented as the sum of the dynamic power dissipation (P_{AC}) and the static power consumption (P_{DC}) .

$$P_{IO} = P_{AC} \times 1.1 + P_{DC}$$

The following table lists values for P_{AC} :

Buffer Type	Power Consumption	Unit
Normal Input	12.4	μW/MHz @ 5.0 V
Bidirectional Input		
4 mA Bidirectional Output	194 + 25 C_L	
4 mA Output		
8 mA Bidirectional Output	353 + 25 C_L	
8 mA Output		

$P_{AC} = P_{IB} \times In \times f \times$ operating rate $+ P_{OB} \times On \times f \times$ operating rate

P_{IB} :	Power Consumption of Input Buffers and Bidirectional Inputs
P_{OB} :	Power Consumption of Output Buffers and Bidirectional Outputs
In :	Total number of input buffers and bidirectional buffer inputs
On :	Total number of output buffers and bidirectional buffer outputs
f :	System frequency

Operating rate : 1.0 if all buffers are switched simultaneously at system frequency
P_{DC} is the caused by off chip loads which are drawing static currents.
$P_{DC} = VO \times IO \times DC_N$

VO :	Output voltage drop - usually 0.4 V
IO :	Output current - usually 4 mA
DC_N :	Number of output buffers and bidirectional buffers driving off chip loads causing static currents.

5. Clock Settings

Clock domain	Clock name	Max. frequency setting	Remark
Core	CLKB	64 MHz	under normal operating conditions (see “4. Run Mode Current/Power Consumption”) *
		32 MHz	for supply voltage between 4.25 and 3.5 V
Resource bus	CLKP	32 MHz	
Ext. Bus	CLKT	32 MHz	
Clock for CAN	CANCLK	32 MHz	

* : **F361GA** : If the maximum frequency of 64 MHz is set for CLKB, it is not allowed to have an odd division factor for CLKT.
F362GA : If the maximum frequency of 64 MHz is set for CLKB and an odd division factor for CLKT (3, 5, 7, 9, 11, 13, 15) has been selected, then the option to create an asymmetrical CLKT must be used (set bit 14 of the F362MD register to “1”) .

6. Converter Characteristics

- A/D Converter

Parameter	Symbol	Value			Unit	Remark
		Min.	Typ.	Max.		
Resolution	—	—	—	10	Bit	
Conversion error	—	—	—	±5.0	LSB	overall error
Non-linearity	—	—	—	±2.5	LSB	
Differential Non-linearity	—	—	—	±1.9	LSB	
Zero Reading voltage	V_{0T}	AVRL – 3.5	AVRL + 0.5	AVRL + 4.5	LSB	
Full scale reading voltage	V_{FST}	AVRH – 5.5	AVRH – 1.5	AVRH + 2.5	LSB	
Input current	$IA@V_{DDA}$	—	3.0	7.0	mA	
Reference voltage current	IR	—	1.6	2.6	mA	

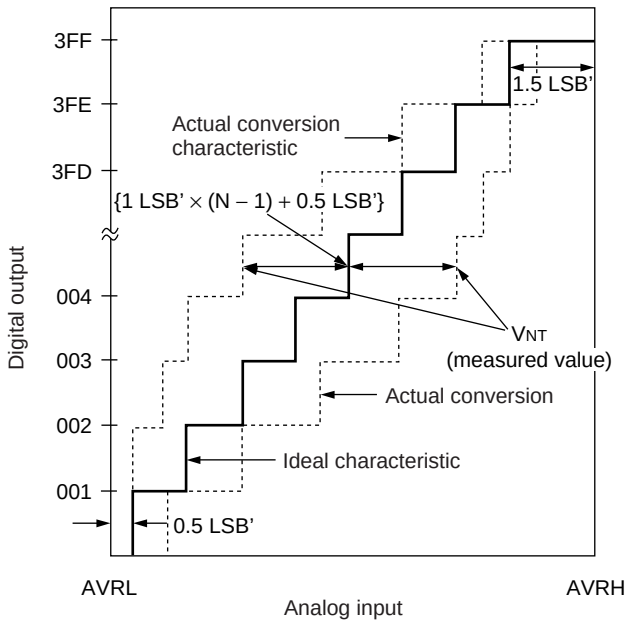
- D/A Converter

Parameter	Symbol	Value			Unit	Remark
		Min.	Typ.	Max.		
Resolution	—	—	—	10	Bit	
Differential linearity error	—	–0.9	—	+0.9	Bit	

7. A/D Converter Glossary

- **Resolution**
  The smallest change in analog voltage detected by A/D converter.
- **Linearity error**
  A deviation of actual conversion characteristic from a line connecting the zero-traction point (between “00 0000 0000” ↔ “00 0000 0001”) to the full-scale transition point (between “11 1111 1110” ↔ “11 1111 1111”) .
- **Differential linearity error**
  A deviation of a step voltage for changing the LSB of output code from ideal input voltage.
- **Total error**
  A difference between actual value and theoretical value. The overall error includes zero-transition error, full-scale transition error and linearity error.

Total error



$$\text{Total error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB'} \times (N - 1) + 0.5\ \text{LSB'}\}}{1\ \text{LSB'}}\ [\text{LSB}]$$

V_{OT}’ (Ideal value) = AVRL + 0.5 LSB’ [V]

V_{FST}’ (Ideal value) = AVRH – 1.5 LSB’ [V]

V_{NT} : A voltage for causing transition of digital output from (N – 1) to N

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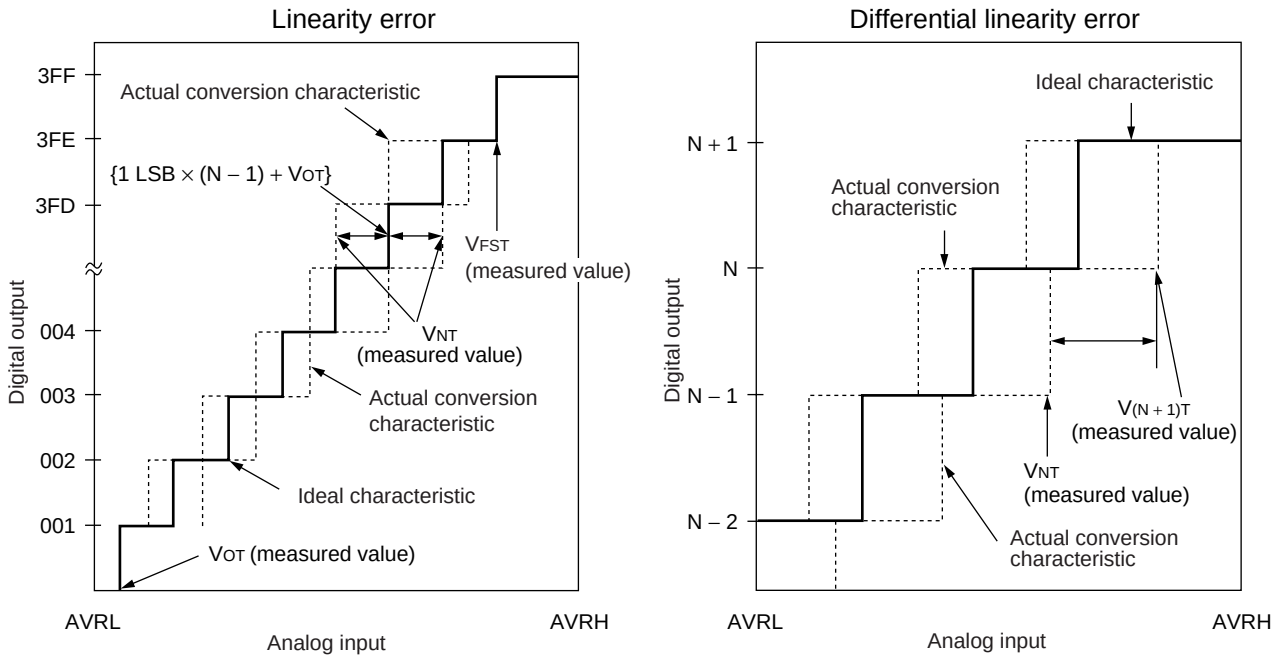


$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + V_{OT}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$\text{Differential linearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\ [\text{LSB}]$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ [\text{V}]$$

$$1\ \text{LSB'}\ (\text{ideal value}) = \frac{\text{AVRH} - \text{AVRL}}{1022}\ [\text{V}]$$

V_{OT} : A voltage for causing transition of digital output from $(000)_H$ to $(001)_H$

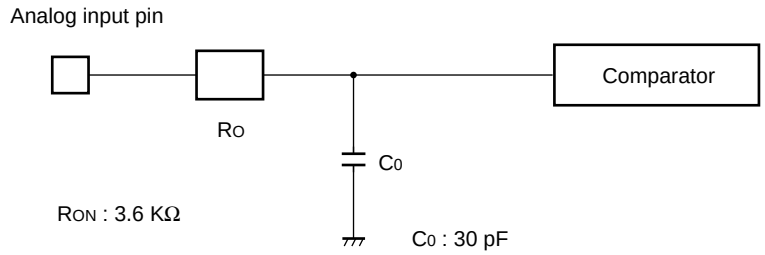
V_{FST} : A voltage for causing transition of digital output from $(3FE)_H$ to $(3FF)_H$

V_{NT} : A voltage for causing transition of digital output from $(N - 1)_H$ to N

8. Notes on Using A/D Converter

Output impedance of external circuit of analog input under following conditions;
Output impedance of external circuit < 4 kΩ.
If output impedance of external circuit is too high, analog voltage sampling time may be too short for accurate sampling.

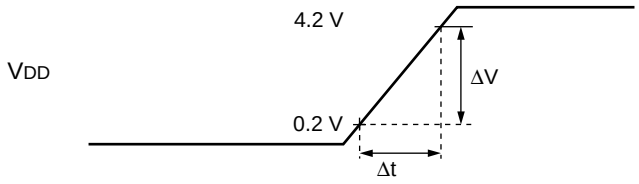
- **Analog input Equivalent Circuit**



- Error
  As the absolute value of AVRH decreases, relative error increases.

9. The Time for Power Supply

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Power supply raising slope	ΔV/Δt	—	—	0.05	V/µs
Power supply raising slope	t_R	80	—	—	µs

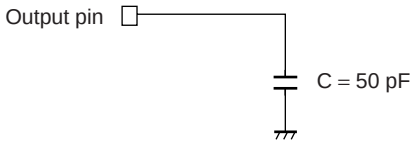


10. AC Characteristics

• Measurement conditions

Parameter	Symbol	Value	Unit	Conditions
"H" level input voltage	V_{IH}	according to I/O spec	V	V_{DD} = 4.25 to 5.25 V, T_A = –40 to +85 °C
"L" level input voltage	V_{IL}		V	
"H" level output voltage	V_{OH}	0.5 × V_{DD}	V	
"L" level output voltage	V_{OL}	0.5 × V_{DD}	V	
"H" level input voltage	V_{IH}	3.0	V	V_{DD} = 3.0 to 3.6 V, T_A = –40 to +85 °C
"L" level input voltage	V_{IL}	0	V	
"H" level output voltage	V_{OH}	0.5 × V_{DD}	V	
"L" level output voltage	V_{OL}	0.5 × V_{DD}	V	

Load conditions

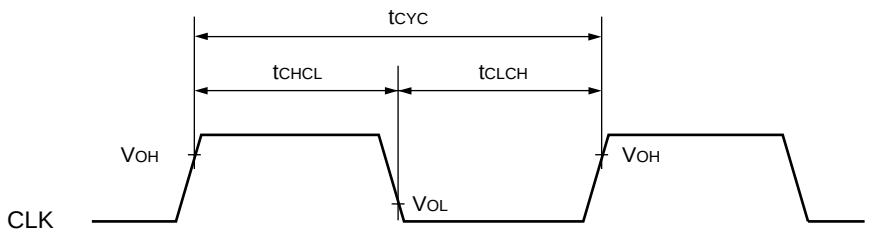


• **External bus clock**

(V_{DD} = 4.25 V to 5.25 V, T_A = –40 °C to +85 °C)

Signal	Symbol	Pin name	Value		Unit
			Min.	Max.	
CLK cycle	t_{CYC}	CLK	t_{CPT}	—	ns
CLK rise → CLK fall	t_{CHCL}	CLK	t_{CYC} / 2 – 10	t_{CYC} / 2 + 10	ns
CLK fall → CLK rise	t_{CLCH}	CLK	t_{CYC} / 2 – 10	t_{CYC} / 2 + 10	ns

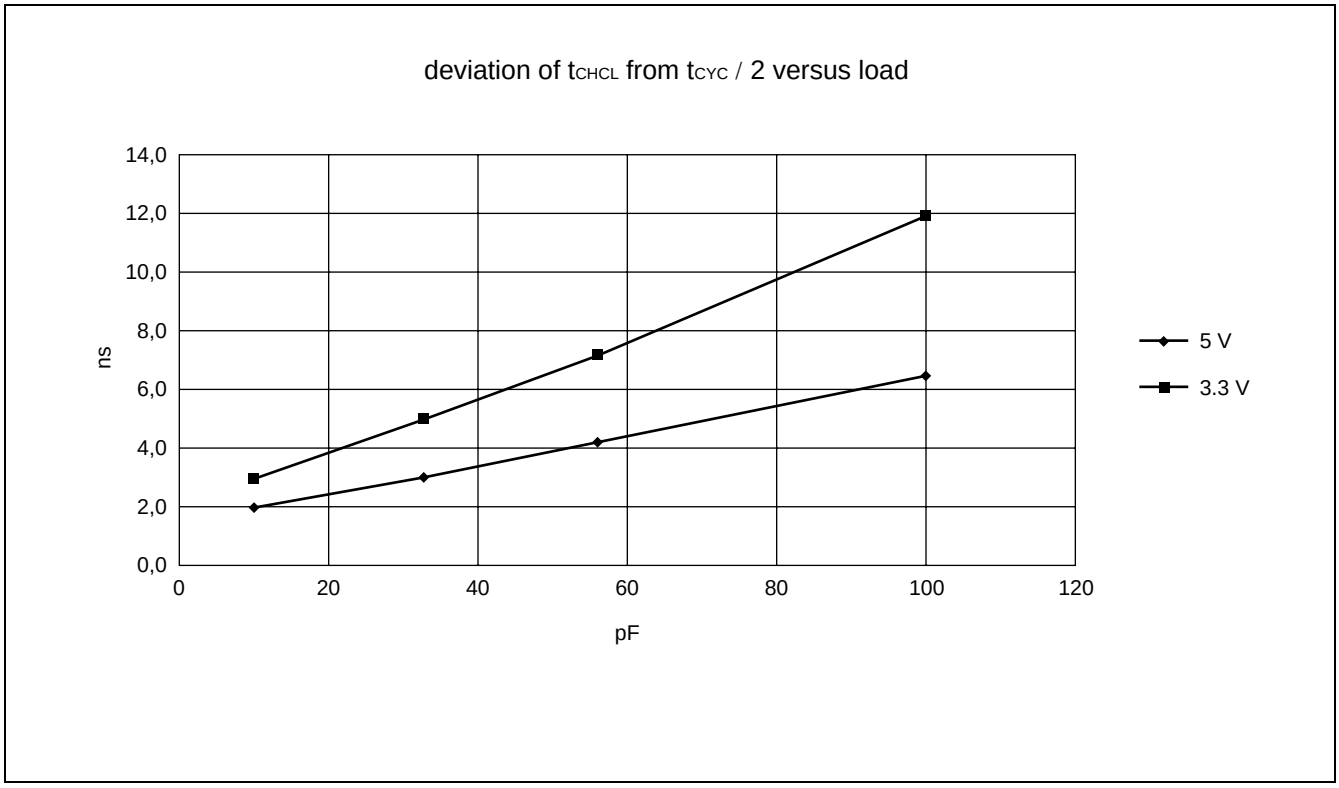
Note : This is only valid for operation without clock modulator



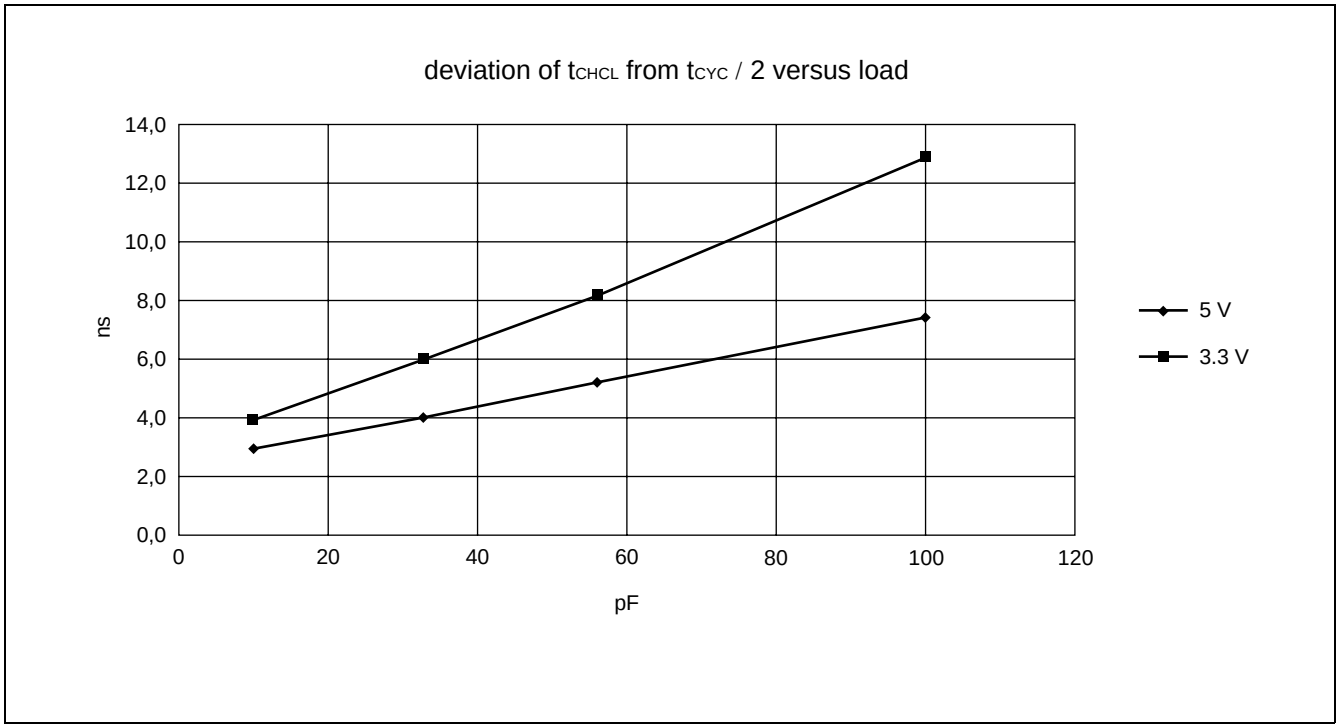
The values for t_{CHCL} and t_{CLCH} are heavily dependent on the load connected to the CLK pin. The following diagrams show this dependency for the worst case situation. The first diagram shows the situation for even division ratios between CLKB and CLKT, the second diagram shows this for odd division ratios between CLKB and CLKT (ASYMCLKT bit is not set) .

It has to note that when the combination of CLK frequency and load at CLK pin is such that rise or fall times are longer than t_{CYC} / 2 the duty ratio can get worse.

Even CLKB/CLKT division ratios :



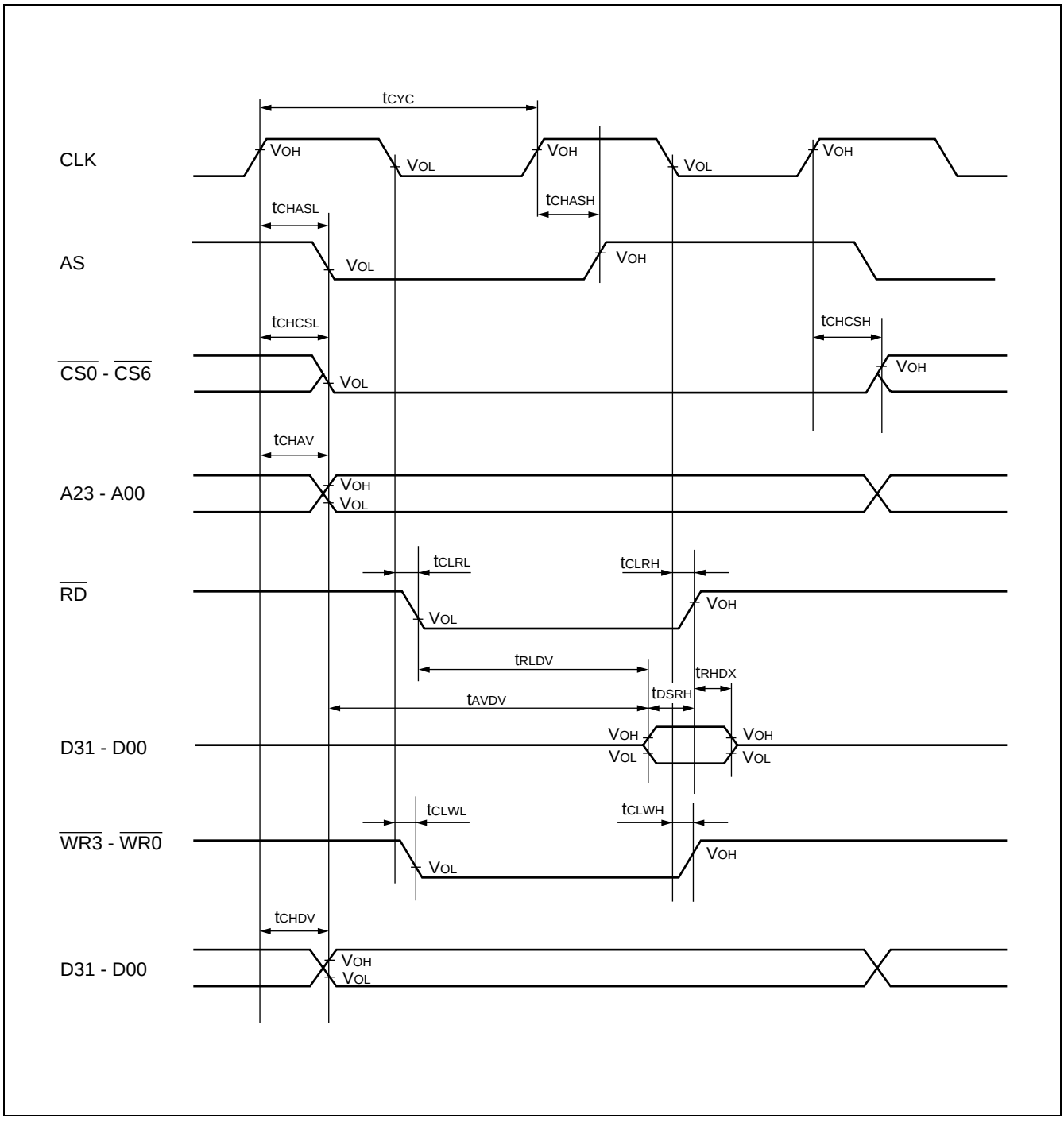
Odd CLKB/CLKT division ratios :



• **External bus interface**

(V_{DD} = 4.25 V to 5.25 V, T_A = –40 °C to +85 °C)

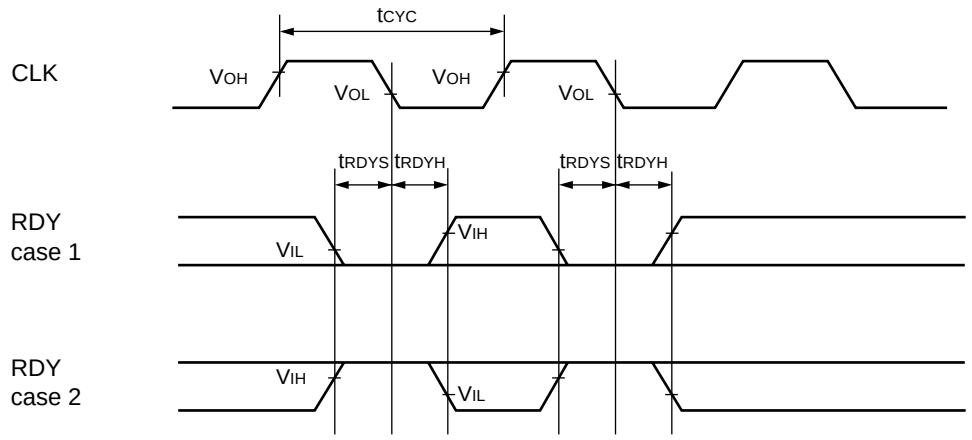
Signal	Symbol	Pin name	Value		Unit
			Min.	Max.	
$\overline{CS6}$ to $\overline{CS0}$ delay time	t_{CHCSL}	CLK $\overline{CS6}$ to $\overline{CS0}$	—	15	ns
$\overline{CS6}$ to $\overline{CS0}$ delay time	t_{CHCSH}		—	15	ns
Address delay time	t_{CHAV}	CLK A20 to A0	—	20	ns
Data delay time	t_{CHDV}	CLK D31 to D0	—	16	ns
$\overline{RD}$ delay time	t_{CLRL}	CLK $\overline{RD}$	—	15	ns
$\overline{RD}$ delay time	t_{CLRH}		—	15	ns
$\overline{WR3}$ to $\overline{WR0}$ delay time	t_{CLWL}	CLK $\overline{WR3}$ to $\overline{WR0}$	—	15	ns
$\overline{WR3}$ to $\overline{WR0}$ delay time	t_{CLWH}		—	15	ns
Effective address ⇒ Effect data input time	t_{AVDV}	A20 to A0 D31 to D0	—	$3 / 2 \times t_{CYC} - 30$	ns
$\overline{RD}$ (fall) → Effect data input time	t_{RLDV}	$\overline{RD}$ D31 to D0	—	$t_{CYC} - 20$	ns
Data set up → $\overline{RD}$ (rise) time	t_{DSRH}		25	—	ns
$\overline{RD}$ (rise) → Data hold time	t_{RHDX}		0	—	ns
AS delay time	t_{CHASL}	AS	—	15	ns
AS delay time	t_{CHASH}	AS	—	15	ns



- **RDY**

(V_{DD} = 4.25 V to 5.25 V, T_A = –40 °C to +85 °C)

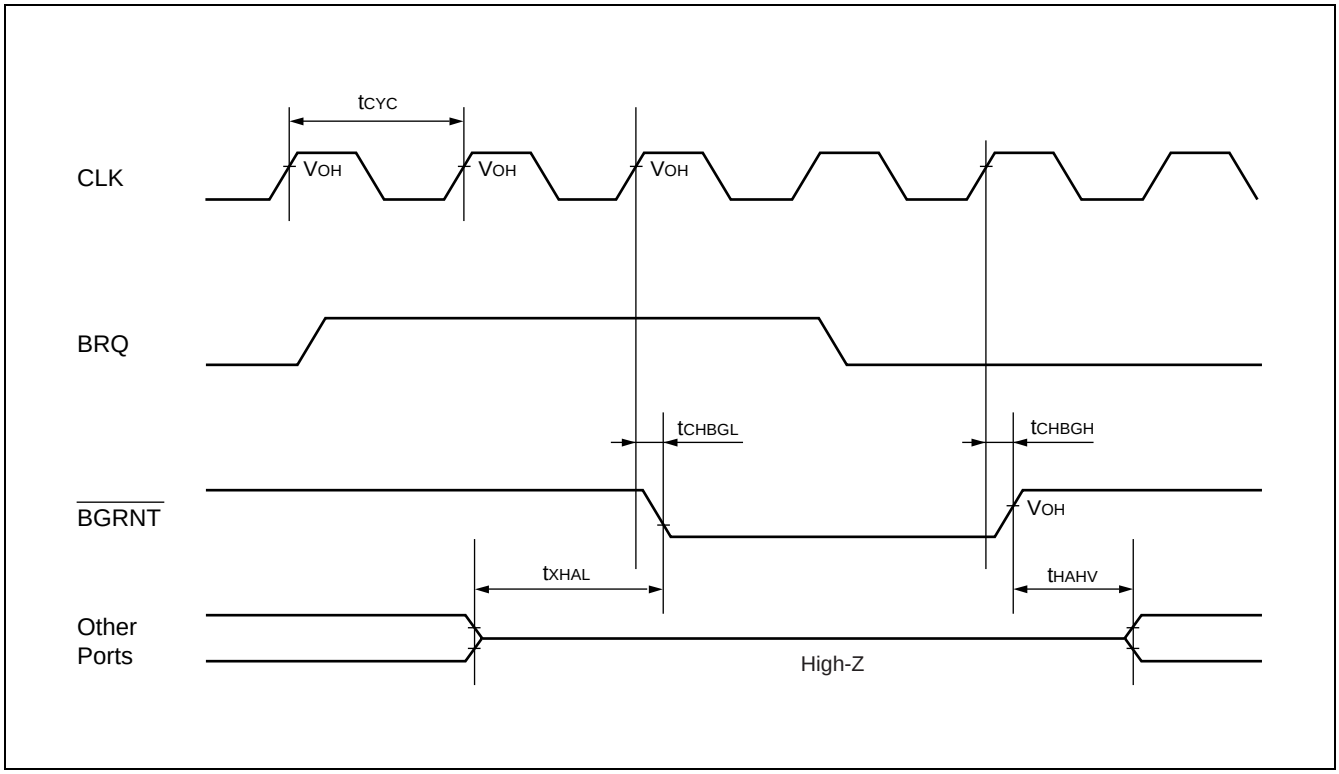
Signal	Symbol	Pin name	Value		Unit
			Min.	Max.	
RDY setup	t_{RDYS}	CLK RDY	16	—	ns
RDY hold	t_{RDYH}	CLK RDY	0	—	ns



• **$\overline{\text{BGRNT}}$**

(V_{DD} = 4.25 V to 5.25 V, T_A = –40 °C to +85 °C)

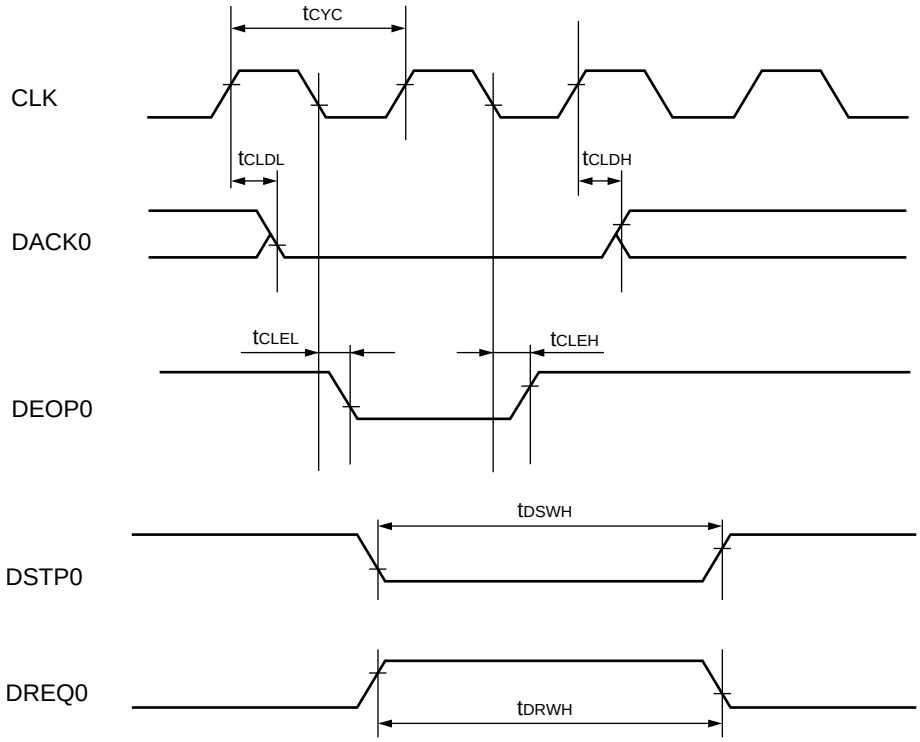
Signal	Symbol	Pin name	Value		Unit
			Min.	Max.	
$\overline{\text{BGRNT}}$	t_{CHBGL}	CLK $\overline{\text{BGRNT}}$	—	10	ns
$\overline{\text{BGRNT}}$	t_{CHBGH}		—	10	ns
Bus access enabled $\overline{\text{BGRNT}}$ falling	t_{XHAL}	$\overline{\text{BGRNT}}$	tcyc – 15	tcyc + 15	ns
Bus access disabled $\overline{\text{BGRNT}}$ rising	t_{HAHV}		tcyc – 15	tcyc + 15	ns



• **DMA**

(V_{DD} = 4.25 V to 5.25 V, T_A = –40 °C to +85 °C)

Signal	Symbol	Pin name	Value		Unit
			Min.	Max.	
DREQ	t_{DRWH}	DREQ0	$5t_{CYC}$	—	ns
DSTP	t_{DSWH}	DSTP0*	$5t_{CYC}$	—	ns
DACK	t_{CLDL}	CLK DACK0	—	20	ns
	t_{CLDH}		—	20	
DEOP	t_{CLEL}	CLK DEOP0	—	20	ns
	t_{CLEH}		—	20	



* : DSTP and DEOP share a pin. The pin is possible to change DSTP and DEOP functions using a port function register.

■ PACKAGE THERMAL RESISTANCE INFORMATION

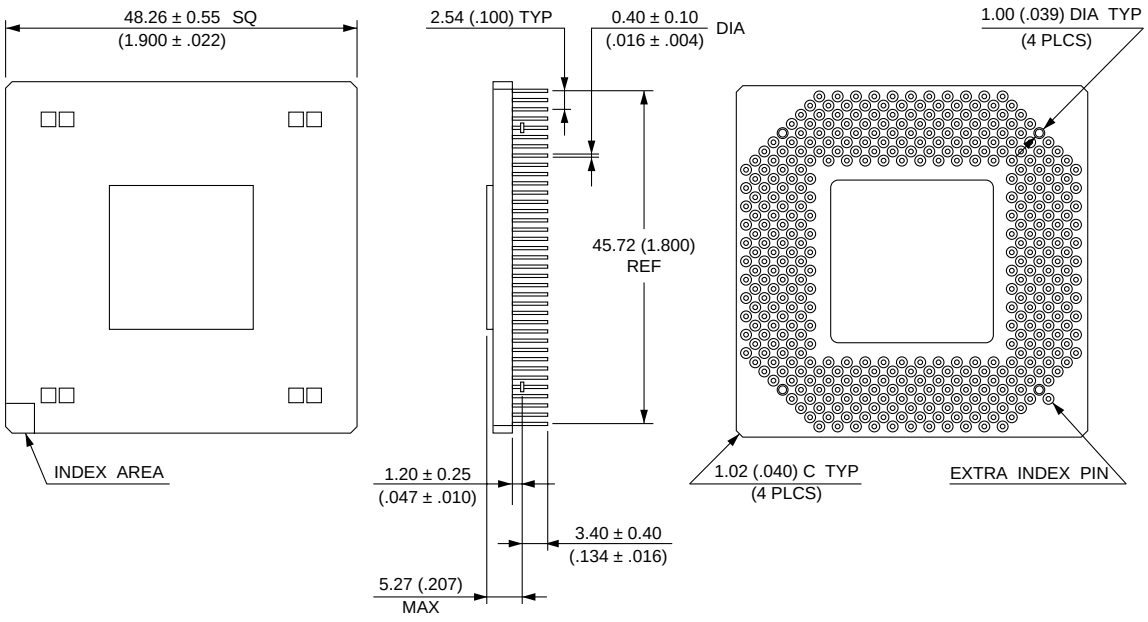
Package	Thermal Resistance [°C/W]			
	Theta-ja			Theta-jc
	0 m/s	1 m/s	3 m/s	
FPT-208P-M04	16	13	11	2.5
PGA-401C-A02	16	8.5	5.5	—

■ ORDERING INFORMATION

Part number	Package	Remarks
MB91FV360GACR	401-pin Ceramic PGA (PGA-401C-A02)	
MB91F361GAPFVS	208-pin Plastic QFP (FPT-208P-M04)	
MB91F362GAPFVS	208-pin Plastic QFP (FPT-208P-M04)	

■ PACKAGE DIMENSIONS

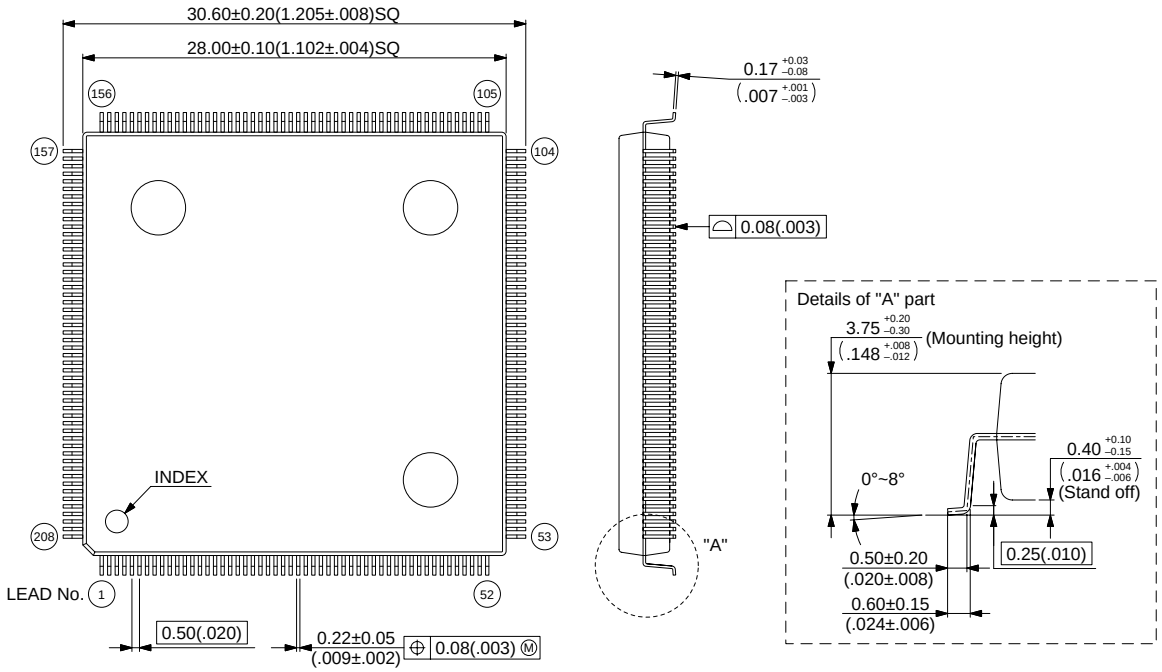
401-pin ceramic PGA
(PGA-401C-A02)



Dimensions in mm (inches).

208-pin plastic QFP
(FPT-208P-M04)

Note : Pins width and pins thickness include plating thickness.



Dimensions in mm (inches).

Note : The design may be modified changed without notice, contact to Fujitsu sales division when using the device.

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