FUJITSU SEMICONDUCTOR
DATA SHEET

DS705-00010-2v0-E

32-bit Microcontroller

FR Family FR81S

MB91590 Series

MB91F591B/F591BS/F591BH/F591BHS/F592B/F592BS/F592BH/F592BHS
MB91F594B/F594BS/F594BH/F594BHS/F596B*/F596BS*/F596BH*/F596BHS*
MB91F597B*/F597BS*/F597BH*/F597BHS*/F599B*/F599BS*/F599BH*/F599BHS*
***:** Under consideration

■ OVERVIEW

This series is Fujitsu 32-bit microcontroller designed for automotive and industrial control applications. It contains the FR81S CPU that is compatible with the FR family. The FR81S has a high level performance among the Fujitsu FR family by enhancing CPU instruction pipeline and load store processing, and improving internal bus transfer.
It is best suited for application control for automotive.

Note: FR, the abbreviation of FUJITSU RISC controller, is a line of products of Fujitsu Semiconductor Limited.

For the information for microcontroller supports, see the following web site.

http://edevice.fujitsu.com/micom/en-support/

2012.1

■ FEATURES

● FR81S CPU Core

- 32-bit RISC, load/store architecture, pipeline 5-stage structure
- Maximum operating frequency: 128 MHz (Source oscillation = 4.0 MHz and 32 multiplied (PLL clock multiplication system))
- General-purpose register : 32 bits ×16 sets
- 16-bit fixed length instructions (basic instruction), 1 instruction per cycle
- Instructions appropriate to embedded applications
  - Memory-to-memory transfer instruction
  - Bit processing instruction
  - Barrel shift instruction etc.
- High-level language support instructions
  - Function entry/exit instructions
  - Register content multi-load and store instructions
- Bit search instructions
  - Logical 1 detection, 0 detection, and change-point detection
- Branch instructions with delay slot
  - Reduced overhead during branch process
- Register interlock function
  - Easy assembler writing
- The support at the built-in / instruction level of the multiplier
  - Signed 32-bit multiplication : 5 cycles
  - Signed 16-bit multiplication : 3 cycles
- Interrupt (PC/PS saving)
  - 6 cycles (16 priority levels)
- The Harvard architecture allows simultaneous execution of program and data access.
- Instruction compatibility with the FR Family
- Built-in memory protection function (MPU)
  - Eight protection areas can be specified commonly for instructions and the data.
  - Control access privilege in both privilege mode and user mode.
- Built-in FPU (floating point arithmetic)
  - IEEE754 compliant
  - Floating-point register 32-bit × 16 sets

● Peripheral functions

- Clock generation (equipped with SSCG function)
  - Main oscillation (4MHz)
  - Sub oscillation (32KHz) or none sub oscillation
  - PLL multiplication rate : 1 to 32 times
- Built-in Program flash memory capacity 1024 + 64KB
- Built-in Data flash memory capacity(WorkFlash) 64KB
- Built-in RAM capacity
  - Main RAM 64KB
  - Backup RAM 8KB
- General-purpose ports (5V Pin) : 63 (dual clock products : 61)
  - Included I^2C pseudo open drain support ports : 4
- General-purpose ports (3V Pin) : 93
  - Included 48 combined external bus interface (For GDC external memory I/F)
- External bus interface
  - GDC external memory for I/F use
  - 25-bit address, 16-bit data
  - Power supply voltage fixed to 3.3V
- DMA Controller
  - Up to 16 channels can be started simultaneously.
  - 2 transfer factors (Internal peripheral request and software)

- A/D converter (successive approximation type)
  - 8/10-bit resolution : 32 channels
  - Conversion time : 3µs
- External interrupt input: 16 channels
  - Level ("H" / "L"), or edge detection (rising or falling) enabled
- LIN-UART
  - 6 channels, ch.2 to ch.7
  - UART, synchronous mode, LIN-UART mode is selectable.
  - LIN protocol Revision 2.1 is supported
  - SPI (Serial Peripheral Interface) supported (synchronous mode)
  - Full-duplex double buffering system
  - LIN synch break detection (linked to the input capture)
  - Built-in dedicated baud rate generator
  - DMA transfer support
- Multi-function serial communication (built-in transmission/reception FIFO memory) : 2 channels

  < UART (Asynchronous serial interface) >
  - Full-duplex double buffering system, 16-byte transmission FIFO memory, 16-byte reception FIFO memory
  - Parity or no parity is selectable.
  - Built-in dedicated baud rate generator
  - An external clock can be used as the transfer clock
  - Parity, frame, and overrun error detect functions provided
  - DMA transfer support

  <CSIO (Synchronous serial interface) >
  - Full-duplex double buffering system, 16-byte transmission FIFO memory, 16-byte reception FIFO memory
  - SPI supported; master and slave systems supported; 5 to 9-bit data length can be set.
  - Built-in dedicated baud rate generator (Master operation)
  - An external clock can be entered. (Slave operation)
  - Overrun error detect function is provided
  - DMA transfer support

  <LIN-UART (Asynchronous Serial Interface for LIN) >
  - Full-duplex double buffering system, 16-byte transmission FIFO memory, 16-byte reception FIFO memory
  - LIN protocol Revision 2.1 supported
  - Master and slave systems supported
  - Framing error and overrun error detection
  - LIN synch break generation and detection; LIN synch delimiter generation
  - Built-in dedicated baud rate generator
  - An external clock can be adjusted by the reload counter
  - DMA transfer support

  < I^2C >
  - Full-duplex double buffering system, 16-byte transmission FIFO memory, 16-byte reception FIFO memory
  - Standard mode (Max. 100kbps) / high-speed mode (Max. 400kbps) supported
  - DMA transfer supported (for transmission only)
- CAN Controller (C-CAN) : 3 channels
  - Transfer speed : Up to 1Mbps
  - 64-transmission/reception message buffering : 1 channel,
    32-transmission/reception message buffering : 2 channels
- PPG : 16-bit × 24 channels
- Reload timer : 16-bit × 4 channels
- Free-run timer : 32-bit × 2 channels (Can select each channel for input capture, output compare)
  32-bit × 2 channels (LSYN (LIN synch field detection) for exclusive input capture)
- Input capture : 32-bit × 6 channels (linked to the free-run timer) LSYN (LIN synch field detected)
  Exclusive 32-bit × 2 channels (linked to the free-run timer)
- Output compare : 32-bit × 4 channels (linked to the free-run timer)
- Sound generator : 5 channels
  - Frequency and amplitude sequencers provided

- Stepping motor controller : 6 channels
  - 8/10-bit PWM
  - High current output supported (4 lines × 6 channels)
  - Can refer back electromotive force using pin-shared A/D converter
- Real-time clock (RTC) (for day, hours, minutes, seconds)
  - Main/sub oscillation frequency can be selected for the operation clock (dual product only)
- Calibration: The hardware watchdog for CR oscillation drive and real-time clock (RTC) for sub clock drive (dual product only)
  - The CR oscillation frequency can be trimmed
  - The main clock to sub clock (dual product only) ratio can be corrected by setting the real-time clock prescaler
- Clock Supervisor
  - Monitoring abnormality (damage of crystal etc.) of sub oscillation (32KHz) (two system clock kinds) of the outside and main oscillation (4 MHz)
  - When abnormality is detected, it switches to the CR clock.
- Base timer : 2 channels
  - 16-bit timer
  - Any of four PWM/PPG/PWC/reload timer functions can be selected and used
  - A 32-bit timer can be used in 2 channels of cascade mode
- CRC generation
- Watchdog timer
  - Hardware watchdog
  - Software watchdog
- NMI
- Interrupt controller
- Interrupt request batch read
  - Multiple interrupts from peripherals can be read by a series of registers.
- I/O relocation
  - Peripheral function pins can be reassigned.
- Low-power consumption mode
  - Sleep / Stop / Watch / Sub RUN mode
  - Stop (power shutdown) / Watch (power shutdown) mode
  - GDC part self-support power supply
- Power on reset
- Low-voltage detection reset(external low-voltage detection)
- Low-voltage detection reset(internal low-voltage detection)
- GDC
  - Internal/memory frequency : 81MHz
  - The resolution of the display which can support : 800 × 480 at the maximum
    Screen overlay of five simultaneous layers at the maximum (window)
    Size of the resolution which can be supported varies depending on color format.
  - Analog video input (NTSC)
  - Digital video input (RGB666/555)
  - YUV input (BT.656)
  - Video image expansion/reduction /invert function is supported
  - RGB Digital output (6-bit × 3)
  - Built-in 2D rendering engine
    The line drawing is supported.
    The Bitblt function is supported.
    Display list operation is supported
    8bpp indirect color
    ARGB-1555 direct color
    Alpha blending, anti-aliasing

- Built-in Sprite engine
  Equipped with automatic display function when booted
  Maximum of 512 sprites are supported
  32 special sprites capable of automatic animation are supported.
  The command list execution is supported.
  1bpp, 2bpp, 4bpp, 8bpp indirect color
  ARGB-1555, RGB-565, ARGB-8888 direct color
  The color format for each sprite can be set.
  Horizontal invert, Vertical invert
  Alpha blending

- Built-in memory (800KB)

- Device Package : LQFP-208, HQFP-208*
- CMOS 90nm Technology
- Power supplies
  - 5V/3.3V Power supply
  - The internal 1.2V is generated from 5V/3.3V with the depression circuit.
  - I/O of an external bus and GDC, 3.3V power supply used.
  - For other I/O, 5V power supply used.
  - If 2 power supplies are used, they must turn on in the specified sequence (5V →3.3V) .

*: Under consideration. For detailed information about mount conditions, contact your sales representative.

■ PRODUCT LINEUP

Item \ Product		MB91F591B/S	MB91F591BH/S
CPU core		FR81S	
Technology		90nm	
Package		LQFP208	
Sub clock		Yes (Non-S series) No (S series)	
Maximum CPU operating frequency		80MHz	
Maximum GDC operating frequency		81MHz	
Built-in CR oscillator		100kHz	
System clock		On chip PLL	
Flash	Main	576KB	
	Sub	64KB	
RAM	Main	40KB	
	Backup	8KB	
VRAM		260KB	
Watchdog timer		1ch Hardware 1ch Software	
Clock supervisor		Initial value "ON"	Initial value "OFF"
Low-voltage detection reset (External low-voltage detection)		Yes	
Low-voltage detection reset (Internal low-voltage detection)		Yes	
NMI function		Yes	
DMA Controller		16ch	
CAN		1ch (64msg) 2ch (32msg)	
USART		LINx6 MFSx2	
A/D converter (8bit/10bit)		1unit/32ch	
Reload timer(16bit)		4ch	
Base timer(16bit)		2ch	
Free-run timer(32bit)		2ch	
Input capture(32bit)		6ch	
Output compare(32bit)		4ch	
PPG timer(16bit)		24ch	
Sound generator		5ch	
Real-time clock		Yes	
External interrupt		16ch	
CR/SUB compensation function		Yes	
CRC generation		Yes	
Stepping motor control		6ch	

Item \ Product	MB91F591B/S	MB91F591BH/S
Stop mode (including power shut-off)	Supported	
Power supply voltage	MICOM : 4.5V to 5.5V GDC : 3.0V to 3.6V	
Operating temperature	-40°C to +105°C	
Allowable power [mW]	1250	
Others	Flash product	
On chip debugger	Yes	

Item \ Product		MB91F592B/S	MB91F592BH/S	MB91F594B/S	MB91F594BH/S
CPU core		FR81S			
Technology		90nm			
Package		LQFP208			
Sub clock		Yes (Non-S series) No (S series)			
Maximum CPU operating frequency		80MHz			
Maximum GDC operating frequency		81MHz			
Built-in CR oscillator		100kHz			
System clock		On chip PLL			
Flash	Main	576KB		1088KB	
	Sub	64KB			
RAM	Main	40KB		64KB	
	Backup	8KB			
VRAM		800KB			
Watchdog timer		1ch Hardware 1ch Software			
Clock supervisor		Initial value "ON"	Initial value "OFF"	Initial value "ON"	Initial value "OFF"
Low-voltage detection reset (External low-voltage detection)		Yes			
Low-voltage detection reset (Internal low-voltage detection)		Yes			
NMI function		Yes			
DMA Controller		16ch			
CAN		1ch (64msg) 2ch (32msg)			
USART		LINx6 MFSx2			
A/D converter (8bit/10bit)		1unit/32ch			
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Base timer(16bit)		2ch			
Free-run timer(32bit)		2ch			
Input capture(32bit)		6ch			
Output compare(32bit)		4ch			
PPG timer(16bit)		24ch			
Sound generator		5ch			
Real-time clock		Yes			
External interrupt		16ch			
CR/SUB compensation function		Yes			
CRC generation		Yes			
Stepping motor control		6ch			

Item \ Product	MB91F592B/S	MB91F592BH/S	MB91F594B/S	MB91F594BH/S
Stop mode (including power shut-off)	Supported			
Power supply voltage	MICOM:4.5V to 5.5V GDC:3.0V to 3.6V			
Operating temperature	-40°C to +105°C			
Allowable power [mW]	1250			
Others	Flash product			
On chip debugger	Yes			

Item \ Product		MB91F596B/S*	MB91F596BH/S*	MB91F597B/S*	MB91F597BH/S*
CPU core		FR81S			
Technology		90nm			
Package		HQFP208			
Sub clock		Yes (Non-S series) No (S series)			
Maximum CPU operating frequency		128MHz			
Maximum GDC operating frequency		81MHz			
Built-in CR oscillator		100kHz			
System clock		On chip PLL			
Flash	Main	576KB			
	Sub	64KB			
RAM	Main	40KB			
	Backup	8KB			
VRAM		260KB		800KB	
Watchdog timer		1ch Hardware 1ch Software			
Clock supervisor		Initial value "ON"	Initial value "OFF"	Initial value "ON"	Initial value "OFF"
Low-voltage detection reset (External low-voltage detection)		Yes			
Low-voltage detection reset (Internal low-voltage detection)		Yes			
NMI function		Yes			
DMA Controller		16ch			
CAN		1ch (64msg) 2ch (32msg)			
USART		LINx6 MFSx2			
A/D converter (8bit/10bit)		1unit/32ch			
Reload timer(16bit)		4ch			
Base timer(16bit)		2ch			
Free-run timer(32bit)		2ch			
Input capture(32bit)		6ch			
Output compare(32bit)		4ch			
PPG timer(16bit)		24ch			
Sound generator		5ch			
Real-time clock		Yes			
External interrupt		16ch			
CR/SUB compensation function		Yes			
CRC generation		Yes			
Stepping motor control		6ch			

Item \ Product	MB91F596B/S*	MB91F596BH/S*	MB91F597B/S*	MB91F597BH/S*
Stop mode (including power shut-off)	Supported			
Power supply voltage	MICOM:4.5V to 5.5V GDC:3.0V to 3.6V			
Operating temperature	-40°C to +105°C			
Allowable power [mW]	2500			
Others	Flash product			
On chip debugger	Yes			

*: Under consideration. For detailed information about mount conditions, contact your sales representative.

Item \ Product		MB91F599B/S*	MB91F599BH/S*
CPU core		FR81S	
Technology		90nm	
Package		HQFP208	
Sub clock		Yes (Non-S series) No (S series)	
Maximum CPU operating frequency		128MHz	
Maximum GDC operating frequency		81MHz	
Built-in CR oscillator		100kHz	
System clock		On chip PLL	
Flash	Main	1088KB	
	Sub	64KB	
RAM	Main	64KB	
	Sub	8KB	
VRAM		800KB	
Watchdog timer		1ch Hardware 1ch Software	
Clock supervisor		Initial value "ON"	Initial value "OFF"
Low-voltage detection reset (External low-voltage detection)		Yes	
Low-voltage detection reset (Internal low-voltage detection)		Yes	
NMI function		Yes	
DMA Controller		16ch	
CAN		1ch (64msg) 2ch (32msg)	
USART		LINx6 MFSx2	
A/D Converter (8bit/10bit)		1unit/32ch	
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Input capture(32bit)		6ch	
Output compare(32bit)		4ch	
PPG timer(16bit)		24ch	
Sound generator		5ch	
Real-time clock		Yes	
External interrupt		16ch	
CR/SUB compensation function		Yes	
CRC generation		Yes	
Stepping motor control		6ch	

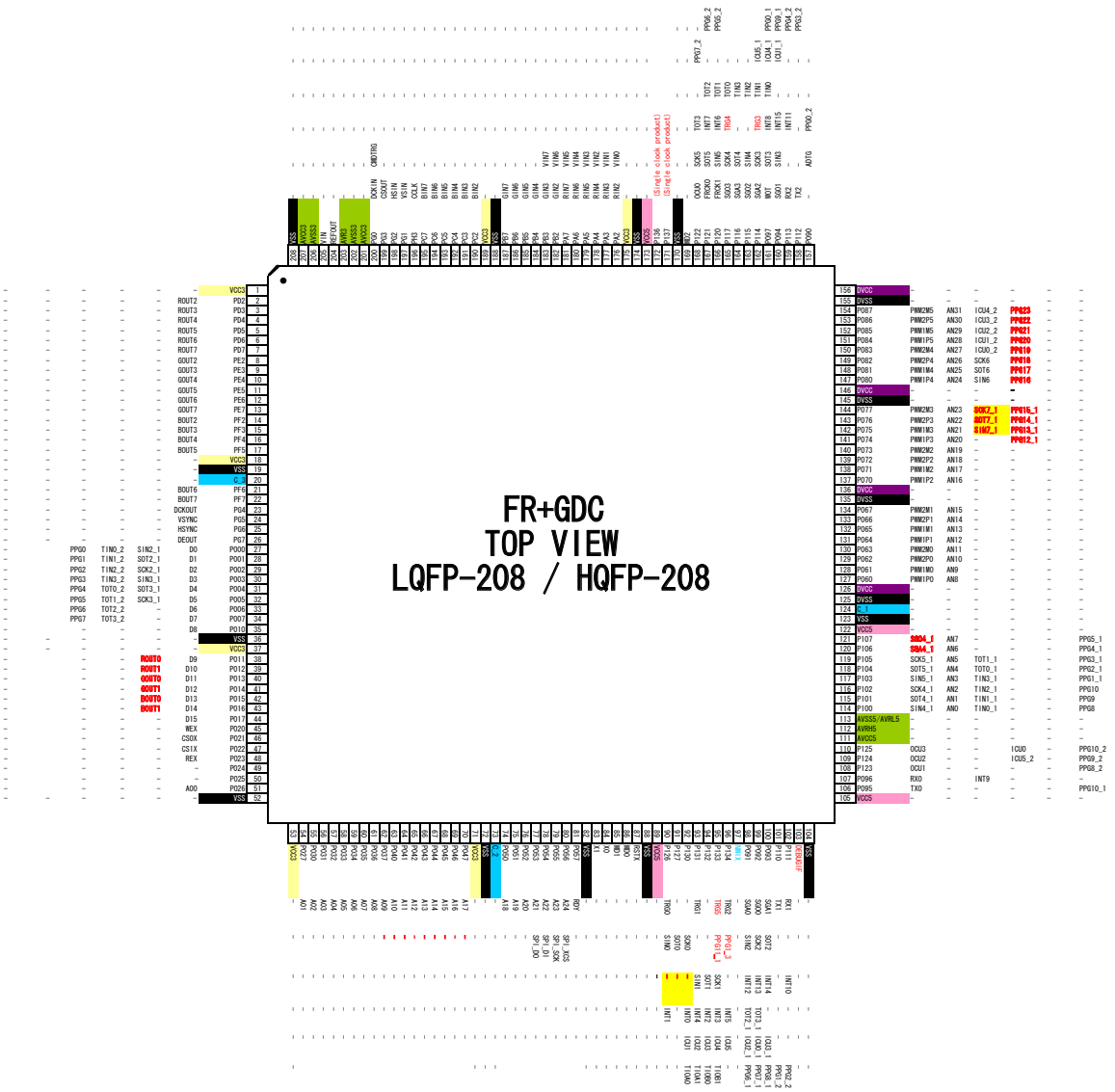
Item \ Product	MB91F599B/S*	MB91F599BH/S*
Stop mode (including power shut-off)	Supported	
Power supply voltage	MICOM:4.5V to 5.5V GDC:3.0V to 3.6V	
Operating temperature	-40°C to +105°C	
Allowable power [mW]	2500	
Others	Flash product	
On chip debugger	Yes	

*: Under consideration. For detailed information about mount conditions, contact your sales representative.

■ PIN ASSIGNMENT

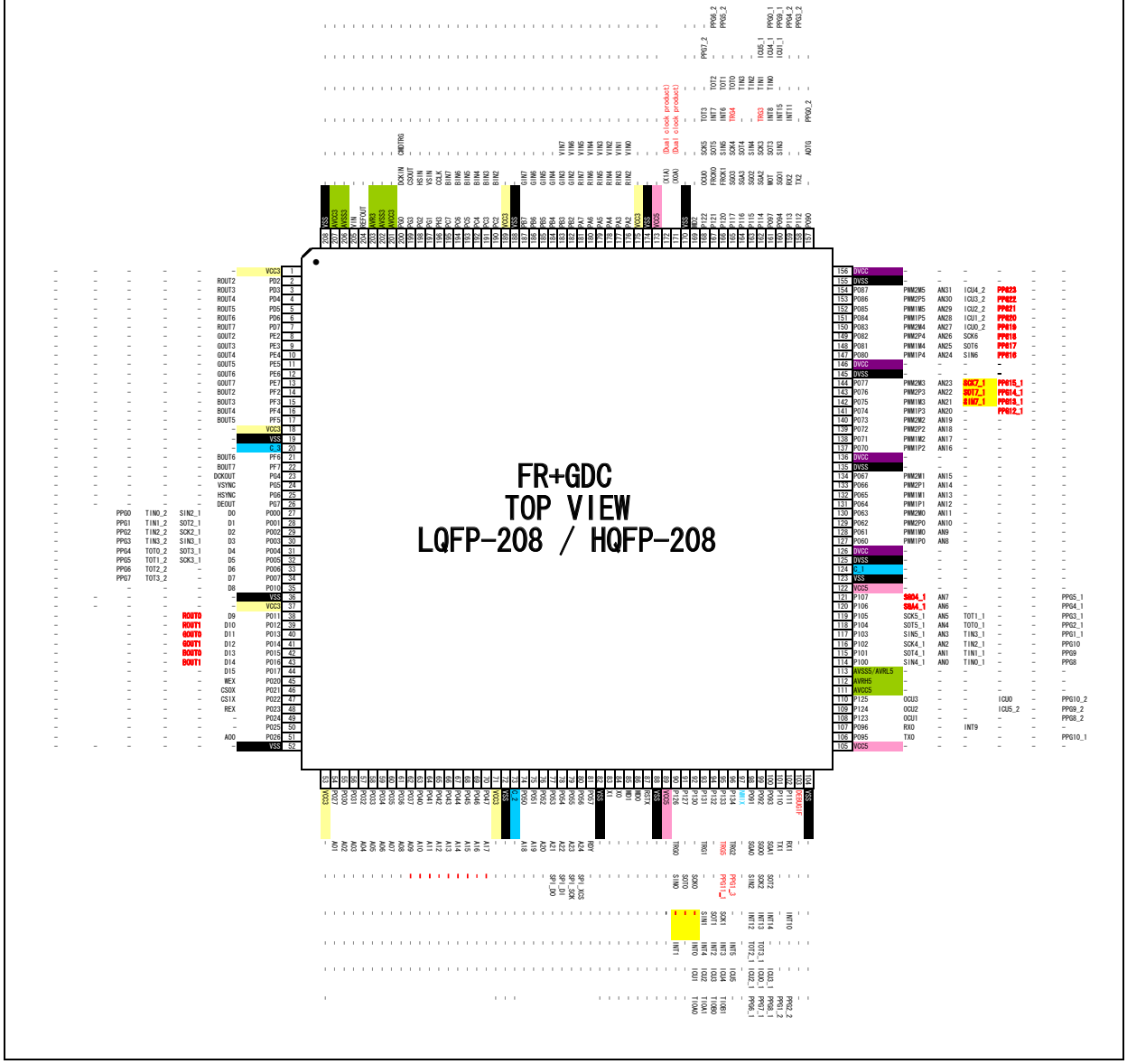
● Pin Assignment (single clock product)

(TOP VIEW)



● Pin Assignment (dual clock product)

(TOP VIEW)



■ PIN DESCRIPTION

Pin no.	Pin Name	Polarity	I/O circuit types*1	Function *2
84	X0	–	L	Main clock oscillation input pin
83	X1	–	L	Main clock oscillation output pin
171 (dual clock product)	X0A	–	N	Sub clock oscillation input pin
172 (dual clock product)	X1A	–	N	Sub clock oscillation output pin
171 (single clock product)	P137	–	A	General-purpose I/O port
172 (single clock product)	P136	–	A	General-purpose I/O port
97	NMIX	N	F1	Non-masking interrupt input pin
170	VSS	–	–	GND pin
87	RSTX	N	F1	External reset input pin
86	MD0	–	P	Mode pin 0
85	MD1	–	P	Mode pin 1
169	MD2	–	F2	Mode pin 2
27	P000	–	O	General-purpose I/O port (3V pin)
	D0	–		External bus · Data bit0 I/O pin
	SIN2_1	–		LIN-UART ch.2 serial data input pin (1)
	TIN0_2	–		Reload timer ch.0 event input pin (2)
	PPG0	–		PPG ch.0 output pin
28	P001	–	O	General-purpose I/O port (3V pin)
	D1	–		External bus · Data bit1 I/O pin
	SOT2_1	–		LIN-UART ch.2 serial data output pin (1)
	TIN1_2	–		Reload timer ch.1 event input pin (2)
	PPG1	–		PPG ch.1 output pin

Pin no.	Pin Name	Polarity	I/O circuit types*1	Function *2
29	P002	–	O	General-purpose I/O port (3V pin)
	D2	–		External bus · Data bit2 I/O pin
	SCK2_1	–		LIN-UART ch.2clock I/O pin (1)
	TIN2_2	–		Reload timer ch.2 event input pin (2)
	PPG2	–		PPG ch.2 output pin
30	P003	–	O	General-purpose I/O port (3V pin)
	D3	–		External bus · Data bit3 I/O pin
	SIN3_1	–		LIN-UART ch.3 serial data input pin (1)
	TIN3_2	–		Reload timer ch.3 event input pin (2)
	PPG3	–		PPG ch.3 output pin
31	P004	–	O	General-purpose I/O port (3V pin)
	D4	–		External bus · Data bit4 I/O pin
	SOT3_1	–		LIN-UART ch.3 serial data output pin (1)
	TOT0_2	–		Reload timer ch.0 output pin (2)
	PPG4	–		PPG ch.4 output pin
32	P005	–	O	General-purpose I/O port (3V pin)
	D5	–		External bus · Data bit5 I/O pin
	SCK3_1	–		LIN-UART ch.3 clock I/O pin (1)
	TOT1_2	–		Reload timer ch.1 output pin (2)
	PPG5	–		PPG ch.5 output pin
33	P006	–	O	General-purpose I/O port (3V pin)
	D6	–		External bus · Data bit6 I/O pin
	TOT2_2	–		Reload timer ch.2 output pin (2)
	PPG6	–		PPG ch.6 output pin
34	P007	–	O	General-purpose I/O port (3V pin)
	D7	–		External bus · Data bit7 I/O pin
	TOT3_2	–		Reload timer ch.3 output pin (2)
	PPG7	–		PPG ch.7 output pin
35	P010	–	O	General-purpose I/O port (3V pin)
	D8	–		External bus · Data bit8 I/O pin
38	P011	–	O	General-purpose I/O port (3V pin)
	D9	–		External bus · Data bit9 I/O pin
	ROUT0	–		Display digital R0 output pin

Pin no.	Pin Name	Polarity	I/O circuit types*1	Function *2
39	P012	–	O	General-purpose I/O port (3V pin)
	D10	–		External bus · Data bit10 I/O pin
	ROUT1	–		Display digital R1 output pin
40	P013	–	O	General-purpose I/O port (3V pin)
	D11	–		External bus · Data bit11 I/O pin
	GOUT0	–		Display digital G0 output pin
41	P014	–	O	General-purpose I/O port (3V pin)
	D12	–		External bus · Data bit12 I/O pin
	GOUT1	–		Display digital G1 output pin
42	P015	–	O	General-purpose I/O port (3V pin)
	D13	–		External bus · Data bit13 I/O pin
	BOUT0	–		Display digital B0 output pin
43	P016	–	O	General-purpose I/O port (3V pin)
	D14	–		External bus · Data bit14 I/O pin
	BOUT1	–		Display digital B1 output pin
44	P017	–	O	General-purpose I/O port (3V pin)
	D15	–		External bus · Data bit15 I/O pin
45	P020	–	O	General-purpose I/O port (3V pin)
	WEX	–		External bus · Write enable output pin
46	P021	–	O	General-purpose I/O port (3V pin)
	CS0X	–		External bus · Chip select 0 output pin
47	P022	–	O	General-purpose I/O port (3V pin)
	CS1X	–		External bus · Chip select 1 output pin
48	P023	–	O	General-purpose I/O port (3V pin)
	REX	–		External bus · Read enable output pin
49	P024	–	O	General-purpose I/O port (3V pin)
50	P025	–	O	General-purpose I/O port (3V pin)
51	P026	–	O	General-purpose I/O port (3V pin)
	A00	–		External bus · Address bit0 output pin
54	P027	–	O	General-purpose I/O port (3V pin)
	A01	–		External bus · Address bit1 output pin
55	P030	–	O	General-purpose I/O port (3V pin)
	A02	–		External bus · Address bit2 output pin
56	P031	–	O	General-purpose I/O port (3V pin)
	A03	–		External bus · Address bit3 output pin

Pin no.	Pin Name	Polarity	I/O circuit types*1	Function *2
57	P032	–	O	General-purpose I/O port (3V pin)
	A04	–		External bus · Address bit4 output pin
58	P033	–	O	General-purpose I/O port (3V pin)
	A05	–		External bus · Address bit5 output pin
59	P034	–	O	General-purpose I/O port (3V pin)
	A06	–		External bus · Address bit6 output pin
60	P035	–	O	General-purpose I/O port (3V pin)
	A07	–		External bus · Address bit7 output pin
61	P036	–	O	General-purpose I/O port (3V pin)
	A08	–		External bus · Address bit8 output pin
62	P037	–	O	General-purpose I/O port (3V pin)
	A09	–		External bus · Address bit9 output pin
63	P040	–	O	General-purpose I/O port (3V pin)
	A10	–		External bus · Address bit10 output pin
64	P041	–	O	General-purpose I/O port (3V pin)
	A11	–		External bus · Address bit11 output pin
65	P042	–	O	General-purpose I/O port (3V pin)
	A12	–		External bus · Address bit12 output pin
66	P043	–	O	General-purpose I/O port (3V pin)
	A13	–		External bus · Address bit13 output pin
67	P044	–	O	General-purpose I/O port (3V pin)
	A14	–		External bus · Address bit14 output pin
68	P045	–	O	General-purpose I/O port (3V pin)
	A15	–		External bus · Address bit15 output pin
69	P046	–	O	General-purpose I/O port (3V pin)
	A16	–		External bus · Address bit16 output pin
70	P047	–	O	General-purpose I/O port (3V pin)
	A17	–		External bus · Address bit17 output pin
74	P050	–	O	General-purpose I/O port (3V pin)
	A18	–		External bus · Address bit18 output pin
75	P051	–	O	General-purpose I/O port(3V pin)
	A19	–		External bus · Address bit19 output pin
76	P052	–	O	General-purpose I/O port(3V pin)
	A20	–		External bus · Address bit20 output pin

Pin no.	Pin Name	Polarity	I/O circuit types*1	Function *2
77	P053	–	O	General-purpose I/O port(3V pin)
	A21	–		External bus · Address bit21 output pin
	SPI_DO	–		SPI data output pin
78	P054	–	O	General-purpose I/O port (3V pin)
	A22	–		External bus · Address bit22 output pin
	SPI_DI	–		SPI data input pin
79	P055	–	O	General-purpose I/O port (3V pin)
	A23	–		External bus · Address bit23 output pin
	SPI_SCK	–		SPI clock output pin
80	P056	–	O	General-purpose I/O port (3V pin)
	A24	–		External bus · Address bit24 output pin
	SPI_XCS	–		SPI chip select output pin
81	P057	–	O	General-purpose I/O port (3V pin)
	RDY	–		External bus · Wait input pin
127	P060	–	E	General-purpose I/O port
	PWM1P0	–		SMC ch.0 output pin
	AN8	–		ADC Analog 8 input pin
128	P061	–	E	General-purpose I/O port
	PWM1M0	–		SMC ch.0 output pin
	AN9	–		ADC Analog 9 input pin
129	P062	–	E	General-purpose I/O port
	PWM2P0	–		SMC ch.0 output pin
	AN10	–		ADC Analog 10 input pin
130	P063	–	E	General-purpose I/O port
	PWM2M0	–		SMC ch.0 output pin
	AN11	–		ADC Analog 11 input pin
131	P064	–	E	General-purpose I/O port
	PWM1P1	–		SMC ch.1 output pin
	AN12	–		ADC Analog 12 input pin
132	P065	–	E	General-purpose I/O port
	PWM1M1	–		SMC ch.1 output pin
	AN13	–		ADC Analog 13 input pin

Pin no.	Pin Name	Polarity	I/O circuit types*1	Function *2
133	P066	–	E	General-purpose I/O port
	PWM2P1	–		SMC ch.1 output pin
	AN14	–		ADC Analog 14 input pin
134	P067	–	E	General-purpose I/O port
	PWM2M1	–		SMC ch.1 output pin
	AN15	–		ADC Analog 15 input pin
137	P070	–	E	General-purpose I/O port
	PWM1P2	–		SMC ch.2 output pin
	AN16	–		ADC Analog 16 input pin
138	P071	–	E	General-purpose I/O port
	PWM1M2	–		SMC ch.2 output pin
	AN17	–		ADC Analog 17 input pin
139	P072	–	E	General-purpose I/O port
	PWM2P2	–		SMC ch.2 output pin
	AN18	–		ADC Analog 18 input pin
140	P073	–	E	General-purpose I/O port
	PWM2M2	–		SMC ch.2 output pin
	AN19	–		ADC Analog 19 input pin
141	P074	–	E	General-purpose I/O port
	PWM1P3	–		SMC ch.3 output pin
	AN20	–		ADC Analog 20 input pin
	PPG12_1	–		PPG ch.12 output pin (1)
142	P075	–	E	General-purpose I/O port
	PWM1M3	–		SMC ch.3 output pin
	AN21	–		ADC Analog 21 input pin
	SIN7_1	–		LIN-UART ch.7 serial data input pin
	PPG13_1	–		PPG ch.13 output pin (1)
143	P076	–	E	General-purpose I/O port
	PWM2P3	–		SMC ch.3 output pin
	AN22	–		ADC Analog 22 input pin
	SOT7_1	–		LIN-UART ch.7 serial data output pin
	PPG14_1	–		PPG ch.14 output pin (1)

Pin no.	Pin Name	Polarity	I/O circuit types*1	Function *2
144	P077	–	E	General-purpose I/O port
	PWM2M3	–		SMC ch.3 output pin
	AN23	–		ADC Analog 23 input pin
	SCK7_1	–		LIN-UART ch.7 clock I/O pin
	PPG15_1	–		PPG ch.15 output pin (1)
147	P080	–	E	General-purpose I/O port
	PWM1P4	–		SMC ch.4 output pin
	AN24	–		ADC Analog 24 input pin
	SIN6	–		LIN-UART ch.6 serial data input pin
	PPG16	–		PPG ch.16 output pin
148	P081	–	E	General-purpose I/O port
	PWM1M4	–		SMC ch.4 output pin
	AN25	–		ADC Analog 25 input pin
	SOT6	–		LIN-UART ch.6 serial data output pin
	PPG17	–		PPG ch.17 output pin
149	P082	–	E	General-purpose I/O port
	PWM2P4	–		SMC ch.4 output pin
	AN26	–		ADC Analog 26 input pin
	SCK6	–		LIN-UART ch.6 clock I/O pin
	PPG18	–		PPG ch.18 output pin
150	P083	–	E	General-purpose I/O port
	PWM2M4	–		SMC ch.4 output pin
	AN27	–		ADC Analog 27 input pin
	ICU0_2	–		Input capture ch.0 input pin (2)
	PPG19	–		PPG ch.19 output pin
151	P084	–	E	General-purpose I/O port
	PWM1P5	–		SMC ch.5 output pin
	AN28	–		ADC Analog 28 input pin
	ICU1_2	–		Input capture ch.1 input pin (2)
	PPG20	–		PPG ch.20 output pin

Pin no.	Pin Name	Polarity	I/O circuit types*1	Function *2
152	P085	–	E	General-purpose I/O port
	PWM1M5	–		SMC ch.5 output pin
	AN29	–		ADC Analog 29 input pin
	ICU2_2	–		Input capture ch.2 input pin (2)
	PPG21	–		PPG ch.21 output pin
153	P086	–	E	General-purpose I/O port
	PWM2P5	–		SMC ch.5 output pin
	AN30	–		ADC Analog 30 input pin
	ICU3_2	–		Input capture ch.3 input pin (2)
	PPG22	–		PPG ch.22 output pin
154	P087	–	E	General-purpose I/O port
	PWM2M5	–		SMC ch.5 output pin
	AN31	–		ADC Analog 31 input pin
	ICU4_2	–		Input capture ch.4 input pin (2)
	PPG23	–		PPG ch.23 output pin
157	P090	–	A	General-purpose I/O port
	ADTG	–		A/D convertor external trigger input pin
	PPG0_2	–		PPG ch.0 output pin (2)
98	P091	–	C	General-purpose I/O port
	SGA0	–		Sound generator ch.0 SGA output pin
	SIN2	–		LIN-UART ch.2 serial data input pin
	INT12	–		INT12 External interrupt input pin
	TOT2_1	–		Reload timer ch.2 output pin (1)
	ICU2_1	–		Input capture ch.2 input pin (1)
	PPG6_1	–		PPG ch.6 output pin (1)
99	P092	–	C	General-purpose I/O port
	SGO0	–		Sound generator ch.0 SGO output pin
	SCK2	–		LIN-UART ch.2 clock I/O pin
	INT13	–		INT13 External interrupt input pin
	TOT3_1	–		Reload timer ch.3 output pin (1)
	ICU0_1	–		Input capture ch.0 input pin (1)
	PPG7_1	–		PPG ch.7 output pin (1)

Pin no.	Pin Name	Polarity	I/O circuit types*1	Function *2
100	P093	–	C	General-purpose I/O port
	SGA1	–		Sound generator ch.1 SGA output pin
	SOT2	–		LIN-UART ch.2 serial data output pin
	INT14	–		INT14 External interrupt input pin
	ICU3_1	–		Input capture ch.3 input pin (1)
	PPG8_1	–		PPG ch.8 output pin (1)
160	P094	–	C	General-purpose I/O port
	SGO1	–		Sound generator ch.1 SGO output pin
	SIN3	–		LIN-UART ch.3 serial data input pin
	INT15	–		INT15 External interrupt input pin
	ICU1_1	–		Input capture ch1 input pin (1)
	PPG9_1	–		PPG ch.9 output pin (1)
106	P095	–	A	General-purpose I/O port
	TX0	–		CAN transmission data0 output pin
	PPG10_1	–		PPG ch.10 output pin (1)
107	P096	–	A	General-purpose I/O port
	RX0	–		CAN reception data0 input pin
	INT9	–		INT9 External interrupt input pin
161	P097	–	C	General-purpose I/O port
	WOT	–		RTC overflow output pin
	SOT3	–		LIN-UART ch.3 serial data output pin
	INT8	–		INT8 External interrupt input pin
	TIN0	–		Reload timer ch.0 event input pin
	ICU4_1	–		Input capture ch.4 input pin (1)
	PPG0_1	–		PPG ch.0 output pin (1)
114	P100	–	C	General-purpose I/O port
	SIN4_1	–		LIN-UART ch.4 serial data input pin (1)
	AN0	–		ADC Analog 0 input pin
	TIN0_1	–		Reload timer ch.0 event input pin (1)
	PPG8	–		PPG ch.8 output pin

Pin no.	Pin Name	Polarity	I/O circuit types*1	Function *2
115	P101	–	C	General-purpose I/O port
	SOT4_1	–		LIN-UART ch.4 serial data output pin (1)
	AN1	–		ADC Analog 1 input pin
	TIN1_1	–		Reload timer ch.1 event input pin (1)
	PPG9	–		PPG ch.9 output pin
116	P102	–	C	General-purpose I/O port
	SCK4_1	–		LIN-UART ch.4 clock I/O pin (1)
	AN2	–		ADC Analog 2 input pin
	TIN2_1	–		Reload timer ch.2 event input pin (1)
	PPG10	–		PPG ch.10 output pin
117	P103	–	C	General-purpose I/O port
	SIN5_1	–		LIN-UART ch.5 serial data input pin (1)
	AN3	–		ADC Analog 3 input pin
	TIN3_1	–		Reload timer ch.3 event input pin (1)
	PPG1_1	–		PPG ch.1 output pin (1)
118	P104	–	C	General-purpose I/O port
	SOT5_1	–		LIN-UART ch.5 serial data output pin (1)
	AN4	–		ADC Analog 4 input pin
	TOT0_1	–		Reload timer ch.0 output pin (1)
	PPG2_1	–		PPG ch.2 output pin (1)
119	P105	–	C	General-purpose I/O port
	SCK5_1	–		LIN-UART ch.5 clock I/O pin (1)
	AN5	–		ADC Analog 5 input pin
	TOT1_1	–		Reload timer ch.1 output pin (1)
	PPG3_1	–		PPG ch.3 output pin (1)
120	P106	–	C	General-purpose I/O port
	SGA4_1	–		Sound generator ch.4 SGA output pin
	AN6	–		ADC Analog 6 input pin
	PPG4_1	–		PPG ch.4 output pin (1)
121	P107	–	C	General-purpose I/O port
	SGO4_1	–		Sound generator ch.4 SGO output pin
	AN7	–		ADC Analog 7 input pin
	PPG5_1	–		PPG ch.5 output pin (1)

Pin no.	Pin Name	Polarity	I/O circuit types*1	Function *2
101	P110	–	C	General-purpose I/O port
	TX1	–		CAN transmission data1 output pin
	PPG1_2	–		PPG ch.1 output pin (2)
102	P111	–	C	General-purpose I/O port
	RX1	–		CAN reception data 1 input pin
	INT10	–		INT10 External interrupt input pin
	PPG2_2	–		PPG ch.2 output pin (2)
158	P112	–	C	General-purpose I/O port
	TX2	–		CAN transmission data 2 output pin
	PPG3_2	–		PPG ch.3 output pin (2)
159	P113	–	C	General-purpose I/O port
	RX2	–		CAN reception data 2 input pin
	INT11	–		INT11 External interrupt input pin
	PPG4_2	–		PPG ch.4 output pin (2)
162	P114	–	C	General-purpose I/O port
	SGA2	–		Sound generator ch.2 SGA output pin
	SCK3	–		LIN-UART ch.3 clock I/O pin
	TRG3	–		PPG trigger 3 input pin (ch.12 to ch.15)
	TIN1	–		Reload timer ch.1 event input pin
	ICU5_1	–		Input capture ch.5 input pin (1)
163	P115	–	C	General-purpose I/O port
	SGO2	–		Sound generator ch.2 SGO output pin
	SIN4	–		LIN-UART ch.4 serial data input pin
	TIN2	–		Reload timer ch.2 event input pin
164	P116	–	C	General-purpose I/O port
	SGA3	–		Sound generator ch.3 SGA output pin
	SOT4	–		LIN-UART ch.4 serial data output pin
	TIN3	–		Reload timer ch.3 event input pin
165	P117	–	C	General-purpose I/O port
	SGO3	–		Sound generator ch.3 SGO output pin
	SCK4	–		LIN-UART ch.4 clock I/O pin
	TRG4	–		PPG trigger 4 input pin (ch.16 to ch.19)
	TOT0	–		Reload timer ch.0 output pin

Pin no.	Pin Name	Polarity	I/O circuit types*1	Function *2
166	P120	–	C	General-purpose I/O port
	FRCK1	–		Free-run timer 1 clock input pin
	SIN5	–		LIN-UART ch.5 serial data input pin
	INT6	–		INT6 External interrupt input pin
	TOT1	–		Reload timer ch.1 output pin
	PPG5_2	–		PPG ch.5 output pin (2)
167	P121	–	C	General-purpose I/O port
	FRCK0	–		Free-run timer 0 clock input pin
	SOT5	–		LIN-UART ch.5 serial data output pin
	INT7	–		INT7 External interrupt input pin
	TOT2	–		Reload timer ch.2 output pin
	PPG6_2	–		PPG ch.6 output pin (2)
168	P122	–	C	General-purpose I/O port
	OCU0	–		Output compare ch.0 output pin
	SCK5	–		LIN-UART ch.5 clock I/O pin
	TOT3	–		Reload timer ch.3 output pin
	PPG7_2	–		PPG ch.7 output pin (2)
108	P123	–	A	General-purpose I/O port
	OCU1	–		Output compare ch.1 output pin
	PPG8_2	–		PPG ch.8 output pin (2)
109	P124	–	A	General-purpose I/O port
	OCU2	–		Output compare ch.2 output pin
	ICU5_2	–		Input capture ch.5 input pin (2)
	PPG9_2	–		PPG ch.9 output pin (2)
110	P125	–	A	General-purpose I/O port
	OCU3	–		Output compare ch.3 output pin
	ICU0	–		Input capture ch.0 input pin
	PPG10_2	–		PPG ch.10 output pin (2)
90	P126	–	A	General-purpose I/O port
	TRG0	–		PPG trigger 0 input pin (ch.0 to ch.3)
	SIN0	–		Multi-UART ch.0 serial data input pin
	INT1	–		INT1 External interrupt input pin

Pin no.	Pin Name	Polarity	I/O circuit types*1	Function *2
91	P127	–	K	General-purpose I/O port
	SOT0	–		Multi-UART ch.0 serial data output pin / I2C ch.0 serial data I/O pin
92	P130	–	K	General-purpose I/O port
	SCK0	–		Multi-UART ch.0 clock I/O pin / I2C ch.0 clock I/O pin
	INT0	–		INT0 External interrupt input pin
	ICU1	–		Input capture ch.1 input pin
	TIOA0	–		Base timer TIOA0 output pin
93	P131	–	A	General-purpose I/O port
	TRG1	–		PPG trigger 1 input pin (ch.4 to ch.7)
	SIN1	–		Multi-UART ch.1 serial data input pin
	INT4	–		INT4 External interrupt input pin
	ICU2	–		Input capture ch.2 input pin
	TIOA1	–		Base timer TIOA1 I/O pin
94	P132	–	K	General-purpose I/O port
	SOT1	–		Multi-UART ch.1 serial data output pin / I2C ch.1 serial data I/O pin
	INT2	–		INT2 External interrupt input pin
	ICU3	–		Input capture ch.3 input pin
	TIOB0	–		Base timer TIOB0 input pin
95	P133	–	K	General-purpose I/O port
	TRG5	–		PPG trigger 5 input pin (ch.20 to ch.23)
	PPG11_1	–		PPG ch.11 output pin (1)
	SCK1	–		Multi-UART ch.1 clock I/O pin / I2C ch.1 clock I/O pin
	INT3	–		INT3 External interrupt input pin
	ICU4	–		Input capture ch.4 input pin
	TIOB1	–		Base timer TIOB1 input pin
96	P134	–	A	General-purpose I/O port
	TRG2	–		PPG trigger 2 input pin (ch.8 to ch.11)
	PPG1_3	–		PPG ch.1 output pin (3)
	INT5	–		INT5 External interrupt input pin
	ICU5	–		Input capture ch.5 input pin
103	DEBUGIF	–	G	DEBUG I/F pin

Pin no.	Pin Name	Polarity	I/O circuit types*1	Function *2
176	PA2	–	O	General-purpose I/O port (3V pin)
	RIN2	–		Capture R2 input pin (RGB mode)
	VIN0	–		Capture VIN0 input pin (656 mode)
177	PA3	–	O	General-purpose I/O port (3V pin)
	RIN3	–		Capture R3 input pin (RGB mode)
	VIN1	–		Capture VIN1 input pin (656 mode)
178	PA4	–	O	General-purpose I/O port (3V pin)
	RIN4	–		Capture R4 input pin (RGB mode)
	VIN2	–		Capture VIN2 input pin (656 mode)
179	PA5	–	O	General-purpose I/O port (3V pin)
	RIN5	–		Capture R5 input pin (RGB mode)
	VIN3	–		Capture VIN3 input pin (656 mode)
180	PA6	–	O	General-purpose I/O port (3V pin)
	RIN6	–		Capture R6 input pin (RGB mode)
	VIN4	–		Capture VIN4 input pin (656 mode)
181	PA7	–	O	General-purpose I/O port (3V pin)
	RIN7	–		Capture R7 input pin (RGB mode)
	VIN5	–		Capture VIN5 input pin (656 mode)
182	PB2	–	O	General-purpose I/O port (3V pin)
	GIN2	–		Capture G2 input pin (RGB mode)
	VIN6	–		Capture VIN6 input pin (656 mode)
183	PB3	–	O	General-purpose I/O port (3V pin)
	GIN3	–		Capture G3 input pin (RGB mode)
	VIN7	–		Capture VIN7 input pin (656 mode)
184	PB4	–	O	General-purpose I/O port (3V pin)
	GIN4	–		Capture G4 input pin (RGB mode)
185	PB5	–	O	General-purpose I/O port (3V pin)
	GIN5	–		Capture G5 input pin (RGB mode)
186	PB6	–	O	General-purpose I/O port (3V pin)
	GIN6	–		Capture G6 input pin (RGB mode)
187	PB7	–	O	General-purpose I/O port (3V pin)
	GIN7	–		Capture G7 input pin (RGB mode)
190	PC2	–	O	General-purpose I/O port (3V pin)
	BIN2	–		Capture B2 input pin (RGB mode)

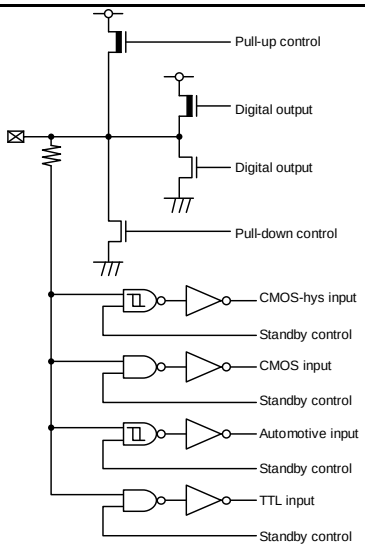
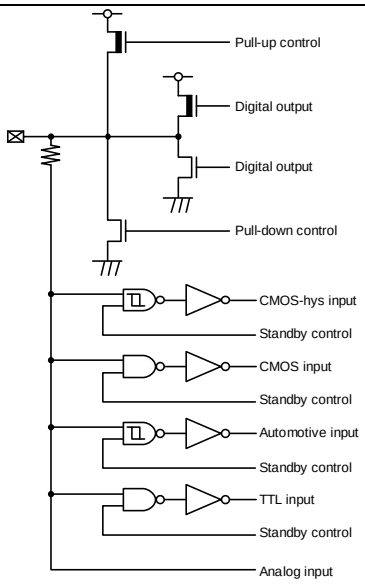
Pin no.	Pin Name	Polarity	I/O circuit types*1	Function *2
191	PC3	–	O	General-purpose I/O port (3V pin)
	BIN3	–		Capture B3 input pin (RGB mode)
192	PC4	–	O	General-purpose I/O port (3V pin)
	BIN4	–		Capture B4 input pin (RGB mode)
193	PC5	–	O	General-purpose I/O port (3V pin)
	BIN5	–		Capture B5 input pin (RGB mode)
194	PC6	–	O	General-purpose I/O port (3V pin)
	BIN6	–		Capture B6 input pin (RGB mode)
195	PC7	–	O	General-purpose I/O port (3V pin)
	BIN7	–		Capture B7 input pin (RGB mode)
2	PD2	–	O	General-purpose I/O port (3V pin)
	ROUT2	–		Display digital R2 output pin
3	PD3	–	O	General-purpose I/O port (3V pin)
	ROUT3	–		Display digital R3 output pin
4	PD4	–	O	General-purpose I/O port (3V pin)
	ROUT4	–		Display digital R4 output pin
5	PD5	–	O	General-purpose I/O port (3V pin)
	ROUT5	–		Display digital R5 output pin
6	PD6	–	O	General-purpose I/O port (3V pin)
	ROUT6	–		Display digital R6 output pin
7	PD7	–	O	General-purpose I/O port (3V pin)
	ROUT7	–		Display digital R7 output pin
8	PE2	–	O	General-purpose I/O port (3V pin)
	GOUT2	–		Display digital G2 output pin
9	PE3	–	O	General-purpose I/O port (3V pin)
	GOUT3	–		Display digital G3 output pin
10	PE4	–	O	General-purpose I/O port (3V pin)
	GOUT4	–		Display digital G4 output pin
11	PE5	–	O	General-purpose I/O port (3V pin)
	GOUT5	–		Display digital G5 output pin
12	PE6	–	O	General-purpose I/O port (3V pin)
	GOUT6	–		Display digital G6 output pin
13	PE7	–	O	General-purpose I/O port (3V pin)
	GOUT7	–		Display digital G7 output pin

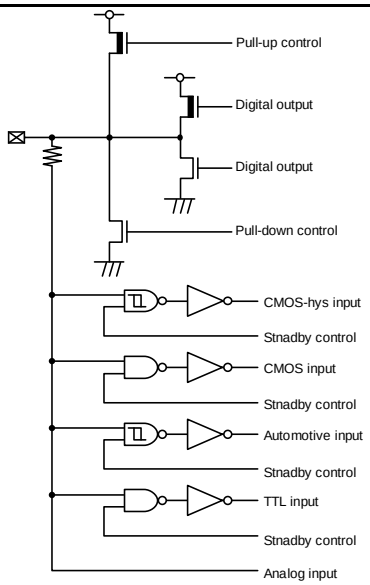
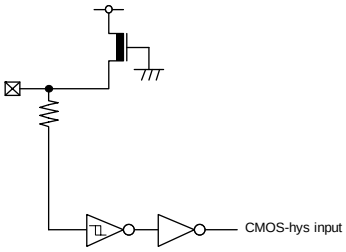
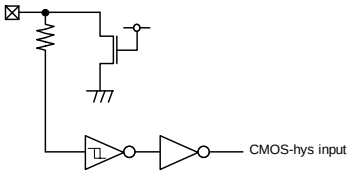
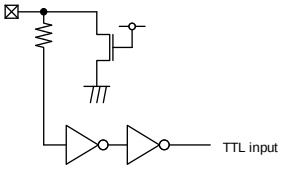
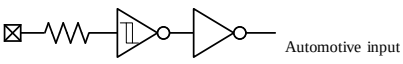
Pin no.	Pin Name	Polarity	I/O circuit types*1	Function *2
14	PF2	–	O	General-purpose I/O port (3V pin)
	BOUT2	–		Display digital B2 output pin
15	PF3	–	O	General-purpose I/O port (3V pin)
	BOUT3	–		Display digital B3 output pin
16	PF4	–	O	General-purpose I/O port (3V pin)
	BOUT4	–		Display digital B4 output pin
17	PF5	–	O	General-purpose I/O port (3V pin)
	BOUT5	–		Display digital B5 output pin
21	PF6	–	O	General-purpose I/O port (3V pin)
	BOUT6	–		Display digital B6 output pin
22	PF7	–	O	General-purpose I/O port(3V pin)
	BOUT7	–		Display digital B7 output pin
200	PG0	–	O	General-purpose I/O port (3V pin)
	DCKIN	–		Display reference clock input pin (for External sync)
	CMDTRG	–		GDC command trigger input pin
197	PG1	–	O	General-purpose I/O port (3V pin)
	VSIN	P		Capture vertical sync signal input pin
198	PG2	–	O	General-purpose I/O port (3V pin)
	HSIN	P		Capture horizontal sync signal input pin
199	PG3	–	O	General-purpose I/O port (3V pin)
	CSOUT	–		Display composite sync signal output pin, Graphics / Video switch (for External sync) output pin
23	PG4	–	O	General-purpose I/O port (3V pin)
	DCKOUT	–		Display reference clock output pin (for Internal sync)
24	PG5	–	O	General-purpose I/O port (3V pin)
	VSYNC	–		Display vertical sync signal output pin (for Internal sync)/ Display vertical sync signal input pin (for External sync)
25	PG6	–	O	General-purpose I/O port (3V pin)
	HSYNC	–		Display horizontal sync signal output pin (for Internal sync)/ Display horizontal sync signal input pin (for External sync)
26	PG7	–	O	General-purpose I/O port (3V pin)
	DEOUT	P		Display enable display period output pin
196	PH3	–	O	General-purpose I/O port (3V pin)
	CCLK	–		For capture, capture clock input pin
204	REFOUT	–	T	Clamp level output pin
203	AVR3	–	S	"L" side reference voltage for NTSC A/D converter pin

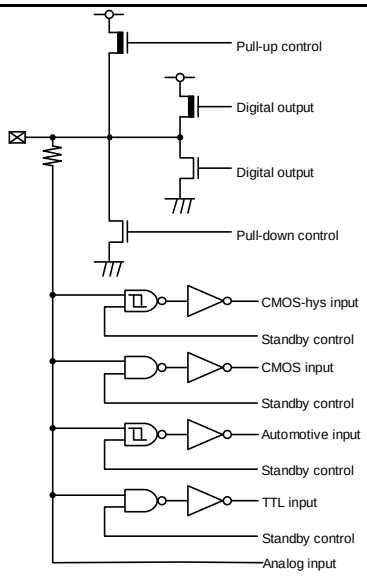
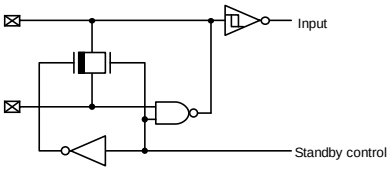
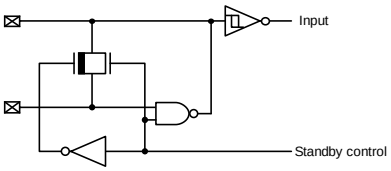
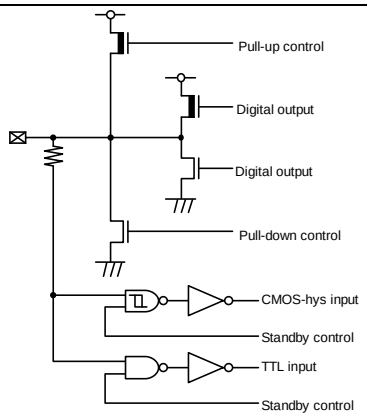
Pin no.	Pin Name	Polarity	I/O circuit types*1	Function *2
205	VIN	–	S	NTSC signal input pin
111	AVCC5	–	–	AD convertor analog power supply pin
201, 207	AVCC3	–	–	For NTSC, AD convertor analog power supply pin
112	AVRH5	–	–	AD convertor upper limit reference voltage pin
113	AVSS5/ AVRL5	–	–	AD convertor GND/ AD convertor lower limit reference voltage pin
202, 206	AVSS3	–	–	NTSC AD convertor GND pin
124	C_1	–	–	Built-in regulator capacitor connected pin 1
73	C_2	–	–	Built-in regulator capacitor connected pin 2
20	C_3	–	–	Built-in regulator capacitor connected pin 3
126, 136,146, 156	DVCC	–	–	SMC large current port power supply pin
125, 135, 145, 155	DVSS	–	–	SMC large current port GND pin
89, 105, 122, 173	VCC5	–	–	+5.0v power supply pin
1, 18, 37, 53, 71, 175, 189	VCC3	–	–	+3.3v power supply pin
19, 36, 52, 72, 82, 88, 104, 123, 174, 188, 208	VSS	–	–	GND pin

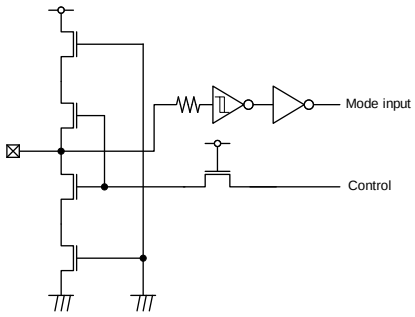
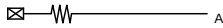
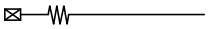
*1: For the I/O circuit types, see **"■ I/O CIRCUIT TYPE".**
*2: For switching, see **"**I/O Port**"** of HARDWARE MANUAL.

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		• General-purpose I/O port • Output 1mA,2mA • Pull-up resistor control 50kΩ • Pull-down resistor control 50kΩ • CMOS input • Schmitt input • TTL input • Automotive input
C		• Analog I/O, General-purpose I/O port • Output 1mA,2mA • Pull-up resistor control 50kΩ • Pull-down resistor control 50kΩ • CMOS input • Schmitt input • TTL input • Automotive input

Type	Circuit	Remarks
E		• Analog input, General-purpose I/O port • Output 1mA,2mA,30mA (large current for SMC) • Pull-up resistor control 50kΩ • Pull-down resistor control 50kΩ • CMOS input • Schmitt input • TTL input • Automotive input
F1		• Schmitt input • Pull-up resistor control 50kΩ (5V cont)
F2		• Schmitt input • Pull-down resistor control 50kΩ (5V cont)
G		• Open-drain I/O • Output 25mA (NOD) • TTL input
J		Automotive input

Type	Circuit	Remarks
K		• Analog input, General-purpose I/O port • Output 1mA,2mA,3mA(I^2C) • Pull-up resistor control 50kΩ • Pull-down resistor control 50kΩ • CMOS input • Schmitt input • TTL input • Automotive input
L		Main oscillation I/O
N		Sub oscillation I/O
O		• Analog input, 3.3V General-purpose I/O port • Output 2mA,5mA,10mA and 20mA • Pull-up resistor control 33kΩ • Pull-down resistor control 33kΩ • Schmitt input • TTL input

Type	Circuit	Remarks
P		• Mode I/O • Schmitt input
S		Analog input(3V)
T		Analog output(3V)

■ HANDLING PRECAUTIONS

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your FUJITSU SEMICONDUCTOR semiconductor devices.

1. Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

• Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

• Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

• Processing and Protection of Pins

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

(1) Preventing Over-Voltage and Over-Current Conditions

Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.

(2) Protection of Output Pins

Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device.

Therefore, avoid this type of connection.

(3) Handling of Unused Input Pins

Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

- **Latch-up**

  Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNPN junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

  CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

  (1) Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.

  (2) Be sure that abnormal current flows do not occur during the power-on sequence.

- **Observance of Safety Regulations and Standards**

  Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

- **Fail-Safe Design**

  Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

- **Precautions Related to Usage of Devices**

  FUJITSU SEMICONDUCTOR semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

  CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

2. Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under FUJITSU SEMICONDUCTOR's recommended conditions. For detailed information about mount conditions, contact your sales representative.

• Lead Insertion Type

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to FUJITSU SEMICONDUCTOR recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

• Surface Mount Type

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. FUJITSU SEMICONDUCTOR recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with FUJITSU SEMICONDUCTOR ranking of recommended conditions.

• Lead-Free Packaging

CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

• Storage of Semiconductor Devices

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

(1) Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.

(2) Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5°C and 30°C.

When you open Dry Package that recommends humidity 40% to 70% relative humidity.

(3) When necessary, FUJITSU SEMICONDUCTOR packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.

(4) Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

- **Baking**

  Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the FUJITSU SEMICONDUCTOR recommended conditions for baking.

  Condition: 125°C/24 h

- **Static Electricity**

  Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

  (1) Maintain relative humidity in the working environment between 40% and 70%.

  Use of an apparatus for ion generation may be needed to remove electricity.

  (2) Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.

  (3) Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ).

  Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.

  (4) Ground all fixtures and instruments, or protect with anti-static measures.

  (5) Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

3. Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

(1) Humidity

Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.

(2) Discharge of Static Electricity

When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.

(3) Corrosive Gases, Dust, or Oil

Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.

(4) Radiation, Including Cosmic Radiation

Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.

(5) Smoke, Flame

CAUTION: Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of FUJITSU SEMICONDUCTOR products in other special environmental conditions should consult with sales representatives.

Please check the latest handling precautions at the following URL.

http://edevice.fujitsu.com/fj/handling-e.pdf

■ HANDLING DEVICES

This section explains the latch-up prevention and treatment of a pin.

• For latch-up prevention

If a voltage higher than VCC or a voltage lower than VSS is applied to an I/O pin, or if a voltage exceeding the ratings is applied between VCC pin and VSS pin, a latch-up may occur in CMOS IC. If the latch-up occurs, the power supply current increases excessively and device elements may be damaged by heat. Take care to prevent any voltage from exceeding the maximum ratings in device application.

Also, the analog power supply (AVCC5, AVRH5), the NTSC power supply (AVCC3, AVR3), analog input and power supply to high-current output buffer pins must not be exceed the digital power supply (VCC5 or VCC3) when the power supply to the analog system and high-current output buffer pins is turned on or off.

In the correct power-on sequence of the microcontroller, turn on the digital power supply (VCC5), analog power supplies (AVCC5, AVRH5), and the power supply of high-current output buffer pins (DVCC) simultaneously. Or, turn on the digital power supply (VCC5), and then turn on analog power supplies (AVCC5, AVRH5) and the power supply of high-current output buffer pins (DVCC).

In the correct power-on sequence of GDC, similarly turn on the digital power supply (VCC3) and the NTSC analog power supply (AVCC3) simultaneously. Or, turn on the digital power supply (VCC3), and then turn on the NTSC analog power supply (AVCC3).

• Treatment of unused pins

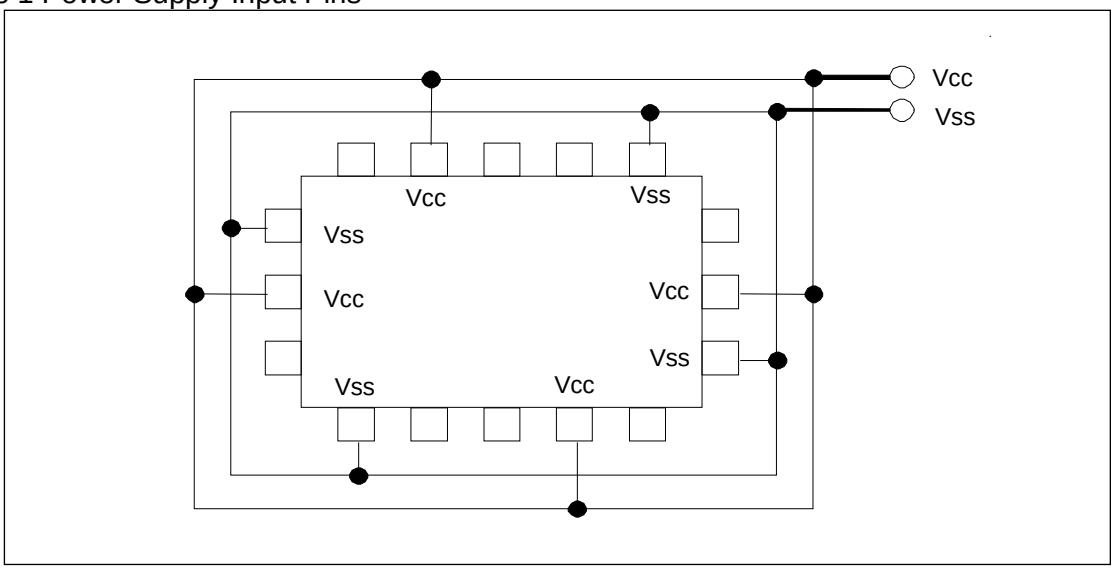
If unused input pins are left open, they may cause a permanent damage to the device due to malfunction or latch-up. Connect a 2kΩ resistor to each of unused pins for pull-up or pull-down processing.

Also, if I/O pins are not used, they must be set to the output state for opening or they must be set to the input state and treated in the same way as for the input pins.

- **Power supply pins**

  The device is designed to ensure that if the device contains multiple VCC pin or VSS pin, the pins that should be at the same potential are interconnected to prevent latch-up or other malfunctions. Further, connect these pins to an external power supply or ground to reduce unwanted radiation, prevent strobe signals from malfunctioning due to a raised ground level, and fulfill the total output current standard, etc. As shown in figure 1, all Vss power supply pins must be treated in the similar way. If multiple Vcc or Vss systems are connected, the device cannot operate correctly even within the guaranteed operating range.

Figure 1 Power Supply Input Pins



The power supply pins should be connected to VCC pin and VSS pin of this device at the low impedance from the power supply source.

In the area close to this device, a ceramic capacitor having the capacitance larger than the capacitor of C pin is recommended to use as a bypass capacitor between theVCC pin and the VSS pin.

- **Crystal oscillation circuit**

  An external noise to the X0 pin or X1 pin may cause a device malfunction. The printed circuit board must be designed to lay out the X0 pin and the X1 pin, crystal oscillator (or ceramic resonator), and the bypass capacitor to be grounded to the close position to the device.

  The printed circuit board artwork is recommended to surround the X0 pin and X1 pin by ground circuits.

- **Mode pins (MD2, MD1, MD0)**

  Connect the MD2, MD1and MD0 mode pin to the VCC pin or VSS pin directly. To prevent an erroneous selection of test mode caused by the noise, reduce the pattern length between each mode pin and the VCC pin or VSS pin on the printed circuit board. Also, use the low-impedance pin connection.

- **During power-on**

  To prevent a malfunction of the voltage step-down circuit built in the device, set the voltage rising time to have 50µs or longer (between 0.2V and 2.7V) during power-on.

- **Notes during PLL clock operation**

  When the PLL clock is selected and if the oscillator is disconnected or if the input is stopped, this clock may continue to operate at the free running frequency of the self oscillator circuit built in the PLL clock. This operation is not guaranteed.

- **Treatment of A/D converter power supply pins**

  Connect the pins to have AVCC5=AVRH5=VCC5 and AVSS5/AVRL5=VSS even if the A/D converter is not used.

  Also, similarly connect the pins of NTSC A/D converter power supply to have AVCC3=VCC3 and AVSS3=VSS. At this time, open VIN/REFOUT.

- **Notes on using external clock**

  An external clock is not supported. None of the external direct clock input can be used for both main clock and sub clock.

- **Power-on sequence of A/D converter analog inputs**

  Be sure to turn on the digital power supply (Vcc5) first, and then turn on the A/D converter power supplies (AVcc5, AVRH5, AVRL5) and analog inputs (AN0 to AN31). Also, turn off the A/D converter power supplies and analog inputs first, and then turn off the digital power supply (Vcc5). When the AVRH5 pin voltage is turned on or off, it must not exceed AVCC5. Even if a common analog input pin is used as an input port, its input voltage must not exceed AVcc5. (However, the analog power supply and digital power supply can be turned on or off simultaneously.)

  Be sure to similarly turn on the digital power supply (VCC3) first, and then turn on the A/D converter power supply (AVCC3) for NTSC and NTSC inputs (VIN, AVR). Also, turn off the A/D converter power supplies and analog inputs first, and then turn off the digital power supply (VCC3).

- **Treatment of power supplies for high current output buffer pins (DVcc, DVss)**

  Be sure to turn on the digital power supply (Vcc) first, and then turn on the power supplies for high current output buffer pins (DVcc, DVss). Also, turn off the power supplies for high current output buffer pins first, and then turn off the digital power supply (Vcc).

  Even if the high current output buffer pins are used as general-purpose ports, the power supplies of high current output buffer pins (DVcc, DVss) must be powered. (The power supplies of high current output buffer pins and the digital power supplies can be turned on or off simultaneously.)

- **Treatment of C pin**

  This device contains a voltage step-down circuit. A capacitor must always be connected to the C pin to assure the internal stabilization of the device. For the standard values, see the "Recommended Operating Conditions" of the latest data sheet.

- **Function switching of a multiplexed port**

  To switch between the port function and the multiplexed pin function, use the PFR (port function register).

- **Low-power consumption mode**

  To transit to the sleep mode, watch mode, stop mode, watch mode(power-off) or stop mode(power-off), follow the procedure explained in the "Activating the sleep mode, watch mode, or stop mode" or the "Activating the watch mode (power-off) or stop mode(power-off)" of " POWER CONSUMPTION CONTROL".

  Power supply for GDC can be turned off separately from the microcontroller.

  Take the following notes when using a monitor debugger.

  · Do not set a break point for the low-power consumption transition program.
  · Do not execute an operation step for the low-power consumption transition program.

- **Precautions when writing to registers including the status flag**

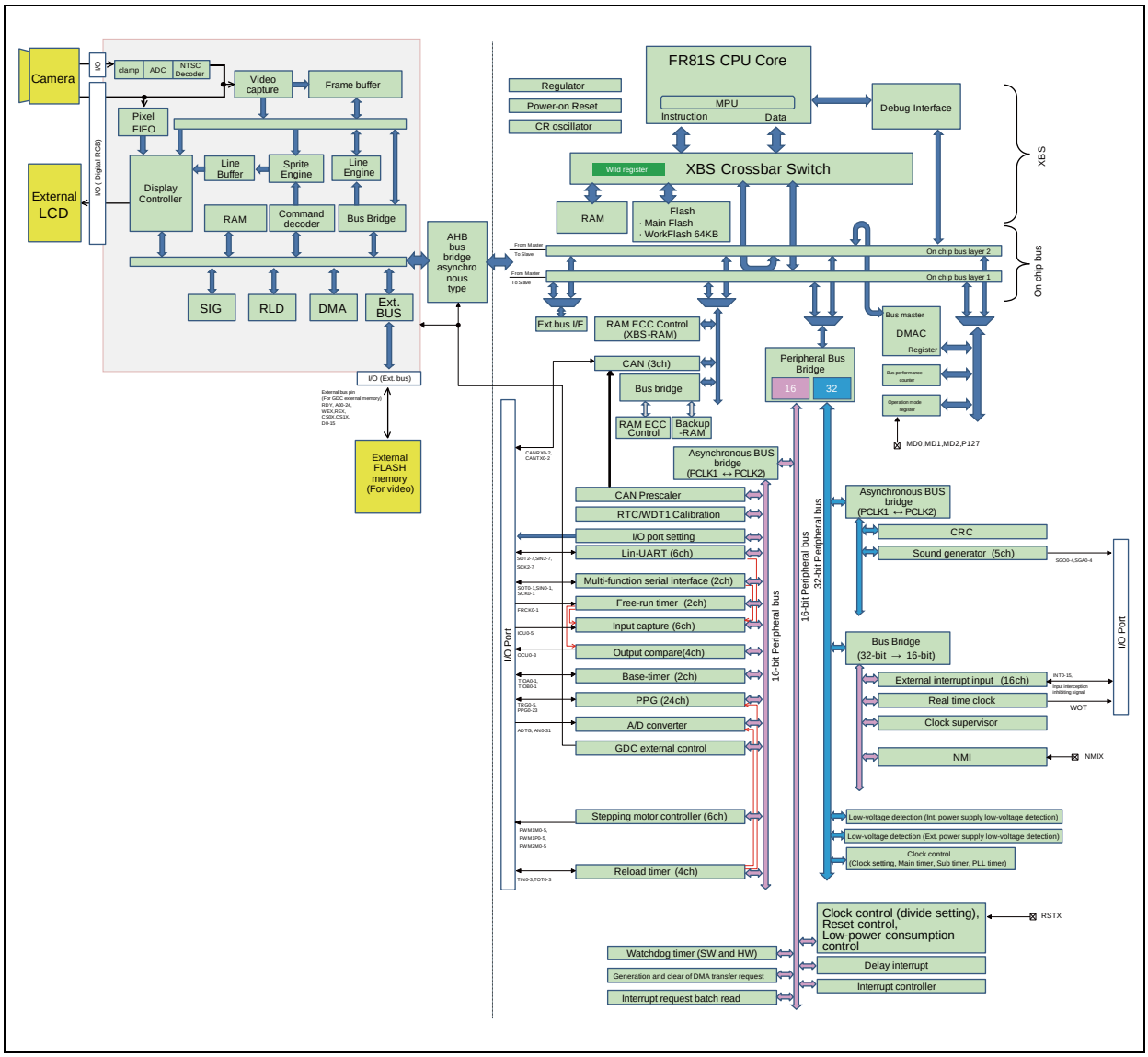
  When writing data in the register that has a status flag (especially, an interrupt request flag) to control function, taking care not to clear its status flag erroneously must be followed.

  The program must be written not to clear the flag to the status bit, and then to set the control bits to have the desired value.

  Especially, if multiple control bits are used, the bit instruction cannot be used. (The bit instruction can access to a single bit only.) By the Byte, Half-word, or Word access, data is written to the control bits and status flag simultaneously. During this time, take care not to clear other bits (in this case, the bits of status flag) erroneously.

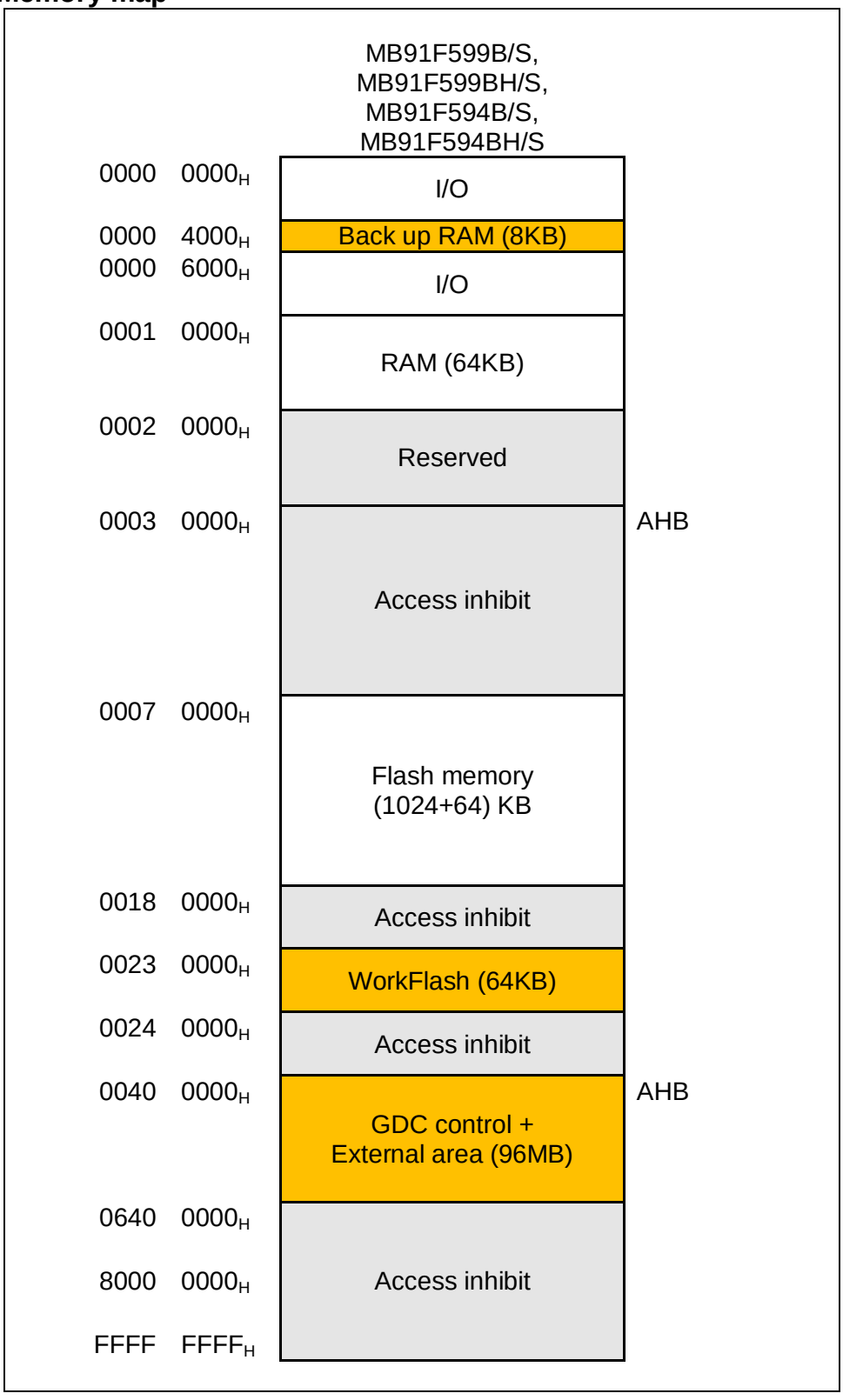
  Note: These points can be ignored because the bit instructions to a register which supports RMW are already taken the points into consideration. Care must be taken when the bit instruction is used to a register which does not support RMW.

■ BLOCK DIAGRAM

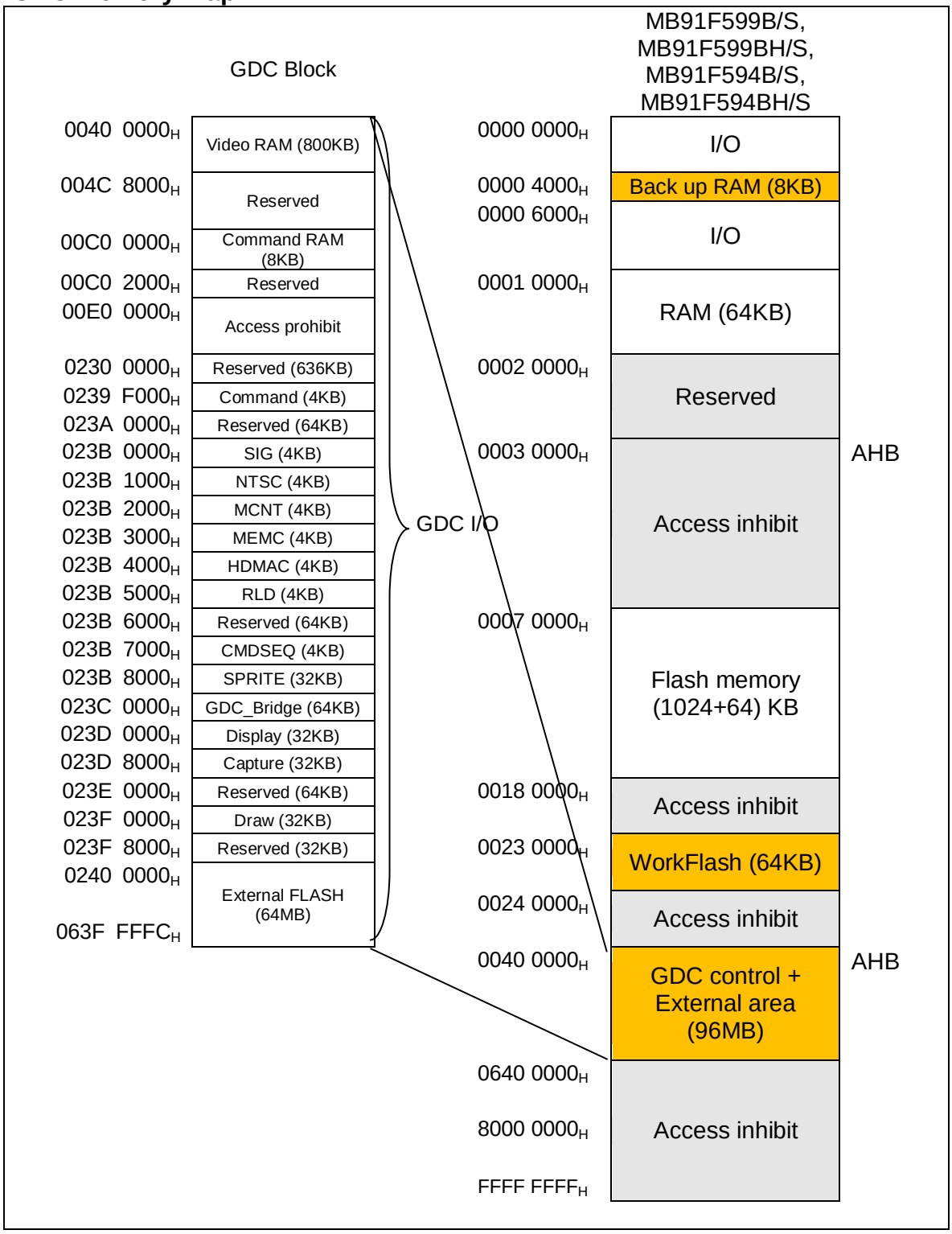


■ MEMORY MAP

● Memory map

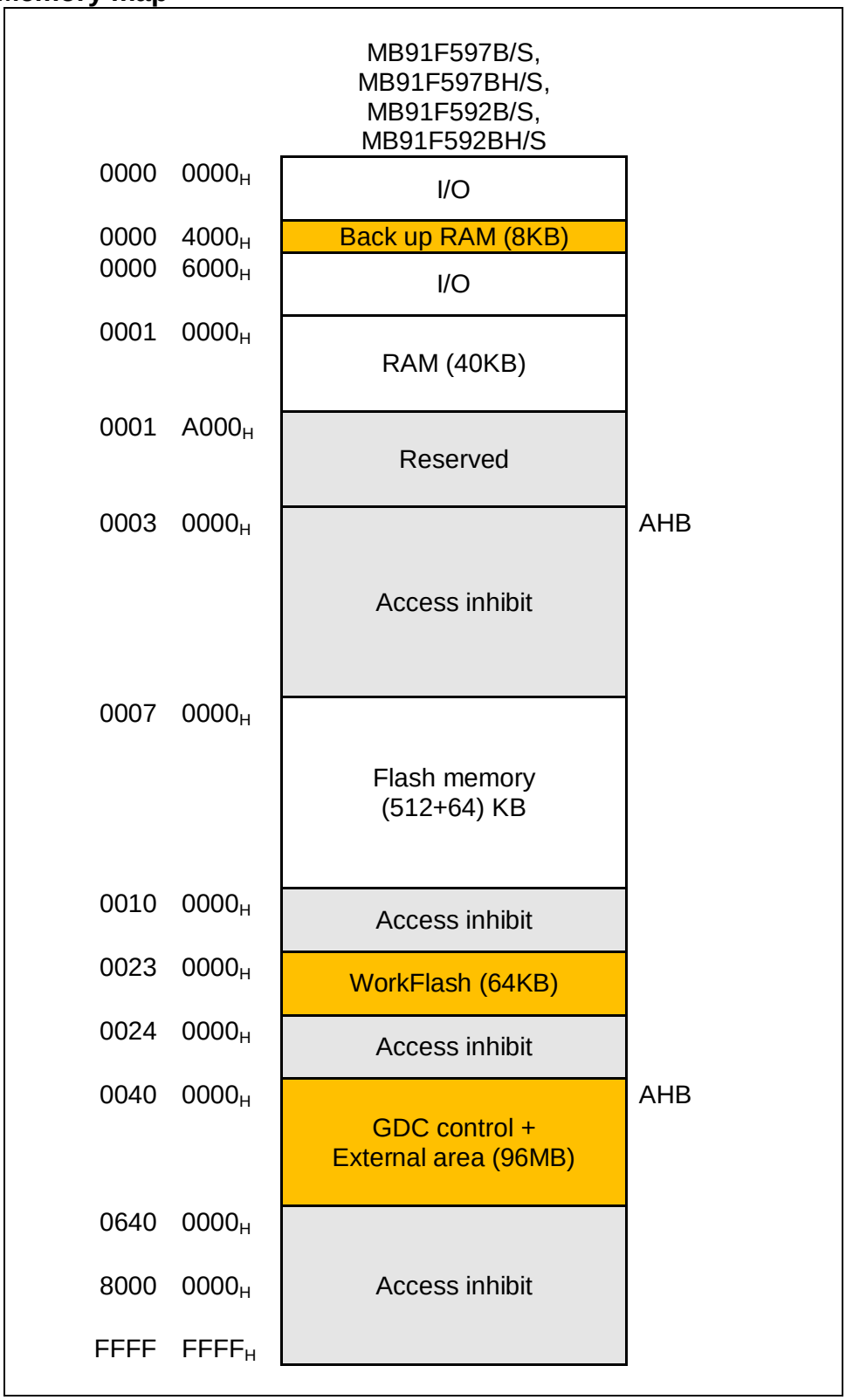


● GDC memory map

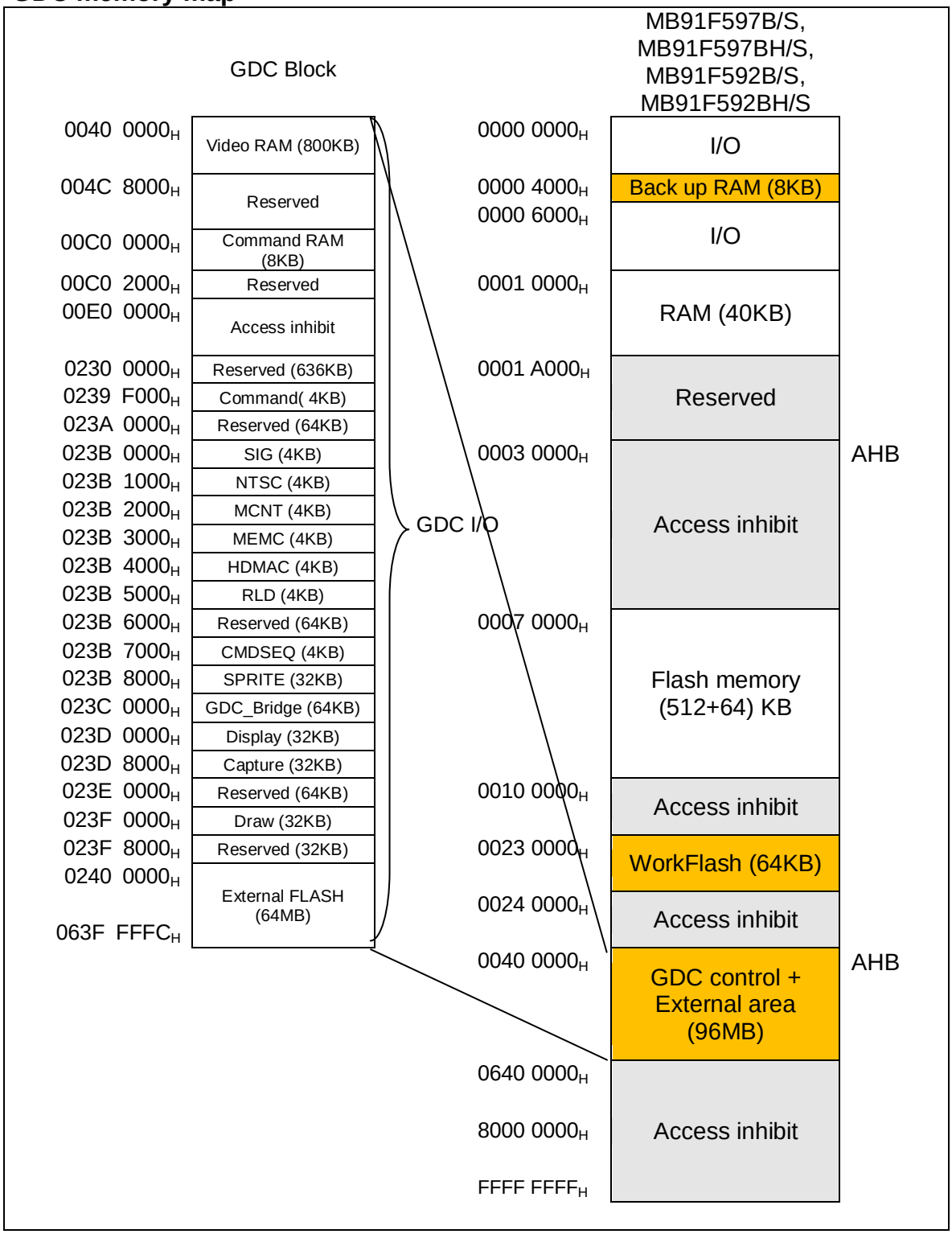


Note: The GDC area is executed mapping with the little endian.

- **Memory map**

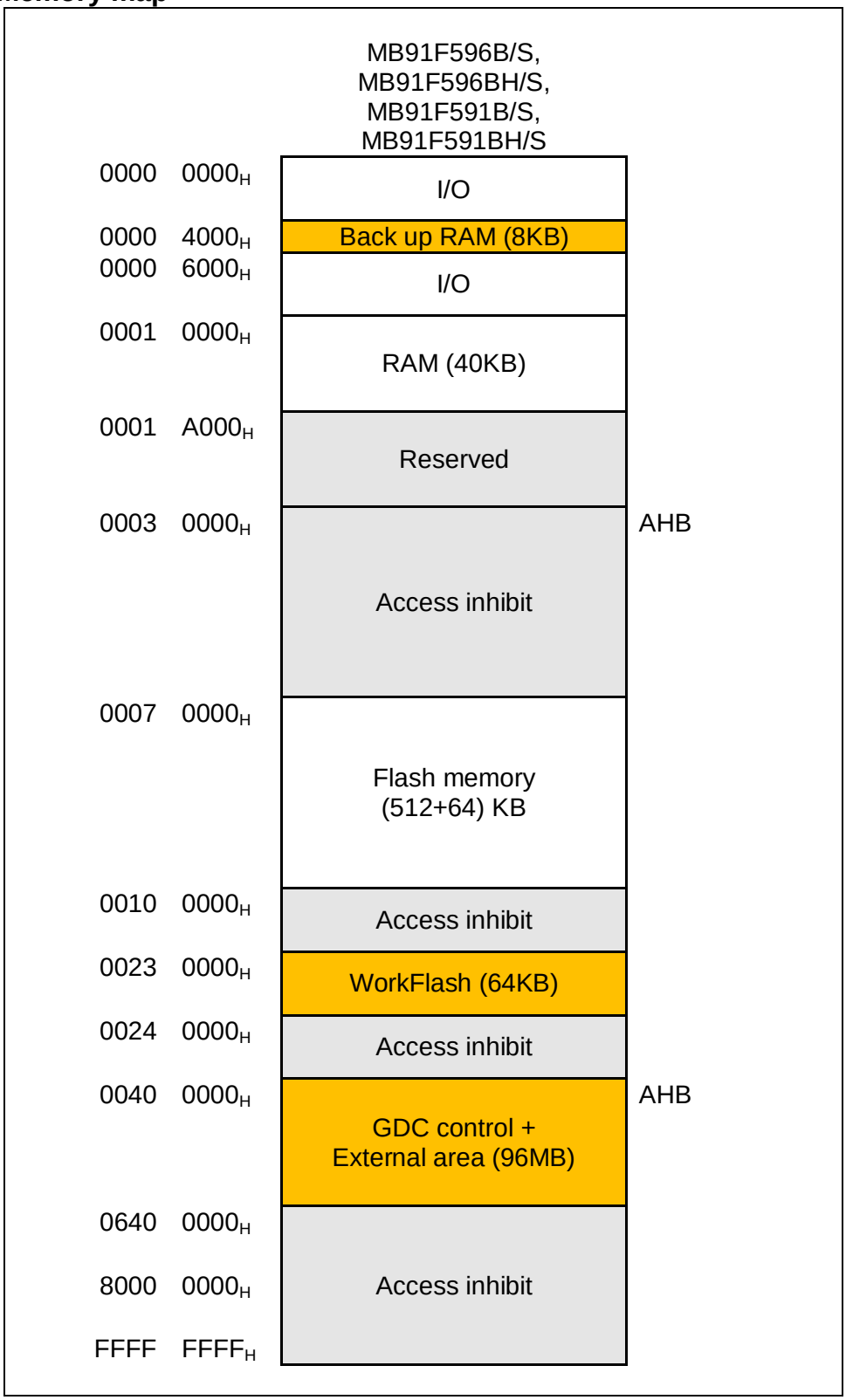

MB91F597B/S,
MB91F597BH/S,
MB91F592B/S,
MB91F592BH/S
0000 0000H
I/O
0000 4000H
Back up RAM (8KB)
0000 6000H
I/O
0001 0000H
RAM (40KB)
0001 A000H
Reserved
0003 0000H
Access inhibit
AHB
0007 0000H
Flash memory
(512+64) KB
0010 0000H
Access inhibit
0023 0000H
WorkFlash (64KB)
0024 0000H
Access inhibit
0040 0000H
GDC control +
External area (96MB)
AHB
0640 0000H
8000 0000H
Access inhibit
FFFF FFFFH

● GDC memory map

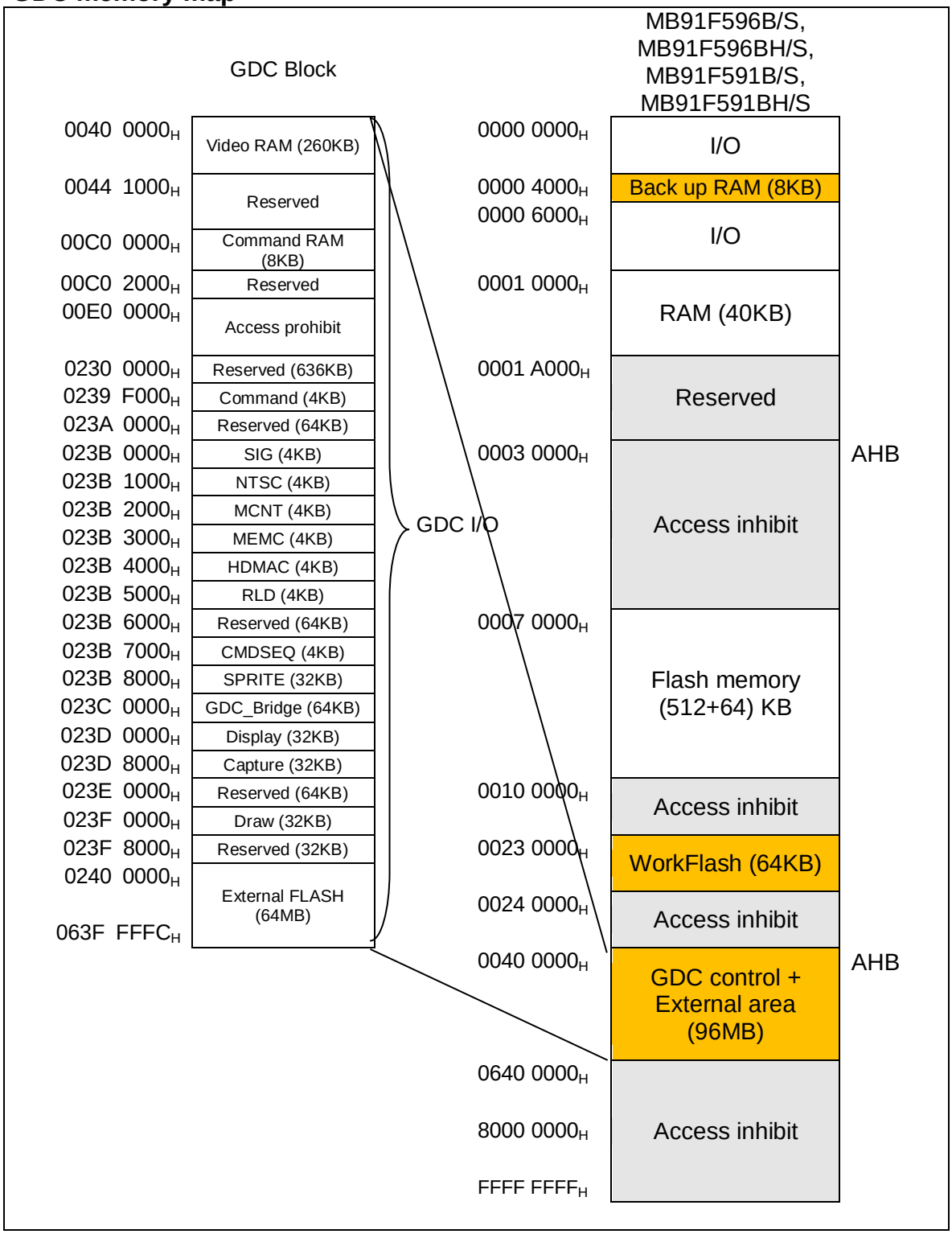


Note: The GDC area is executed mapping with the little endian.

- **Memory map**


MB91F596B/S,
MB91F596BH/S,
MB91F591B/S,
MB91F591BH/S
0000 0000H
I/O
0000 4000H
Back up RAM (8KB)
0000 6000H
I/O
0001 0000H
RAM (40KB)
0001 A000H
Reserved
0003 0000H
Access inhibit
AHB
0007 0000H
Flash memory
(512+64) KB
0010 0000H
Access inhibit
0023 0000H
WorkFlash (64KB)
0024 0000H
Access inhibit
0040 0000H
GDC control +
External area (96MB)
AHB
0640 0000H
8000 0000H
Access inhibit
FFFF FFFFH

● GDC memory map

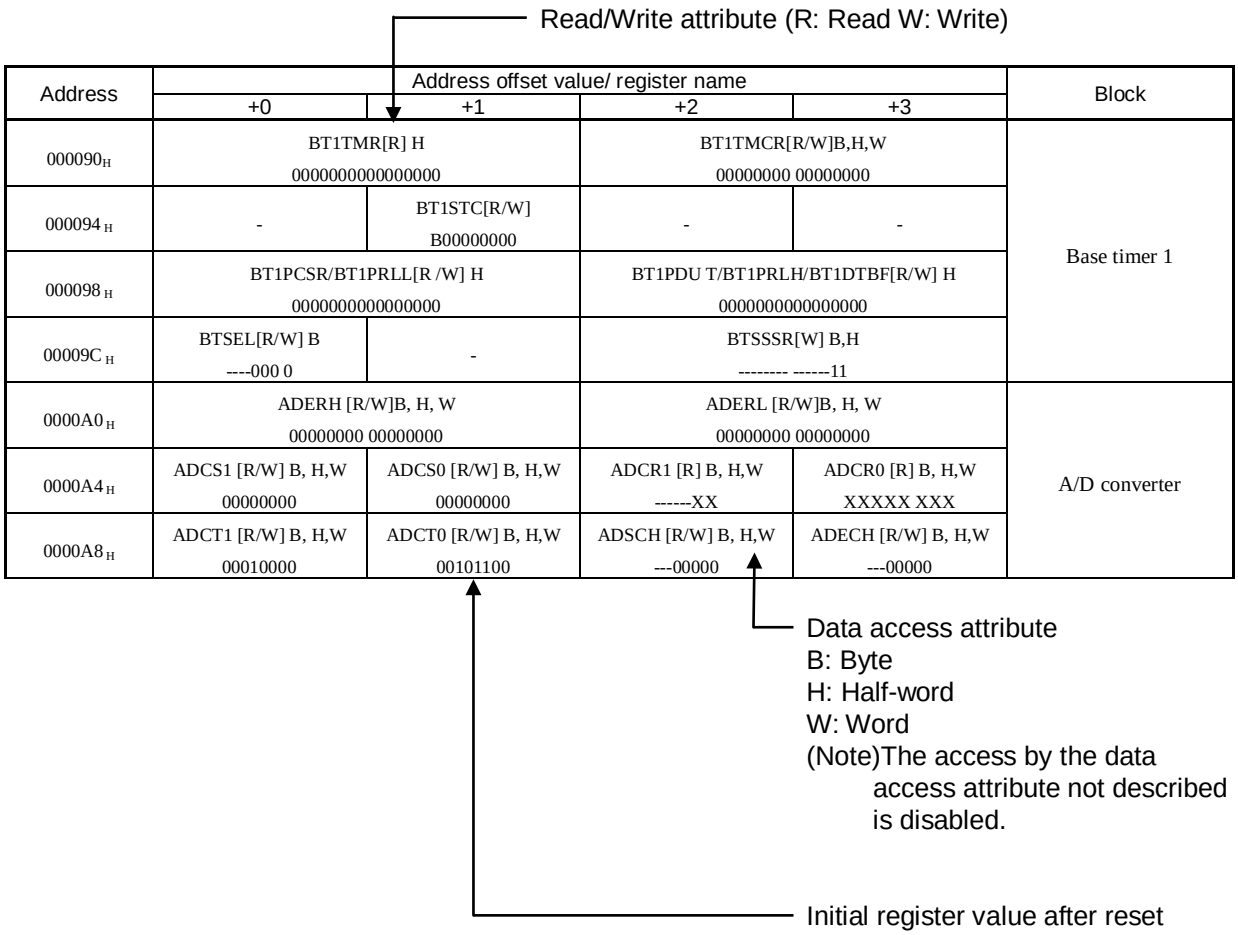


Note: The GDC area is executed mapping with the little endian.

■ I/O MAP

The following I/O map shows the relationship between memory space and registers for peripheral resources.

• Legend of I/O Map



Address	Address offset value/ register name				Block
	+0	+1	+2	+3	
000090_H	BT1TMR[R] H 0000000000000000		BT1TMCR[R/W]B,H,W 00000000 00000000		Base timer 1
000094_H	-	BT1STC[R/W] B00000000	-	-	
000098_H	BT1PCSR/BT1PRLL[R /W] H 0000000000000000		BT1PDU T/BT1PRLH/BT1DTBF[R/W] H 0000000000000000		
$00009C_H$	BTSEL[R/W] B ----000 0	-	BTSSSR[W] B,H -------- ------11		
$0000A0_H$	ADERH [R/W]B, H, W 00000000 00000000		ADERL [R/W]B, H, W 00000000 00000000		A/D converter
$0000A4_H$	ADCS1 [R/W] B, H,W 00000000	ADCS0 [R/W] B, H,W 00000000	ADCR1 [R] B, H,W ------XX	ADCR0 [R] B, H,W XXXXX XXX	
$0000A8_H$	ADCT1 [R/W] B, H,W 00010000	ADCT0 [R/W] B, H,W 00101100	ADSCH [R/W] B, H,W ---00000	ADECH [R/W] B, H,W ---00000	

The initial register value after reset indicates as follows:

- "1": Initial value "1"
- "0": Initial value "0"
- "X": Initial value undefined
- "-": Reserved bit/Undefined bit
- "*": Initial value "0" or "1" according to the setting

Note: The access by the data access attribute not described is disabled.

• I/O Map

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000000_H	PDR00[R/W] B,H,W XXXXXXXX	PDR01[R/W] B,H,W XXXXXXXX	PDR02[R/W] B,H,W XXXXXXXX	PDR03[R/W] B,H,W XXXXXXXX	Port data register
000004_H	PDR04[R/W] B,H,W XXXXXXXX	PDR05[R/W] B,H,W XXXXXXXX	PDR06[R/W] B,H,W XXXXXXXX	PDR07[R/W] B,H,W XXXXXXXX	
000008_H	PDR08[R/W] B,H,W XXXXXXXX	PDR09[R/W] B,H,W XXXXXXXX	PDR10[R/W] B,H,W XXXXXXXX	PDR11[R/W] B,H,W XXXXXXXX	
$00000C_H$	PDR12[R/W] B,H,W XXXXXXXX	PDR13[R/W] B,H,W XX-XXXXX	—	—	
000010_H	PDRA[R/W] B,H,W XXXXXX--	PDRB[R/W] B,H,W XXXXXX--	PDRC[R/W] B,H,W XXXXXX--	PDRD[R/W] B,H,W XXXXXX--	
000014_H	PDRE[R/W] B,H,W XXXXXX--	PDRF[R/W] B,H,W XXXXXX--	PDRG[R/W] B,H,W XXXXXXXX	PDRH[R/W] B,H,W ----X---	
000018_H to 000028_H	—	—	—	—	Reserved
$00002C_H$ to 000030_H	—	—	—	—	Reserved
000034_H to 000038_H	—	—	—	—	Reserved
$00003C_H$	WDTCR0[R/W] B,H,W -0--0000	WDTCPR0[W] B,H,W 00000000	WDTCR1[R] B,H,W ----0110	WDTCPR1[W] B,H,W 00000000	Watchdog timer [S]
000040_H	—	—	—	—	Reserved
000044_H	DICR [R/W] B XXXXXXX0	—	—	—	Delay interrupt
000048_H to $00005C_H$	—	—	—	—	Reserved
000060_H	TMRLRA0 [R/W] H XXXXXXXX XXXXXXXX		TMR0 [R] H XXXXXXXX XXXXXXXX		Reload timer 0
000064_H	TMRLRB0 [R/W] H XXXXXXXX XXXXXXXX		TMCSR0 [R/W] B, H,W 00000000 0-000000		
000068_H to $00007C_H$	—	—	—	—	Reserved

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000080_H	BT0TMR [R] H 0000000000000000		BT0TMCR [R/W] H -0000000 00000000		Base timer 0
000084_H	—	BT0STC [R/W] B 0000-000	—	—	
000088_H	BT0PCSR/BT0PRLL [R/W] H 0000000000000000		BT0PDUT/BT0PRLH/BT0DTBF [R/W] H 0000000000000000		
$00008C_H$	—	—	—	—	
000090_H	BT1TMR [R] H 0000000000000000		BT1TMCR [R/W] H -0000000 00000000		Base timer 1
000094_H	—	BT1STC [R/W] B 0000-000	—	—	
000098_H	BT1PCSR/BT1PRLL [R/W] H 0000000000000000		BT1PDUT/BT1PRLH/BT1DTBF [R/W] H 0000000000000000		
$00009C_H$	BTSEL01 [R/W] B ----0000	—	BTSSSR [W] B,H -------- ------11		Base timer 0,1
$0000A0_H$	ADERH [R/W] B, H, W 00000000 00000000		ADERL [R/W] B, H, W 00000000 00000000		A/D converter
$0000A4_H$	ADCS1 [R/W] B, H,W 0000000-	ADCS0 [R/W] B, H,W 00000000	ADCR1 [R] B, H,W ------XX	ADCR0 [R] B, H,W XXXXXXXX	
$0000A8_H$	ADCT1 [R/W] B, H,W 00010000	ADCT0 [R/W] B, H,W 00101100	ADSCH [R/W] B, H,W ---00000	ADECH [R/W] B, H,W ---00000	
$0000AC_H$	—	—	—	—	Reserved
$0000B0_H$	SCR0/(IBCR0) [R/W] B,H,W 0--00000	SMR0 [R/W] B,H,W 000-0000	SSR0 [R/W] B,H,W 0-000011	ESCR0/(IBSR0) [R/W] B,H,W -0000000	Multi-UART0 *1 : Byte access is possible only for access to lower 8 bits *2 : Reserved because I^2C mode is not set immediately after reset.
$0000B4_H$	RDR0/(TDR0)[R/W] B,H,W *1 -------0 00000000		BGR0 [R/W] H,W 00000000 00000000		
$0000B8_H$	— / (ISMK0) [R/W] B,H,W -------- *2	— / (ISBA0) [R/W] B,H,W -------- *2	—	—	
$0000BC_H$	FCR10 [R/W] B,H,W ---00100	FCR00 [R/W] B,H,W -0000000	FBYTE20 [R/W] B,H,W 00000000	FBYTE10 [R/W] B,H,W 00000000	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$0000C0_H$	SCR1/(IBCR1) [R/W] B,H,W 0--00000	SMR1 [R/W] B,H,W 000-0000	SSR1 [R/W] B,H,W 0-000011	ESCR1/(IBSR1) [R/W] B,H,W -0000000	Multi-UART1 *1 : Byte access is possible only for access to lower 8 bits *2 : Reserved because I^2C mode is not set immediately after reset.
$0000C4_H$	RDR1/(TDR1)[R/W] B,H,W *1 -------0 00000000		BGR1 [R/W] H,W 00000000 00000000		
$0000C8_H$	— / (ISMK1) [R/W] B,H,W -------- *2	— /(ISBA1) [R/W] B,H,W -------- *2	—	—	
$0000CC_H$	FCR11 [R/W] B, H, W ---00100	FCR01[R/W] B, H, W -0000000	FBYTE21 [R/W] B,H,W 00000000	FBYTE11[R/W] B,H,W 00000000	
$0000D0_H$	SCR2 [R/W] B, H, W 00000000	SMR2 [R/W] B, H, W 00000000	SSR2 [R/W] B, H, W 00001000	RDR2 /TDR2 [R/W] B, H, W 00000000	LIN-UART2
$0000D4_H$	ESCR2 [R/W] B, H, W 00000X00	ECCR2 [R/W] B, H, W -0000-XX	BGR2 [R/W] B, H, W -0000000 00000000		
$0000D8_H$	SCR3 [R/W] B, H, W 00000000	SMR3 [R/W] B, H, W 00000000	SSR3 [R/W] B, H, W 00001000	RDR3 /TDR3 [R/W] B, H, W 00000000	LIN-UART3
$0000DC_H$	ESCR3 [R/W] B, H, W 00000X00	ECCR3 [R/W] B, H, W -0000-XX	BGR3 [R/W] B, H, W -0000000 00000000		
$0000E0_H$	SCR4 [R/W] B, H, W 00000000	SMR4 [R/W] B, H, W 00000000	SSR4 [R/W] B, H, W 00001000	RDR4 /TDR4 [R/W] B, H, W 00000000	LIN-UART4
$0000E4_H$	ESCR4 [R/W] B, H, W 00000X00	ECCR4 [R/W] B, H, W -0000-XX	BGR4 [R/W] B, H, W -0000000 00000000		
$0000E8_H$	SCR5 [R/W] B, H, W 00000000	SMR5 [R/W] B, H, W 00000000	SSR5 [R/W] B, H, W 00001000	RDR5 /TDR5 [R/W] B, H, W 00000000	LIN-UART5
$0000EC_H$	ESCR5 [R/W] B, H, W 00000X00	ECCR5 [R/W] B, H, W -0000-XX	BGR5 [R/W] B, H, W -0000000 00000000		
$0000F0_H$	SCR6 [R/W] B, H, W 00000000	SMR6 [R/W] B, H, W 00000000	SSR6 [R/W] B, H, W 00001000	RDR6 /TDR6 [R/W] B, H, W 00000000	LIN-UART6
$0000F4_H$	ESCR6 [R/W] B, H, W 00000X00	ECCR6 [R/W] B, H, W -0000-XX	BGR6 [R/W] B, H, W -0000000 00000000		
$0000F8_H$	SCR7 [R/W] B, H, W 00000000	SMR7 [R/W] B, H, W 00000000	SSR7 [R/W] B, H, W 00001000	RDR7 /TDR7 [R/W] B, H, W 00000000	LIN-UART7
$0000FC_H$	ESCR7 [R/W] B, H, W 00000X00	ECCR7 [R/W] B, H, W -0000-XX	BGR7 [R/W] B, H, W -0000000 00000000		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000100_H	TMRLRA1 [R/W] H XXXXXXXX XXXXXXXX		TMR1 [R] H XXXXXXXX XXXXXXXX		Reload timer 1
000104_H	TMRLRB1 [R/W] H XXXXXXXX XXXXXXXX		TMCSR1 [R/W] B, H,W 00000000 0-000000		
000108_H	TMRLRA2 [R/W] H XXXXXXXX XXXXXXXX		TMR2 [R] H XXXXXXXX XXXXXXXX		Reload timer 2
$00010C_H$	TMRLRB2 [R/W] H XXXXXXXX XXXXXXXX		TMCSR2 [R/W] B, H,W 00000000 0-000000		
000110_H	TMRLRA3 [R/W] H XXXXXXXX XXXXXXXX		TMR3 [R] H XXXXXXXX XXXXXXXX		Reload timer 3
000114_H	TMRLRB3 [R/W] H XXXXXXXX XXXXXXXX		TMCSR3 [R/W] B, H,W 00000000 0-000000		
000118_H to 000140_H	—	—	—	—	Reserved
000144_H	GCN13 [R/W] H 00110010 00010000		—	GCN23 [R/W] B ----0000	PPG12,13,14,15 control
000148_H	GCN14 [R/W] H 00110010 00010000		—	GCN24 [R/W] B ----0000	PPG16,17,18,19 control
$00014C_H$	GCN15 [R/W] H 00110010 00010000		—	GCN25 [R/W] B ----0000	PPG20,21,22,23 control
000150_H	PTMR11 [R] H,W 11111111 11111111		PCSR11 [W] H, W XXXXXXXX XXXXXXXX		PPG11
000154_H	PDUT11 [W] H,W XXXXXXXX XXXXXXXX		PCN11 [R/W] B, H,W 0000000- 000000-0		
000158_H	PTMR12 [R] H,W 11111111 11111111		PCSR12 [W] H,W XXXXXXXX XXXXXXXX		PPG12
$00015C_H$	PDUT12 [W] H,W XXXXXXXX XXXXXXXX		PCN12 [R/W] B, H,W 0000000- 000000-0		
000160_H	PTMR13 [R] H,W 11111111 11111111		PCSR13 [W] H,W XXXXXXXX XXXXXXXX		PPG13
000164_H	PDUT13 [W] H,W XXXXXXXX XXXXXXXX		PCN13 [R/W] B, H,W 0000000- 000000-0		
000168_H	PTMR14 [R] H,W 11111111 11111111		PCSR14 [W] H,W XXXXXXXX XXXXXXXX		PPG14
$00016C_H$	PDUT14 [W] H,W XXXXXXXX XXXXXXXX		PCN14 [R/W] B, H,W 0000000- 000000-0		
000170_H	PTMR15 [R] H,W 11111111 11111111		PCSR15 [W] H,W XXXXXXXX XXXXXXXX		PPG15
000174_H	PDUT15 [W] H,W XXXXXXXX XXXXXXXX		PCN15 [R/W] B, H,W 0000000- 000000-0		
000178_H	PTMR16 [R] H,W 11111111 11111111		PCSR16 [W] H, W XXXXXXXX XXXXXXXX		PPG16
$00017C_H$	PDUT16 [W] H,W XXXXXXXX XXXXXXXX		PCN16 [R/W] B, H,W 0000000- 000000-0		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000180_H	PTMR17 [R] H,W 11111111 11111111		PCSR17 [W] H,W XXXXXXXX XXXXXXXX		PPG17
000184_H	PDUT17 [W] H,W XXXXXXXX XXXXXXXX		PCN17 [R/W] B, H,W 0000000- 000000-0		
000188_H	PTMR18 [R] H,W 11111111 11111111		PCSR18 [W] H,W XXXXXXXX XXXXXXXX		PPG18
$00018C_H$	PDUT18 [W] H,W XXXXXXXX XXXXXXXX		PCN18 [R/W] B, H,W 0000000- 000000-0		
000190_H	PTMR19 [R] H,W 11111111 11111111		PCSR19 [W] H,W XXXXXXXX XXXXXXXX		PPG19
000194_H	PDUT19 [W] H,W XXXXXXXX XXXXXXXX		PCN19 [R/W] B, H,W 0000000- 000000-0		
000198_H	PTMR20 [R] H,W 11111111 11111111		PCSR20 [W] H,W XXXXXXXX XXXXXXXX		PPG20
$00019C_H$	PDUT20 [W] H,W XXXXXXXX XXXXXXXX		PCN20 [R/W] B, H,W 0000000- 000000-0		
$0001A0_H$	PTMR21 [R] H,W 11111111 11111111		PCSR21 [W] H, W XXXXXXXX XXXXXXXX		PPG21
$0001A4_H$	PDUT21 [W] H,W XXXXXXXX XXXXXXXX		PCN21 [R/W] B, H,W 0000000- 000000-0		
$0001A8_H$	PTMR22 [R] H,W 11111111 11111111		PCSR22 [W] H,W XXXXXXXX XXXXXXXX		PPG22
$0001AC_H$	PDUT22 [W] H,W XXXXXXXX XXXXXXXX		PCN22 [R/W] B, H,W 0000000- 000000-0		
$0001B0_H$	PTMR23 [R] H,W 11111111 11111111		PCSR23 [W] H,W XXXXXXXX XXXXXXXX		PPG23
$0001B4_H$	PDUT23 [W] H,W XXXXXXXX XXXXXXXX		PCN23 [R/W] B, H,W 0000000- 000000-0		
$0001B8_H$ to $0001FC_H$	—	—	—	—	Reserved
000200_H	PWC20 [R/W] H,W ------XX XXXXXXXX		PWC10 [R/W] H,W ------XX XXXXXXXX		Stepping motor controller
000204_H	—	PWC0 [R/W] B -00000--	PWS20 [R/W] B,H,W -0000000	PWS10 [R/W] B,H,W --000000	
000208_H	PWC21 [R/W] H,W ------XX XXXXXXXX		PWC11 [R/W] H,W ------XX XXXXXXXX		
$00020C_H$	—	PWC1 [R/W] B -00000--	PWS21 [R/W] B,H,W -0000000	PWS11 [R/W] B,H,W --000000	
000210_H	PWC22 [R/W] H,W ------XX XXXXXXXX		PWC12 [R/W] H,W ------XX XXXXXXXX		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000214_H	—	PWC2 [R/W] B -00000--	PWS22 [R/W] B,H,W -0000000	PWS12 [R/W] B,H,W --000000	Stepping motor controller
000218_H	PWC23 [R/W] H,W ------XX XXXXXXXX		PWC13 [R/W] H,W ------XX XXXXXXXX		
$00021C_H$	—	PWC3 [R/W] B -00000--	PWS23 [R/W] B,H,W -0000000	PWS13 [R/W] B,H,W --000000	
000220_H	PWC24 [R/W] H,W ------XX XXXXXXXX		PWC14 [R/W] H,W ------XX XXXXXXXX		
000224_H	—	PWC4 [R/W] B -00000--	PWS24 [R/W] B,H,W -0000000	PWS14 [R/W] B,H,W --000000	
000228_H	PWC25 [R/W] H,W ------XX XXXXXXXX		PWC15 [R/W] H,W ------XX XXXXXXXX		
$00022C_H$	—	PWC5 [R/W] B -00000--	PWS25 [R/W] B,H,W -0000000	PWS15 [R/W] B,H,W --000000	
000230_H to $00023C_H$	—	—	—	—	Reserved
000240_H	CPCLR0 [R/W] W 11111111 11111111 11111111 11111111				Free-run timer 0
000244_H	TCDT0 [R/W] W 00000000 00000000 00000000 00000000				
000248_H	TCCSH0 [R/W]B, H, W 0-----00	TCCSL0 [R/W]B, H, W -1-00000	—		
$00024C_H$	CPCLR1 [R/W] W 11111111 11111111 11111111 11111111				Free-run timer 1
000250_H	TCDT1 [R/W] W 00000000 00000000 00000000 00000000				
000254_H	TCCSH1 [R/W]B, H, W 0-----00	TCCSL1 [R/W]B, H, W -1-00000	—		
000258_H	—	—	—	—	Reserved
$00025C_H$	GCN10 [R/W] H 00110010 00010000		—	GCN20 [R/W] B ----0000	PPG0,1,2,3 control
000260_H	GCN11 [R/W] H 00110010 00010000		—	GCN21 [R/W] B ----0000	PPG4,5,6,7 control
000264_H	GCN12 [R/W] H 00110010 00010000		—	GCN22 [R/W] B ----0000	PPG8,9,10,11 control

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000268_H	—	—	—	PPGDIV [R/W] B ------00	PPG0
$00026C_H$	PTMR0 [R] H,W 11111111 11111111		PCSR0 [W] H,W XXXXXXXX XXXXXXXX		
000270_H	PDUT0 [W] H,W XXXXXXXX XXXXXXXX		PCN0 [R/W] B, H,W 0000000- 000000-0		
000274_H	PTMR1 [R] H,W 11111111 11111111		PCSR1 [W] H, W XXXXXXXX XXXXXXXX		PPG1
000278_H	PDUT1 [W] H,W XXXXXXXX XXXXXXXX		PCN1 [R/W] B, H,W 0000000- 000000-0		
$00027C_H$	PTMR2 [R] H,W 11111111 11111111		PCSR2 [W] H,W XXXXXXXX XXXXXXXX		PPG2
000280_H	PDUT2 [W] H,W XXXXXXXX XXXXXXXX		PCN2 [R/W] B, H,W 0000000- 000000-0		
000284_H	PTMR3 [R] H,W 11111111 11111111		PCSR3 [W] H,W XXXXXXXX XXXXXXXX		PPG3
000288_H	PDUT3 [W] H,W XXXXXXXX XXXXXXXX		PCN3 [R/W] B, H,W 0000000- 000000-0		
$00028C_H$	PTMR4 [R] H,W 11111111 11111111		PCSR4 [W] H,W XXXXXXXX XXXXXXXX		PPG4
000290_H	PDUT4 [W] H,W XXXXXXXX XXXXXXXX		PCN4 [R/W] B, H,W 0000000- 000000-0		
000294_H	PTMR5 [R] H,W 11111111 11111111		PCSR5 [W] H,W XXXXXXXX XXXXXXXX		PPG5
000298_H	PDUT5 [W] H,W XXXXXXXX XXXXXXXX		PCN5 [R/W] B, H,W 0000000- 000000-0		
$00029C_H$	PTMR6 [R] H,W 11111111 11111111		PCSR6 [W] H,W XXXXXXXX XXXXXXXX		PPG6
$0002A0_H$	PDUT6 [W] H,W XXXXXXXX XXXXXXXX		PCN6 [R/W] B, H,W 0000000- 000000-0		
$0002A4_H$	PTMR7 [R] H,W 11111111 11111111		PCSR7 [W] H,W XXXXXXXX XXXXXXXX		PPG7
$0002A8_H$	PDUT7 [W] H,W XXXXXXXX XXXXXXXX		PCN7 [R/W] B, H,W 0000000- 000000-0		
$0002AC_H$	PTMR8 [R] H,W 11111111 11111111		PCSR8 [W] H,W XXXXXXXX XXXXXXXX		PPG8
$0002B0_H$	PDUT8 [W] H,W XXXXXXXX XXXXXXXX		PCN8 [R/W] B, H,W 0000000- 000000-0		
$0002B4_H$	PTMR9 [R] H,W 11111111 11111111		PCSR9 [W] H,W XXXXXXXX XXXXXXXX		PPG9
$0002B8_H$	PDUT9 [W] H,W XXXXXXXX XXXXXXXX		PCN9 [R/W] B, H,W 0000000- 000000-0		
$0002BC_H$	PTMR10 [R] H,W 11111111 11111111		PCSR10 [W] H,W XXXXXXXX XXXXXXXX		PPG10
$0002C0_H$	PDUT10 [W] H,W XXXXXXXX XXXXXXXX		PCN10 [R/W] B, H,W 0000000- 000000-0		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$0002C4_H$	IPCP0 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Input Capture 0,1
$0002C8_H$	IPCP1 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0002CC_H$	ICFS01 [R/W] B, H, W ------00	—	LSYNS0 [R/W] B, H, W --000000	ICS01 [R/W] B, H, W 00000000	
$0002D0_H$	IPCP2 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Input Capture 2,3
$0002D4_H$	IPCP3 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0002D8_H$	ICFS23 [R/W] B, H, W ------00	—	—	ICS23 [R/W] B, H, W 00000000	
$0002DC_H$	IPCP4 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Input Capture 4,5
$0002E0_H$	IPCP5 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0002E4_H$	ICFS45 [R/W] B, H, W ------00	—	—	ICS45 [R/W] B, H, W 00000000	
$0002E8_H$	OCCP0 [R/W] W 00000000 00000000 00000000 00000000				Output compare 0,1
$0002EC_H$	OCCP1 [R/W] W 00000000 00000000 00000000 00000000				
$0002F0_H$	OCFS01 [R/W] B, H, W ------11	—	OCSH01[R/W] B, H, W ---0--00	OCSL01[R/W] B, H, W 0000--00	
$0002F4_H$	OCCP2 [R/W] W 00000000 00000000 00000000 00000000				Output compare 2,3
$0002F8_H$	OCCP3 [R/W] W 00000000 00000000 00000000 00000000				
$0002FC_H$	OCFS23 [R/W] B, H, W ------11	—	OCSH23[R/W] B, H, W ---0--00	OCSL23[R/W] B, H, W 0000--00	
000300_H to $00030C_H$	—	—	—	—	Reserved

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000310_H	—	—	MPUCR [R/W] H 000000-0 ----0100		MPU [S] (Only the CPU can access this area)
000314_H	—	—	—	—	
000318_H	—				
$00031C_H$	—	—	—		
000320_H	DPVAR [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000324_H	—	—	DPVSR [R/W] H -------- 00000--0		
000328_H	DEAR [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00032C_H$	—	—	DESR [R/W] H -------- 00000--0		
000330_H	PABR0 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
000334_H	—	—	PACR0 [R/W] H 000000-0 00000--0		
000338_H	PABR1 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
$00033C_H$	—	—	PACR1 [R/W] H 000000-0 00000--0		
000340_H	PABR2 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
000344_H	—	—	PACR2 [R/W] H 000000-0 00000--0		
000348_H	PABR3 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
$00034C_H$	—	—	PACR3 [R/W] H 000000-0 00000--0		
000350_H	PABR4 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
000354_H	—	—	PACR4 [R/W] H 000000-0 00000--0		
000358_H	PABR5 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
$00035C_H$	—	—	PACR5 [R/W] H 000000-0 00000--0		
000360_H	PABR6 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
000364_H	—	—	PACR6 [R/W] H 000000-0 00000--0		
000368_H	PABR7 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$00036C_H$	—	—	PACR7 [R/W] H 000000-0 00000--0		MPU [S] (Only the CPU can access this area)
000370_H	PABR8 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				MPU [S] (Only product mounting MPU 12ch or 16ch) (Only the CPU can access this area)
000374_H	—	—	PACR8 [R/W] H 000000-0 00000--0		
000378_H	PABR9[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
$00037C_H$	—	—	PACR9 [R/W] H 000000-0 00000--0		
000380_H	PABR10 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
000384_H	—	—	PACR10 [R/W] H 000000-0 00000--0		
000388_H	PABR11 [R/W] ,W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
$00038C_H$	—	—	PACR11 [R/W] H 000000-0 00000--0		
000390_H	PABR12 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				MPU [S] (Only product mounting MPU 16ch) (Only the CPU can access this area)
000394_H	—	—	PACR12 [R/W] H 000000-0 00000--0		
000398_H	PABR13 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
$00039C_H$	—	—	PACR13 [R/W] H 000000-0 00000--0		
$0003A0_H$	PABR14 [R/W]W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
$0003A4_H$	—	—	PACR14 [R/W] H 000000-0 00000--0		
$0003A8_H$	PABR15 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
$0003AC_H$	—	—	PACR15 [R/W] H 000000-0 00000--0		
$0003B0_H$ to $0003FC_H$	—	—	—	—	Reserved [S]
000400_H	ICSEL0[R/W] B, H, W -----000	ICSEL1[R/W] B, H, W -----000	ICSEL2[R/W] B, H, W -------0	ICSEL3[R/W] B, H, W -------0	Generation and clear of DMA transfer request
000404_H	ICSEL4[R/W] B, H, W -------0	ICSEL5[R/W] B, H, W -------0	ICSEL6[R/W] B, H, W -----000	ICSEL7[R/W] B, H, W -----000	
000408_H	ICSEL8[R/W] B, H, W ------00	ICSEL9[R/W] B, H, W ------00	ICSEL10[R/W] B, H, W ------00	ICSEL11[R/W] B, H, W ------00	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$00040C_H$	ICSEL12[R/W] B, H, W ------00	ICSEL13[R/W] B, H, W -------0	ICSEL14[R/W] B, H, W -------0	ICSEL15[R/W] B, H, W --------	Generation and clear of DMA transfer request
000410_H	ICSEL16[R/W] B, H, W --------	ICSEL17[R/W] B, H, W --------	ICSEL18[R/W] B, H, W --------	ICSEL19[R/W] B, H, W -----000	
000414_H	ICSEL20[R/W] B, H, W -----000	ICSEL21[R/W] B, H, W ------00	ICSEL22[R/W] B, H, W ------00	—	
000418_H	IRPR0H[R] B, H, W 00------	IRPR0L[R] B, H, W 00------	IRPR1H[R] B, H, W 00------	IRPR1L[R] B, H, W 00------	Interrupt request batch read register
$00041C_H$	IRPR2H[R] B, H, W 00------	IRPR2L[R] B, H, W 00------	IRPR3H[R] B, H, W 000000--	IRPR3L[R] B, H, W 000000--	
000420_H	IRPR4H[R] B, H, W 0000----	IRPR4L[R] B, H, W 0000----	IRPR5H[R] B, H, W 0000----	IRPR5L[R] B, H, W 0-------	
000424_H	IRPR6H[R] B, H, W 00--0---	IRPR6L[R] B, H, W 000-----	IRPR7H[R] B, H, W -00-----	IRPR7L[R] B, H, W ------0-	
000428_H	IRPR8H[R] B, H, W 00------	IRPR8L[R] B, H, W 00------	IRPR9H[R] B, H, W 00------	IRPR9L[R] B, H, W 00------	
$00042C_H$	—	—	—	—	Reserved
000430_H	IRPR12H[R] B, H, W 00------	IRPR12L[R] B, H, W 00------	IRPR13H[R] B, H, W 000-----	IRPR13L[R] B, H, W 00000---	Interrupt request batch read register
000434_H	IRPR14H[R] B, H, W 00000000	IRPR14L[R] B, H, W 00000000	IRPR15H[R] B, H, W 000-----	—	
000438_H, $00043C_H$	—	—	—	—	Reserved
000440_H	ICR00 [R/W] B, H, W ---11111	ICR01 [R/W] B, H, W ---11111	ICR02 [R/W] B, H, W ---11111	ICR03 [R/W] B, H, W ---11111	Interrupt controller [S]
000444_H	ICR04 [R/W] B, H, W ---11111	ICR05 [R/W] B, H, W ---11111	ICR06 [R/W] B, H, W ---11111	ICR07 [R/W] B, H, W ---11111	
000448_H	ICR08 [R/W] B, H, W ---11111	ICR09 [R/W] B, H, W ---11111	ICR10 [R/W] B, H, W ---11111	ICR11 [R/W] B, H, W ---11111	
$00044C_H$	ICR12 [R/W] B, H, W ---11111	ICR13 [R/W] B, H, W ---11111	ICR14 [R/W] B, H, W ---11111	ICR15 [R/W] B, H, W ---11111	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000450_H	ICR16 [R/W] B, H, W ---11111	ICR17 [R/W] B, H, W ---11111	ICR18 [R/W] B, H, W ---11111	ICR19 [R/W] B, H, W ---11111	Interrupt controller [S]
000454_H	ICR20 [R/W] B, H, W ---11111	ICR21 [R/W] B, H, W ---11111	ICR22 [R/W] B, H, W ---11111	ICR23 [R/W] B, H, W ---11111	
000458_H	ICR24 [R/W] B, H, W ---11111	ICR25 [R/W] B, H, W ---11111	ICR26 [R/W] B, H, W ---11111	ICR27 [R/W] B, H, W ---11111	
$00045C_H$	ICR28 [R/W] B, H, W ---11111	ICR29 [R/W] B, H, W ---11111	ICR30 [R/W] B, H, W ---11111	ICR31 [R/W] B, H, W ---11111	
000460_H	ICR32 [R/W] B, H, W ---11111	ICR33 [R/W] B, H, W ---11111	ICR34 [R/W] B, H, W ---11111	ICR35 [R/W] B, H, W ---11111	
000464_H	ICR36 [R/W] B, H, W ---11111	ICR37 [R/W] B, H, W ---11111	ICR38 [R/W] B, H, W ---11111	ICR39 [R/W] B, H, W ---11111	
000468_H	ICR40 [R/W] B, H, W ---11111	ICR41 [R/W] B, H, W ---11111	ICR42 [R/W] B, H, W ---11111	ICR43 [R/W] B, H, W ---11111	
$00046C_H$	ICR44 [R/W] B, H, W ---11111	ICR45 [R/W] B, H, W ---11111	ICR46 [R/W] B, H, W ---11111	ICR47 [R/W] B, H, W ---11111	
000470_H to $00047C_H$	—	—	—	—	Reserved [S]
000480_H	RSTRR [R] B, H, W XXXX--XX	RSTCR [R/W] B, H, W 111----0	STBCR [R/W] B, H, W *3 000---11	—	Reset control [S] Power consumption control [S] * 3:Writing to STBCR by DMA is disabled
000484_H	—	—	—	—	Reserved [S]
000488_H	DIVR0 [R/W] B, H, W 000-----	DIVR1 [R/W] B, H, W 0001----	DIVR2 [R/W] B, H, W 0011----	—	Clock control [S]
$00048C_H$	—	—	—	—	Reserved [S]
000490_H	IORR0[R/W] B, H, W -0000000	IORR1[R/W] B, H, W -0000000	IORR2[R/W] B, H, W -0000000	IORR3[R/W] B, H, W -0000000	DMA transfer request from a peripheral [S]
000494_H	IORR4[R/W] B, H, W -0000000	IORR5[R/W] B, H, W -0000000	IORR6[R/W] B, H, W -0000000	IORR7[R/W] B, H, W -0000000	
000498_H	IORR8[R/W] B, H, W -0000000	IORR9[R/W] B, H, W -0000000	IORR10[R/W] B, H, W -0000000	IORR11[R/W] B, H, W -0000000	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$00049C_H$	IORR12[R/W] B, H, W -0000000	IORR13[R/W] B, H, W -0000000	IORR14[R/W] B, H, W -0000000	IORR15[R/W] B, H, W -0000000	DMA transfer request from a peripheral [S]
$0004A0_H$	—	—	—	—	Reserved
$0004A4_H$	CANPRE [R/W] B,H,W ----0000	—	—	—	CAN prescaler
$0004A8_H$	—	—	—	—	Reserved
$0004AC_H$	—	—	—	—	Reserved
$0004B0_H$	—	—	—	—	Reserved
$0004B4_H$	—	—	—	—	Reserved
$0004B8_H$	CUCR0 [R/W] B,H,W -------- ---0--00		CUTD0 [R/W] B,H,W 10000000 00000000		RTC/WDT1 calibration (Calibration)
$0004BC_H$	CUTR0 [R] B,H,W -------- 00000000 00000000 00000000				
$0004C0_H$	—	—	—	—	
$0004C4_H$	CUCR1 [R/W] B,H,W -------- ---0--00		CUTD1[R/W] B,H,W 11000011 01010000		
$0004C8_H$	CUTR1 [R] B,H,W -------- 00000000 00000000 00000000				
$0004CC_H$	CRTR [R/W] B,H,W 01111111	—	—	—	RC trimming setting register
$0004D0_H$ to $0004DC_H$	—	—	—	—	Reserved
$0004E0_H$ to $00050C_H$	—	—	—	—	Reserved
000510_H	CSELR [R/W] B,H,W 001---00	CMONR [R] B,H,W 001---00	MTMCR [R/W] B,H,W 00001111	STMCR [R/W] B,H,W 0000-111	Clock control [S]
000514_H	PLLCR [R/W] B,H,W -------- 11110000		CSTBR [R/W] B,H,W -0000000	PTMCR [R/W] B,H,W 00------	
000518_H	—	—	CPUAR [R/W] B,H,W 0----XXX	—	Reset [S]
$00051C_H$	—	—	—	—	Reserved [S]
000520_H	CCPSSELR [R/W] B,H,W -------0	—	—	CCPSDIVR [R/W] B,H,W -000-000	Clock control 2
000524_H	—	CCPLLFBR [R/W] B,H,W -0000000	CCSSFBR0 [R/W] B,H,W --000000	CCSSFBR1 [R/W] B,H,W ---00000	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000528_H	—	CCSSCCR0 [R/W] B,H,W ----0000	CCSSCCR1 [R/W] H,W 000----- --------		Clock control 2
$00052C_H$	—	CCCGRCR0 [R/W] B,H,W 00----00	CCCGRCR1 [R/W] B,H,W 00000000	CCCGRCR2 [R/W] B,H,W 00000000	
000530_H	CCRTSELR [R/W] B,H,W 0------0	—	CCPMUCR0 [R/W] B,H,W 0-----00	CCPMUCR1 [R/W] B,H,W 0--00000	
000534_H	—	—	—	—	
000538_H	—	—	—	—	
$00053C_H$	—	—	—	—	
000540_H to $00054C_H$	—	—	—	—	Reserved
000550_H	EIRR0 [R/W] B,H,W XXXXXXXX	ENIR0 [R/W] B,H,W 00000000	ELVR0 [R/W] B,H,W 00000000 00000000		External interrupt (INT0 to INT7)
000554_H	EIRR1 [R/W] B,H,W XXXXXXXX	ENIR1 [R/W] B,H,W 00000000	ELVR1 [R/W] B,H,W 00000000 00000000		External interrupt (INT8 to INT15)
000558_H	—	—	—	—	Reserved
$00055C_H$	—	—	WTDR[R/W] H 00000000 00000000		Real-time clock
000560_H	—	WTCRH [R/W] B ------00	WTCRM [R/W] B,H 00000000	WTCRL [R/W] B,H ----00-0	
000564_H	—	WTBRH [R/W] B --XXXXXX	WTBRM [R/W] B XXXXXXXX	WTBRL [R/W] B XXXXXXXX	
000568_H	WTHR [R/W] B,H ---00000	WTMR [R/W] B,H --000000	WTSR [R/W] B --000000	—	
$00056C_H$	—	CSVCR [R/W] B -001110- -001010-*4	—	—	Clock supervisor *4:An initial value is different by part number.For details, refer to the CSVCR register in chapter “Clock Supervisor”
000570_H to $00057C_H$	—	—	—	—	Reserved

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000580_H	REGSEL [R/W] B,H,W 0110011-	—	—	—	Regulator control
000584_H	LVD5R [R/W] B,H,W -------1	LVD5F [R/W] B,H,W 0-100--1	LVD [R/W] B,H,W 01000--0	—	Low-power detection
000588_H	GLVD5R[R/W] B,H,W 0-01-0-X	GLVD5F[R/W] B,H,W 0-0100-X	GLVD[R/W] B,H,W 010000-X	—	
$00058C_H$	—	—	—	—	Reserved
000590_H	PMUSTR [R/W] B,H,W 0-----1X	PMUCTLR [R/W] B,H,W 0-00----	PWRTMCTL [R/W] B,H,W -----011	—	PMU
000594_H	PMUINTF0 [R/W] B,H,W 00000000	PMUINTF1 [R/W] B,H,W 00000000	PMUINTF2 [R/W] B,H,W 0000----	—	
000598_H	GSTR[R] B,H,W 0-------	GCTLR[R/W] B,H,W 0000-111	—	—	
$00059C_H$	—	—	—	—	
$0005A0_H$ to $0005FC_H$	—	—	—	—	Reserved
000600_H to $00060C_H$	—	—	—	—	Reserved[S]
000610_H to $00063C_H$	—	—	—	—	Reserved[S]
000640_H to $00064C_H$	—	—	—	—	Reserved[S]
000650_H to $00067C_H$	—	—	—	—	Reserved[S]
000680_H to $00068C_H$	—	—	—	—	Reserved[S]
000690_H to $0006BC_H$	—	—	—	—	Reserved[S]
$0006C0_H$ to $0006CC_H$	—	—	—	—	Reserved[S]
$0006D0_H$ to $0006F0_H$	—	—	—	—	Reserved

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
0006F4$_H$	—	—	—	—	Reserved
0006F8$_H$ to 00070C$_H$	—	—	—	—	Reserved
000710$_H$	BPCCRA[R/W] B 00000000	BPCCRB[R/W] B 00000000	BPCCRC[R/W] B 00000000	—	Bus performance counter
000714$_H$	BPCTRA[R/W] W 00000000 00000000 00000000 00000000				
000718$_H$	BPCTRB[R/W] W 00000000 00000000 00000000 00000000				
00071C$_H$	BPCTRC[R/W] W 00000000 00000000 00000000 00000000				
000720$_H$ to 0007F8$_H$	—	—	—	—	Reserved
0007FC$_H$	BMODR[R] B, H, W XXXXXXXX	—	—	—	Operation mode
000800$_H$ to 00083C$_H$	—	—	—	—	Reserved [S]
000840$_H$	FCTLR[R/W] H -0--1000 0--0----		—	FSTR[R/W] B -----001	Flash memory register [S]
000844$_H$ to 000854$_H$	—	—	—	—	Reserved [S]
000858$_H$	—	—	WREN[R/W] H 00000000 00000000		Wild register [S]
00085C$_H$ to 00087C$_H$	—	—	—	—	Reserved [S]
000880$_H$	WRAR00[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				Wild register [S]
000884$_H$	WRDR00[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000888$_H$	WRAR01[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
00088C$_H$	WRDR01[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000890$_H$	WRAR02[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
000894$_H$	WRDR02[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000898$_H$	WRAR03[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$00089C_H$	WRDR03[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Wild register [S]
$0008A0_H$	WRAR04[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008A4_H$	WRDR04[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008A8_H$	WRAR05[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008AC_H$	WRDR05[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008B0_H$	WRAR06[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008B4_H$	WRDR06[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008B8_H$	WRAR07[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008BC_H$	WRDR07[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008C0_H$	WRAR08[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008C4_H$	WRDR08[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008C8_H$	WRAR09[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008CC_H$	WRDR09[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008D0_H$	WRAR10[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008D4_H$	WRDR10[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008D8_H$	WRAR11[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008DC_H$	WRDR11[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008E0_H$	WRAR12[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008E4_H$	WRDR12[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008E8_H$	WRAR13[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008EC_H$	WRDR13[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008F0_H$	WRAR14[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008F4_H$	WRDR14[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$0008F8_H$	WRAR15[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				Wild register [S]
$0008FC_H$	WRDR15[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000900_H to $000BF8_H$	—	—	—	—	Reserved
$000BFC_H$	—	—	UER [W] B,H,W -------- -------X		OCDU
$000C00_H$	DCCR0[R/W] W 0----000 --00--00 00000000 0-000000				DMA controller [S]
$000C04_H$	DCSR0[R/W] H 0------- -----000		DTCR0[R/W] H 00000000 00000000		
$000C08_H$	DSAR0[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C0C_H$	DDAR0[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C10_H$	DCCR1[R/W] W 0----000 --00--00 00000000 0-000000				
$000C14_H$	DCSR1[R/W] H 0------- -----000		DTCR1[R/W] H 00000000 00000000		
$000C18_H$	DSAR1[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C1C_H$	DDAR1[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C20_H$	DCCR2[R/W] W 0----000 --00--00 00000000 0-000000				
$000C24_H$	DCSR2[R/W] H 0------- -----000		DTCR2[R/W] H 00000000 00000000		
$000C28_H$	DSAR2[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C2C_H$	DDAR2[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C30_H$	DCCR3[R/W] W 0----000 --00--00 00000000 0-000000				
$000C34_H$	DCSR3[R/W] H 0------- -----000		DTCR3[R/W] H 00000000 00000000		
$000C38_H$	DSAR3[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C3C_H$	DDAR3[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C40_H$	DCCR4[R/W] W 0----000 --00--00 00000000 0-000000				
$000C44_H$	DCSR4[R/W] H 0------- -----000		DTCR4[R/W] H 00000000 00000000		
$000C48_H$	DSAR4[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$000C4C_H$	DDAR4[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				DMA controller [S]
$000C50_H$	DCCR5[R/W] W 0----000 --00--00 00000000 0-000000				
$000C54_H$	DCSR5[R/W] H 0------- -----000		DTCR5[R/W] H 00000000 00000000		
$000C58_H$	DSAR5[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C5C_H$	DDAR5[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C60_H$	DCCR6[R/W] W 0----000 --00--00 00000000 0-000000				
$000C64_H$	DCSR6[R/W] H 0------- -----000		DTCR6[R/W] H 00000000 00000000		
$000C68_H$	DSAR6[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C6C_H$	DDAR6[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C70_H$	DCCR7[R/W] W 0----000 --00--00 00000000 0-000000				
$000C74_H$	DCSR7[R/W] H 0------- -----000		DTCR7[R/W] H 00000000 00000000		
$000C78_H$	DSAR7[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C7C_H$	DDAR7[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C80_H$	DCCR8[R/W] W 0----000 --00--00 00000000 0-000000				
$000C84_H$	DCSR8[R/W] H 0------- -----000		DTCR8[R/W] H 00000000 00000000		
$000C88_H$	DSAR8[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C8C_H$	DDAR8[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C90_H$	DCCR9[R/W] W 0----000 --00--00 00000000 0-000000				
$000C94_H$	DCSR9[R/W] H 0------- -----000		DTCR9[R/W] H 00000000 00000000		
$000C98_H$	DSAR9[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C9C_H$	DDAR9[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000CA0_H$	DCCR10[R/W] W 0----000 --00--00 00000000 0-000000				
$000CA4_H$	DCSR10[R/W] H 0------- -----000		DTCR10[R/W] H 00000000 00000000		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$000CA8_H$	DSAR10[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				DMA controller [S]
$000CAC_H$	DDAR10[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000CB0_H$	DCCR11[R/W] W 0----000 --00--00 00000000 0-000000				
$000CB4_H$	DCSR11[R/W] H 0------- -----000		DTCR11[R/W] H 00000000 00000000		
$000CB8_H$	DSAR11[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000CBC_H$	DDAR11[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000CC0_H$	DCCR12[R/W] W 0----000 --00--00 00000000 0-000000				
$000CC4_H$	DCSR12[R/W] H 0------- -----000		DTCR12[R/W] H 00000000 00000000		
$000CC8_H$	DSAR12[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000CCC_H$	DDAR12[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000CD0_H$	DCCR13[R/W] W 0----000 --00--00 00000000 0-000000				
$000CD4_H$	DCSR13[R/W] H 0------- -----000		DTCR13[R/W] H 00000000 00000000		
$000CD8_H$	DSAR13[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000CDC_H$	DDAR13[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000CE0_H$	DCCR14[R/W] W 0----000 --00--00 00000000 0-000000				
$000CE4_H$	DCSR14[R/W] H 0------- -----000		DTCR14[R/W] H 00000000 00000000		
$000CE8_H$	DSAR14[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000CEC_H$	DDAR14[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000CF0_H$	DCCR15[R/W] W 0----000 --00--00 00000000 0-000000				
$000CF4_H$	DCSR15[R/W] H 0------- -----000		DTCR15[R/W] H 00000000 00000000		
$000CF8_H$	DSAR15[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000CFC_H$	DDAR15[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$000D00_H$ to $000DF0_H$	—	—	—	—	Reserved [S]
$000DF4_H$	—	—	DNMIR[R/W] B 0------0	DILVR[R/W] B ---11111	DMA controller [S]
$000DF8_H$	DMACR[R/W] W 0------- -------- 0------- --------				
$000DFC_H$	—	—	—	—	Reserved [S]
$000E00_H$	DDR00[R/W] B,H,W 00000000	DDR01[R/W] B,H,W 00000000	DDR02[R/W] B,H,W 00000000	DDR03[R/W] B,H,W 00000000	Data direction register
$000E04_H$	DDR04[R/W] B,H,W 00000000	DDR05[R/W] B,H,W 00000000	DDR06[R/W] B,H,W 00000000	DDR07[R/W] B,H,W 00000000	
$000E08_H$	DDR08[R/W] B,H,W 00000000	DDR09[R/W] B,H,W 00000000	DDR10[R/W] B,H,W 00000000	DDR11[R/W] B,H,W 00000000	
$000E0C_H$	DDR12[R/W] B,H,W 00000000	DDR13[R/W] B,H,W 00-00000	—	—	
$000E10_H$	DDRA[R/W] B,H,W 000000--	DDRB[R/W] B,H,W 000000--	DDRC[R/W] B,H,W 000000--	DDRD[R/W] B,H,W 000000--	
$000E14_H$	DDRE[R/W] B,H,W 000000--	DDRF[R/W] B,H,W 000000--	DDRG[R/W] B,H,W 00000000	DDRH[R/W] B,H,W ----0---	
$000E18_H$ to $000E1C_H$	—	—	—	—	Reserved
$000E20_H$	PFR00[R/W] B,H,W 00000000	PFR01[R/W] B,H,W 00000000	PFR02[R/W] B,H,W 00000000	PFR03[R/W] B,H,W 00000000	Port function register
$000E24_H$	PFR04[R/W] B,H,W 00000000	PFR05[R/W] B,H,W -0000000	PFR06[R/W] B,H,W 00000000	PFR07[R/W] B,H,W 00000000	
$000E28_H$	PFR08[R/W] B,H,W 00000000	PFR09[R/W] B,H,W 0-000000	PFR10[R/W] B,H,W 00000000	PFR11[R/W] B,H,W 00000000	
$000E2C_H$	PFR12[R/W] B,H,W 0-000000	PFR13[R/W] B,H,W ---00000	—	—	
$000E30_H$	PFRA[R/W] B,H,W --------	PFRB[R/W] B,H,W --------	PFRC[R/W] B,H,W --------	PFRD[R/W] B,H,W 000000--	
$000E34_H$	PFRE[R/W] B,H,W 000000--	PFRF[R/W] B,H,W 000000--	PFRG[R/W] B,H,W 00000---	PFRH[R/W] B,H,W --------	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$000E38_H$ to $000E3C_H$	—	—	—	—	Reserved
$000E40_H$	PDDR00[R] B,H,W XXXXXXXX	PDDR01[R] B,H,W XXXXXXXX	PDDR02[R] B,H,W XXXXXXXX	PDDR03[R] B,H,W XXXXXXXX	Input data direct read register
$000E44_H$	PDDR04[R] B,H,W XXXXXXXX	PDDR05[R] B,H,W XXXXXXXX	PDDR06[R] B,H,W XXXXXXXX	PDDR07[R] B,H,W XXXXXXXX	
$000E48_H$	PDDR08[R] B,H,W XXXXXXXX	PDDR09[R] B,H,W XXXXXXXX	PDDR10[R] B,H,W XXXXXXXX	PDDR11[R] B,H,W XXXXXXXX	
$000E4C_H$	PDDR12[R] B,H,W XXXXXXXX	PDDR13[R] B,H,W XX-XXXXX	—	—	
$000E50_H$	PDDRA[R] B,H,W XXXXXX--	PDDRB[R] B,H,W XXXXXX--	PDDRC[R] B,H,W XXXXXX--	PDDRD[R] B,H,W XXXXXX--	
$000E54_H$	PDDRE[R] B,H,W XXXXXX--	PDDRF[R] B,H,W XXXXXX--	PDDRG[R] B,H,W XXXXXXXX	PDDRH[R] B,H,W ----X---	
$000E58_H$ to $000E5C_H$	—	—	—	—	Reserved
$000E60_H$	EPFR00[R/W] B,H,W 00000000	EPFR01[R/W] B,H,W ----0000	EPFR02[R/W] B,H,W ---00000	EPFR03[R/W] B,H,W ---00000	Extended port function register
$000E64_H$	EPFR04[R/W] B,H,W ---00000	EPFR05[R/W] B,H,W ---00000	EPFR06[R/W] B,H,W ---00000	EPFR07[R/W] B,H,W ---00000	
$000E68_H$	EPFR08[R/W] B,H,W ---00000	EPFR09[R/W] B,H,W ---00000	EPFR10[R/W] B,H,W -0000000	EPFR11[R/W] B,H,W --000000	
$000E6C_H$	EPFR12[R/W] B,H,W --000000	EPFR13[R/W] B,H,W --000000	EPFR14[R/W] B,H,W --000000	EPFR15[R/W] B,H,W -0000000	
$000E70_H$	EPFR16[R/W] B,H,W 00000000	EPFR17[R/W] B,H,W 00000000	EPFR18[R/W] B,H,W 10000000	EPFR19[R/W] B,H,W 11111111	
$000E74_H$	EPFR20[R/W] B,H,W -1111111	EPFR21[R/W] B,H,W 00000000	EPFR22[R/W] B,H,W 00000000	EPFR23[R/W] B,H,W 00000000	
$000E78_H$	EPFR24[R/W] B,H,W -----000	EPFR25[R/W] B,H,W -----000	EPFR26[R/W] B,H,W ----0000	EPFR27[R/W] B,H,W ---00000	
$000E7C_H$	EPFR28[R/W] B,H,W ------00	EPFR29[R/W] B,H,W 00000000	EPFR30[R/W] B,H,W 00000000	EPFR31[R/W] B,H,W 00000000	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$000E80_H$	EPFR32[R/W] B,H,W 00000000	EPFR33[R/W] B,H,W ---00000	EPFR34[R/W] B,H,W ---00000	EPFR35[R/W] B,H,W ---00000	Extended port function register
$000E84_H$	EPFR36[R/W] B,H,W ---00000	EPFR37[R/W] B,H,W 00000000	EPFR38[R/W] B,H,W ---00000	EPFR39[R/W] B,H,W 00000000	Extended port function register
$000E88_H$	EPFR40[R/W] B,H,W --000000	EPFR41[R/W] B,H,W -----000	EPFR42[R/W] B,H,W ------00	EPFR43[R/W] B,H,W 00000000	
$000E8C_H$	EPFR44[R/W] B,H,W 00000000	EPFR45[R/W] B,H,W 00000000	EPFR46[R/W] B,H,W --000000	EPFR47[R/W] B,H,W -------0	
$000E90_H$	EPFR48[R/W] B,H,W 00000000	EPFR49[R/W] B,H,W 00000000	EPFR50[R/W] B,H,W 00000000	EPFR51[R/W] B,H,W ---00000	
$000E94_H$	EPFR52[R/W] B,H,W -----000	EPFR53[R/W] B,H,W ---00000	EPFR54[R/W] B,H,W ----0000	EPFR55[R/W] B,H,W ------01	
$000E98_H$ to $000E9C_H$	—	—	—	—	Reserved
$000EA0_H$	PPCR00[R/W] B,H,W 11111111	PPCR01[R/W] B,H,W 11111111	PPCR02[R/W] B,H,W 11111111	PPCR03[R/W] B,H,W 11111111	Port pull-up/down control register
$000EA4_H$	PPCR04[R/W] B,H,W 11111111	PPCR05[R/W] B,H,W 11111111	PPCR06[R/W] B,H,W 11111111	PPCR07[R/W] B,H,W 11111111	
$000EA8_H$	PPCR08[R/W] B,H,W 11111111	PPCR09[R/W] B,H,W 11111111	PPCR10[R/W] B,H,W 11111111	PPCR11[R/W] B,H,W 11111111	
$000EAC_H$	PPCR12[R/W] B,H,W 11111111	PPCR13[R/W] B,H,W 11-11111	—	—	
$000EB0_H$	PPCRA[R/W] B,H,W 111111--	PPCRB[R/W] B,H,W 111111--	PPCRC[R/W] B,H,W 111111--	PPCRD[R/W] B,H,W 111111--	
$000EB4_H$	PPCRE[R/W] B,H,W 111111--	PPCRF[R/W] B,H,W 111111--	PPCRG[R/W] B,H,W 11111111	PPCRH[R/W] B,H,W ----1---	
$000EB8_H$ to $000EBC_H$	—	—	—	—	Reserved
$000EC0_H$	PPER00[R/W] B,H,W 00000000	PPER01[R/W] B,H,W 00000000	PPER02[R/W] B,H,W 00000000	PPER03[R/W] B,H,W 00000000	Port pull-up/down enable register
$000EC4_H$	PPER04[R/W] B,H,W 00000000	PPER05[R/W] B,H,W 00000000	PPER06[R/W] B,H,W 00000000	PPER07[R/W] B,H,W 00000000	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$000EC8_H$	PPER08[R/W] B,H,W 00000000	PPER09[R/W] B,H,W 00000000	PPER10[R/W] B,H,W 00000000	PPER11[R/W] B,H,W 00000000	Port pull-up/down enable register
$000ECC_H$	PPER12[R/W] B,H,W 00000000	PPER13[R/W] B,H,W 00-00000	—	—	Port pull-up/down enable register
$000ED0_H$	PPERA[R/W] B,H,W 000000--	PPERB[R/W] B,H,W 000000--	PPERC[R/W] B,H,W 000000--	PPERD[R/W] B,H,W 000000--	
$000ED4_H$	PPERE[R/W] B,H,W 000000--	PPERF[R/W] B,H,W 000000--	PPERG[R/W] B,H,W 00000000	PPERH[R/W] B,H,W ----0---	
$000ED8_H$ to $000EDC_H$	—	—	—	—	Reserved
$000EE0_H$	PILR00[R/W] B,H,W 11111111	PILR01[R/W] B,H,W 11111111	PILR02[R/W] B,H,W 11111111	PILR03[R/W] B,H,W 11111111	Port input level selection register
$000EE4_H$	PILR04[R/W] B,H,W 11111111	PILR05[R/W] B,H,W 11111111	PILR06[R/W] B,H,W 11111111	PILR07[R/W] B,H,W 11111111	
$000EE8_H$	PILR08[R/W] B,H,W 11111111	PILR09[R/W] B,H,W 11111111	PILR10[R/W] B,H,W 11111111	PILR11[R/W] B,H,W 11111111	
$000EEC_H$	PILR12[R/W] B,H,W 11111111	PILR13[R/W] B,H,W 11-11111	—	—	
$000EF0_H$	PILRA[R/W] B,H,W 111111--	PILRB[R/W] B,H,W 111111--	PILRC[R/W] B,H,W 111111--	PILRD[R/W] B,H,W 111111--	
$000EF4_H$	PILRE[R/W] B,H,W 111111--	PILRF[R/W] B,H,W 111111--	PILRG[R/W] B,H,W 11111111	PILRH[R/W] B,H,W ----1---	
$000EF8_H$ to $000EFC_H$	—	—	—	—	Reserved
$000F00_H$	—	—	—	—	Extended Port input level selection register
$000F04_H$	—	—	EPILR06[R/W] B,H,W 00000000	EPILR07[R/W] B,H,W 00000000	
$000F08_H$	EPILR08[R/W] B,H,W 00000000	EPILR09[R/W] B,H,W 00000000	EPILR10[R/W] B,H,W 00000000	EPILR11[R/W] B,H,W 00000000	
$000F0C_H$	EPILR12[R/W] B,H,W 00000000	EPILR13[R/W] B,H,W 00-00000	—	—	
$000F10_H$	—	—	—	—	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$000F14_H$	—	—	—	—	Extended Port input level selection register
$000F18_H$ to $000F1C_H$	—	—	—	—	Reserved
$000F20_H$	—	—	—	—	Port output drive register
$000F24_H$	—	—	PODR06[R/W] B,H,W 00000000	PODR07[R/W] B,H,W 00000000	
$000F28_H$	PODR08[R/W] B,H,W 00000000	PODR09[R/W] B,H,W 00000000	PODR10[R/W] B,H,W 00000000	PODR11[R/W] B,H,W 00000000	
$000F2C_H$	PODR12[R/W] B,H,W 00000000	PODR13[R/W] B,H,W 00-00000	—	—	
$000F30_H$	—	—	—	—	
$000F34_H$	—	—	—	—	
$000F38_H$	EPODR06[R/W] B,H,W 00000000	EPODR07[R/W] B,H,W 00000000	EPODR08[R/W] B,H,W 00000000	—	Extended Port output drive register
$000F3C_H$	EPODRGD [R/W]B,H,W ----1010	EPODRGF [R/W]B,H,W --101010	—	—	
$000F40_H$	PORTEN [R/W] B,H,W -------0	—	—	—	Port input enable register
$000F44_H$ to $000F4C_H$	—	—	—	—	Reserved
$000F50_H$	—	GPLLCR[R/W] B,H,W 0------0	PTIMCR[R/W] B,H,W ----1111	PEDIVCR[R/W] B,H,W -000-000	GDC control register
$000F54_H$	—	PDIVCR[R/W] B,H,W -0000000	SDIVCR0[R/W] B,H,W --000000	SDIVCR1[R/W] B,H,W ---00000	
$000F58_H$	—	SSSCR0[R/W] B,H,W ----0000	SSSCR1[R/W] H,W 000----- --------		
$000F5C_H$	—	PGRCR0[R/W] B,H,W 00----00	PGRCR1[R/W] B,H,W 00000000	PGRCR2[R/W] B,H,W 00000000	
$000F60_H$	—	SGRCR0[R/W] B,H,W 00----00	SGRCR1[R/W] B,H,W 00000000	SGRCR2[R/W] B,H,W 00000000	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$000F64_H$	—	GDCCR[R/W] B,H,W --000001	GDCTRGR [R/W] B,H,W 0000--00	GDCSWPR [R/W] B,H,W ---00101	GDC control register
$000F68_H$ to $000F9C_H$	—	—	—	—	Reserved
$000FA0_H$	CPCLR2 [R/W] W 11111111 11111111 11111111 11111111				Dedicated LSYN input capture free-run timer 2
$000FA4_H$	TCDT2 [R/W] W 00000000 00000000 00000000 00000000				
$000FA8_H$	TCCSH2 [R/W] B, H, W 0-----00	TCCSL2 [R/W] B, H, W -1-00000	—		
$000FAC_H$	CPCLR3 [R/W] W 11111111 11111111 11111111 11111111				Dedicated LSYN input capture free-run timer 3
$000FB0_H$	TCDT3 [R/W] W 00000000 00000000 00000000 00000000				
$000FB4_H$	TCCSH3 [R/W] B, H, W 0-----00	TCCSL3 [R/W] B, H, W -1-00000	—		
$000FB8_H$ to $000FCC_H$	—	—	—	—	Reserved
$000FD0_H$	IPCP6 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Dedicated LSYN input capture 6,7
$000FD4_H$	IPCP7 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000FD8_H$	ICFS67 [R/W] B, H, W ------00	—	LSYNS1 [R/W] B,H,W ------00	ICS67 [R/W] B, H, W 00000000	
$000FDC_H$ to $000FFC_H$	—	—	—	—	Reserved
001000_H	SACR [R/W] B,H,W -------0	PICD [R/W] B,H,W ----0011	—	—	Synchronous/asynchronous switching control
001004_H to $00103C_H$	—	—	—	—	Reserved
001040_H	—	SGDER0[R/W] B,H,W 00000000	SGCR0[R/W] B,H,W -0000-0- 000--000		Sound generator 0
001044_H	SGAR0[R/W] B,H,W 00000000 00000000		SGFR0[R/W] B,H,W 00000000	SGNR0[R/W] B,H,W 00000000	
001048_H	SGTCR0[R/W] B,H,W 00000000	SGIDR0[R/W] B,H,W 00000000	SGPCR0[R/W] B,H,W 00000000 11111111		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$00104C_H$	SGDMAR0[W] B,H,W 00000000 00000000 00000000 00000000				Sound generator 0
001050_H to $00105C_H$	—	—	—	—	Reserved
001060_H	—	SGDER1[R/W] B,H,W 00000000	SGCR1[R/W] B,H,W -0000-0- 000--000		Sound generator 1
001064_H	SGAR1[R/W] B,H,W 00000000 00000000		SGFR1[R/W] B,H,W 00000000	SGNR1[R/W] B,H,W 00000000	
001068_H	SGTCR1[R/W] B,H,W 00000000	SGIDR1[R/W] B,H,W 00000000	SGPCR1[R/W] B,H,W 00000000 11111111		
$00106C_H$	SGDMAR1[W] B,H,W 00000000 00000000 00000000 00000000				
001070_H to $00107C_H$	—	—	—	—	Reserved
001080_H	—	SGDER2[R/W] B,H,W 00000000	SGCR2[R/W] B,H,W -0000-0- 000--000		Sound generator 2
001084_H	SGAR2[R/W] B,H,W 00000000 00000000		SGFR2[R/W] B,H,W 00000000	SGNR2[R/W] B,H,W 00000000	
001088_H	SGTCR2[R/W] B,H,W 00000000	SGIDR2[R/W] B,H,W 00000000	SGPCR2[R/W] B,H,W 00000000 11111111		
$00108C_H$	SGDMAR2[W] B,H,W 00000000 00000000 00000000 00000000				
001090_H to $00109C_H$	—	—	—	—	Reserved
$0010A0_H$	—	SGDER3[R/W] B,H,W 00000000	SGCR3[R/W] B,H,W -0000-0- 000—000		Sound generator 3
$0010A4_H$	SGAR3[R/W] B,H,W 00000000 00000000		SGFR3[R/W] B,H,W 00000000	SGNR3[R/W] B,H,W 00000000	
$0010A8_H$	SGTCR3[R/W] B,H,W 00000000	SGIDR3[R/W] B,H,W 00000000	SGPCR3[R/W] B,H,W 00000000 11111111		
$0010AC_H$	SGDMAR3[W] B,H,W 00000000 00000000 00000000 00000000				
$0010B0_H$ to $0010BC_H$	—	—	—	—	Reserved

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$0010C0_H$	—	SGDER4[R/W] B,H,W 00000000	SGCR4[R/W] B,H,W -0000-0- 000--000		Sound generator 4
$0010C4_H$	SGAR4[R/W] B,H,W 00000000 00000000		SGFR4[R/W] B,H,W 00000000	SGNR4[R/W] B,H,W 00000000	
$0010C8_H$	SGTCR4[R/W] B,H,W 00000000	SGIDR4[R/W] B,H,W 00000000	SGPCR4[R/W] B,H,W 00000000 11111111		
$0010CC_H$	SGDMAR4[W] B,H,W 00000000 00000000 00000000 00000000				
$0010D0_H$ to $00112C_H$	—	—	—	—	Reserved
001130_H	—	—	—	CRCCR[R/W] B,H,W -0000000	CRC arithmetic operation
001134_H	CRCINIT[R/W] B,H,W 1111111 1111111 1111111 1111111				
001138_H	CRCIN[R/W] B,H,W 00000000 00000000 00000000 00000000				
$00113C_H$	CRCR[R] B,H,W 1111111 1111111 1111111 1111111				
001140_H to $0013FC_H$	—	—	—	—	Reserved
001400_H to $001FFC_H$	—	—	—	—	Reserved (3KB)
002000_H	CTRLR0 [R/W] B,H,W -------- 000-0001		STATR0[R/W] B,H,W -------- 00000000		CAN0 (64msg)
002004_H	ERRCNT0 [R] B,H,W 00000000 00000000		BTR0[R/W] B,H,W -0100011 00000001		
002008_H	INTR0 [R] B,H,W 00000000 00000000		TESTR0[R/W] B,H,W -------- X00000--		
$00200C_H$	BRPER0 [R/W] B,H,W -------- ----0000		—		
002010_H	IF1CREQ0 [R/W] B,H,W 0------- 00000001		IF1CMSK0 [R/W] B,H,W -------- 00000000		
002014_H	IF1MSK20 [R/W] B,H,W 11-11111 11111111		IF1MSK10 [R/W] B,H,W 11111111 11111111		
002018_H	IF1ARB20 [R/W] B,H,W 00000000 00000000		IF1ARB10 [R/W] B,H,W 00000000 00000000		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$00201C_H$	IF1MCTR0 [R/W] B,H,W 00000000 0---0000		—		CAN0 (64msg)
002020_H	IF1DTA10 [R/W] B,H,W 00000000 00000000		IF1DTA20[R/W] B,H,W 00000000 00000000		
002024_H	IF1DTB10 [R/W] B,H,W 00000000 00000000		IF1DTB20 [R/W] B,H,W 00000000 00000000		
002028_H, $00202C_H$	Reserved				
002030_H, 002034_H	Reserved (IF1 data mirror)				
002038_H, $00203C_H$	Reserved				
002040_H	IF2CREQ0 [R/W] B,H,W 0------- 00000001		IF2CMSK0 [R/W] B,H,W -------- 00000000		
002044_H	IF2MSK20 [R/W] B,H,W 11-11111 11111111		IF2MSK10 [R/W] B,H,W 11111111 11111111		
002048_H	IF2ARB20 [R/W] B,H,W 00000000 00000000		IF2ARB10 [R/W] B,H,W 00000000 00000000		
$00204C_H$	IF2MCTR0 [R/W] B,H,W 00000000 0---0000		—		
002050_H	IF2DTA10 [R/W] B,H,W 00000000 00000000		IF2DTA20 [R/W] B,H,W 00000000 00000000		
002054_H	IF2DTB10 [R/W] B,H,W 00000000 00000000		IF2DTB20 [R/W] B,H,W 00000000 00000000		
002058_H, $00205C_H$	Reserved				
002060_H, 002064_H	Reserved (IF2 data mirror)				
002068_H to $00207C_H$	Reserved				
002080_H	TREQR20 [R] B,H,W 00000000 00000000		TREQR10 [R] B,H,W 00000000 00000000		
002084_H	TREQR40 [R] B,H,W 00000000 00000000		TREQR30 [R] B,H,W 00000000 00000000		
002088_H	—		—		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$00208C_H$	—		—		CAN0 (64msg)
002090_H	NEWDT20 [R] B,H,W 00000000 00000000		NEWDT10 [R] B,H,W 00000000 00000000		
002094_H	NEWDT40 [R] B,H,W 00000000 00000000		NEWDT30 [R]B,H,W 00000000 00000000		
002098_H	—		—		
$00209C_H$	—		—		
$0020A0_H$	INTPND20 [R] B,H,W 00000000 00000000		INTPND10 [R] B,H,W 00000000 00000000		
$0020A4_H$	INTPND40 [R] B,H,W 00000000 00000000		INTPND30 [R] B,H,W 00000000 00000000		
$0020A8_H$	—		—		
$0020AC_H$	—		—		
$0020B0_H$	MSGVAL20 [R] B,H,W 00000000 00000000		MSGVAL10 [R] B,H,W 00000000 00000000		
$0020B4_H$	MSGVAL40 [R] B,H,W 00000000 00000000		MSGVAL30 [R] B,H,W 00000000 00000000		
$0020B8_H$	—		—		
$0020BC_H$	—		—		
$0020C0_H$ to $0020FC_H$	Reserved				
002100_H	CTRLR1 [R/W] B,H,W -------- 000-0001		STATR1[R/W] B,H,W -------- 00000000		CAN1 (32msg)
002104_H	ERRCNT1 [R] B,H,W 00000000 00000000		BTR1[R/W] B,H,W -0100011 00000001		
002108_H	INTR1 [R] B,H,W 00000000 00000000		TESTR1[R/W] B,H,W -------- X00000--		
$00210C_H$	BRPER1 [R/W] B,H,W -------- ----0000		—		
002110_H	IF1CREQ1 [R/W] B,H,W 0------- 00000001		IF1CMSK1 [R/W] B,H,W -------- 00000000		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
002114_H	IF1MSK21 [R/W] B,H,W 11-11111 11111111		IF1MSK11 [R/W] B,H,W 11111111 11111111		CAN1 (32msg)
002118_H	IF1ARB21 [R/W] B,H,W 00000000 00000000		IF1ARB11 [R/W] B,H,W 00000000 00000000		
$00211C_H$	IF1MCTR1 [R/W] B,H,W 00000000 0---0000		—		
002120_H	IF1DTA11 [R/W] B,H,W 00000000 00000000		IF1DTA21 [R/W] B,H,W 00000000 00000000		
002124_H	IF1DTB11 [R/W] B,H,W 00000000 00000000		IF1DTB21 [R/W] B,H,W 00000000 00000000		
002128_H, $00212C_H$	Reserved				
002130_H, 002134_H	Reserved (IF1 data mirror)				
002138_H, $00213C_H$	Reserved				
002140_H	IF2CREQ1 [R/W] B,H,W 0------- 00000001		IF2CMSK1 [R/W] B,H,W -------- 00000000		
002144_H	IF2MSK21 [R/W] B,H,W 11-11111 11111111		IF2MSK11 [R/W] B,H,W 11111111 11111111		
002148_H	IF2ARB21 [R/W] B,H,W 00000000 00000000		IF2ARB11 [R/W] B,H,W 00000000 00000000		
$00214C_H$	IF2MCTR1 [R/W] B,H,W 00000000 0---0000		—		
002150_H	IF2DTA11 [R/W] B,H,W 00000000 00000000		IF2DTA21 [R/W] B,H,W 00000000 00000000		
002154_H	IF2DTB11 [R/W] B,H,W 00000000 00000000		IF2DTB21 [R/W] B,H,W 00000000 00000000		
002158_H, $00215C_H$	Reserved				
002160_H, 002164_H	Reserved (IF2 data mirror)				
002168_H to $00217C_H$	Reserved				
002180_H	TREQR21 [R] B,H,W 00000000 00000000		TREQR11 [R] B,H,W 00000000 00000000		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
002184_H	—		—		CAN1 (32msg)
002188_H	—		—		
$00218C_H$	—		—		
002190_H	NEWDT21 [R] B,H,W 00000000 00000000		NEWDT11 [R] B,H,W 00000000 00000000		
002194_H	—		—		
002198_H	—		—		
$00219C_H$	—		—		
$0021A0_H$	INTPND21 [R] B,H,W 00000000 00000000		INTPND11 [R] B,H,W 00000000 00000000		
$0021A4_H$	—		—		
$0021A8_H$	—		—		
$0021AC_H$	—		—		
$0021B0_H$	MSGVAL21 [R] B,H,W 00000000 00000000		MSGVAL11 [R] B,H,W 00000000 00000000		
$0021B4_H$	—		—		
$0021B8_H$	—		—		
$0021BC_H$	—		—		
$0021C0_H$ to $0021FC_H$	Reserved				
002200_H	CTRLR2 [R/W] B,H,W -------- 000-0001		STATR2[R/W] B,H,W -------- 00000000		CAN2 (32msg)
002204_H	ERRCNT2[R] B,H,W 00000000 00000000		BTR2[R/W] B,H,W -0100011 00000001		
002208_H	INTR2[R] B,H,W 00000000 00000000		TESTR2[R/W] B,H,W -------- X00000--		
$00220C_H$	BRPER2 [R/W] B,H,W -------- ----0000		—		
002210_H	IF1CREQ2[R/W] B,H,W 0------- 00000001		IF1CMSK2[R/W] B,H,W -------- 00000000		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
002214_H	IF1MSK22 [R/W] B,H,W 11-11111 11111111		IF1MSK12 [R/W] B,H,W 11111111 11111111		CAN2 (32msg)
002218_H	IF1ARB22 [R/W] B,H,W 00000000 00000000		IF1ARB12 [R/W] B,H,W 00000000 00000000		
$00221C_H$	IF1MCTR2[R/W] B,H,W 00000000 0---0000		—		
002220_H	IF1DTA12 [R/W] B,H,W 00000000 00000000		IF1DTA22 [R/W] B,H,W 00000000 00000000		
002224_H	IF1DTB12 [R/W] B,H,W 00000000 00000000		IF1DTB22 [R/W] B,H,W 00000000 00000000		
002228_H, $00222C_H$	Reserved				
002230_H, 002234_H	Reserved (IF1 data mirror)				
002238_H, $00223C_H$	Reserved				
002240_H	IF2CREQ2[R/W] B,H,W 0------- 00000001		IF2CMSK2[R/W] B,H,W -------- 00000000		
002244_H	IF2MSK22 [R/W] B,H,W 11-11111 11111111		IF2MSK12[R/W] B,H,W 11111111 11111111		
002248_H	IF2ARB22[R/W] B,H,W 00000000 00000000		IF2ARB12[R/W] B,H,W 00000000 00000000		
$00224C_H$	IF2MCTR2[R/W] B,H,W 00000000 0---0000		—		
002250_H	IF2DTA12[R/W] B,H,W 00000000 00000000		IF2DTA22[R/W] B,H,W 00000000 00000000		
002254_H	IF2DTB12[R/W] B,H,W 00000000 00000000		IF2DTB22[R/W] B,H,W 00000000 00000000		
002258_H, $00225C_H$	Reserved				
002260_H, 002264_H	Reserved (IF2 data mirror)				
002268_H to $00227C_H$	Reserved				
002280_H	TREQR22[R] B,H,W 00000000 00000000		TREQR12[R] B,H,W 00000000 00000000		
002284_H	—		—		
002288_H	—		—		
$00228C_H$	—		—		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
002290 H	NEWDT22[R] B,H,W 00000000 00000000		NEWDT12[R] B,H,W 00000000 00000000		CAN2 (32msg)
002294H	—		—		
002298H	—		—		
00229CH	—		—		
0022A0H	INTPND22[R] B,H,W 00000000 00000000		INTPND12[R] B,H,W 00000000 00000000		
0022A4H	—		—		
0022A8H	—		—		
0022ACH	—		—		
0022B0H	MSGVAL22[R] B,H,W 00000000 00000000		MSGVAL12[R] B,H,W 00000000 00000000		
0022B4H	—		—		
0022B8H	—		—		
0022BCH	—		—		
0022C0H to 0022FCH	—	—	—	—	Reserved
002300H	DFCTLR[R/W]B,H,W -0------ --------		—	DFSTR [R/W] B,H,W -----001	WorkFlash
002304H	—	—	—	—	
002308H	FLIFCTLR [R/W] B,H,W ---0--00	—	FLIFFER1 [R/W] B,H,W --------	FLIFFER2 [R/W] B,H,W --------	
00230CH to 0023FCH	—	—	—	—	Reserved
002400H	SEEARX[R] B,H,W --000000 00000000		DEEARX[R] B,H,W --000000 00000000		XBS RAM ECC control register
002404H	EECSRX [R/W] B,H,W ----0000	—	EFEARX[R/W] B,H,W --000000 00000000		
002408H	—	EFECRX[R/W] B,H,W -------0 00000000 00000000			
00240CH to 002FFCH	—	—	—	—	Reserved

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
003000_H	SEEARA[R] B,H,W -----000 00000000		DEEARA[R] B,H,W -----000 00000000		Backup RAM ECC control register
003004_H	EECSRA [R/W] B,H,W ----0000	—	EFEARA[R/W] B,H,W -----000 00000000		
003008_H	—	EFECRA[R/W] B,H,W -------0 00000000 00000000			
$00300C_H$ to $003FFC_H$	—	—	—	—	Reserved
004000_H to $005FFC_H$	Backup RAM				Backup RAM area
006000_H to $00EFFC_H$	—	—	—	—	Reserved
$00F000_H$ to $00FEFC_H$	—	—	—	—	Reserved [S]
$00FF00_H$	DSUCR [R/W] B,H,W -------- -------0		—	—	OCDU [S]
$00FF04_H$ to $00FF0C_H$	—	—	—	—	Reserved [S]
$00FF10_H$	PCSR [R/W] B,H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				OCDU [S]
$00FF14_H$	PSSR [R/W] B,H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00FF18_H$ to $00FFF4_H$	—	—	—	—	Reserved [S]
$00FFF8_H$	EDIR1 [R] B,H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				OCDU [S]
$00FFFC_H$	EDIR0 [R] B,H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

[S]: It is a system register. The illegal instruction exception (data access error) is generated in these registers in the user mode when reading and writing to it.

■ INTERRUPT VECTOR TABLE

This list shows the assignments of interrupt factors and interrupt vectors/interrupt control registers.

● Interrupt vector

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN*1
	Decimal	Hexa-decimal				
Reset	0	00	-	$3FC_H$	$000FFFFC_H$	-
System reserved	1	01	-	$3F8_H$	$000FFFF8_H$	-
System reserved	2	02	-	$3F4_H$	$000FFFF4_H$	-
System reserved	3	03	-	$3F0_H$	$000FFFF0_H$	-
System reserved	4	04	-	$3EC_H$	$000FFFEC_H$	-
FPU exception	5	05	-	$3E8_H$	$000FFFE8_H$	-
Exception of instruction access protection violation	6	06	-	$3E4_H$	$000FFFE4_H$	-
Exception of data access protection violation	7	07	-	$3E0_H$	$000FFFE0_H$	-
Data access error interrupt	8	08	-	$3DC_H$	$000FFFDC_H$	-
INTE instruction	9	09	-	$3D8_H$	$000FFFD8_H$	-
Instruction break	10	0A	-	$3D4_H$	$000FFFD4_H$	-
System Reserved	11	0B	-	$3D0_H$	$000FFFD0_H$	-
System Reserved	12	0C	-	$3CC_H$	$000FFFCC_H$	-
System Reserved	13	0D	-	$3C8_H$	$000FFFC8_H$	-
Exception of invalid instruction	14	0E	-	$3C4_H$	$000FFFC4_H$	-
NMI request/ XBS RAM double-bit error generation/ Backup RAM double-bit error generation	15	0F	15 (F_H) Fixed	$3C0_H$	$000FFFC0_H$	-
External interrupt 0-7	16	10	ICR00	$3BC_H$	$000FFFBC_H$	0
External interrupt 8-15	17	11	ICR01	$3B8_H$	$000FFFB8_H$	1
Reload timer 0/1	18	12	ICR02	$3B4_H$	$000FFFB4_H$	2
Reload timer 2/3	19	13	ICR03	$3B0_H$	$000FFFB0_H$	3
Multi-function serial interface ch.0(reception completed)/ Multi-function serial interface ch.0(status)	20	14	ICR04	$3AC_H$	$000FFFAC_H$	4 *2
Multi-function serial interface ch.0(transmission completed)	21	15	ICR05	$3A8_H$	$000FFFA8_H$	5
Multi-function serial interface ch.1(reception completed)/ Multi-function serial interface ch.1(status)	22	16	ICR06	$3A4_H$	$000FFFA4_H$	6*2
Multi-function serial interface ch.1(transmission completed)	23	17	ICR07	$3A0_H$	$000FFFA0_H$	7
LIN-UART2(reception completed)	24	18	ICR08	$39C_H$	$000FFF9C_H$	8

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN*1
	Decimal	Hexa-decimal				
LIN-UART2(transmission completed)	25	19	ICR09	398_H	$000FFF98_H$	9
LIN-UART3(reception completed)	26	1A	ICR10	394_H	$000FFF94_H$	10
LIN-UART3(transmission completed)	27	1B	ICR11	390_H	$000FFF90_H$	11
LIN-UART4(reception completed)	28	1C	ICR12	$38C_H$	$000FFF8C_H$	12
LIN-UART4(transmission completed)	29	1D	ICR13	388_H	$000FFF88_H$	13
LIN-UART5(reception completed)	30	1E	ICR14	384_H	$000FFF84_H$	14
LIN-UART5(transmission completed)	31	1F	ICR15	380_H	$000FFF80_H$	15
LIN-UART6(reception completed)	32	20	ICR16	$37C_H$	$000FFF7C_H$	16
LIN-UART6(transmission completed)	33	21	ICR17	378_H	$000FFF78_H$	17
CAN0	34	22	ICR18	374_H	$000FFF74_H$	-
CAN1	35	23	ICR19	370_H	$000FFF70_H$	-
CAN2	36	24	ICR20	$36C_H$	$000FFF6C_H$	-
Real time clock	37	25	ICR21	368_H	$000FFF68_H$	-
Sound generator 0 / LIN-UART7(reception completed)	38	26	ICR22	364_H	$000FFF64_H$	22
Sound generator 1 / LIN-UART7(transmission completed)	39	27	ICR23	360_H	$000FFF60_H$	23
PPG0/1/10/11/20/21	40	28	ICR24	$35C_H$	$000FFF5C_H$	24
PPG2/3/12/13/22/23	41	29	ICR25	358_H	$000FFF58_H$	25
PPG4/5/14/15	42	2A	ICR26	354_H	$000FFF54_H$	26
PPG6/7/16/17	43	2B	ICR27	350_H	$000FFF50_H$	27
PPG8/9/18/19	44	2C	ICR28	$34C_H$	$000FFF4C_H$	28
GDC / GDC_ALM	45	2D	ICR29	348_H	$000FFF48_H$	29
Main timer/Sub timer/PLL timer	46	2E	ICR30	344_H	$000FFF44_H$	30
Clock calibration unit (Sub oscillation) / Sound generator 4	47	2F	ICR31	340_H	$000FFF40_H$	31*3
A/D converter	48	30	ICR32	$33C_H$	$000FFF3C_H$	32
Clock calibration Unit (CR oscillation)	49	31	ICR33	338_H	$000FFF38_H$	33*3
Free-run timer 0/2	50	32	ICR34	334_H	$000FFF34_H$	-
Free-run timer 1/3	51	33	ICR35	330_H	$000FFF30_H$	-
ICU0/6(fetching)	52	34	ICR36	$32C_H$	$000FFF2C_H$	36
ICU1/7(fetching)	53	35	ICR37	328_H	$000FFF28_H$	37
ICU2(fetching)	54	36	ICR38	324_H	$000FFF24_H$	38
ICU3(fetching)	55	37	ICR39	320_H	$000FFF20_H$	39
ICU4(fetching)	56	38	ICR40	$31C_H$	$000FFF1C_H$	40
ICU5(fetching)	57	39	ICR41	318_H	$000FFF18_H$	41
OCU0/1(match)	58	3A	ICR42	314_H	$000FFF14_H$	42
OCU2/3(match)	59	3B	ICR43	310_H	$000FFF10_H$	43
Base timer 0 IRQ0 / Base timer 0 IRQ1 / Sound generator 2	60	3C	ICR44	$30C_H$	$000FFF0C_H$	44

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN*1
	Decimal	Hexa-decimal				
Base timer 1 IRQ0 / Base timer 1 IRQ1/ Sound generator3 / XBS RAM single bit error generation / Backup RAM single bit error generation	61	3D	ICR45	308_H	$000FFF08_H$	45*4
DMAC0/1/2/3/4/5/6/7/8/9/10/11/12/13/14/15	62	3E	ICR46	304_H	$000FFF04_H$	-
Delay interrupt	63	3F	ICR47	300_H	$000FFF00_H$	-
System Reserved (Used for REALOS™*5.)	64	40	-	$2FC_H$	$000FFEFC_H$	-
System Reserved (Used for REALOS.)	65	41	-	$2F8_H$	$000FFEF8_H$	-
Used with the INT instruction.	66 | 255	42 | FF	-	$2F4_H$ | 000_H	$000FFEF4_H$ | $000FFC00_H$	-

*1: Does not support a DMA transfer request caused by an interrupt generated from a peripheral to which no RN (Resource Number) is assigned.
*2: The status of the multi function serial interface does not support a DMA transfer request caused by I^2C reception.
*3: The clock calibration unit does not support a DMA transfer caused by an interrupt.
*4: No support for a DMA transfer caused by an interrupt because of the RAM ECC bit error.
*5: REALOS is a trademark of Fujitsu Semiconductor Limited, Japan.

■ ELECTRICAL CHARACTERISTICS

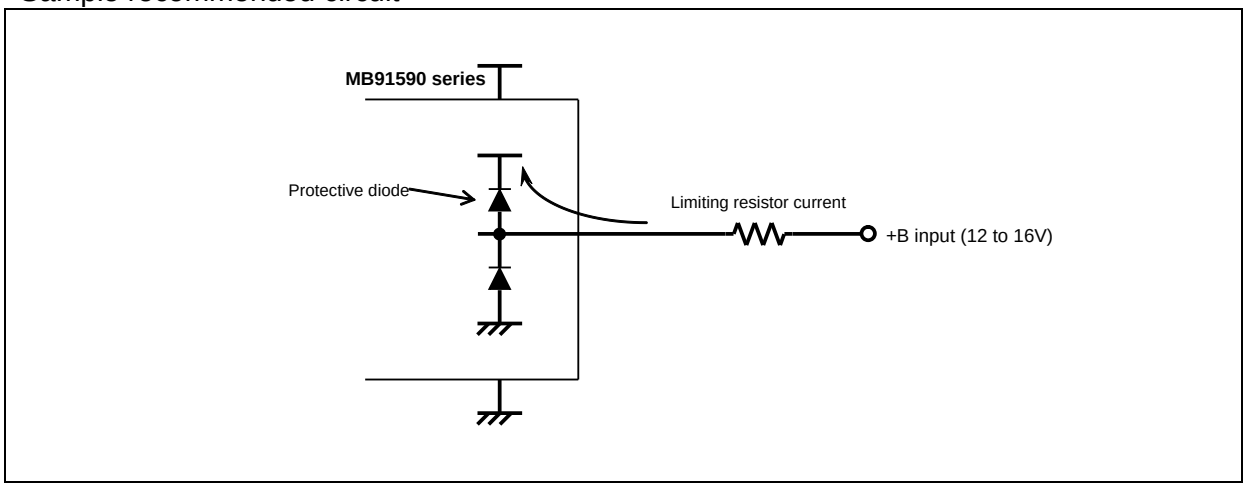
1. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1,*2	$V_{CC}5$	Vss-0.3	Vss+6.0	V	
	$V_{CC}3$	Vss-0.3	Vss+4.0	V	Vcc3 ≤ Vcc5
	DV_{CC}	Vss-0.3	Vss+6.0	V	DVcc ≤ Vcc5
Analog power supply voltage*1,*2	$AV_{CC}5$	Vss-0.3	Vss+6.0	V	AVRH5 ≤ AVcc5 ≤ Vcc5
	$AV_{CC}3$	Vss-0.3	Vss+4.0	V	AVR3 ≤ AVcc3 ≤ Vcc3
Analog reference voltage*1	AVRH5	Vss-0.3	Vss+6.0	V	AVRH5 ≤ AVcc5
	AVR3	Vss-0.3	Vss+4.0	V	AVR3 ≤ AVcc3
Input voltage*1	V_{I1}	Vss-0.3	Vcc5+0.3	V	5V pins other than SMC multiplied pins
	V_{I2}	Vss-0.3	Vcc3+0.3	V	3.3V dedicated pin
	V_{I3}	Vss-0.3	Vcc5+0.3	V	SMC shared pin
Analog pin input voltage*1	$V_{IA}5$	Vss-0.3	Vcc5+0.3	V	
	$V_{IA}3$	Vss-0.3	Vcc3+0.3	V	
Output voltage*1	V_{O1}	Vss-0.3	Vcc5+0.3	V	5V pins other than SMC multiplied pins
	V_{O2}	Vss-0.3	Vcc3+0.3	V	3.3V dedicated pin
	V_{O3}	Vss-0.3	Vcc5+0.3	V	SMC shared pin
Maximum clamp current	I_{CLAMP}	–	4	mA	*9
Total maximum clamp current	$\Sigma\|I_{CLAMP}\|$	–	20	mA	*9
"L" level maximum output current *3	I_{OL1}	–	7	mA	When setting to 2mA*6
	I_{OL2}	–	40	mA	When setting to 30mA*7
	I_{OL3}	–	30	mA	When setting to 20mA*8
"L" level average output current *4	I_{OLAV1}	–	2	mA	When setting to 2mA*6
	I_{OLAV2}	–	30	mA	When setting to 30mA*7
	I_{OLAV3}	–	20	mA	When setting to 20mA*8
"L" level total output current *5	ΣI_{OL1}	–	50	mA	*6
	ΣI_{OL2}	–	250	mA	*7
	ΣI_{OL3}	–	50	mA	*8
"H" level maximum output current *3	I_{OH1}	–	-7	mA	When setting to 2mA*6
	I_{OH2}	–	-40	mA	When setting to 30mA*7
	I_{OH3}	–	-30	mA	When setting to 20mA*8
"H" level average output current *4	I_{OHAV1}	–	-2	mA	When setting to 2mA*6
	I_{OHAV2}	–	-30	mA	When setting to 30mA*7
	I_{OHAV3}	–	-20	mA	When setting to 20mA*8

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
"H" level total output current *5	ΣI_{OH1}	–	-50	mA	*6
	ΣI_{OH2}	–	-250	mA	*7
	ΣI_{OH3}	–	-50	mA	*8
Power consumption	P_D	–	1250	mW	LQFP product
		–	2500	mW	HQFP product
Operating temperature	T_A	-40	+105	°C	
Storage temperature	Tstg	-55	+150	°C	

*1: These parameters are based on the condition that V_{SS}=AV_{SS}=DV_{SS}=0.0V
*2: Caution must be taken that AV_{CC}5 and DV_{CC} do not exceed V_{CC}5.Similarly,AV_{CC}3 must not exceed V_{CC}3.
*3: The maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.
*4: The average output current is defined as the value of the average current flowing through any one of the corresponding pins for a 10 ms period. The average value is the operation current × the operation ratio.
*5: The total output current is defined as the maximum current value flowing through all of corresponding pins.
*6: Outputs other than p60-p87 and 3V pin.
*7: Output of P60-P87 pins.
*8: Output of 3V pin.
*9: ・Corresponding pins: all general-purpose ports except P90/ADTG.(Except for the dedicated analog port)
・Use within recommended operating conditions.
・Use at DC voltage (current).
・The + B signal should always be applied by connecting a limiting resistor between the + B signal and the microcontroller.
・The value of the limiting resistor should be set so that the current input to the microcontroller pin does not exceed rated values at any time regardless of instantaneously or constantly when the + B signal is input.
・Note that when the microcontroller drive current is low, such as in the low power consumption modes, the + B input potential can increase the potential at the VCC pin via a protective diode, possibly affecting other devices.
・Note that if the + B signal is input when the microcontroller is off (not fixed at 0 V), since the power is supplied through the pin, the microcontroller may operate incompletely.
・Note that if the +B signal is input at power-on, since the power is supplied through the pin, the power-on reset may not function in the power supply voltage.
・Do not leave + B input pins open.

Sample recommended circuit



WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

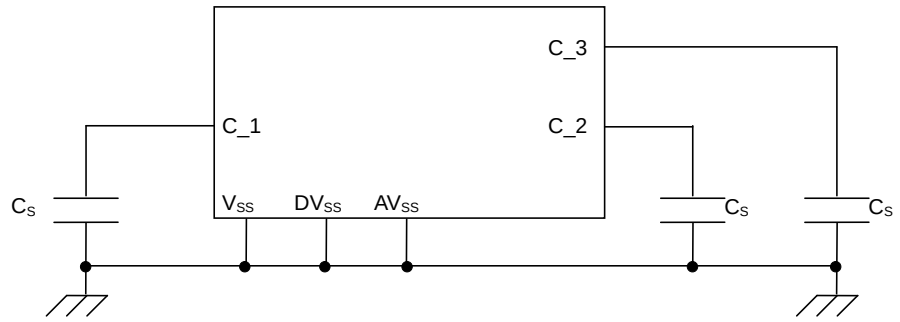
2. Recommended operating conditions

(V_{SS}=DV_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power supply voltage	$V_{CC}5$	4.5	5.5	V	Recommended operation guarantee range
	DV_{CC}	4.5	5.5	V	
	$AV_{CC}5$	4.5	5.5	V	
	$V_{CC}3$	3.0	3.6	V	
	$AV_{CC}3$	3.0	3.6	V	
	$V_{CC}5$	3.5	5.5	V	Operation guarantee range
	DV_{CC}	3.5	5.5	V	
	$AV_{CC}5$	3.5	5.5	V	
	$V_{CC}3$	2.7	3.6	V	
	$AV_{CC}3$	2.7	3.6	V	
Smoothing capacitor*	C_S	4.7 (tolerance within ±50%)		µF	Use a ceramic capacitor or a capacitor that has the similar frequency characteristics. Use a capacitor with a capacitance greater than C_S as the smoothing capacitor on the VCC pin.
Operating temperature	T_A	-40	+105	°C	

*: Refer to the following diagram for details on the connection of smoothing capacitor C_S.

・C Pin Connection Diagram



WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the electrical characteristics of the device are warranted when the device is operated within these ranges.
Always use semiconductor devices within their recommended operating condition ranges.
Operation outside these ranges may adversely affect reliability and could result in device failure.
No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact sales representatives beforehand.

3. DC characteristics

(T_A:Recommended operating conditions, $V_{CC}5$=5.0V ± 10%, $V_{CC}3$=3.3V ± 10%, V_{SS}=DV_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IH1}	P060 to P067 P070 to P077	CMOS input level is selected	0.7×$V_{CC}5$	–	$V_{CC}5$+0.3	V	
	V_{IH2}	P080 to P087 P090 to P097	CMOS hysteresis input level is selected	0.7×$V_{CC}5$	–	$V_{CC}5$+0.3	V	
	V_{IH3}	P100 to P107 P110 to P117	Automotive input level is selected	0.8×$V_{CC}5$	–	$V_{CC}5$+0.3	V	
	V_{IH4}	P120 to P127 P130 to P137	TTL input level is selected	2.0	–	$V_{CC}5$+0.3	V	
	V_{IH5}	RSTX,NMIX, MD2	–	0.7×$V_{CC}5$	–	$V_{CC}5$+0.3	V	
	V_{IH7}	MD0,MD1	–	0.7×$V_{CC}5$	–	$V_{CC}5$+0.3	V	
	V_{IH8}	DEBUGIF	–	2.0	–	$V_{CC}5$+0.3	V	
	V_{IH10}	P000 to P007 P010 to P017 P020 to P027 P030 to P037 P040 to P047 P050 to P057 PA2 to PA7 PB2 to PB7 PC2 to PC7 PD2 to PD7 PE2 to PE7 PF2 to PF7 PG0 to PG7 PH3	CMOS hysteresis input level is selected	0.7×$V_{CC}3$	–	$V_{CC}3$+0.3	V	3.3V dedicated pin
	V_{IH11}		TTL input level is selected	2.0	–	$V_{CC}3$+0.3	V	

(T_A:Recommended operating conditions, $V_{CC}5$=5.0V ± 10%, $V_{CC}3$=3.3V ± 10%, V_{SS}=DV_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level output voltage	V_{OH1}	P060 to P067 P070 to P077 P080 to P087 P090 to P097 P100 to P107 P110 to P117 P120 to P127 P130 to P137	$V_{CC}5$ = 4.5V I_{OH} = -1.0mA	$V_{CC}5$-0.5	–	$V_{CC}5$	V	
	V_{OH2}		$V_{CC}5$ = 4.5V I_{OH} = -2.0mA	$V_{CC}5$-0.5	–	$V_{CC}5$	V	
	V_{OH3}	P060 to P067 P070 to P077 P080 to P087	DV_{CC} = 4.5V I_{OH} = -30.0mA	DV_{CC}-0.5	–	DV_{CC}	V	SMC shared pin
	V_{OH4}	P000 to P007 P010 to P017 P020 to P027 P030 to P037 P040 to P047 P050 to P057 PA2 to PA7 PB2 to PB7 PC2 to PC7 PD2 to PD7 PE2 to PE7 PF2 to PF7 PG0 to PG7 PH3	$V_{CC}3$ = 3.0V I_{OH} = -2.0mA	$V_{CC}3$-0.5	–	$V_{CC}3$	V	3.3V dedicated pin
	V_{OH5}		$V_{CC}3$ = 3.0V I_{OH} = -5.0mA					
	V_{OH6}		$V_{CC}3$ = 3.0V I_{OH} = -10.0mA					
	V_{OH7}		$V_{CC}3$ = 3.0V I_{OH} = -20.0mA					

(T_A:Recommended operating conditions, $V_{CC}5$=5.0V ± 10%, $V_{CC}3$=3.3V ± 10%, V_{SS}=DV_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"L" level input voltage	V_{IL1}	P060 to P067 P070 to P077 P080 to P087 P090 to P097 P100 to P107 P110 to P117 P120 to P127 P130 to P137	CMOS input level is selected	Vss-0.3	–	0.3×$V_{CC}5$	V	
	V_{IL2}		CMOS hysteresis Input level is selected	Vss-0.3	–	0.3×$V_{CC}5$	V	
	V_{IL3}		Automotive input level is selected	Vss-0.3	–	0.5×$V_{CC}5$	V	
	V_{IL4}		TTL input level is selected	Vss-0.3	–	0.8	V	
	V_{IL5}	RSTX,NMIX, MD2	–	Vss-0.3	–	0.3×$V_{CC}5$	V	
	V_{IL7}	MD0,MD1	–	Vss-0.3	–	0.3×$V_{CC}5$	V	
	V_{IL8}	DEBUGIF	–	Vss-0.3	–	0.8	V	
	V_{IL10}	P000 to P007 P010 to P017 P020 to P027 P030 to P037 P040 to P047 P050 to P057 PA2 to PA7 PB2 to PB7 PC2 to PC7 PD2 to PD7 PE2 to PE7 PF2 to PF7 PG0 to PG7 PH3	CMOS hysteresis input level is selected	Vss-0.3	–	0.3×$V_{CC}3$	V	3.3V dedicated pin
	V_{IL11}		TTL input level is selected	Vss-0.3	–	0.8	V	

(T_A:Recommended operating conditions, $V_{CC}5$=5.0V ± 10%, $V_{CC}3$=3.3V ± 10%, V_{SS}=DV_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"L" level output voltage	V_{OL1}	P060 to P067 P070 to P077 P080 to P087 P090 to P097	$V_{CC}5$ = 4.5V I_{OL} = 1.0mA	0	–	0.4	V	
	V_{OL2}	P100 to P107 P110 to P117 P120 to P127 P130 to P137	$V_{CC}5$ = 4.5V I_{OL} = 2.0mA	0	–	0.4	V	
	V_{OL3}	P060 to P067 P070 to P077 P080 to P087	DV_{CC} = 4.5V I_{OL} = 30.0mA	0	–	0.55	V	SMC shared pin
	V_{OL4}	P127 P130 P132 P133	$V_{CC}5$ = 4.5V I_{OL} = 3.0mA	0	–	0.4	V	I^2C shared pin (I^2C is selected)
	V_{OL5}	DEBUGIF	$V_{CC}5$ = 2.7V I_{OL} = 25.0mA	0	–	0.25	V	
	V_{OL6}	P000 to P007 P010 to P017 P020 to P027 P030 to P037 P040 to P047 P050 to P057 PA2 to PA7 PB2 to PB7 PC2 to PC7 PD2 to PD7 PE2 to PE7 PF2 to PF7 PG0 to PG7 PH3	$V_{CC}3$ = 3.0V I_{OL} = 2.0mA	0	–	0.4	V	3.3V dedicated pin
	V_{OL7}		$V_{CC}3$ = 3.0V I_{OL} = 5.0mA					
	V_{OL8}		$V_{CC}3$ = 3.0V I_{OL} = 10.0mA					
	V_{OL9}		$V_{CC}3$ = 3.0V I_{OL} = 20.0mA					

(T_A:Recommended operating conditions, $V_{CC}5$=5.0V ± 10%, $V_{CC}3$=3.3V ± 10%, V_{SS}=DV_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input leak current	II_L	All input pins	VCC=DVCC=AVCC=5.5V VSS<VI<VCC	-5	–	+5	µA	
Pull-up resistance	R_{UP1}	RSTX,NMIX	–	25	–	100	kΩ	
	R_{UP2}	All 5V port input pins	Pull-up resistance is selected	25	–	100	kΩ	
	R_{UP3}	All 3V port input pins	Pull-up resistance is selected	17	–	66	kΩ	
Pull-down resistance	R_{DOWN1}	MD2	–	25	–	100	kΩ	
	R_{DOWN2}	All 5V port input pins	Pull-down resistance is selected	25	–	100	kΩ	
	R_{DOWN3}	All 3V port input pins	Pull-down resistance is selected	17	–	66	kΩ	
Input capacitance	C_{IN1}	Other than $V_{CC}3$, $V_{CC}5$, V_{SS}, DV_{CC}, DV_{SS}, $AV_{CC}3$,$AV_{SS}3$, $AV_{CC}5$,$AV_{SS}5$, C1,C2,C3, P060 to P067, P070 to P077, P080 to P087	–	–	5	15	pF	
	C_{IN2}	P060 to P067, P070 to P077, P080 to P087	When using SMC	–	15	45	pF	

(T_A:Recommended operating conditions, V_{CC}=5.0V±10%, V_{CC}3=3.3V±10%, V_{SS}=DV_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current	$I_{CC}5$	$V_{CC}5$	At normal operation F_{CP}=128MHz, Fcpp=32MHz	–	80	120	mA	
			At normal operation F_{CP}=80MHz, Fcpp=40MHz	–	60	100	mA	
			At FLASH write F_{CP}=128MHz, Fcpp=32MHz	–	95	135	mA	*3
			At FLASH erase F_{CP}=128MHz, Fcpp=32MHz	–	95	135	mA	*3
	$I_{CCS}5$		At sleep mode F_{CP}=128MHz, Fcpp=32MHz	–	25	65	mA	
	$I_{CCBS}5$		At bus sleep mode F_{CP}=128MHz, Fcpp=32MHz	–	15	55	mA	
	$I_{CCT}5$		At RTC mode, 4 MHz source oscillation	–	650	1800	µA	When using external clock*[1], T_A=+25°C
				–	800	1950		When using crystal T_A=+25°C
	$I_{CCTS}5$		When RTC mode shutdown, 4 MHz source oscillation	–	130	230	µA	When using external clock*[1], T_A=+25°C
				–	280	380	µA	When using crystal T_A=+25°C
	$I_{CCH}5$		At stop mode	–	250	1400	µA	T_A=+25°C
	$I_{CCHS}5$		When stop mode shutdown	–	100	200	µA	T_A=+25°C
	$I_{CC}3$	$V_{CC}3$	When GDC normal operation F_{gdC}=81MHz, $F_{gdC\text{-}IF}$=108MHz,	–	100	200	mA	
			When GDC operation stop	–	2	100	mA	
			When GDC side regulator stop	–	70	200	µA	
	I_A3	$AV_{CC}3$	When NTSC operates	–	30	60	mA	At AVR3=AVss3
			When NTSC stop	–	5	10	mA	At AVR3=AVss3

(T_A:Recommended operating conditions, V_{CC}=5.0V ± 10%, V_{CC}3=3.3V±10%, V_{SS}=DV_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
High current output drive capacity Phase-to-phase deviation1	ΔV_{OH3}	PWM1Pn, PWM1Mn, PWM2Pn, PWM2Mn, n=0 to 5	DVcc=4.5V I_{OH}=30.0mA Maximum deviation of V_{OH3}	–	–	90	mV	*2
High current output drive capacity Phase-to-phase deviation2	ΔV_{OL3}	PWM1Pn, PWM1Mn, PWM2Pn, PWM2Mn, n=0 to 5	Vcc=4.5V I_{OL}=30.0mA Maximum deviation of V_{OL2}	–	–	90	mV	*2

*1: The power supply current value when the external clock is supplied from the X1 pin. Note that the power supply current value when using the external clock is different from that using the oscillator.

*2: If PWM1P0/PWM1M0/PWM2P0/PWM2M0 of ch.0 is turned on simultaneously, the maximum deviation of V_{OH3} / V_{OL3} for each pin is defined. Same for other channels.

*3: This product contains both program flash and WorkFlash. This parameter is defined when only one of them is in the write/erase state.

4. AC Characteristics

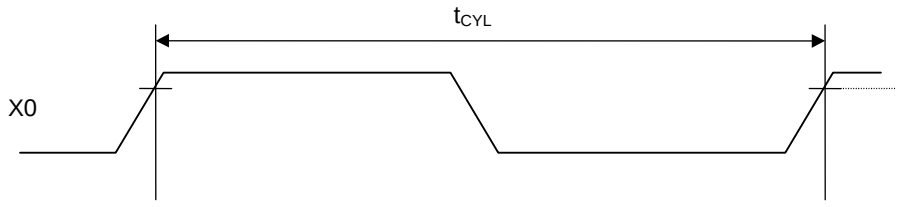
(1) Main Clock Timing

(T_A:Recommended operating conditions, $V_{CC}5$=5.0V ± 10%, V_{SS}=DV_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Source oscillation clock frequency	F_C	X0,X1	–	–	4	–	MHz	
Source oscillation clock cycle time	t_{CYL}	X0,X1	–	–	250	–	ns	–
Internal operating clock frequency*	F_{CP}	–	–	2	–	128	MHz	CPU clock
	F_{CPP}	–	–	2	–	40	MHz	Peripheral bus clock
Internal operating clock cycle time*	t_{CP}	–	–	7.8125	–	500	ns	CPU clock
	t_{CPP}	–	–	25	–	500	ns	Peripheral bus clock
CAN PLL jitter (when lock)	t_{PJ}	–	–	-10	–	+10	ns	F_{CP}=80MHz (4MHz×Multiplied by 20)
Built-in CR oscillation frequency	F_{CCR}	–	–	50	100	200	kHz	

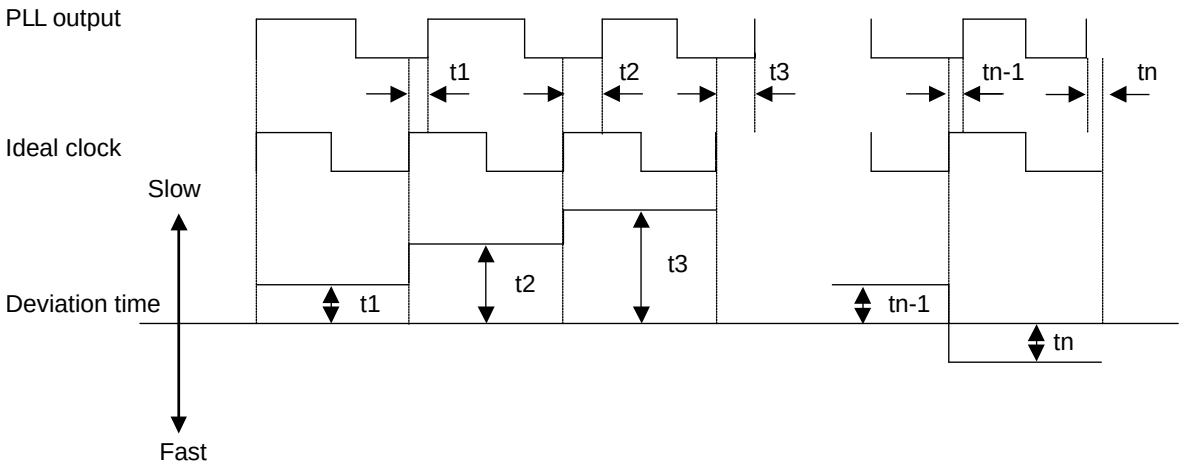
*: The maximum / minimum value is defined when using the main clock and PLL clock.

・X0,X1 clock timing



・CAN PLL jitter

Deviation time from the ideal clock is assured per cycle out of 20, 000 cycles.

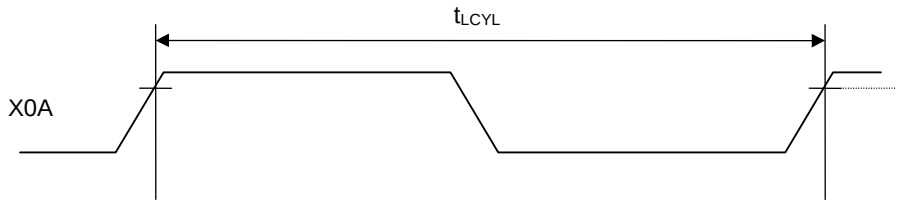


(1-2) Sub clock timing(products without s-suffix)

(T_A:Recommended operating conditions, $V_{CC}5$=5.0V ± 10%, V_{SS}=DV_{SS}=AV_{SS}=0.0V)

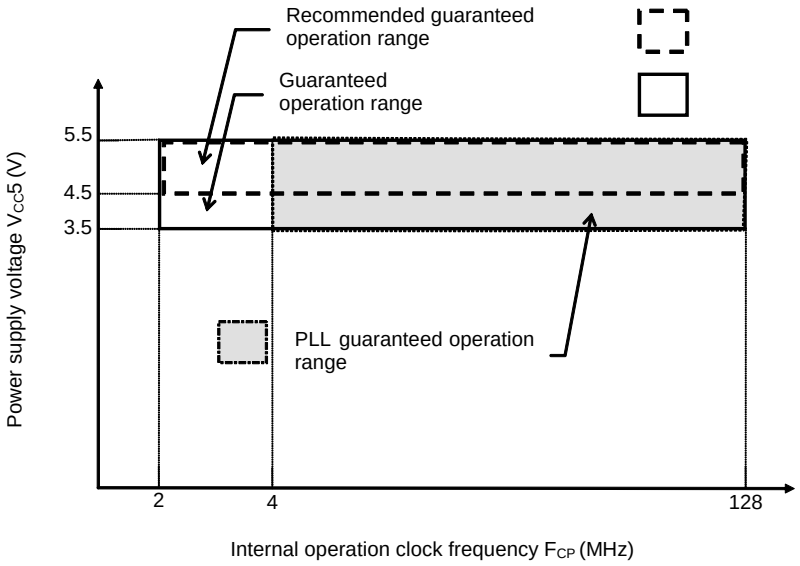
Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Source oscillation clock frequency	F_{CL}	X0A,X1A	–	–	32.768	–	kHz	
Source oscillation clock cycle time	t_{LCYL}	X0A,X1A		–	30.52	–	µs	

・X0A,X1A clock timing



・Guaranteed operation range(5V operating microcontroller section)

Internal operation clock frequency vs. Power supply voltage

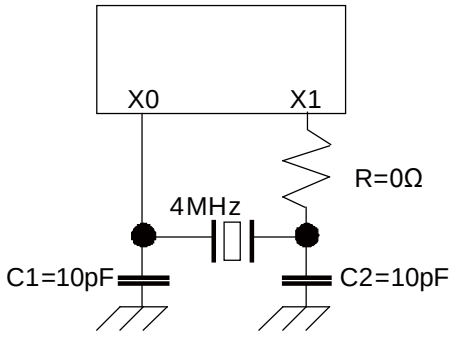


Note: The CPU will be reset at the power supply voltage 4V±0.3V or less.

Oscillation clock frequency vs. Internal operation clock frequency

		Internal operation clock frequency							
		Main Clock	PLL clock						
			Multiplied by 1	Multiplied by 2	Multiplied by 3	Multiplied by 4	...	Multiplied by 20	Multiplied by 32
Oscillation clock frequency	4MHz	2MHz	4MHz	8MHz	12MHz	16MHz	...	80MHz	128MHz

・Example of oscillation circuit

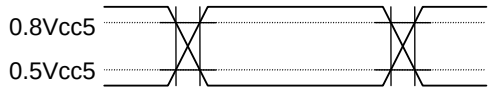


Note: As to the product with its clock supervisor's initial value is "ON", when the oscillator is unable to start within 20ms from the stop state the clock supervisor will detect the oscillation stop. As a result, the CPU moves to the fail safe operation.
Design your print circuit board so that the oscillator can start oscillation within 20ms.

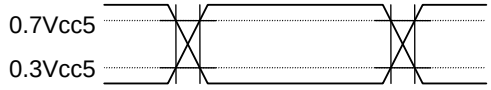
AC characteristics are specified by the following measurement reference voltage values.

・Input Signal Waveform

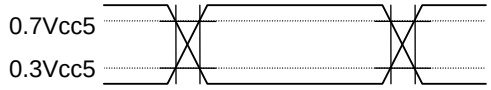
Hysteresis Input Pin (Automotive)



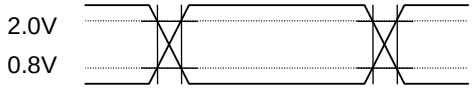
Hysteresis Input Pin (CMOS Normal)



Hysteresis Input Pin (CMOS Hysteresis)

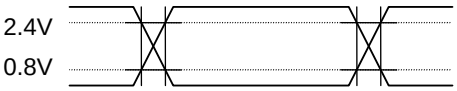


TTL Input Pin



・Output Signal Waveform

Output Pin

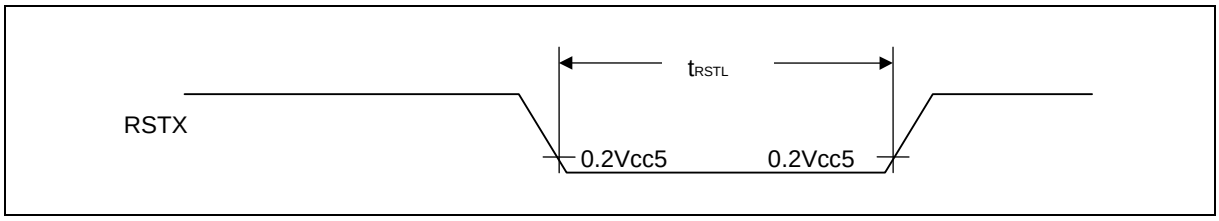


(2) Reset Input

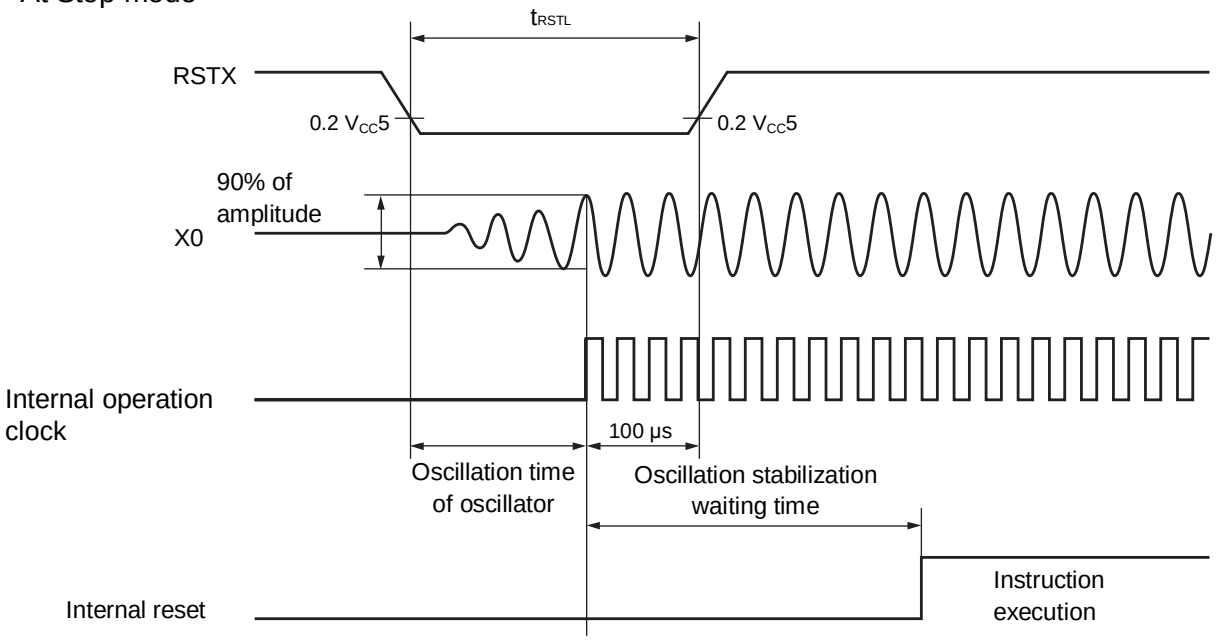
(T_A: Recommended operating conditions, $V_{CC}5$=5.0V ± 10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Reset input time	t_{RSTL}	RSTX	–	10	–	µs	When normal operation
				Oscillation time of oscillator*+ 100µs	–	ms	At Stop mode
				100µs	–	µs	At RTC mode
Width for reset input removal				1µs	–	µs	

*: The oscillation time of the oscillator is the time it takes for the amplitude of the oscillations to reach 90%. For crystal oscillators, this time is between several ms and several tens of ms, for ceramic oscillators the time is between several hundred µs and several ms, and for an external clock, the time is 0 ms.



・At Stop mode



(3) Power-on Conditions

(T_A: Recommended operating conditions, V_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Level detection voltage	–	$V_{CC}5$	–	2.1	2.3	2.5	V	When turning on power for microcontroller
Level detection hysteresis width	–	$V_{CC}5$	–	–	–	125	mV	During voltage drop
Level detection time	–	–	–	–	–	30	us	*1
Slope detection undetected standard	–	$V_{CC}5$	$V_{CC}5$ = at level detection release level time	–	–	4	mV/µs	*2
Power off time	t_{OFF}	$V_{CC}5$	–	50	–	–	ms	*3

*1: If the fluctuation of the power supply is faster than the low voltage detection time, there is the possibility to generate or release after the power supply voltage has exceeded the detection voltage range.

*2: When setting the power supply fluctuation to this standard or less, it is possible to suppress the slope detection. This is the standard when the power supply fluctuation is stable.

*3: This time is to start the slope detection at next power on after power down and internal charge loss.

(4) Multi-function Serial

(4-1) UART timing

Bit setting: SMR: MD2=0, SMR: MD1=1, SMR: MD0=0, SMR: SCINV=0, SCR: SPI=0

(T_A: Recommended operating conditions, $V_{CC}5$=5.0V ± 10%, V_{SS}=AV_{SS}=0.0V)

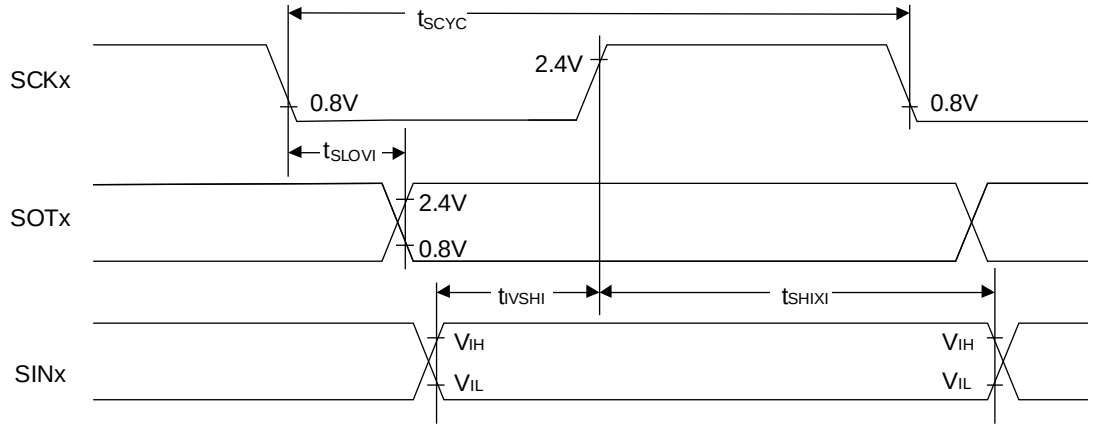
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0,SCK1	–	$4t_{CPP}$	–	ns	Internal shift clock mode: C_L=50pF(When drive capability is 2mA or more.) C_L=20pF(When drive capability is 1mA)
SCK ↓ → SOT delay time	t_{SLOVI}	SCK0,SCK1 SOT0,SOT1		-30	+30	ns	
Valid SIN → SCK ↑setup time	t_{IVSHI}	SCK0,SCK1 SIN0,SIN1		34	–	ns	
SCK ↑ → Valid SIN hold time	t_{SHIXI}			0	–	ns	
Serial clock "H"pulse width	t_{SHSL}	SCK0,SCK1	–	t_{CPP}+10	–	ns	External shift clock mode: C_L=50pF(When drive capability is 2mA or more.) C_L=20pF(When drive capability is 1mA)
Serial clock "L" pulse width	t_{SLSH}			$2t_{CPP}$-10	–	ns	
SCK ↓ → SOT delay time	t_{SLOVE}	SCK0,SCK1 SOT0,SOT1		–	33	ns	
Valid SIN → SCK ↑setup time	t_{IVSHE}	SCK0,SCK1 SIN0,SIN1		10	–	ns	
SCK ↑ → Valid SIN hold time	t_{SHIXE}			20	–	ns	
SCK fall time	t_F	SCK0,SCK1		–	5	ns	
SCK rise time	t_R	SCK0,SCK1		–	5	ns	

Notes: ・AC characteristic in CLK synchronized mode.

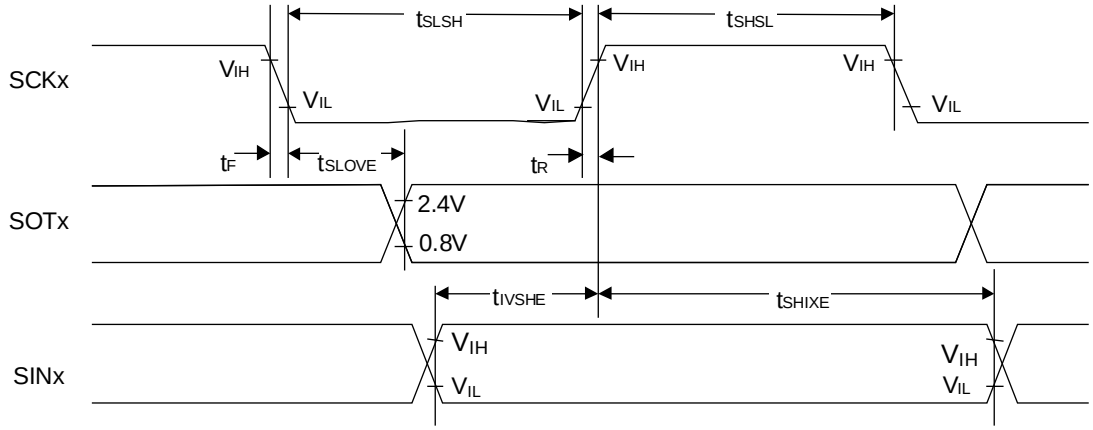
・C_L is the load capacitance applied to pins during testing.

・The maximum bard rate is limited by internal operation clock used and other parameters. Refer to Hardware Manual for details.

• Internal shift clock mode



• External shift clock mode



Bit setting: SMR: MD2=0, SMR: MD1=1, SMR: MD0=0, SMR: SCINV=1, SCR: SPI=0

(T_A: Recommended operating conditions, $V_{CC}5$=5.0V ± 10%, V_{SS}=AV_{SS}=0.0V)

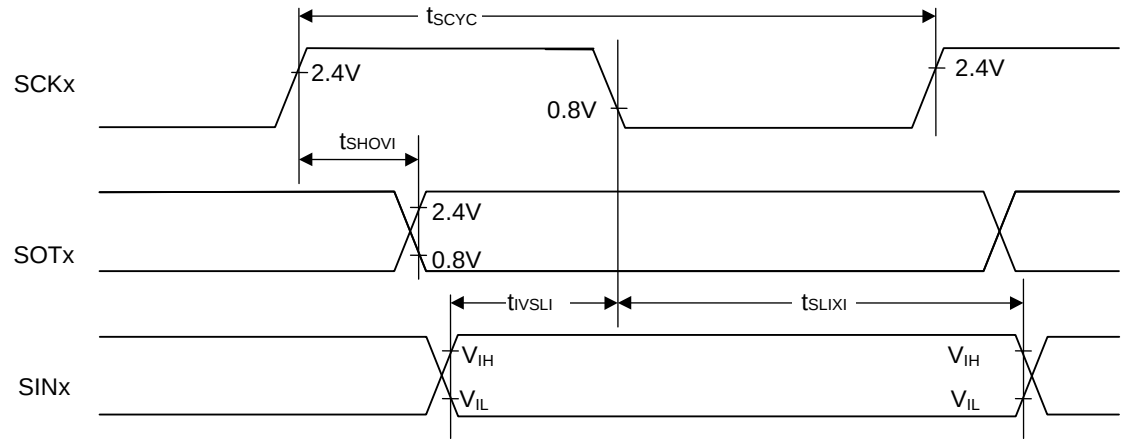
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0,SCK1	–	$4t_{CPP}$	–	ns	Internal shift clock mode: C_L=50pF(When drive capability is 2mA or more.) C_L=20pF(When drive capability is 1mA)
SCK ↑ → SOT delay time	t_{SHOVI}	SCK0,SCK1 SOT0,SOT1		-30	+30	ns	
Valid SIN → SCK ↓setup time	t_{IVSLI}	SCK0,SCK1 SIN0,SIN1		34	–	ns	
SCK ↓ → Valid SIN hold time	t_{SLIXI}			0	–	ns	
Serial clock "H" pulse width	t_{SHSL}	SCK0,SCK1	–	t_{CPP}+10	–	ns	External shift clock mode: C_L=50pF(When drive capability is 2mA or more.) C_L=20pF(When drive capability is 1mA)
Serial clock "L"pulse width	t_{SLSH}			$2t_{CPP}$-10	–	ns	
SCK ↑ → SOT delay time	t_{SHOVE}	SCK0,SCK1 SOT0,SOT1		–	33	ns	
Valid SIN → SCK ↓setup time	t_{IVSLE}	SCK0,SCK1 SIN0,SIN1		10	–	ns	
SCK↓ → Valid SIN hold time	t_{SLIXE}			20	–	ns	
SCK fall time	tF	SCK0,SCK1		–	5	ns	
SCK rise time	tR	SCK0,SCK1		–	5	ns	

Notes: • AC characteristic in CLK synchronized mode.

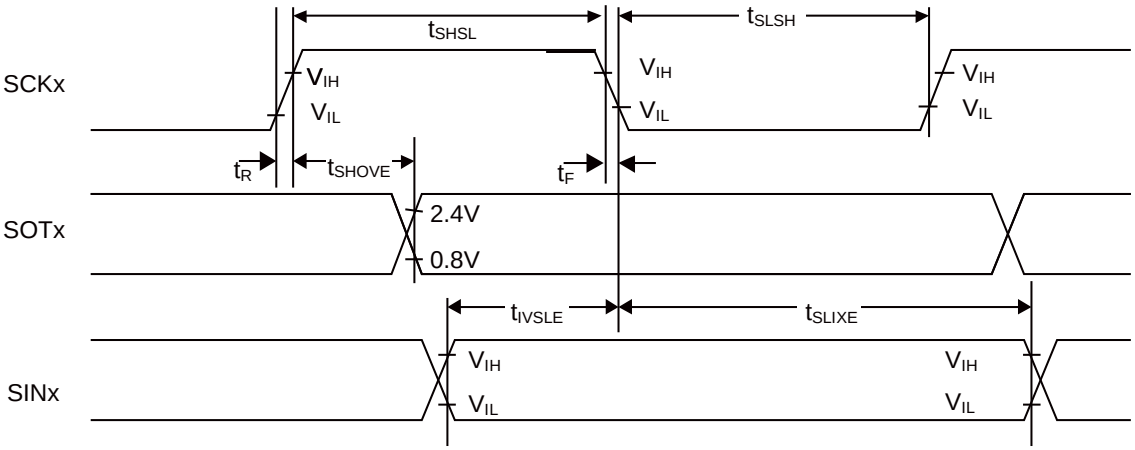
• C_L is the load capacitance applied to pins during testing.

• The maximum bard rate is limited by internal operation clock used and other parameters. Refer to Hardware Manual for details.

・Internal shift clock mode



・External shift clock mode



Bit setting: SMR: MD2=0, SMR: MD1=1, SMR: MD0=0, SMR: SCINV=0, SCR: SPI=1

(T_A: Recommended operating conditions, $V_{CC}5$=5.0V ± 10%, V_{SS}=AV_{SS}=0.0V)

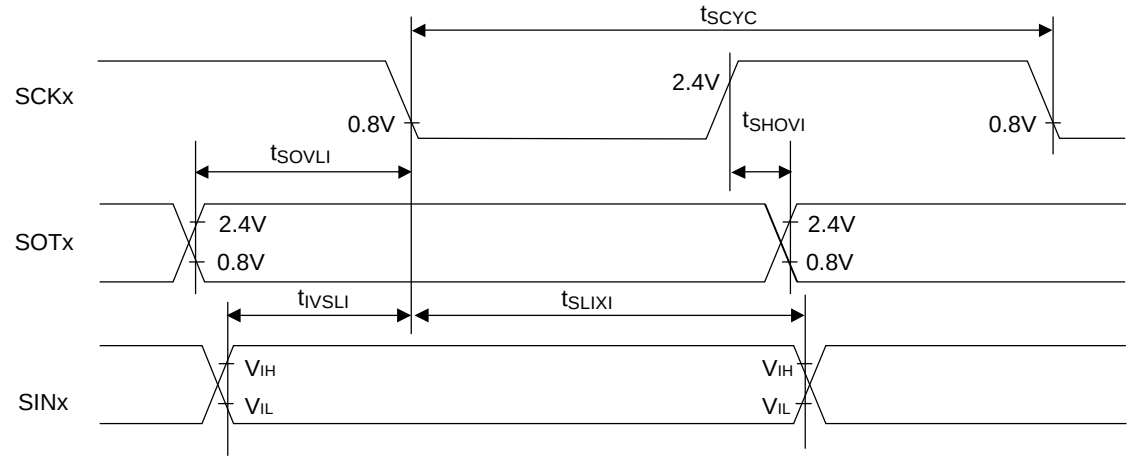
Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Min	
Serial clock cycle time	t_{SCYC}	SCK0,SCK1	Internal shift clock mode C_L=50pF(When drive capability is 2mA or more.) C_L=20pF(When drive capability is 1mA)	$4t_{CPP}$	–	ns
SCK↑→SOT delay time	t_{SHOVI}	SCK0,SCK1, SOT0,SOT1		-30	+30	ns
Valid SIN→SCK↓ setup time	t_{IVSLI}	SCK0,SCK1, SIN0,SIN1		34	–	ns
SCK↓→ Valid SIN hold time	t_{SLIXI}			0	–	ns
SOT→SCK↓ delay time	t_{SOVLI}	SCK0,SCK1, SOT0,SOT1		$2t_{CPP}$-30	–	ns
Serial clock "H" pulse width	t_{SHSL}	SCK0,SCK1	External shift clock mode C_L=50pF(When drive capability is 2mA or more.) C_L=20pF(When drive capability is 1mA)	t_{CPP}+10	–	ns
Serial clock "L" pulse width	t_{SLSH}			$2t_{CPP}$-10	–	ns
SCK↑→SOT delay time	t_{SHOVE}	SCK0,SCK1, SOT0,SOT1		–	33	ns
Valid SIN→SCK↓ setup time	t_{IVSLE}	SCK0,SCK1, SIN0,SIN1		10	–	ns
SCK↓→ Valid SIN hold time	t_{SLIXE}			20	–	ns
SCK fall time	tF	SCK0,SCK1		–	5	ns
SCK rise time	tR	SCK0,SCK1		–	5	ns

Notes: • AC characteristic in CLK synchronized mode.

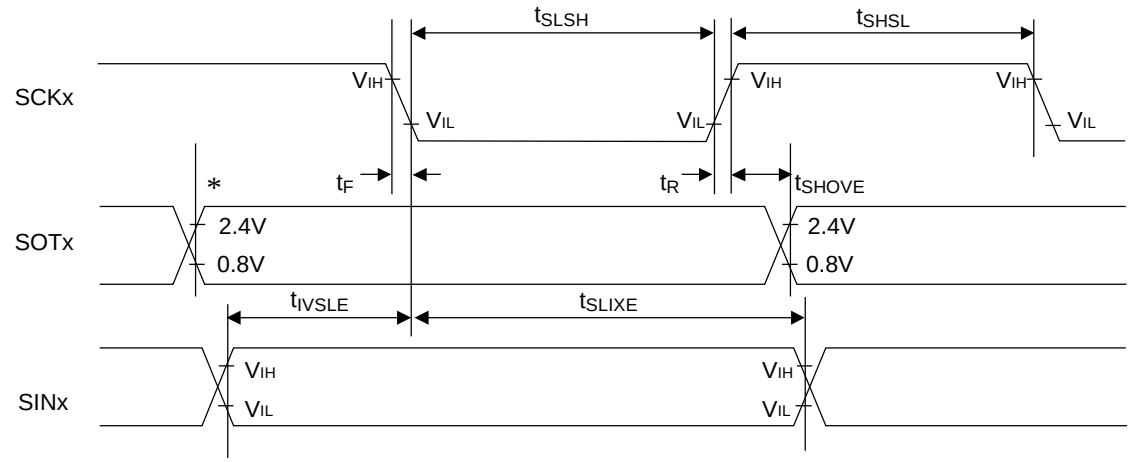
• C_L is the load capacitance applied to pins during testing.

• The maximum bard rate is limited by internal operation clock used and other parameters. Refer to Hardware Manual for details.

・Internal shift clock mode



・External shift clock mode



*: Changes when writing to TDR register

Bit setting: SMR: MD2=0, SMR: MD1=1, SMR: MD0=0, SMR: SCINV=1, SCR: SPI=1

(T_A: Recommended operating conditions, $V_{CC}5$=5.0V ± 10%, V_{SS}=AV_{SS}=0.0V)

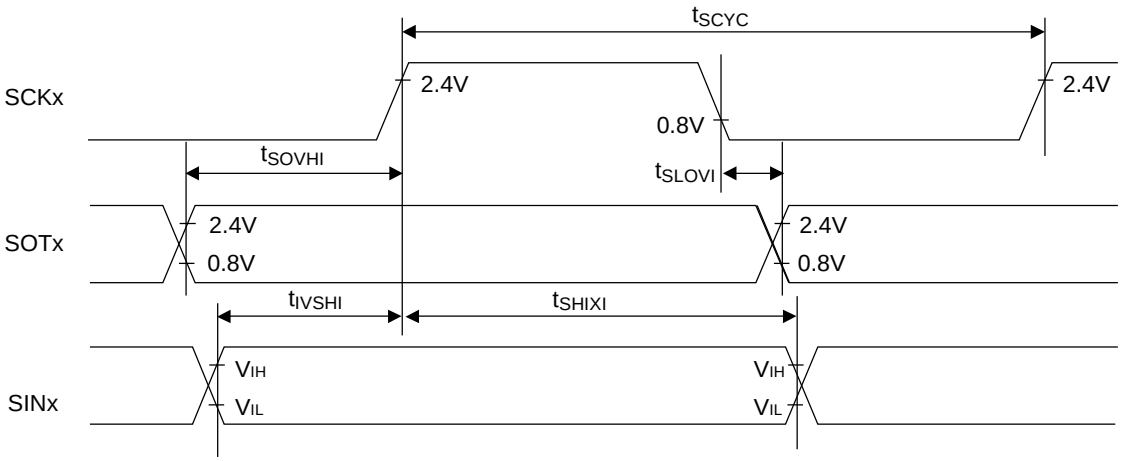
Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Min	
Serial clock cycle time	t_{SCYC}	SCK0,SCK1	Internal shift clock mode C_L=50pF(When drive capability is 2mA or more.) C_L=20pF(When drive capability is 1mA)	$4t_{CPP}$	–	ns
SCK↓→SOT delay time	t_{SLOVI}	SCK0,SCK1, SOT0,SOT1		-30	+30	ns
Valid SIN→SCK↑ setup time	t_{IVSHI}	SCK0,SCK1, SIN0,SIN1		34	–	ns
SCK↑→ Valid SIN hold time	t_{SHIXI}			0	–	ns
SOT→SCK↑ delay time	t_{SOVHI}	SCK0,SCK1, SOT0,SOT1		$2t_{CPP}$-30	–	ns
Serial clock "H"pulse width	t_{SHSL}	SCK0,SCK1	External shift clock mode C_L=50pF(When drive capability is 2mA or more.) C_L=20pF(When drive capability is 1mA)	t_{CPP}+10	–	ns
Serial clock "L" pulse width	t_{SLSH}			$2t_{CPP}$-10	–	ns
SCK↓→SOT delay time	t_{SLOVE}	SCK0,SCK1, SOT0,SOT1		–	33	ns
Valid SIN→SCK↑ setup time	t_{IVSHE}	SCK0,SCK1, SIN0,SIN1		10	–	ns
SCK↑→ Valid SIN hold time	t_{SHIXE}			20	–	ns
SCK fall time	t_F	SCK0,SCK1		–	5	ns
SCK rise time	t_R	SCK0,SCK1		–	5	ns

Notes: • AC characteristic in CLK synchronized mode.

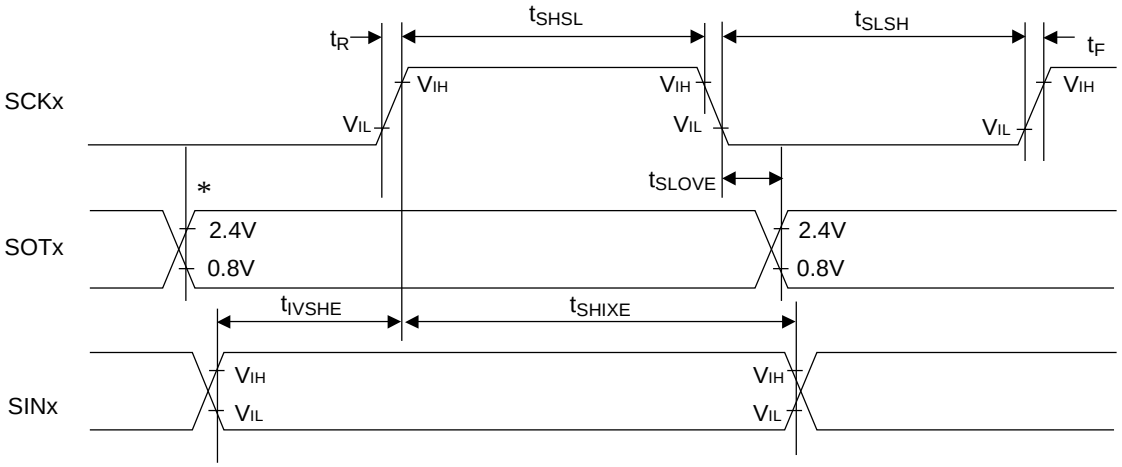
• C_L is the load capacitance applied to pins during testing.

• The maximum bard rate is limited by internal operation clock used and other parameters. Refer to Hardware Manual for details.

・Internal shift clock mode



・External shift clock mode

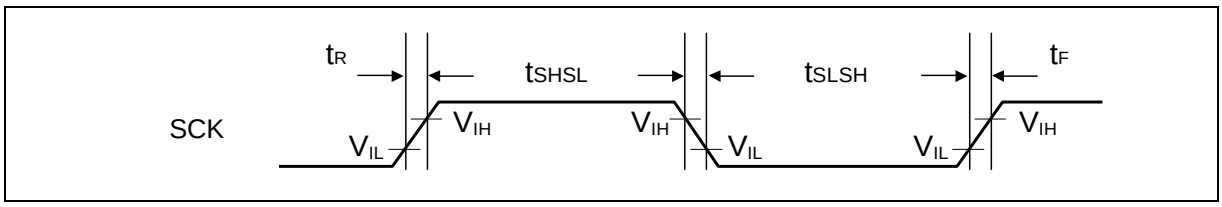


*: Changes when writing to TDR register

(4-2)External clock (EXT = 1): asynchronous only

(T_A: Recommended operating conditions, $V_{CC}5$=5.0V±10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock "H" pulse width	t_{SHSL}	SCK0, SCK1	C_L=50pF (When drive capability is 2mA or more.) C_L=20pF (When drive capability is 1mA)	t_{CPP}+10	-	ns
Serial clock "L" pulse width	t_{SLSH}			t_{CPP}+10	-	ns
SCK fall time	t_F			-	5	ns
SCK rise time	t_R			-	5	ns



(4-3) I^2C timing

(T_A: Recommended operating conditions, $V_{CC}5$=5.0V ± 10%, V_{SS}=AV_{SS}=0.0V)

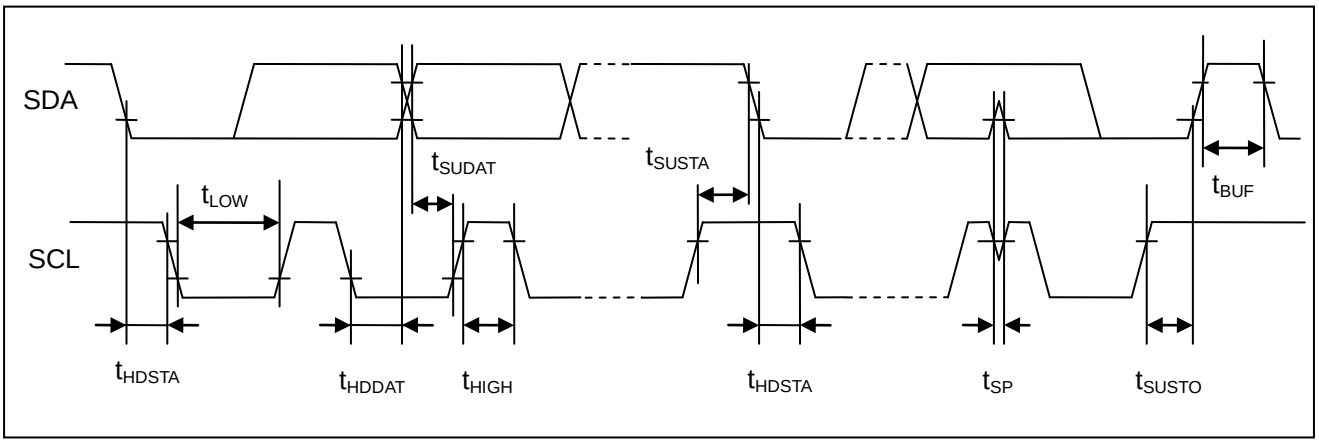
Parameter	Symbol	Pin name	Conditions	Standard mode		High-speed mode*3		Unit	Remarks
				Min	Max	Min	Max		
SCL clock frequency	f_{SCL}	SCK0,SCK1,	C_L=50pF (When drive capability is 2mA or more.) C_L=20pF (When drive capability is 1mA) R = (V_P/I_{OL}) *1	0	100	0	400	kHz	
Repeat "start" condition hold time SDA ↓ → SCL ↓	t_{HDSTA}	SOT0,SOT1, (SDA) SCK0,SCK1, (SCL)		4.0	–	0.6	–	µs	
Period of "L" for SCL clock	t_{LOW}	SCK0,SCK1, (SCL)		4.7	–	1.3	–	µs	
Period of "H" for SCL clock	t_{HIGH}	SCK0,SCK1, (SCL)		4.0	–	0.6	–	µs	
Repeat "start" condition setup time SCL ↑ → SDA ↓	t_{SUSTA}	SCK0,SCK1, (SCL)		4.7	–	0.6	–	µs	
Data hold time SCL ↓ → SDA ↓ ↑	t_{HDDAT}	SOT0,SOT1, (SDA) SCK0,SCK1, (SCL)		0	3.45*2	0	0.9*3	µs	
Data setup time SDA ↓ ↑ → SCL ↑	t_{SUDAT}	SOT0,SOT1, (SDA) SCK0,SCK1, (SCL)		250	–	100	–	ns	
"Stop" condition setup time SCL ↑ → SDA ↑	t_{SUSTO}	SOT0,SOT1, (SDA) SCK0,SCK1, (SCL)		4.0	–	0.6	–	µs	
Bus-free time between "stop" condition and "start" condition	t_{BUF}	–		4.7	–	1.3	–	µs	
Noise filter	t_{SP}	–	–	$2t_{CPP}$ *4	–	$2t_{CPP}$ *4	–	ns	

*1: R and C_L represent the pull-up resistance and load capacitance of the SCL and SDA output lines, respectively.
Vp shows that the power-supply voltage of the pull-up resistor and I_{OL} shows the V_{OL} guarantee current.

*2: The maximum t_{HDDAT} only has to be met if the device does not extend the "L" width (t_{LOW}) of the SCL signal.

*3: A high-speed mode I^2C bus device can be used on a standard mode I^2C bus system as long as the device satisfies the requirement of "$t_{SUDAT} \geq 250$ ns".

*4: t_{CPP} is the peripheral clock cycle time. Adjust the clock of the bus in the surrounding to 8MHz or more when use I^2C.


SDA
SCL
tLOW
tSUDAT
tSUSTA
tBUF
tHDSTA
tHDDAT
tHIGH
tHDSTA
tSP
tSUSTO

(5)LIN-UART timing

・Bit setting: ESCR: SCES=0, ECCR: SCDE=0

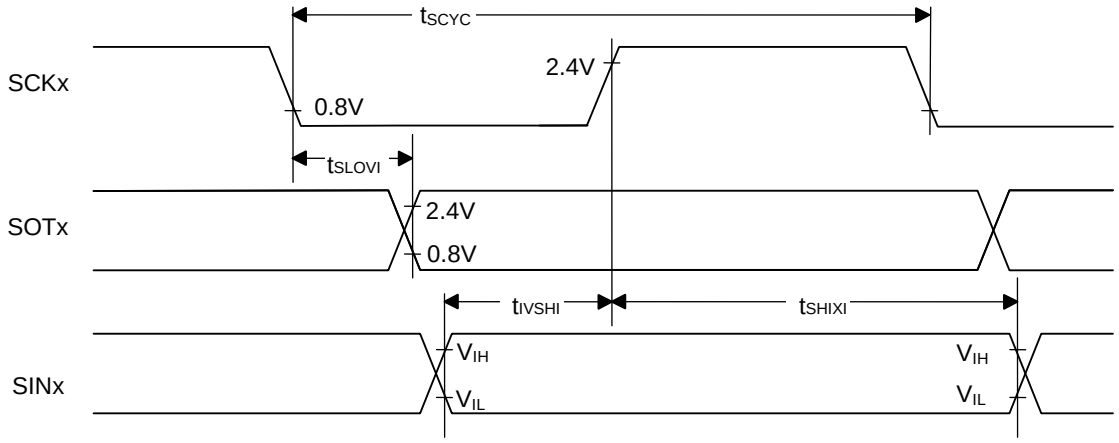
(T_A: Recommended operating conditions, $V_{CC}5$=5.0V ± 10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK2,SCK3, SCK4,SCK5, SCK6,SCK7	–	$5t_{CPP}$	–	ns	Internal shift clock mode: C_L=80pF + 1・TTL
SCK ↓ → SOT delay time	t_{SLOVI}	SCK2,SCK3, SCK4,SCK5, SCK6,SCK7, SOT2,SOT3, SOT4,SOT5, SOT6,SOT7		-50	+50	ns	
Valid SIN → SCK ↑setup time	t_{IVSHI}	SCK2,SCK3, SCK4,SCK5, SCK6,SCK7, SIN2,SIN3, SIN4,SIN5, SIN6,SIN7		t_{CPP}+80	–	ns	
SCK ↑ → Valid SIN hold time	t_{SHIXI}			0	–	ns	
Serial clock "L" pulse width	t_{SLSH}	SCK2,SCK3, SCK4,SCK5, SCK6,SCK7	–	$3t_{CPP}$-t_R	–	ns	External shift clock mode: C_L=80pF + 1・TTL
Serial clock "H" pulse width	t_{SHSL}			t_{CPP}+10	–	ns	
SCK ↓ → SOT delay time	t_{SLOVE}	SCK2,SCK3, SCK4,SCK5, SCK6,SCK7, SOT2,SOT3, SOT4,SOT5, SOT6,SOT7		–	$2t_{CPP}$+60	ns	
Valid SIN → SCK ↑setup time	t_{IVSHE}	SCK2,SCK3, SCK4,SCK5, SCK6,SCK7, SIN2,SIN3, SIN4,SIN5, SIN6,SIN7		30	–	ns	
SCK ↑ → Valid SIN hold time	t_{SHIXE}			t_{CPP}+30	–	ns	
SCK fall time	t_F	SCK2,SCK3, SCK4,SCK5, SCK6,SCK7		–	10	ns	
SCK rise time	t_R			–	40	ns	

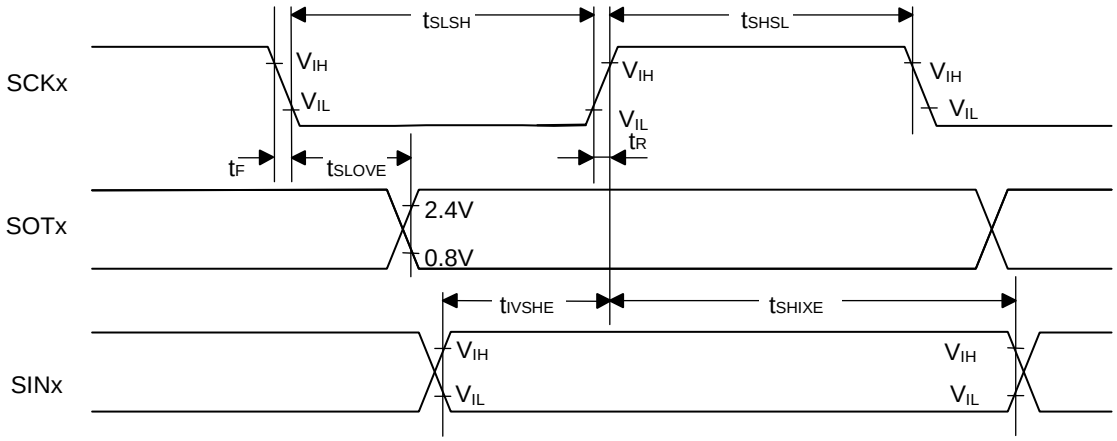
Notes: ・C_L is the load capacitance applied to pins during testing.

・The maximum bard rate is limited by internal operation clock used and other parameters. Refer to Hardware Manual for details.

・Internal shift clock mode



・External shift clock mode



・Bit setting: ESCR: SCES=1, ECCR: SCDE=0

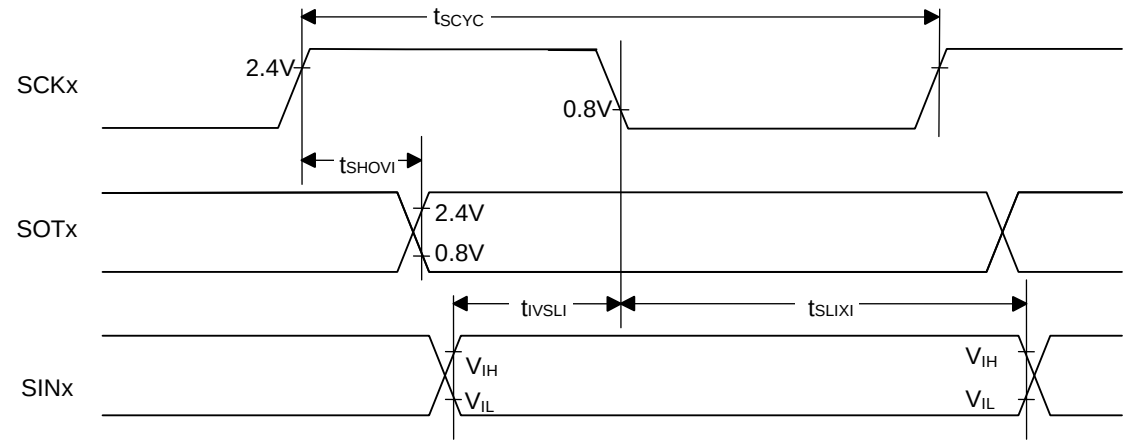
(T_A: Recommended operating conditions, $V_{CC}5$=5.0V ± 10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK2,SCK3, SCK4,SCK5, SCK6,SCK7	–	$5t_{CPP}$	–	ns	Internal shift clock mode: C_L=80pF+1・TTL
SCK ↑ → SOT delay time	t_{SHOVI}	SCK2,SCK3, SCK4,SCK5, SCK6,SCK7, SOT2,SOT3, SOT4,SOT5, SOT6,SOT7		-50	+50	ns	
Valid SIN → SCK ↓setup time	t_{IVSLI}	SCK2,SCK3, SCK4,SCK5, SCK6,SCK7, SIN2,SIN3, SIN4,SIN5, SIN6,SIN7		t_{CPP}+80	–	ns	
SCK ↓ → Valid SIN hold time	t_{SLIXI}			0	–	ns	
Serial clock "H" pulse width	t_{SHSL}	SCK2,SCK3, SCK4,SCK5, SCK6,SCK7	–	$3t_{CPP}$-t_R	–	ns	External shift clock mode: C_L=80pF+1・TTL
Serial clock "L" pulse width	t_{SLSH}			t_{CPP}+10	–	ns	
SCK ↑ → SOT delay time	t_{SHOVE}	SCK2,SCK3, SCK4,SCK5, SCK6,SCK7, SOT2,SOT3, SOT4,SOT5, SOT6,SOT7		–	$2t_{CPP}$+60	ns	
Valid SIN → SCK ↓setup time	t_{IVSLE}	SCK2,SCK3, SCK4,SCK5, SCK6,SCK7, SIN2,SIN3, SIN4,SIN5, SIN6,SIN7		30	–	ns	
SCK ↓ → Valid SIN hold time	t_{SLIXE}			t_{CPP}+30	–	ns	
SCK fall time	t_F	SCK2,SCK3, SCK4,SCK5, SCK6,SCK7		–	10	ns	
SCK rise time	t_R			–	40	ns	

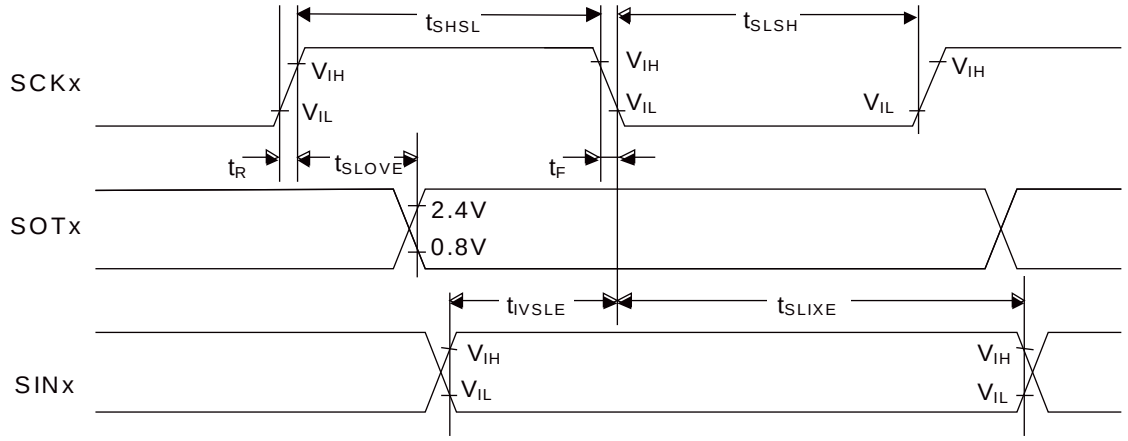
Notes: ・C_L is the load capacitance applied to pins during testing.

・The maximum bard rate is limited by internal operation clock used and other parameters. Refer to Hardware Manual for details.

・Internal shift clock mode



・External shift clock mode



・Bit setting: ESCR: SCES=0, ECCR: SCDE=1

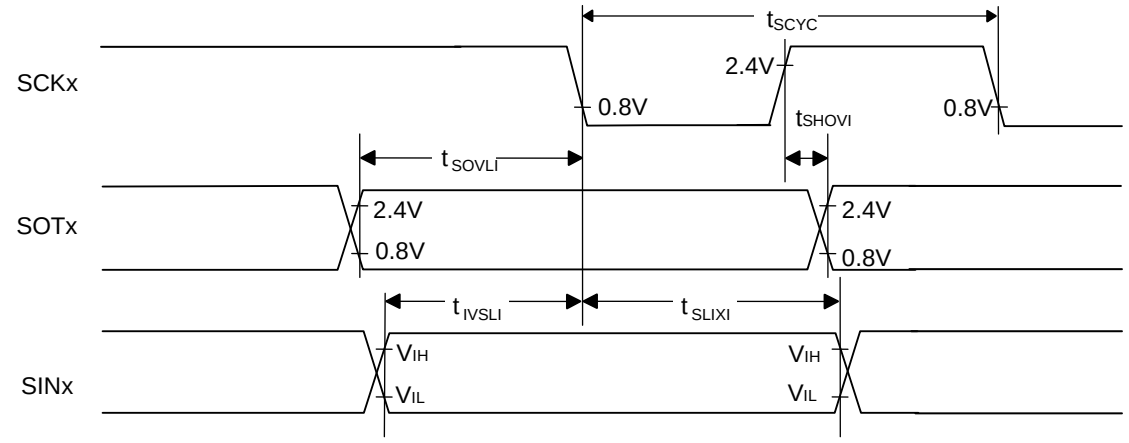
(T_A: Recommended operating conditions, $V_{CC}5$=5.0V ± 10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK2,SCK3, SCK4,SCK5, SCK6,SCK7	–	$5t_{CPP}$	–	ns	Internal shift clock Mode: C_L=80pF + 1 ・TTL
SCK ↑ → SOT delay time	t_{SHOVI}	SCK2,SCK3, SCK4,SCK5, SCK6,SCK7, SOT2,SOT3, SOT4,SOT5, SOT6,SOT7		-50	+50	ns	
Valid SIN→ SCK ↓ setup time	t_{IVSLI}	SCK2,SCK3, SCK4,SCK5, SCK6,SCK7, SIN2,SIN3, SIN4,SIN5, SIN6,SIN7		t_{CPP}+80	–	ns	
SCK ↓ → Valid SIN hold time	t_{SLIXI}			0	–	ns	
SOT → SCK ↓ delay time	t_{SOVLI}	SCK2,SCK3, SCK4,SCK5, SCK6,SCK7, SOT2,SOT3, SOT4,SOT5, SOT6,SOT7		$3t_{CPP}$-70	–	ns	

Notes: ・C_L is the load capacitance applied to pins during testing.

・The maximum bard rate is limited by internal operation clock used and other parameters. Refer to Hardware Manual for details.

・Internal shift clock mode



・Bit setting: ESCR: SCES=1, ECCR: SCDE=1

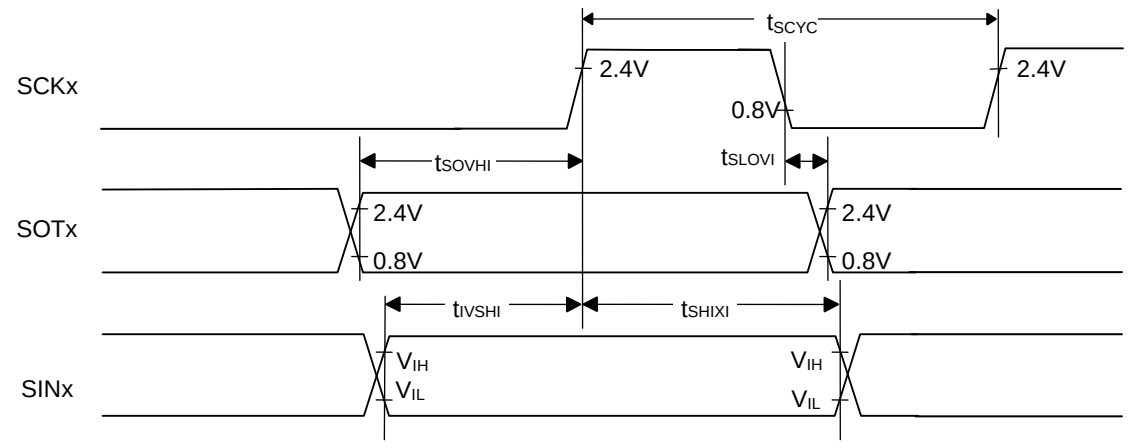
(T_A: Recommended operating conditions, $V_{CC}5$=5.0V ± 10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK2,SCK3, SCK4,SCK5, SCK6,SCK7	–	$5t_{CPP}$	–	ns	Internal shift clock mode: C_L=80pF+1・TTL
SCK ↓ → SOT delay time	t_{SLOVI}	SCK2,SCK3, SCK4,SCK5, SCK6,SCK7, SOT2,SOT3, SOT4,SOT5, SOT6,SOT7		-50	+50	ns	
Valid SIN → SCK ↑setup time	t_{IVSHI}	SCK2,SCK3, SCK4,SCK5, SCK6,SCK7, SIN2,SIN3, SIN4,SIN5, SIN6,SIN7		t_{CPP}+80	–	ns	
SCK ↑ → Valid SIN hold time	t_{SHIXI}			0	–	ns	
SOT → SCK ↑ delay time	t_{SOVHI}	SCK2,SCK3, SCK4,SCK5, SCK6,SCK7, SOT2,SOT3, SOT4,SOT5, SOT6,SOT7		$3t_{CPP}$-70	–	ns	

Notes: ・C_L is the load capacitance applied to pins during testing.

・The maximum bard rate is limited by internal operation clock used and other parameters. Refer to Hardware Manual for details.

・Internal shift clock mode

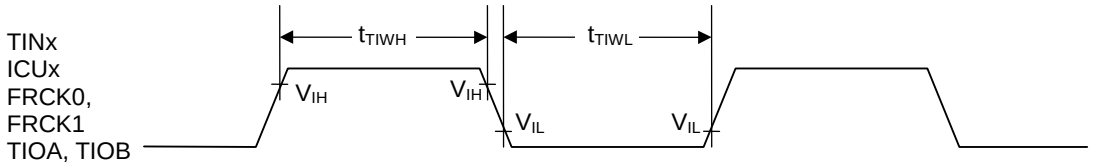


(6) Timer input timing

(T_A: Recommended operating conditions, $V_{CC}5$=5.0V ± 10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH} t_{TIWL}	TIN0,TIN1, TIN2,TIN3, ICU0 to ICU5, FRCK0,FRCK1, TIOA,TIOB	–	$4t_{CPP}$	–	ns	

・Timer input timing

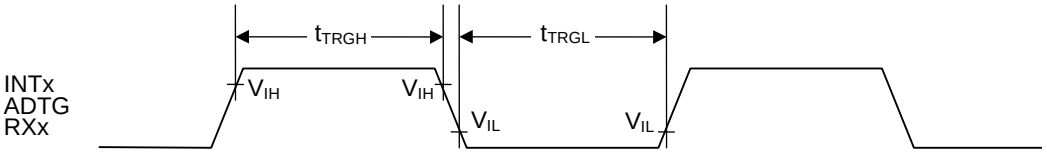


(7) Trigger input timing

(T_A: Recommended operating conditions, $V_{CC}5$=5.0V ± 10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH} t_{TRGL}	INT0 to INT15, ADTG, RX0, RX1, RX2	–	$5t_{CPP}$	–	ns	
				1	–	µs	At stop mode

・Trigger input timing

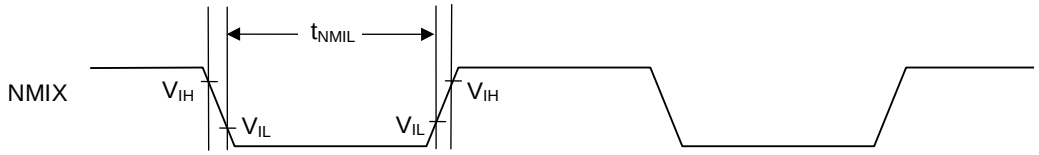


(8) NMI input timing

(T_A: Recommended operating conditions, $V_{CC}5$=5.0V ± 10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{NMIL}	NMIX	–	$4t_{CPP}$	–	ns	

・NMIX input timing



(9) Low voltage detection (External low-voltage detection)

(T_A: Recommended operating conditions, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply voltage range	$V_{CC}5$	VCC5	–	–	–	5.5	V	Microcontroller unit
	$V_{CC}3$	VCC3	–	–	–	3.6	V	GDC unit
Detection voltage	V_{DL}	VCC5	*1	3.9	4.1	4.3	V	When power-supply voltage falls at microcontroller unit and detection level is set initially
		VCC3	*1	2.2	2.4	2.6	V	When power-supply voltage falls at GDC unit and detection level is set initially
Hysteresis width	V_{HYS}	VCC5/ VCC3	–	–	–	125	mV	When power-supply voltage rises
Low voltage detection time	Td	–	–	–	–	30	µs	
Power supply voltage fluctuation rate	–	VCC5 VCC3	–	-2	–	2	V/ms	*2

*1: If the power supply voltage fluctuates within the time less than the low voltage detection time (Td), there is a possibility that the low-voltage detection will occur or stop after the power supply voltage passes the detection range.

*2: In order to perform the low-voltage detection at the detection voltage (V_{DL}), be sure to suppress fluctuation of the power supply voltage within the limits of the power supply voltage fluctuation rate.

(10) Low voltage detection (Internal low-voltage detection)

(T_A: Recommended operating conditions, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply voltage range	V_{RDP5}	VCC	–	–	–	1.3	V	
Detection voltage	V_{RDL}		*	0.8	0.9	1.0	V	When power-supply voltage falls
Hysteresis width	V_{RHYS}		–	–	–	50	mV	When power-supply voltage rises
Low voltage detection time	Td	–	–	–	–	30	µs	

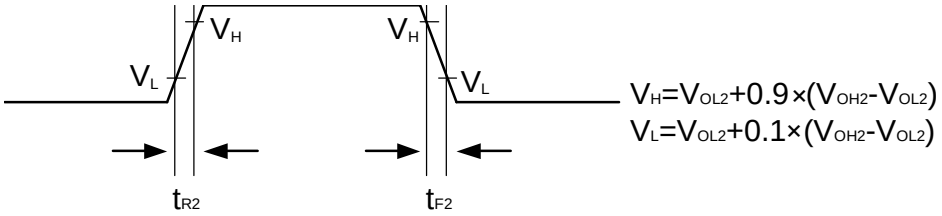
*: If the fluctuation of the power supply is faster than the low voltage detection time(Td), there is a possibility to generate or release after the power supply voltage has exceeded the detection voltage range.

(11) High current output slew rate

(T_A: Recommended operating conditions, $V_{CC}5=AV_{CC}5=5.0V \pm 10\%$, $V_{SS}=AV_{SS}=0.0V$)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Output rise /fall time	t_{R2} t_{F2}	P060 to P067, P070 to P077, P080 to P087	–	15	–	100	ns	load capacitance 85pF

・Slew rate output timing



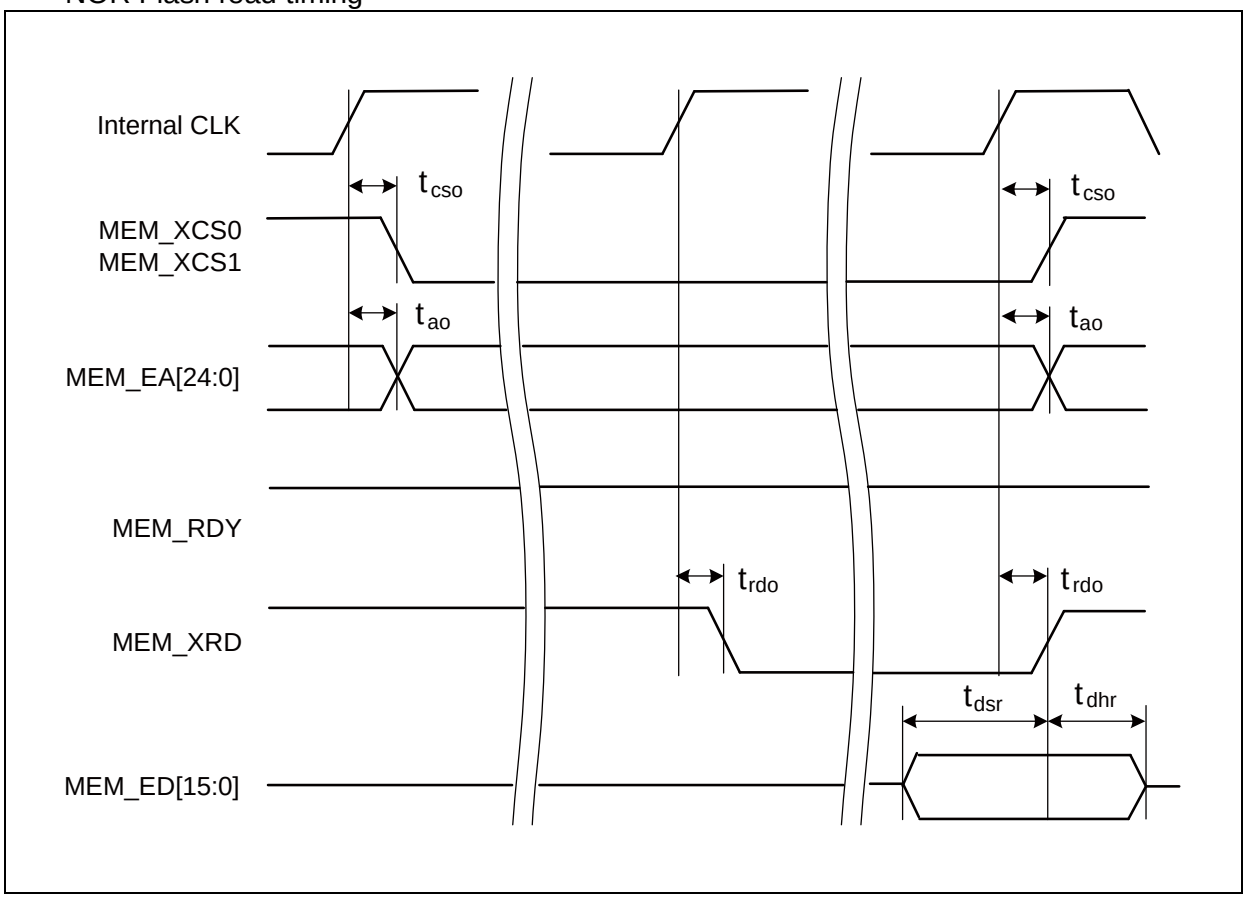
(12) Memory controller

(T_A: Recommended operating conditions, $V_{CC}3$=3.3V ± 10%, V_{SS}=AV_{SS}=0.0V)

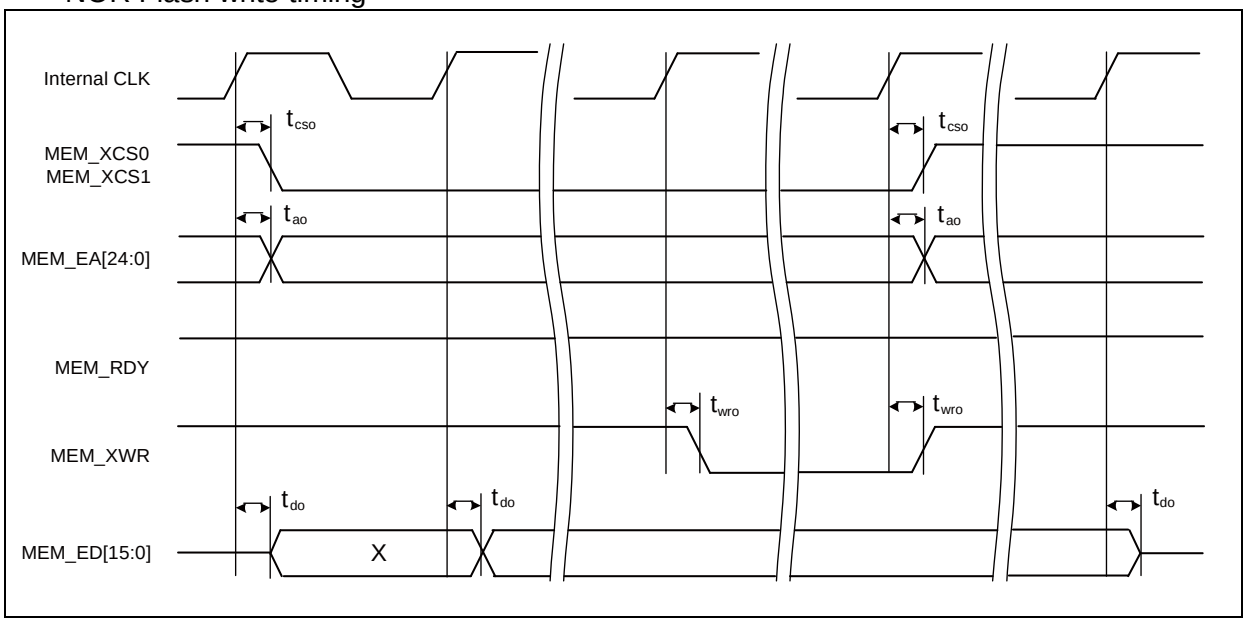
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Chip Select delay time	t_{cso}	MEM_XCS0 MEM_XCS1	–	–	18	ns	
Address delay time	t_{ao}	MEM_EA[24:0]		–	18	ns	
Data output delay time	t_{do}	MEM_ED[15:0]		–	18	ns	
Data output → HiZ time	t_{doz}			–	18	ns	
NOR Flash data setup time	t_{dsr}			20	–	ns	
NOR Flash data hold time	t_{dhr}			0	–	ns	
NOR Flash page Read data setup time	t_{dsp}			20	–	ns	
NOR Flash page Read data hold time	t_{dhp}			0	–	ns	
XRD delay time	t_{rdo}	MEM_XRD		–	18	ns	
XWR delay time	t_{wro}	MEM_XWR		–	18	ns	

Output delay is reference clock is an internal clock. The reference clock of MEM_RDY is an internal clock.

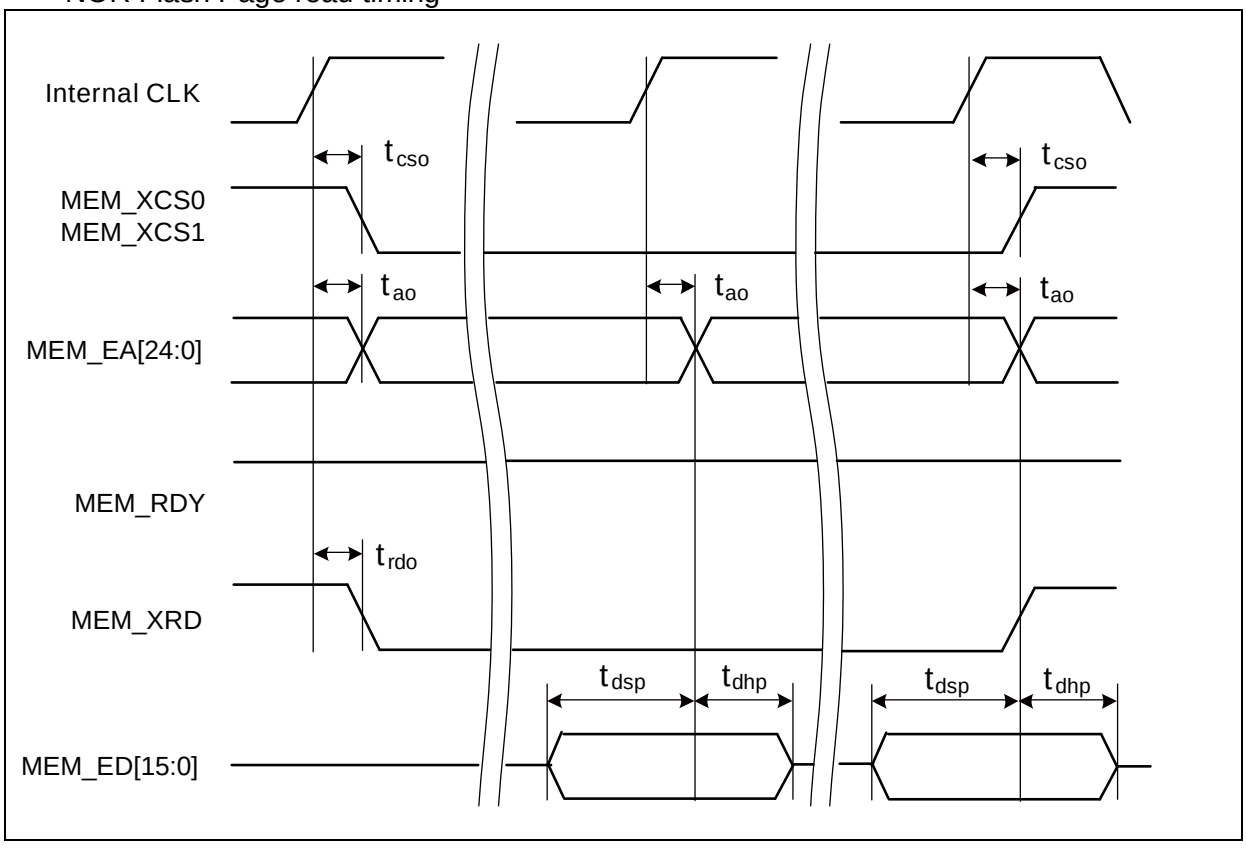
・NOR Flash read timing



・NOR Flash write timing



・NOR Flash Page read timing



(13) GDC display signal

(13-1) Clock

AC timing of video interface clock signal

(T_A: Recommended operating conditions, $V_{CC}3$=3.3V ± 10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
DCLKI frequency	Fdclki0	DCLKI	–	54	MHz	
DCLKI "H"width	Thdclki0		18	–	ns	
DCLKI "L"width	Tldclki0		18	–	ns	
DCLK frequency	Tldclk0	DCLK (internal)	–	54	MHz	*1
DCLKO frequency	Fdclko0	DCLKO	–	54	MHz	*2

*1: The internal display clock of PLL synchronous mode is generated with internal PLL of display clock prescaler.

*2: DCLKI or PLL internal display clock is output.

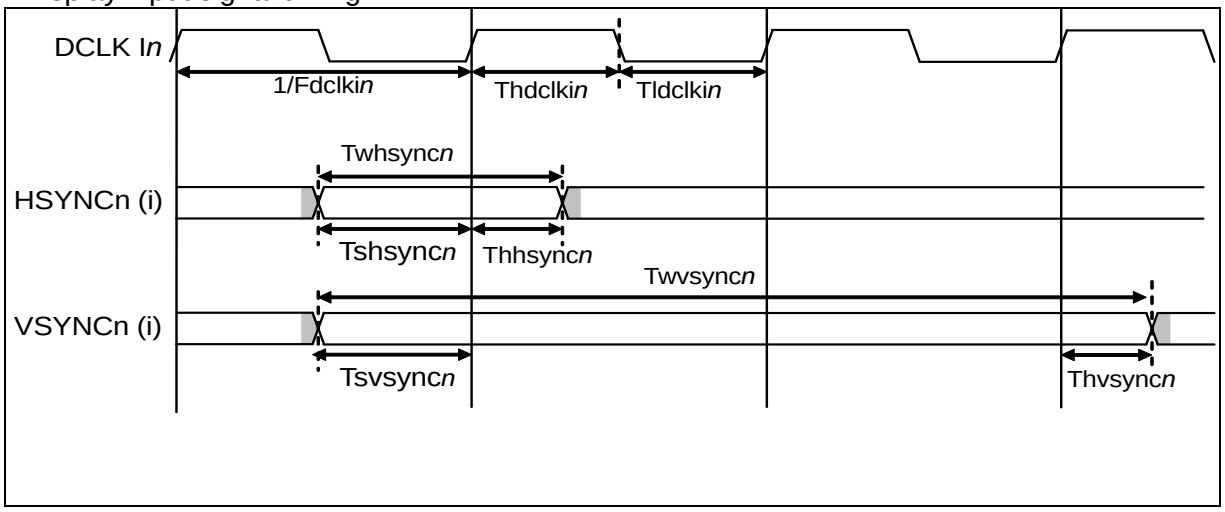
Apply only DCLKI synchronous mode. (reference clock= DCLKI)

・AC timing of video interface input signal

(T_A: Recommended operating conditions, $V_{CC}3$=3.3V ± 10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
HSYNC input setup time	Tshsync0	HSYNC(i)	4	–	–	ns	
HSYNC input hold time	Thhsync0		1	–	–	ns	
VSYNC input pulse width	Twvsync0	VSYNC(i)	1	–	–	HSYNC	

・Display input signal timing



(13-2) AC Characteristics of Display Output Signal

・Clock Mode

There are multiple clock modes for display output clocks, as shown in Table 1. The AC timing parameters vary depending on modes. The AC timing parameters are specified for each mode.

Table 1 Clock Mode for Display Output

Setting register bit field				Clock mode name
DCM1	DCM3			
CKS	DCKed	DCKD	DCKinv	
0	0	0	0	Built-in PLL standard mode
0	0	0	1	Built-in PLL reverse edge mode
0	1	0	0	Cannot be used.
0	1	0	1	
0	0	Other than 0	0	Built-in PLL delay mode
0	0	Other than 0	1	Built-in PLL reverse edge and delay mode
0	1	Other than 0	0	Built-in PLL both edge and delay mode
0	1	Other than 0	1	
1	0	0	0	DCLKI input standard mode
1	0	0	1	DCLKI input reverse edge mode
1	1	0	0	Cannot be used.
1	1	0	1	
1	0	Other than 0	0	
1	0	Other than 0	1	
1	1	Other than 0	0	
1	1	Other than 0	1	

・AC Timing Parameters

This section describes parameters used for AC timing specifications. Select whether you use the DCLKO reverse edge mode, depending on the use/non-use of delay mode.

When the delay mode is not used:
Use the DCLKO reverse edge mode when the external display device (TFT) receives the signal at the rising edge of DCLKO.
Use the DCLKO standard mode when the external display device (TFT) receives the signal at the falling edge of DCLKO.

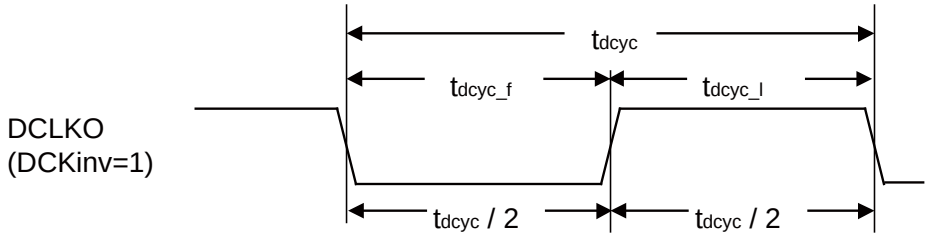
When the delay mode is used:
Use the DCLKO standard mode when the external display device (TFT) receives the signal at the rising edge of DCLKO.
Use the DCLKO reverse edge mode when the external display device (TFT) receives the signal at the falling edge of DCLKO.

Note: Clock duty ratio when the clock frequency division ratio is even or odd

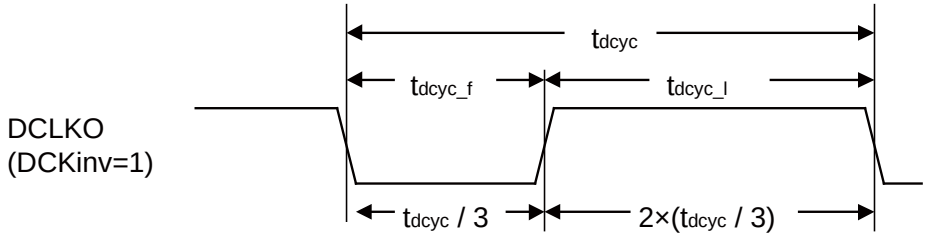
AC specifications use the half-cycle of the display output clock DCLKO as a parameter. In AC specifications, the first half-cycle is indicated as t_{dcyc_f}, and the second half-cycle is indicated as t_{dcyc_l}. Note that clock duty ratio will not be 50%:50% when the clock frequency division ratio (specified in SC field of DCM1 register) is odd. If the clock frequency division ratio is odd, the first half-cycle t_{dcyc_f} becomes different from the second half-cycle t_{dcyc_l}.

Figure 1 Clock duty ratio when the clock frequency division ratio is even or odd

・When the frequency division ratio is even



・Example: When the frequency division ratio is odd (frequency division ratio = 3)

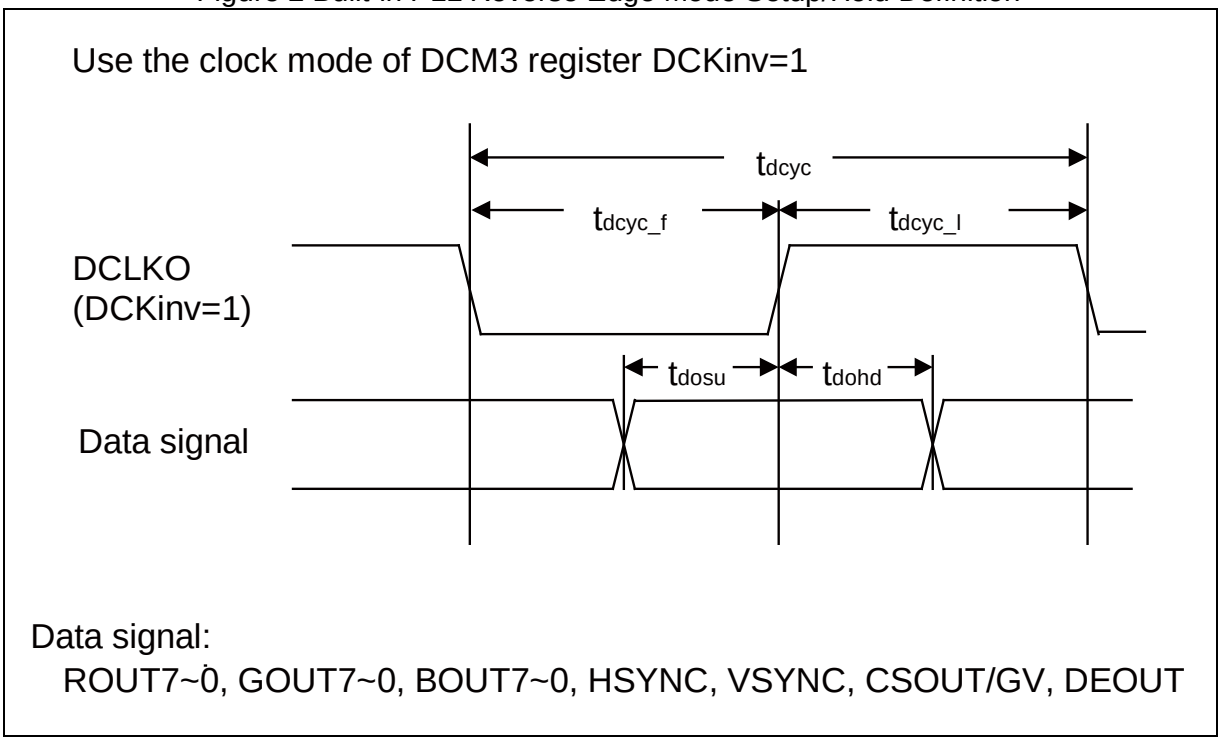


When the clock frequency division ratio is 5, t_{dcyc_f} : t_{dcyc_l} will be 2:3.

Built-in PLL reverse edge mode (DCM3.DCKinv=1)

Figure 2 shows the setup/hold definition when the external display device receives the signal at the rising edge of DCLKO.

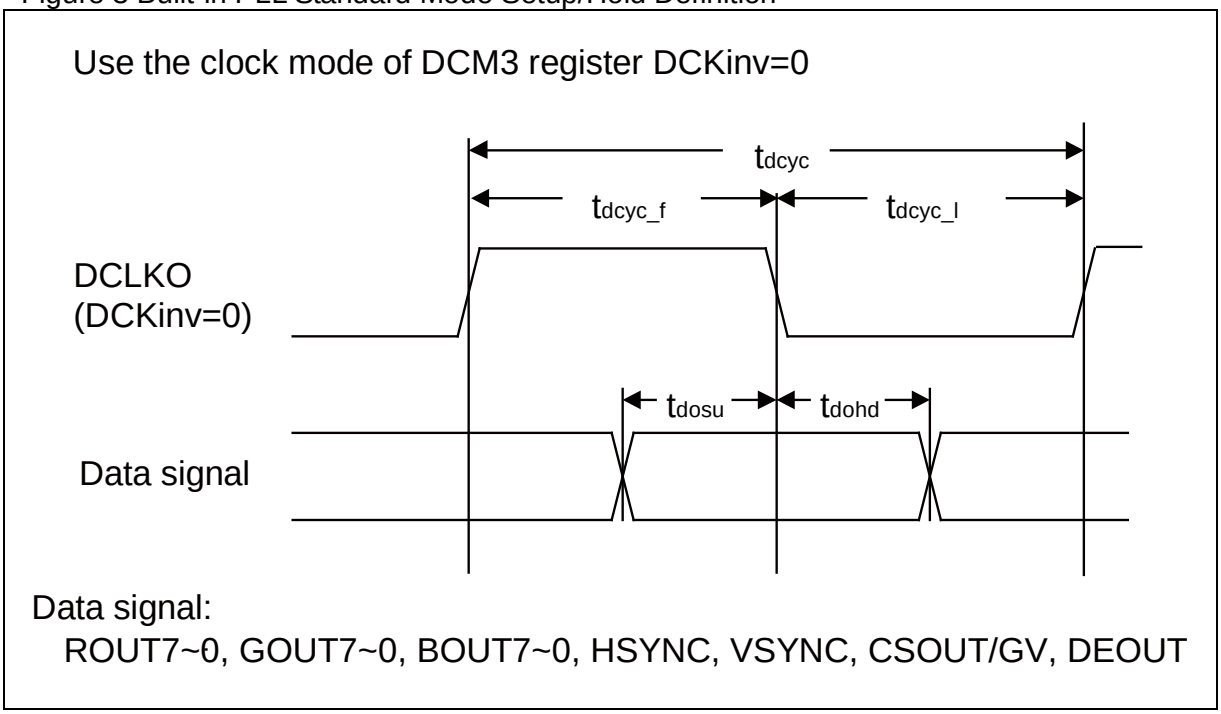
Figure 2 Built-in PLL Reverse Edge Mode Setup/Hold Definition



Built-in PLL standard mode (DCM3.DCKinv=0)

Figure 3 shows the setup/hold definition when the external display device receives the signal at the falling edge of DCLKO.

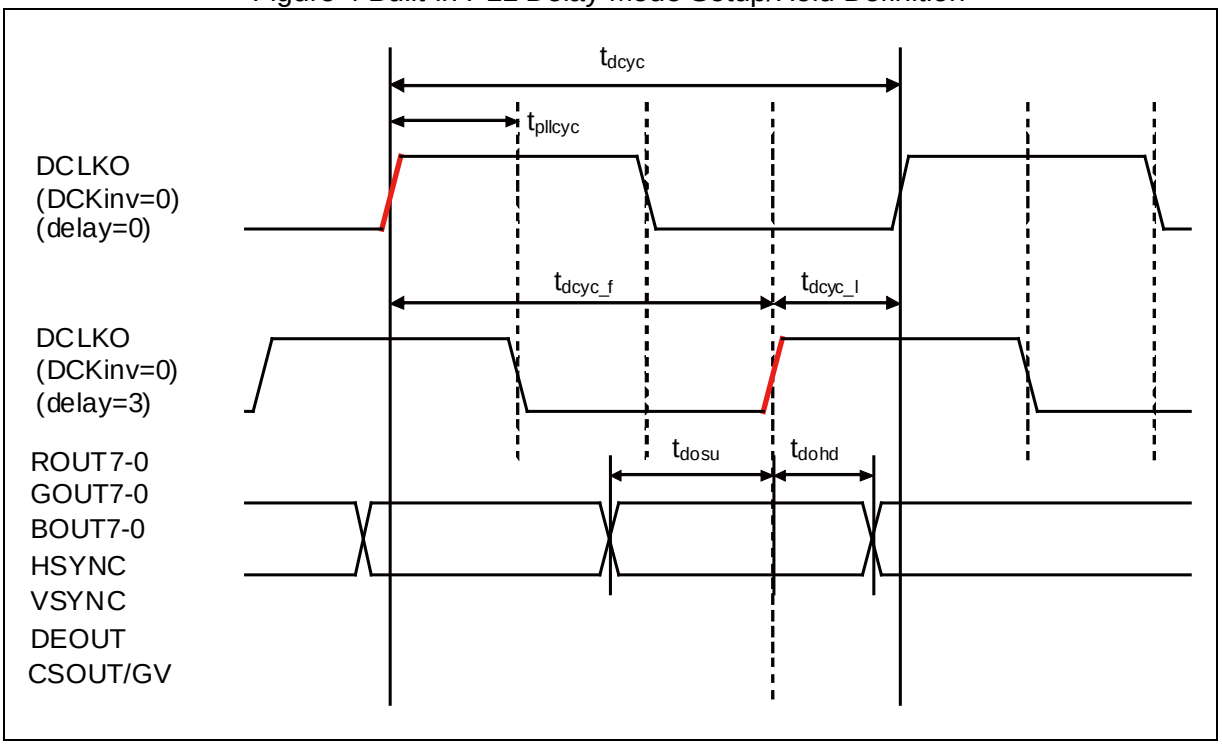
・Figure 3 Built-in PLL Standard Mode Setup/Hold Definition



Built-in PLL delay mode (DCM3.DCKinv=0)

Figure 4 shows the setup/hold definition when the external display device receives the signal at the rising edge of DCLKO. (Example: When frequency division ratio = 4)

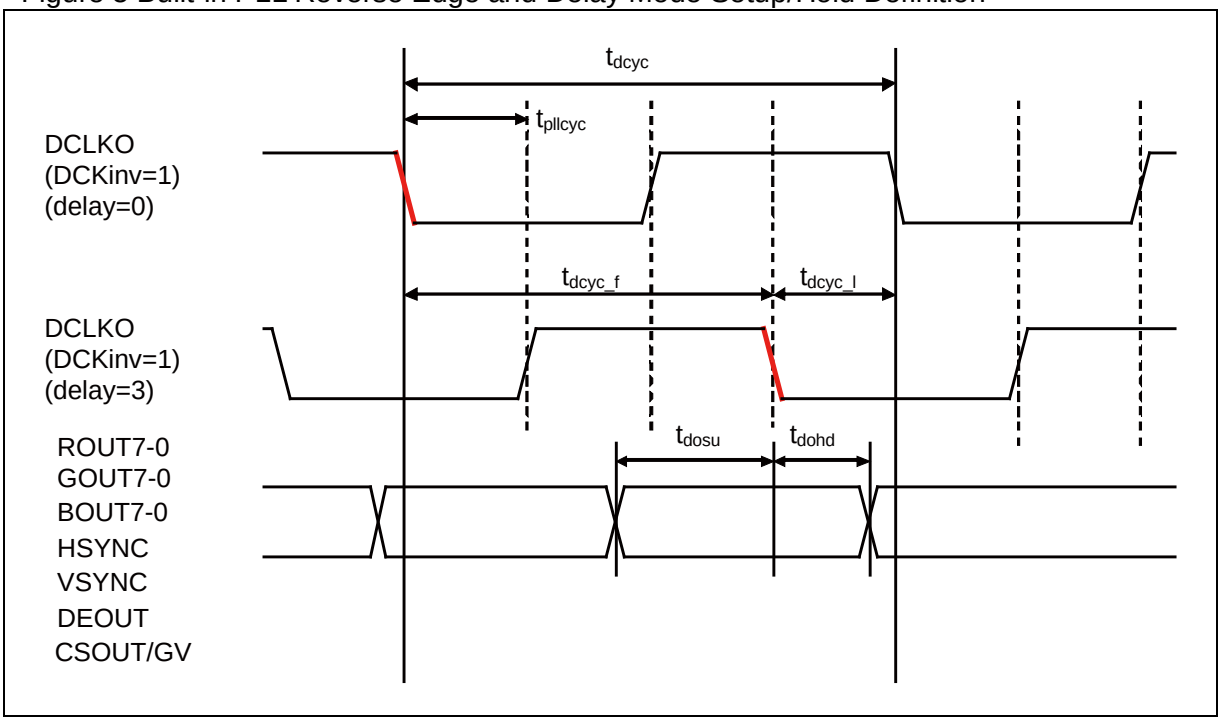
Figure 4 Built-in PLL Delay Mode Setup/Hold Definition



Built-in PLL reverse edge and delay mode (DCM3.DCKinv=1)

Figure 5 shows the setup/hold definition when the external display device receives the signal at the falling edge of DCLKO. (Example: When frequency division ratio = 4)

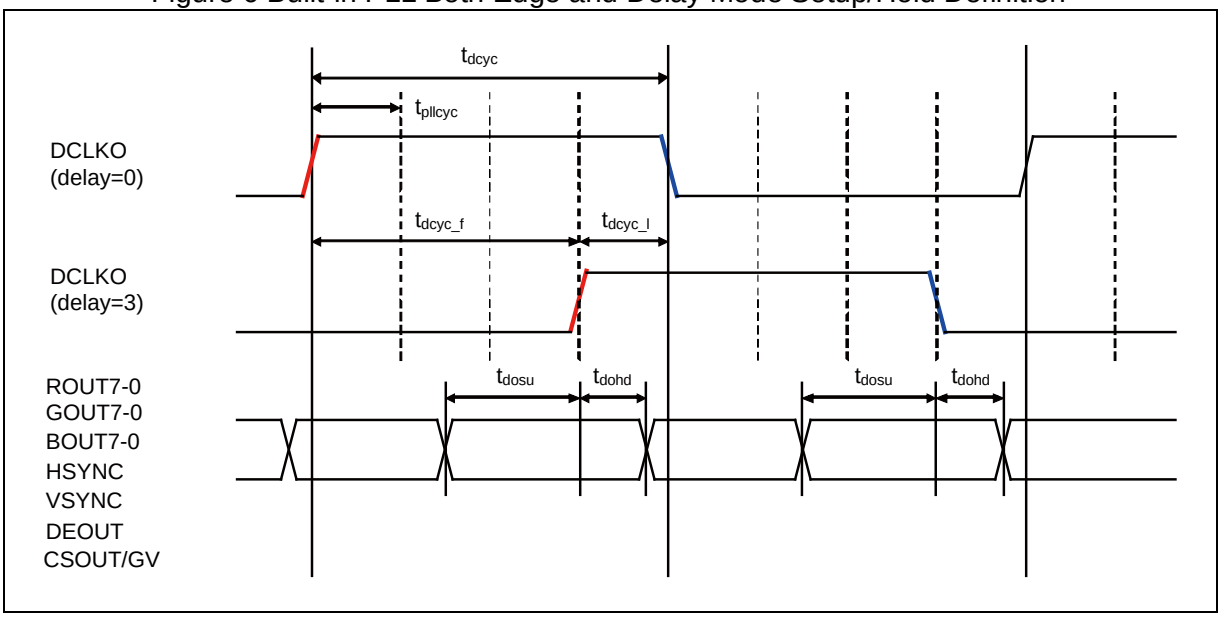
・Figure 5 Built-in PLL Reverse Edge and Delay Mode Setup/Hold Definition



Built-in PLL both edge and delay mode (DCM3.DCKinv=0)

Figure 6 shows the setup/hold definition when the external display device (TFT) receives the signal both at the rising edge and the falling edge of DCLKO. (Example: When frequency division ratio = 4)
Although there are two sampling locations in both edge mode; one at the rising edge and the other at the falling edge, the values of setup/hold definition are same.

Figure 6 Built-in PLL Both Edge and Delay Mode Setup/Hold Definition



Setup/Hold Definition in Delay Mode

The delay mode is a mode realized with DCLKO delay function, and it can provide delay to DCLKO signal output itself. This can be used when both the following conditions are satisfied.

- The internal PLL is used to generate DCLKO (CKS field of DCM register = 0)
- The frequency division ratio to the internal PLL of DCLKO is 2 or more (SC field of DCM register > 0)

The delay value is set as the unit for internal PLL clock by DCKD field of DCM3 register. The meanings of DCKD setting value are shown below.

When the internal PLL frequency division ratio = 2

DCKD	Delay
000000	No additional delay
000100	+1 PLL clock

When the internal PLL frequency division ratio > 2

DCKD	Delay
000000	No additional delay
000010	+2 PLL clock
000100	+3 PLL clock
000110	+4 PLL clock
:	:
111110	+17 PLL clock

In delay mode, t_{dcyc_f} and t_{dcyc_l} are defined by the delay value above (e.g. "2" of "+2 PLL clock") as shown below.

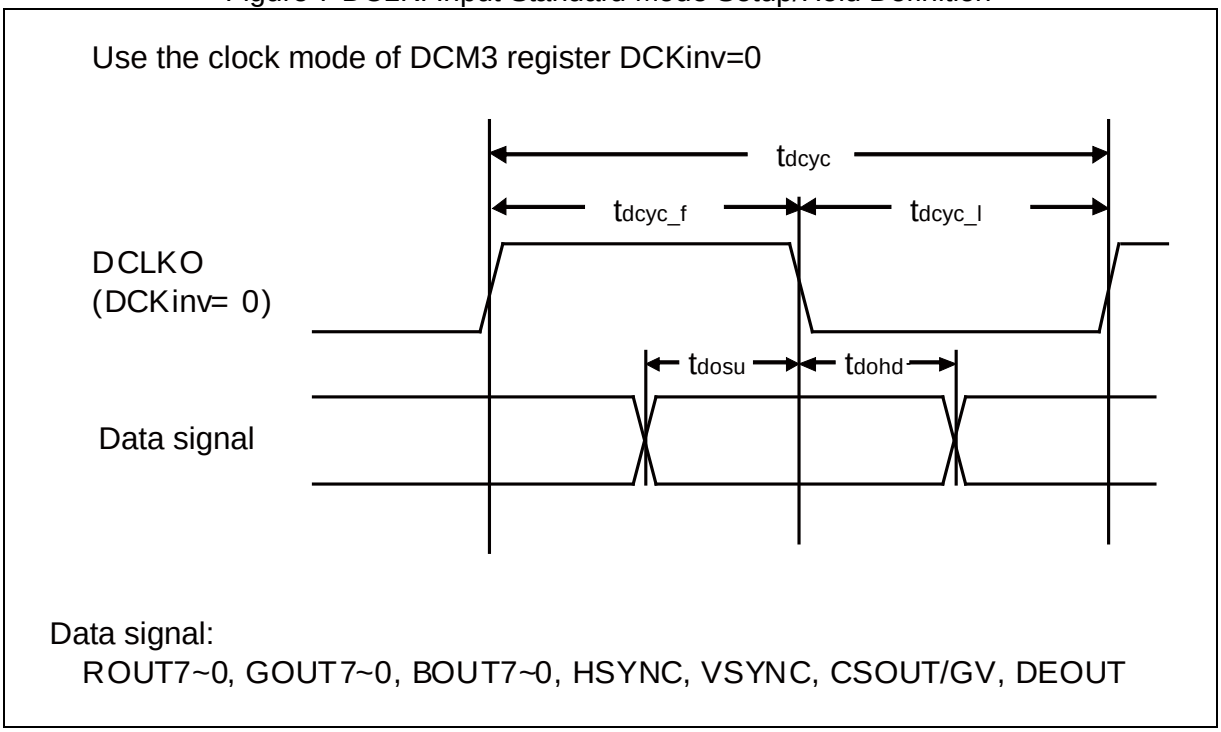
t_{dcyc_f} = Delay value × t_{pllcyc}

$t_{dcyc\_l} = t_{dcyc} - t_{dcyc\_f}$

DCLKI Input Standard Mode (DCM3.DCKinv=0)

Figure 7 shows the setup/hold definition when the external display device (TFT) receives the signal at the falling edge of DCLKO.

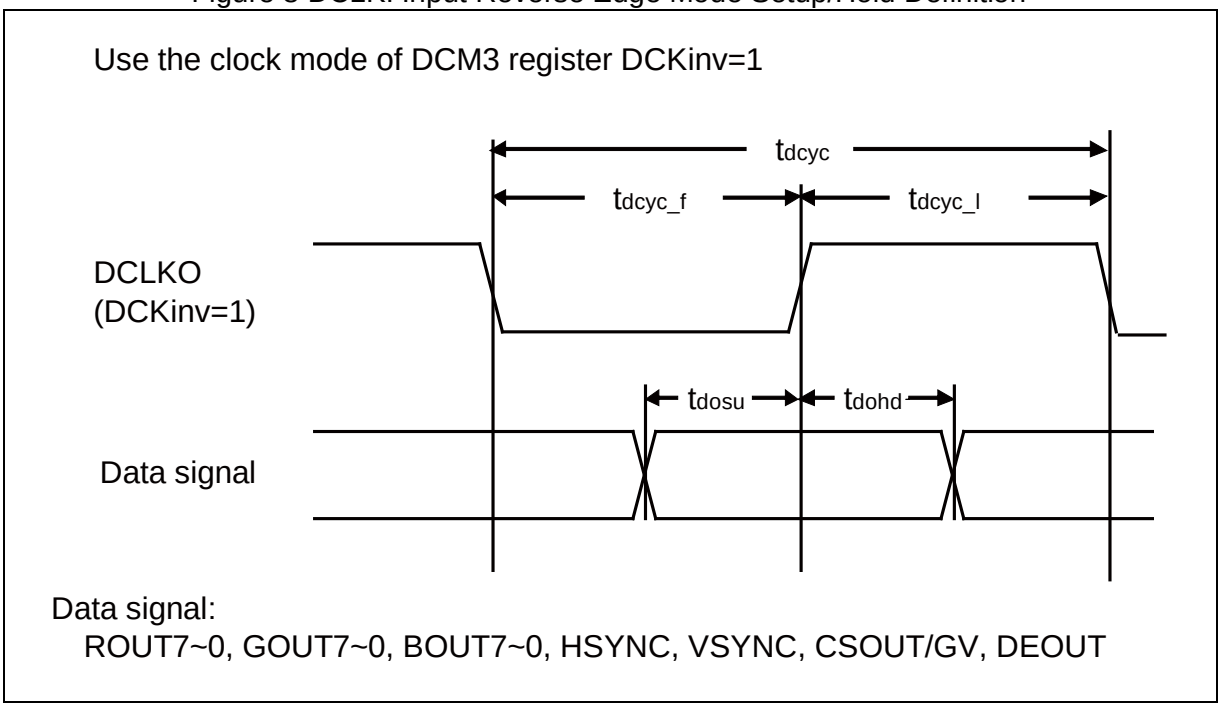
Figure 7 DCLKI Input Standard Mode Setup/Hold Definition



DCLKI Input Reverse Edge Mode (DCM3.DCKinv=1)

Figure 8 shows the setup/hold definition when the external display device (TFT) receives the signal at the rising edge of DCLKO.

Figure 8 DCLKI Input Reverse Edge Mode Setup/Hold Definition



・AC Timing Specifications

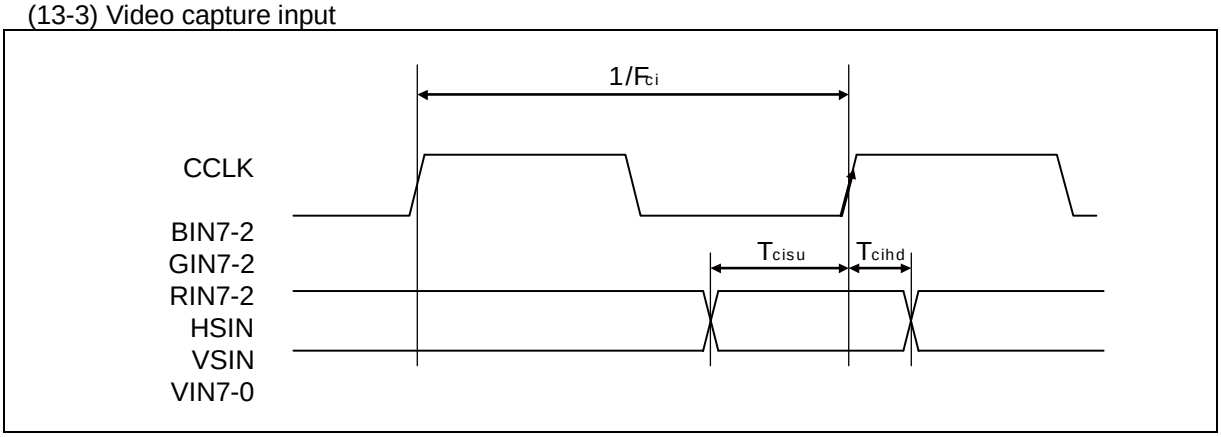
Parameter	Symbol	min.
Display clock cycle time	t_{dcyc}	18.5 ns

External load condition 50 pF

Parameter	Symbol	DCLKO Reference edge	IO drive capability setting	
			10 mA	2 mA
Setup time	t_{dosu}	neg, pos *	t_{dcyc_f} - 8.5ns	t_{dcyc_f} - 10.2ns
Hold time	t_{dohd}		t_{dcyc_l} - 1.7ns	t_{dcyc_l} - 3.3ns

*: DCLKO reference edge: This is the reference clock edge for setup time and hold time.
Pos = The external display device receives the signal at the rising edge of DCLKO.
Neg = The external display device receives the signal at the falling edge of DCLKO.

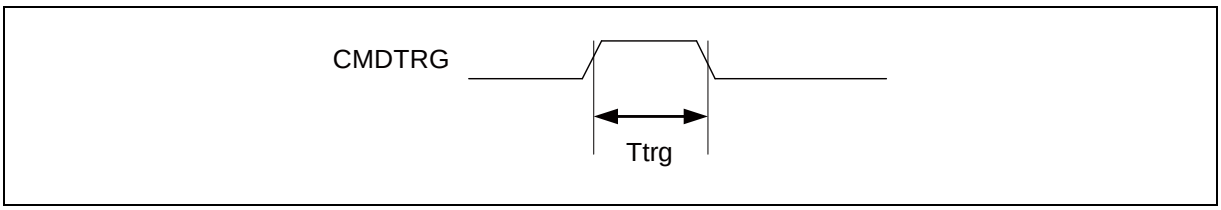
(13-3) Video capture input



Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
Capture input frequency	Fci	CCLK	–	81.0	MHz	
Capture input setup time	Tcisu	BIN7-2, GIN7-2, RIN7-2, HSIN, VSIN, VIN7-0	3.0	–	ns	
Capture input hold time	Tcihd		0.0	–	ns	

(14) GDC command trigger signal

Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
Input trigger pulse width	Ttrg	CMDTRG	160	–	ns	



5. A/D Converter

(1) Electrical Characteristics

(T_A: Recommended operating conditions, $V_{CC}5=AV_{CC}5=5.0V \pm 10\%$, $V_{SS}=AV_{SS}=0.0V$)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	–	–	–	–	10	bit	
Total error	–	–	–	–	±3	LSB	
Non linearity error	–	–	–	–	±2.5	LSB	
Differential linearity error	–	–	–	–	±1.9	LSB	
Zero transition voltage	V_{OT}	AN0 to AN31	AV_{SS}-1.5LSB	–	AV_{SS}+2.5LSB	V	1LSB=(AV_{CC}-AV_{SS}) / 1024
Full-scale transition voltage	V_{FST}	AN0 to AN31	AVRH5-3.5LSB	–	AVRH5+0.5LSB	V	
Sampling time	t_{SMP}	–	1.2	–	–	µs	*1
Compare time	t_{CMP}	–	1.8	–	–	µs	*1
A/D conversion time	t_{CNV}	–	3.0	–	–	µs	*1
Analog port input current	I_{AIN}	AN0 to AN31	-5	–	+5	µA	$V_{AVSS} \leq V_{AIN} \leq V_{AVCC}$
Analog input voltage	V_{AIN}	AN0 to AN31	AV_{SS}	–	AVRH5	V	
Reference voltage	AVRH	AVRH5	4.5	–	5.5	V	AVRH5 ≤ AV_{CC}5
	AVRL	AVSS	–	0.0	–	V	
Power supply current	I_A	AVCC	–	–	4.0	mA	
	I_{AH}		–	–	6.0	µA	*2
	I_R	AVRH5	–	600	900	µA	
	I_{RH}		–	–	5	µA	*2
Variation between channels	–	AN0 to AN31	–	–	4	LSB	

*1: Time for each channel.

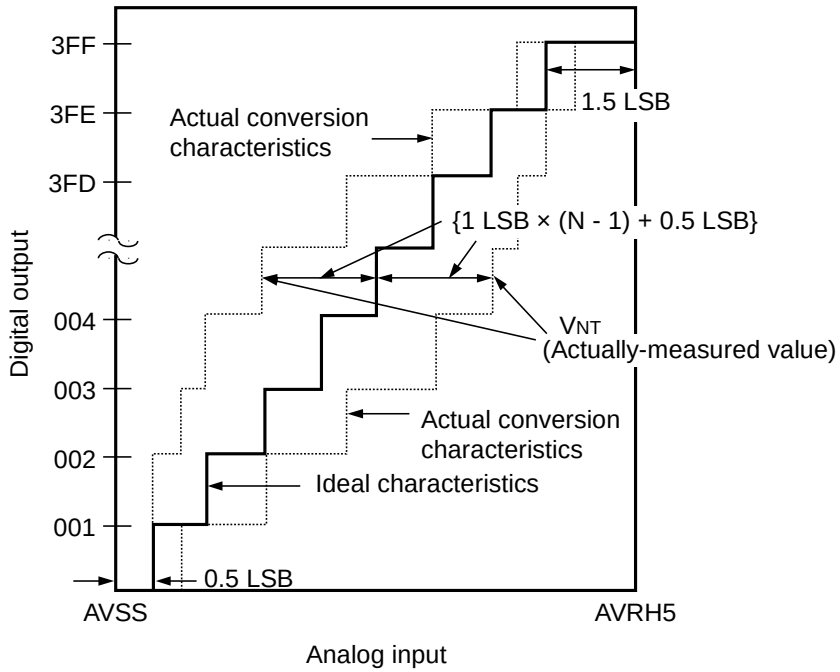
*2: Power supply current (V_{CC} = AV_{CC} = 5.0 V) is specified if A/D converter is not operating and CPU is stopped.

Note: Be sure to use the clock with a frequency between 8MHz and 17MHz for the ADC compare clock in order to ensure its accuracy.

(2) Definition of A/D Converter Terms

Resolution	: Analog variation that is recognized by an A/D converter.
Non linearity error	: Deviation of the actual conversion characteristics from a straight line that connects the zero transition point ("00 0000 0000"← →"00 0000 0001") to the full-scale transition point ("111111 1110" ← →"11 1111 1111").
Differential linearity error	: Deviation of the input voltage from the ideal value that is required to change the output code by LSB.
Total error	: Difference between the actual value and the theoretical value. The total error includes zero transition error, full-scale transition error, and non linearity error.

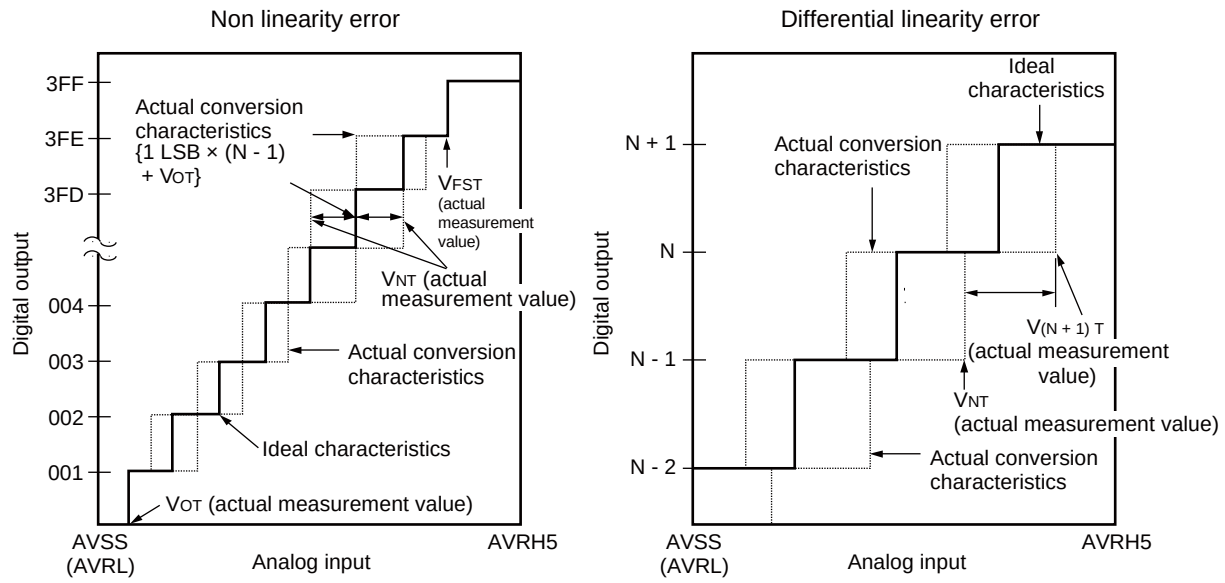
Total error



$$\text{Total error of digital output N} = \frac{V_{NT} - \{1LSB\} \times (N - 1) + 0.5LSB\}}{1LSB} \text{ [LSB]}$$

$$1LSB \text{ (Ideal value)} = \frac{AVRH5 - AVSS}{1024} \text{ [V]}$$

N: A/D converter digital output value.
V_{OT} (Ideal value) = AVSS + 0.5 LSB[V]
V_{FST} (Ideal value) = AVRH5 - 1.5 LSB[V]
V_{NT}: Voltage at which the digital output changes from (N - 1) to N.



$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1LSB\} \times (N - 1) + V_{OT}}{1LSB} \text{ [LSB]}$$

$$\text{Differential linearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1 \text{ [LSB]}$$

$$1LSB = \frac{V_{FST} - V_{OT}}{1022} \text{ [V]}$$

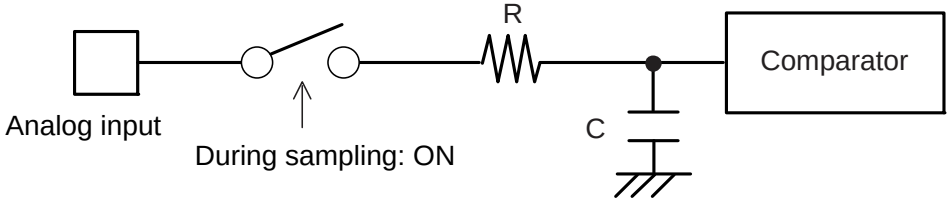
V_{OT} : Voltage at which the digital output changes from "000_H" to "001_H".
V_{FST} : Voltage at which the digital output changes from "$3FE_H$" to "$3FF_H$".

(3) Notes on Using A/D Converter

<About the output impedance of the analog input of external circuit>

· External impedance values of the external input of 4.2 kΩ or lower (sampling time = 1.2 µs@ machine clock of 16 MHz) are recommended. When the external impedance is too high, the sampling time for analog voltages may not be sufficient. In this case, it is recommended to connect the capacitor (approx. 0.1 µF) to the analog input pin.

• Analog input circuit model



	R	C
MB91590series	4.0kΩ (Max)	16.1pF (Max)

Note: Listed values must be considered as reference values.

6. Flash memory

(1) Electrical Characteristics

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time	–	200	800	ms	8 Kbyte sector*1, excluding internal preprogramming time
	–	300	1100	ms	8 Kbyte sector*1, including internal preprogramming time
	–	400	2000	ms	64 Kbyte sector*1, excluding internal preprogramming time
	–	700	3700	ms	64 Kbyte sector*1, including internal preprogramming time
8-bit writing time	–	9	288	µs	Exclusive of overhead time at system level*1
16-bit writing time	–	12	384	µs	Exclusive of overhead time at system level*1
ECC writing time	–	9	288	µs	Exclusive of overhead time at system level*1
Erase cycle*2/ Data retain time	1,000 cycles/ 20 years, 10,000 cycles/ 10 years, 100,000 cycles/ 5 years	–	–	–	Temperature at writing/erasing Tj<+105°C, Average T_A=+85°C*3

*1: The guaranteed value for erasure up to 100,000 cycles.
*2: Number of erase cycles for each sector.
*3: This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at + 85°C).

(2) Notes

While the Flash memory is written, shutdown of the external power (Vcc5) is prohibited.
In the application system where Vcc5 might be shut down while writing, be sure to turn the power off by using an external voltage detector.

To put it concretely, after the external power supply voltage falls below the detection voltage (V_{DL}*1), hold Vcc5 at 2.7V or more within the duration calculated by the following expression:

Td*1[µs] + (period of PCLK [µs] x 257) + 50 [µs]

*1: See “4.AC Characteristics (9) Low-voltage detection (External low-voltage detection) ”

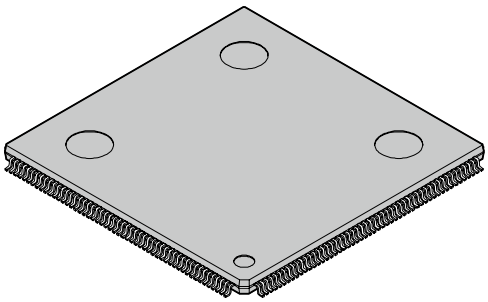
■ ORDERING INFORMATION

Part number	Package
MB91F591BPMC-GSE1	208-pin plastic LQFP (FPT-208P-M06)
MB91F591BSPMC-GSE1	
MB91F591BHPMC-GSE1	
MB91F591BHSPMC-GSE1	
MB91F592BPMC-GSE1	
MB91F592BSPMC-GSE1	
MB91F592BHPMC-GSE1	
MB91F592BHSPMC-GSE1	
MB91F594BPMC-GSE1	
MB91F594BSPMC-GSE1	
MB91F594BHPMC-GSE1	
MB91F594BHSPMC-GSE1	

■ PACKAGE DIMENSIONS

● Dimension of LQFP-208(FPT-208P-M06)

208-pin plastic LQFP

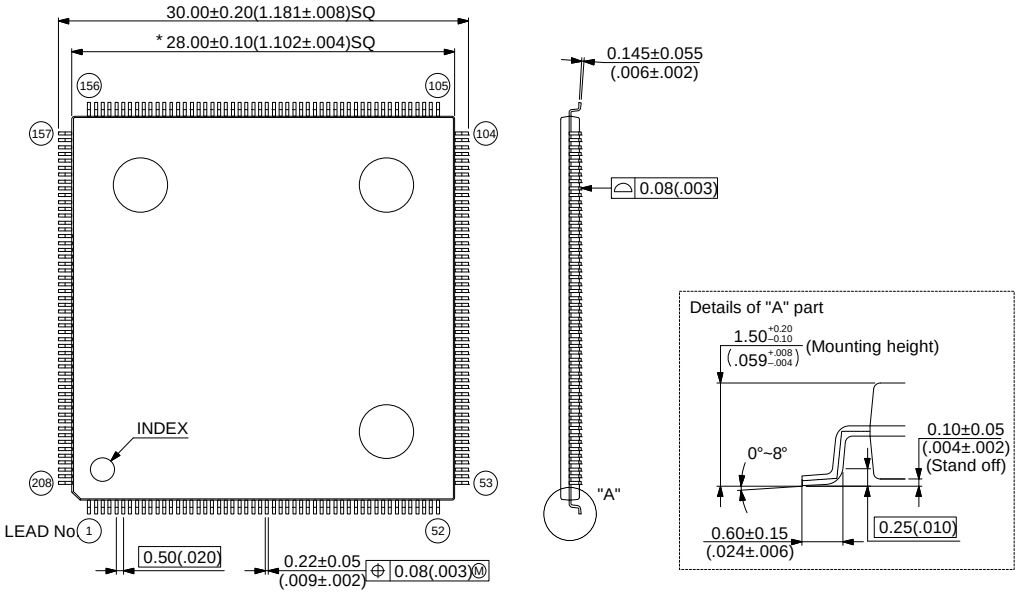


(FPT-208P-M06)

Lead pitch	0.50 mm
Package width × package length	28.0 × 28.0 mm
Lead shape	Gullwing
Sealing method	Plastic mold
Mounting height	1.70 mm MAX
Weight	2.55 g
Code (Reference)	P-LFQFP208-28×28-0.50

208-pin plastic LQFP
(FPT-208P-M06)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.

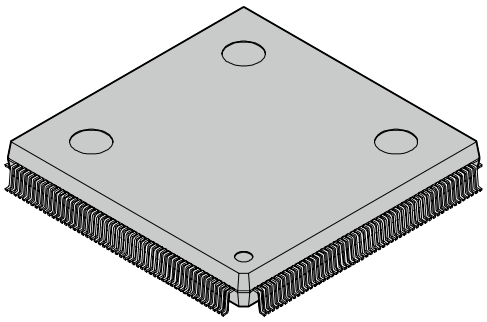


Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

● Dimension of HQFP-208(FPT-208P-M04)(Under consideration)

208-pin plastic QFP

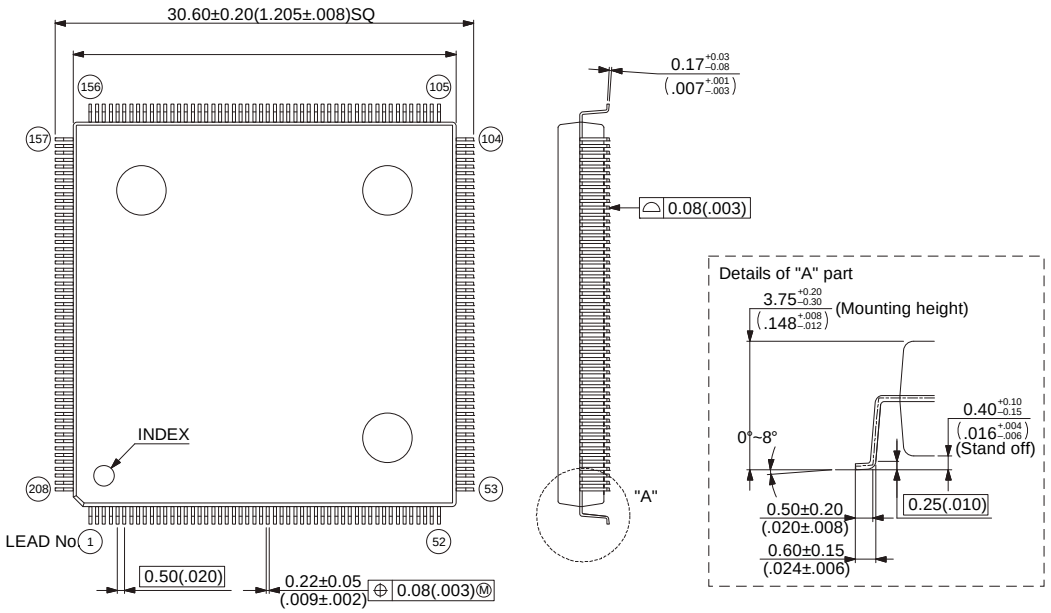


(FPT-208P-M04)

Lead pitch	0.50 mm
Package width × package length	28.0 mm × 28.0 mm
Lead shape	Gullwing
Sealing method	Plastic mold
Mounting height	3.95 mm MAX
Weight	5.71g
Remark	Low heat resistance type

208-pin plastic QFP
(FPT-208P-M04)

Note 1) * : These dimensions do not include resin protrusion
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

■ MAJOR CHANGES IN THIS EDITION

Page	Section	Page Change Results (See this data sheet for the detail.)
-	-	Contact the sales representative for the detail of changed parts.

MEMO

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