

# 32-Bit Microcontroller

CMOS

## FR30 Series

### MB91F127/F128

#### ■ DESCRIPTION

This model, designed on the basis of 32-bit RISC CPU (FR30 series), is a standard single-chip micro controller with built-in I/O resources and bus control functions. The functions are suitable for built-in control that requires high-speed CPU processing.

MB91F127 includes 256 Kbytes built-in flash memory and 14 Kbytes built-in RAM. MB91F128 includes 510 Kbytes built-in flash memory and 14 Kbytes built-in RAM.

The specifications of the devices are best suited for applications requiring high-level CPU processing capabilities, such as navigation system, high-performance FAX, and printer controller.

#### ■ FEATURES

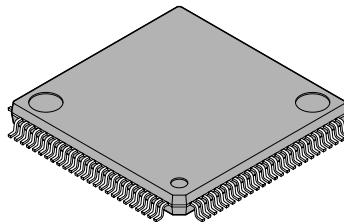
##### FR-CPU

- 32-bit RISC (FR30), load/store architecture, 5-step pipeline
- Operating frequency : Internal 25 MHz
- General register : 32bit x 16 registers
- 16-bit fixed-length instructions (primitives), 1 instruction/1 cycle
- Instructions of memory-to-memory transfer, bit processing, and barrel shift : Instructions suitable for built-in control

*(Continued)*

#### ■ PACKAGE

100 pin, Plastic LQFP



(FPT-100P-M05)

# MB91F127/F128

- Function entry/exit instructions, multi load/store instruction for register data : High-level language compatible instructions
- Register interlock functions : Simple description of assembler language
- Branch instructions with delay slot : Reduced overhead on branching process
- Built-in multiplier/ Supporting at instruction level
  - Signed 32-bit multiplying : 5 cycles
  - Signed 16-bit multiplying : 3 cycles
- Interrupt (saving PC and PS) : 6 cycles, 16 priority levels

## Bus interface

- Maximum of 25 MHz internal operation rate
- 25-bit address bus (32 MB space)
- 16-bit address output, 8/16-bit data input/output
- Basic bus cycle : 2-clock cycle
- Chip selection outputs specifiable in a minimum of 64 Kbytes steps : 6 outputs
- Automatic wait cycle : Specifiable flexibly from 0 cycle to 7 cycles for each area
- Supporting time-division input/output interface for address/data (for area 1 only)
- Unassigned data/address terminals are available as input/output ports
- Supporting little endian mode (selecting one area from area 1 to area 5)

## DMAC (DMA controller)

- 8 channels
- Transfer factor : Interrupt request of built-in resources
- Transfer sequence : Step transfer/Block transfer/Burst transfer/Consecutive transfer
- Transfer data length : Selectable among 8 bits, 16 bits, and 32 bits
- Pausing is allowed by interrupt request

## UART

- 3 channels
- Full-duplex double buffer
- Data length : 7 to 9 bits (no parity), 6 to 8 bits (with parity)
- Asynchronous (start-stop synchronization) or CLK synchronous communication is selectable
- Multi processor mode
- Built-in 16-bit timer (U-Timer) used as a baud-rate generator : Generates an arbitrary baud rate
- External clock is available as a transfer clock
- Error detection : parity, frame, and overrun

## A/D converter (sequential transducer)

- 8/10-bit resolution, 8 channels
- Sequential comparison and transducer : At 25 MHz, 5.2  $\mu$ s
- Built-in sample and hold circuit
- Conversion mode : Selectable among single conversion, scan conversion, and repeat conversion
- Activation : Selectable among software, external trigger, and built-in timer

## Reload timer

- 16-bit timer : 3 channels
- Internal clock : 2-clock cycle resolution, selectable among 2/8/32 dividing and external clock

(Continued)

(Continued)

## Other interval timers

- 16-bit timer : 3 channels (U-Timer)
- PPG timer : 4 channels
- 16-bit OCU : 4 channels, ICU : 4 channels, Free-run timer : 1 channel
- Watchdog timer: 1 channel

## Flash memory 510 KB

- 510 KB FLASH ROM: Read/Write/Erase is allowed with a same power

## Built-in RAM 14 KB

- D-bus RAM 12 KB, C-bus RAM 2 KB

## Bit search module

- Position of a first bit that changes between "1" and "0" is searched in one cycle, within an MSB of one word.

## Interrupt controller

- External interrupt input : Normal interrupt×6 (INT0 to INT5)
- Internal interrupt factors : UART, DMAC, A/D, Reload timer, UTIMER, delay interrupt, PPG, ICU, and OCU
- Priority levels are programmable (16 levels)

## Reset factors

- Power-on reset/watchdog timer/software reset/external reset

## Low power consumption mode

- Sleep/stop mode

## Clock control

- Built-in PLL circuit, selectable among 1-multiplication, and 2-multiplication
- Gearing function : Operation clock frequencies are freely and independently specifiable for CPU and peripherals.  
Gear clocks are selectable among 1/1, 1/2, 1/4, and 1/8 (or among 1/2, 1/4, 1/8, and 1/16).  
Upper limit of peripheral operations is 25 MHz.

## Others

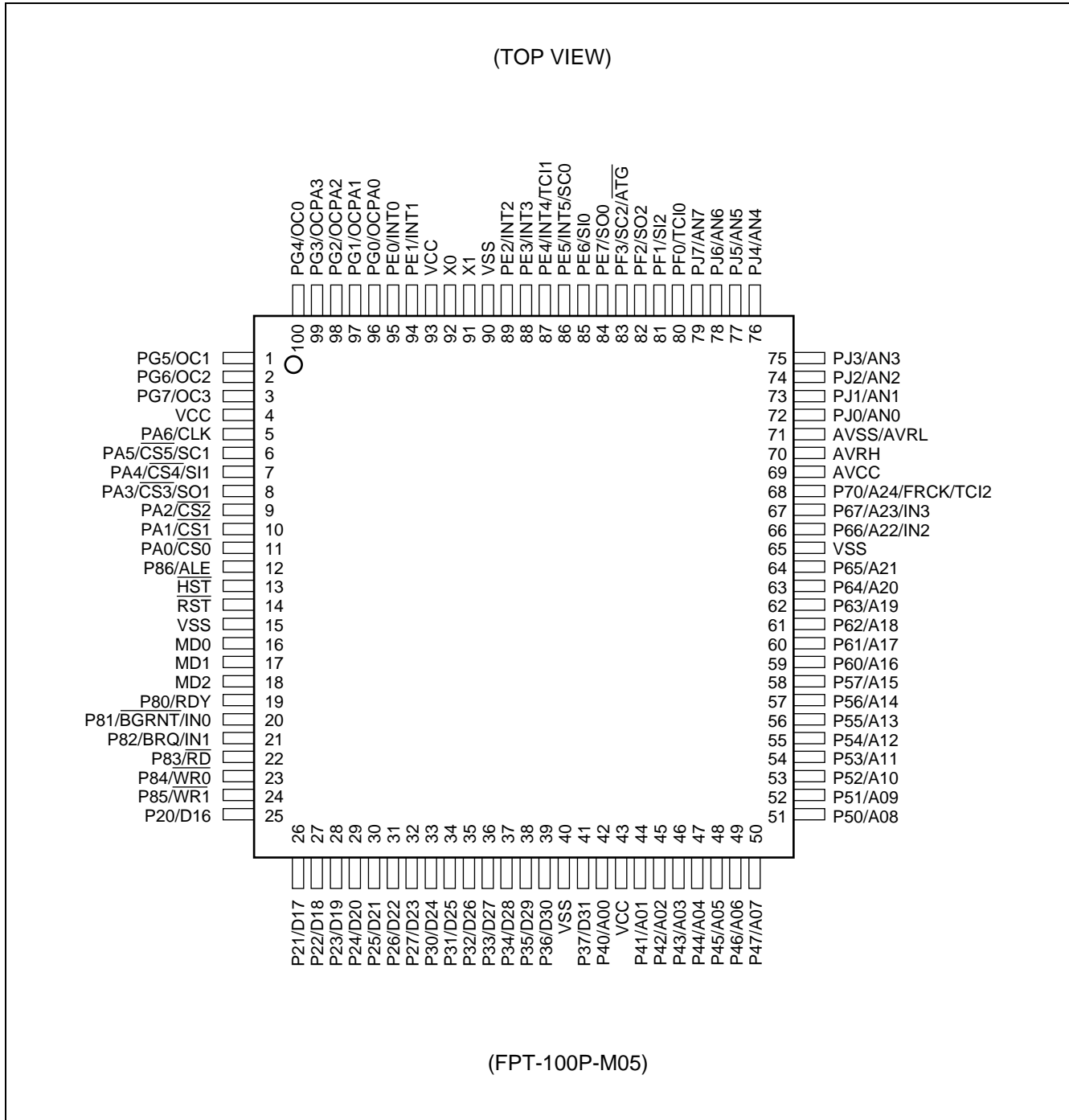
- Package : LQFP-100
- CMOS technology : 0.35 μm
- Power supply voltage : 3.3 V±0.3 V

## ■ SERIES CONFIGURATION

| Model name   | MB91F127            | MB91F128            | MB91FV129          |
|--------------|---------------------|---------------------|--------------------|
| Outline      | Quantity production | Quantity production | Evaluation product |
| FLASH memory | 256 KB              | 510 KB              | 510 KB             |
| D-bus RAM    | 12 KB               | 12 KB               | 16 KB              |
| C-bus RAM    | 2 KB                | 2 KB                | 2 KB               |

# MB91F127/F128

## ■ PIN ASSIGNMENT



## ■ PIN DESCRIPTION

Note that the numbers in the table are not pin numbers on a package.

| No.  | Pin name   | Input/output circuit type | Description   |
|--|--|---------------------------|---|
| 1<br>2<br>3<br>4<br>5<br>6<br>7<br>8   | D16/P20<br>D17/P21<br>D18/P22<br>D19/P23<br>D20/P24<br>D21/P25<br>D22/P26<br>D23/P27   | D                         | Bit 16 through bit 23 of external data bus.<br>The terminals are available as general I/O ports (P20 through P27) when external bus width is specified at 8 bits or in single-chip mode.  |
| 9<br>10<br>11<br>12<br>13<br>14<br>15<br>16  | D24/P30<br>D25/P31<br>D26/P32<br>D27/P33<br>D28/P34<br>D29/P35<br>D30/P36<br>D31/P37   | D                         | Bit 24 through bit 31 of external data bus.<br>The terminals are available as general I/O ports (P30 through P37) when the terminals are not used.  |
| 17<br>18<br>19<br>20<br>21<br>22<br>23<br>24<br>25<br>26<br>27<br>28<br>29<br>30<br>31<br>32 | A00/P40<br>A01/P41<br>A02/P42<br>A03/P43<br>A04/P44<br>A05/P45<br>A06/P46<br>A07/P47<br>A08/P50<br>A09/P51<br>A10/P52<br>A11/P53<br>A12/P54<br>A13/P55<br>A14/P56<br>A15/P57 | D                         | Bit 00 through bit 15 of external address bus.<br>The terminals are available as general I/O ports (P40 through P47 and P50 through P57) when the terminals are not used as address buses.  |
| 33<br>34<br>35<br>36<br>37<br>38<br>39<br>40   | A16/P60<br>A17/P61<br>A18/P62<br>A19/P63<br>A20/P64<br>A21/P65<br>A22/P66/IN2<br>A23/P67/IN3   | D                         | Bit 16 through bit 23 of external address bus.<br>The terminals are available as general I/O ports (P60 through P67) when the terminals are not used as address busses.<br>[IN2,IN3]: Input terminals of input capture.<br>This function is active when input capture is operating. |

(Continued)

# MB91F127/F128

| No.  | Pin name   | Input/output circuit type | Description   |                         |                         |                  |                  |            |                         |                         |                |            |                         |                |                |
|--|--|---------------------------|---|-------------------------|-------------------------|------------------|------------------|------------|-------------------------|-------------------------|----------------|------------|-------------------------|----------------|----------------|
| 41   | A24/P70/FRCK/TCI2  | D                         | Bit 24 of external address bus.<br>[P70] A24, FRCK and TCI2 are available as general input ports when they are not used.<br>[FRCK] External clock input of free-run timer. This function is active when external clock input of free-run timer is used.<br>[TCI2] External clock input of timer 2. This function is active when external clock input of timer 2 is used.  |                         |                         |                  |                  |            |                         |                         |                |            |                         |                |                |
| 42   | RDY/P80  | D                         | External ready input. Enter "0" when bus cycle under execution does not complete. This terminal is available as general input/output port when it is not used.  |                         |                         |                  |                  |            |                         |                         |                |            |                         |                |                |
| 43   | $\overline{\text{BGRNT}}$ /P81/IN0   | D                         | External bus open receive output. This terminal outputs "L" when an external bus is released. This terminal is available as general input/output port when it is not used.<br>[IN0] Input capture input.<br>This function is active when input capture is under input operation.  |                         |                         |                  |                  |            |                         |                         |                |            |                         |                |                |
| 44   | BRQ/P82/IN1  | D                         | External bus open request input. Enter "1" when releasing external bus. This terminal is available as general input/output port when it is not used.<br>[IN1] Input capture input.<br>This function is active when input capture is under input operation.  |                         |                         |                  |                  |            |                         |                         |                |            |                         |                |                |
| 45   | $\overline{\text{RD}}$ /P83  | D                         | External bus read strobe.<br>This terminal is available as general input/output port when it is not used.   |                         |                         |                  |                  |            |                         |                         |                |            |                         |                |                |
| 46   | $\overline{\text{WR0}}$ /P84   | D                         | External bus write strobe. Control signals and data bus byte positions are related as the following :   |                         |                         |                  |                  |            |                         |                         |                |            |                         |                |                |
| 47   | $\overline{\text{WR1}}$ /P85   | D                         | <table border="1"> <thead> <tr> <th></th> <th>16-bit bus width</th> <th>8-bit bus width</th> <th>Single chip mode</th> </tr> </thead> <tbody> <tr> <td>D31 to D24</td> <td><math>\overline{\text{WR0}}</math></td> <td><math>\overline{\text{WR0}}</math></td> <td>(port allowed)</td> </tr> <tr> <td>D23 to D16</td> <td><math>\overline{\text{WR1}}</math></td> <td>(port allowed)</td> <td>(port allowed)</td> </tr> </tbody> </table> |                         | 16-bit bus width        | 8-bit bus width  | Single chip mode | D31 to D24 | $\overline{\text{WR0}}$ | $\overline{\text{WR0}}$ | (port allowed) | D23 to D16 | $\overline{\text{WR1}}$ | (port allowed) | (port allowed) |
|  |  |                           |   | 16-bit bus width        | 8-bit bus width         | Single chip mode |                  |            |                         |                         |                |            |                         |                |                |
|  |  |                           | D31 to D24  | $\overline{\text{WR0}}$ | $\overline{\text{WR0}}$ | (port allowed)   |                  |            |                         |                         |                |            |                         |                |                |
| D23 to D16   | $\overline{\text{WR1}}$  | (port allowed)            | (port allowed)  |                         |                         |                  |                  |            |                         |                         |                |            |                         |                |                |
| Note : $\overline{\text{WR1}}$ is set to Hi-z during resetting.<br>For using with 16-bit bus width, use an external pull-up resistor.<br>[P84 or P85] Available as general input/output ports when $\overline{\text{WR0}}$ and $\overline{\text{WR1}}$ are not used. |  |                           |   |                         |                         |                  |                  |            |                         |                         |                |            |                         |                |                |
| 48<br>49<br>50   | $\overline{\text{CS0}}$ /PA0<br>$\overline{\text{CS1}}$ /PA1<br>$\overline{\text{CS2}}$ /PA2 | D                         | Chip select 0 output (Low active)<br>Chip select 1 output (Low active)<br>Chip select 2 output (Low active)<br>[PA0, 1, or 2] Available as general input/output ports when $\overline{\text{CS0}}$ , $\overline{\text{CS1}}$ and $\overline{\text{CS2}}$ are not used.  |                         |                         |                  |                  |            |                         |                         |                |            |                         |                |                |

(Continued)

| No.  | Pin name   | Input/output circuit type | Description   |
|--|--|---------------------------|---|
| 51<br>52<br>53                               | $\overline{CS3}$ /PA3/SO1<br>$\overline{CS4}$ /PA4/SI1<br>$\overline{CS5}$ /PA5/SC1          | D                         | Chip select 3, 4, 5 output (Low active).<br>[PA3,4,5] Available as general input/output ports when channel 1 of chip select UART is not used.<br>[SO1,SI1,SC1] Data output, data input, and clock terminals of UART1. Active when UART1 operation is allowed.   |
| 54   | CLK/PA6  | D                         | System clock output. Outputs a same clock as the same frequency of external bus operation.<br>[PA6] Available as general input/output ports it is not used.   |
| 55<br>56<br>57<br>58<br>59<br>60<br>61<br>62 | OCPA0/PG0<br>OCPA1/PG1<br>OCPA2/PG2<br>OCPA3/PG3<br>OC0/PG4<br>OC1/PG5<br>OC2/PG6<br>OC3/PG7 | D                         | [OCPA0 to 3] PPG timer outputs. The function is active when PPG timer output is allowed.<br>[OC0 to 3] Output comparison output. The function is active when output comparison output is allowed. [PB0-7] Available as general input/output ports it is not used.                                       |
| 63<br>64<br>65                               | MD0<br>MD1<br>MD2  | B                         | Mode terminals 0 through 2. The terminals specify basic operation mode of MCU.<br>Use the terminals by connecting them directly to VCC or VSS.  |
| 66<br>67                                     | X0<br>X1   | A                         | Clock (oscillation) input.<br>Clock (oscillation) output.   |
| 68   | $\overline{RST}$   | C                         | External reset input.   |
| 69   | $\overline{HST}$   | C                         | Hardware standby input.   |
| 70   | P86/ALE  | D                         | [ALE] Address latch signal output. The function is active when ALE output of EPCR is allowed.   |
| 71<br>72                                     | INT0/PE0<br>INT1/PE1<br>INT2/PE2<br>INT3/PE3   | D                         | [INT0,1,2,3] External interrupt request inputs. The input is used whenever necessary if external interrupt is allowed. Output of other functions must be suspended if not on purpose.<br>[PE0,1,2,3] General input/output port  |
| 75<br>76                                     | INT4/PE4/TC11<br>INT5/PE5/SC0  | D                         | [INT4,5] External interrupt request inputs. The input is used whenever necessary if concerned external interrupt is allowed. Output of other functions must be suspended if not on purpose.<br>[TC11] External clock input of timer 1. [SC0] Clock input of UART0.<br>[PE4,5] General input/output port |
| 77   | SI0/PE6  | D                         | [SI0] Data input of UART0. This function is active when data input of UART0 is allowed.<br>[PE6] General input/output port  |
| 78   | SO0/PE7  | D                         | [SO0] Data output of UART0. This function is active when data output of UART0 is allowed.<br>[PE7] General input/output port  |

(Continued)

# MB91F127/F128

(Continued)

| No.       | Pin name   | Input/output circuit type | Description   |
|-----------|--|---------------------------|---|
| 79        | PF0/TCI0   | D                         | [TCI0] External clock input of timer 0.   |
|           |  |                           | [PF0] General input/output port   |
| 80        | SI2/PF1  | D                         | [SI2] Data input of UART2. This function is active when data input of UART2 is allowed.   |
|           |  |                           | [PF1] General input/output port   |
| 81        | SO2/PF2  | D                         | [SO2] Data output of UART2. This function is active when data output of UART2 is allowed.   |
|           |  |                           | [PF2] General input/output port. This function is active when data output of UART2 is disallowed.   |
| 82        | SC2/PF3/ $\overline{\text{ATG}}$   | D                         | [SC2] Clock input of UART2<br>[ATG] External trigger input of A/D converter. The input is used whenever necessary if a function concerned is selected. Output of other functions must be suspended if not on purpose. |
|           |  |                           | [PF3] General input/output port   |
| 83 to 90  | AN0/PJ0<br>AN1/PJ1<br>AN2/PJ2<br>AN3/PJ3<br>AN4/PJ4<br>AN5/PJ5<br>AN6/PJ6<br>AN7/PJ7 | E                         | [AN0 to AN7] Analog input of A/D converter. This function is active when analog input is specified in AIC register.   |
|           |  |                           | [PJ0 through PJ7] General input/output ports  |
| 91        | AVCC   | —                         | VCC power supply for A/D converter  |
| 92        | AVRH   | —                         | Reference voltage of A/D converter (high potential side). Be sure to turn on or off this terminal with a potential higher than AVRH applied to VCC.   |
| 93        | AVSS/AVRL  | —                         | A/D converter VSS power source and reference voltage (low potential side).  |
| 94 to 96  | VCC  | —                         | Power sources of digital circuits. Be sure to connect power source to all terminals when the device is used.  |
| 97 to 100 | VSS  | —                         | Ground level of digital circuits.   |

Note : Most of the above terminals multiplex inputs and outputs of I/O ports and resources, as indicated as "XXXX/PXX". If the outputs of ports and resources conflict with each other on the terminals, resources take preferences.



## INPUT/OUTPUT CIRCUIT TYPE

| Type | Circuit | Remarks  |
|------|---------|--|
| A    |         | <ul style="list-style-type: none"> <li>• For 25 MHz system</li> <li>• Oscillation feedback register :<br/>Approx. 1MΩ</li> <li>• Standby control is available.</li> </ul>    |
| B    |         | <ul style="list-style-type: none"> <li>• CMOS level input</li> <li>• High-voltage control is available for FLASH test.</li> </ul>  |
| C    |         | <ul style="list-style-type: none"> <li>• CMOS level hysteresis input</li> <li>• Standby control is not available.</li> </ul>   |
| D    |         | <ul style="list-style-type: none"> <li>• CMOS level output</li> <li>• CMOS level hysteresis input</li> <li>• Standby control is available</li> </ul>                         |
| E    |         | <ul style="list-style-type: none"> <li>• Standby control is available</li> <li>• CMOS level output</li> <li>• CMOS level hysteresis input</li> <li>• Analog input</li> </ul> |

# MB91F127/F128

## ■ HANDLING DEVICES

### 1. Preventing latch up

On a CMOS IC, latch up may occur when a voltage higher than VCC or a voltage lower than VSS is applied to input terminal or output terminal, or when a voltage exceeding rated level is applied across VCC and VSS. Latch up causes drastic increase of power source current, which may result in destruction of the element by heat. Take extra care not to exceed maximum rating in use. Also, take extra care so that analog terminal does not exceed digital power source.

### 2. Treatment of unused input terminals

Leaving unused terminals open may cause malfunction. Apply pull-up or pull-down treatment on unused terminals.

### 3. External reset input

Complete resetting of internal system requires inputting "L" level signal to  $\overline{\text{RST}}$  terminal for a minimum of 5 machine cycles.

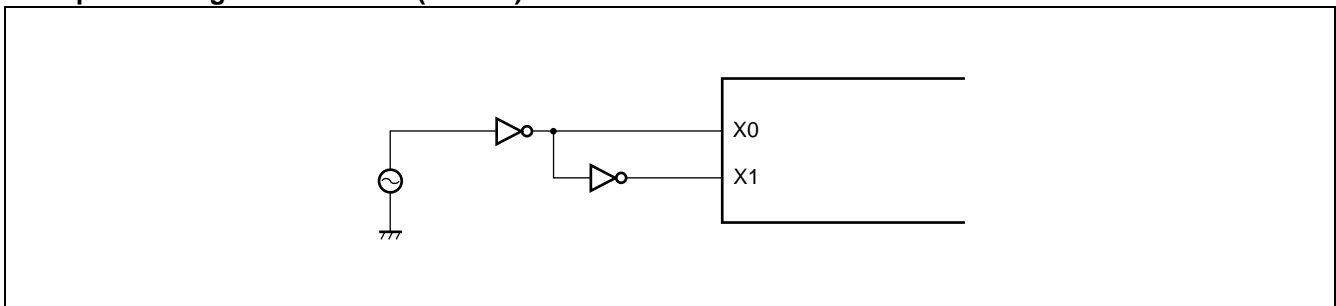
### 4. Notes on using external clock

When using an external clock, supply a clock signal to X0 terminal and supply its antiphase clock to X1 terminal simultaneously. In this case, do not use STOP mode (oscillation stop mode). (Because X1 terminal halts with "H" output under STOP status.)

Under a 12.5 MHz frequency, the device operates with a clock supplied to X0 terminal only.

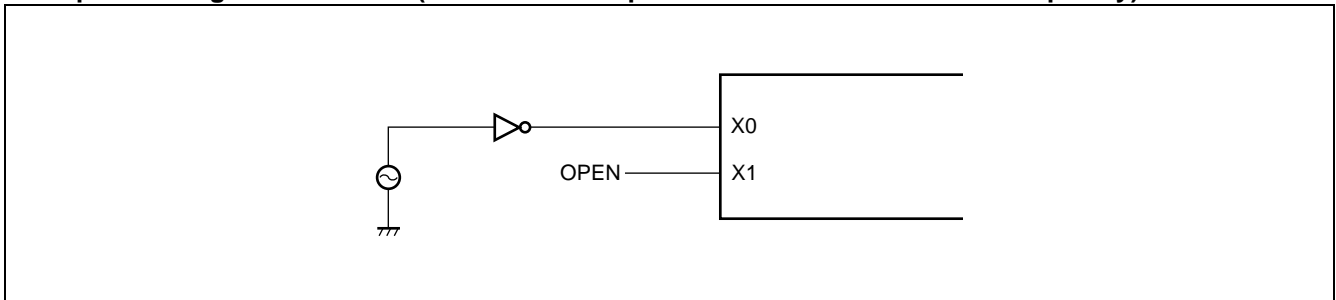
Figures show examples of using an external clock.

#### Example of using external clock (normal)



Note : STOP mode (oscillation stop mode) is not available.

#### Example of using external clock (allowed under operation at 12.5 MHz or lower frequency)



## 5. Connecting power supply terminals (VCC, VSS)

If two or more VCC, VSS terminals are used, the terminals to be placed under the same potentials are connected with each other internally for preventing malfunctions such as latch up. However, for reducing unwanted radiation, preventing malfunctions of strobe signals and observing total power and current ratings, be sure to connect all of these terminals to power supply and ground externally.

Connecting power supply to VCC - VSS in impedance as low as possible is desirable.

## 6. Crystal oscillator circuit

Noises around X0 and X1 terminals causes malfunction of the device. Design printed wiring so that X0, X1, and crystal oscillator (or ceramic oscillator), and bypass capacitor to the ground are aligned as close as possible one another. Also the wiring of those elements should not cross with other wiring if possible. Printed wiring with ground wires around X0 and X1 terminals ensures more stable operations. Such designing is strongly recommended.

## 7. Treating NC terminals

Be sure to leave NC terminals open.

## 8. Mode terminals (MD0 through MD2)

Do not connect the mode terminals directly to VCC or VSS.

For preventing malfunctions caused by noises, make printed traces between the mode terminals and VCC or VSS as short as possible, and connect the elements in lower impedance.

## 9. Turning power on

Be sure to turn on the power of the device with  $\overline{\text{RST}}$  terminal placed under "L" level. Ensure a period at a minimum of 5 cycles of internal operation clock before placing the terminal under "H" level.

## 10. Terminal status upon turning on power

Status upon turning on the power is indefinite. Upon turning on the power, oscillation starts and the circuit is initialized.

## 11. Oscillation input upon turning on power

Upon turning on the power, be sure to input a clock signal until oscillation stabilizing wait status is released.

## 12. Initializing power-on reset

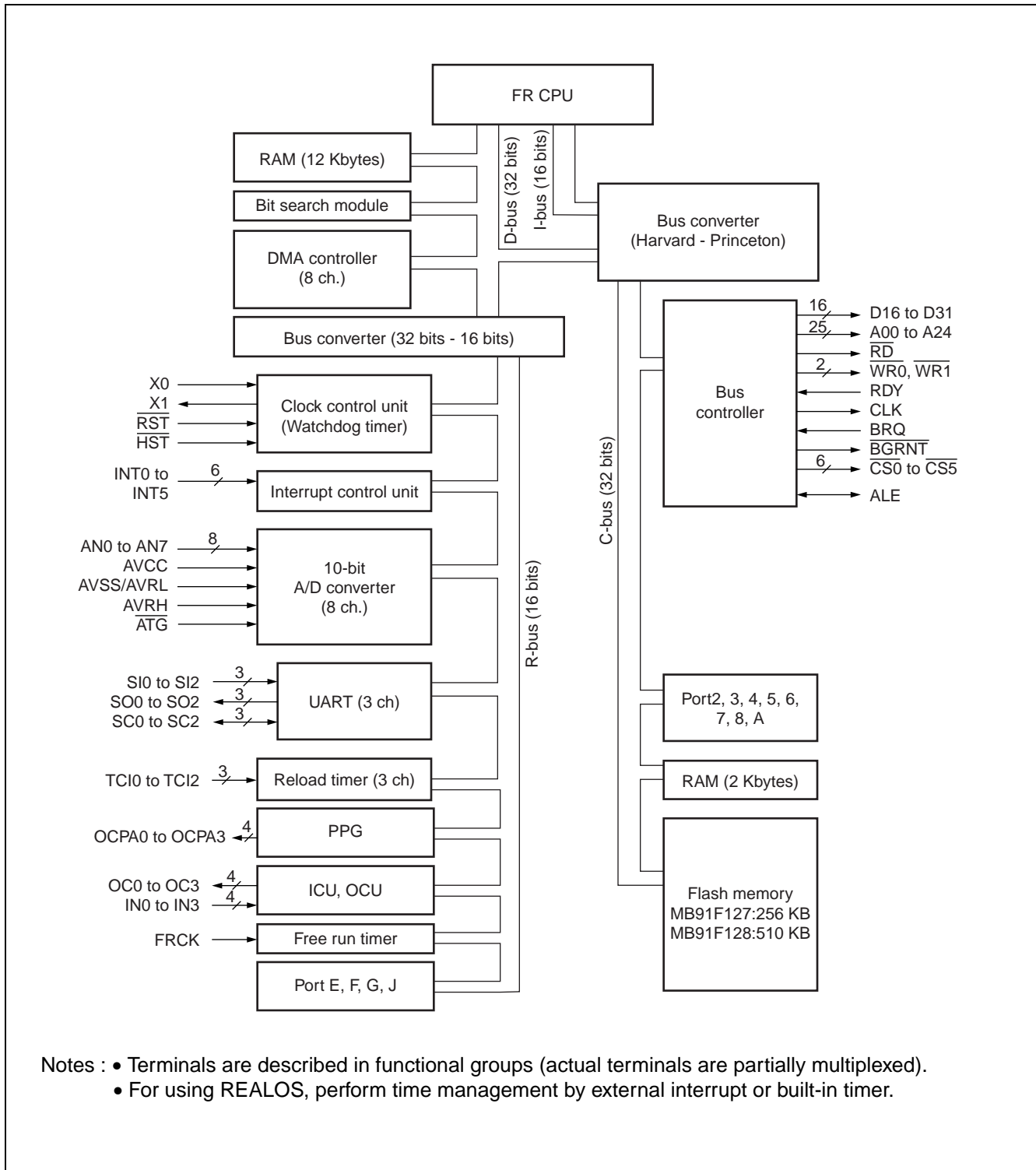
The device includes some built-in registers that are initialized only with power-on reset operation. For initializing the registers, perform power-on reset by turning on the power again.

## 13. Recovery from Sleep/Stop status

For recovering from Sleep/Stop status initiated by a program in C-Bus RAM, reset the device instead of recovering by an interrupt process.

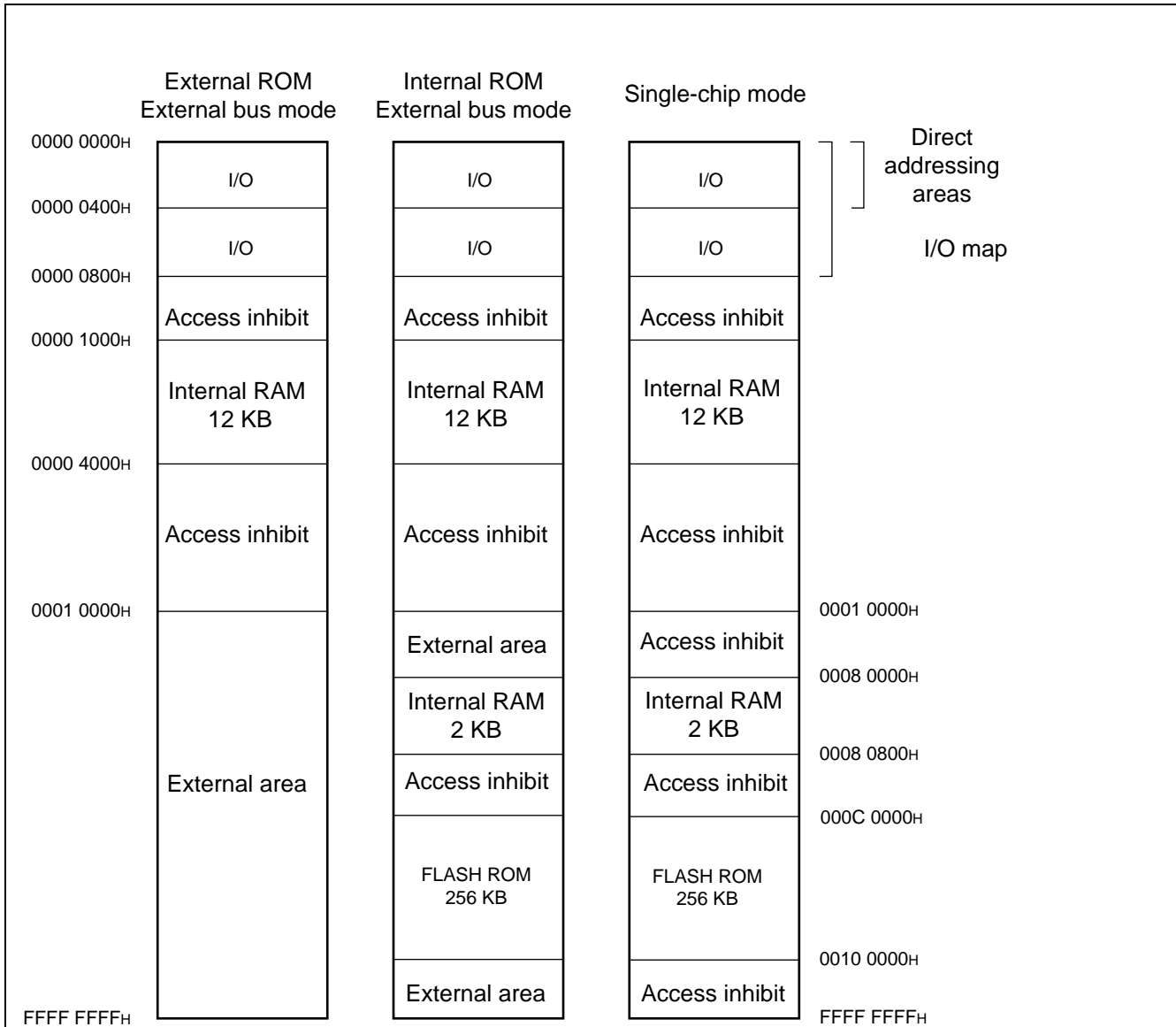
# MB91F127/F128

## ■ BLOCK DIAGRAM



## ■ CPU CORE MEMORY SPACE

### • MB91F127



Note : External area is not accessible in single-chip mode. When accessing to external areas, select the internal ROM external bus mode in mode register.

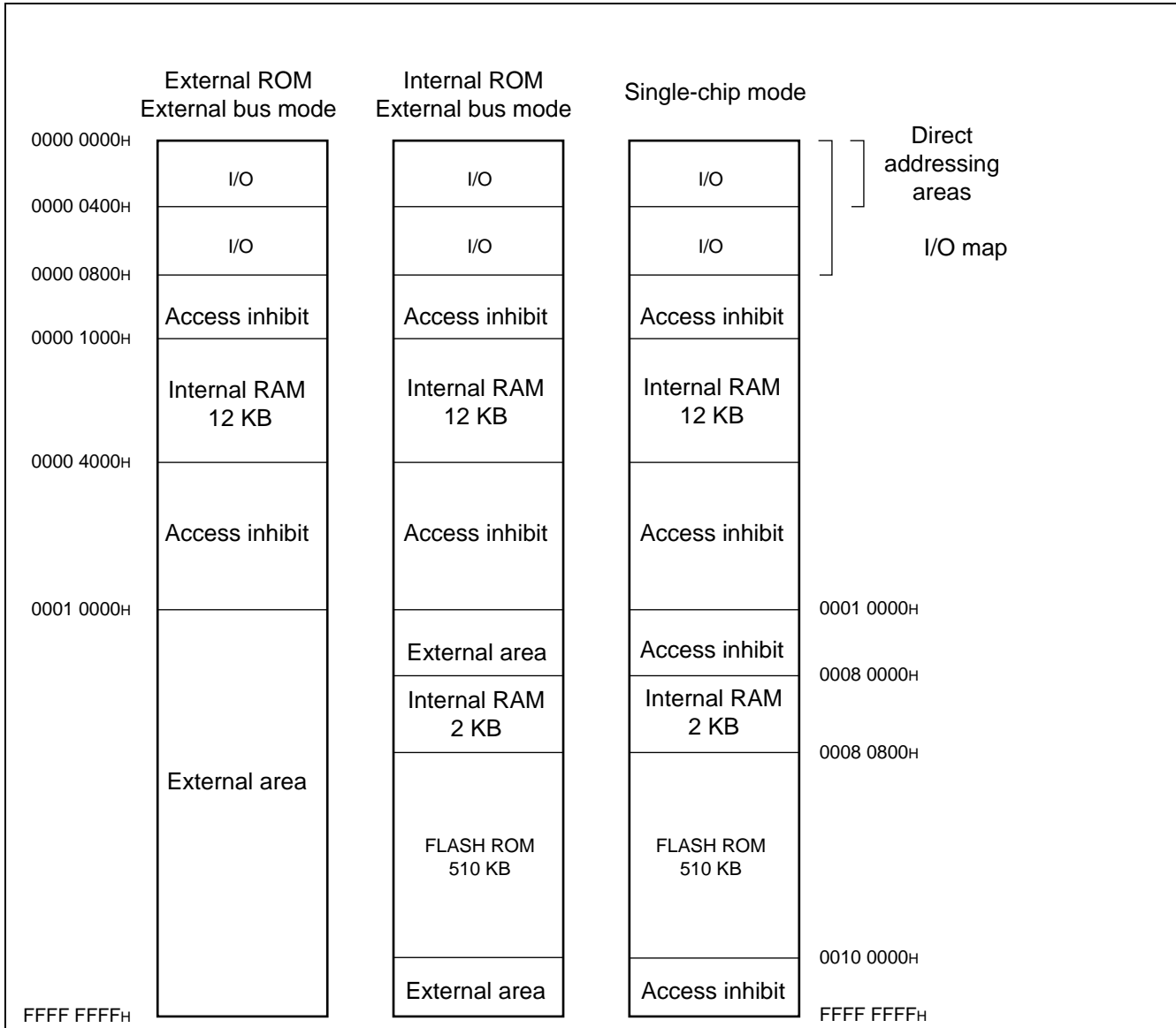
### Direct addressing areas

The areas described below are used for I/O processes. The areas, referred to as “direct addressing areas,” allow specifying an operand address directly by an instruction. The direct addressing areas varies as the following, depending on size of the data to be accessed.

- Byte-data access : 0 to 0FF<sub>H</sub>
- Half-word data access : 0 to 1FF<sub>H</sub>
- Word-data access : 0 to 3FF<sub>H</sub>

# MB91F127/F128

## • MB91F128



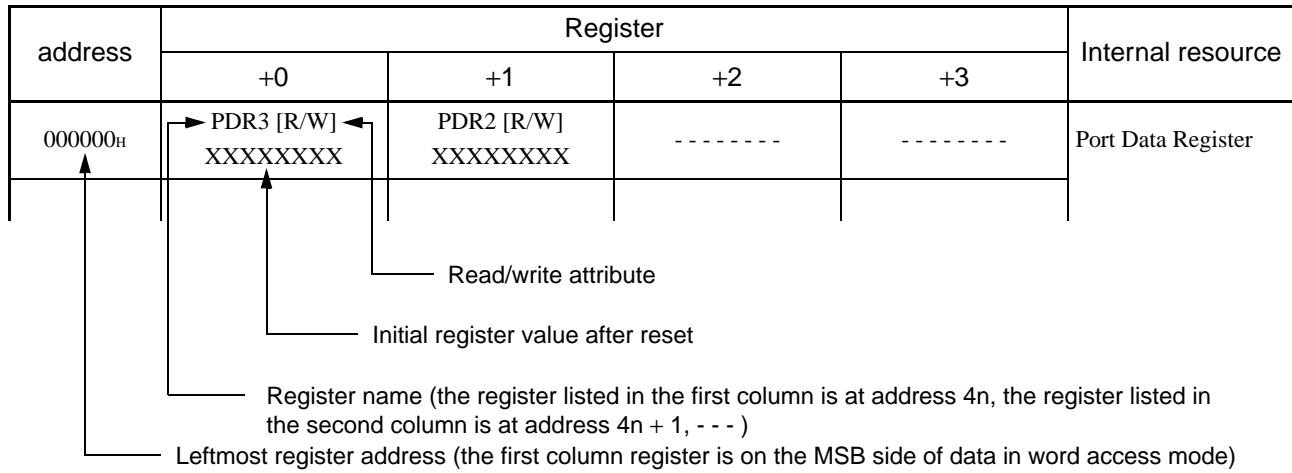
Note : External area is not accessible in single-chip mode. When accessing to external areas, select the internal ROM external bus mode in mode register.

### Direct addressing areas

The areas described below are used for I/O processes. The areas, referred to as “direct addressing areas,” allow specifying an operand address directly by an instruction. The direct addressing areas varies as the following, depending on size of the data to be accessed.

- Byte-data access : 0 to 0FF<sub>H</sub>
- Half-word data access : 0 to 1FF<sub>H</sub>
- Word-data access : 0 to 3FF<sub>H</sub>

## ■ LEGEND OF I/O MAP



Note : Register bit values indicate initial values as shown below :

“1” : Initial value “1”

“0” : Initial value “0”

“X” : Initial value “X”

“-” : Register does not exist physically in this position.

# MB91F127/F128

## ■ I/O MAP

| Address | Register                       |                        |                                  |                        | Internal resource                    |
|---------|--------------------------------|------------------------|----------------------------------|------------------------|--------------------------------------|
|         | +0                             | +1                     | +2                               | +3                     |                                      |
| 000000H | PDR3 [R/W]<br>XXXXXXXX         | PDR2 [R/W]<br>XXXXXXXX | —                                | —                      | Port data Register                   |
| 000004H | PDR7 [R/W]<br>-----X           | PDR6 [R/W]<br>XXXXXXXX | PDR5 [R/W]<br>XXXXXXXX           | PDR4 [R/W]<br>XXXXXXXX |                                      |
| 000008H | —                              | PDRA [R/W]<br>XXXXXXXX | —                                | PDR8[R/W]<br>--XXXXXX  |                                      |
| 00000CH | —                              |                        |                                  |                        |                                      |
| 000010H | —                              | —                      | PDRE [R/W]<br>XXXXXXXX           | PDRF [R/W]<br>XXXXXXXX |                                      |
| 000014H | PDRG [R/W]<br>XXXXXXXX         | —                      | —                                | PDRJ [R/W]<br>XXXXXXXX |                                      |
| 000018H | —                              | —                      | —                                | —                      | Reserved                             |
| 00001CH | SSR [R/W]<br>00001-00          | SIDR [R/W]<br>XXXXXXXX | SCR [R/W]<br>00000100            | SMR [R/W]<br>00--0-00  | UART0                                |
| 000020H | SSR [R/W]<br>00001-00          | SIDR [R/W]<br>XXXXXXXX | SCR [R/W]<br>00000100            | SMR [R/W]<br>00--0-00  | UART1                                |
| 000024H | SSR [R/W]<br>00001-00          | SIDR [R/W]<br>XXXXXXXX | SCR [R/W]<br>00000100            | SMR [R/W]<br>00--0-00  | UART2                                |
| 000028H | TMRLR [W]<br>XXXXXXXX XXXXXXXX |                        | TMR [W]<br>XXXXXXXX XXXXXXXX     |                        | Reload Timer 0                       |
| 00002CH | —                              |                        | TMCSR [R/W]<br>----0000 00000000 |                        |                                      |
| 000030H | TMRLR [W]<br>XXXXXXXX XXXXXXXX |                        | TMR [W]<br>XXXXXXXX XXXXXXXX     |                        | Reload Timer 1                       |
| 000034H | —                              |                        | TMCSR [R/W]<br>----0000 00000000 |                        |                                      |
| 000038H | —                              |                        | —                                |                        | Reserved                             |
| 00003CH | TMRLR [W]<br>XXXXXXXX XXXXXXXX |                        | TMR [W]<br>XXXXXXXX XXXXXXXX     |                        | Reload Timer 2                       |
| 000040H | —                              |                        | TMCSR [R/W]<br>----0000 00000000 |                        |                                      |
| 000044H | IPCP1[R]<br>XXXXXXXX XXXXXXXX  |                        | IPCP0[R]<br>XXXXXXXX XXXXXXXX    |                        | 16 bit ICU                           |
| 000048H | IPCP3[R]<br>XXXXXXXX XXXXXXXX  |                        | IPCP2[R]<br>XXXXXXXX XXXXXXXX    |                        |                                      |
| 00004CH | —                              | ICS23[R/W]<br>00000000 | —                                | ICS01[R/W]<br>00000000 |                                      |
| 000050H | ADCR [W]<br>00101-XX XXXXXXXX  |                        | ADCS [R/W]<br>00000000 00000000  |                        | A/D converter<br>(Serially compared) |



| Address             | Register                             |                        |                                    |                           | Internal resource          |
|---------------------|--------------------------------------|------------------------|------------------------------------|---------------------------|----------------------------|
|                     | +0                                   | +1                     | +2                                 | +3                        |                            |
| 000054 <sub>H</sub> | OCCP1[R/W]<br>XXXXXXXX XXXXXXXX      |                        | OCCP0[R/W]<br>XXXXXXXX XXXXXXXX    |                           | 16 bit OCU                 |
| 000058 <sub>H</sub> | OCCP3[R/W]<br>XXXXXXXX XXXXXXXX      |                        | OCCP2[R/W]<br>XXXXXXXX XXXXXXXX    |                           |                            |
| 00005C <sub>H</sub> | —                                    |                        | —                                  |                           | Reserved                   |
| 000060 <sub>H</sub> | —                                    |                        | —                                  |                           |                            |
| 000064 <sub>H</sub> | OCS2, 3[R/W]<br>XXX00000 0000XX00    |                        | OCS0, 1[R/W]<br>XXX00000 0000XX00  |                           | 16 bit OCU                 |
| 000068 <sub>H</sub> | —                                    |                        | —                                  |                           | Reserved                   |
| 00006C <sub>H</sub> | TCDT [R/W]<br>00000000 00000000      |                        | TCCS [R/W]<br>0 - - - - - 00000000 |                           | Free run timer             |
| 000070 <sub>H</sub> | —                                    |                        | —                                  |                           | Reserved                   |
| 000074 <sub>H</sub> | —                                    |                        | —                                  |                           | Reserved                   |
| 000078 <sub>H</sub> | UTM/UTIMR [R/W]<br>00000000 00000000 |                        | —                                  | UTIMC[R/W]<br>0 - - 00001 | U-Timer0                   |
| 00007C <sub>H</sub> | UTM/UTIMR [R/W]<br>00000000 00000000 |                        | —                                  | UTIMC[R/W]<br>0 - - 00001 | U-Timer1                   |
| 000080 <sub>H</sub> | UTM/UTIMR [R/W]<br>00000000 00000000 |                        | —                                  | UTIMC[R/W]<br>0 - - 00001 | U-Timer2                   |
| 000084 <sub>H</sub> | —                                    |                        | —                                  |                           | Reserved                   |
| 000088 <sub>H</sub> | —                                    |                        | —                                  |                           |                            |
| 00008C <sub>H</sub> | —                                    |                        | —                                  |                           | Reserved                   |
| 000090 <sub>H</sub> | —                                    |                        | —                                  |                           |                            |
| 000094 <sub>H</sub> | EIRR [R/W]<br>00000000               | ENIR [R/W]<br>00000000 | —                                  |                           | External interrupt/<br>NMI |
| 000098 <sub>H</sub> | EHVR [R/W]<br>- - - - 0000           | ELVR [R/W]<br>00000000 | —                                  |                           |                            |

(Continued)

# MB91F127/F128

| Address             | Register                        |                     |                                |                        | Internal resource       |
|---------------------|---------------------------------|---------------------|--------------------------------|------------------------|-------------------------|
|                     | +0                              | +1                  | +2                             | +3                     |                         |
| 00009C <sub>H</sub> | —                               |                     |                                |                        | Reserved                |
| 0000A0 <sub>H</sub> | —                               |                     |                                |                        |                         |
| 0000A4 <sub>H</sub> | —                               |                     |                                |                        |                         |
| 0000A8 <sub>H</sub> | —                               |                     |                                |                        |                         |
| 0000AC <sub>H</sub> | —                               |                     |                                |                        |                         |
| 0000B0 <sub>H</sub> | —                               |                     |                                |                        |                         |
| 0000B4 <sub>H</sub> | —                               |                     |                                |                        |                         |
| 0000B8 <sub>H</sub> | —                               |                     |                                |                        |                         |
| 0000BC <sub>H</sub> | —                               |                     |                                |                        |                         |
| 0000C0 <sub>H</sub> | —                               |                     |                                |                        |                         |
| 0000C4 <sub>H</sub> | —                               |                     |                                |                        |                         |
| 0000C8 <sub>H</sub> | —                               |                     |                                |                        |                         |
| 0000CC <sub>H</sub> | —                               |                     |                                |                        |                         |
| 0000D0 <sub>H</sub> | —                               | —                   | DDRE [W]<br>00000000           | DDRF [W]<br>00000000   | Port direction register |
| 0000D4 <sub>H</sub> | —                               | AIC3[W]<br>11111111 | —                              | —                      | A/D converter           |
| 0000D8 <sub>H</sub> | DDRG [W]<br>00000000            | —                   | —                              | DDRJ [W]<br>00000000   | Port direction register |
| 0000DC <sub>H</sub> | GCN1 [R/W]<br>00110010 00010000 |                     | -----                          | GCN2[R/W]<br>00000000  | PPG ctl                 |
| 0000E0 <sub>H</sub> | PTMR0 [R]<br>11111111 11111111  |                     | PCSR0 [W]<br>XXXXXXXX XXXXXXXX |                        | PPG0                    |
| 0000E4 <sub>H</sub> | PDUT0 [W]<br>XXXXXXXX XXXXXXXX  |                     | PCNH0[R/W]<br>0000000 -        | PCNL0[R/W]<br>00000000 |                         |
| 0000E8 <sub>H</sub> | PTMR1 [R]<br>11111111 11111111  |                     | PCSR1 [W]<br>XXXXXXXX XXXXXXXX |                        | PPG1                    |
| 0000EC <sub>H</sub> | PDUT1 [W]<br>XXXXXXXX XXXXXXXX  |                     | PCNH1[R/W]<br>0000000 -        | PCNL1[R/W]<br>00000000 |                         |
| 0000F0 <sub>H</sub> | PTMR2 [R]<br>11111111 11111111  |                     | PCSR2 [W]<br>XXXXXXXX XXXXXXXX |                        | PPG2                    |
| 0000F4 <sub>H</sub> | PDUT2 [W]<br>XXXXXXXX XXXXXXXX  |                     | PCNH2[R/W]<br>0000000 -        | PCNL2[R/W]<br>00000000 |                         |
| 0000F8 <sub>H</sub> | PTMR3 [R]<br>11111111 11111111  |                     | PCSR3 [W]<br>XXXXXXXX XXXXXXXX |                        | PPG3                    |
| 0000FC <sub>H</sub> | PDUT3 [W]<br>XXXXXXXX XXXXXXXX  |                     | PCNH3[R/W]<br>0000000 -        | PCNL3[R/W]<br>00000000 |                         |

(Continued)

www.DataSheet4U.com

| Address  | Register   |    |    |    | Internal resource |
|--|--|----|----|----|-------------------|
|  | +0   | +1 | +2 | +3 |                   |
| 000100 <sub>H</sub><br>to<br>0001FC <sub>H</sub> | —  |    |    |    | Reserved          |
| 000200 <sub>H</sub>                              | DPDP [R/W]<br>----- -0000000                       |    |    |    | DMAC              |
| 000204 <sub>H</sub>                              | DACSR [R/W]<br>00000000 00000000 00000000 00000000 |    |    |    |                   |
| 000208 <sub>H</sub>                              | DATCR [R/W]<br>----- --XX0000 --XX0000 --XX0000    |    |    |    |                   |
| 00020C <sub>H</sub>                              | —  |    |    |    |                   |
| 000210 <sub>H</sub><br>to<br>0002FC <sub>H</sub> | —  |    |    |    | Reserved          |
| 000300 <sub>H</sub><br>to<br>0003EC <sub>H</sub> | —  |    |    |    | Reserved          |
| 0003F0 <sub>H</sub>                              | BSD0 [W]<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX    |    |    |    | Bit search module |
| 0003F4 <sub>H</sub>                              | BSD1 [R/W]<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX  |    |    |    |                   |
| 0003F8 <sub>H</sub>                              | BSDC [W]<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX    |    |    |    |                   |
| 0003FC <sub>H</sub>                              | BSRR [R/W]<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX  |    |    |    |                   |

*(Continued)*

# MB91F127/F128

| Address  | Register                         |                        |                         |                        | Internal resource         |
|--|----------------------------------|------------------------|-------------------------|------------------------|---------------------------|
|  | +0                               | +1                     | +2                      | +3                     |                           |
| 000400 <sub>H</sub>                              | ICR00 [R/W]<br>---11111          | ICR01[R/W]<br>---11111 | ICR02[R/W]<br>---11111  | ICR03[R/W]<br>---11111 | Interrupt controller      |
| 000404 <sub>H</sub>                              | ICR04[R/W]<br>---11111           | ICR05[R/W]<br>---11111 | ICR06[R/W]<br>---11111  | ICR07[R/W]<br>---11111 |                           |
| 000408 <sub>H</sub>                              | ICR08 [R/W]<br>---11111          | ICR09[R/W]<br>---11111 | ICR10[R/W]<br>---11111  | ICR11[R/W]<br>---11111 |                           |
| 00040C <sub>H</sub>                              | ICR12[R/W]<br>---11111           | ICR13[R/W]<br>---11111 | ICR14[R/W]<br>---11111  | ICR15[R/W]<br>---11111 |                           |
| 000410 <sub>H</sub>                              | ICR16[R/W]<br>---11111           | ICR17[R/W]<br>---11111 | ICR18[R/W]<br>---11111  | ICR19[R/W]<br>---11111 |                           |
| 000414 <sub>H</sub>                              | ICR20[R/W]<br>---11111           | ICR21[R/W]<br>---11111 | ICR22[R/W]<br>---11111  | ICR23[R/W]<br>---11111 |                           |
| 000418 <sub>H</sub>                              | ICR24 [R/W]<br>---11111          | ICR25[R/W]<br>---11111 | ICR26[R/W]<br>---11111  | ICR27[R/W]<br>---11111 |                           |
| 00041C <sub>H</sub>                              | ICR28[R/W]<br>---11111           | ICR29[R/W]<br>---11111 | ICR30[R/W]<br>---11111  | ICR31[R/W]<br>---11111 |                           |
| 000420 <sub>H</sub>                              | ICR32[R/W]<br>---11111           | ICR33[R/W]<br>---11111 | ICR34[R/W]<br>---11111  | ICR35[R/W]<br>---11111 |                           |
| 000424 <sub>H</sub>                              | ICR36[R/W]<br>---11111           | ICR37[R/W]<br>---11111 | ICR38[R/W]<br>---11111  | ICR39[R/W]<br>---11111 |                           |
| 000428 <sub>H</sub>                              | ICR40[R/W]<br>---11111           | ICR41[R/W]<br>---11111 | ICR42[R/W]<br>---11111  | ICR43[R/W]<br>---11111 |                           |
| 00042C <sub>H</sub>                              | ICR44[R/W]<br>---11111           | ICR45[R/W]<br>---11111 | ICR46[R/W]<br>---11111  | ICR47[R/W]<br>---11111 |                           |
| 000430 <sub>H</sub>                              | DICR [R/W]<br>-----0             | HRCL [R/W]<br>---11111 | —                       | —                      | Delay interrupt           |
| 000434 <sub>H</sub><br>to<br>00047C <sub>H</sub> | —                                |                        |                         |                        | Reserved                  |
| 000480 <sub>H</sub>                              | RSRR/WTCR<br>[R/W]<br>1XXXX - 00 | STCR [R/W]<br>000111-- | PDDR [R/W]<br>---- 0000 | CTBR [W]<br>XXXXXXXX   | Clock controller<br>block |
| 000484 <sub>H</sub>                              | GCR [R/W]<br>110011 - 1          | WPR [W]<br>XXXXXXXX    | —                       | —                      |                           |
| 000488 <sub>H</sub>                              | PTCR [R/W]<br>00 -- 0 ---        | —                      |                         |                        | PLL controller<br>block   |
| 00048C <sub>H</sub><br>to<br>0005FC <sub>H</sub> | —                                |                        |                         |                        | Reserved                  |

(Continued)

(Continued)

| Address  | Register                          |                          |                                   |                          | Internal resource                    |
|--|-----------------------------------|--------------------------|-----------------------------------|--------------------------|--------------------------------------|
|  | +0                                | +1                       | +2                                | +3                       |                                      |
| 000600 <sub>H</sub>                              | DDR3 [W]<br>00000000              | DDR2 [W]<br>00000000     | —                                 | —                        | Data direction register              |
| 000604 <sub>H</sub>                              | DDR7 [W]<br>----- 0               | DDR6 [W]<br>00000000     | DDR5 [W]<br>00000000              | DDR4 [W]<br>00000000     |                                      |
| 000608 <sub>H</sub>                              | —                                 | DDRA [W]<br>-0000000     | —                                 | DDR8 [W]<br>-- 000000    |                                      |
| 00060C <sub>H</sub>                              | ASR1 [W]<br>00000000 00000001     |                          | AMR1 [W]<br>00000000 00000000     |                          | External bus interface               |
| 000610 <sub>H</sub>                              | ASR2 [W]<br>00000000 00000010     |                          | AMR2 [W]<br>00000000 00000000     |                          |                                      |
| 000614 <sub>H</sub>                              | ASR3 [W]<br>00000000 00000011     |                          | AMR3 [W]<br>00000000 00000000     |                          |                                      |
| 000618 <sub>H</sub>                              | ASR4 [W]<br>00000000 00000100     |                          | AMR4 [W]<br>00000000 00000000     |                          |                                      |
| 00061C <sub>H</sub>                              | ASR5 [W]<br>00000000 00000101     |                          | AMR5 [W]<br>00000000 00000000     |                          |                                      |
| 000620 <sub>H</sub>                              | AMD0 [R/W]<br>--- XX111           | AMD1 [R/W]<br>0 -- 00000 | AMD32[R/W]<br>00000000            | AMD4 [R/W]<br>0 -- 00000 |                                      |
| 000624 <sub>H</sub>                              | AMD5[R/W]<br>0 -- 00000           | DSCR [W]<br>00000000     | RFCR [R/W]<br>--XXXXXX 00 --- 000 |                          |                                      |
| 000628 <sub>H</sub>                              | EPCR0 [W]<br>-- 1 - 1100 -1111111 |                          | EPCR1 [W]<br>----- 1 11111111     |                          |                                      |
| 00062C <sub>H</sub>                              | DMCR4 [R/W]<br>00000000 0000000-  |                          | DMCR5 [R/W]<br>00000000 0000000-  |                          |                                      |
| 000630 <sub>H</sub><br>to<br>0007BC <sub>H</sub> | —                                 |                          |                                   |                          |                                      |
| 0007C0 <sub>H</sub>                              | FSTR [R/W]<br>000XXXX0            | —                        | —                                 | —                        | Flash memory                         |
| 0007C4 <sub>H</sub><br>to<br>0007F8 <sub>H</sub> | —                                 |                          |                                   |                          | Reserved                             |
| 0007FC <sub>H</sub>                              | —                                 | —                        | LER [W]<br>----- 000              | MODR [W]<br>XXXXXXXXX    | Little endian register mode register |

Note : Do not issue RMW instructions to a register with write-only bit.

RMW instructions (RMW : Read modify write)

AND Rj, @Ri      OR Rj, @Ri      EOR Rj, @Ri

ANDH Rj, @Ri    ORH Rj, @Ri      EORH Rj, @Ri

ANDB Rj, @Ri    ORB Rj, @Ri      EORB Rj, @Ri

BANDL #u4, @Ri    BORL #u4, @Ri    BEORL #u4, @Ri

BANDH #u4, @Ri    BORH #u4, @Ri    BEORH #u4, @Ri

Data in "Reserved" or "-" area is indefinite.

# MB91F127/F128

## ■ INTERRUPT CAUSES, INTERRUPT VECTORS AND INTERRUPT CONTROL REGISTER ALLOCATIONS

| Interrupt causes                | Interrupt number |             | Interrupt level               |                  | TBR default Address*2 |
|---------------------------------|------------------|-------------|-------------------------------|------------------|-----------------------|
|                                 | Decimal          | Hexadecimal | Register*1                    | Offset           |                       |
| Reset                           | 0                | 00          | —                             | 3FC <sub>H</sub> | 000FFFFC <sub>H</sub> |
| Reserved by system              | 1                | 01          | —                             | 3F8 <sub>H</sub> | 000FFFF8 <sub>H</sub> |
| Reserved by system              | 2                | 02          | —                             | 3F4 <sub>H</sub> | 000FFFF4 <sub>H</sub> |
| Reserved by system              | 3                | 03          | —                             | 3F0 <sub>H</sub> | 000FFFF0 <sub>H</sub> |
| Reserved by system              | 4                | 04          | —                             | 3EC <sub>H</sub> | 000FFFE <sub>C</sub>  |
| Reserved by system              | 5                | 05          | —                             | 3E8 <sub>H</sub> | 000FFFE8 <sub>H</sub> |
| Reserved by system              | 6                | 06          | —                             | 3E4 <sub>H</sub> | 000FFFE4 <sub>H</sub> |
| Reserved by system              | 7                | 07          | —                             | 3E0 <sub>H</sub> | 000FFFE0 <sub>H</sub> |
| Reserved by system              | 8                | 08          | —                             | 3DC <sub>H</sub> | 000FFFD <sub>C</sub>  |
| Reserved by system              | 9                | 09          | —                             | 3D8 <sub>H</sub> | 000FFFD8 <sub>H</sub> |
| Reserved by system              | 10               | 0A          | —                             | 3D4 <sub>H</sub> | 000FFFD4 <sub>H</sub> |
| Reserved by system              | 11               | 0B          | —                             | 3D0 <sub>H</sub> | 000FFFD0 <sub>H</sub> |
| Reserved by system              | 12               | 0C          | —                             | 3CC <sub>H</sub> | 000FFFCC <sub>H</sub> |
| Reserved by system              | 13               | 0D          | —                             | 3C8 <sub>H</sub> | 000FFFC8 <sub>H</sub> |
| Undefined instruction exception | 14               | 0E          | —                             | 3C4 <sub>H</sub> | 000FFFC4 <sub>H</sub> |
| NMI request                     | 15               | 0F          | 15 (F <sub>H</sub> )<br>fixed | 3C0 <sub>H</sub> | 000FFFC0 <sub>H</sub> |
| External interrupt 0            | 16               | 10          | ICR00                         | 3BC <sub>H</sub> | 000FFFBC <sub>H</sub> |
| External interrupt 1            | 17               | 11          | ICR01                         | 3B8 <sub>H</sub> | 000FFFB8 <sub>H</sub> |
| External interrupt 2            | 18               | 12          | ICR02                         | 3B4 <sub>H</sub> | 000FFFB4 <sub>H</sub> |
| External interrupt 3            | 19               | 13          | ICR03                         | 3B0 <sub>H</sub> | 000FFFB0 <sub>H</sub> |
| UART 0 reception complete       | 20               | 14          | ICR04                         | 3AC <sub>H</sub> | 000FFFAC <sub>H</sub> |
| UART 1 reception complete       | 21               | 15          | ICR05                         | 3A8 <sub>H</sub> | 000FFFA8 <sub>H</sub> |
| UART 2 reception complete       | 22               | 16          | ICR06                         | 3A4 <sub>H</sub> | 000FFFA4 <sub>H</sub> |
| UART 0 transmission complete    | 23               | 17          | ICR07                         | 3A0 <sub>H</sub> | 000FFFA0 <sub>H</sub> |
| UART 1 transmission complete    | 24               | 18          | ICR08                         | 39C <sub>H</sub> | 000FFF9C <sub>H</sub> |
| UART 2 transmission complete    | 25               | 19          | ICR09                         | 398 <sub>H</sub> | 000FFF98 <sub>H</sub> |

(Continued)

| Interrupt causes      | Interrupt number |             | Interrupt level |                  | TBR default Address*2 |
|-----------------------|------------------|-------------|-----------------|------------------|-----------------------|
|                       | Decimal          | Hexadecimal | Register*1      | Offset           |                       |
| DMAC 0 (end, error)   | 26               | 1A          | ICR10           | 394 <sub>H</sub> | 000FFF94 <sub>H</sub> |
| DMAC 1 (end, erro)    | 27               | 1B          | ICR11           | 390 <sub>H</sub> | 000FFF90 <sub>H</sub> |
| DMAC 2 (end, erro)    | 28               | 1C          | ICR12           | 38C <sub>H</sub> | 000FFF8C <sub>H</sub> |
| DMAC 3 (end, erro)    | 29               | 1D          | ICR13           | 388 <sub>H</sub> | 000FFF88 <sub>H</sub> |
| DMAC 4 (end, erro)    | 30               | 1E          | ICR14           | 384 <sub>H</sub> | 000FFF84 <sub>H</sub> |
| DMAC 5 (end, erro)    | 31               | 1F          | ICR15           | 380 <sub>H</sub> | 000FFF80 <sub>H</sub> |
| DMAC 6 (end, erro)    | 32               | 20          | ICR16           | 37C <sub>H</sub> | 000FFF7C <sub>H</sub> |
| DMAC 7 (end, erro)    | 33               | 21          | ICR17           | 378 <sub>H</sub> | 000FFF78 <sub>H</sub> |
| A/D (sequential type) | 34               | 22          | ICR18           | 374 <sub>H</sub> | 000FFF74 <sub>H</sub> |
| Reload timer 0        | 35               | 23          | ICR19           | 370 <sub>H</sub> | 000FFF70 <sub>H</sub> |
| Reload timer 1        | 36               | 24          | ICR20           | 36C <sub>H</sub> | 000FFF6C <sub>H</sub> |
| Reload timer 2        | 37               | 25          | ICR21           | 368 <sub>H</sub> | 000FFF68 <sub>H</sub> |
| External interrupt 4  | 38               | 26          | ICR22           | 364 <sub>H</sub> | 000FFF64 <sub>H</sub> |
| External interrupt 5  | 39               | 27          | ICR23           | 360 <sub>H</sub> | 000FFF60 <sub>H</sub> |
| Reserved by system    | 40               | 28          | ICR24           | 35C <sub>H</sub> | 000FFF5C <sub>H</sub> |
| Reserved by system    | 41               | 29          | ICR25           | 358 <sub>H</sub> | 000FFF58 <sub>H</sub> |
| U-TIMER 0             | 42               | 2A          | ICR26           | 354 <sub>H</sub> | 000FFF54 <sub>H</sub> |
| U-TIMER 1             | 43               | 2B          | ICR27           | 350 <sub>H</sub> | 000FFF50 <sub>H</sub> |
| U-TIMER 2             | 44               | 2C          | ICR28           | 34C <sub>H</sub> | 000FFF4C <sub>H</sub> |
| FLASH memory          | 45               | 2D          | ICR29           | 348 <sub>H</sub> | 000FFF48 <sub>H</sub> |
| Reserved by system    | 46               | 2E          | ICR30           | 344 <sub>H</sub> | 000FFF44 <sub>H</sub> |
| Reserved by system    | 47               | 2F          | ICR31           | 340 <sub>H</sub> | 000FFF40 <sub>H</sub> |
| PPG0                  | 48               | 30          | ICR32           | 33C <sub>H</sub> | 000FFF3C <sub>H</sub> |
| PPG1                  | 49               | 31          | ICR33           | 338 <sub>H</sub> | 000FFF38 <sub>H</sub> |
| PPG2                  | 50               | 32          | ICR34           | 334 <sub>H</sub> | 000FFF34 <sub>H</sub> |
| PPG3                  | 51               | 33          | ICR35           | 330 <sub>H</sub> | 000FFF30 <sub>H</sub> |
| ICU0 (capture)        | 52               | 34          | ICR36           | 32C <sub>H</sub> | 000FFF2C <sub>H</sub> |
| ICU1 (capture)        | 53               | 35          | ICR37           | 328 <sub>H</sub> | 000FFF28 <sub>H</sub> |
| ICU2 (capture)        | 54               | 36          | ICR38           | 324 <sub>H</sub> | 000FFF24 <sub>H</sub> |
| ICU3 (capture)        | 55               | 37          | ICR39           | 320 <sub>H</sub> | 000FFF20 <sub>H</sub> |

(Continued)

# MB91F127/F128

(Continued)

| Interrupt causes                          | Interrupt number |                | Interrupt level |  | TBR default Address*2                               |
|---|------------------|----------------|-----------------|--|---|
|   | Decimal          | Hexadecimal    | Register*1      | Offset                                     |   |
| OCU0 (match)                              | 56               | 38             | ICR40           | 31C <sub>H</sub>                           | 000FFF1C <sub>H</sub>                               |
| OCU1 (match)                              | 57               | 39             | ICR41           | 318 <sub>H</sub>                           | 000FFF18 <sub>H</sub>                               |
| OCU2 (match)                              | 58               | 3A             | ICR42           | 314 <sub>H</sub>                           | 000FFF14 <sub>H</sub>                               |
| OCU3 (match)                              | 59               | 3B             | ICR43           | 310 <sub>H</sub>                           | 000FFF10 <sub>H</sub>                               |
| Reserved by system                        | 60               | 3C             | ICR44           | 30C <sub>H</sub>                           | 000FFF0C <sub>H</sub>                               |
| 16 bit free-run timer                     | 61               | 3D             | ICR45           | 308 <sub>H</sub>                           | 000FFF08 <sub>H</sub>                               |
| Reserved by system                        | 62               | 3E             | ICR46           | 304 <sub>H</sub>                           | 000FFF04 <sub>H</sub>                               |
| Delay interrupt cause bit                 | 63               | 3F             | ICR47           | 300 <sub>H</sub>                           | 000FFF00 <sub>H</sub>                               |
| Reserved by system<br>(used by REALOS) *3 | 64               | 40             | —               | 2FC <sub>H</sub>                           | 000FFEFC <sub>H</sub>                               |
| Reserved by system<br>(used by REALOS) *3 | 65               | 41             | —               | 2F8 <sub>H</sub>                           | 000FFE8 <sub>H</sub>                                |
| Used by INT                               | 66<br>to<br>255  | 42<br>to<br>FF | —               | 2F4 <sub>H</sub><br>to<br>000 <sub>H</sub> | 000FEF4 <sub>H</sub><br>to<br>000FFC00 <sub>H</sub> |

\*1 : ICR specifies interrupt levels for interrupt requests, using the registers in interrupt controller.  
ICR is provided for each interrupt request.

\*2 : TBR is a register that indicates a head address of the vector table for EIT.  
An address that is found by adding offset values defined by TBR and EIT cause, is a vector address.

\*3 : If REALOS/FR is used, 0x40 and 0x41 interrupts are used for system code.

Information : An 1 Kbyte area starting with an address indicated by TBR is the vector area for EIT. Size of the area for one vector is 4 byte. Relation between a vector number and a vector address is as follows:

$$\begin{aligned} \text{vctadr} &= \text{TBR} + \text{vctofs} \\ &= \text{TBR} + (3\text{FC}_{\text{H}} - 4 \times \text{vct}) \end{aligned}$$

Vctadr Vector address, vctofs: Vector offset, vct: Vector number



## ■ ELECTRICAL CHARACTERISTICS

### 1. Absolute Maximum Ratings

( $V_{SS} = AV_{SS} = 0\text{ V}$ )

| Parameter                              | Symbol               | Rating         |                 | Unit | Remarks |
|--|----------------------|----------------|-----------------|------|---------|
|  |                      | Min            | Max             |      |         |
| Power supply voltage                   | $V_{CC}$             | $V_{SS} - 0.3$ | $V_{SS} + 4.0$  | V    |         |
| Analog supply voltage                  | $AV_{CC}$            | $V_{SS} - 0.3$ | $V_{SS} + 4.0$  | V    | *1      |
| Analog reference voltage               | $AVRH$               | $V_{SS} - 0.3$ | $V_{SS} + 4.0$  | V    | *1      |
| Input voltage                          | $V_I$                | $V_{SS} - 0.3$ | $V_{CC} + 0.3$  | V    |         |
| Analog input voltage                   | $V_{IA}$             | $V_{SS} - 0.3$ | $AV_{CC} + 0.3$ | V    |         |
| Output voltage                         | $V_O$                | $V_{SS} - 0.3$ | $V_{CC} + 0.3$  | V    |         |
| Maximum clamp current                  | $I_{CLAMP}$          | -2.0           | +2.0            | mA   | *5      |
| Total maximum clamp current            | $\Sigma  I_{CLAMP} $ | —              | 20              | mA   | *5      |
| “L” level maximum output current       | $I_{OL}$             | —              | 10              | mA   | *2      |
| “L” level average output current       | $I_{OLAV}$           | —              | 4               | mA   | *3      |
| “L” level maximum total output current | $\Sigma I_{OL}$      | —              | 100             | mA   |         |
| “L” level average total output current | $\Sigma I_{OLAV}$    | —              | 50              | mA   | *4      |
| “H” level maximum output current       | $I_{OH}$             | —              | -10             | mA   | *2      |
| “H” level average output current       | $I_{OHAV}$           | —              | -4              | mA   | *3      |
| “H” level maximum total output current | $\Sigma I_{OH}$      | —              | -50             | mA   |         |
| “H” level average total output current | $\Sigma I_{OHAV}$    | —              | -20             | mA   | *4      |
| Power consumption                      | $P_d$                | —              | 500             | mW   |         |
| Operating temperature                  | $T_A$                | -30            | +70             | °C   |         |
| Storage temperature                    | $T_{stg}$            | -55            | +150            | °C   |         |

\*1 : Care must be taken that  $AV_{CC}$ ,  $AVRH$  do not exceed  $V_{CC} + 0.3\text{ V}$ . Also, care must be taken that  $AVRH$  do not exceed  $AV_{CC}$ .

\*2 : Maximum output current defines a peak value of a specific terminal.

\*3 : Average output current defines a mean value of current flow within a period of 100 ms in a specific terminal.

\*4 : Average total output current defines a mean value of current flow within a period of 100 ms in all terminals.

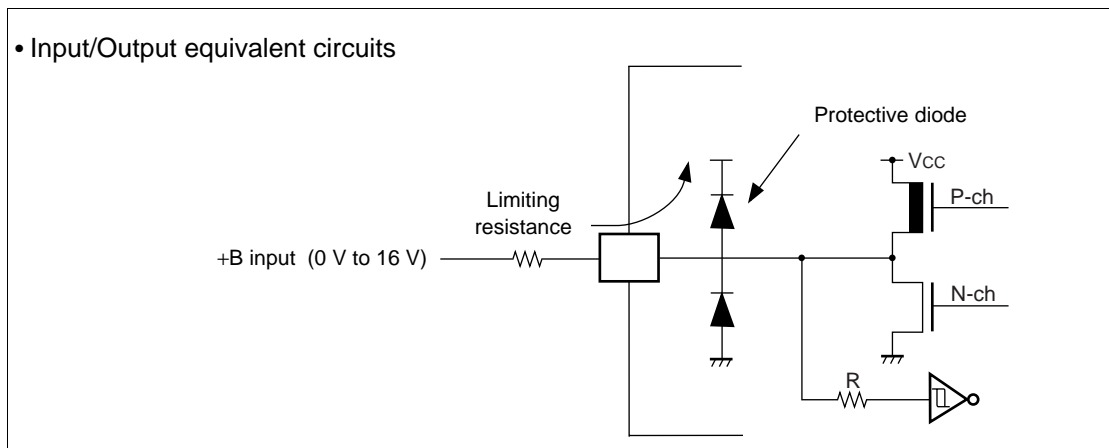
\*5 : • Applicable to pins : D16 to D31, A00 to A24, RDY,  $\overline{BGRNT}$ , BRQ,  $\overline{RD}$ ,  $\overline{WR0}$ ,  $\overline{WR1}$ ,  $\overline{CS0}$  to  $\overline{CS5}$ , CLK, OCPA0 to OCPA3, OC0 to OC3, ALE, INT0 to INT5, SI0, SI2, SO0, SO2, TCI0, SC2

- Use within recommended operating conditions.
- Use at DC voltage (current) .
- The +B signal should always be applied with a limiting resistance placed between the +B signal and the microcontroller.

# MB91F127/F128

(Continued)

- The value of the limiting resistance should be set so that when the signal is applied the input current to the microcontroller pins does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the VCC pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V), the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on reset.
- Care must be taken not to leave the input pin open.
- Sample recommended circuits



**WARNING:** Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

## 2. Recommended Operating Conditions

( $V_{SS} = AV_{SS} = 0\text{ V}$ )

| Parameter                | Symbol    | Value          |                | Unit | Remarks                                |
|--------------------------|-----------|----------------|----------------|------|--|
|                          |           | Min            | Max            |      |  |
| Power supply             | $V_{CC}$  | 3.0            | 3.6            | V    | Normal operation                       |
|                          |           | 2.0            | 3.6            |      | Retain RAM data under "stop" condition |
| Analog supply voltage    | $AV_{CC}$ | $V_{SS} - 0.3$ | $V_{SS} + 3.6$ | V    |  |
| Analog reference voltage | $AV_{RH}$ | $AV_{SS}$      | $AV_{CC}$      | V    |  |
| Operating temperature    | $T_A$     | -30            | +70            | °C   |  |

**WARNING:** The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

# MB91F127/F128

## 3. DC Characteristics

( $AV_{CC} = V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  $AV_{SS} = V_{SS} = 0 \text{ V}$ ,  $T_A = -30 \text{ }^\circ\text{C}$  to  $+70 \text{ }^\circ\text{C}$ )

| Parameter                | Symbol    | Pin name                              | Condition   | Value               |     |                     | Unit          | Remarks       |
|--------------------------|-----------|---------------------------------------|---|---------------------|-----|---------------------|---------------|---------------|
|                          |           |                                       |   | Min                 | Typ | Max                 |               |               |
| "H" level input voltage  | $V_{IHS}$ | Hysteresis input terminal             | —   | $0.8 \times V_{CC}$ | —   | $V_{CC} + 0.3$      | V             | *             |
| "L" level input voltage  | $V_{ILS}$ | Hysteresis input terminal             | —   | $V_{SS} - 0.3$      | —   | $0.2 \times V_{CC}$ | V             | *             |
| "H" level output voltage | $V_{OH}$  | Port2 to PortJ                        | $V_{CC} = 3.3 \text{ V}$<br>$I_{OH} = -4.0 \text{ mA}$        | $V_{CC} - 0.5$      | —   | —                   | V             |               |
| "L" level output voltage | $V_{OL}$  | Port2 to PortJ                        | $V_{CC} = 3.3 \text{ V}$<br>$I_{OL} = 4.0 \text{ mA}$         | —                   | —   | 0.4                 | V             |               |
| Input leak current       | $I_{LI}$  | Port2 to PortJ                        | $V_{CC} = 3.6 \text{ V}$<br>$V_{SS} < V_I < V_{CC}$           | —                   | —   | $\pm 5$             | $\mu\text{A}$ |               |
| Power supply current     | $I_{CC}$  | VCC                                   | 25 MHz<br>$V_{CC} = 3.3 \text{ V}$                            | —                   | 75  | 100                 | mA            |               |
|                          | $I_{CC}$  |                                       | 25 MHz<br>$V_{CC} = 3.3 \text{ V}$                            | —                   | 85  | 120                 | mA            | FLASH writing |
|                          | $I_{CCS}$ |                                       | 25 MHz<br>$V_{CC} = 3.3 \text{ V}$                            | —                   | 60  | 85                  | mA            | Sleeping      |
|                          | $I_{CCH}$ |                                       | $T_A = 25 \text{ }^\circ\text{C}$<br>$V_{CC} = 3.3 \text{ V}$ | —                   | 10  | 150                 | $\mu\text{A}$ | Stopping      |
| Input capacity           | $C_{IN}$  | Other than AVCC, AVSS, AVRH, VCC, VSS | —   | —                   | 10  | —                   | pF            |               |

\* : Refer to "■ INPUT/OUTPUT CIRCUIT TYPE".

## 4. AC Characteristics

### (1) Clock Timing Ratings

(V<sub>CC</sub> = 3.3 V ± 0.3 V, AV<sub>SS</sub> = V<sub>SS</sub> = 0 V, T<sub>A</sub> = -30 °C to +70 °C)

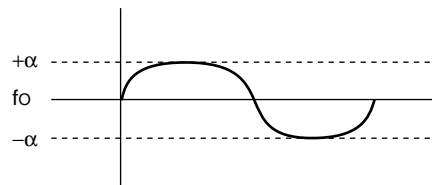
| Parameter  | Symbol                             | Condition         | Value          |         | Unit | Remarks   |    |
|--|------------------------------------|-------------------|----------------|---------|------|---|----|
|  |                                    |                   | Min            | Max     |      |   |    |
| Clock frequency<br>(High speed, automatic oscillation) | f <sub>c</sub>                     | —                 | 10             | 25      | MHz  | Self oscillation allowable range  |    |
| Clock frequency<br>(High speed, PLL used)              |                                    |                   | 10             | 25      | MHz  | PLL-use allowable area for self oscillation and external clock input *1 |    |
| Clock frequency<br>(High speed, 1/2 division input)    |                                    |                   | 10             | 25      | MHz  | External clock input allowable range                                    |    |
| Clock cycle time                                       |                                    |                   | t <sub>c</sub> | 40      | 100  | ns  |    |
| Frequency regulation<br>(when locked)                  |                                    |                   | Δf             | —       | 10   | %   | *2 |
| Input clock pulse width                                | P <sub>WH</sub> , P <sub>WL</sub>  | —                 | 9.5            | —       | ns   |   |    |
| Input clock rise and fall time                         | t <sub>CR</sub><br>t <sub>CF</sub> | —                 | —              | 8       | ns   | (t <sub>CR</sub> + t <sub>CF</sub> )                                    |    |
| Internal operation clock frequency                     | CPU system                         | f <sub>CP</sub>   | 0.625 *3       | 25      | MHz  |   |    |
|  | Peripheral system                  | f <sub>CPP</sub>  | 0.625 *3       | 25      | MHz  |   |    |
| Internal operation clock cycle time                    | CPU system                         | t <sub>CP</sub>   | 40             | 1600 *3 | ns   |   |    |
|  | Peripheral system                  | t <sub>LCPP</sub> | 40             | 1600 *3 | ns   |   |    |

\*1 : Although PLL allows selection among x1 and x2 multiplication modes, the selection is limited by oscillation frequency as follows:

Specifying "x2 multiplication" is not allowed if oscillation frequency exceeds 12.5 MHz.

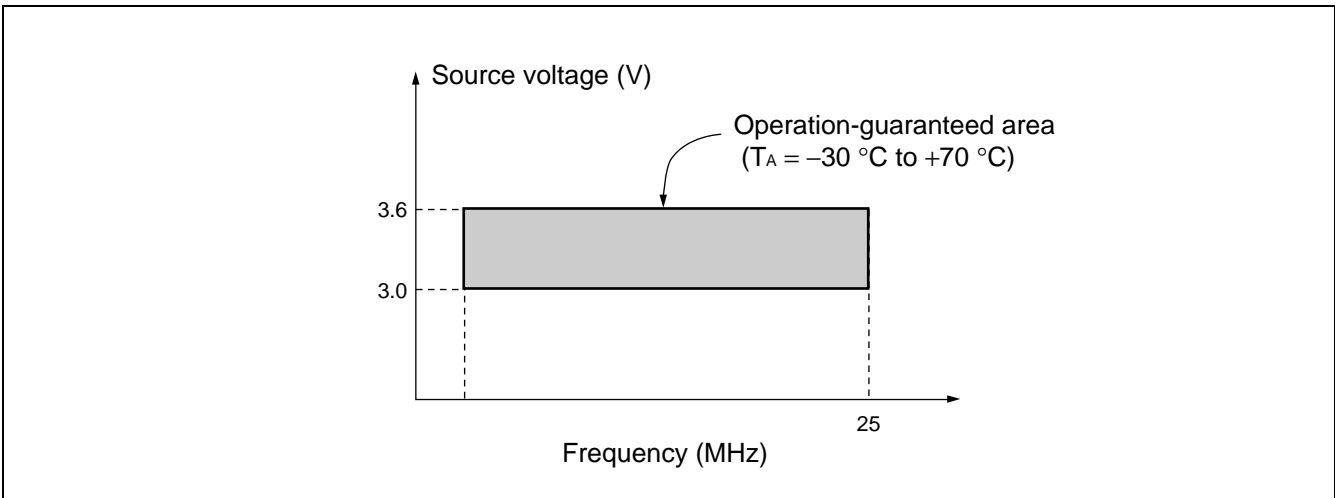
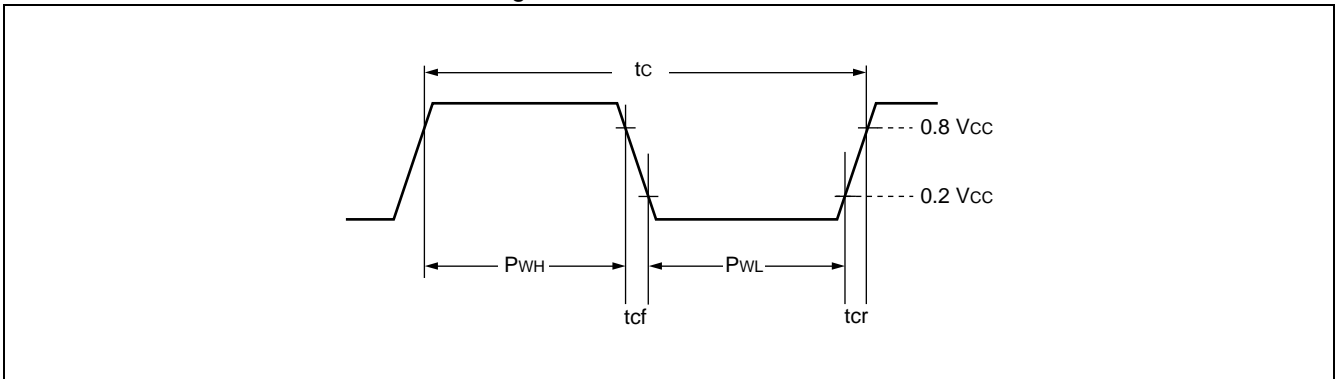
\*2 : Frequency regulation indicates a maximum fluctuation from a specified center frequency under locked frequency multiplication.

$$\Delta f = \frac{|\alpha|}{f_0} \times 100 (\%)$$



# MB91F127/F128

\*3 : This is a value in the case where 10 MHz signal, a minimum value of clock frequency, is input to X0 and where 1/2-division in oscillation circuit and 1/8-gear are used.



## (2) Clock Output Timing

( $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $T_A = -30\text{ }^\circ\text{C}$  to  $+70\text{ }^\circ\text{C}$ )

| Parameter                                     | Symbol     | Pin name | Condition | Value                     |                           | Unit | Remarks |
|---|------------|----------|-----------|---------------------------|---------------------------|------|---------|
|   |            |          |           | Min                       | Max                       |      |         |
| Cycle time                                    | $t_{CYC}$  | CLK      | —         | $t_{CP}$                  | —                         | ns   | *1      |
| CLK $\uparrow$ $\rightarrow$ CLK $\downarrow$ | $t_{CHCL}$ | CLK      |           | $1/2 \times t_{CYC} - 10$ | $1/2 \times t_{CYC} + 10$ | ns   | *2      |
| CLK $\downarrow$ $\rightarrow$ CLK $\uparrow$ | $t_{CLCH}$ | CLK      |           | $1/2 \times t_{CYC} - 10$ | $1/2 \times t_{CYC} + 10$ | ns   | *3      |

\*1 :  $t_{CYC}$  is a frequency of 1 clock cycle indicating gear cycle.

\*2 : The values indicate specifications where x1 gear cycle is used.

If gear cycle of 1/2, 1/4, or 1/8 is specified, calculate in the formula below by substituting 1/2, 1/4, or 1/8 into n.

$$\text{Min : } (1 - n / 2) \times t_{CYC} - 10$$

$$\text{Max : } (1 - n / 2) \times t_{CYC} + 10$$

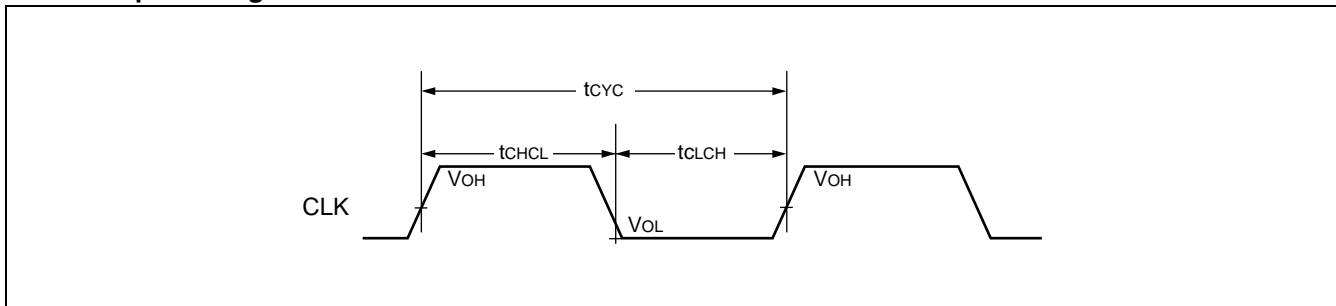
\*3 : The values indicate specifications where x1 gear cycle is used.

If gear cycle of 1/2, 1/4, or 1/8 is specified, calculate in the formula below by substituting 1/2, 1/4, or 1/8 into n.

$$\text{Min : } n / 2 \times t_{CYC} - 10$$

$$\text{Max : } n / 2 \times t_{CYC} + 10$$

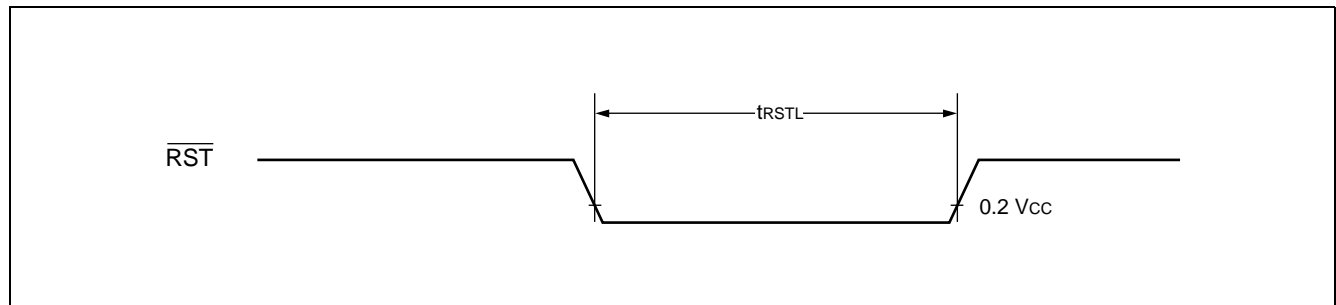
### Clock output timing



## (3) Reset Input Ratings

( $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $T_A = -30\text{ }^\circ\text{C}$  to  $+70\text{ }^\circ\text{C}$ )

| Parameter        | Symbol     | Pin name                | Condition | Value             |     | Unit | Remarks |
|------------------|------------|-------------------------|-----------|-------------------|-----|------|---------|
|                  |            |                         |           | Min               | Max |      |         |
| Reset input time | $t_{RSTL}$ | $\overline{\text{RST}}$ | —         | $t_{CP} \times 5$ | —   | ns   |         |

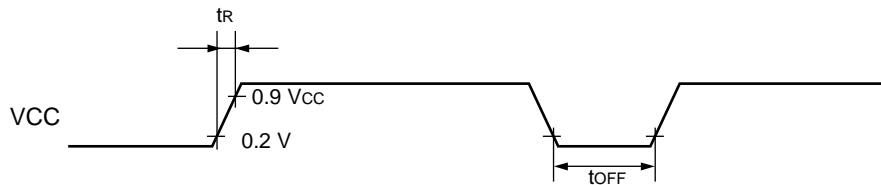


# MB91F127/F128

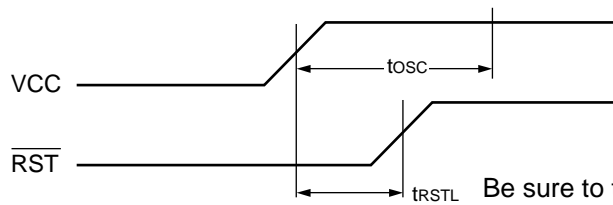
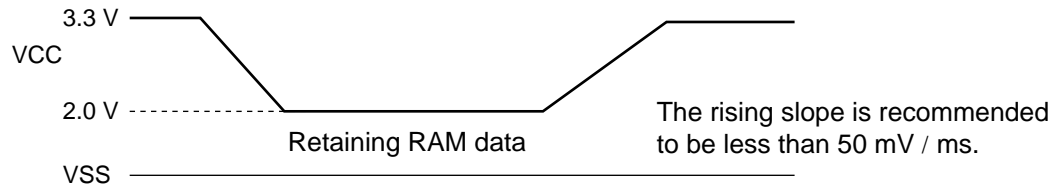
## (4) Power-on Reset

( $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $T_A = -30\text{ }^\circ\text{C}$  to  $+70\text{ }^\circ\text{C}$ )

| Parameter                         | Symbol    | Pin name | Condition               | Value   |     | Unit | Remarks   |
|-----------------------------------|-----------|----------|-------------------------|---|-----|------|---|
|                                   |           |          |                         | Min   | Max |      |   |
| Power supply rise time            | $t_R$     | VCC      | $V_{CC} = 3.3\text{ V}$ | —   | 20  | ms   | $V_{CC} < 0.2\text{ V}$ before turning on power |
| Power supply shut off time        | $t_{OFF}$ | VCC      | —                       | 2   | —   | ms   |   |
| Oscillation stabilizing wait time | $t_{OSC}$ | —        | —                       | $2 \times t_c \times 2^{21} + 100\text{ }\mu\text{s}$ | —   | ns   |   |



A sudden change of supply voltage may activate the power-on reset function. It is recommended that power voltage should be changed smoothly with less fluctuation of voltages.



Be sure to turn on the power while keeping  $\overline{\text{RST}}$  terminal at L level first. When the power becomes  $V_{CC}$  level, rise the voltage to H level after a period of  $t_{RSTL}$ .



## (5) Normal Bus Access Read/Write Operation

( $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $T_A = -30\text{ }^\circ\text{C}$  to  $+70\text{ }^\circ\text{C}$ )

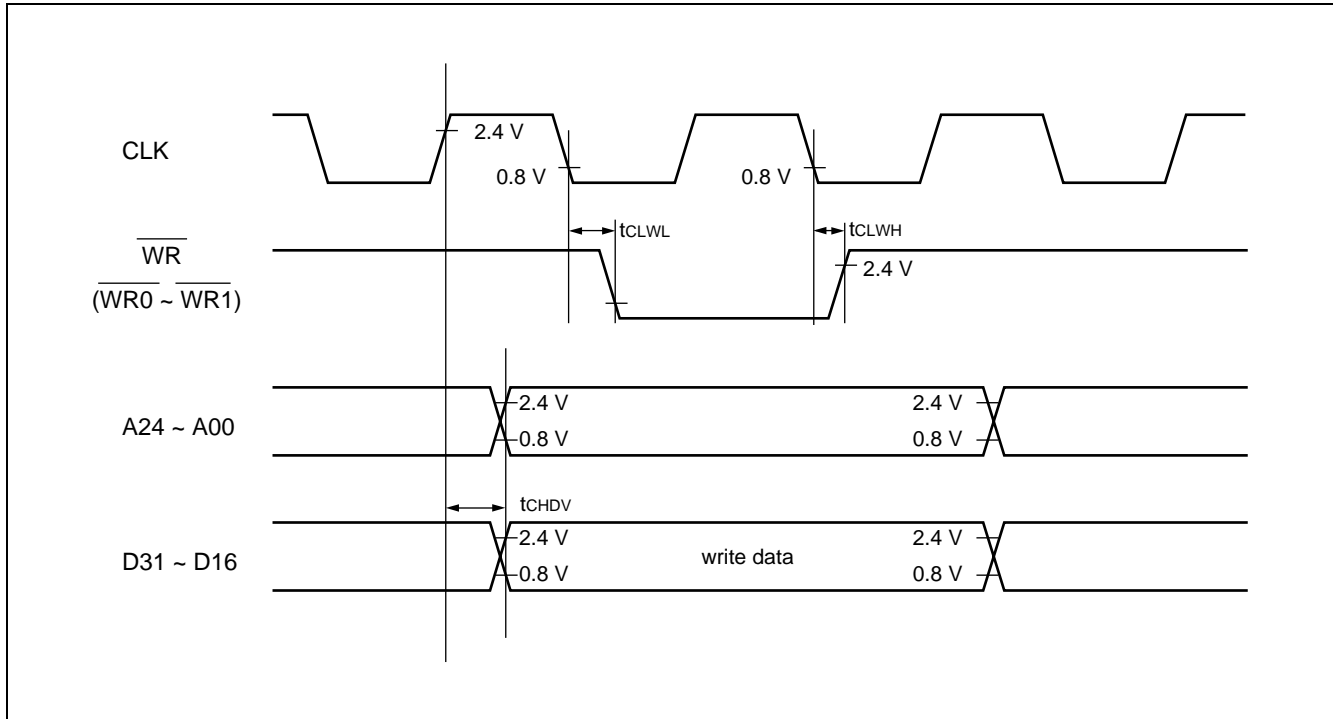
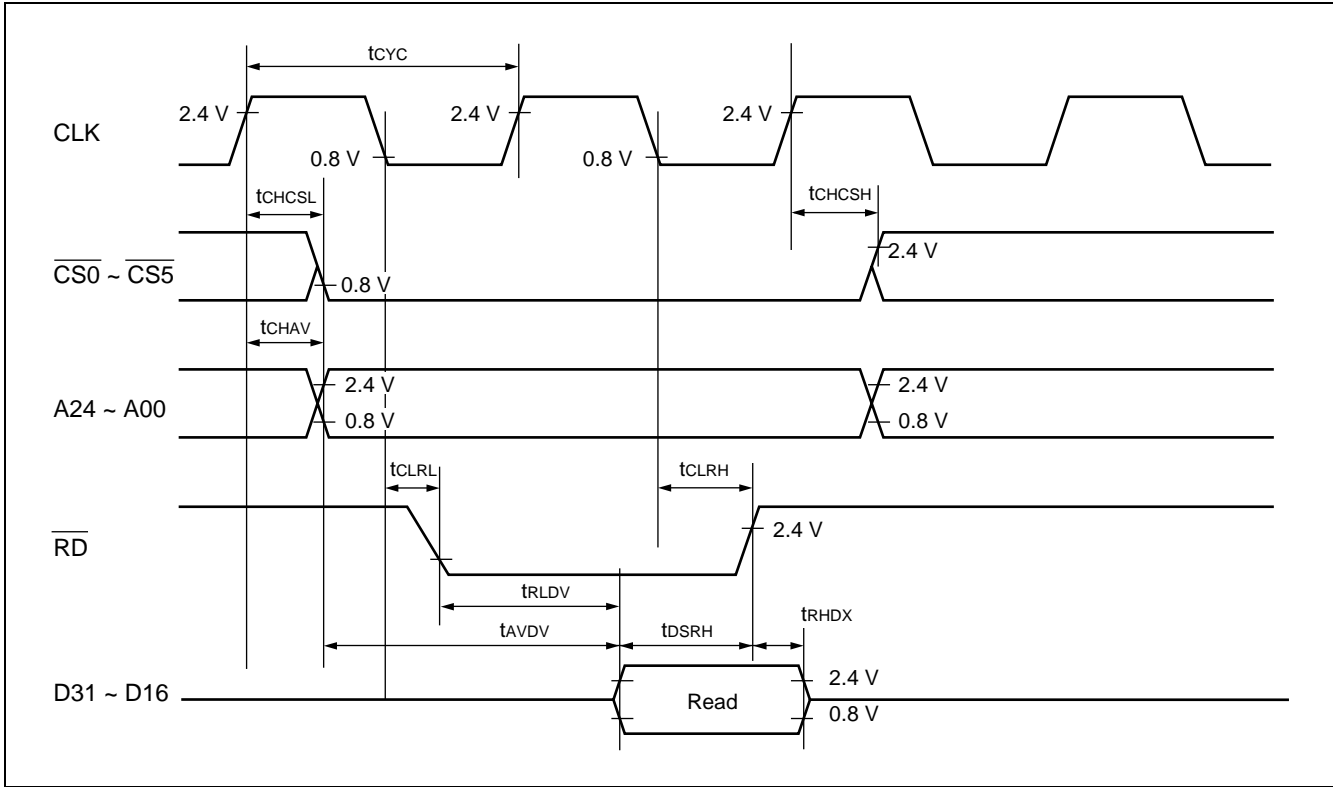
| Parameter   | Symbol      | Pin name                              | Condition | Value |                           | Unit | Remarks  |
|---|-------------|---------------------------------------|-----------|-------|---------------------------|------|----------|
|   |             |                                       |           | Min   | Max                       |      |          |
| CS0 to CS5 delay time   | $t_{CHCSL}$ | CLK                                   | —         | —     | 15                        | ns   |          |
| CS0 to CS5 delay time   | $t_{CHCSH}$ | $\overline{CS0}$ to $\overline{CS5}$  |           | —     | 15                        | ns   |          |
| Address delay time  | $t_{CHAV}$  | CLK<br>A24 to A00                     |           | —     | 15                        | ns   |          |
| Data delay time   | $t_{CHDV}$  | CLK<br>D31 to D16                     |           | —     | 15                        | ns   |          |
| $\overline{RD}$ delay time                                    | $t_{CLRRL}$ | CLK<br>RD                             |           | —     | 15                        | ns   |          |
| $\overline{RD}$ delay time                                    | $t_{CLRHL}$ |                                       |           | —     | 15                        | ns   |          |
| $\overline{WR0}, \overline{1}$ delay time                     | $t_{CLWL}$  | CLK<br>$\overline{WR0}, \overline{1}$ |           | —     | 15                        | ns   |          |
| $\overline{WR0}, \overline{1}$ delay time                     | $t_{CLWH}$  |                                       |           | —     | 15                        | ns   |          |
| Valid address→<br>Valid data input time                       | $t_{AVDV}$  | A24 to A00<br>D31 to D16              |           | —     | $3/2 \times t_{cyc} - 25$ | ns   | *1<br>*2 |
| $\overline{RD}\downarrow\rightarrow$<br>Valid data input time | $t_{RLDV}$  | $\overline{RD}$<br>D31 to D16         |           | —     | $t_{cyc} - 25$            | ns   | *1       |
| Data setup<br>→ $\overline{RD}\uparrow$ Time                  | $t_{DSRH}$  |                                       |           | 25    | —                         | ns   |          |
| $\overline{RD}\uparrow\rightarrow$<br>Data hold time          | $t_{RHDX}$  |                                       |           | 0     | —                         | ns   |          |

\*1 : If the bus is expanded by automatic wait insertion or RDY input, add time ( $t_{cyc} \times$  the number of expanded cycles) to the rated value.

\*2 : The ratings are based on conditions with "gear cycle  $\times 1$ ". If gear cycle of 1/2, 1/4, or 1/8 is specified, calculate in the formula below by substituting 1/2, 1/4, or 1/8 into n.

Formula :  $(2 - n / 2) \times t_{cyc} - 25$

# MB91F127/F128



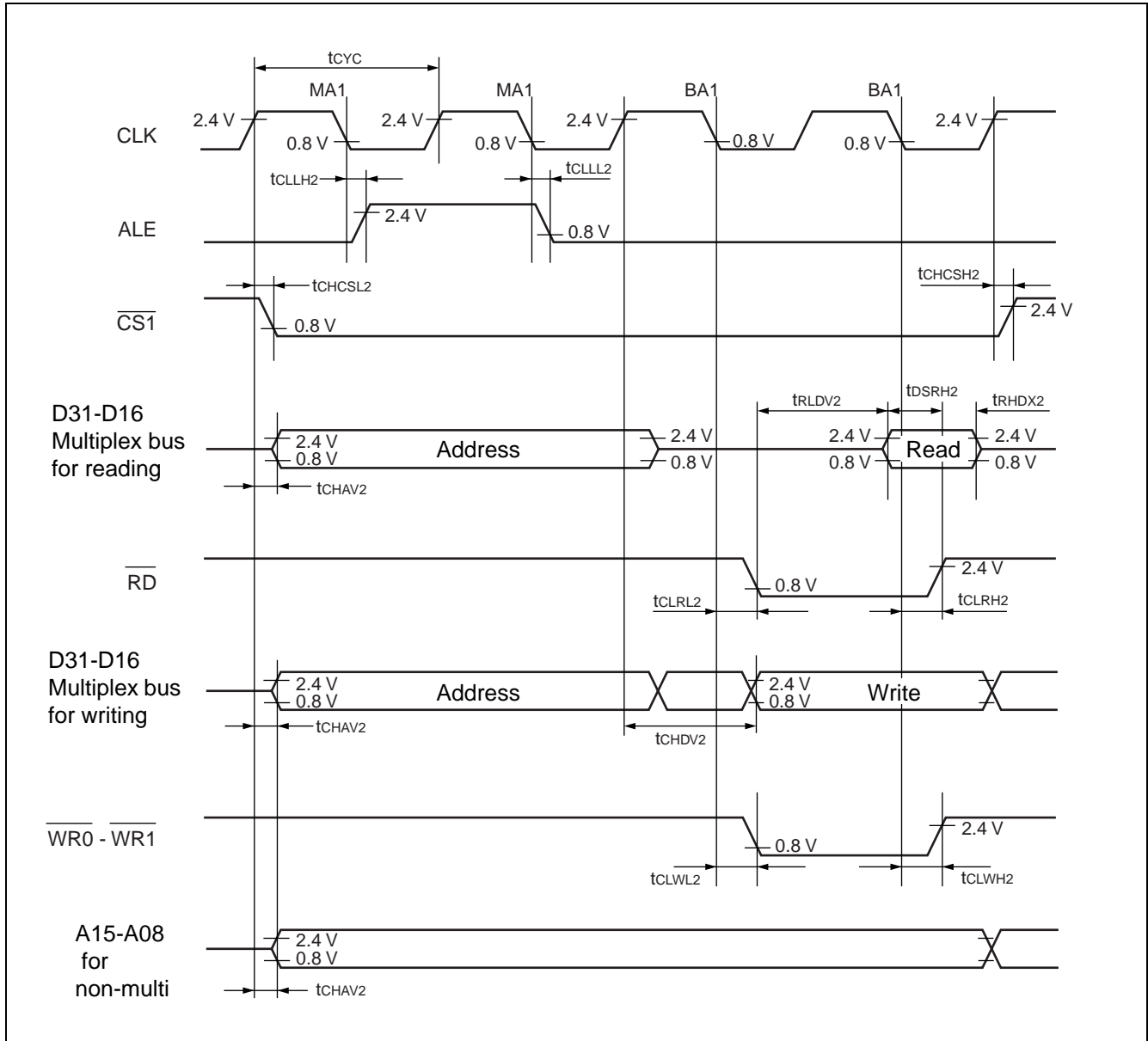
## (6) Timeshared Bus Access Read/Write Operations

( $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $T_A = -30\text{ }^\circ\text{C}$  to  $+70\text{ }^\circ\text{C}$ )

| Parameter  | Symbol       | Pin name   | Condition | Value |                | Unit | Remarks |
|--|--------------|--|-----------|-------|----------------|------|---------|
|  |              |  |           | Min   | Max            |      |         |
| ALE delay time   | $t_{CLLH2}$  | CLK  | —         | —     | 10             | —    |         |
| ALE delay time   | $t_{CLLL2}$  | ALE  |           | —     | 10             | —    |         |
| $\overline{\text{CS1}}$ delay time                                   | $t_{CHCSL2}$ | CLK  |           | —     | 15             | —    |         |
| $\overline{\text{CS1}}$ delay time                                   | $t_{CHCSH2}$ | $\overline{\text{CS1}}$                            |           | —     | 15             | ns   |         |
| Address delay time   | $t_{CHAV2}$  | CLK  |           | —     | 15             | ns   |         |
| Data delay time  | $t_{CHDV2}$  | D31 to D16   |           | —     | 15             | ns   |         |
| $\overline{\text{RD}}$ delay time                                    | $t_{CLRL2}$  | CLK  |           | —     | 10             | ns   |         |
| $\overline{\text{RD}}$ delay time                                    | $t_{CLRH2}$  | $\overline{\text{RD}}$                             |           | —     | 10             | ns   |         |
| $\overline{\text{WR0}}, \overline{1}$ delay time                     | $t_{CLWL2}$  | CLK  |           | —     | 10             | ns   |         |
| $\overline{\text{WR0}}, \overline{1}$ pulse width                    | $t_{CLWH2}$  | $\overline{\text{WR0}}$<br>$\overline{\text{WR1}}$ |           | —     | 10             | ns   |         |
| $\overline{\text{RD}}\downarrow\rightarrow$<br>Valid data input time | $t_{RLDV2}$  | $\overline{\text{RD}}$<br>D31 to D16               |           | —     | $t_{cyc} - 25$ | —    | *       |
| Data setup<br>$\rightarrow\overline{\text{RD}}\uparrow$ time         | $t_{DSRH2}$  |  |           | 25    | —              | ns   |         |
| $\overline{\text{RD}}\uparrow\rightarrow$<br>Data hold time          | $t_{RHDX2}$  |  |           | 0     | —              | ns   |         |

\* : If the bus is expanded by automatic wait insertion or RDY input, add time ( $t_{cyc} \times$  the number of expanded cycles) to the rated value.

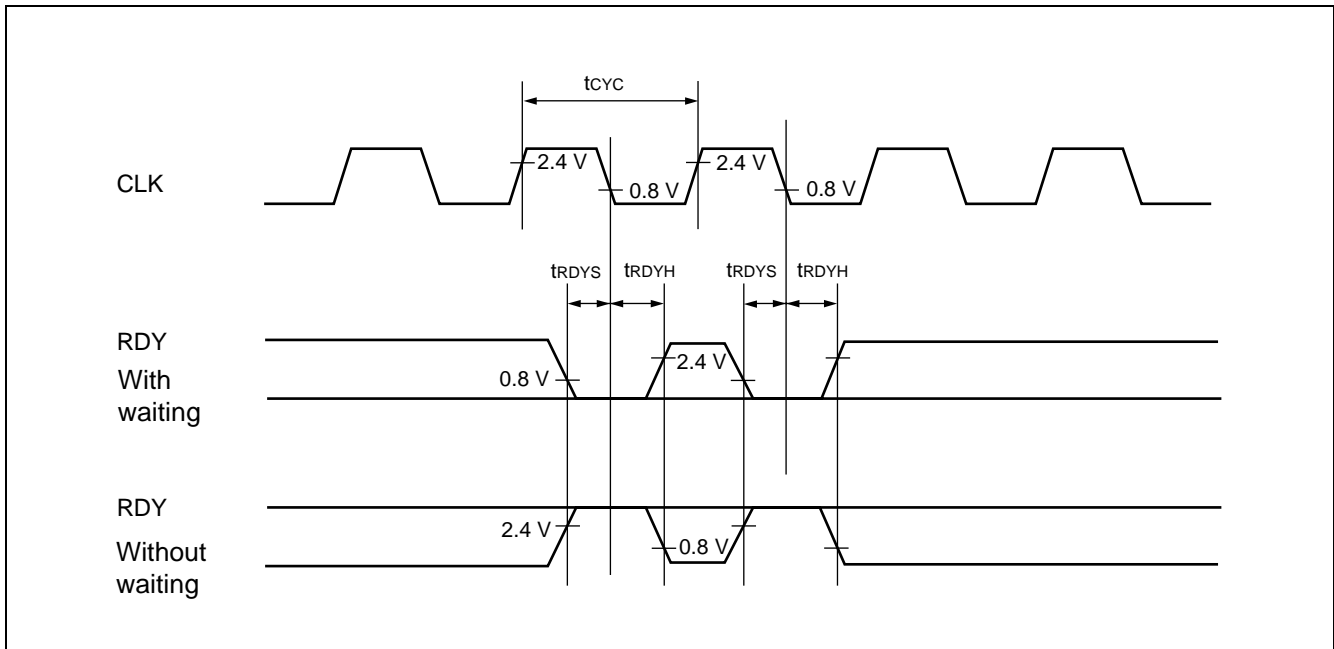
# MB91F127/F128



## (7) Ready Input Timing

( $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $AV_{SS} = V_{SS} = 0\text{ V}$ ,  $T_A = -30\text{ }^{\circ}\text{C}$  to  $+70\text{ }^{\circ}\text{C}$ )

| Parameter               | Symbol     | Pin name   | Condition | Value |     | Unit | Remarks |
|-------------------------|------------|------------|-----------|-------|-----|------|---------|
|                         |            |            |           | Min   | Max |      |         |
| RDY setup time<br>RCLK↓ | $t_{RDYS}$ | RDY<br>CLK | —         | 15    | —   | ns   |         |
| CLK↓→<br>RDY hold time  | $t_{RDYH}$ | CLK<br>RDY |           | 0     | —   | ns   |         |



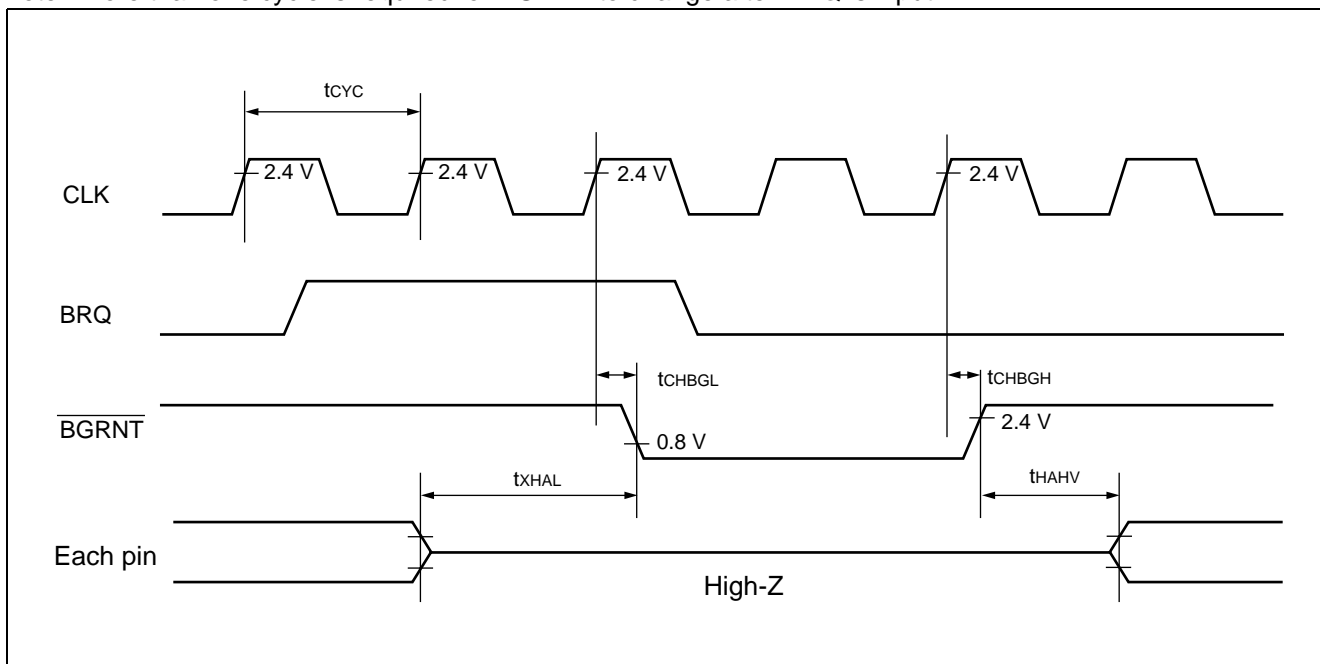
# MB91F127/F128

## (8) Hold Timing

( $V_{CC} = 3.0\text{ V} \pm 0.3\text{ V}$ ,  $AV_{SS} = V_{SS} = 0\text{ V}$ ,  $T_A = -30\text{ }^\circ\text{C}$  to  $+70\text{ }^\circ\text{C}$ )

| Parameter                                   | Symbol      | Pin name              | Condition | Value          |                | Unit | Remarks |
|---|-------------|-----------------------|-----------|----------------|----------------|------|---------|
|   |             |                       |           | Min            | Max            |      |         |
| BGRNT $\bar{}$ delay time                   | $t_{CHBGL}$ | CLK<br>BGRNT $\bar{}$ | —         | —              | 10             | ns   |         |
| BGRNT $\bar{}$ delay time                   | $t_{CHBGH}$ |                       |           | —              | 10             | ns   |         |
| Terminal floating<br>→BGRNT $\bar{}$ ↓ time | $t_{XHAL}$  | BGRNT $\bar{}$        |           | $t_{CYC} - 10$ | $t_{CYC} + 10$ | ns   |         |
| BGRNT $\bar{}$ ↑<br>→Terminal valid time    | $t_{HAHV}$  |                       |           | $t_{CYC} - 10$ | $t_{CYC} + 10$ | ns   |         |

Note : More than one cycle is required for BGRNT $\bar{}$  to change after BRQ is input.



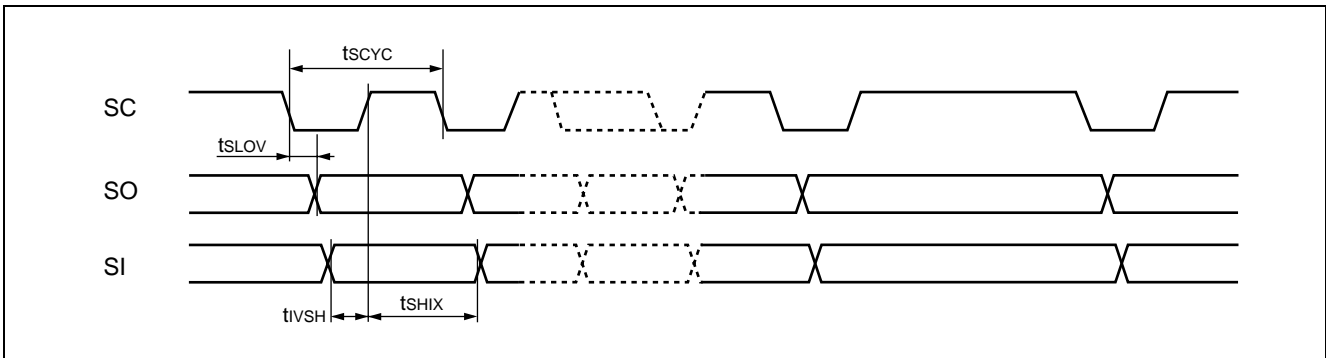
## (9) UART Timing

( $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $T_A = -30\text{ }^\circ\text{C}$  to  $+70\text{ }^\circ\text{C}$ )

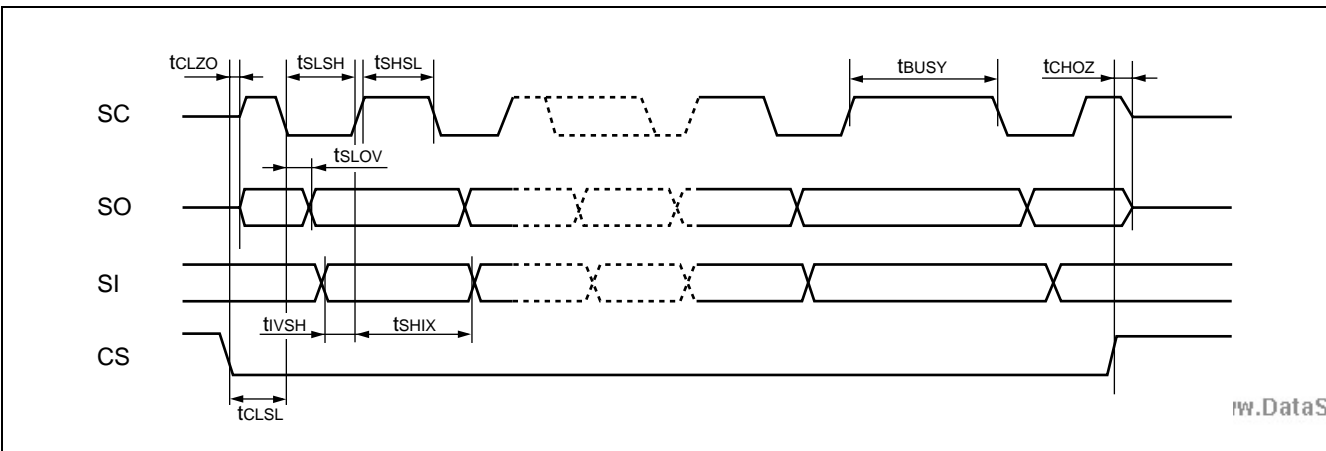
| Parameter  | Symbol     | Pin name | Condition                 | Value               |                | Unit | Remarks |
|--|------------|----------|---------------------------|---------------------|----------------|------|---------|
|  |            |          |                           | Min                 | Max            |      |         |
| Serial clock cycle time                          | $t_{SCYC}$ | —        | Internal shift clock mode | $8 t_{CYCP}^*$      | —              | ns   |         |
| SC $\downarrow$ $\rightarrow$ SO delay time      | $t_{SLOV}$ | —        |                           | -10                 | +50            | ns   |         |
| Valid SI $\rightarrow$ SC $\uparrow$             | $t_{IVSH}$ | —        |                           | 50                  | —              | ns   |         |
| SC $\uparrow$ $\rightarrow$ Valid SI hold time   | $t_{SHIX}$ | —        |                           | 50                  | —              | ns   |         |
| Serial clock "H" pulse width                     | $t_{SHSL}$ | —        | External shift clock mode | $4 t_{CYCP}^* - 10$ | —              | ns   |         |
| Serial clock "L" pulse width                     | $t_{LSLH}$ | —        |                           | $4 t_{CYCP}^* - 10$ | —              | ns   |         |
| SC $\downarrow$ $\rightarrow$ SO delay time      | $t_{SLOV}$ | —        |                           | 0                   | 50             | ns   |         |
| Valid SI $\rightarrow$ SC $\uparrow$             | $t_{IVSH}$ | —        |                           | 50                  | —              | ns   |         |
| SC $\uparrow$ $\rightarrow$ Valid SI hold time   | $t_{SHIX}$ | —        |                           | 50                  | —              | ns   |         |
| Serial busy time                                 | $t_{BUSY}$ | —        |                           | —                   | $6 t_{CYCP}^*$ | ns   |         |
| CS $\downarrow$ $\rightarrow$ SC, SO delay time  | $t_{CLZO}$ | —        |                           | —                   | 50             | ns   |         |
| CS $\downarrow$ $\rightarrow$ SC input mask time | $t_{CLSL}$ | —        |                           | —                   | $3 t_{CYCP}^*$ | ns   |         |
| SC $\uparrow$ $\rightarrow$ SC, SO Hi-z time     | $t_{CHOZ}$ | —        | —                         | 50                  | ns             |      |         |

\* :  $t_{CYCP}$  is a cycle time of peripheral system clock.

### Internal shift clock mode



### External shift clock mode



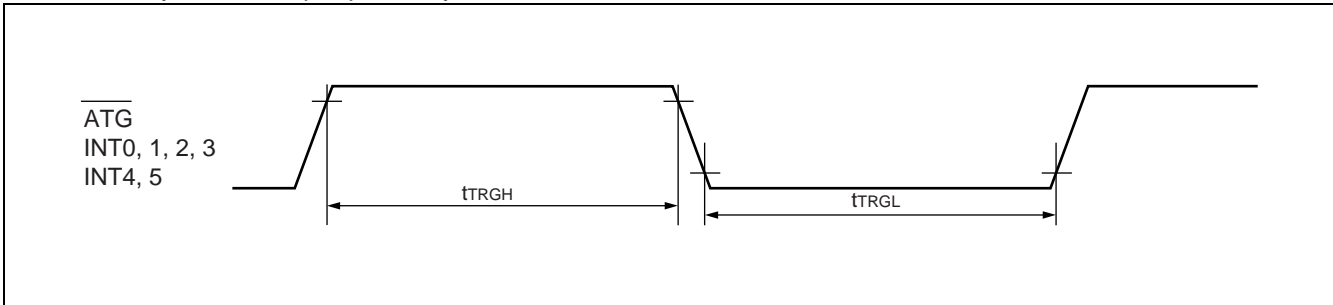
# MB91F127/F128

## (10) Trigger Input Timing

( $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $T_A = -30\text{ }^\circ\text{C}$  to  $+70\text{ }^\circ\text{C}$ )

| Parameter         | Symbol                   | Pin name  | Condition | Value          |     | Unit | Remarks |
|-------------------|--------------------------|---|-----------|----------------|-----|------|---------|
|                   |                          |   |           | Min            | Max |      |         |
| Input pulse width | $t_{TRGH}$<br>$t_{TRGL}$ | $\overline{\text{ATG}}$ ,<br>INT0, 1, 2, 3<br>INT4, 5 | —         | $5 t_{CYCP}^*$ | —   | ns   |         |

\* :  $t_{CYCP}$  is a cycle time of peripheral system clock.





## (11) A/D Converter Block Electrical Characteristics

( $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  $AV_{SS} = V_{SS} = 0 \text{ V}$ ,  $T_A = -30 \text{ }^\circ\text{C}$  to  $+70 \text{ }^\circ\text{C}$ )

| Parameter                        | Symbol    | Pin name   | Value                       |                             |                             | Unit          | Remarks |
|----------------------------------|-----------|------------|-----------------------------|-----------------------------|-----------------------------|---------------|---------|
|                                  |           |            | Min                         | Typ                         | Max                         |               |         |
| Resolution                       | —         | —          | —                           | 10                          | 10                          | BIT           |         |
| Total error                      | —         | —          | —                           | —                           | $\pm 4.0$                   | LSB           |         |
| Linearity error                  | —         | —          | —                           | —                           | $\pm 3.5$                   | LSB           |         |
| Differential linearity error     | —         | —          | —                           | —                           | $\pm 2.0$                   | LSB           |         |
| Zero transition voltage          | $V_{0t}$  | AN0 to AN7 | $AV_{SS} - 1.5 \text{ LSB}$ | $AV_{SS} + 0.5 \text{ LSB}$ | $AV_{SS} + 2.5 \text{ LSB}$ | mV            |         |
| Full-scale transition voltage    | $V_{FST}$ | AN0 to AN7 | $AVRH - 5.5 \text{ LSB}$    | $AVRH - 1.5 \text{ LSB}$    | $AVRH + 0.5 \text{ LSB}$    | mV            |         |
| Conversion time                  | —         | —          | 5.3                         | —                           | —                           | $\mu\text{s}$ |         |
| Analog input current             | $I_{AIN}$ | AN0 to AN7 | —                           | 0.1                         | 10                          | $\mu\text{A}$ |         |
| Analog input voltage             | $V_{AIN}$ | AN0 to AN7 | $AV_{SS}$                   | —                           | $AVRH$                      | V             |         |
| Reference voltage                | —         | $AVRH$     | $AV_{SS}$                   | —                           | $AV_{CC}$                   | V             |         |
| Power supply current             | $I_A$     | $AVCC$     | —                           | 3.0                         | 5.0                         | mA            |         |
|                                  | $I_{AH}$  |            | —                           | —                           | 5.0                         | $\mu\text{A}$ |         |
| Reference voltage supply current | $I_R$     | $AVRH$     | —                           | 100                         | 150                         | $\mu\text{A}$ |         |
|                                  | $I_{RH}$  |            | —                           | —                           | 10                          | $\mu\text{A}$ |         |
| Variation among channels         | —         | AN0 to AN7 | —                           | —                           | 4                           | LSB           |         |

Notes : • Relatively, the errors increase as  $|AVRH|$  value becomes smaller.

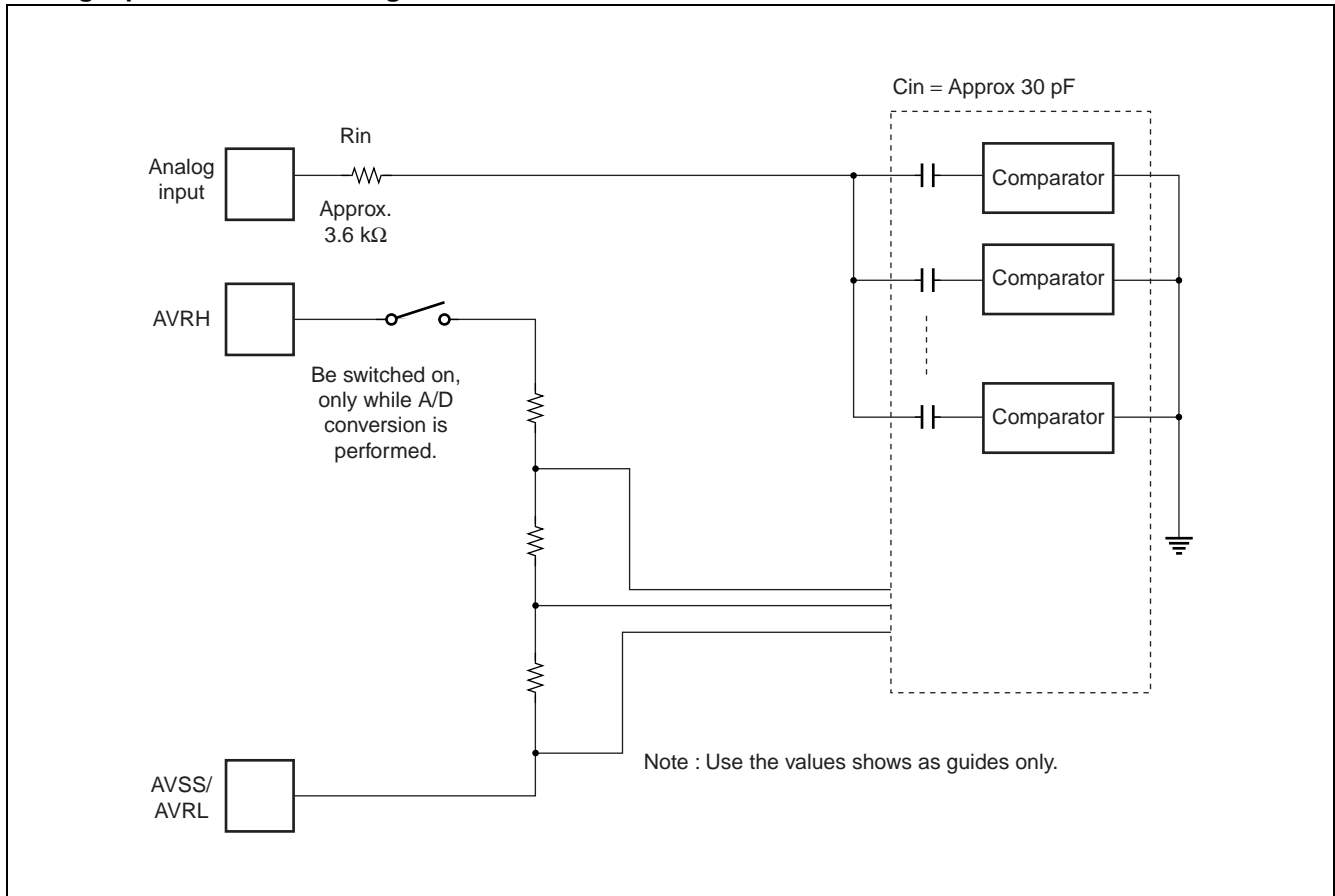
- Define an output impedance of external circuit analog input under the following conditions :

Output impedance of external circuit  $\leq 2 \text{ (k}\Omega\text{)}$

If an output impedance of external circuit is exceedingly high, sampling time for analog voltage may run short.

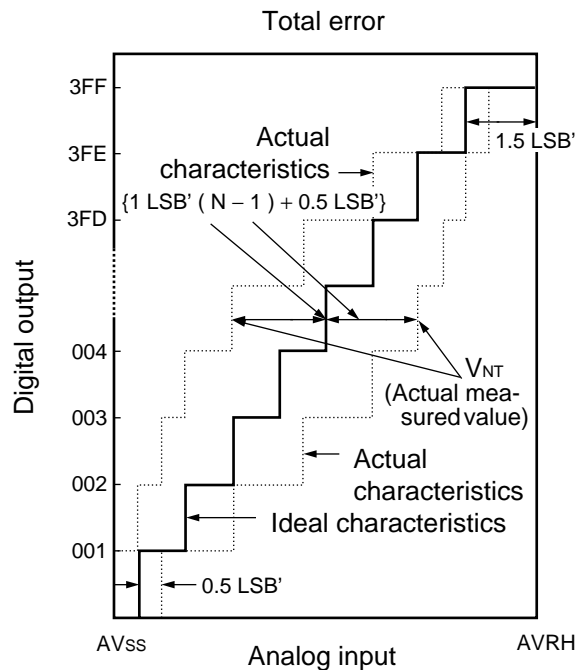
# MB91F127/F128

Analog input circuit model diagram



## 5. A/D Converter Block Electrical Characteristics

- Resolution  
Analog variations recognized by an A/D converter.
- Linearity error  
Deviation of actual conversion characteristics from an ideal line, which is across zero-transition point (“00 0000 0000” $\leftrightarrow$  “00 0000 0001”) and full-scale transition point (“11 1111 1110” $\leftrightarrow$  “11 1111 1111”)
- Differential linearity error  
Deviation from ideal value of input voltage, which is required for changing output code by 1 LSB.
- Total error  
Difference between actual value and ideal value. The error includes zero-transition error, full-scale transition error, and linearity error.



$$1 \text{ LSB}' (\text{Ideal value}) = \frac{AVRH - AVSS}{1024} \text{ [V]}$$

$$\text{Total error of digital output } N = \frac{V_{NT} - \{1 \text{ LSB}' \times (N - 1) + 0.5 \text{ LSB}'\}}{1 \text{ LSB}'}$$

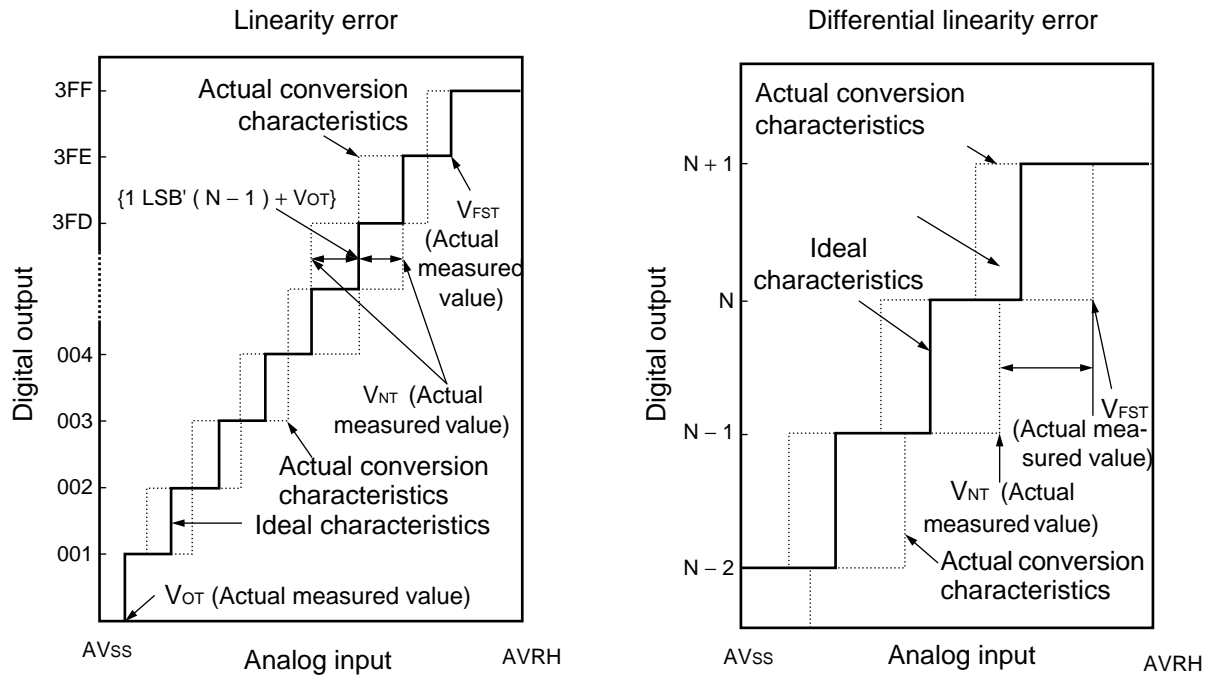
$V_{NT}$  : Transition voltage for digital output to change from (N+1) to N.

$$V_{OT}' (\text{Ideal value}) = AVSS + 0.5 \text{ LSB}' \text{ [V]}$$

$$V_{FST}' (\text{Ideal value}) = AVRH - 1.5 \text{ LSB}' \text{ [V]}$$

(Continued)

(Continued)



$$\text{Linearity error of digital output } N = \frac{V_{NT} - \{1 \text{ LSB}' \times (N - 1) + V_{OT}\}}{1 \text{ LSB}'} \quad [\text{LSB}]$$

$$\text{Differential linearity error of digital output } N = \frac{V_{(N+1)T} - V_{NT}}{1 \text{ LSB}'} - 1 \quad [\text{LSB}]$$

$$1 \text{ LSB} = \frac{V_{FST} - V_{OT}}{1022} \quad [\text{V}]$$

$V_{OT}$  : Transition voltage for digital output to change from  $(000)_H$  to  $(001)_H$ .

$V_{FST}$  : Transition voltage for digital output to change from  $(3FE)_H$  to  $(3FF)_H$ .

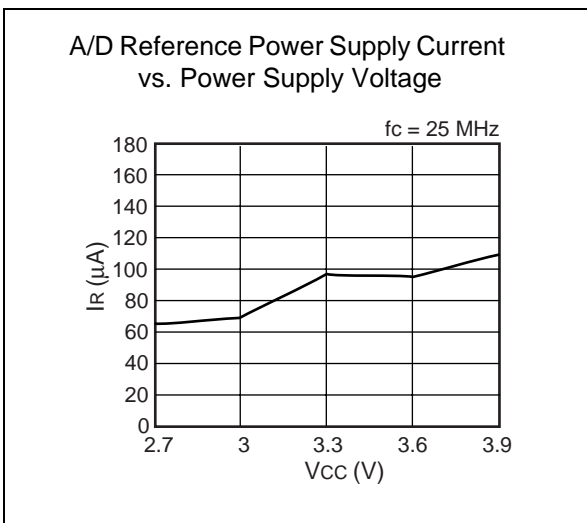
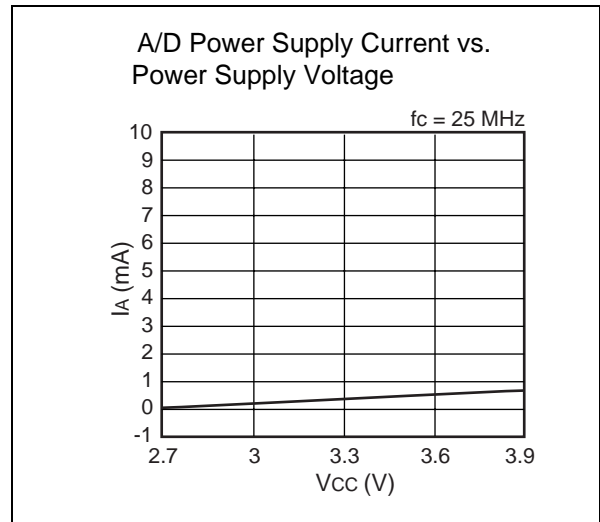
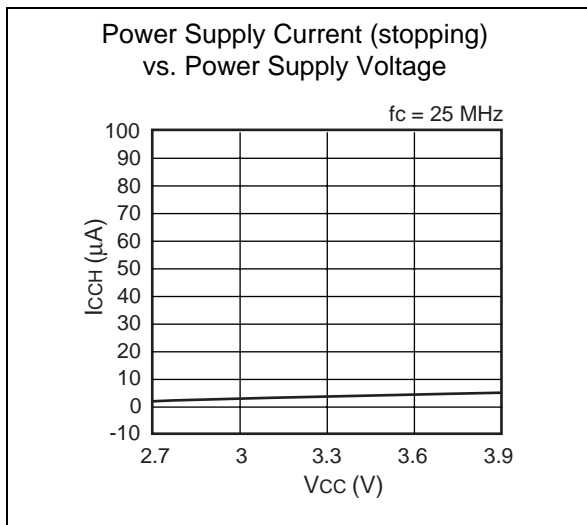
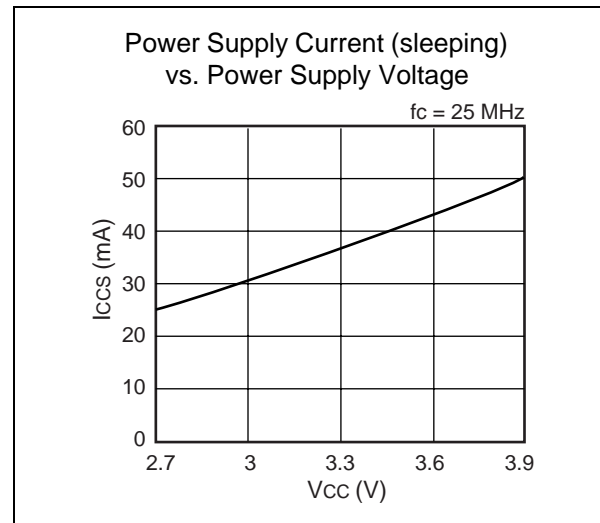
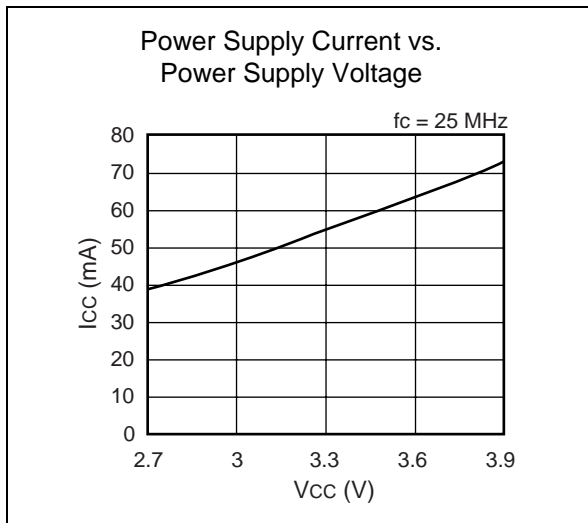
## ■ FLASH MEMORY WRITE/ERASE CHARACTERISTICS

| Parameter                             | Condition  | Value |         |      | Unit          | Remarks  |
|---------------------------------------|--|-------|---------|------|---------------|--|
|                                       |  | Min   | Typ     | Max  |               |  |
| Sector erase time                     | $T_A = +25\text{ }^\circ\text{C}$ ,<br>$V_{CC} = 3.3\text{ V}$ | —     | 1       | 15   | s             | Not including time for internal writing before deletion. |
| Chip erase time                       |  | —     | 4       | —    | s             | Not including time for internal writing before deletion. |
| Half byte (16 bit width) writing time |  | —     | 16      | 3600 | $\mu\text{s}$ | Not including system-level overhead time.                |
| Write/erase cycle                     | —  | —     | 10,000  | —    | cycle         |  |
| Data holding time                     | —  | —     | 100,000 | —    | h             |  |

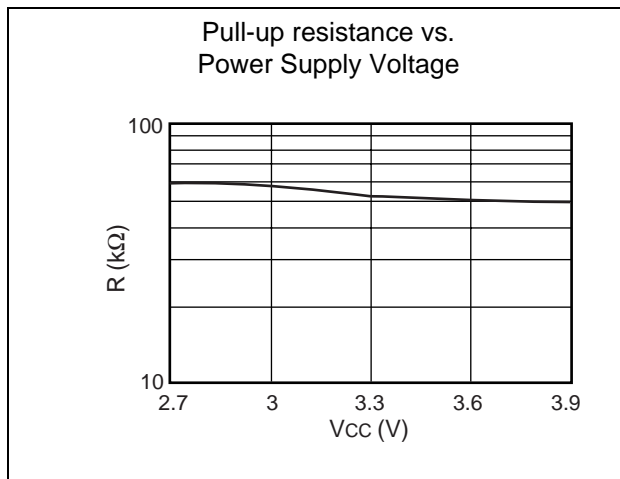
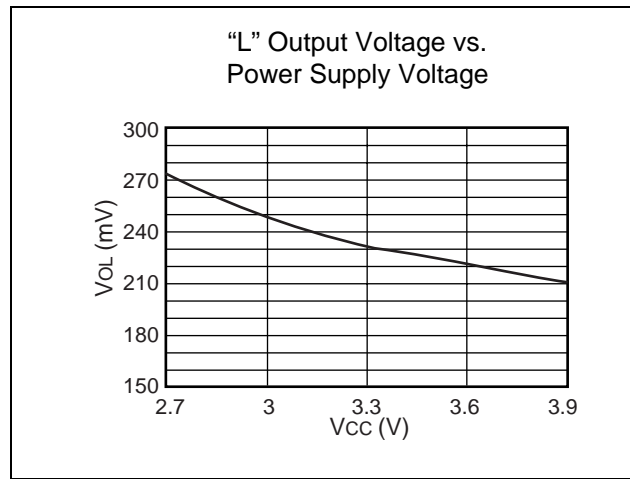
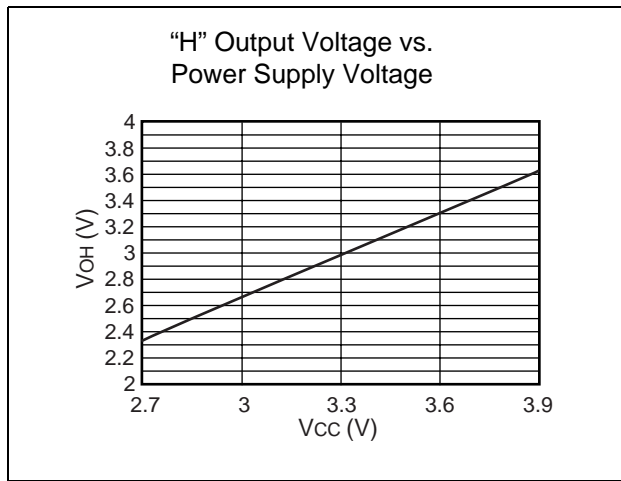
# MB91F127/F128

## EXAMPLE CHARACTERISTICS

- Power Supply Current



- Output Voltage



# MB91F127/F128

## ■ ORDERING INFORMATION

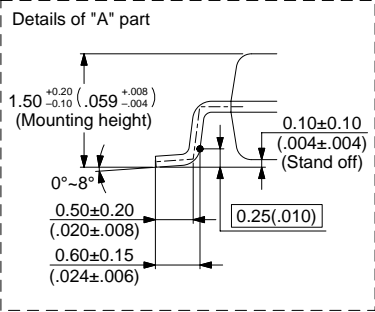
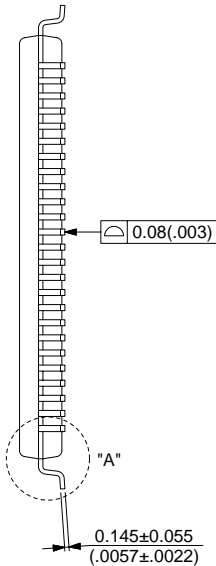
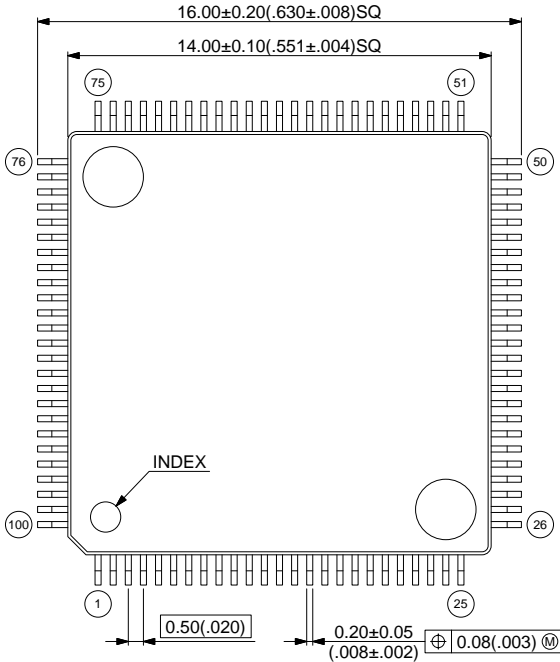
| Part number | Package                                | Remarks |
|-------------|--|---------|
| MB91F127PFV | 100-pin plastic LQFP<br>(FPT-100P-M05) |         |
| MB91F128PFV | 100-pin plastic LQFP<br>(FPT-100P-M05) |         |



■ PACKAGE DIMENSIONS

100-pin plastic LQFP  
(FPT-100P-M05)

\*Pins width and pins thickness include plating thickness.



© 2000 FUJITSU LIMITED F100007S-3c-5

Dimensions in mm (inches)

## FUJITSU LIMITED

All Rights Reserved.

The contents of this document are subject to change without notice. Customers are advised to consult with FUJITSU sales representatives before ordering.

The information and circuit diagrams in this document are presented as examples of semiconductor device applications, and are not intended to be incorporated in devices for actual use. Also, FUJITSU is unable to assume responsibility for infringement of any patent rights or other rights of third parties arising from the use of this information or circuit diagrams.

The products described in this document are designed, developed and manufactured as contemplated for general use, including without limitation, ordinary industrial use, general office use, personal use, and household use, but are not designed, developed and manufactured as contemplated (1) for use accompanying fatal risks or dangers that, unless extremely high safety is secured, could have a serious effect to the public, and could lead directly to death, personal injury, severe physical damage or other loss (i.e., nuclear reaction control in nuclear facility, aircraft flight control, air traffic control, mass transport control, medical life support system, missile launch control in weapon system), or (2) for use requiring extremely high reliability (i.e., submersible repeater and artificial satellite).

Please note that Fujitsu will not be liable against you and/or any third party for any claims or damages arising in connection with above-mentioned uses of the products.

Any semiconductor devices have an inherent chance of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

If any products described in this document represent goods or technologies subject to certain restrictions on export under the Foreign Exchange and Foreign Trade Law of Japan, the prior authorization by Japanese government will be required for export of those products from Japan.

F0201  
© FUJITSU LIMITED Printed in Japan