FUJITSU SEMICONDUCTOR
DATA SHEET

DS07–12624–4E

*8-bit Microcontrollers*

**CMOS**

# F²MC-8FX MB95160MA Series

## MB95168MA/F168MA/F168NA/F168JA/ MB95FV100D-103

## ■ DESCRIPTION

The MB95160MA series is general-purpose, single-chip microcontrollers. In addition to a compact instruction set, the microcontrollers contain a variety of peripheral functions.

Note : F²MC is the abbreviation of FUJITSU Flexible Microcontroller.

## ■ FEATURE

- F²MC-8FX CPU core
  Instruction set optimized for controllers
  - Multiplication and division instructions
  - 16-bit arithmetic operations
  - Bit test branch instruction
  - Bit manipulation instructions etc.
- Clock
  - Main clock
  - Main PLL clock
  - Sub clock
  - Sub PLL clock

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For the information for microcontroller supports, see the following web site.
This web site includes the **"Customer Design Review Supplement"** which provides the latest cautions on system development and the minimal requirements to be checked to prevent problems before the system development.

http://edevice.fujitsu.com/micom/en-support/


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- Timer
  - 8/16-bit compound timer × 2 channels
    Can be used to interval timer, PWC timer, PWM timer and input capture.
  - 8/16-bit PPG × 2 channels
  - 16-bit PPG × 1 channel
  - Time-base timer × 1 channel
  - Watch prescaler × 1 channel
- LIN-UART × 1 channel
  - LIN function, clock asynchronous (UART) or clock synchronous (SIO) serial data transfer capable
  - Full duplex double buffer
- UART/SIO × 1 channel
  - Clock asynchronous (UART) or clock synchronous (SIO) serial data transfer capable
  - Full duplex double buffer
- $I^2C$ × 1 channel
  Built-in wake-up function
- External interrupt × 8 channels
  - Interrupt by edge detection (rising, falling, or both edges can be selected)
  - Can be used to recover from low-power consumption (standby) modes.
- 8/10-bit A/D converter × 8 channels
  8-bit or 10-bit resolution can be selected.
- LCD controller (LCDC)
  - 32 SEG × 4 COM (Max 128 pixels)
  - With blinking function
- Low-power consumption (standby) mode
  - Stop mode
  - Sleep mode
  - Watch mode
  - Time-base timer mode
- I/O port
  - The number of maximum ports : Max 52
  - Port configuration
    - General-purpose I/O ports (N-ch open drain) : 2 ports
    - General-purpose I/O ports (CMOS) : 50 ports
- Programmable input voltage levels of port
  Automotive input level / CMOS input level / hysteresis input level
- Flash memory security function (Flash memory product only)
  Protects the content of Flash memory

## ■ PRODUCT LINEUP

| Parameter \ Part number | | MB95168MA | MB95F168MA | MB95F168NA | MB95F168JA |
|---|---|---|---|---|---|
| Type | | Mask ROM product | Flash memory product | | |
| ROM capacity | | 60 Kbytes | | | |
| RAM capacity | | 2 Kbytes | | | |
| Reset output | | Yes/No selectable | Yes | | No |
| Option* | Clock system | Dual clock | | | |
| | Low voltage detection reset | Yes/No selectable | No | Yes | |
| | Clock supervisor | Yes/No selectable | No | | Yes |
| CPU functions | | Number of basic instructions : 136<br>Instruction bit length : 8 bits<br>Instruction length : 1 to 3 bytes<br>Data bit length : 1, 8, and 16 bits<br>Minimum instruction execution time : 61.5 ns (at machine clock frequency 16.25 MHz)<br>Interrupt processing time : 0.6 µs (at machine clock frequency 16.25 MHz) | | | |
| Peripheral functions | Ports (Max 52 ports) | General-purpose I/O port (N-ch open drain) : 2 ports<br>General-purpose I/O port (CMOS) : 50 ports<br>Programmable input voltage levels of port :<br>Automotive input level / CMOS input level / hysteresis input level | | | |
| | Time-base timer (1 channel) | Interrupt cycle : 0.5 ms, 2.1 ms, 8.2 ms, 32.8 ms (at main oscillation clock 4 MHz) | | | |
| | Watchdog timer | Reset generated cycle<br>At main oscillation clock 10 MHz : Min 105 ms<br>At sub oscillation clock 32.768 kHz (for dual clock product) : Min 250 ms | | | |
| | Wild register | Capable of replacing 3 bytes of ROM data | | | |
| | $I^2C$ (1 channel) | Master/slave sending and receiving<br>Bus error function and arbitration function<br>Detecting transmitting direction function<br>Start condition repeated generation and detection functions<br>Built-in wake-up function | | | |
| | UART/SIO (1 channel) | Data transfer capable in UART/SIO<br>Full duplex double buffer,<br>variable data length (5/6/7/8-bit), built-in baud rate generator<br>NRZ type transfer format, error detected function<br>LSB-first or MSB-first can be selected.<br>Clock synchronous (SIO) or clock asynchronous (UART) serial data transfer capable | | | |
| | LIN-UART (1 channel) | Dedicated reload timer allowing a wide range of communication speeds to be set.<br>Full duplex double buffer.<br>Capable of serial data transfer synchronous or asynchronous to clock signal.<br>LIN functions available as the LIN master or LIN slave. | | | |
| | 8/10-bit A/D converter (8 channels) | 8-bit or 10-bit resolution can be selected. | | | |

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| Parameter \ Part number | | MB95168MA | MB95F168MA | MB95F168NA | MB95F168JA |
|---|---|---|---|---|---|
| Peripheral functions | LCD controller (LCDC) | COM output : 4 (Max)<br>SEG output : 32 (Max)<br>LCD drive power supply (bias) pin : 4<br>32 SEG × 4 COM : 128 pixels can be displayed.<br>Duty LCD mode<br>Operable in LCD standby mode<br>With blinking function<br>Built-in division resistance for LCD drive | | | |
| | 8/16-bit compound timer (2 channels) | Each channel of the timer can be used as “8-bit timer × 2 channels” or “16-bit timer × 1 channel”.<br>Built-in timer function, PWC function, PWM function, capture function, and square wave form output<br>Count clock : 7 internal clocks and external clock can be selected. | | | |
| | 16-bit PPG (1 channel) | PWM mode or one-shot mode can be selected.<br>Counter operating clock : Eight selectable clock sources<br>Support for external trigger start | | | |
| | 8/16-bit PPG (2 channels) | Each channel of the PPG can be used as “8-bit PPG × 2 channels” or “16-bit PPG × 1 channel”.<br>Counter operating clock : Eight selectable clock sources | | | |
| | Watch counter | Count clock : Four selectable clock sources (125 ms, 250 ms, 500 ms, or 1 s)<br>Counter value can be set from 0 to 63. (Capable of counting for 1 minute when selecting clock source 1 second and setting counter value to 60) | | | |
| | Watch prescaler (1 channel) | 4 selectable interval times (125 ms, 250 ms, 500 ms, or 1 s) | | | |
| | External interrupt (8 channels) | Interrupt by edge detection (rising, falling, or both edges can be selected.)<br>Can be used to recover from standby modes. | | | |
| Flash memory | | — | Supports automatic programming, Embedded Algorithm<br>Write/Erase/Erase-Suspend/Resume commands<br>A flag indicating completion of the algorithm<br>Number of write/erase cycles (Minimum) : 10000 times<br>Data retention time: 20 years<br>Erase can be performed on each block<br>Block protection with external programming voltage<br>Flash Security Feature for protecting the content of the Flash | | |
| Standby mode | | Sleep, stop, watch, and time-base timer | | | |

* : For details of option, refer to “■ MASK OPTION”.

Note : Part number of evaluation product in MB95160MA series is MB95FV100D-103. When using it, the MCU board (MB2146-303A-E) is required.

## ■ OSCILLATION STABILIZATION WAIT TIME

The initial value of the main clock oscillation stabilization wait time is fixed to the maximum value. The maximum value is shown as follows.

| Oscillation stabilization wait time | Remarks |
|---|---|
| $(2^{14}-2)/F_{CH}$ | Approx. 4.10 ms (at main oscillation clock 4 MHz) |

## ■ PACKAGES AND CORRESPONDING PRODUCTS

| Package \ Part number | MB95168MA | MB95F168MA/ F168NA/F168JA | MB95FV100D-103 |
|---|---|---|---|
| FPT-64P-M23 | ○ | ○ | × |
| FPT-64P-M24 | ○ | ○ | × |
| BGA-224P-M08 | × | × | ○ |

○ : Available
× : Unavailable

## ■ DIFFERENCES AMONG PRODUCTS AND NOTES ON SELECTING PRODUCTS

• Notes on Using Evaluation Products

The evaluation product has not only the functions of the MB95160MA series but also those of other products to support software development for multiple series and models of the F²MC-8FX family. The I/O addresses for peripheral resources not used by the MB95160MA series are therefore access-barred. Read/write access to these access-barred addresses may cause peripheral resources supposed to be unused to operate, resulting in unexpected malfunctions of hardware or software.

Particularly, do not use word access to odd numbered byte address in the prohibited areas (If these access are used, the address may be read or written unexpectedly).

Also, as the read values of prohibited addresses on the evaluation product are different to the values on the Flash memory products or Mask ROM products, do not use these values in the program.

The functions corresponding to certain bits in single-byte registers may not be supported depending on the type of Flash memory products and Mask ROM products. However, reading or writing to these bits will not cause malfunction of the hardware. Also, the products with either evaluation, Flash memory or Mask ROM are designed to have the same operation in software and hardware.

• Difference of Memory Spaces

If the amount of memory on the evaluation product is different from that of the Flash memory and Mask ROM products, carefully check the difference in the amount of memory from the model to be actually used when developing software.

For details of memory space, refer to “■ CPU CORE”.

• Current Consumption

Current in Flash memory products is consumed more than Mask ROM products.
For details of current consumption, refer to “■ ELECTRICAL CHARACTERISTICS”.

• Package

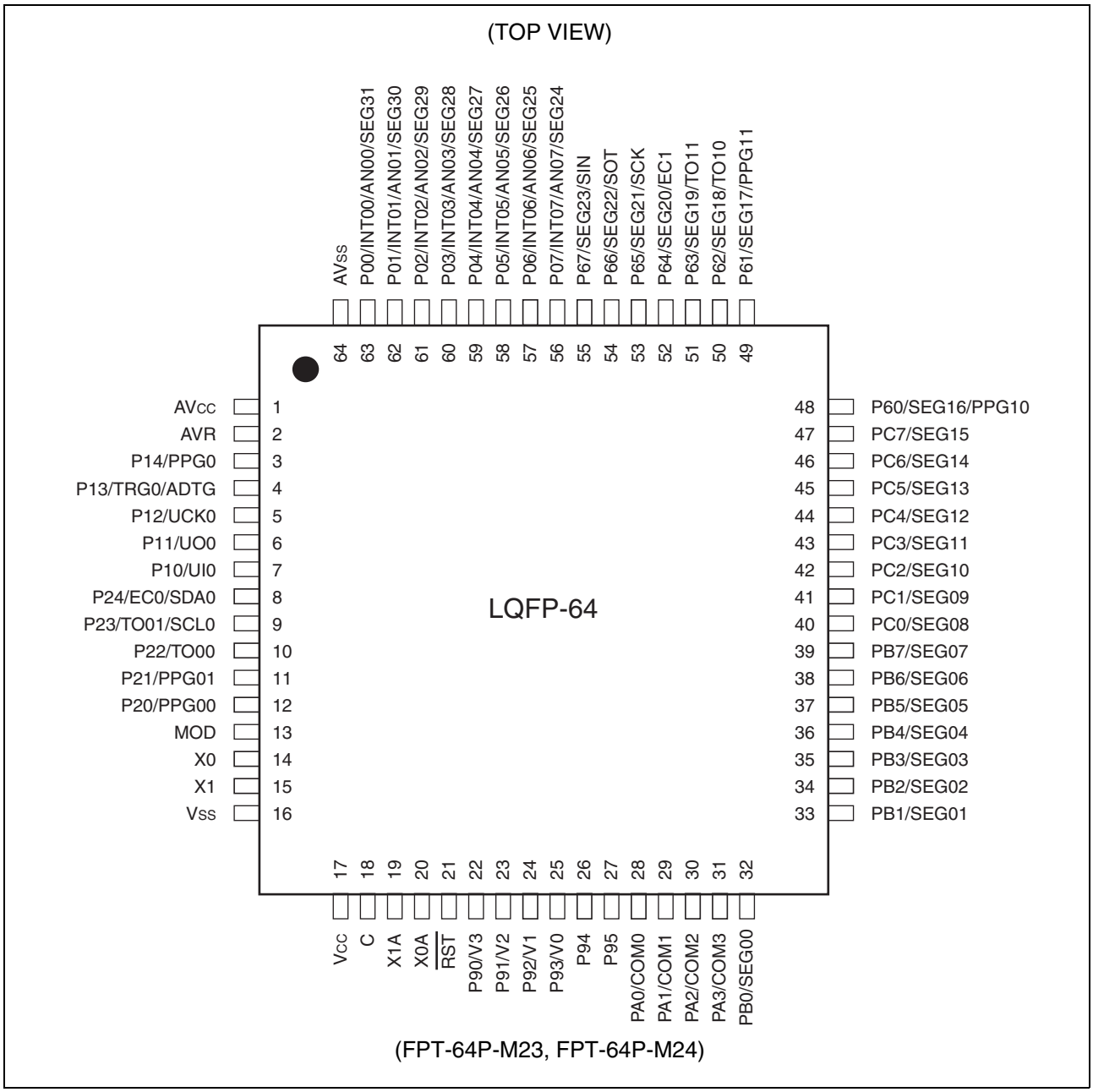
For details of information on each package, refer to “■ PACKAGES AND CORRESPONDING PRODUCTS” and “■ PACKAGE DIMENSIONS”.

• Operating voltage

The operating voltage is different among the evaluation, Flash memory products and Mask ROM products.

For details of operating voltage, refer to “■ ELECTRICAL CHARACTERISTICS”

## ■ PIN ASSIGNMENT



## ■ PIN DESCRIPTION

| Pin no. | Pin name | I/O circuit type*1 | Function |
|---|---|---|---|
| 1 | $AV_{CC}$ | — | A/D converter power supply pin |
| 2 | AVR | — | A/D converter reference input pin |
| 3 | P14/PPG0 | H | General-purpose I/O port.<br>The pin is shared with 16-bit PPG ch.0 output. |
| 4 | P13/TRG0/ ADTG | | General-purpose I/O port.<br>The pin is shared with 16-bit PPG ch.0 trigger input (TRG0) and A/D converter trigger input (ADTG) . |
| 5 | P12/UCK0 | | General-purpose I/O port.<br>The pin is shared with UART/SIO ch.0 clock I/O. |
| 6 | P11/UO0 | | General-purpose I/O port.<br>The pin is shared with UART/SIO ch.0 data output. |
| 7 | P10/UI0 | G | General-purpose I/O port.<br>The pin is shared with UART/SIO ch.0 data input. |
| 8 | P24/EC0/ SDA0 | I | General-purpose I/O port.<br>The pin is shared with 8/16-bit compound timer ch.0 clock input (EC0) and $I^2C$ ch.0 data I/O (SDA0) . |
| 9 | P23/TO01/ SCL0 | | General-purpose I/O port.<br>The pin is shared with 8/16-bit compound timer ch.0 output (TO01) and $I^2C$ ch.0 clock I/O (SCL0) . |
| 10 | P22/TO00 | H | General-purpose I/O port.<br>The pin is shared with 8/16-bit compound timer ch.0 output. |
| 11 | P21/PPG01 | | General-purpose I/O port.<br>The pin is shared with 8/16-bit PPG ch.0 output. |
| 12 | P20/PPG00 | | General-purpose I/O port.<br>The pin is shared with 8/16-bit PPG ch.0 output. |
| 13 | MOD | B | Operating mode designation pin |
| 14 | X0 | A | Main clock oscillation pins |
| 15 | X1 | | |
| 16 | $V_{SS}$ | — | Power supply pin (GND) |
| 17 | $V_{CC}$ | — | Power supply pin |
| 18 | C | — | Capacitor connection pin |
| 19 | X1A | A | Sub clock oscillation pins (32 kHz) |
| 20 | X0A | | |
| 21 | $\overline{RST}$ | B’ | Reset pin |
| 22 | P90/V3 | R | General-purpose I/O ports.<br>The pins are shared with power supply pin for LCDC drive. |
| 23 | P91/V2 | | |
| 24 | P92/V1 | | |
| 25 | P93/V0 | | |

*(Continued)*

| Pin no. | Pin name | I/O circuit type*1 | Function |
|---|---|---|---|
| 26 | P94 | S | General-purpose I/O ports. |
| 27 | P95*2 | | |
| 28 | PA0/COM0 | M | General-purpose I/O ports.<br>The pins are shared with LCDC COM output (COM0 to COM3). |
| 29 | PA1/COM1 | | |
| 30 | PA2/COM2 | | |
| 31 | PA3/COM3 | | |
| 32 | PB0/SEG00 | M | General-purpose I/O ports.<br>The pins are shared with LCDC SEG output (SEG00 to SEG07). |
| 33 | PB1/SEG01 | | |
| 34 | PB2/SEG02 | | |
| 35 | PB3/SEG03 | | |
| 36 | PB4/SEG04 | | |
| 37 | PB5/SEG05 | | |
| 38 | PB6/SEG06 | | |
| 39 | PB7/SEG07 | | |
| 40 | PC0/SEG08 | M | General-purpose I/O ports.<br>The pins are shared with LCDC SEG output (SEG08 to SEG15). |
| 41 | PC1/SEG09 | | |
| 42 | PC2/SEG10 | | |
| 43 | PC3/SEG11 | | |
| 44 | PC4/SEG12 | | |
| 45 | PC5/SEG13 | | |
| 46 | PC6/SEG14 | | |
| 47 | PC7/SEG15 | | |
| 48 | P60/SEG16/ PPG10 | M | General-purpose I/O ports.<br>The pins are shared with LCDC SEG output (SEG16, SEG17) and 8/16-bit PPG ch.1 output (PPG10, PPG11) . |
| 49 | P61/SEG17/ PPG11 | | |
| 50 | P62/SEG18/ TO10 | | General-purpose I/O port.<br>The pin is shared with LCDC SEG output (SEG18) and 8/16-bit compound timer ch.1 output (TO10) . |
| 51 | P63/SEG19/ TO11 | | General-purpose I/O port.<br>The pin is shared with LCDC SEG output (SEG19) and 8/16-bit compound timer ch.1 output (TO11) . |
| 52 | P64/SEG20/ EC1 | | General-purpose I/O port.<br>The pin is shared with LCDC SEG output (SEG20) and 8/16-bit compound timer ch.1 clock input (EC1) . |
| 53 | P65/SEG21/ SCK | | General-purpose I/O port.<br>The pin is shared with LCDC SEG output (SEG21) and LIN-UART clock I/O (SCK) . |
| 54 | P66/SEG22/ SOT | | General-purpose I/O port.<br>The pin is shared with LCDC SEG output (SEG22) and LIN-UART data output (SOT) . |

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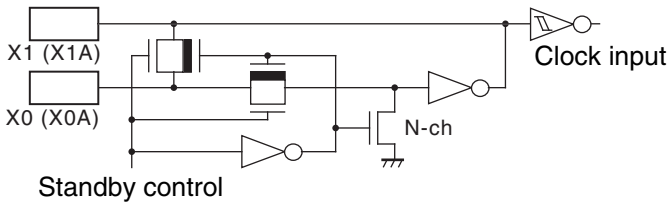
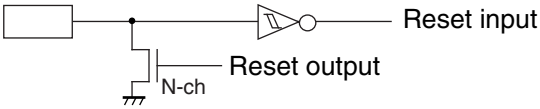
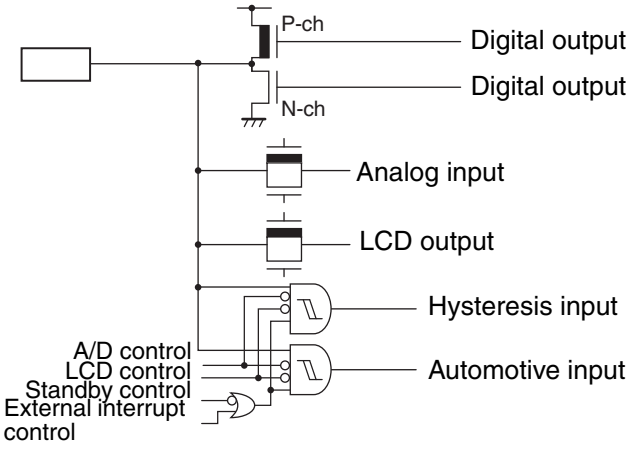
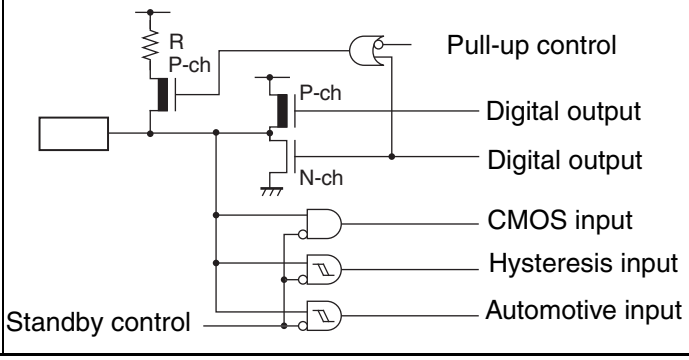
| Pin no. | Pin name | I/O circuit type*1 | Function |
|---|---|---|---|
| 55 | P67/SEG23/ SIN | N | General-purpose I/O port. The pin is shared with LCDC SEG output (SEG23) and LIN-UART data input (SIN) . |
| 56 | P07/INT07/ AN07/SEG24 | F | General-purpose I/O ports. The pins are shared with external interrupt input (INT00 to INT07), A/D analog input (AN00 to AN07) and LCDC SEG output (SEG31 to SEG24) . |
| 57 | P06/INT06/ AN06/SEG25 | | |
| 58 | P05/INT05/ AN05/SEG26 | | |
| 59 | P04/INT04/ AN04/SEG27 | | |
| 60 | P03/INT03/ AN03/SEG28 | | |
| 61 | P02/INT02/ AN02/SEG29 | | |
| 62 | P01/INT01/ AN01/SEG30 | | |
| 63 | P00/INT00/ AN00/SEG31 | | |
| 64 | $AV_{SS}$ | — | Power supply pin (GND) of A/D converter |

*1 : Refer to “■ I/O CIRCUIT TYPE” for details on the I/O circuit types.

*2 : When using P07 for segment output (SEG24) of LCDC, P95 can not be used as an output port. It can be used only as an input port.

## ■ I/O CIRCUIT TYPE

| Type | Circuit | Remarks |
|---|---|---|
| A |  | • Oscillation circuit<br>• High-speed side<br>Feedback resistance : approx. 1 MΩ<br>• Low-speed side<br>Feedback resistance : approx. 10 MΩ |
| B |  | • Only for input<br>• Hysteresis input |
| B’ |  | • Hysteresis input<br>• Reset output |
| F |  | • CMOS output<br>• LCD output<br>• Hysteresis input<br>• Analog input<br>• Automotive input |
| G |  | • CMOS output<br>• CMOS input<br>• Hysteresis input<br>• With pull-up control<br>• Automotive input |

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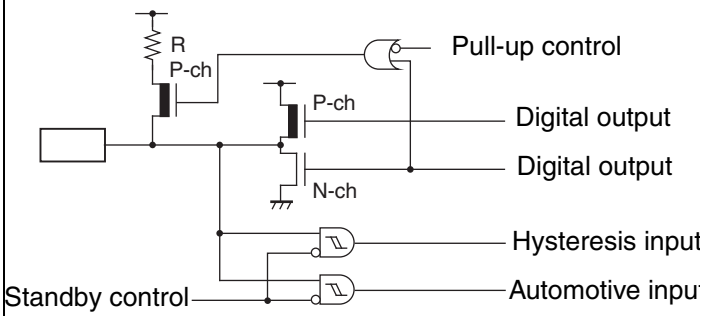
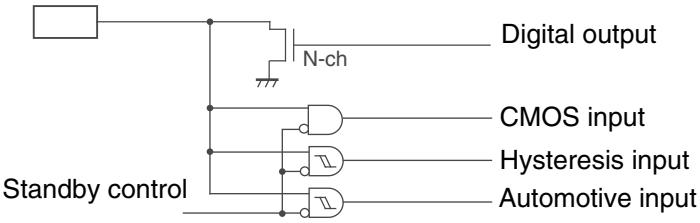
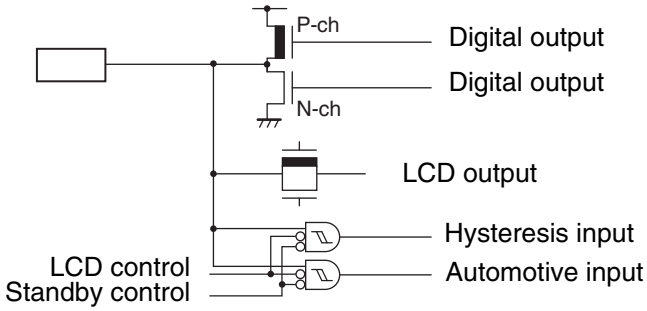
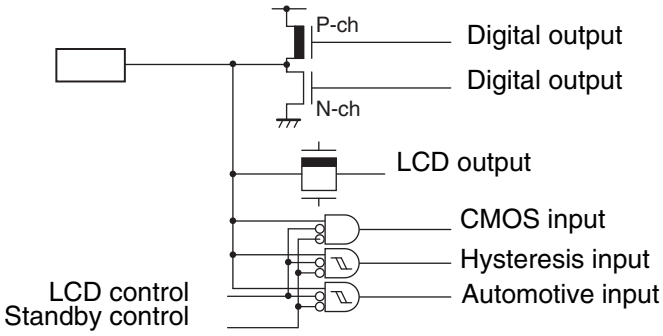
| Type | Circuit | Remarks |
|---|---|---|
| H |  | • CMOS output<br>• Hysteresis input<br>• With pull-up control<br>• Automotive input |
| I |  | • N-ch open drain output<br>• CMOS input<br>• Hysteresis input<br>• Automotive input |
| M |  | • CMOS output<br>• LCD output<br>• Hysteresis input<br>• Automotive input |
| N |  | • CMOS output<br>• LCD output<br>• CMOS input<br>• Hysteresis input<br>• Automotive input |

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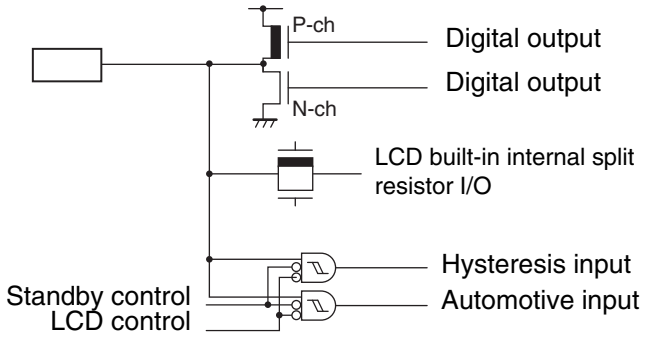
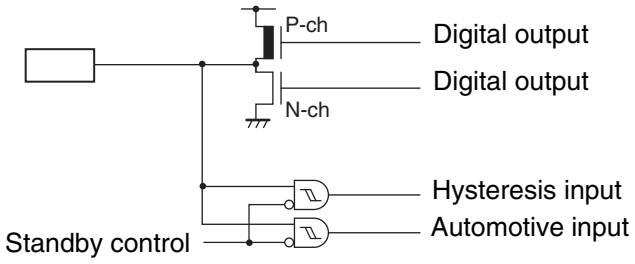
| Type | Circuit | Remarks |
|---|---|---|
| R |  | • CMOS output<br>• LCD power supply<br>• Hysteresis input<br>• Automotive input |
| S |  | • CMOS output<br>• LCD power supply<br>• Hysteresis input<br>• Automotive input |

## ■ HANDLING DEVICES

• Preventing Latch-up

Care must be taken to ensure that maximum voltage ratings are not exceeded when they are used.

Latch-up may occur on CMOS ICs if voltage higher than $V_{CC}$ or lower than $V_{SS}$ is applied to input and output pins
other than medium- and high-withstand voltage pins or if higher than the rating voltage is applied between $V_{CC}$ pin and $V_{SS}$ pin.

When latch-up occurs, power supply current increases rapidly and might thermally damage elements.

• Stable Supply Voltage

Supply voltage should be stabilized.

A sudden change in power-supply voltage may cause a malfunction even within the guaranteed operating range of the Vcc power-supply voltage.

For stabilization, in principle, keep the variation in Vcc ripple (p-p value) in a commercial frequency range (50/60 Hz) not to exceed 10% of the standard Vcc value and suppress the voltage variation so that the transient variation rate does not exceed 0.1 V/ms during a momentary change such as when the power supply is switched.

• Precautions for Use of External Clock

Even when an external clock is used, oscillation stabilization wait time is required for power-on reset, wake-up from sub clock mode or stop mode.

• Serial communication

There is a possibility to receive wrong data due to noise or other causes on the serial communication.

Therefore, design a printed circuit board so as to avoid noise.

Consider receiving of wrong data when designing the system. For example apply a checksum and retransmit the data if an error occurs.

**PIN CONNECTION**

• Treatment of Unused Pin

Leaving unused input pins unconnected can cause abnormal operation or latch-up, leaving to permanent damage. Unused input pins should always be pulled up or down through resistance of at least 2 kΩ. Any unused input/output pins may be set to output mode and left open, or set to input mode and treated the same as unused input pins. If there is unused output pin, make it to open.

• Power Supply Pins

In products with multiple $V_{CC}$ or $V_{SS}$ pins, the pins of the same potential are internally connected in the device to avoid abnormal operations including latch-up. However, you must connect the pins to external power supply and a ground line to lower the electro-magnetic emission level, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating.

Moreover, connect the current supply source with the $V_{CC}$ and $V_{SS}$ pins of this device at the low impedance.

It is also advisable to connect a ceramic bypass capacitor of approximately 0.1 μF between $V_{CC}$ and $V_{SS}$ pins near this device.

• Mode Pin (MOD)

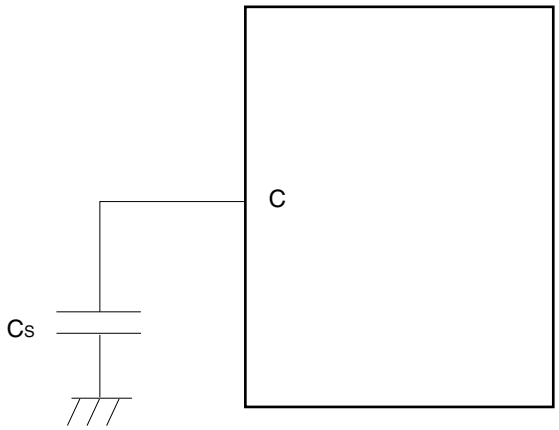
Connect the MOD pin directly to $V_{CC}$ or $V_{SS}$.

To prevent the device unintentionally entering test mode due to noise, lay out the printed circuit board so as to minimize the distance from the MOD pin to $V_{CC}$ or $V_{SS}$ and to provide a low-impedance connection.

• C Pin

Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. A bypass capacitor of $V_{CC}$ pin must have a capacitance value higher than $C_S$. For connection of smoothing capacitor $C_S$, refer to the diagram below.

• C pin connection diagram




• Analog Power Supply

Always set the same potential to $AV_{CC}$ and $V_{CC}$ pins. When $V_{CC} > AV_{CC}$, the current may flow through the AN00 to AN07 pins.

• Treatment of Power Supply Pins on A/D Converter

Connect to be $AV_{CC} = V_{CC}$ and $AV_{SS} = AVR = V_{SS}$ even if the A/D converter is not in use.

Noise riding on the $AV_{CC}$ pin may cause accuracy degradation. So, connect approx. 0.1 µF ceramic capacitor as a bypass capacitor between $AV_{CC}$ and $AV_{SS}$ pins in the vicinity of this device.

## ■ PROGRAMMING FLASH MEMORY MICROCONTROLLERS USING PARALLEL PROGRAMMER

**• Supported Parallel Programmers and Adapters**

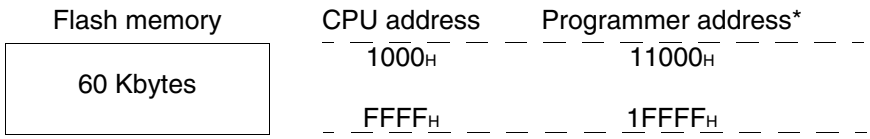
The following table lists supported parallel programmers and adapters.

| Package | Applicable adapter model | Parallel programmers |
|---|---|---|
| FPT-64P-M23 | TEF110-95F168HPMC | AF9708 (Ver 02.35G or more)<br>AF9709/B (Ver 02.35G or more)<br>AF9723+AF9834 (Ver 02.08E or more) |
| FPT-64P-M24 | TEF110-95F168HPMC1 | |

Note : For information on applicable adapter models and parallel programmers, contact the following:
Flash Support Group, Inc. TEL: +81-53-428-8380

**• Sector Configuration**

The individual sectors of Flash memory correspond to addresses used for CPU access and programming by the parallel programmer as follows:

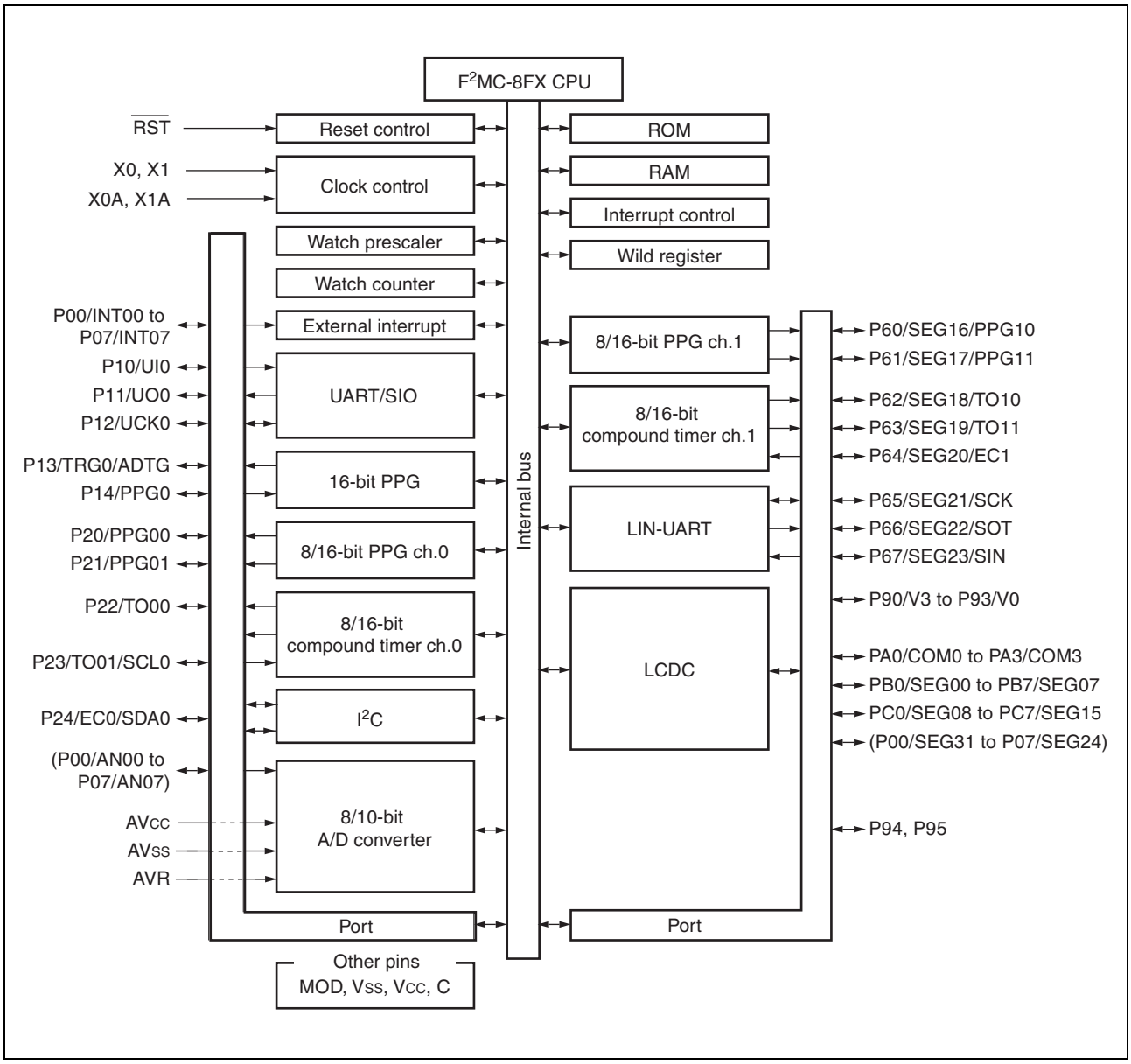



*: Programmer addresses are corresponding to CPU addresses, used when the parallel programmer programs data into Flash memory.
These programmer addresses are used for the parallel programmer to program or erase data in Flash memory.

**• Programming Method**

1) Set the type code of the parallel programmer to 17222.
2) Load program data to programmer addresses $11000_H$ to $1FFFF_H$.
3) Programmed by parallel programmer

## ■ BLOCK DIAGRAM

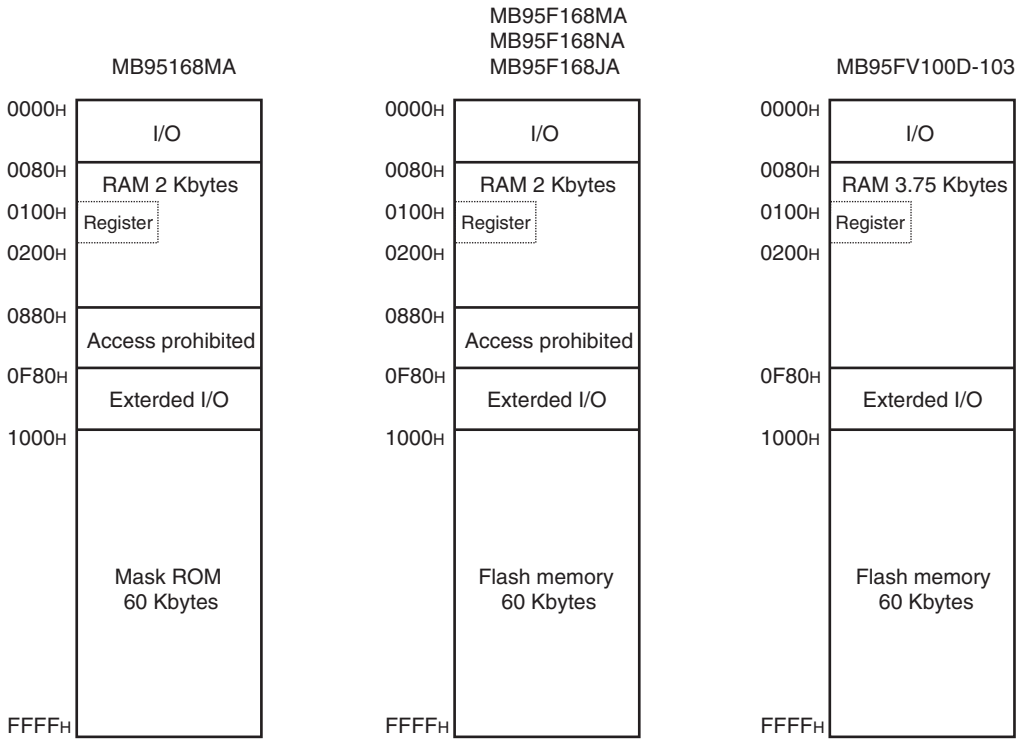


## ■ CPU CORE

### 1. Memory space

Memory space of the MB95160MA series is 64 Kbytes and consists of I/O area, data area, and program area. The memory space includes special-purpose areas such as the general-purpose registers and vector table. Memory map of the MB95160MA series is shown below.

• Memory Map



## 2. Register

The MB95160MA series has two types of registers; dedicated registers in the CPU and general-purpose registers in the memory. The dedicated registers are as follows:

Program counter (PC) : A 16-bit register to indicate locations where instructions are stored.

Accumulator (A) : A 16-bit register for temporary storage of arithmetic operations. In the case of an 8-bit data processing instruction, the lower 1 byte is used.

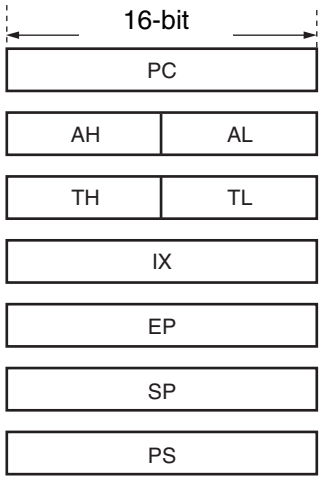
Temporary accumulator (T) : A 16-bit register which performs arithmetic operations with the accumulator. In the case of an 8-bit data processing instruction, the lower 1 byte is used.

Index register (IX) : A 16-bit register for index modification.

Extra pointer (EP) : A 16-bit pointer to point to a memory address.

Stack pointer (SP) : A 16-bit register to indicate a stack area.

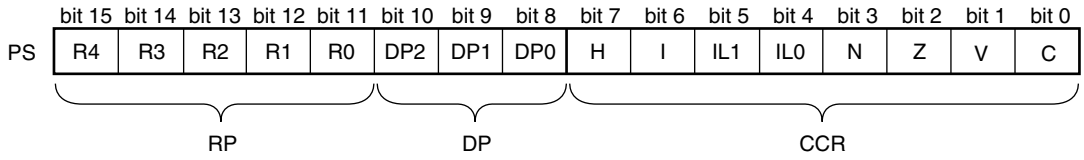
Program status (PS) : A 16-bit register for storing a register bank pointer, a direct bank pointer, and a condition code register.




| | Initial Value |
|---|---|
| : Program counter | $FFFD_H$ |
| : Accumulator | $0000_H$ |
| : Temporary accumulator | $0000_H$ |
| : Index register | $0000_H$ |
| : Extra pointer | $0000_H$ |
| : Stack pointer | $0000_H$ |
| : Program status | $0030_H$ |

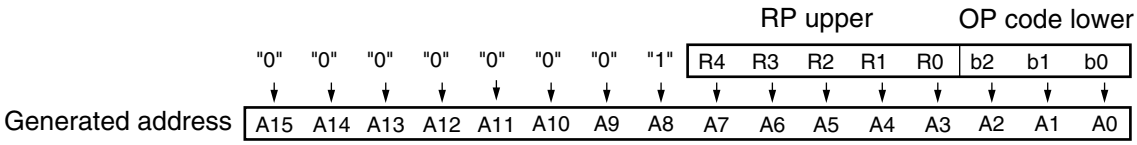
The PS can further be divided into higher 8 bits for use as a register bank pointer (RP) and a direct bank pointer (DP) and the lower 8 bits for use as a condition code register (CCR). (Refer to the diagram below.)

• Structure of the Program Status



The RP indicates the address of the register bank currently being used. The relationship between the content of RP and the real address conforms to the conversion rule illustrated below:

• Rule for Conversion of Actual Addresses in the General-purpose Register Area




The DP specifies the area for mapping instructions (16 different instructions such as MOV A, dir) using direct addresses to $0080_H$ to $00FF_H$.

| Direct bank pointer (DP2 to DP0) | Specified address area | Mapping area |
|---|---|---|
| $XXX_B$ (no effect to mapping) | $0000_H$ to $007F_H$ | $0000_H$ to $007F_H$ (without mapping) |
| $000_B$ (initial value) | $0080_H$ to $00FF_H$ | $0080_H$ to $00FF_H$ (without mapping) |
| $001_B$ | | $0100_H$ to $017F_H$ |
| $010_B$ | | $0180_H$ to $01FF_H$ |
| $011_B$ | | $0200_H$ to $027F_H$ |
| $100_B$ | | $0280_H$ to $02FF_H$ |
| $101_B$ | | $0300_H$ to $037F_H$ |
| $110_B$ | | $0380_H$ to $03FF_H$ |
| $111_B$ | | $0400_H$ to $047F_H$ |

The CCR consists of the bits indicating arithmetic operation results or transfer data contents and the bits that control CPU operations at interrupt.

H flag : Set to “1” when a carry or a borrow from bit 3 to bit 4 occurs as a result of an arithmetic operation. Cleared to “0” otherwise. This flag is for decimal adjustment instructions.

I flag : Interrupt is enabled when this flag is set to “1”. Interrupt is disabled when this flag is set to “0”. The flag is set to “0” when reset.

IL1, IL0 : Indicates the level of the interrupt currently enabled. Processes an interrupt only if its request level is higher than the value indicated by these bits.

| IL1 | IL0 | Interrupt level | Priority |
|---|---|---|---|
| 0 | 0 | 0 | High |
| 0 | 1 | 1 | ↕ |
| 1 | 0 | 2 | |
| 1 | 1 | 3 | Low (no interruption) |

N flag : Set to “1” if the MSB is set to “1” as the result of an arithmetic operation. Cleared to “0” when the bit is set to “0”.

Z flag : Set to “1” when an arithmetic operation results in “0”. Cleared to “0” otherwise.

V flag : Set to “1” if the complement on 2 overflows as a result of an arithmetic operation. Cleared to “0” otherwise.

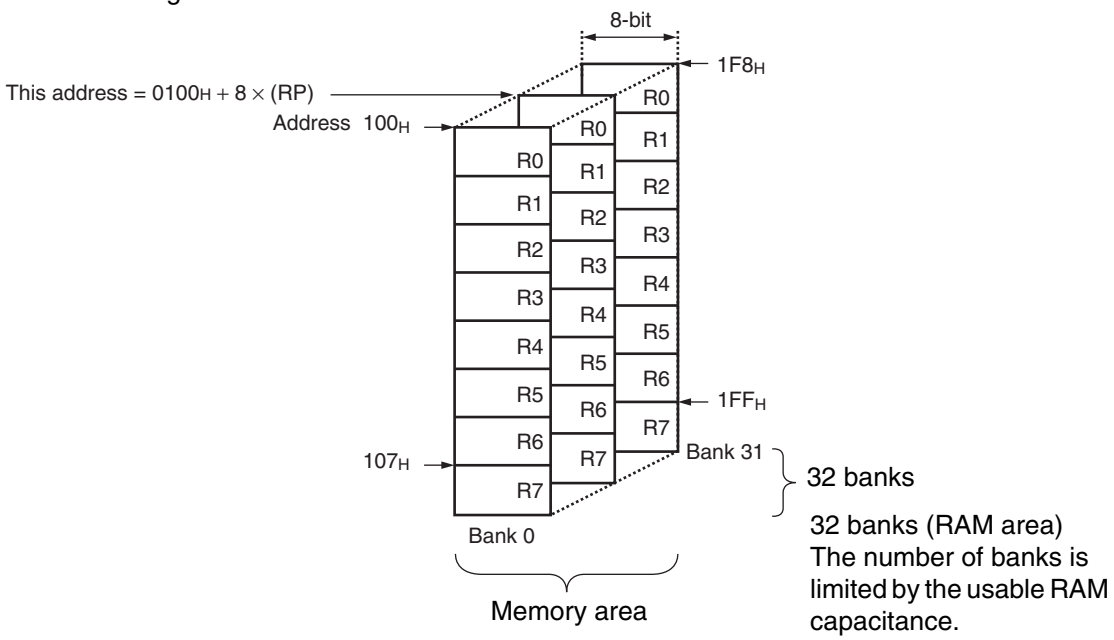
C flag : Set to “1” when a carry or a borrow from bit 7 occurs as a result of an arithmetic operation. Cleared to “0” otherwise. Set to the shift-out value in the case of a shift instruction.

The following general-purpose registers are provided:

General-purpose registers: 8-bit data storage registers

The general-purpose registers are 8 bits and located in the register banks on the memory. 1-bank contains 8-register. Up to a total of 32 banks can be used on the MB95160MA series. The bank currently in use is specified by the register bank pointer (RP), and the lower 3 bits of OP code indicates the general-purpose register 0 (R0) to general-purpose register 7 (R7).

- Register Bank Configuration



## ■ I/O MAP

| Address | Register abbreviation | Register name | R/W | Initial value |
|---|---|---|---|---|
| 0000H | PDR0 | Port 0 data register | R/W | 00000000B |
| 0001H | DDR0 | Port 0 direction register | R/W | 00000000B |
| 0002H | PDR1 | Port 1 data register | R/W | 00000000B |
| 0003H | DDR1 | Port 1 direction register | R/W | 00000000B |
| 0004H | — | (Disabled) | — | — |
| 0005H | WATR | Oscillation stabilization wait time setting register | R/W | 11111111B |
| 0006H | PLLC | PLL control register | R/W | 00000000B |
| 0007H | SYCC | System clock control register | R/W | 1010X011B |
| 0008H | STBC | Standby control register | R/W | 00000000B |
| 0009H | RSRR | Reset factor register | R/W | XXXXXXXXB |
| 000AH | TBTC | Time-base timer control register | R/W | 00000000B |
| 000BH | WPCR | Watch prescaler control register | R/W | 00000000B |
| 000CH | WDTC | Watchdog timer control register | R/W | 00000000B |
| 000DH | — | (Disabled) | — | — |
| 000EH | PDR2 | Port 2 data register | R/W | 00000000B |
| 000FH | DDR2 | Port 2 direction register | R/W | 00000000B |
| 0010H to 0015H | — | (Disabled) | — | — |
| 0016H | PDR6 | Port 6 data register | R/W | 00000000B |
| 0017H | DDR6 | Port 6 direction register | R/W | 00000000B |
| 0018H to 001BH | — | (Disabled) | — | — |
| 001CH | PDR9 | Port 9 data register | R/W | 00000000B |
| 001DH | DDR9 | Port 9 direction register | R/W | 00000000B |
| 001EH | PDRA | Port A data register | R/W | 00000000B |
| 001FH | DDRA | Port A direction register | R/W | 00000000B |
| 0020H | PDRB | Port B data register | R/W | 00000000B |
| 0021H | DDRB | Port B direction register | R/W | 00000000B |
| 0022H | PDRC | Port C data register | R/W | 00000000B |
| 0023H | DDRC | Port C direction register | R/W | 00000000B |
| 0024H to 002CH | — | (Disabled) | — | — |

*(Continued)*

| Address | Register abbreviation | Register name | R/W | Initial value |
|---|---|---|---|---|
| 002D$_H$ | PUL1 | Port 1 pull-up register | R/W | 00000000$_B$ |
| 002E$_H$ | PUL2 | Port 2 pull-up register | R/W | 00000000$_B$ |
| 002F$_H$ to 0035$_H$ | — | (Disabled) | — | — |
| 0036$_H$ | T01CR1 | 8/16-bit compound timer 01 control status register 1 ch.0 | R/W | 00000000$_B$ |
| 0037$_H$ | T00CR1 | 8/16-bit compound timer 00 control status register 1 ch.0 | R/W | 00000000$_B$ |
| 0038$_H$ | T11CR1 | 8/16-bit compound timer 11 control status register 1 ch.1 | R/W | 00000000$_B$ |
| 0039$_H$ | T10CR1 | 8/16-bit compound timer 10 control status register 1 ch.1 | R/W | 00000000$_B$ |
| 003A$_H$ | PC01 | 8/16-bit PPG1 control register ch.0 | R/W | 00000000$_B$ |
| 003B$_H$ | PC00 | 8/16-bit PPG0 control register ch.0 | R/W | 00000000$_B$ |
| 003C$_H$ | PC11 | 8/16-bit PPG1 control register ch.1 | R/W | 00000000$_B$ |
| 003D$_H$ | PC10 | 8/16-bit PPG0 control register ch.1 | R/W | 00000000$_B$ |
| 003E$_H$ to 0041$_H$ | — | (Disabled) | — | — |
| 0042$_H$ | PCNTH0 | 16-bit PPG status control register (upper byte) ch.0 | R/W | 00000000$_B$ |
| 0043$_H$ | PCNTL0 | 16-bit PPG status control register (lower byte) ch.0 | R/W | 00000000$_B$ |
| 0044$_H$ to 0047$_H$ | — | (Disabled) | — | — |
| 0048$_H$ | EIC00 | External interrupt circuit control register ch.0/ch.1 | R/W | 00000000$_B$ |
| 0049$_H$ | EIC10 | External interrupt circuit control register ch.2/ch.3 | R/W | 00000000$_B$ |
| 004A$_H$ | EIC20 | External interrupt circuit control register ch.4/ch.5 | R/W | 00000000$_B$ |
| 004B$_H$ | EIC30 | External interrupt circuit control register ch.6/ch.7 | R/W | 00000000$_B$ |
| 004C$_H$ to 004F$_H$ | — | (Disabled) | — | — |
| 0050$_H$ | SCR | LIN-UART serial control register | R/W | 00000000$_B$ |
| 0051$_H$ | SMR | LIN-UART serial mode register | R/W | 00000000$_B$ |
| 0052$_H$ | SSR | LIN-UART serial status register | R/W | 00001000$_B$ |
| 0053$_H$ | RDR/TDR | LIN-UART reception/transmission data register | R/W | 00000000$_B$ |
| 0054$_H$ | ESCR | LIN-UART extended status control register | R/W | 00000100$_B$ |
| 0055$_H$ | ECCR | LIN-UART extended communication control register | R/W | 000000XX$_B$ |
| 0056$_H$ | SMC10 | UART/SIO serial mode control register 1 ch.0 | R/W | 00000000$_B$ |
| 0057$_H$ | SMC20 | UART/SIO serial mode control register 2 ch.0 | R/W | 00100000$_B$ |
| 0058$_H$ | SSR0 | UART/SIO serial status register ch.0 | R/W | 00000001$_B$ |

*(Continued)*

| Address | Register abbreviation | Register name | R/W | Initial value |
|---|---|---|---|---|
| 0059H | TDR0 | UART/SIO serial output data register ch.0 | R/W | 00000000B |
| 005AH | RDR0 | UART/SIO serial input data register ch.0 | R | 00000000B |
| 005BH to 005FH | — | (Disabled) | — | — |
| 0060H | IBCR00 | I²C bus control register 0 ch.0 | R/W | 00000000B |
| 0061H | IBCR10 | I²C bus control register 1 ch.0 | R/W | 00000000B |
| 0062H | IBSR0 | I²C bus status register ch.0 | R | 00000000B |
| 0063H | IDDR0 | I²C data register ch.0 | R/W | 00000000B |
| 0064H | IAAR0 | I²C address register ch.0 | R/W | 00000000B |
| 0065H | ICCR0 | I²C clock control register ch.0 | R/W | 00000000B |
| 0066H to 006BH | — | (Disabled) | — | — |
| 006CH | ADC1 | 8/10-bit A/D converter control register 1 | R/W | 00000000B |
| 006DH | ADC2 | 8/10-bit A/D converter control register 2 | R/W | 00000000B |
| 006EH | ADDH | 8/10-bit A/D converter data register (upper byte) | R/W | 00000000B |
| 006FH | ADDL | 8/10-bit A/D converter data register (lower byte) | R/W | 00000000B |
| 0070H | WCSR | Watch counter status register | R/W | 00000000B |
| 0071H | — | (Disabled) | — | — |
| 0072H | FSR | Flash memory status register | R/W | 000X0000B |
| 0073H | SWRE0 | Flash memory sector writing control register 0 | R/W | 00000000B |
| 0074H | SWRE1 | Flash memory sector writing control register 1 | R/W | 00000000B |
| 0075H | — | (Disabled) | — | — |
| 0076H | WREN | Wild register address compare enable register | R/W | 00000000B |
| 0077H | WROR | Wild register data test setting register | R/W | 00000000B |
| 0078H | — | Register bank pointer (RP) , Mirror of direct bank pointer (DP) | — | — |
| 0079H | ILR0 | Interrupt level setting register 0 | R/W | 11111111B |
| 007AH | ILR1 | Interrupt level setting register 1 | R/W | 11111111B |
| 007BH | ILR2 | Interrupt level setting register 2 | R/W | 11111111B |
| 007CH | ILR3 | Interrupt level setting register 3 | R/W | 11111111B |
| 007DH | ILR4 | Interrupt level setting register 4 | R/W | 11111111B |
| 007EH | ILR5 | Interrupt level setting register 5 | R/W | 11111111B |
| 007FH | — | (Disabled) | — | — |
| 0F80H | WRARH0 | Wild register address setting register (upper byte) ch.0 | R/W | 00000000B |

*(Continued)*

| Address | Register abbreviation | Register name | R/W | Initial value |
|---|---|---|---|---|
| 0F81H | WRARL0 | Wild register address setting register (lower byte) ch.0 | R/W | 00000000B |
| 0F82H | WRDR0 | Wild register data setting register ch.0 | R/W | 00000000B |
| 0F83H | WRARH1 | Wild register address setting register (upper byte) ch.1 | R/W | 00000000B |
| 0F84H | WRARL1 | Wild register address setting register (lower byte) ch.1 | R/W | 00000000B |
| 0F85H | WRDR1 | Wild register data setting register ch.1 | R/W | 00000000B |
| 0F86H | WRARH2 | Wild register address setting register (upper byte) ch.2 | R/W | 00000000B |
| 0F87H | WRARL2 | Wild register address setting register (lower byte) ch.2 | R/W | 00000000B |
| 0F88H | WRDR2 | Wild register data setting register ch.2 | R/W | 00000000B |
| 0F89H to 0F91H | — | (Disabled) | — | — |
| 0F92H | T01CR0 | 8/16-bit compound timer 01 control status register 0 ch.0 | R/W | 00000000B |
| 0F93H | T00CR0 | 8/16-bit compound timer 00 control status register 0 ch.0 | R/W | 00000000B |
| 0F94H | T01DR | 8/16-bit compound timer 01 data register ch.0 | R/W | 00000000B |
| 0F95H | T00DR | 8/16-bit compound timer 00 data register ch.0 | R/W | 00000000B |
| 0F96H | TMCR0 | 8/16-bit compound timer 00/01 timer mode control register ch.0 | R/W | 00000000B |
| 0F97H | T11CR0 | 8/16-bit compound timer 11 control status register 0 ch.1 | R/W | 00000000B |
| 0F98H | T10CR0 | 8/16-bit compound timer 10 control status register 0 ch.1 | R/W | 00000000B |
| 0F99H | T11DR | 8/16-bit compound timer 11 data register ch.1 | R/W | 00000000B |
| 0F9AH | T10DR | 8/16-bit compound timer 10 data register ch.1 | R/W | 00000000B |
| 0F9BH | TMCR1 | 8/16-bit compound timer 10/11 timer mode control register ch.1 | R/W | 00000000B |
| 0F9CH | PPS01 | 8/16-bit PPG1 cycle setting buffer register ch.0 | R/W | 11111111B |
| 0F9DH | PPS00 | 8/16-bit PPG0 cycle setting buffer register ch.0 | R/W | 11111111B |
| 0F9EH | PDS01 | 8/16-bit PPG1 duty setting buffer register ch.0 | R/W | 11111111B |
| 0F9FH | PDS00 | 8/16-bit PPG0 duty setting buffer register ch.0 | R/W | 11111111B |
| 0FA0H | PPS11 | 8/16-bit PPG1 cycle setting buffer register ch.1 | R/W | 11111111B |
| 0FA1H | PPS10 | 8/16-bit PPG0 cycle setting buffer register ch.1 | R/W | 11111111B |
| 0FA2H | PDS11 | 8/16-bit PPG1 duty setting buffer register ch.1 | R/W | 11111111B |
| 0FA3H | PDS10 | 8/16-bit PPG0 duty setting buffer register ch.1 | R/W | 11111111B |
| 0FA4H | PPGS | 8/16-bit PPG start register | R/W | 00000000B |
| 0FA5H | REVC | 8/16-bit PPG output inversion register | R/W | 00000000B |
| 0FA6H to 0FA9H | — | (Disabled) | — | — |

*(Continued)*

| Address | Register abbreviation | Register name | R/W | Initial value |
|---|---|---|---|---|
| 0FAA$_H$ | PDCRH0 | 16-bit PPG down counter register (upper byte) ch.0 | R | 00000000$_B$ |
| 0FAB$_H$ | PDCRL0 | 16-bit PPG down counter register (lower byte) ch.0 | R | 00000000$_B$ |
| 0FAC$_H$ | PCSRH0 | 16-bit PPG cycle setting buffer register (upper byte) ch.0 | R/W | 11111111$_B$ |
| 0FAD$_H$ | PCSRL0 | 16-bit PPG cycle setting buffer register (lower byte) ch.0 | R/W | 11111111$_B$ |
| 0FAE$_H$ | PDUTH0 | 16-bit PPG duty setting buffer register (upper byte) ch.0 | R/W | 11111111$_B$ |
| 0FAF$_H$ | PDUTL0 | 16-bit PPG duty setting buffer register (lower byte) ch.0 | R/W | 11111111$_B$ |
| 0FB0$_H$ to 0FBB$_H$ | — | (Disabled) | — | — |
| 0FBC$_H$ | BGR1 | LIN-UART baud rate generator register 1 | R/W | 00000000$_B$ |
| 0FBD$_H$ | BGR0 | LIN-UART baud rate generator register 0 | R/W | 00000000$_B$ |
| 0FBE$_H$ | PSSR0 | UART/SIO dedicated baud rate generator prescaler selecting register ch.0 | R/W | 00000000$_B$ |
| 0FBF$_H$ | BRSR0 | UART/SIO dedicated baud rate generator setting register ch.0 | R/W | 00000000$_B$ |
| 0FC0$_H$ to 0FC2$_H$ | — | (Disabled) | — | — |
| 0FC3$_H$ | AIDRL | A/D input disable register (lower byte) | R/W | 00000000$_B$ |
| 0FC4$_H$ | LCDCC | LCDC control register | R/W | 00010000$_B$ |
| 0FC5$_H$ | LCDCE1 | LCDC enable register 1 | R/W | 00110000$_B$ |
| 0FC6$_H$ | LCDCE2 | LCDC enable register 2 | R/W | 00000000$_B$ |
| 0FC7$_H$ | LCDCE3 | LCDC enable register 3 | R/W | 00000000$_B$ |
| 0FC8$_H$ | LCDCE4 | LCDC enable register 4 | R/W | 00000000$_B$ |
| 0FC9$_H$ | LCDCE5 | LCDC enable register 5 | R/W | 00000000$_B$ |
| 0FCA$_H$ | — | (Disabled) | — | — |
| 0FCB$_H$ | LCDCB1 | LCDC blinking setting register 1 | R/W | 00000000$_B$ |
| 0FCC$_H$ | LCDCB2 | LCDC blinking setting register 2 | R/W | 00000000$_B$ |
| 0FCD$_H$ to 0FDC$_H$ | LCDRAM | LCDC display RAM | R/W | 00000000$_B$ |
| 0FDD$_H$ to 0FE2$_H$ | — | (Disabled) | — | — |
| 0FE3$_H$ | WCDR | Watch counter data register | R/W | 00111111$_B$ |

*(Continued)*

*(Continued)*

| Address | Register abbreviation | Register name | R/W | Initial value |
|---|---|---|---|---|
| 0FE4H to 0FE6H | — | (Disabled) | — | — |
| 0FE7H | ILSR2 | Input level select register 2 | R/W | 00000000B |
| 0FE8H, 0FE9H | — | (Disabled) | — | — |
| 0FEAH | CSVCR | Clock supervisor control register | R/W | 00011100B |
| 0FEBH to 0FEDH | — | (Disabled) | — | — |
| 0FEEH | ILSR | Input level selecting register | R/W | 00000000B |
| 0FEFH | WICR | Interrupt pin control register | R/W | 01000000B |
| 0FF0H to 0FFFH | — | (Disabled) | — | — |

• R/W access symbols
  R/W : Readable/Writable
  R : Read only
  W : Write only

• Initial value symbols
  0 : The initial value of this bit is “0”.
  1 : The initial value of this bit is “1”.
  X : The initial value of this bit is undefined.

Note : Do not write to the “ (Disabled) ”. Reading the “ (Disabled) ” returns an undefined value.

## ■ INTERRUPT SOURCE TABLE

| Interrupt source | Interrupt request number | Vector table address | | Bit name of interrupt level setting register | Same level priority order (at simultaneous occurrence) |
|---|---|---|---|---|---|
| | | Upper | Lower | | |
| External interrupt ch.0 | IRQ0 | FFFA$_H$ | FFFB$_H$ | L00 [1 : 0] | High |
| External interrupt ch.4 | | | | | |
| External interrupt ch.1 | IRQ1 | FFF8$_H$ | FFF9$_H$ | L01 [1 : 0] | |
| External interrupt ch.5 | | | | | |
| External interrupt ch.2 | IRQ2 | FFF6$_H$ | FFF7$_H$ | L02 [1 : 0] | |
| External interrupt ch.6 | | | | | |
| External interrupt ch.3 | IRQ3 | FFF4$_H$ | FFF5$_H$ | L03 [1 : 0] | |
| External interrupt ch.7 | | | | | |
| UART/SIO ch.0 | IRQ4 | FFF2$_H$ | FFF3$_H$ | L04 [1 : 0] | |
| 8/16-bit compound timer ch.0 (Lower) | IRQ5 | FFF0$_H$ | FFF1$_H$ | L05 [1 : 0] | |
| 8/16-bit compound timer ch.0 (Upper) | IRQ6 | FFEE$_H$ | FFEF$_H$ | L06 [1 : 0] | |
| LIN-UART (reception) | IRQ7 | FFEC$_H$ | FFED$_H$ | L07 [1 : 0] | |
| LIN-UART (transmission) | IRQ8 | FFEA$_H$ | FFEB$_H$ | L08 [1 : 0] | |
| 8/16-bit PPG ch.1 (Lower) | IRQ9 | FFE8$_H$ | FFE9$_H$ | L09 [1 : 0] | |
| 8/16-bit PPG ch.1 (Upper) | IRQ10 | FFE6$_H$ | FFE7$_H$ | L10 [1 : 0] | |
| (Unused) | IRQ11 | FFE4$_H$ | FFE5$_H$ | L11 [1 : 0] | |
| 8/16-bit PPG ch.0 (Upper) | IRQ12 | FFE2$_H$ | FFE3$_H$ | L12 [1 : 0] | |
| 8/16-bit PPG ch.0 (Lower) | IRQ13 | FFE0$_H$ | FFE1$_H$ | L13 [1 : 0] | |
| 8/16-bit compound timer ch.1 (Upper) | IRQ14 | FFDE$_H$ | FFDF$_H$ | L14 [1 : 0] | |
| 16-bit PPG ch.0 | IRQ15 | FFDC$_H$ | FFDD$_H$ | L15 [1 : 0] | |
| I$^2$C ch.0 | IRQ16 | FFDA$_H$ | FFDB$_H$ | L16 [1 : 0] | |
| (Unused) | IRQ17 | FFD8$_H$ | FFD9$_H$ | L17 [1 : 0] | |
| 8/10-bit A/D converter | IRQ18 | FFD6$_H$ | FFD7$_H$ | L18 [1 : 0] | |
| Time-base timer | IRQ19 | FFD4$_H$ | FFD5$_H$ | L19 [1 : 0] | |
| Watch prescaler/Watch counter | IRQ20 | FFD2$_H$ | FFD3$_H$ | L20 [1 : 0] | |
| (Unused) | IRQ21 | FFD0$_H$ | FFD1$_H$ | L21 [1 : 0] | |
| 8/16-bit compound timer ch.1 (Lower) | IRQ22 | FFCE$_H$ | FFCF$_H$ | L22 [1 : 0] | |
| Flash memory | IRQ23 | FFCC$_H$ | FFCD$_H$ | L23 [1 : 0] | Low |

## ■ ELECTRICAL CHARACTERISTICS

### 1. Absolute Maximum Ratings

| Parameter | Symbol | Rating | | Unit | Remarks |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Power supply voltage*1 | $V_{CC}$, $AV_{CC}$ | Vss − 0.3 | Vss + 6.0 | V | *2 |
| | AVR | Vss − 0.3 | Vss + 6.0 | | *2 |
| Power supply voltage for LCD | V0 to V3 | Vss − 0.3 | Vss + 6.0 | V | *3 |
| Input voltage*1 | $V_I$ | Vss − 0.3 | Vss + 6.0 | V | *4 |
| Output voltage*1 | $V_O$ | Vss − 0.3 | Vss + 6.0 | V | *4 |
| Maximum clamp current | $I_{CLAMP}$ | − 2.0 | + 2.0 | mA | Applicable to pins*5 |
| Total maximum clamp current | $\Sigma\lvert I_{CLAMP}\rvert$ | — | 20 | mA | Applicable to pins*5 |
| “L” level maximum output current | $I_{OL}$ | — | 15 | mA | Applicable to pins*5 |
| “L” level average current | $I_{OLAV}$ | — | 4 | mA | Applicable to pins*5<br>Average output current = operating current × operating ratio (1 pin) |
| “L” level total maximum output current | $\Sigma I_{OL}$ | — | 100 | mA | |
| “L” level total average output current | $\Sigma I_{OLAV}$ | — | 50 | mA | Total average output current = operating current × operating ratio (Total of pins) |
| “H” level maximum output current | $I_{OH}$ | — | − 15 | mA | Applicable to pins*5 |
| “H” level average current | $I_{OHAV}$ | — | − 4 | mA | Applicable to pins*5<br>Average output current = operating current × operating ratio (1 pin) |
| “H” level total maximum output current | $\Sigma I_{OH}$ | — | − 100 | mA | |
| “H” level total average output current | $\Sigma I_{OHAV}$ | — | − 50 | mA | Total average output current = operating current × operating ratio (Total of pins) |
| Power consumption | Pd | — | 320 | mW | |
| Operating temperature | $T_A$ | − 40 | + 85 | °C | |
| Storage temperature | Tstg | − 55 | + 150 | °C | |

*(Continued)*

*(Continued)*

*1 : The parameter is based on $V_{SS}$ = 0.0 V.

*2 : Apply equal potential to $AV_{CC}$ and $V_{CC}$. AVR should not exceed $AV_{CC}$ + 0.3 V.

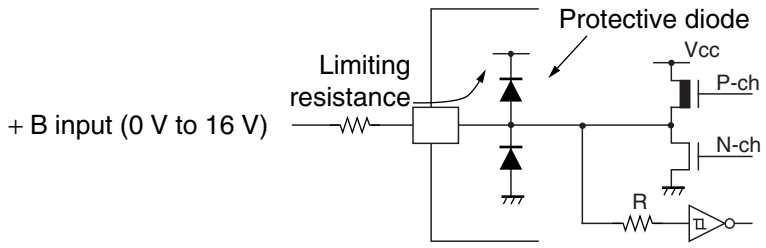
*3 : V0 to V3 should not exceed $V_{CC}$ + 0.3 V.

*4 : $V_I$ and Vo should not exceed $V_{CC}$ + 0.3 V. $V_I$ must not exceed the rating voltage. However, if the maximum current to/from an input is limited by some means with external components, the $I_{CLAMP}$ rating supersedes the $V_I$ rating.

*5 : Applicable to pins :
P00 to P07, P10 to P14, P20 to P22,P60 to P67, P90 to P95, PA0 to PA3, PB0 to PB7, PC0 to PC7

- Use within recommended operating conditions.
- Use at DC voltage (current).
- + B signal is an input signal that exceeds $V_{CC}$ voltage. The + B signal should always be applied a limiting resistance placed between the + B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the + B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the $V_{CC}$ pin, and this affects other devices.
- Note that if the + B signal is inputted when the microcontroller power supply is off (not fixed at 0 V), the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the + B input is applied during power-on, the power supply is provided from the pins and the resulting power supply voltage may not be sufficient to operate the power-on reset.
- Care must be taken not to leave the + B input pin open.
- Note that analog system input/output pins other than the A/D input pins (LCD drive pins, etc.) cannot accept + B signal input.
- Sample recommended circuits :

- Input/Output Equivalent circuits




WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

## 2. Recommended Operating Conditions

(Vss = 0.0 V)

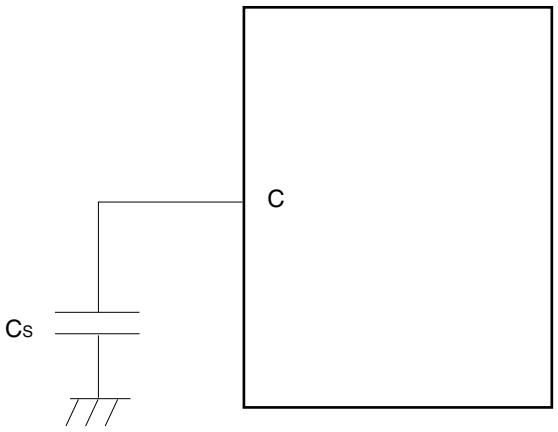
| Parameter | Symbol | Condi-tions | Value Min | Value Max | Unit | Remarks | |
|---|---|---|---|---|---|---|---|
| Power supply voltage | $V_{CC}$, $AV_{CC}$ | — | 2.42*1,*2 | 5.5*1 | V | In normal operating | Other than MB95FV100D-103 |
| | | | 2.3 | 5.5 | | Hold condition in STOP mode | |
| | | | 2.7 | 5.5 | | In normal operating | MB95FV100D-103 |
| | | | 2.3 | 5.5 | | Hold condition in STOP mode | |
| Power supply voltage for LCD | V0 to V3 | | $V_{SS}$ | $V_{CC}$ | V | The range of liquid crystal power supply (The optimal value depends on liquid crystal display elements used.) | |
| A/D converter reference input voltage | AVR | | 4.0 | $AV_{CC}$ | V | | |
| Smoothing capacitor | $C_S$ | | 0.1 | 1.0 | µF | *3 | |
| Operating temperature | $T_A$ | | − 40 | + 85 | °C | Other than MB95FV100D-103 | |
| | | | + 5 | +35 | °C | MB95FV100D-103 | |

*1 : The values vary with the operating frequency, machine clock or analog guarantee range.

*2 : When the low voltage detection reset is used, reset occurs while the low voltage is detected. For details on Low voltage detection, see "(9) Low Voltage Detection" in "4. AC Characteristics ".

*3 : Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. A bypass capacitor of $V_{CC}$ pin must have a capacitor value higher than $C_S$. For connection of smoothing capacitor $C_S$, refer to the diagram below.

• C pin connection diagram




WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

### 3. DC Characteristics

(Vcc = 5.0 V ± 10%, Vss = 0.0 V, $T_A$ = − 40 °C to + 85 °C)

| Parameter | Symbol | Pin name | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| "H" level input voltage | $V_{IH1}$ | P10, P67 | *1 | 0.7 $V_{CC}$ | — | $V_{CC}$ + 0.3 | V | When selecting CMOS input level |
| | $V_{IH2}$ | P23, P24 | *1 | 0.7 $V_{CC}$ | — | $V_{SS}$ + 5.5 | V | |
| | $V_{IHA}$ | P00 to P07, P10 to P14, P20 to P22, P60 to P67, P90 to P95, PA0 to PA3, PB0 to PB7, PC0 to PC7 | — | 0.8 $V_{CC}$ | — | $V_{CC}$ + 0.3 | V | Port inputs if Automotive input levels are selected |
| | $V_{IHS1}$ | P00 to P07, P10 to P14, P20 to P22, P60 to P67, P90 to P95, PA0 to PA3, PB0 to PB7, PC0 to PC7 | *1 | 0.8 $V_{CC}$ | — | $V_{CC}$ + 0.3 | V | Hysteresis input |
| | $V_{IHS2}$ | P23, P24 | *1 | 0.8 $V_{CC}$ | — | $V_{SS}$ + 5.5 | V | |
| | $V_{IHM}$ | $\overline{RST}$, MOD | — | 0.8 $V_{CC}$ | — | $V_{CC}$ + 0.3 | V | |
| "L" level input voltage | $V_{IL}$ | P10,P23, P24,P67 | *1 | $V_{SS}$ − 0.3 | — | 0.3 $V_{CC}$ | V | Hysteresis input (When selecting CMOS input level) |
| | $V_{ILA}$ | P00 to P07, P10 to P14, P20 to P24, P60 to P67, P90 to P95, PA0 to PA3, PB0 to PB7, PC0 to PC7 | — | $V_{SS}$ − 0.3 | — | 0.5 $V_{CC}$ | V | Port inputs if Automotive input levels are selected |
| | $V_{ILS}$ | P00 to P07, P10 to P14, P20 to P24, P60 to P67, P90 to P95, PA0 to PA3, PB0 to PB7, PC0 to PC7 | *1 | $V_{SS}$ − 0.3 | — | 0.2 $V_{CC}$ | V | Hysteresis input |
| | $V_{ILM}$ | $\overline{RST}$, MOD | — | $V_{SS}$ − 0.3 | — | 0.3 $V_{CC}$ | V | Hysteresis input |
| "H" level output voltage | $V_{OH}$ | All output pins | $I_{OH}$ = − 4.0 mA | $V_{cc}$ − 0.5 | — | — | V | |
| "L" level output voltage | $V_{OL}$ | $\overline{RST}$*2, All output pins | $I_{OL}$ = 4.0 mA | — | — | 0.4 | V | |

*(Continued)*

(Vcc = 5.0 V ± 10%, Vss = 0.0 V, $T_A$ = − 40 °C to + 85 °C)

| Parameter | Symbol | Pin name | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Input leakage current (Hi-Z output leakage current) | $I_{LI}$ | Ports other than P23, P24 | 0.0 V < $V_I$ < $V_{CC}$ | − 5 | — | + 5 | µA | When the pull-up prohibition setting |
| Open drain output leakage current | $I_{LIOD}$ | P23, P24 | 0.0 V < $V_I$ < $V_{SS}$ + 5.5 V | — | — | 5 | µA | |
| Pull-up resistor | $R_{PULL}$ | P10 to P14, P20 to P22 | $V_I$ = 0.0 V | 25 | 50 | 100 | kΩ | When the pull-up permission setting |
| Pull-down resistor | $R_{MOD}$ | MOD | $V_I$ = $V_{CC}$ | 50 | 100 | 200 | kΩ | Mask ROM product only |
| Input capacitance | $C_{IN}$ | Other than $AV_{CC}$, $AV_{SS}$, AVR, $V_{CC}$, $V_{SS}$ | f = 1 MHz | — | 5 | 15 | pF | |
| Power supply current*3 | $I_{CC}$ | $V_{CC}$ (External clock operation) | $F_{CH}$ = 20 MHz $F_{MP}$ = 10 MHz Main clock mode (divided by 2) | — | 9.5 | 12.5 | mA | Flash memory product (At other than Flash memory writing and erasing) |
| | | | | — | 30.0 | 35.0 | mA | Flash memory product (At Flash memory writing and erasing) |
| | | | | — | 7.2 | 9.5 | mA | Mask ROM product |
| | | | $F_{CH}$ = 32 MHz $F_{MP}$ = 16 MHz Main clock mode (divided by 2) | — | 15.2 | 20.0 | mA | Flash memory product (At other than Flash memory writing and erasing) |
| | | | | — | 35.7 | 42.5 | mA | Flash memory product (At Flash memory writing and erasing) |
| | | | | — | 11.6 | 15.2 | mA | Mask ROM product |
| | $I_{CCS}$ | | $F_{CH}$ = 20 MHz $F_{MP}$ = 10 MHz Main Sleep mode (divided by 2) | — | 4.5 | 7.5 | mA | |
| | | | $F_{CH}$ = 32 MHz $F_{MP}$ = 16 MHz Main Sleep mode (divided by 2) | — | 7.2 | 12.0 | mA | |

*(Continued)*

(Vcc = 5.0 V ± 10%, Vss = 0.0 V, $T_A$ = − 40 °C to + 85 °C)

| Parameter | Symbol | Pin name | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Power supply current*3 | $I_{CCL}$ | $V_{CC}$ (External clock operation) | $F_{CL}$ = 32 kHz<br>$F_{MPL}$ = 16 kHz<br>Sub clock mode (divided by 2)<br>$T_A$ = + 25 °C | — | 45 | 100 | µA | |
| | $I_{CCLS}$ | | $F_{CL}$ = 32 kHz<br>$F_{MPL}$ = 16 kHz<br>Sub sleep mode (divided by 2)<br>$T_A$ = + 25 °C | — | 10 | 81 | µA | |
| | $I_{CCT}$ | | $F_{CL}$ = 32 kHz<br>Watch mode<br>Main stop mode<br>$T_A$ = + 25 °C | — | 4.6 | 27.0 | µA | |
| | $I_{CCMPLL}$ | | $F_{CH}$ = 4 MHz<br>$F_{MP}$ = 10 MHz<br>Main PLL mode (multiplied by 2.5) | — | 9.3 | 12.5 | mA | Flash memory product |
| | | | | — | 7 | 9.5 | mA | Mask ROM product |
| | | | $F_{CH}$ = 6.4 MHz<br>$F_{MP}$ = 16 MHz<br>Main PLL mode (multiplied by 2.5) | — | 14.9 | 20.0 | mA | Flash memory product |
| | | | | — | 11.2 | 15.2 | mA | Mask ROM product |
| | $I_{CCSPLL}$ | | $F_{CL}$ = 32 kHz<br>$F_{MPL}$ = 128 kHz<br>Sub PLL mode (multiplied by 4),<br>$T_A$ = + 25 °C | — | 160 | 400 | µA | |
| | $I_{CTS}$ | | $F_{CH}$ = 10 MHz<br>Time-base timer mode<br>$T_A$ = + 25 °C | — | 0.15 | 1.10 | mA | |
| | $I_{CCH}$ | | Sub stop mode<br>$T_A$ = + 25 °C | — | 5 | 20 | µA | |
| | $I_A$ | $AV_{CC}$ | $F_{CH}$ = 16 MHz<br>At operating of A/D conversion | — | 2.4 | 4.7 | mA | |
| | $I_{AH}$ | | $F_{CH}$ = 16 MHz<br>At stopping of A/D conversion<br>$T_A$ = + 25 °C | — | 1 | 5 | µA | |
| LCD internal division resistance | $R_{LCD}$ | — | Between V3 and $V_{SS}$ | — | 300 | — | kΩ | |
| COM0 to COM3 output impedance | $R_{VCOM}$ | COM0 to COM3 | V1 to V3 = 5.0 V | — | — | 5 | kΩ | |
| SEG00 to SEG31 output impedance | $R_{VSEG}$ | SEG00 to SEG31 | | — | — | 7 | kΩ | |

*(Continued)*

*(Continued)*

| Parameter | Symbol | Pin name | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| LCD leak current | $I_{LCDL}$ | V0 to V3, COM0 to COM3 SEG00 to SEG31 | — | − 1 | — | + 1 | µA | |

*1 : The input level of P10, P23, P24 and P67 can be switched to either the “CMOS input level” or “hysteresis input level”. The switching of the input level can be set by the input level selection register (ILSR) .

*2 : Product without clock supervisor only

*3 :
- The power-supply current is determined by the external clock. When both low voltage detection option and clock supervisor option are selected, the power-supply current will be a value of adding current consumption of the low voltage detection circuit ($I_{LVD}$) and current consumption of built-in CR oscillator ($I_{CSV}$) to the specified value.
- Refer to “4. AC Characteristics (1) Clock Timing” for $F_{CH}$ and $F_{CL}$.
- Refer to “4. AC Characteristics (2) Source Clock/Machine Clock” for $F_{MP}$ and $F_{MPL}$.

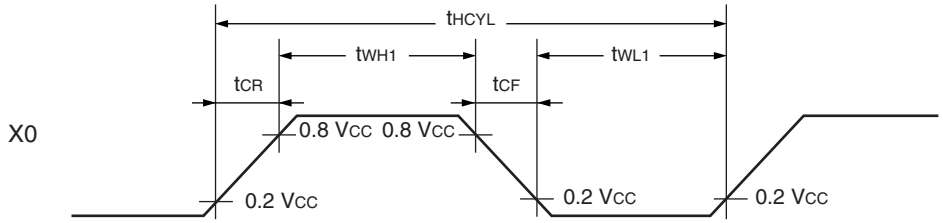
## 4. AC Characteristics

### (1) Clock Timing

(Vcc = 2.42 V to 5.5 V, Vss = 0.0 V, $T_A$ = − 40 °C to + 85 °C)

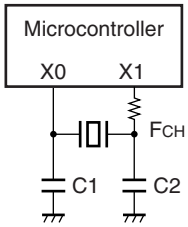
| Parameter | Symbol | Pin name | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Clock frequency | $F_{CH}$ | X0, X1 | — | 1.00 | — | 16.25 | MHz | When using main oscillation circuit |
| | | | | 1.00 | — | 32.50 | MHz | When using external clock |
| | | | | 3.00 | — | 10.00 | MHz | Main PLL multiplied by 1 |
| | | | | 3.00 | — | 8.13 | MHz | Main PLL multiplied by 2 |
| | | | | 3.00 | — | 6.50 | MHz | Main PLL multiplied by 2.5 |
| | | | | 3.00 | — | 4.06 | MHz | Main PLL multiplied by 4 |
| | $F_{CL}$ | X0A, X1A | | — | 32.768 | — | kHz | When using sub oscillation circuit |
| | | | | — | 32.768 | — | kHz | When using sub PLL |
| Clock cycle time | $t_{HCYL}$ | X0, X1 | | 61.5 | — | 1000 | ns | When using oscillation circuit |
| | | | | 30.8 | — | 1000 | ns | When using external clock |
| | $t_{LCYL}$ | X0A, X1A | | — | 30.5 | — | µs | When using sub clock |
| Input clock pulse width | $t_{WH1}$ $t_{WL1}$ | X0 | | 61.5 | — | — | ns | When using external clock Duty ratio is about 30% to 70%. |
| | $t_{WH2}$ $t_{WL2}$ | X0A | | — | 15.2 | — | µs | |
| Input clock rise time and fall time | $t_{CR}$ $t_{CF}$ | X0, X0A | | — | — | 5 | ns | When using external clock |

• Input wave form for using external clock (main clock)

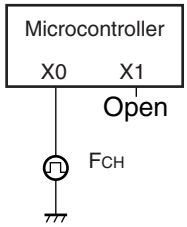



• Figure of Main Clock Input Port External Connection

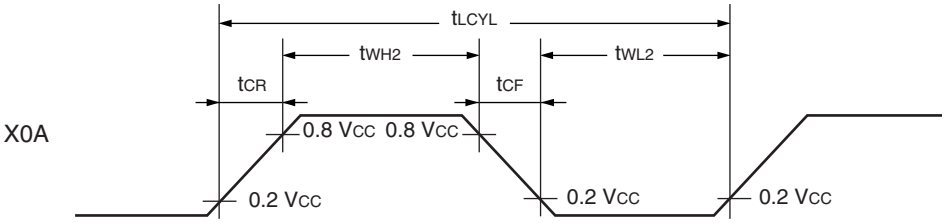
When using a crystal or ceramic oscillator




When using external clock

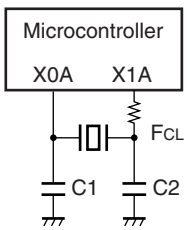



• Input wave form for using external clock (sub clock)

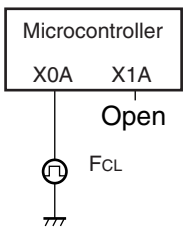



• Figure of Sub clock Input Port External Connection

When using a crystal or ceramic oscillator




When using external clock



### (2) Source Clock/Machine Clock

(Vcc = 5.0 V ± 10%, Vss = 0.0 V, $T_A$ = − 40 °C to + 85 °C)

| Parameter | Symbol | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Source clock cycle time*1 (Clock before setting division) | $t_{SCLK}$ | — | 61.5 | — | 2000 | ns | When using main clock<br>Min : $F_{CH}$ = 8.125 MHz, PLL multiplied by 2<br>Max : $F_{CH}$ = 1 MHz, divided by 2 |
| | | | 7.6 | — | 61.0 | µs | When using sub clock<br>Min : $F_{CL}$ = 32 kHz, PLL multiplied by 4<br>Max : $F_{CL}$ = 32 kHz, divided by 2 |
| Source clock frequency | $F_{SP}$ | | 0.50 | — | 16.25 | MHz | When using main clock |
| | $F_{SPL}$ | | 16.384 | — | 131.072 | kHz | When using sub clock |
| Machine clock cycle time*2 (Minimum instruction execution time) | $t_{MCLK}$ | | 61.5 | — | 32000 | ns | When using main clock<br>Min : $F_{SP}$ = 16.25 MHz, no division<br>Max : $F_{SP}$ = 0.5 MHz, divided by 16 |
| | | | 7.6 | — | 976.5 | µs | When using sub clock<br>Min : $F_{SPL}$ = 131 kHz, no division<br>Max : $F_{SPL}$ = 16 kHz, divided by 16 |
| Machine clock frequency | $F_{MP}$ | | 0.031 | — | 16.250 | MHz | When using main clock |
| | $F_{MPL}$ | | 1.024 | — | 131.072 | kHz | When using sub clock |

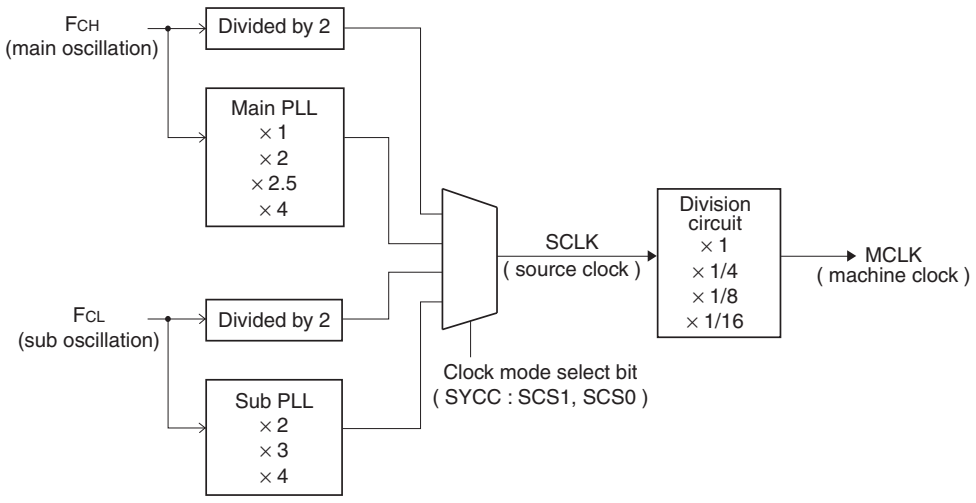
*1 : Clock before setting division due to machine clock division ratio selection bit (SYCC : DIV1 and DIV0) . This source clock is divided by the machine clock division ratio selection bit (SYCC : DIV1 and DIV0) , and it becomes the machine clock. Further, the source clock can be selected as follows.

- Main clock divided by 2
- PLL multiplication of main clock (select from 1, 2, 2.5, 4 multiplication)
- Sub clock divided by 2
- PLL multiplication of sub clock (select from 2, 3, 4 multiplication)

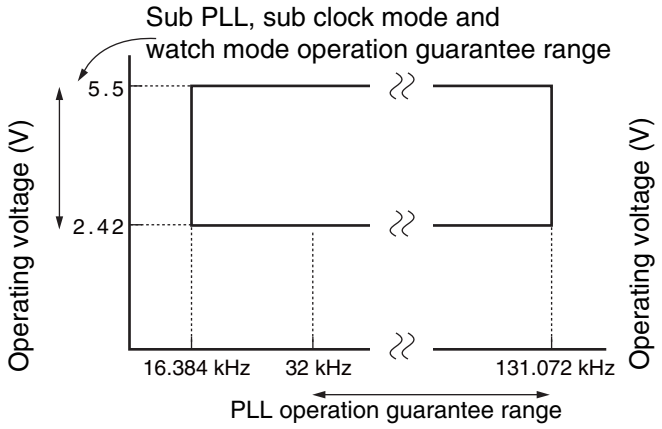
*2 : Operation clock of the microcontroller. Machine clock can be selected as follows.

- Source clock (no division)
- Source clock divided by 4
- Source clock divided by 8
- Source clock divided by 16

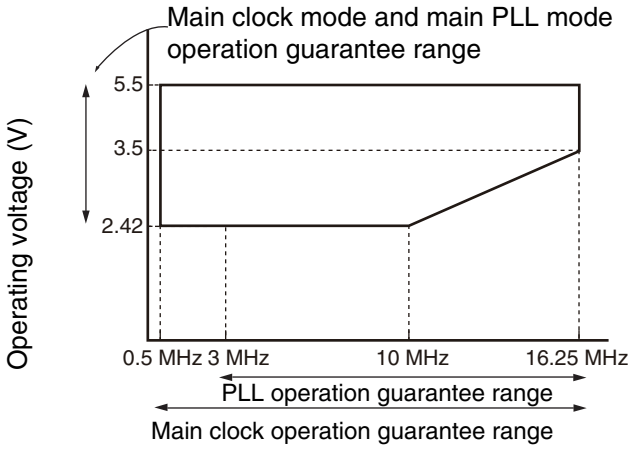
• Outline of clock generation block



• Operating voltage - Operating frequency (When $T_A$ = − 40 °C to + 85 °C)
  • MB95168MA/F168MA/F168NA/F168JA

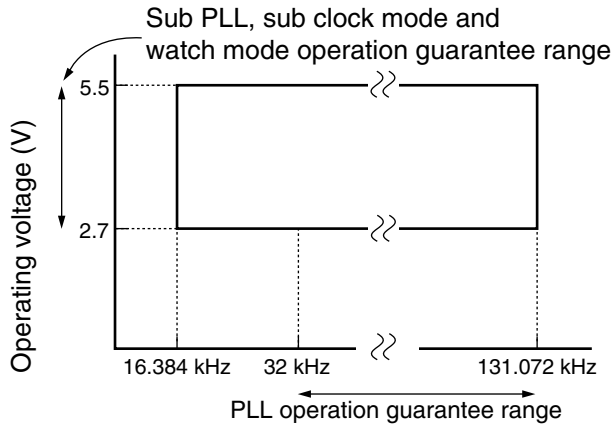



Source clock frequency ($F_{SPL}$)

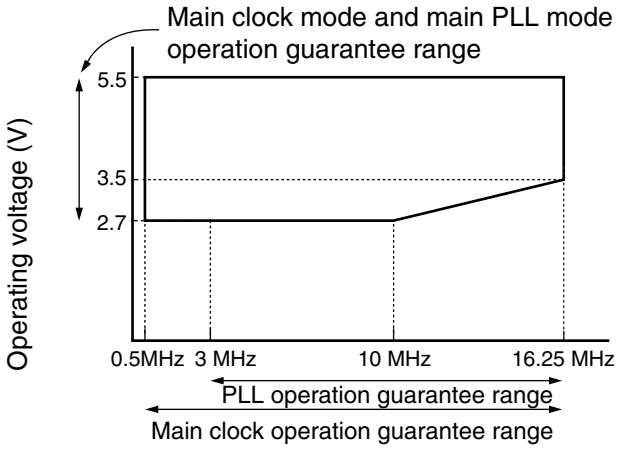



Source clock frequency ($F_{SP}$)

• Operating voltage - Operating frequency (When $T_A$ = + 5 °C to + 35 °C)
  • MB95FV100D-103

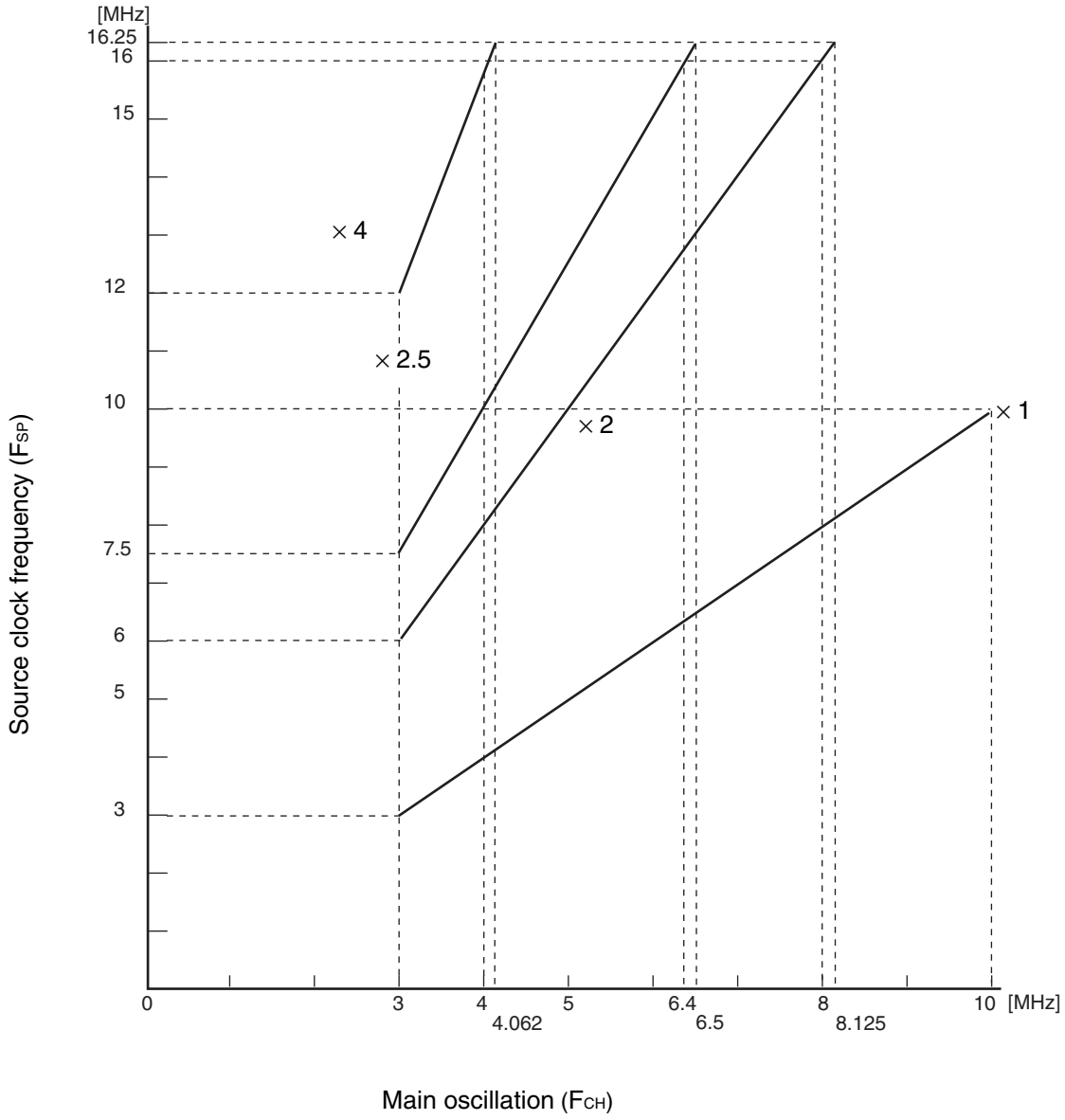



Source clock frequency ($F_{SPL}$)




Source clock frequency ($F_{SP}$)

• Main PLL operation frequency



### (3) External Reset

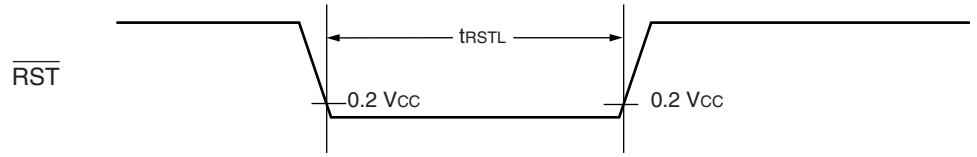
(Vcc = 5.0 V ± 10%, Vss = 0.0 V, $T_A$ = − 40 °C to + 85 °C)

| Parameter | Symbol | Pin name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| $\overline{RST}$ "L" level pulse width | $t_{RSTL}$ | $\overline{RST}$ | — | 2 $t_{MCLK}$*1 | — | ns | At normal operating |
| | | | | Oscillation time of oscillator*2 + 100 | — | µs | At stop mode, sub clock mode, sub sleep mode, and watch mode |
| | | | | 100 | — | µs | At time-base timer mode |

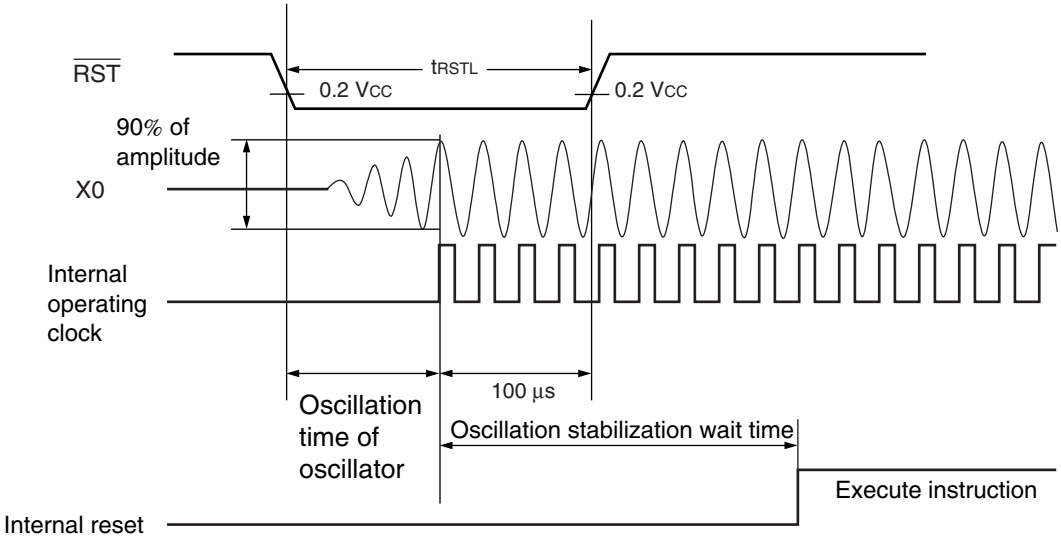
*1 : Refer to " (2) Source Clock/Machine Clock" for $t_{MCLK}$.

*2 : Oscillation time of oscillator is the time that the amplitude reaches 90%. In the crystal oscillator, the oscillation time is between several ms and tens of ms. In ceramic oscillators, the oscillation time is between hundreds of µs and several ms. In the external clock, the oscillation time is 0 ms.

• At normal operating



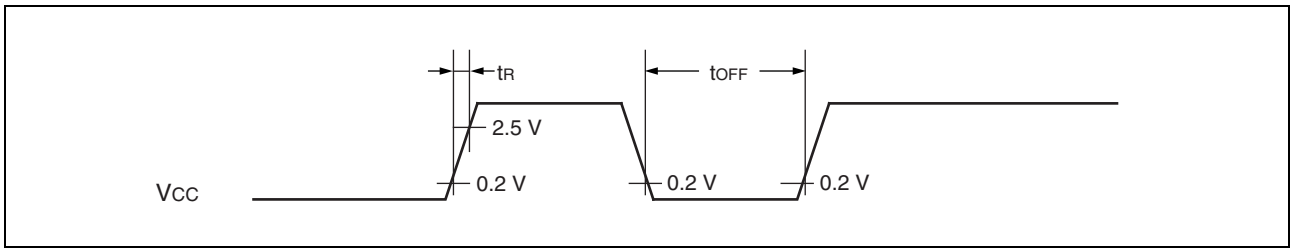

• At stop mode, sub clock mode, sub sleep mode, watch mode, and power-on



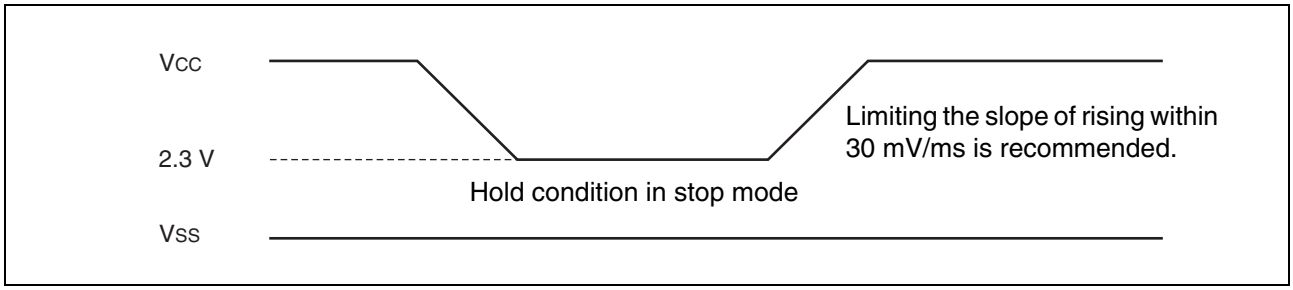
### (4) Power-on Reset

(Vss = 0.0 V, $T_A$ = − 40 °C to + 85 °C)

| Parameter | Symbol | Pin name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Power supply rising time | $t_R$ | $V_{CC}$ | — | — | 50 | ms | |
| Power supply cutoff time | $t_{OFF}$ | | | 1 | — | ms | Waiting time until power-on |




Note : Sudden change of power supply voltage may activate the power-on reset function. When changing power supply voltages during operation, set the slope of rising within 30 mV/ms as shown below.

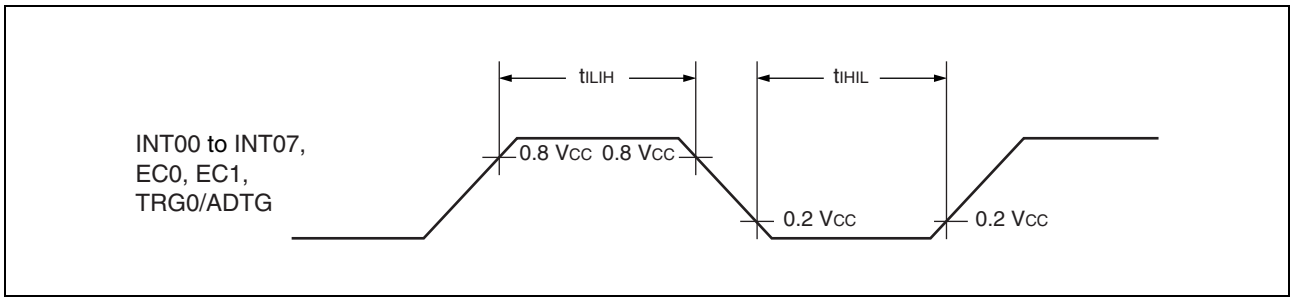


### (5) Peripheral Input Timing

(Vcc = 5.0 V ± 10%, Vss = 0.0 V, $T_A$ = − 40 °C to + 85 °C)

| Parameter | Symbol | Pin name | Conditions | Value | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| Peripheral input “H” pulse width | $t_{ILIH}$ | INT00 to INT07, EC0, EC1, TRG0/ADTG | — | 2 $t_{MCLK}$* | — | ns |
| Peripheral input “L” pulse width | $t_{IHIL}$ | | | 2 $t_{MCLK}$* | — | ns |

* : Refer to “ (2) Source Clock/Machine Clock” for $t_{MCLK}$.



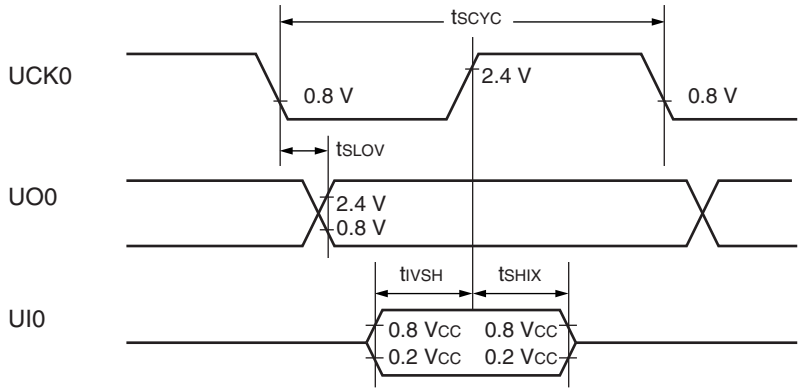
### (6) UART/SIO, Serial I/O Timing

(Vcc = 5.0 V ± 10%, Vss = 0.0 V, $T_A$ = − 40 °C to + 85 °C)

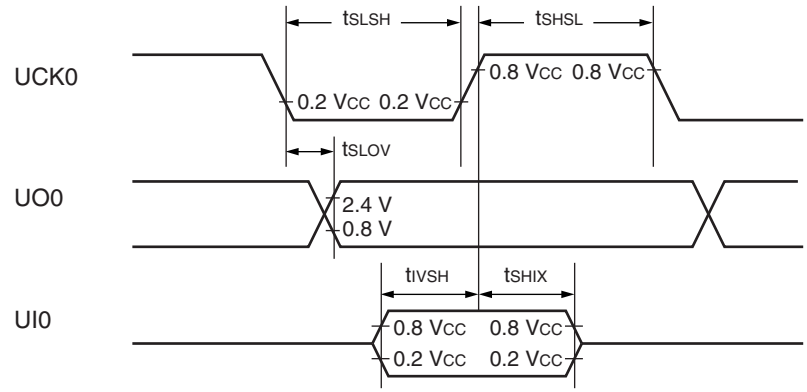
| Parameter | Symbol | Pin name | Conditions | Value | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| Serial clock cycle time | $t_{SCYC}$ | UCK0 | Internal clock operation output pin : $C_L$ = 80 pF + 1TTL. | 4 $t_{MCLK}$* | — | ns |
| UCK ↓ → UO time | $t_{SLOV}$ | UCK0, UO0 | | − 190 | + 190 | ns |
| Valid UI → UCK ↑ | $t_{IVSH}$ | UCK0, UI0 | | 2 $t_{MCLK}$* | — | ns |
| UCK ↑ → valid UI hold time | $t_{SHIX}$ | UCK0, UI0 | | 2 $t_{MCLK}$* | — | ns |
| Serial clock “H” pulse width | $t_{SHSL}$ | UCK0 | External clock operation output pin : $C_L$ = 80 pF + 1TTL. | 4 $t_{MCLK}$* | — | ns |
| Serial clock “L” pulse width | $t_{SLSH}$ | UCK0 | | 4 $t_{MCLK}$* | — | ns |
| UCK ↓ → UO time | $t_{SLOV}$ | UCK0, UO0 | | — | 190 | ns |
| Valid UI → UCK ↑ | $t_{IVSH}$ | UCK0, UI0 | | 2 $t_{MCLK}$* | — | ns |
| UCK ↑ → valid UI hold time | $t_{SHIX}$ | UCK0, UI0 | | 2 $t_{MCLK}$* | — | ns |

* : Refer to “ (2) Source Clock/Machine Clock” for $t_{MCLK}$.

• Internal shift clock mode




• External shift clock mode



### (7) LIN-UART Timing

**Sampling at the rising edge of sampling clock*1 and prohibited serial clock delay*2**
**(ESCR register : SCES bit = 0, ECCR register : SCDE bit = 0)**

(Vcc = 5.0 V ± 10%, Vss = 0.0 V, $T_A$ = –40 °C to + 85 °C)

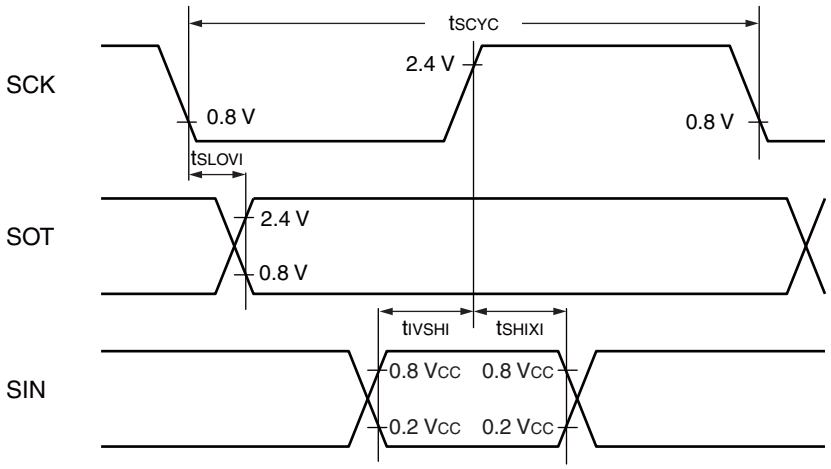
| Parameter | Symbol | Pin name | Conditions | Value | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| Serial clock cycle time | $t_{SCYC}$ | SCK | Internal clock operation output pin : $C_L$ = 80 pF + 1 TTL. | 5 $t_{MCLK}$*3 | — | ns |
| SCK ↓ → SOT delay time | $t_{SLOVI}$ | SCK, SOT | | –95 | + 95 | ns |
| Valid SIN → SCK ↑ | $t_{IVSHI}$ | SCK, SIN | | $t_{MCLK}$*3 + 190 | — | ns |
| SCK ↑ → valid SIN hold time | $t_{SHIXI}$ | SCK, SIN | | 0 | — | ns |
| Serial clock “L” pulse width | $t_{SLSH}$ | SCK | External clock operation output pin : $C_L$ = 80 pF + 1 TTL. | 3 $t_{MCLK}$*3 – $t_R$ | — | ns |
| Serial clock “H” pulse width | $t_{SHSL}$ | SCK | | $t_{MCLK}$*3 + 95 | — | ns |
| SCK ↓ → SOT delay time | $t_{SLOVE}$ | SCK, SOT | | — | 2 $t_{MCLK}$*3 + 95 | ns |
| Valid SIN → SCK ↑ | $t_{IVSHE}$ | SCK, SIN | | 190 | — | ns |
| SCK ↑ → valid SIN hold time | $t_{SHIXE}$ | SCK, SIN | | $t_{MCLK}$*3 + 95 | — | ns |
| SCK fall time | $t_F$ | SCK | | — | 10 | ns |
| SCK rise time | $t_R$ | SCK | | — | 10 | ns |

*1 : Provide switch function whether sampling of reception data is performed at rising edge or falling edge of the serial clock.

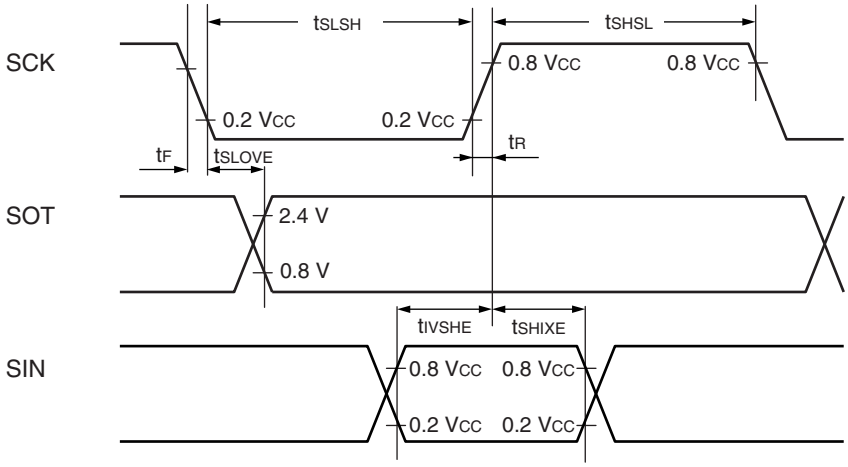
*2 : Serial clock delay function is used to delay half clock for the output signal of serial clock.

*3 : Refer to “ (2) Source Clock/Machine Clock” for $t_{MCLK}$.

- Internal shift clock mode




- External shift clock mode



**Sampling at the falling edge of sampling clock*1 and prohibited serial clock delay*2**
**(ESCR register : SCES bit = 1, ECCR register : SCDE bit = 0)**

($V_{CC}$ = 5.0 V ± 10%, $V_{SS}$ = 0.0 V, $T_A$ = –40 °C to + 85 °C)

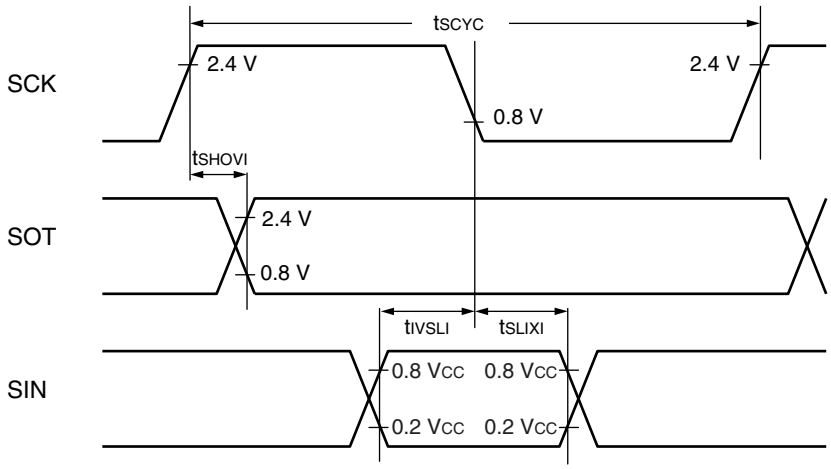
| Parameter | Symbol | Pin name | Conditions | Value | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| Serial clock cycle time | $t_{SCYC}$ | SCK | Internal clock operation output pin : $C_L$ = 80 pF + 1 TTL. | 5 $t_{MCLK}$*3 | — | ns |
| SCK↑→ SOT delay time | $t_{SHOVI}$ | SCK, SOT | | –95 | + 95 | ns |
| Valid SIN→SCK↓ | $t_{IVSLI}$ | SCK, SIN | | $t_{MCLK}$*3 + 190 | — | ns |
| SCK↓→ valid SIN hold time | $t_{SLIXI}$ | SCK, SIN | | 0 | — | ns |
| Serial clock “H” pulse width | $t_{SHSL}$ | SCK | External clock operation output pin : $C_L$ = 80 pF + 1 TTL. | 3 $t_{MCLK}$*3 – $t_R$ | — | ns |
| Serial clock “L” pulse width | $t_{SLSH}$ | SCK | | $t_{MCLK}$*3 + 95 | — | ns |
| SCK↑ →SOT delay time | $t_{SHOVE}$ | SCK, SOT | | — | 2 $t_{MCLK}$*3 + 95 | ns |
| Valid SIN→SCK↓ | $t_{IVSLE}$ | SCK, SIN | | 190 | — | ns |
| SCK↓→ valid SIN hold time | $t_{SLIXE}$ | SCK, SIN | | $t_{MCLK}$*3 + 95 | — | ns |
| SCK fall time | $t_F$ | SCK | | — | 10 | ns |
| SCK rise time | $t_R$ | SCK | | — | 10 | ns |

*1 : Provide switch function whether sampling of reception data is performed at rising edge or falling edge of the serial clock.

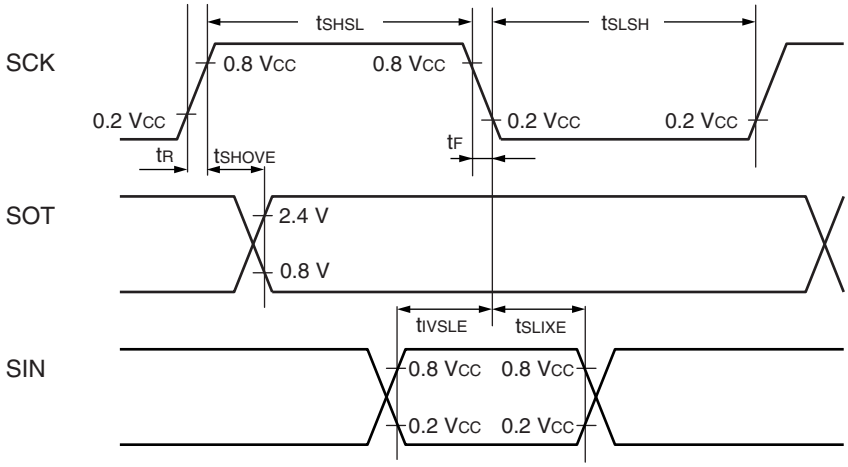
*2 : Serial clock delay function is used to delay half clock for the output signal of serial clock.

*3 : Refer to “ (2) Source Clock/Machine Clock” for $t_{MCLK}$.

- Internal shift clock mode




- External shift clock mode



**Sampling at the rising edge of sampling clock*1 and enabled serial clock delay*2**
**(ESCR register : SCES bit = 0, ECCR register : SCDE bit = 1)**

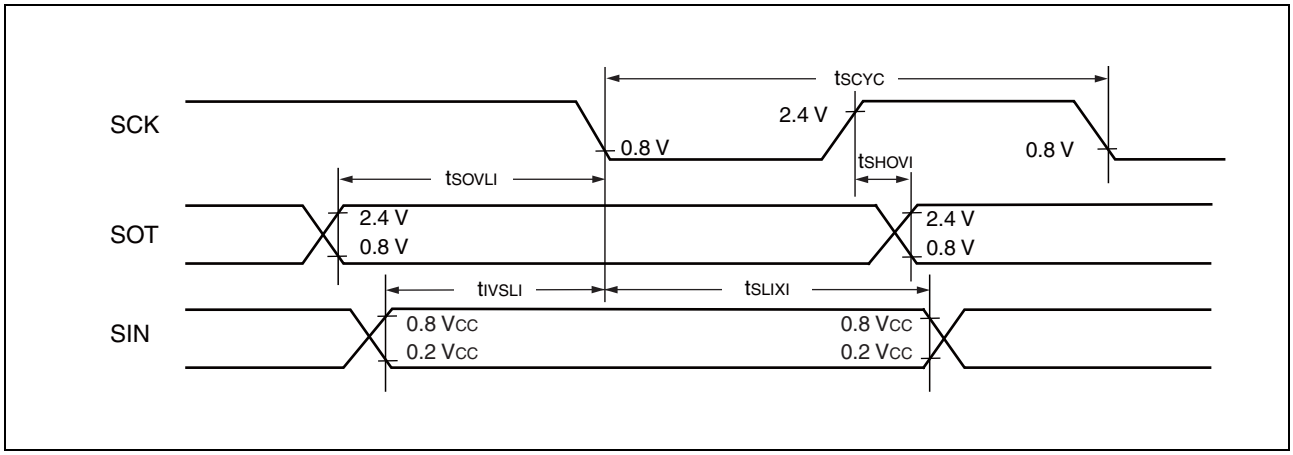
($V_{CC}$ = 5.0 V ± 10%, $V_{SS}$ = 0.0 V, $T_A$ = –40 °C to + 85 °C)

| Parameter | Symbol | Pin name | Conditions | Value | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| Serial clock cycle time | $t_{SCYC}$ | SCK | Internal clock operation output pin : $C_L$ = 80 pF + 1 TTL. | 5 $t_{MCLK}$*3 | — | ns |
| SCK↑→ SOT delay time | $t_{SHOVI}$ | SCK, SOT | | –95 | + 95 | ns |
| Valid SIN→SCK↓ | $t_{IVSLI}$ | SCK, SIN | | $t_{MCLK}$*3 + 190 | — | ns |
| SCK↓→ valid SIN hold time | $t_{SLIXI}$ | SCK, SIN | | 0 | — | ns |
| SOT→SCK↓ delay time | $t_{SOVLI}$ | SCK, SOT | | — | 4 $t_{MCLK}$*3 | ns |

*1 : Provide switch function whether sampling of reception data is performed at rising edge or falling edge of the serial clock.

*2 : Serial clock delay function is used to delay half clock for the output signal of serial clock.

*3 : Refer to " (2) Source Clock/Machine Clock" for $t_{MCLK}$.



**Sampling at the falling edge of sampling clock*1 and enabled serial clock delay*2**
**(ESCR register : SCES bit = 1, ECCR register : SCDE bit = 1)**

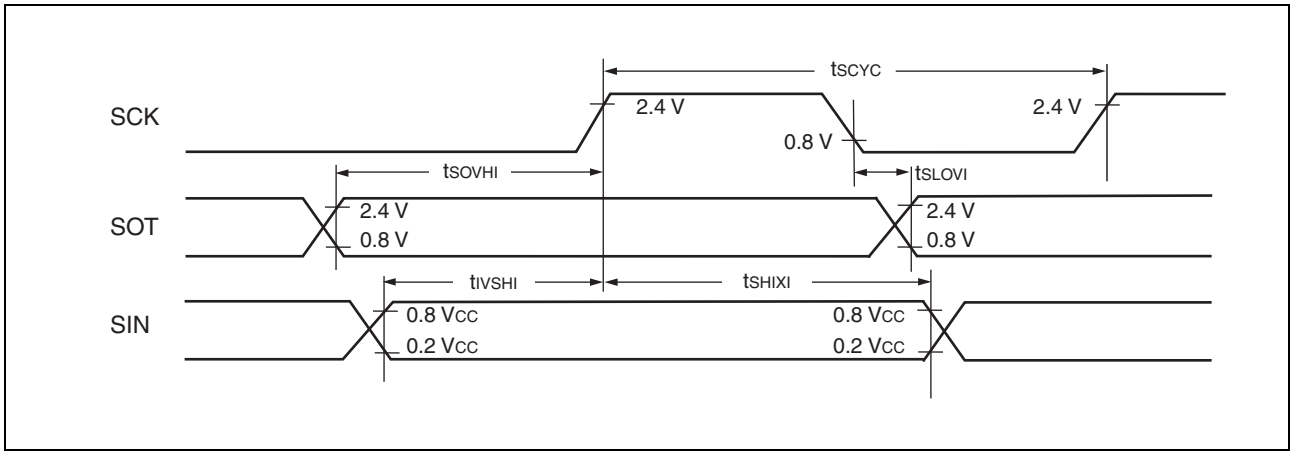
($V_{CC}$ = 5.0 V ± 10%, $V_{SS}$ = 0.0 V, $T_A$ = –40 °C to + 85 °C)

| Parameter | Sym-bol | Pin name | Conditions | Value | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| Serial clock cycle time | $t_{SCYC}$ | SCK | Internal clock operation output pin : $C_L$ = 80 pF + 1 TTL. | 5 $t_{MCLK}$*3 | — | ns |
| SCK↓→SOT delay time | $t_{SLOVI}$ | SCK, SOT | | –95 | + 95 | ns |
| Valid SIN→SCK↑ | $t_{IVSHI}$ | SCK, SIN | | $t_{MCLK}$*3 + 190 | — | ns |
| SCK↑ → valid SIN hold time | $t_{SHIXI}$ | SCK, SIN | | 0 | — | ns |
| SOT→SCK↑ delay time | $t_{SOVHI}$ | SCK, SOT | | — | 4 $t_{MCLK}$*3 | ns |

*1 : Provide switch function whether sampling of reception data is performed at rising edge or falling edge of the serial clock.

*2 : Serial clock delay function is used to delay half clock for the output signal of serial clock.

*3 : Refer to " (2) Source Clock/Machine Clock" for $t_{MCLK}$.



### (8) I²C Timing

($V_{CC}$ = 5.0 V ± 10%, $AV_{SS}$ = $V_{SS}$ = 0.0 V, $T_A$ = − 40 °C to + 85 °C)

| Parameter | Symbol | Pin name | Conditions | Value | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Standard-mode | | Fast-mode | | |
| | | | | Min | Max | Min | Max | |
| SCL clock frequency | $f_{SCL}$ | SCL0 | R = 1.7 kΩ, C = 50 pF*1 | 0 | 100 | 0 | 400 | kHz |
| (Repeat) Start condition hold time SDA ↓ → SCL ↓ | $t_{HD;STA}$ | SCL0 SDA0 | | 4.0 | — | 0.6 | — | µs |
| SCL clock “L” width | $t_{LOW}$ | SCL0 | | 4.7 | — | 1.3 | — | µs |
| SCL clock “H” width | $t_{HIGH}$ | SCL0 | | 4.0 | — | 0.6 | — | µs |
| (Repeat) Start condition setup time SCL ↑ → SDA ↓ | $t_{SU;STA}$ | SCL0 SDA0 | | 4.7 | — | 0.6 | — | µs |
| Data hold time SCL ↓ → SDA ↓ ↑ | $t_{HD;DAT}$ | SCL0 SDA0 | | 0 | 3.45*2 | 0 | 0.9*3 | µs |
| Data setup time SDA ↓ ↑ → SCL ↑ | $t_{SU;DAT}$ | SCL0 SDA0 | | 0.25*4 | — | 0.1*4 | — | µs |
| Stop condition setup time SCL ↑ → SDA ↑ | $t_{SU;STO}$ | SCL0 SDA0 | | 4.0 | — | 0.6 | — | µs |
| Bus free time between stop condition and start condition | $t_{BUF}$ | SCL0 SDA0 | | 4.7 | — | 1.3 | — | µs |

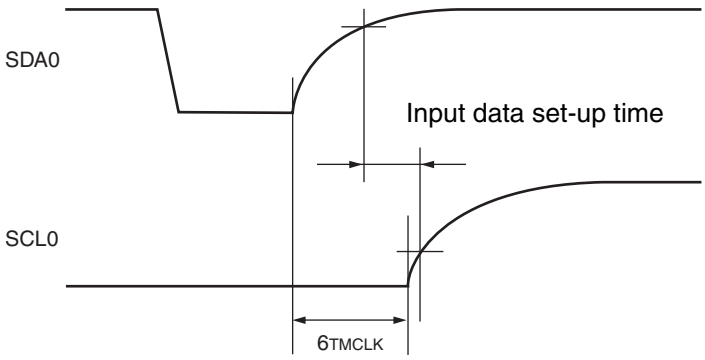
*1 : R, C : Pull-up resistor and load capacitor of the SCL and SDA lines.

*2 : The maximum $t_{HD;DAT}$ have only to be met if the device dose not stretch the “L” width ($t_{LOW}$) of the SCL signal.

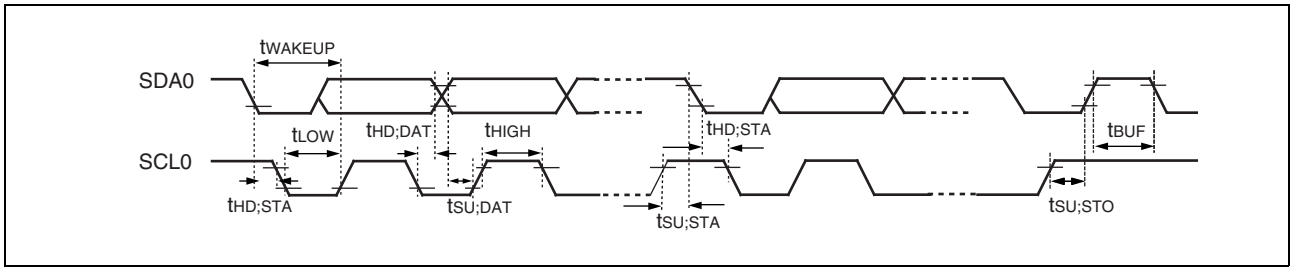
*3 : A fast-mode I²C-bus device can be used in a standard-mode I²C-bus system, but the requirement $t_{SU;DAT} \geq$ 250 ns must then be met.

*4 : Refer to “ • Note of SDA and SCL set-up time”.

• Note of SDA and SCL set-up time




The rating of the input data set-up time in the device connected to the bus cannot be satisfied depending on the load capacitance or pull-up resistor.
Be sure to adjust the pull-up resistor of SDA and SCL if the rating of the input data set-up time cannot be satisfied.


SDA0
SCL0
tWAKEUP
tLOW
tHD;DAT
tHIGH
tHD;STA
tBUF
tHD;STA
tSU;DAT
tSU;STA
tSU;STO

($V_{CC}$ = 5.0 V ± 10%, $AV_{SS}$ = $V_{SS}$ = 0.0 V, $T_A$ = –40 °C to + 85 °C)

| Parameter | Symbol | Pin name | Conditions | Value*2 | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| SCL clock “L” width | $t_{LOW}$ | SCL0 | R = 1.7 kΩ, C = 50 pF*1 | (2 + nm / 2) $t_{MCLK}$ – 20 | — | ns | Master mode |
| SCL clock “H” width | $t_{HIGH}$ | SCL0 | | (nm / 2) $t_{MCLK}$ – 20 | (nm / 2 ) $t_{MCLK}$ + 20 | ns | Master mode |
| Start condition hold time | $t_{HD;STA}$ | SCL0 SDA0 | | (–1 + nm / 2) $t_{MCLK}$ – 20 | (–1 + nm) $t_{MCLK}$ + 20 | ns | Master mode Maximum value is applied when m, n = 1, 8. Otherwise, the minimum value is applied. |
| Stop condition setup time | $t_{SU;STO}$ | SCL0 SDA0 | | (1 + nm / 2) $t_{MCLK}$ – 20 | (1 + nm / 2) $t_{MCLK}$ + 20 | ns | Master mode |
| Start condition setup time | $t_{SU;STA}$ | SCL0 SDA0 | | (1 + nm / 2) $t_{MCLK}$ – 20 | (1 + nm / 2) $t_{MCLK}$ + 20 | ns | Master mode |
| Bus free time between stop condition and start condition | $t_{BUF}$ | SCL0 SDA0 | | (2 nm + 4) $t_{MCLK}$ – 20 | — | ns | |
| Data hold time | $t_{HD;DAT}$ | SCL0 SDA0 | | 3 $t_{MCLK}$ – 20 | — | ns | Master mode |
| Data setup time | $t_{SU;DAT}$ | SCL0 SDA0 | | (–2 + nm / 2) $t_{MCLK}$ – 20 | (–1 + nm / 2) $t_{MCLK}$ + 20 | ns | Master mode When assuming that “L” of SCL is not extended, the minimum value is applied to first bit of continuous data. Otherwise, the maximum value is applied. |
| Setup time between clearing interrupt and SCL rising | $t_{SU;INT}$ | SCL0 | | (nm / 2) $t_{MCLK}$ – 20 | (1 + nm / 2) $t_{MCLK}$ + 20 | ns | Minimum value is applied to interrupt at 9th SCL↓. Maximum value is applied to interrupt at 8th SCL↓. |
| SCL clock “L” width | $t_{LOW}$ | SCL0 | | 4 $t_{MCLK}$ – 20 | — | ns | At reception |
| SCL clock “H” width | $t_{HIGH}$ | SCL0 | | 4 $t_{MCLK}$ – 20 | — | ns | At reception |
| Start condition detection | $t_{HD;STA}$ | SCL0 SDA0 | | 2 $t_{MCLK}$ – 20 | — | ns | Undetected when 1 $t_{MCLK}$ is used at reception |

*(Continued)*

*(Continued)*

($V_{CC}$ = 5.0 V ± 10%, $AV_{SS}$ = $V_{SS}$ = 0.0 V, $T_A$ = –40 °C to + 85 °C)

| Parameter | Symbol | Pin name | Conditions | Value*2 | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Stop condition detection | $t_{SU;STO}$ | SCL0 SDA0 | R = 1.7 kΩ, C = 50 pF*1 | 2 $t_{MCLK}$ – 20 | — | ns | Undetected when 1 $t_{MCLK}$ is used at reception |
| Restart condition detection condition | $t_{SU;STA}$ | SCL0 SDA0 | | 2 $t_{MCLK}$ – 20 | — | ns | Undetected when 1 $t_{MCLK}$ is used at reception |
| Bus free time | $t_{BUF}$ | SCL0 SDA0 | | 2 $t_{MCLK}$ – 20 | — | ns | At reception |
| Data hold time | $t_{HD;DAT}$ | SCL0 SDA0 | | 2 $t_{MCLK}$ – 20 | — | ns | At slave transmission mode |
| Data setup time | $t_{SU;DAT}$ | SCL0 SDA0 | | $t_{LOW}$ – 3 $t_{MCLK}$ – 20 | — | ns | At slave transmission mode |
| Data hold time | $t_{HD;DAT}$ | SCL0 SDA0 | | 0 | — | ns | At reception |
| Data setup time | $t_{SU;DAT}$ | SCL0 SDA0 | | $t_{MCLK}$ – 20 | — | ns | At reception |
| SDA↓→SCL↑ (at wakeup function) | $t_{WAKE-UP}$ | SCL0 SDA0 | | Oscillation stabilization wait time + 2 $t_{MCLK}$ – 20 | — | ns | |

*1 : R, C : Pull-up resistor and load capacitor of the SCL and SDA lines.

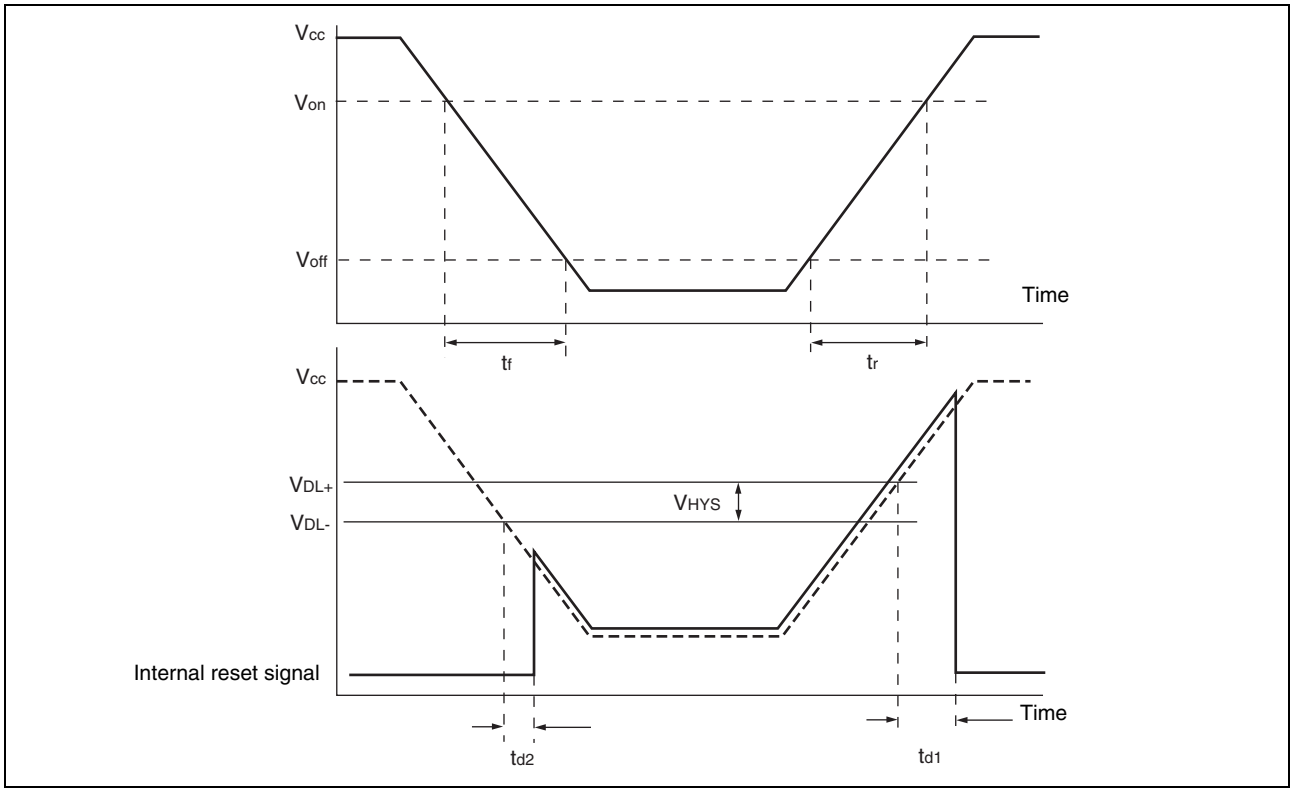
*2 : •Refer to " (2) Source Clock/Machine Clock" for $t_{MCLK}$.

- m is CS4 bit and CS3 bit (bit 4 and bit 3) of I²C clock control register (ICCR) .
- n is CS2 bit to CS0 bit (bit 2 to bit 0) of I²C clock control register (ICCR) .
- Actual timing of I²C is determined by m and n values set by the machine clock ($t_{MCLK}$) and CS4 to CS0 of ICCR0 register.
- Standard-mode :
  m and n can be set at the range : 0.9 MHz < $t_{MCLK}$ (machine clock) < 10 MHz.
  Setting of m and n determines the machine clock that can be used below.
  (m, n) = (1, 8) : 0.9 MHz < $t_{MCLK}$ ≤ 1 MHz
  (m, n) = (1, 22) , (5, 4) , (6, 4) , (7, 4) , (8, 4) : 0.9 MHz < $t_{MCLK}$ ≤ 2 MHz
  (m, n) = (1, 38) , (5, 8) , (6, 8) , (7, 8) , (8, 8) : 0.9 MHz < $t_{MCLK}$ ≤ 4 MHz
  (m, n) = (1, 98) : 0.9 MHz < $t_{MCLK}$ ≤ 10 MHz
- Fast-mode :
  m and n can be set at the range : 3.3 MHz < $t_{MCLK}$ (machine clock) < 10 MHz.
  Setting of m and n determines the machine clock that can be used below.
  (m, n) = (1, 8) : 3.3 MHz < $t_{MCLK}$ ≤ 4 MHz
  (m, n) = (1, 22) , (5, 4) : 3.3 MHz < $t_{MCLK}$ ≤ 8 MHz
  (m, n) = (6, 4) : 3.3 MHz < $t_{MCLK}$ ≤ 10 MHz

### (9) Low Voltage Detection

(Vss = 0.0 V, $T_A$ = –40 °C to + 85 °C)

| Parameter | Symbol | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Release voltage | $V_{DL+}$ | — | 2.52 | 2.70 | 2.88 | V | At power-supply rise |
| Detection voltage | $V_{DL-}$ | | 2.42 | 2.60 | 2.78 | V | At power-supply fall |
| Hysteresis width | $V_{HYS}$ | | 70 | 100 | — | mV | |
| Power-supply start voltage | $V_{off}$ | | — | — | 2.3 | V | |
| Power-supply end voltage | $V_{on}$ | | 4.9 | — | — | V | |
| Power-supply voltage change time (at power supply rise) | $t_r$ | | 0.3 | — | — | µs | Slope of power supply that reset release signal generates |
| | | | — | 3000 | — | µs | Slope of power supply that reset release signal generates within rating ($V_{DL+}$) |
| Power-supply voltage change time (at power supply fall) | $t_f$ | | 300 | — | — | µs | Slope of power supply that reset detection signal generates |
| | | | — | 300 | — | µs | Slope of power supply that reset detection signal generates within rating ($V_{DL-}$) |
| Reset release delay time | $t_{d1}$ | | — | — | 400 | µs | |
| Reset detection delay time | $t_{d2}$ | | — | — | 30 | µs | |
| Current consumption | $I_{LVD}$ | | — | 38 | 50 | µA | Current consumption of low voltage detection circuit only |



### (10) Clock Supervisor Clock

(Vcc = 5.0 V ± 10%, Vss = 0.0 V, $T_A$ = –40 °C to + 85 °C)

| Parameter | Symbol | Condi-tions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Oscillation frequency | $f_{OUT}$ | — | 50 | 100 | 200 | kHz | |
| Oscillation start time | $t_{wk}$ | | — | — | 10 | µs | |
| Current consumption | $I_{CSV}$ | | — | 20 | 36 | µA | Current consumption of built-in CR oscillator, at 100 kHz oscillation |

## 5. A/D Converter

### (1) A/D Converter Electrical Characteristics

($AV_{CC} = V_{CC}$ = 4.0 V to 5.5 V, $AV_{SS} = V_{SS}$ = 0.0 V, $T_A$ = − 40 °C to + 85 °C)

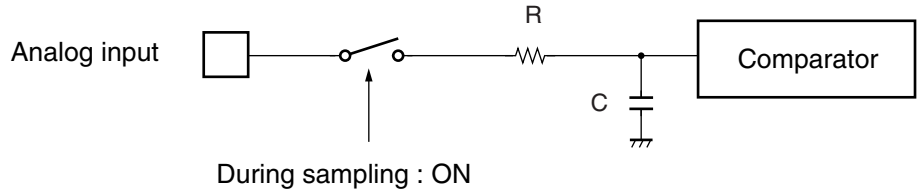
| Parameter | Symbol | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Resolution | — | — | — | — | 10 | bit | |
| Total error | | | − 3.0 | — | + 3.0 | LSB | |
| Linearity error | | | − 2.5 | — | + 2.5 | LSB | |
| Differential linear error | | | − 1.9 | — | + 1.9 | LSB | |
| Zero transition voltage | $V_{OT}$ | — | $AV_{SS}$ − 1.5 LSB | $AV_{SS}$ + 0.5 LSB | $AV_{SS}$ + 2.5 LSB | V | |
| Full-scale transition voltage | $V_{FST}$ | | AVR − 3.5 LSB | AVR − 1.5 LSB | AVR + 0.5 LSB | V | |
| Compare time | — | | 0.9 | — | 16500 | µs | 4.5 V ≤ AVcc ≤ 5.5 V |
| | | | 1.8 | — | 16500 | µs | 4.0 V ≤ AVcc < 4.5 V |
| Sampling time | — | | 0.6 | — | ∞ | µs | 4.5 V ≤ AVcc ≤ 5.5 V, At external impedance < 5.4 kΩ |
| | | | 1.2 | — | ∞ | µs | 4.0 V ≤ AVcc < 4.5 V, At external impedance < 2.4 kΩ |
| Analog input current | $I_{AIN}$ | | − 0.3 | — | + 0.3 | µA | |
| Analog input voltage | $V_{AIN}$ | | $AV_{SS}$ | — | AVR | V | |
| Reference voltage | — | | $AV_{SS}$ + 4.0 | — | $AV_{CC}$ | V | AVR pin |
| Reference voltage supply current | $I_R$ | | — | 600 | 900 | µA | AVR pin, during A/D operation |
| | $I_{RH}$ | | — | — | 5 | µA | AVR pin, at stop mode |

### (2) Notes on Using A/D Converter

- **About the external impedance of analog input and its sampling time**

A/D converter with sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting A/D conversion precision. Therefore, to satisfy the A/D conversion precision standard, consider the relationship between the external impedance and minimum sampling time and either adjust the register value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value. Also, if the sampling time cannot be sufficient, connect a capacitor of about 0.1 µF to the analog input pin.

- Analog input equivalent circuit

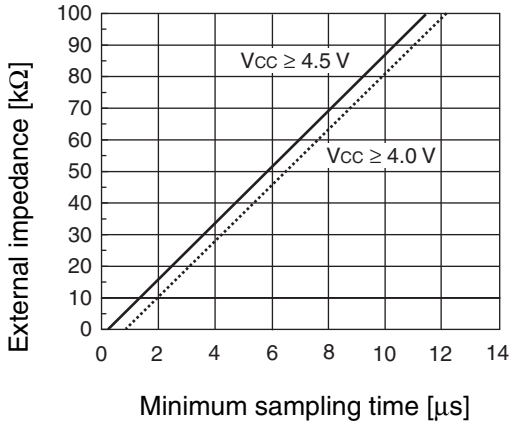



| | R | C |
|---|---|---|
| 4.5 V ≤ $V_{CC}$ ≤ 5.5 V | 2.0 kΩ (Max) | 16 pF (Max) |
| 4.0 V ≤ $V_{CC}$ < 4.5 V | 8.2 kΩ (Max) | 16 pF (Max) |

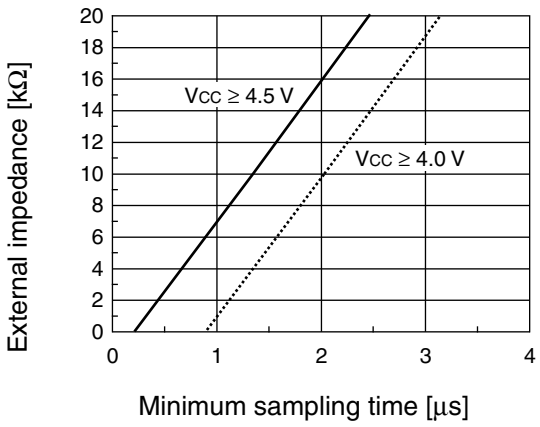
Note : The values are reference values.

- The relationship between external impedance and minimum sampling time

(External impedance = 0 kΩ to 100 kΩ)




(External impedance = 0 kΩ to 20 kΩ)



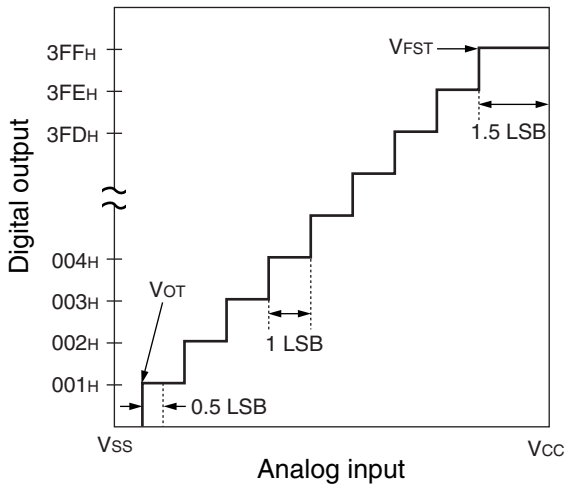

- **About errors**

As |$V_{CC}$ – $V_{SS}$| becomes smaller, values of relative errors grow larger.

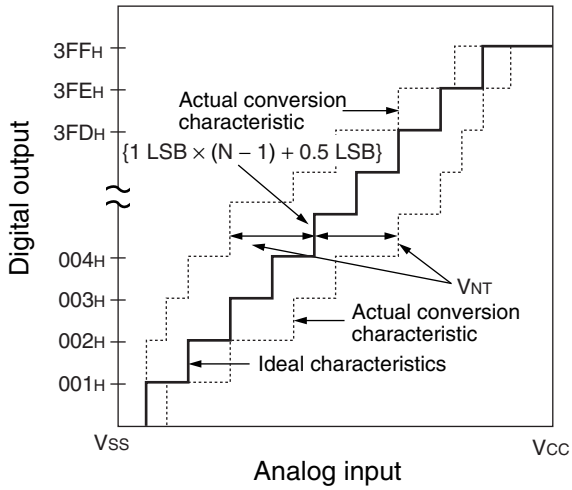
**(3) Definition of A/D Converter Terms**

- Resolution
  The level of analog variation that can be distinguished by the A/D converter.
  When the number of bits is 10, analog voltage can be divided into $2^{10} = 1024$.
- Linearity error (unit : LSB)
  The deviation between the value along a straight line connecting the zero transition point (“00 0000 0000” ← → “00 0000 0001”) of a device and the full-scale transition point (“11 1111 1111” ← → “11 1111 1110”) compared with the actual conversion values obtained.
- Differential linear error (Unit : LSB)
  Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value.
- Total error (unit: LSB)
  Difference between actual and theoretical values, caused by a zero transition error, full-scale transition error, linearity error, quantum error, and noise.

Ideal I/O characteristics




Total error




$$1\ \text{LSB} = \frac{V_{CC} - V_{SS}}{1024}\ \text{(V)}$$

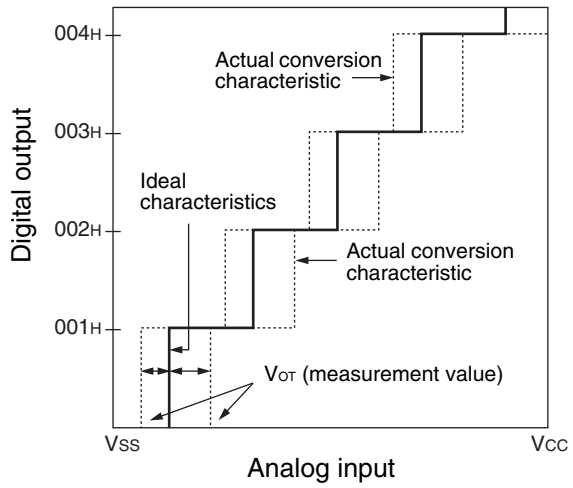
$$\text{Total error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ \text{[LSB]}$$

N : A/D converter digital output value
$V_{NT}$ : A voltage at which digital output transits from $(N - 1)_H$ to $N_H$

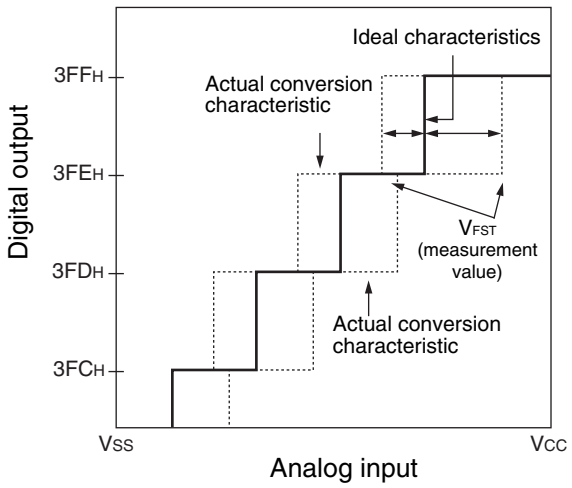
*(Continued)*

*(Continued)*

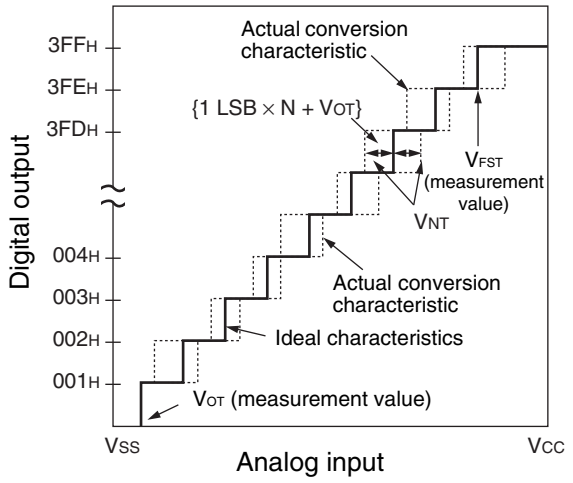
Zero transition error



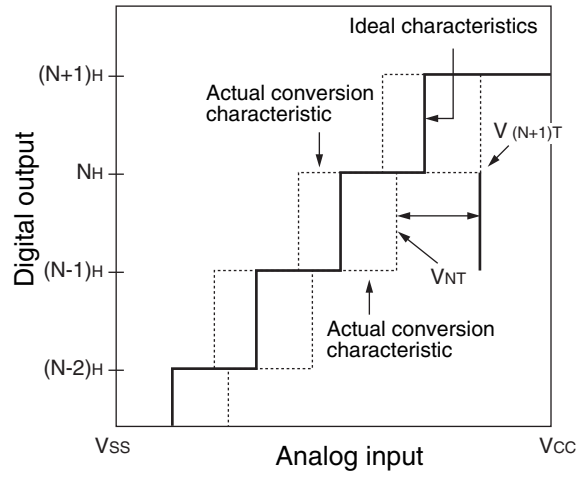

Full-scale transition error




Linearity error




Differential linear error




$$\text{Linearity error in digital output N} = \frac{V_{NT} - \{1\ LSB \times N + V_{OT}\}}{1\ LSB}$$

$$\text{Differential linear error in digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ LSB} - 1$$

N : A/D converter digital output value
$V_{NT}$ : A voltage at which digital output transits from (N – 1) H to $N_H$
$V_{OT}$ (Ideal value) = $V_{SS}$ + 0.5 LSB [V]
$V_{FST}$ (Ideal value) = $V_{CC}$ – 1.5 LSB [V]

## 6. Flash Memory Program/Erase Characteristics

| Parameter | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| Chip erase time | — | — | 1*1 | 15*2 | s | Excludes $00_H$ programming prior erasure. |
| Byte programming time | | — | 32 | 3600 | µs | Excludes system-level overhead. |
| Erase/program cycle | | 10000 | — | — | cycle | |
| Power supply voltage at erase/program | | 4.5 | — | 5.5 | V | |
| Flash memory data retention time | | 20*3 | — | — | year | Average $T_A$ = + 85 °C |

*1 : $T_A$ = + 25 °C, $V_{CC}$ = 5.0 V, 10000 cycles

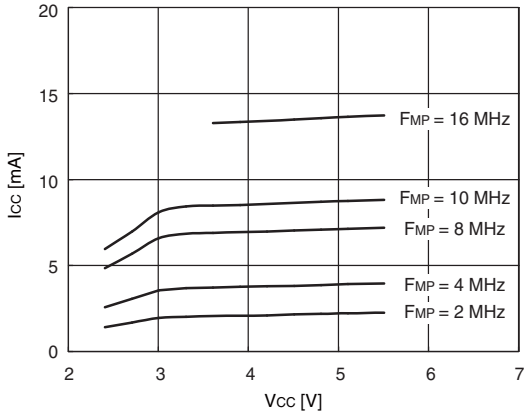
*2 : $T_A$ = + 85 °C, $V_{CC}$ = 4.5 V, 10000 cycles

*3 : This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at +85 °C) .

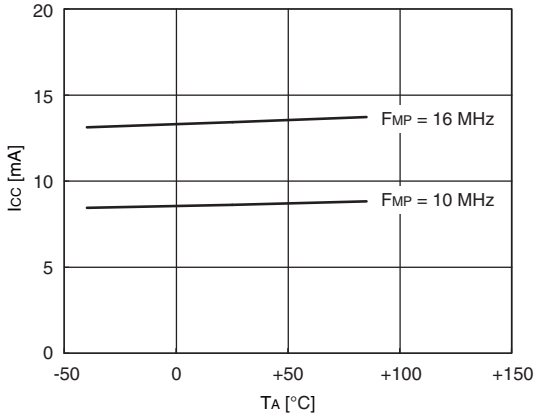
## ■ EXAMPLE CHARACTERISTICS

**• Power supply current temperature (MB95F168MA/F168NA/F168JA)**

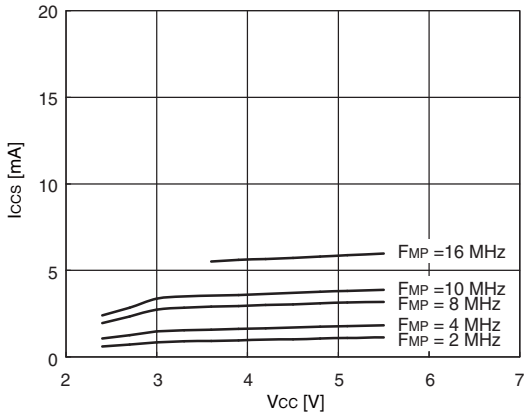
$I_{CC}$ – $V_{CC}$
$T_A$ = + 25 °C, $F_{MP}$ = 2, 4, 8, 10, 16 MHz (divided by 2)
Main clock mode, at external clock operating



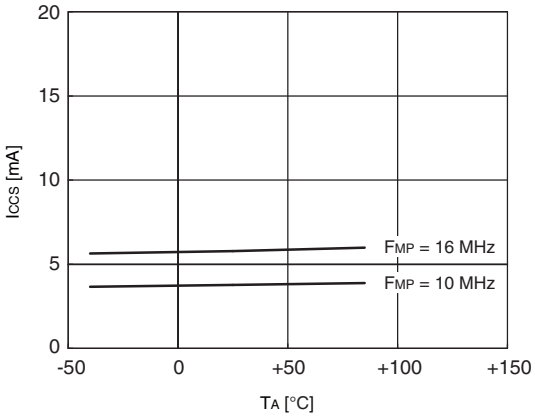

$I_{CC}$ – $T_A$
$V_{CC}$ = 5.5 V, $F_{MP}$ = 10, 16 MHz (divided by 2)
Main clock mode, at external clock operating



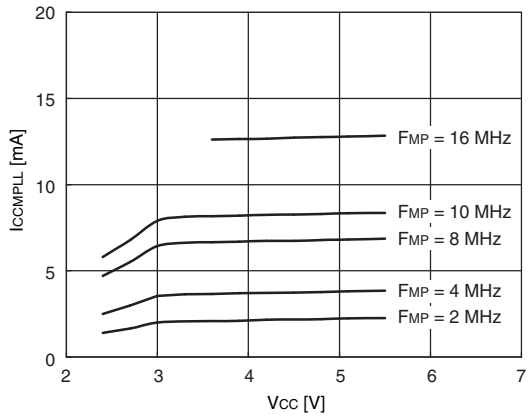

$I_{CCS}$ – $V_{CC}$
$T_A$ = + 25 °C, $F_{MP}$ = 2, 4, 8, 10, 16 MHz (divided by 2)
Main sleep mode, at external clock operating



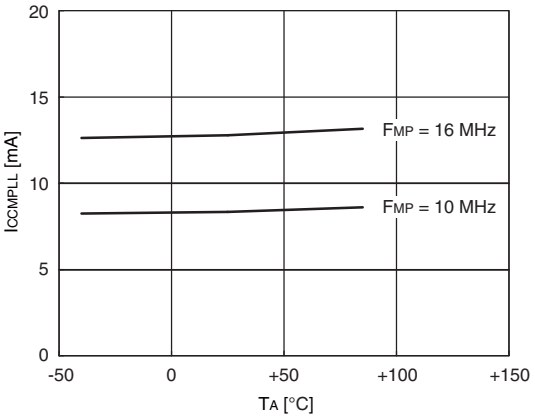

$I_{CCS}$ – $T_A$
$V_{CC}$ = 5.5 V, $F_{MP}$ = 10, 16 MHz (divided by 2)
Main sleep mode, at external clock operating




$I_{CCMPLL}$ – $V_{CC}$
$T_A$ = + 25 °C, $F_{MP}$ = 2, 4, 8, 10, 16 MHz
(Main PLL multiplied by 2.5)
Main PLL mode, at external clock operating




$I_{CCMPLL}$ – $T_A$
$V_{CC}$ = 5.5 V, $F_{MP}$ = 10, 16 MHz (Main PLL multiplied by 2.5)
Main PLL mode, at external clock operating

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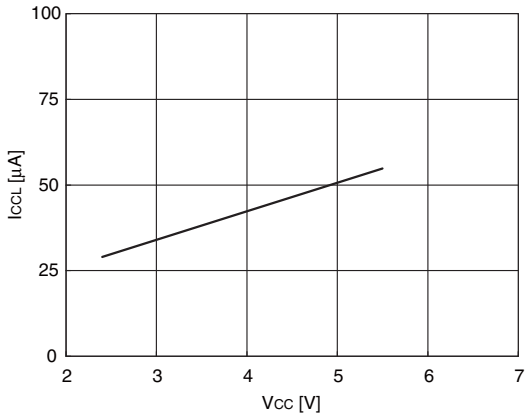
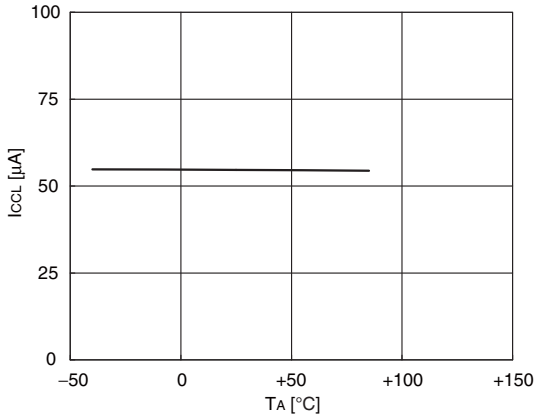
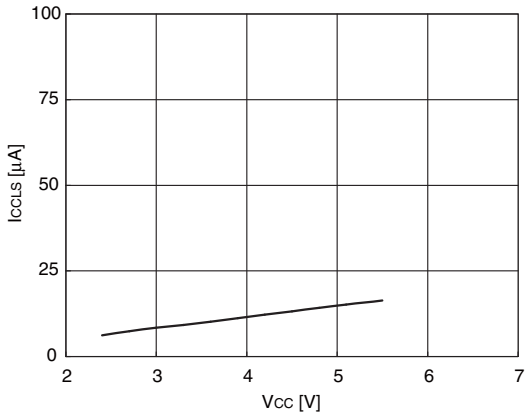
$I_{CCL}$ – $V_{CC}$
$T_A$ = + 25 °C, $F_{MPL}$ = 16 kHz (divided by 2)
Sub clock mode, at external clock operating



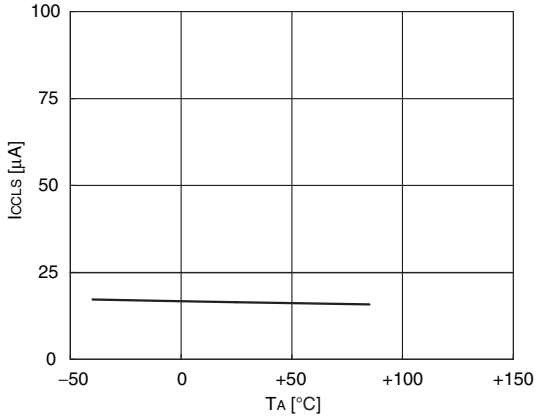

$I_{CCL}$ – $T_A$
$V_{CC}$ = 5.5 V, $F_{MPL}$ = 16 kHz (divided by 2)
Sub clock mode, at external clock operating



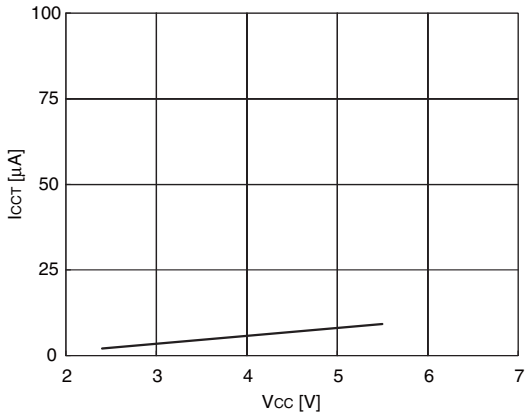

$I_{CCLS}$ – $V_{CC}$
$T_A$ = + 25 °C, $F_{MPL}$ = 16 kHz (divided by 2)
Sub sleep mode, at external clock operating



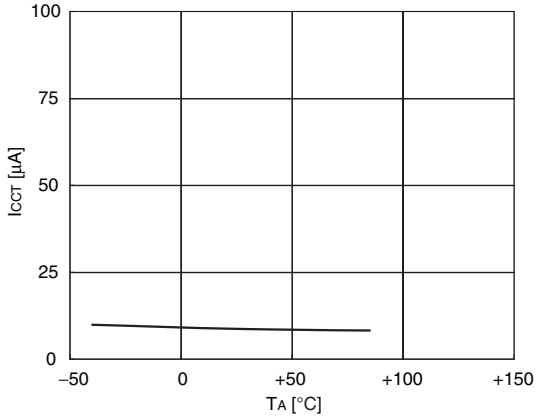

$I_{CCLS}$ – $T_A$
$V_{CC}$ = 5.5 V, $F_{MPL}$ = 16 kHz (divided by 2)
Sub sleep mode, at external clock operating




$I_{CCT}$ – $V_{CC}$
$T_A$ = + 25 °C, $F_{MPL}$ = 16 kHz (divided by 2)
Clock mode, at external clock operating




$I_{CCT}$ – $T_A$
$V_{CC}$ = 5.5 V, $F_{MPL}$ = 16 kHz (divided by 2)
Clock mode, at external clock operating

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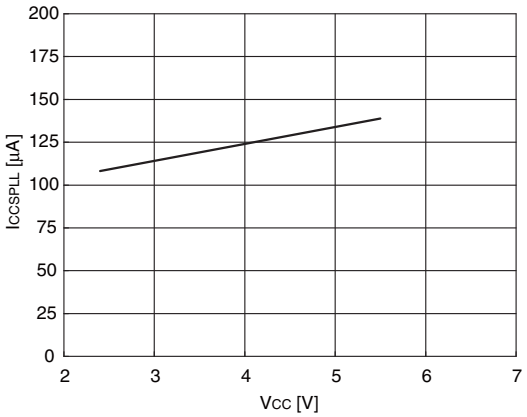
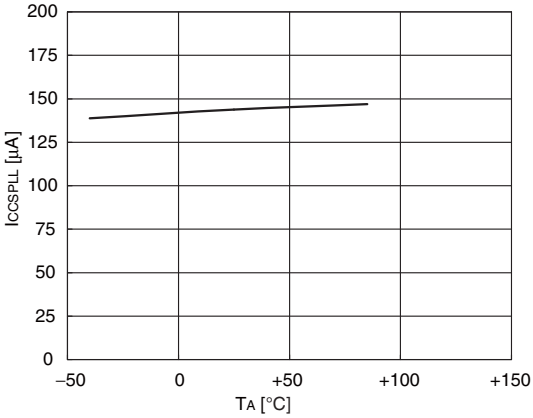
$I_{CCSPLL}$ – $V_{CC}$

$T_A$ = + 25 °C, $F_{MPL}$ = 128 kHz (Main PLL multiplied by 4)
Sub PLL mode, at external clock operating



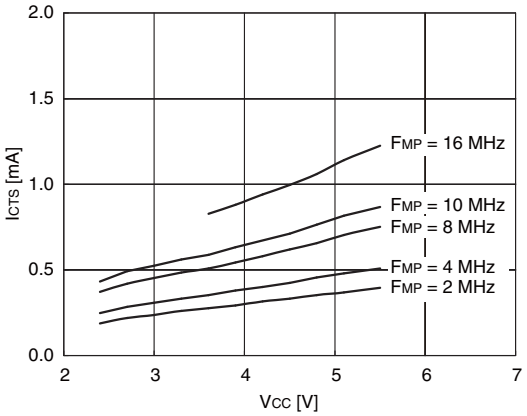

$I_{CCSPLL}$ – $T_A$

$V_{CC}$ = 5.5 V, $F_{MPL}$ = 128 kHz (Main PLL multiplied by 4)
Sub PLL mode, at external clock operating



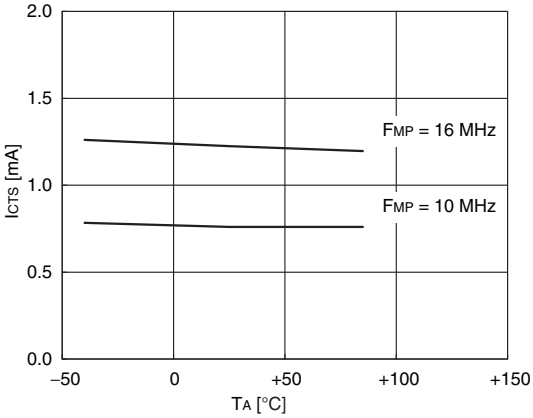

$I_{CTS}$ – $V_{CC}$

$T_A$ = + 25 °C, $F_{MP}$ = 2, 4, 8, 10, 16 MHz (divided by 2)
Time-base timer mode, at external clock operating



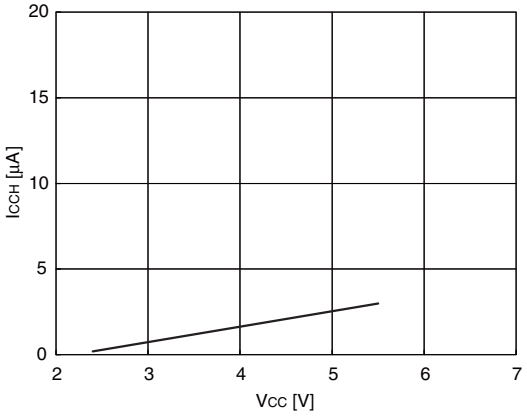

$I_{CTS}$ – $T_A$

$V_{CC}$ = 5.5 V, $F_{MP}$ = 10, 16 MHz (divided by 2)
Time-base timer mode, at external clock operating



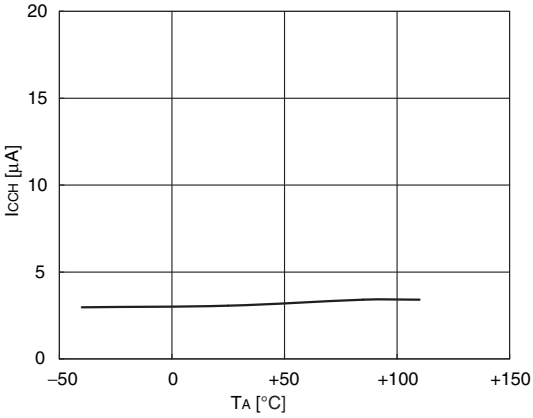

$I_{CCH}$ – $V_{CC}$

$T_A$ = + 25 °C, $F_{MPL}$ = (stop)
Sub stop mode, at external clock stopping




$I_{CCH}$ – $T_A$

$V_{CC}$ = 5.5 V, $F_{MPL}$ = (stop)
Sub stop mode, at external clock stopping

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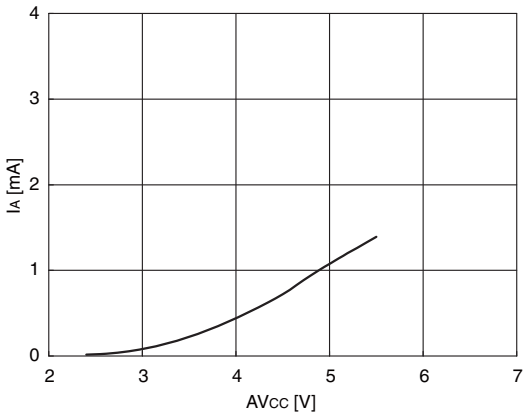
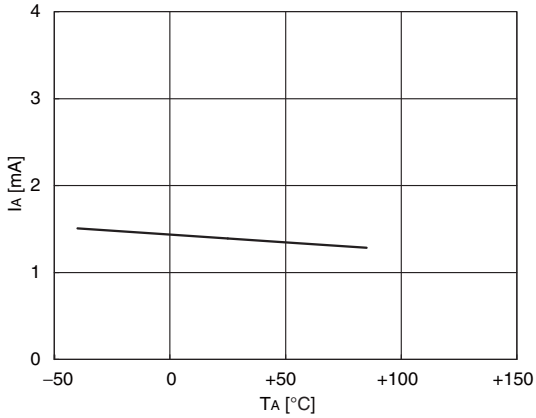
$I_A$ – $AV_{CC}$

$T_A$ = + 25 °C, $F_{MP}$ = 16 MHz (divided by 2)
Main clock mode, at external clock operating



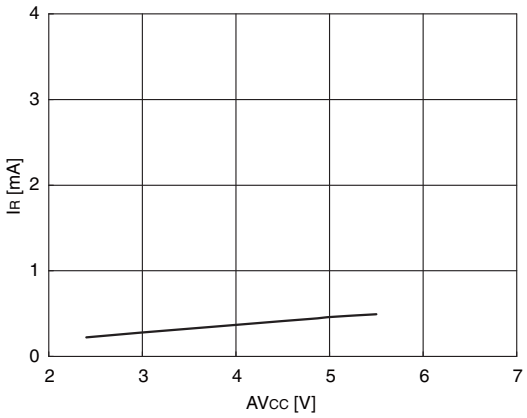

$I_A$ – $T_A$

$V_{CC}$ = 5.5 V, $F_{MP}$ = 16 MHz (divided by 2)
Main clock mode, at external clock operating



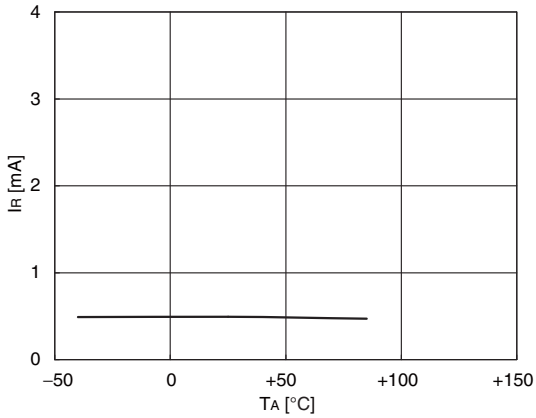

$I_R$ – $AV_{CC}$

$T_A$ = + 25 °C, $F_{MP}$ = 16 MHz (divided by 2)
Main clock mode, at external clock operating



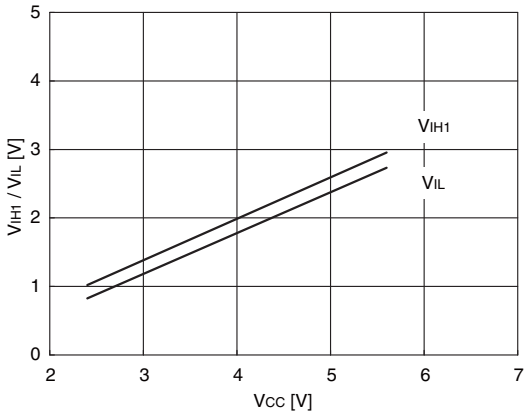

$I_R$ – $T_A$

$V_{CC}$ = 5.5 V, $F_{MP}$ = 16 MHz (divided by 2)
Main clock mode, at external clock operating

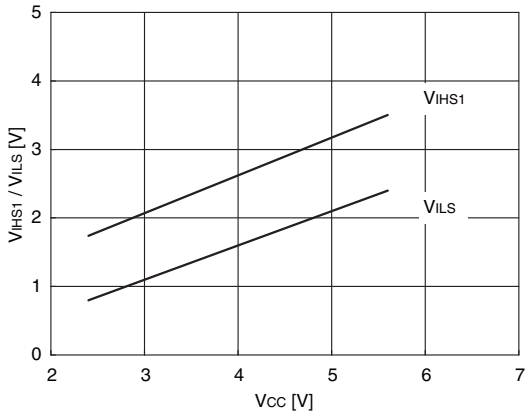


• **Input voltage (MB95F168MA/F168NA/F168JA)**

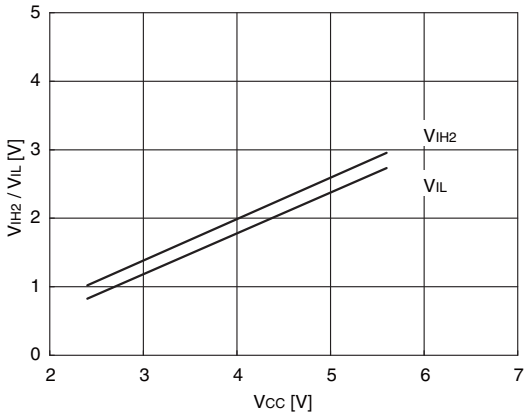
$V_{IH1}$ – $V_{CC}$ and $V_{IL}$ – $V_{CC}$
$T_A$ = + 25 °C



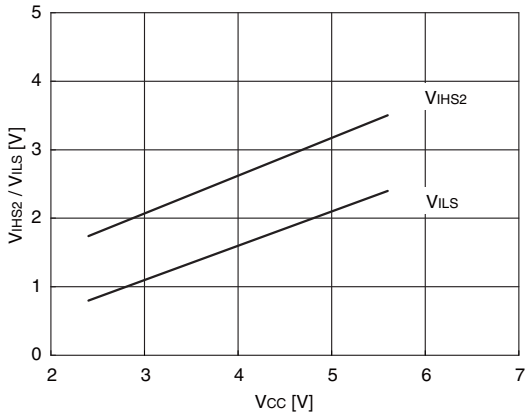

$V_{IHS1}$ – $V_{CC}$ and $V_{ILS}$ – $V_{CC}$
$T_A$ = + 25 °C



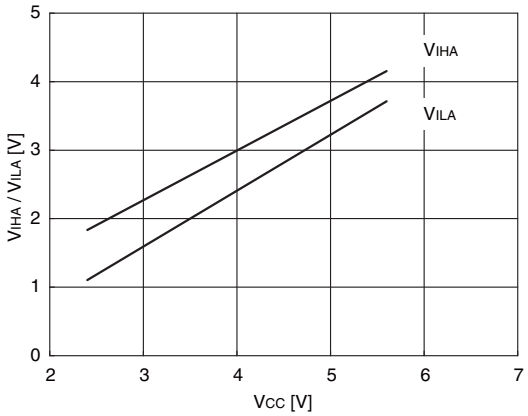

$V_{IH2}$ – $V_{CC}$ and $V_{IL}$ – $V_{CC}$
$T_A$ = + 25 °C



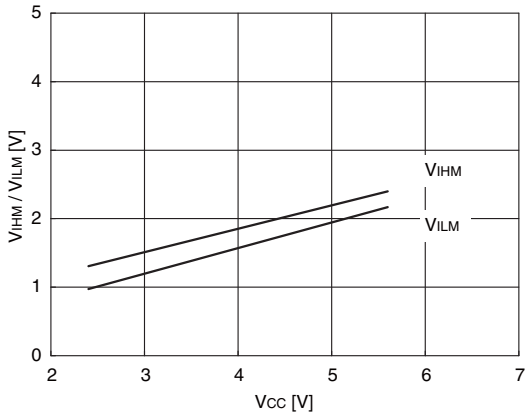

$V_{IHS2}$ – $V_{CC}$ and $V_{ILS}$ – $V_{CC}$
$T_A$ = + 25 °C




$V_{IHA}$ – $V_{CC}$ and $V_{ILA}$ – $V_{CC}$
$T_A$ = + 25 °C

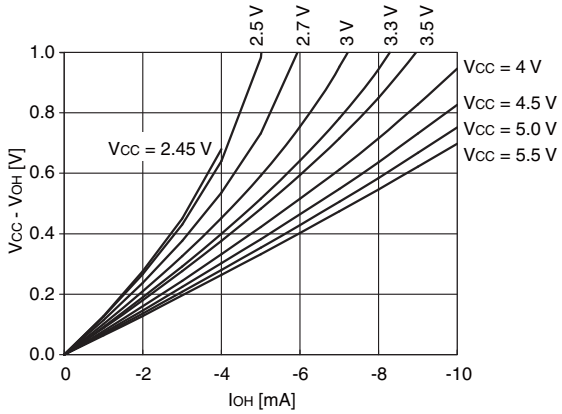



$V_{IHM}$ – $V_{CC}$ and $V_{ILM}$ – $V_{CC}$
$T_A$ = + 25 °C

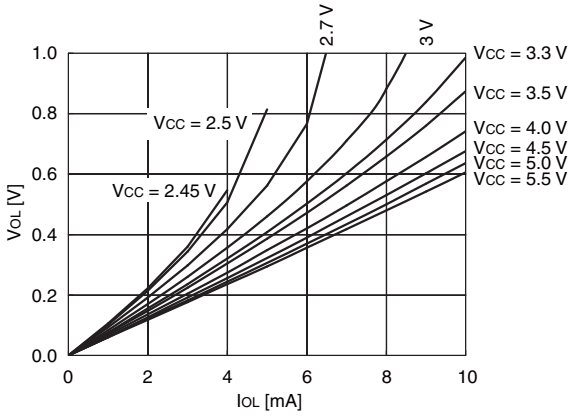


• **Output voltage (MB95F168MA/F168NA/F168JA)**

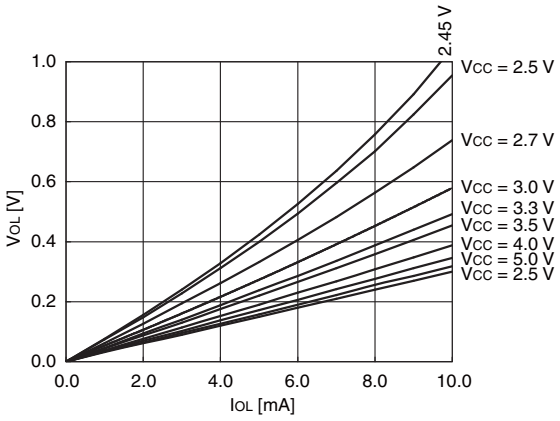
$(V_{CC} - V_{OH}) - I_{OH}$
$T_A = +25\ °C$




$V_{OL} - I_{OL}$
$T_A = +25\ °C$

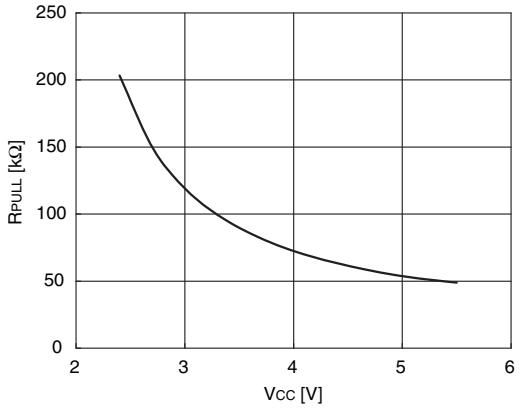



$V_{OL} - I_{OL}$
$T_A = +25\ °C$




• **Pull-up (MB95F168MA/F168NA/F168JA)**

$R_{PULL} - V_{CC}$
$T_A = +25\ °C$



## ■ MASK OPTION

| No. | Part number | MB95168MA | MB95F168MA/ MB95F168NA/ MB95F168JA | MB95FV100D-103 |
|---|---|---|---|---|
| | Specifying procedure | Specified when ordering ROM | Setting disabled | Setting disabled |
| 1 | Clock mode select*<br>• Single-system clock mode<br>• Dual-system clock mode | Dual-system clock mode | Dual-system clock mode | Changing by the switch on MCU board |
| 2 | Low voltage detection reset*<br>• With low voltage detection reset<br>• Without low voltage detection reset | Specified when ordering ROM | Specified by part number | Changing by the switch on MCU board |
| 3 | Clock supervisor*<br>• With clock supervisor<br>• Without clock supervisor | Specified when ordering ROM | Specified by part number | Changing by the switch on MCU board |
| 4 | Reset output*<br>• With reset output<br>• Without reset output | Specified when ordering ROM | Specified by part number | MCU board switch sets as follows;<br>• With clock supervisor:<br>Without reset output<br>• Without clock supervisor:<br>With reset output |
| 5 | Oscillation stabilization wait time | Fixed to oscillation stabilization wait time of $(2^{14} - 2) / F_{CH}$ | Fixed to oscillation stabilization wait time of $(2^{14} - 2) / F_{CH}$ | Fixed to oscillation stabilization wait time of $(2^{14} - 2) / F_{CH}$ |

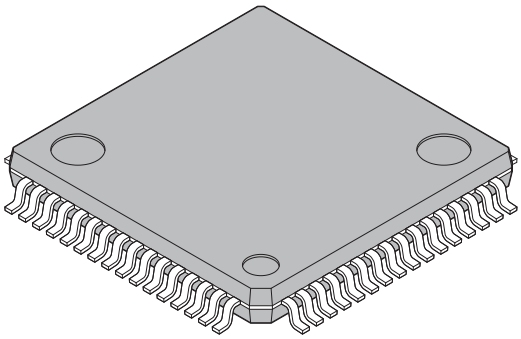
* : Refer to table below about clock mode select, low voltage detection reset, clock supervisor select and reset output.

| Part number | Clock mode select | Low voltage detection reset | Clock supervisor | Reset output |
|---|---|---|---|---|
| MB95168MA | Dual-system | No | No | Yes |
| | | Yes | No | Yes |
| | | Yes | Yes | No |
| MB95F168MA | Dual-system | No | No | Yes |
| MB95F168NA | | Yes | No | Yes |
| MB95F168JA | | Yes | Yes | No |
| MB95FV100D-103 | Single-system | No | No | Yes |
| | | Yes | No | Yes |
| | | Yes | Yes | No |
| | Dual-system | No | No | Yes |
| | | Yes | No | Yes |
| | | Yes | Yes | No |

## ■ ORDERING INFORMATION

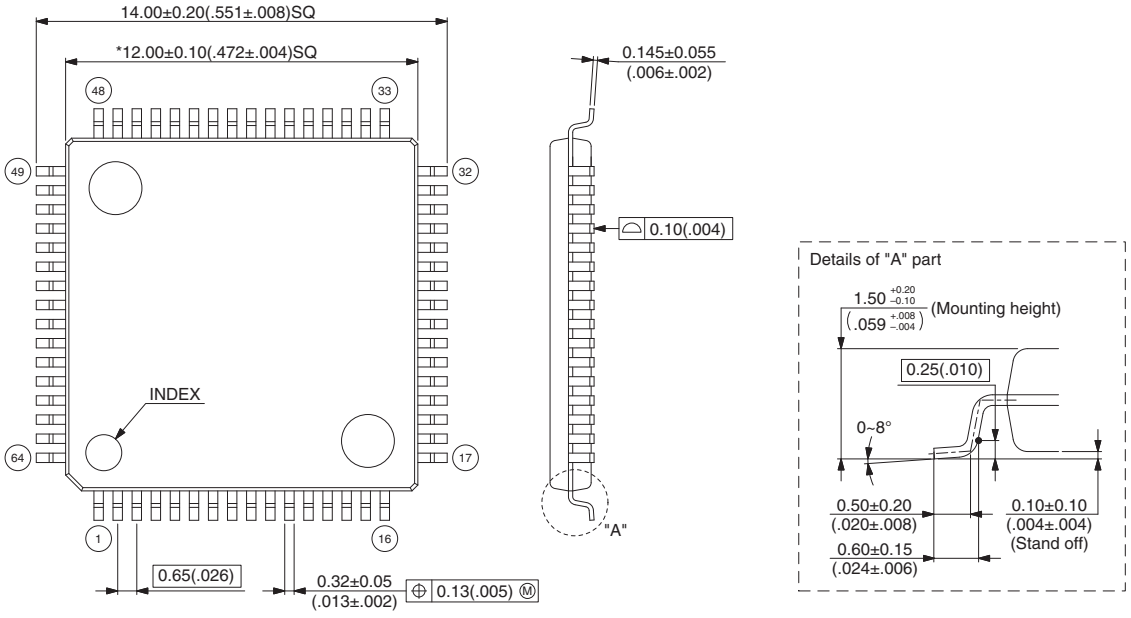
| Part number | Package |
|---|---|
| MB95F168MAPMC<br>MB95F168NAPMC<br>MB95F168JAPMC<br>MB95168MAPMC | 64-pin plastic LQFP<br>(FPT-64P-M23) |
| MB95F168MAPMC1<br>MB95F168NAPMC1<br>MB95F168JAPMC1<br>MB95168MAPMC1 | 64-pin plastic LQFP<br>(FPT-64P-M24) |
| MB2146-303A-E<br>(MB95FV100D-103PBT) | MCU board<br>(224-pin plastic PFBGA<br>(BGA-224P-M08)) |

## ■ PACKAGE DIMENSIONS

| 64-pin plastic LQFP | | |
|---|---|---|
|  | Lead pitch | 0.65 mm |
| | Package width × package length | 12.0 × 12.0 mm |
| | Lead shape | Gullwing |
| | Sealing method | Plastic mold |
| | Mounting height | 1.70 mm MAX |
| | Weight | 0.47 g |
| (FPT-64P-M23) | Code (Reference) | P-LQFP64-12×12-0.65 |

64-pin plastic LQFP
(FPT-64P-M23)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



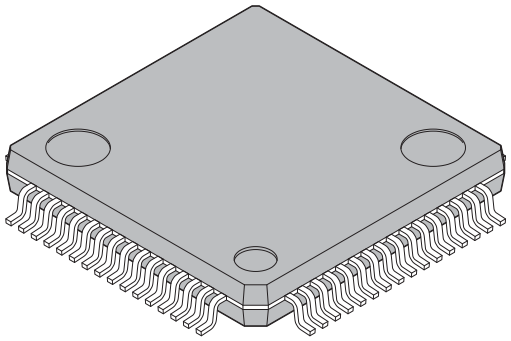



Dimensions in mm (inches).
Note: The values in parentheses are reference values

Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

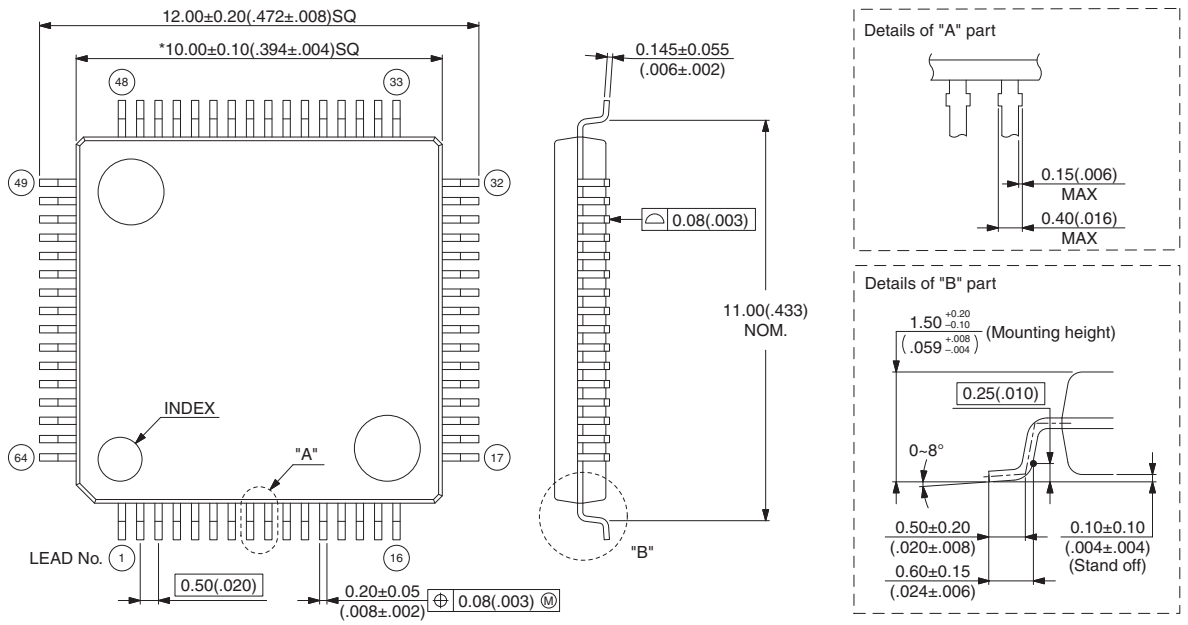
*(Continued)*

*(Continued)*

| 64-pin plastic LQFP | | |
|---|---|---|
|  (FPT-64P-M24) | Lead pitch | 0.50 mm |
| | Package width × package length | 10.0 mm × 10.0 mm |
| | Lead shape | Gullwing |
| | Sealing method | Plastic mold |
| | Code (Reference) | P-LFQFP64-10×10-0.50 |
| | | |
| | | |

64-pin plastic LQFP
(FPT-64P-M24)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.






Dimensions in mm (inches).
Note: The values in parentheses are reference values

Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

## ■ MAJOR CHANGES IN THIS EDITION

| Page | Section | Change Results |
|---|---|---|
| 35 | ■ ELECTRICAL CHARACTERISTICS<br>3. DC Characteristics | Corrected note *1 below the table.<br>(The value is 2.88 V when the low voltage detection reset is used.<br>→ The input level of P10, P23, P24 and P67 can be switched to either the “CMOS input level” or “Hysteresis input level”. The switching of the input level can be set by the input level selection register (ILSR) .) |

The vertical lines marked in the left side of the page show the changes.

# MEMO

# MEMO

# MEMO

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