FUJITSU SEMICONDUCTOR
DATA SHEET

DS702-00004-1v0-E

8-bit Microcontrollers

CMOS

New 8FX MB95410H/470H Series

MB95F414H/F414K/F416H/F416K/F418H/F418K
MB95F474H/F474K/F476H/F476K/F478H/F478K

■ DESCRIPTION

MB95410H/470H is a series of general-purpose, single-chip microcontrollers. In addition to a compact instruction set, the microcontrollers of this series contain a variety of peripheral resources.

■ FEATURES

- F²MC-8FX CPU core
  Instruction set optimized for controllers
  - Multiplication and division instructions
  - 16-bit arithmetic operations
  - Bit test branch instructions
  - Bit manipulation instructions, etc.

Note: F²MC is the abbreviation of FUJITSU Flexible Microcontroller.

- Clock
  - Selectable main clock source
    Main OSC clock (up to 16.25 MHz, maximum machine clock frequency: 8.125 MHz)
    External clock (up to 32.5 MHz, maximum machine clock frequency: 16.25 MHz)
    Main CR clock (1/8/10/12.5 MHz ±2%, maximum machine clock frequency: 12.5 MHz)
    Main PLL clock (up to 16.25 MHz, maximum machine clock frequency: 16.25 MHz)
  - Selectable subclock source
    Sub-OSC clock (32.768 kHz)
    External clock (32.768 kHz)
    Sub-CR clock (Typ: 100 kHz, Min: 50 kHz, Max: 200 kHz)
- Timer
  - 8/16-bit composite timer × 2 channels
  - 8/16-bit PPG × 2 channels
  - 16-bit reload timer × 1 channel
  - Event counter × 1 channel
  - Time-base timer × 1 channel
  - Watch prescaler × 1 channel
- UART-SIO
  - Capable of clock-asynchronous (UART) serial data transfer and clock-synchronous (SIO) serial data transfer
  - Full duplex double buffer

(Continued)

For the information for microcontroller supports, see the following website.

http://edevice.fujitsu.com/micom/en-support/

Copyright©2010-2011 FUJITSU SEMICONDUCTOR LIMITED All rights reserved
2011.5

FUJITSU

(Continued)

- I²C
  Built-in wake-up function
- External interrupt
  - Interrupt by edge detection (rising edge, falling edge, and both edges can be selected)
  - Can be used to wake up the device from different low power consumption (standby) modes
- 8/10-bit A/D converter
  - 8-bit or 10-bit resolution can be selected
- LCD controller (LCDC)
  - On MB95F414H/F414K/F416H/F416K/F418H/F418K, LCD output can be selected from 40 SEG × 4 COM to 36 SEG × 8 COM.
  - On MB95F474H/F474K/F476H/F476K/F478H/F478K, LCD output can be selected from 32 SEG × 4 COM to 28 SEG × 8 COM.
  - Internal divider resistor whose resistance value can be selected from 10 kΩ or 100 kΩ through software
  - Interrupt in sync with the LCD module frame frequency
  - Blinking function
  - Inverted display function
- Low power consumption (standby) modes
  - Stop mode
  - Sleep mode
  - Watch mode
  - Time-base timer mode
- I/O port
  - MB95F414H/F416H/F418H (maximum no. of I/O ports: 74)
    General-purpose I/O ports (N-ch open drain) : 3
    General-purpose I/O ports (CMOS I/O) : 71
  - MB95F414K/F416K/F418K (maximum no. of I/O ports: 75)
    General-purpose I/O ports (N-ch open drain) : 4
    General-purpose I/O ports (CMOS I/O) : 71
  - MB95F474H/F476H/F478H (maximum no. of I/O ports: 58)
    General-purpose I/O ports (N-ch open drain) : 3
    General-purpose I/O ports (CMOS I/O) : 55
  - MB95F474K/F476K/F478K (maximum no. of I/O ports: 59)
    General-purpose I/O ports (N-ch open drain) : 4
    General-purpose I/O ports (CMOS I/O) : 55
- On-chip debug
  - 1-wire serial control
  - Serial writing supported (asynchronous mode)
- Hardware/software watchdog timer
  - Built-in hardware watchdog timer
  - Built-in software watchdog timer
- Low-voltage detection reset circuit
  Built-in low-voltage detector
- Clock supervisor counter
  Built-in clock supervisor counter function
- Programmable port input voltage level
  CMOS input level / hysteresis input level
- Dual operation Flash memory
  The program/erase operation and the read operation can be executed in different banks (upper bank/lower bank) simultaneously.
- Flash memory security function
  Protects the content of the Flash memory

■ PRODUCT LINE-UP

• MB95410H Series

Part number / Package	MB95F414H	MB95F416H	MB95F418H	MB95F414K	MB95F416K	MB95F418K
Type	Flash memory product					
Clock supervisor counter	It supervises the main clock oscillation.					
Program ROM capacity	20 Kbyte	36 Kbyte	60 Kbyte	20 Kbyte	36 Kbyte	60 Kbyte
RAM capacity	496 bytes	1008 bytes	2032 bytes	496 bytes	1008 bytes	2032 bytes
Low-voltage detection reset	No			Yes		
Reset input	Dedicated			Selected through software		
CPU functions	• Number of basic instructions : 136 • Instruction bit length : 8 bits • Instruction length : 1 to 3 bytes • Data bit length : 1, 8 and 16 bits • Minimum instruction execution time : 61.5 ns (machine clock frequency = 16.25 MHz) • Interrupt processing time : 0.6 µs (machine clock frequency = 16.25 MHz)					
General-purpose I/O	• I/O ports (Max) : 74 • CMOS I/O : 71 • N-ch open drain: 3			• I/O ports (Max) : 75 • CMOS I/O : 71 • N-ch open drain: 4		
Time-base timer	Interval time: 0.256 ms - 8.3 s (external clock frequency = 4 MHz)					
Hardware/ software watchdog timer	• Reset generation cycle Main oscillation clock at 10 MHz: 105 ms (Min) • The sub-CR clock can be used as the source clock of the hardware watchdog timer.					
Wild register	It can be used to replace three bytes of data.					
I²C	1 channel					
	• Master/Slave sending and receiving • Bus error function and arbitration function • Detecting transmitting direction function • Start condition repeated generation and detection functions • Built-in wake-up function					
UART/SIO	3 channels					
	• Data transfer with UART/SIO is enabled. • It has a full duplex double buffer, variable data length (5/6/7/8 bits), a built-in baud rate generator and an error detection function. • It uses the NRZ type transfer format. • LSB-first data transfer and MSB-first data transfer are available to use. • Clock-asynchronous (UART) serial data transfer and clock-synchronous (SIO) serial data transfer is enabled.					
8/10-bit A/D converter	8 channels					
	8-bit or 10-bit resolution can be selected.					

(Continued)

(Continued)

Part number / Package	MB95F414H	MB95F416H	MB95F418H	MB95F414K	MB95F416K	MB95F418K
8/16-bit composite timer	2 channels					
	• Each timer can be configured as an "8-bit timer × 2 channels" or a "16-bit timer × 1 channel". • It has built-in timer function, PWC function, PWM function and input capture function. • Count clock: it can be selected from internal clocks (seven types) and external clocks. • It can output square wave.					
LCD controller (LCDC)	• COM output: 4 or 8 (selectable) • SEG output: 36 or 40 (selectable) - If the number of COM outputs is 4, the maximum number of SEG outputs is 40, and the maximum number of pixels that can be displayed 160 (4×40). - If the number of COM outputs is 8, the maximum number of SEG outputs is 36, and the maximum number of pixels that can be displayed 288 (8×36). • LCD drive power supply (bias) pins: 5 (Max)					
	• Duty LCD mode • LCD standby mode • Blinking function • Internal divider resistor whose resistance value can be selected from 10 kΩ or 100 kΩ through software • Interrupt in sync with the LCD module frame frequency • Inverted display function					
16-bit reload timer	1 channel					
	• Two clock modes and two counter operating modes can be selected • Square waveform output • Count clock: it can be selected from internal clocks (seven types) and external clocks. • Counter operating mode: reload mode or one-shot mode can be selected					
Event counter	By configuring the 16-bit reload timer and the 8/16-bit composite timer ch. 1, event counter function can be implemented. When the event counter function is used, the 16-bit reload timer and the 8/16-bit composite timer ch. 1 are unavailable.					
8/16-bit PPG	2 channels					
	• Each channel of the PPG can be used as “8-bit PPG × 2 channels” or “16-bit PPG × 1 channel” • Counter operating clock: Eight selectable clock sources					
Watch counter	• Count clock: Four selectable clock sources (125 ms, 250 ms, 500 ms or 1 s) • Counter value can be set from 0 to 63. (Capable of counting for 1 minute when the clock source is 1 second and the counter value is to 60)					
External interrupt	8 channels					
	• Interrupt by edge detection (The rising edge, falling edge, or both edges can be selected.) • It can be used to wake up the device from the standby mode.					
On-chip debug	• 1-wire serial control • It supports serial writing. (asynchronous mode)					
Watch prescaler	Eight different time intervals can be selected. (62.5 ms, 125 ms, 250 ms, 500 ms, 1 s, 2 s, 4 s, 8 s)					
Flash memory	• It supports automatic programming, Embedded Algorithm, program/erase/erase-suspend/erase-resume commands. • It has a flag indicating the completion of the operation of Embedded Algorithm. • Number of program/erase cycles: 100000 • Data retention time: 20 years • Flash security feature for protecting the content of the Flash memory					
Standby mode	Sleep mode, stop mode, watch mode, time-base timer mode					
Package	FPT-80P-M37					

- MB95470H Series

Part number / Package	MB95F474H	MB95F476H	MB95F478H	MB95F474K	MB95F476K	MB95F478K
Type	Flash memory product					
Clock supervisor counter	It supervises the main clock oscillation.					
Program ROM capacity	20 Kbyte	36 Kbyte	60 Kbyte	20 Kbyte	36 Kbyte	60 Kbyte
RAM capacity	496 bytes	1008 bytes	2032 bytes	496 bytes	1008 bytes	2032 bytes
Low-voltage detection reset	No			Yes		
Reset input	Dedicated			Selected through software		
CPU functions	• Number of basic instructions : 136 • Instruction bit length : 8 bits • Instruction length : 1 to 3 bytes • Data bit length : 1, 8 and 16 bits • Minimum instruction execution time : 61.5 ns (machine clock frequency = 16.25 MHz) • Interrupt processing time : 0.6 µs (machine clock frequency = 16.25 MHz)					
General-purpose I/O	• I/O ports (Max) : 58 • CMOS I/O : 55 • N-ch open drain: 3			• I/O ports (Max) : 59 • CMOS I/O : 55 • N-ch open drain: 4		
Time-base timer	Interval time: 0.256 ms - 8.3 s (external clock frequency = 4 MHz)					
Hardware/ software watchdog timer	• Reset generation cycle Main oscillation clock at 10 MHz: 105 ms (Min) • The sub-CR clock can be used as the source clock of the hardware watchdog timer.					
Wild register	It can be used to replace three bytes of data.					
I^2C	1 channel					
	• Master/Slave sending and receiving • Bus error function and arbitration function • Detecting transmitting direction function • Start condition repeated generation and detection functions • Built-in wake-up function					
UART/SIO	3 channels					
	• Data transfer with UART/SIO is enabled. • It has a full duplex double buffer, variable data length (5/6/7/8 bits), a built-in baud rate generator and an error detection function. • It uses the NRZ type transfer format. • LSB-first data transfer and MSB-first data transfer are available to use. • Clock-asynchronous (UART) serial data transfer and clock-synchronous (SIO) serial data transfer is enabled.					
8/10-bit A/D converter	8 channels					
	8-bit or 10-bit resolution can be selected.					
8/16-bit composite timer	2 channels					
	• Each timer can be configured as an "8-bit timer × 2 channels" or a "16-bit timer × 1 channel". • It has built-in timer function, PWC function, PWM function and input capture function. • Count clock: it can be selected from internal clocks (seven types) and external clocks. • It can output square wave.					

(Continued)

(Continued)

Part number / Package	MB95F474H	MB95F476H	MB95F478H	MB95F474K	MB95F476K	MB95F478K
LCD controller (LCDC)	• COM output: 4 or 8 (selectable) • SEG output: 28 or 32 (selectable) - If the number of COM outputs is 4, the maximum number of SEG outputs is 32, and the maximum number of pixels that can be displayed 128 (4×32). - If the number of COM outputs is 8, the maximum number of SEG outputs is 28, and the maximum number of pixels that can be displayed 224 (8×28). • LCD drive power supply (bias) pins: 4 (Max)					
	• Duty LCD mode • LCD standby mode • Blinking function • Internal divider resistor whose resistance value can be selected from 10 kΩ or 100 kΩ through software • Inverted display function					
16-bit reload timer	1 channel					
	• Two clock modes and two counter operating modes can be selected • Square waveform output • Count clock: it can be selected from internal clocks (seven types) and external clocks. • Counter operating mode: reload mode or one-shot mode can be selected					
Event counter	By configuring the 16-bit reload timer and the 8/16-bit composite timer ch. 1, event counter function can be implemented. When the event counter function is used, the 16-bit reload timer and the 8/16-bit composite timer ch. 1 are unavailable.					
8/16-bit PPG	2 channels					
	• Each channel of the PPG can be used as “8-bit PPG × 2 channels” or “16-bit PPG × 1 channel“ • Counter operating clock: Eight selectable clock sources					
Watch counter	• Count clock: Four selectable clock sources (125 ms, 250 ms, 500 ms or 1 s) • Counter value can be set from 0 to 63. (Capable of counting for 1 minute when the clock source is 1 second and the counter value is to 60)					
External interrupt	8 channels					
	Interrupt by edge detection (The rising edge, falling edge, or both edges can be selected.) It can be used to wake up the device from the standby mode.					
On-chip debug	• 1-wire serial control • It supports serial writing. (asynchronous mode)					
Watch prescaler	Eight different time intervals can be selected. (62.5 ms, 125 ms, 250 ms, 500 ms, 1 s, 2 s, 4 s, 8 s)					
Flash memory	• It supports automatic programming, Embedded Algorithm, program/erase/erase-suspend/erase-resume commands. • It has a flag indicating the completion of the operation of Embedded Algorithm. • Number of program/erase cycles: 100000 • Data retention time: 20 years • Flash security feature for protecting the content of the Flash memory					
Standby mode	Sleep mode, stop mode, watch mode, time-base timer mode					
Package	FPT-64P-M38 FPT-64P-M39					

■ OSCILLATION STABILIZATION WAIT TIME

The main CR clock oscillation stabilization wait time is fixed to the maximum value. Below is the maximum value.

Oscillation stabilization wait time	Remarks
$(2^{10} - 2) / F_{CRH}$	Approx. 128 µs (when the main CR clock is 8 MHz)

The main PLL clock oscillation stabilization wait time is fixed to the maximum value. Below is the maximum value.

Oscillation stabilization wait time	Remarks
$(2^{14} - 2) / F_{CH}$	Approx. 14.1 ms (when the main PLL clock is 4 MHz)

■ PACKAGES AND CORRESPONDING PRODUCTS

Part number / Package	MB95F414H	MB95F416H	MB95F418H	MB95F414K	MB95F416K	MB95F418K
FPT-80P-M37	O					

Part number / Package	MB95F474H	MB95F476H	MB95F478H	MB95F474K	MB95F476K	MB95F478K
FPT-64P-M38	O					
FPT-64P-M39	O					

O: Available

■ DIFFERENCES AMONG PRODUCTS AND NOTES ON PRODUCT SELECTION

• Current consumption

When using the on-chip debug function, take account of the current consumption of flash erase/write.

For details of current consumption, see "■ ELECTRICAL CHARACTERISTICS".

• Package

For details of information on each package, see "■ PACKAGES AND CORRESPONDING PRODUCTS" and "■ PACKAGE DIMENSION".

• Operating voltage

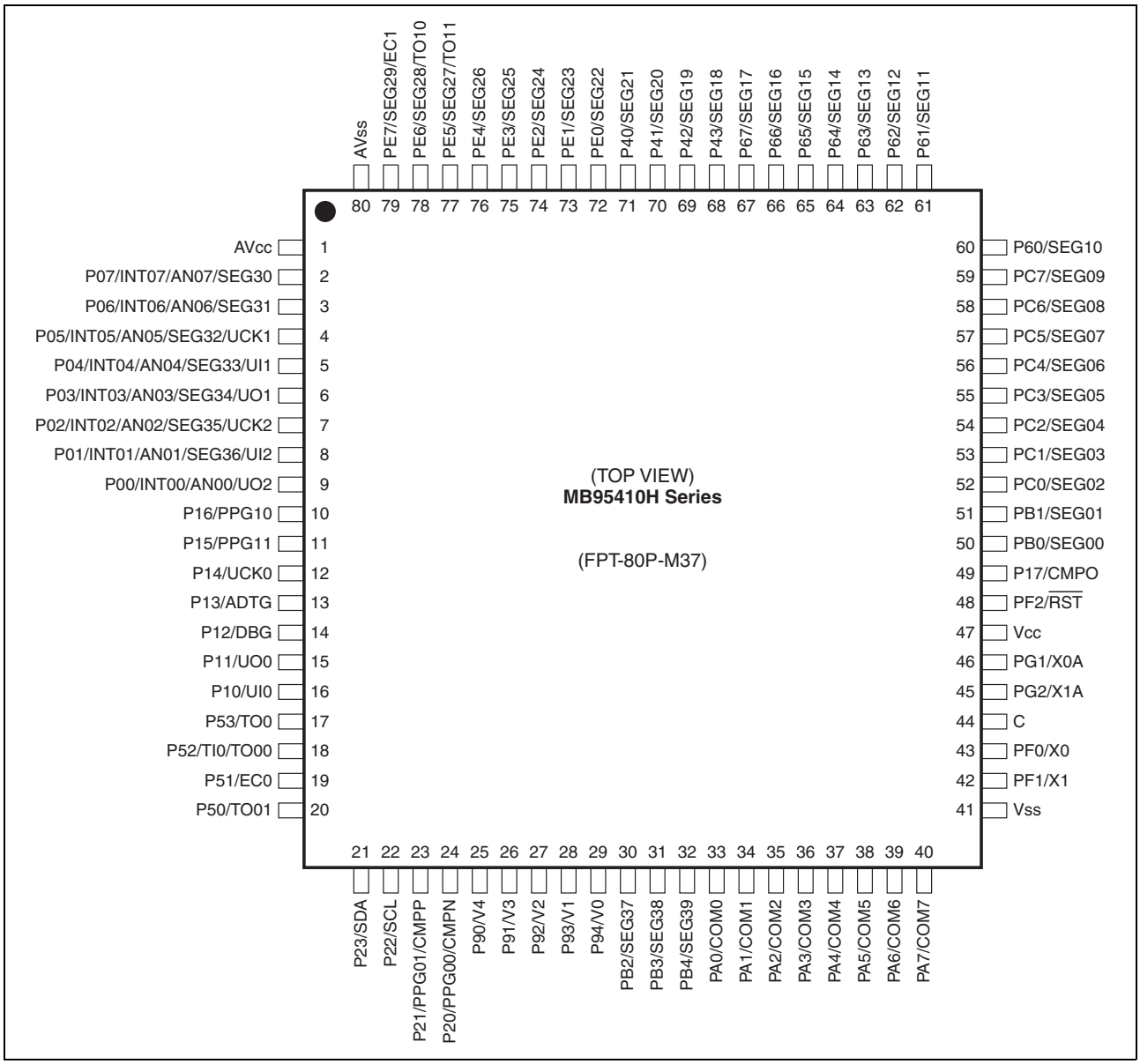
The operating voltage varies, depending on whether the on-chip debug function is used or not.

For details of the operating voltage, see "■ ELECTRICAL CHARACTERISTICS".

• On-chip debug function

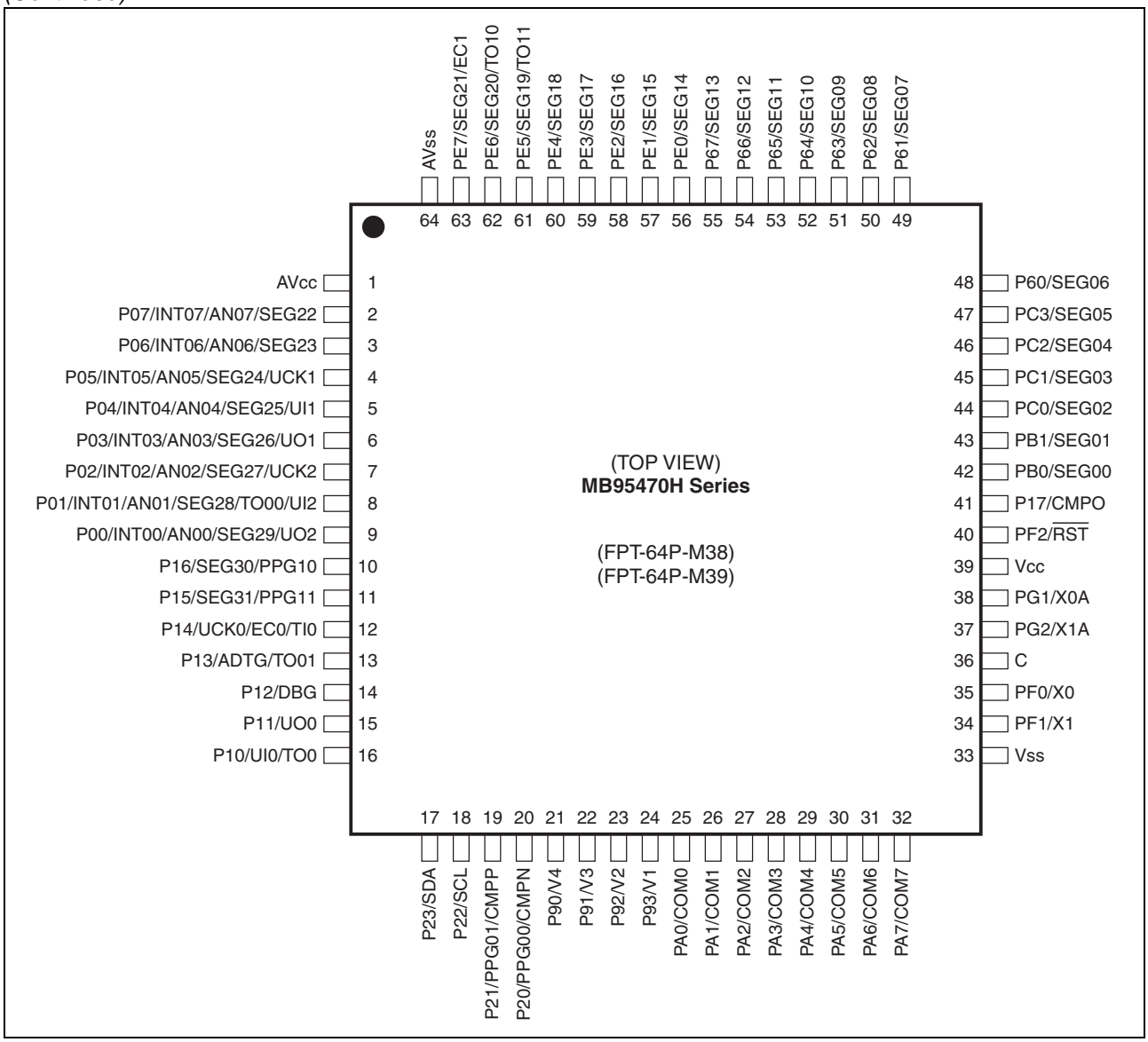
The on-chip debug function requires that V_{CC}, V_{SS} and 1 serial-wire be connected to an evaluation tool. For details of the connection method, refer to "CHAPTER 31 EXAMPLE OF SERIAL PROGRAMMING CONNECTION" in the hardware manual of the MB95410H/470H Series.

■ PIN ASSIGNMENT



(Continued)

(Continued)


AVss
PE7/SEG21/EC1
PE6/SEG20/TO10
PE5/SEG19/TO11
PE4/SEG18
PE3/SEG17
PE2/SEG16
PE1/SEG15
PE0/SEG14
P67/SEG13
P66/SEG12
P65/SEG11
P64/SEG10
P63/SEG09
P62/SEG08
P61/SEG07
64 63 62 61 60 59 58 57 56 55 54 53 52 51 50 49
AVcc 1
P07/INT07/AN07/SEG22 2
P06/INT06/AN06/SEG23 3
P05/INT05/AN05/SEG24/UCK1 4
P04/INT04/AN04/SEG25/UI1 5
P03/INT03/AN03/SEG26/UO1 6
P02/INT02/AN02/SEG27/UCK2 7
P01/INT01/AN01/SEG28/TO00/UI2 8
P00/INT00/AN00/SEG29/UO2 9
P16/SEG30/PPG10 10
P15/SEG31/PPG11 11
P14/UCK0/EC0/TI0 12
P13/ADTG/TO01 13
P12/DBG 14
P11/UO0 15
P10/UI0/TO0 16
(TOP VIEW)
MB95470H Series
(FPT-64P-M38)
(FPT-64P-M39)
48 P60/SEG06
47 PC3/SEG05
46 PC2/SEG04
45 PC1/SEG03
44 PC0/SEG02
43 PB1/SEG01
42 PB0/SEG00
41 P17/CMPO
40 PF2/RST
39 Vcc
38 PG1/X0A
37 PG2/X1A
36 C
35 PF0/X0
34 PF1/X1
33 Vss
17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32
P23/SDA
P22/SCL
P21/PPG01/CMPP
P20/PPG00/CMPN
P90/V4
P91/V3
P92/V2
P93/V1
PA0/COM0
PA1/COM1
PA2/COM2
PA3/COM3
PA4/COM4
PA5/COM5
PA6/COM6
PA7/COM7

■ PIN DESCRIPTION (MB95410H Series)

Pin no.	Pin name	I/O circuit type*	Function
1	AV_{CC}	—	A/D converter power supply pin
2	P07	S	General-purpose I/O port
	INT07		External interrupt input pin
	AN07		A/D analog input pin
	SEG30		LCDC SEG output pin
3	P06	S	General-purpose I/O port
	INT06		External interrupt input pin
	AN06		A/D analog input pin
	SEG31		LCDC SEG output pin
4	P05	S	General-purpose I/O port
	INT05		External interrupt input pin
	AN05		A/D analog input pin
	SEG32		LCDC SEG output pin
	UCK1		UART/SIO ch. 1 clock I/O pin
5	P04	V	General-purpose I/O port
	INT04		External interrupt input pin
	AN04		A/D analog input pin
	SEG33		LCDC SEG output pin
	UI1		UART/SIO ch. 1 data input pin
6	P03	S	General-purpose I/O port
	INT03		External interrupt input pin
	AN03		A/D analog input pin
	SEG34		LCDC SEG output pin
	UO1		UART/SIO ch. 1 data output pin
7	P02	S	General-purpose I/O port
	INT02		External interrupt input pin
	AN02		A/D analog input pin
	SEG35		LCDC SEG output pin
	UCK2		UART/SIO ch. 2 clock I/O pin
8	P01	V	General-purpose I/O port
	INT01		External interrupt input pin
	AN01		A/D analog input pin
	SEG36		LCDC SEG output pin
	UI2		UART/SIO ch. 2 data input pin

(Continued)

Pin no.	Pin name	I/O circuit type*	Function
9	P00	W	General-purpose I/O port
	INT00		External interrupt input pin
	AN00		A/D analog input pin
	UO2		UART/SIO ch. 2 data output pin
10	P16	Y	General-purpose I/O port
	PPG10		8/16-bit PPG ch. 1 output pin
11	P15	Y	General-purpose I/O port
	PPG11		8/16-bit PPG ch. 1 output pin
12	P14	H	General-purpose I/O port
	UCK0		UART/SIO ch. 0 clock I/O pin
13	P13	H	General-purpose I/O port
	ADTG		A/D trigger input (ADTG) pin
14	P12	D	General-purpose I/O port
	DBG		DBG input pin
15	P11	H	General-purpose I/O port
	UO0		UART/SIO ch. 0 data output pin
16	P10	G	General-purpose I/O port
	UI0		UART/SIO ch. 0 data input pin
17	P53	H	General-purpose I/O port
	TO0		16-bit reload timer output pin
18	P52	H	General-purpose I/O port
	TI0		16-bit reload timer input pin
	TO00		8/16-bit composite timer ch. 0 output pin
19	P51	H	General-purpose I/O port
	EC0		8/16-bit composite timer ch. 0 clock input pin
20	P50	H	General-purpose I/O port
	TO01		8/16-bit composite timer ch. 0 output pin
21	P23	I	General-purpose I/O port
	SDA		I^2C data I/O pin
22	P22	I	General-purpose I/O port
	SCL		I^2C clock I/O pin
23	P21	T	General-purpose I/O port
	PPG01		8/16-bit PPG ch. 0 output pin
	CMPP		Voltage comparator input pin
24	P20	T	General-purpose I/O port
	PPG00		8/16-bit PPG ch. 0 output pin
	CMPN		Voltage comparator input pin

(Continued)

Pin no.	Pin name	I/O circuit type*	Function
25	P90	R	General-purpose I/O port
	V4		LCDC drive power supply pin
26	P91	R	General-purpose I/O port
	V3		LCDC drive power supply pin
27	P92	R	General-purpose I/O port
	V2		LCDC drive power supply pin
28	P93	R	General-purpose I/O port
	V1		LCDC drive power supply pin
29	P94	R	General-purpose I/O port
	V0		LCDC drive power supply pin
30	PB2	M	General-purpose I/O port
	SEG37		LCDC SEG output pin
31	PB3	M	General-purpose I/O port
	SEG38		LCDC SEG output pin
32	PB4	M	General-purpose I/O port
	SEG39		LCDC SEG output pin
33	PA0	M	General-purpose I/O port
	COM0		LCDC COM output pin
34	PA1	M	General-purpose I/O port
	COM1		LCDC COM output pin
35	PA2	M	General-purpose I/O port
	COM2		LCDC COM output pin
36	PA3	M	General-purpose I/O port
	COM3		LCDC COM output pin
37	PA4	M	General-purpose I/O port
	COM4		LCDC COM output pin
38	PA5	M	General-purpose I/O port
	COM5		LCDC COM output pin
39	PA6	M	General-purpose I/O port
	COM6		LCDC COM output pin
40	PA7	M	General-purpose I/O port
	COM7		LCDC COM output pin
41	V_{SS}	—	Power supply pin (GND)
42	PF1	B	General-purpose I/O port
	X1		Main clock oscillation pin
43	PF0	B	General-purpose I/O port
	X0		Main clock oscillation pin

(Continued)

Pin no.	Pin name	I/O circuit type*	Function
44	C	—	Capacitor connection pin
45	PG2	C	General-purpose I/O port
	X1A		Subclock oscillation pin (32 kHz)
46	PG1	C	General-purpose I/O port
	X0A		Subclock oscillation pin (32 kHz)
47	V_{CC}	—	Power supply pin
48	PF2	A	General-purpose I/O port
	$\overline{RST}$		Reset pin Dedicate reset pin for MB95F414H/F416H/F418H
49	P17	H	General-purpose I/O port
	CMPO		Voltage comparator output pin
50	PB0	M	General-purpose I/O port
	SEG00		LCDC SEG output pin
51	PB1	M	General-purpose I/O port
	SEG01		LCDC SEG output pin
52	PC0	M	General-purpose I/O port
	SEG02		LCDC SEG output pin
53	PC1	M	General-purpose I/O port
	SEG03		LCDC SEG output pin
54	PC2	M	General-purpose I/O port
	SEG04		LCDC SEG output pin
55	PC3	M	General-purpose I/O port
	SEG05		LCDC SEG output pin
56	PC4	M	General-purpose I/O port
	SEG06		LCDC SEG output pin
57	PC5	M	General-purpose I/O port
	SEG07		LCDC SEG output pin
58	PC6	M	General-purpose I/O port
	SEG08		LCDC SEG output pin
59	PC7	M	General-purpose I/O port
	SEG09		LCDC SEG output pin
60	P60	M	General-purpose I/O port
	SEG10		LCDC SEG output pin
61	P61	M	General-purpose I/O port
	SEG11		LCDC SEG output pin
62	P62	M	General-purpose I/O port
	SEG12		LCDC SEG output pin

(Continued)

Pin no.	Pin name	I/O circuit type*	Function
63	P63	M	General-purpose I/O port
	SEG13		LCDC SEG output pin
64	P64	M	General-purpose I/O port
	SEG14		LCDC SEG output pin
65	P65	M	General-purpose I/O port
	SEG15		LCDC SEG output pin
66	P66	M	General-purpose I/O port
	SEG16		LCDC SEG output pin
67	P67	M	General-purpose I/O port
	SEG17		LCDC SEG output pin
68	P43	M	General-purpose I/O port
	SEG18		LCDC SEG output pin
69	P42	M	General-purpose I/O port
	SEG19		LCDC SEG output pin
70	P41	M	General-purpose I/O port
	SEG20		LCDC SEG output pin
71	P40	M	General-purpose I/O port
	SEG21		LCDC SEG output pin
72	PE0	M	General-purpose I/O port
	SEG22		LCDC SEG output pin
73	PE1	M	General-purpose I/O port
	SEG23		LCDC SEG output pin
74	PE2	M	General-purpose I/O port
	SEG24		LCDC SEG output pin
75	PE3	M	General-purpose I/O port
	SEG25		LCDC SEG output pin
76	PE4	M	General-purpose I/O port
	SEG26		LCDC SEG output pin
77	PE5	M	General-purpose I/O port
	SEG27		LCDC SEG output pin
	TO11		8/16-bit composite timer ch. 1 output pin
78	PE6	M	General-purpose I/O port
	SEG28		LCDC SEG output pin
	TO10		8/16-bit composite timer ch. 1 output pin

(Continued)

(Continued)

Pin no.	Pin name	I/O circuit type*	Function
79	PE7	M	General-purpose I/O port
	SEG29		LCDC SEG output pin
	EC1		8/16-bit composite timer ch. 1 clock input pin
80	AV_{SS}	—	A/D converter power supply pin (GND)

*: For the I/O circuit types, see "■ I/O CIRCUIT TYPE".

■ PIN DESCRIPTION (MB95470H Series)

Pin no.	Pin name	I/O circuit type*	Function
1	AV_{CC}	—	A/D converter power supply pin
2	P07	S	General-purpose I/O port
	INT07		External interrupt input pin
	AN07		A/D analog input pin
	SEG22		LCDC SEG output pin
3	P06	S	General-purpose I/O port
	INT06		External interrupt input pin
	AN06		A/D analog input pin
	SEG23		LCDC SEG output pin
4	P05	S	General-purpose I/O port
	INT05		External interrupt input pin
	AN05		A/D analog input pin
	SEG24		LCDC SEG output pin
	UCK1		UART/SIO ch. 1 clock I/O pin
5	P04	V	General-purpose I/O port
	INT04		External interrupt input pin
	AN04		A/D analog input pin
	SEG25		LCDC SEG output pin
	UI1		UART/SIO ch. 1 data input pin
6	P03	S	General-purpose I/O port
	INT03		External interrupt input pin
	AN03		A/D analog input pin
	SEG26		LCDC SEG output pin
	UO1		UART/SIO ch. 1 data output pin
7	P02	S	General-purpose I/O port
	INT02		External interrupt input pin
	AN02		A/D analog input pin
	SEG27		LCDC SEG output pin
	UCK2		UART/SIO ch. 2 clock I/O pin
8	P01	V	General-purpose I/O port
	INT01		External interrupt input pin
	AN01		A/D analog input pin
	SEG28		LCDC SEG output pin
	TO00		8/16-bit composite timer ch. 0 output pin
	UI2		UART/SIO ch. 2 data input pin

(Continued)

Pin no.	Pin name	I/O circuit type*	Function
9	P00	S	General-purpose I/O port
	INT00		External interrupt input pin
	AN00		A/D analog input pin
	SEG29		LCDC SEG output pin
	UO2		UART/SIO ch. 2 data output pin
10	P16	M	General-purpose I/O port
	SEG30		LCDC SEG output pin
	PPG10		8/16-bit PPG ch. 1 output pin
11	P15	M	General-purpose I/O port
	SEG31		LCDC SEG output pin
	PPG11		8/16-bit PPG ch. 1 output pin
12	P14	H	General-purpose I/O port
	UCK0		UART/SIO ch. 0 clock I/O pin
	EC0		8/16-bit composite timer ch. 0 clock input pin
	TI0		16-bit reload timer input pin
13	P13	H	General-purpose I/O port
	ADTG		A/D trigger input (ADTG) pin
	TO01		8/16-bit composite timer ch. 0 output pin
14	P12	D	General-purpose I/O port
	DBG		DBG input pin
15	P11	H	General-purpose I/O port
	UO0		UART/SIO ch. 0 data output pin
16	P10	G	General-purpose I/O port
	UI0		UART/SIO ch. 0 data input pin
	TO0		16-bit reload timer output pin
17	P23	I	General-purpose I/O port
	SDA		I^2C data I/O pin
18	P22	I	General-purpose I/O port
	SCL		I^2C clock I/O pin
19	P21	T	General-purpose I/O port
	PPG01		8/16-bit PPG ch. 0 output pin
	CMPP		Voltage comparator input pin
20	P20	T	General-purpose I/O port
	PPG00		8/16-bit PPG ch. 0 output pin
	CMPN		Voltage comparator input pin

(Continued)

Pin no.	Pin name	I/O circuit type*	Function
21	P90	R	General-purpose I/O port
	V4		LCDC drive power supply pin
22	P91	R	General-purpose I/O port
	V3		LCDC drive power supply pin
23	P92	R	General-purpose I/O port
	V2		LCDC drive power supply pin
24	P93	R	General-purpose I/O port
	V1		LCDC drive power supply pin
25	PA0	M	General-purpose I/O port
	COM0		LCDC COM output pin
26	PA1	M	General-purpose I/O port
	COM1		LCDC COM output pin
27	PA2	M	General-purpose I/O port
	COM2		LCDC COM output pin
28	PA3	M	General-purpose I/O port
	COM3		LCDC COM output pin
29	PA4	M	General-purpose I/O port
	COM4		LCDC COM output pin
30	PA5	M	General-purpose I/O port
	COM5		LCDC COM output pin
31	PA6	M	General-purpose I/O port
	COM6		LCDC COM output pin
32	PA7	M	General-purpose I/O port
	COM7		LCDC COM output pin
33	V_{SS}	—	Power supply pin (GND)
34	PF1	B	General-purpose I/O port
	X1		Main clock oscillation pin
35	PF0	B	General-purpose I/O port
	X0		Main clock oscillation pin
36	C	—	Capacitor connection pin
37	PG2	C	General-purpose I/O port
	X1A		Subclock oscillation pin (32 kHz)
38	PG1	C	General-purpose I/O port
	X0A		Subclock oscillation pin (32 kHz)
39	V_{CC}	—	Power supply pin
40	PF2	A	General-purpose I/O port
	$\overline{RST}$		Reset pin Dedicated reset pin for MB95F474H/F476H/F478H

(Continued)

Pin no.	Pin name	I/O circuit type*	Function
41	P17	H	General-purpose I/O port
	CMPO		Voltage comparator output pin
42	PB0	M	General-purpose I/O port
	SEG00		LCDC SEG output pin
43	PB1	M	General-purpose I/O port
	SEG01		LCDC SEG output pin
44	PC0	M	General-purpose I/O port
	SEG02		LCDC SEG output pin
45	PC1	M	General-purpose I/O port
	SEG03		LCDC SEG output pin
46	PC2	M	General-purpose I/O port
	SEG04		LCDC SEG output pin
47	PC3	M	General-purpose I/O port
	SEG05		LCDC SEG output pin
48	P60	M	General-purpose I/O port
	SEG06		LCDC SEG output pin
49	P61	M	General-purpose I/O port
	SEG07		LCDC SEG output pin
50	P62	M	General-purpose I/O port
	SEG08		LCDC SEG output pin
51	P63	M	General-purpose I/O port
	SEG09		LCDC SEG output pin
52	P64	M	General-purpose I/O port
	SEG10		LCDC SEG output pin
53	P65	M	General-purpose I/O port
	SEG11		LCDC SEG output pin
54	P66	M	General-purpose I/O port
	SEG12		LCDC SEG output pin
55	P67	M	General-purpose I/O port
	SEG13		LCDC SEG output pin
56	PE0	M	General-purpose I/O port
	SEG14		LCDC SEG output pin
57	PE1	M	General-purpose I/O port
	SEG15		LCDC SEG output pin

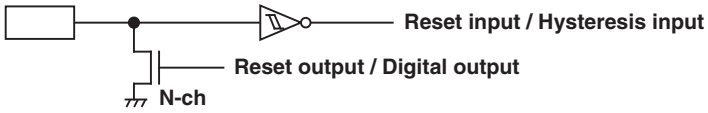
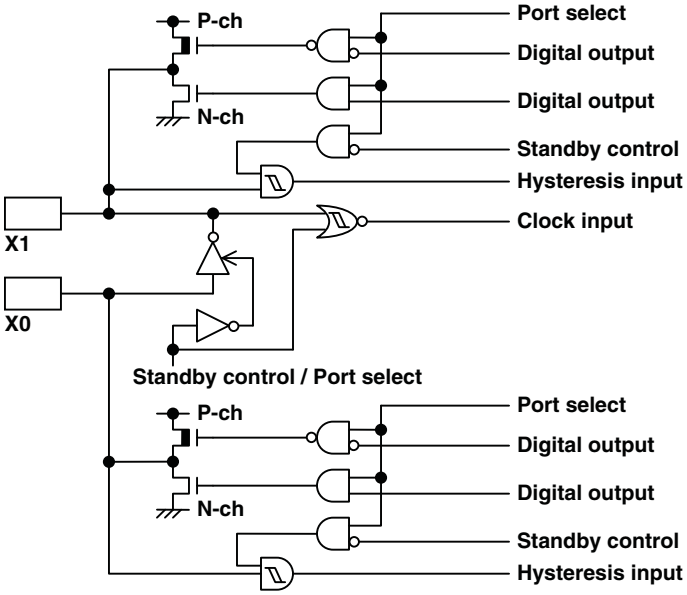
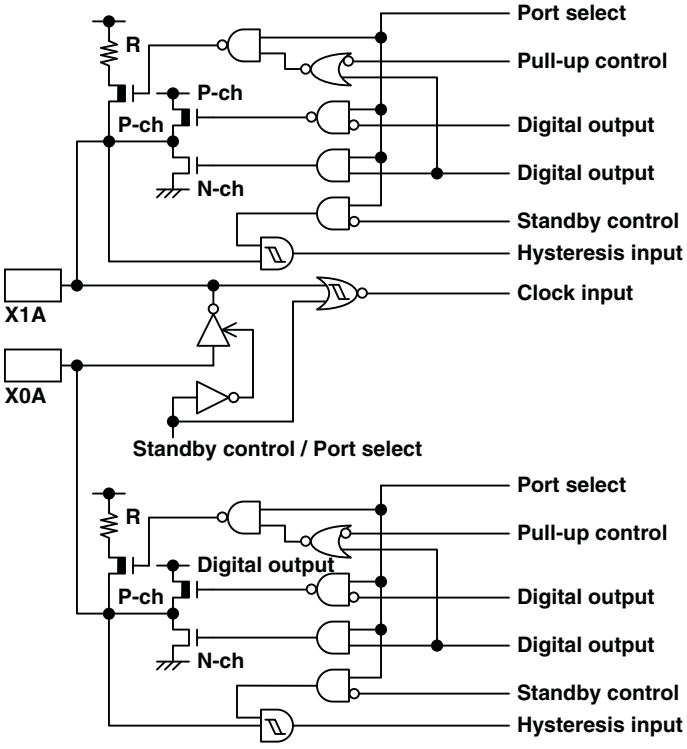
(Continued)

(Continued)

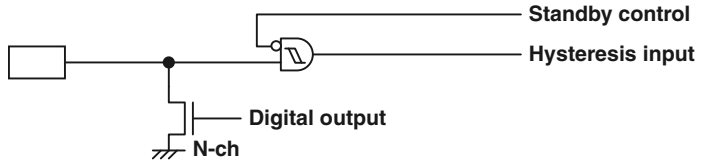
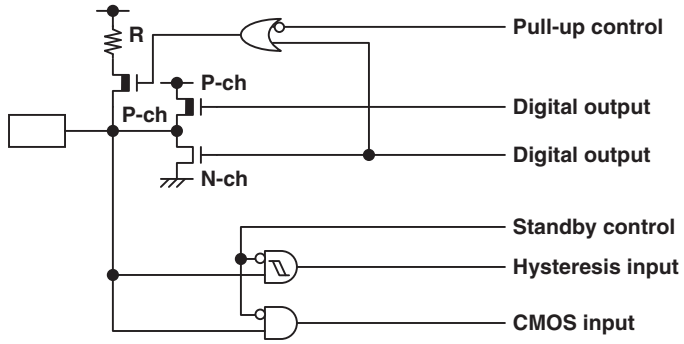
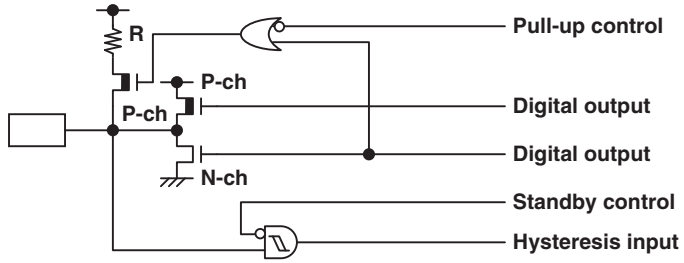
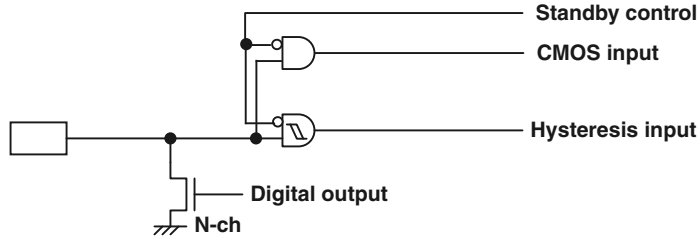
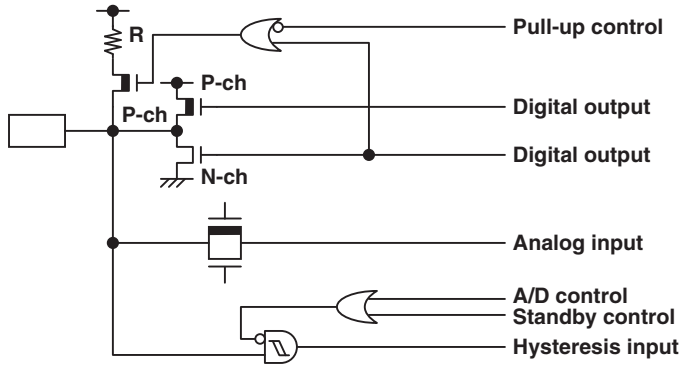
Pin no.	Pin name	I/O circuit type*	Function
58	PE2	M	General-purpose I/O port
	SEG16		LCDC SEG output pin
59	PE3	M	General-purpose I/O port
	SEG17		LCDC SEG output pin
60	PE4	M	General-purpose I/O port
	SEG18		LCDC SEG output pin
61	PE5	M	General-purpose I/O port
	SEG19		LCDC SEG output pin
	TO11		8/16-bit composite timer ch. 1 output pin
62	PE6	M	General-purpose I/O port
	SEG20		LCDC SEG output pin
	TO10		8/16-bit composite timer ch. 1 output pin
63	PE7	M	General-purpose I/O port
	SEG21		LCDC SEG output pin
	EC1		8/16-bit composite timer ch. 1 clock input pin
64	AV_{SS}	—	A/D converter power supply pin (GND)

*: For the I/O circuit types, see “■ I/O CIRCUIT TYPE”.

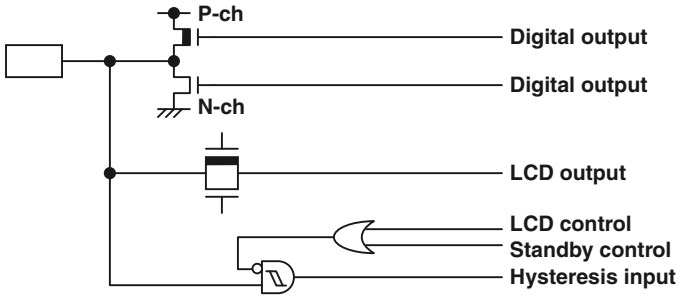
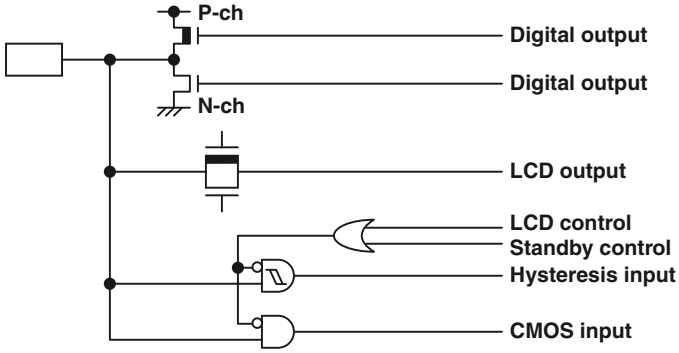
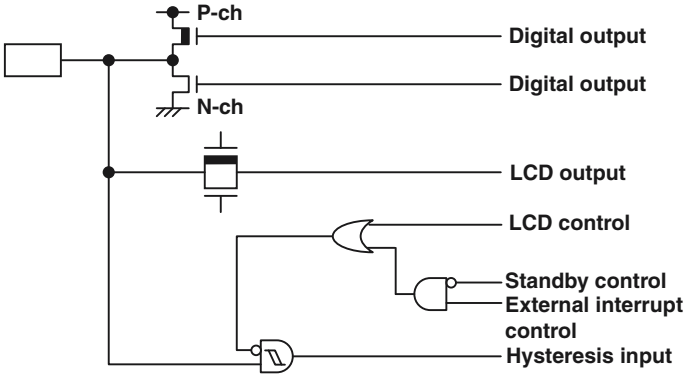
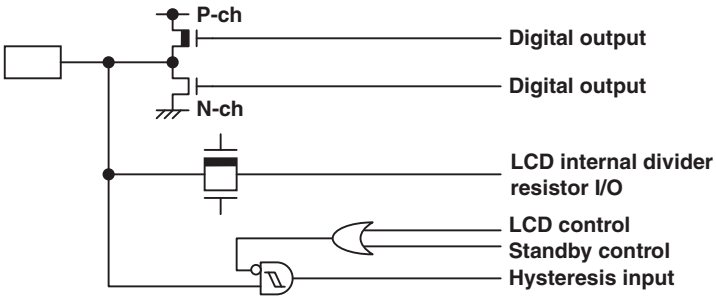
■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		• N-ch open drain output • Hysteresis input • Reset output
B		• Oscillation circuit • High-speed side Feedback resistance: approx. 1 MΩ • CMOS output • Hysteresis input
C		• Oscillation circuit • Low-speed side Feedback resistance: approx. 10 MΩ • CMOS output • Hysteresis input • Pull-up control available

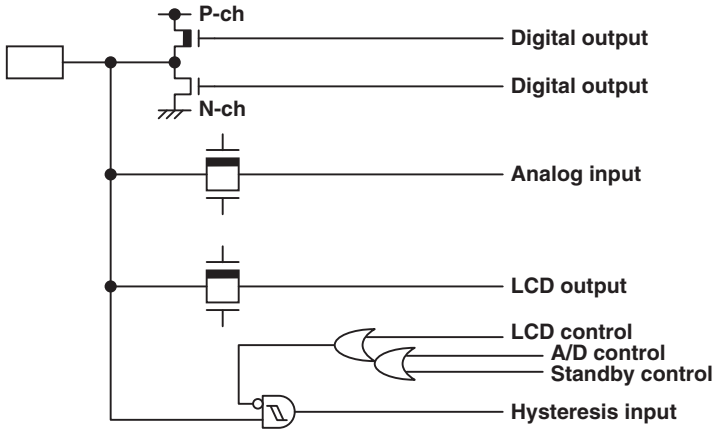
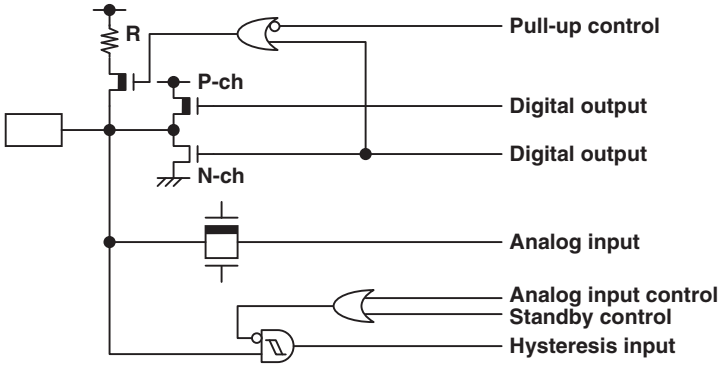
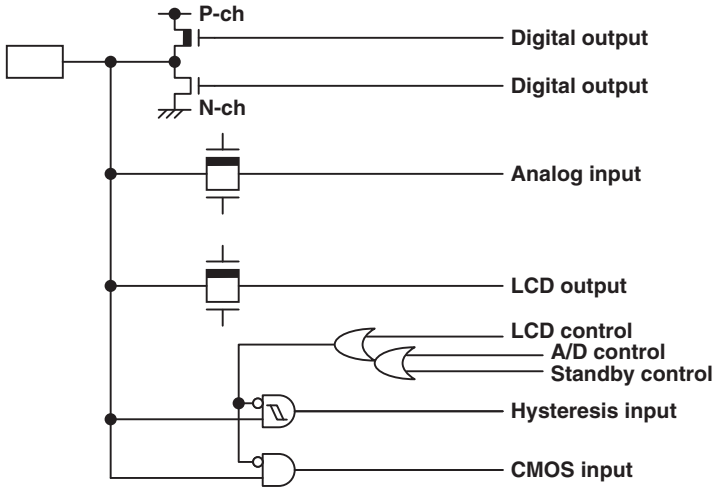
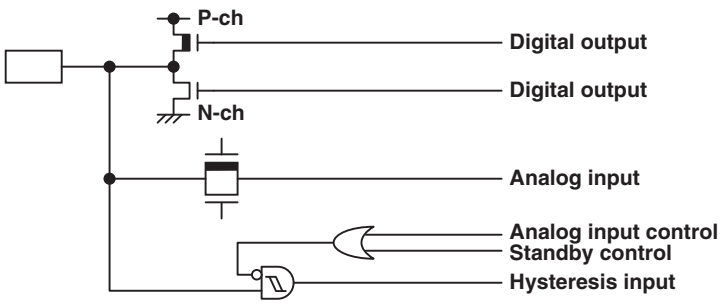
(Continued)

Type	Circuit	Remarks
D		• N-ch open drain output • Hysteresis input
G		• CMOS output • Hysteresis input • CMOS input • Pull-up control available
H		• CMOS output • Hysteresis input • Pull-up control available
I		• N-ch open drain output • CMOS input • Hysteresis input
J		• CMOS output • Hysteresis input • Analog input • Pull-up control available

(Continued)

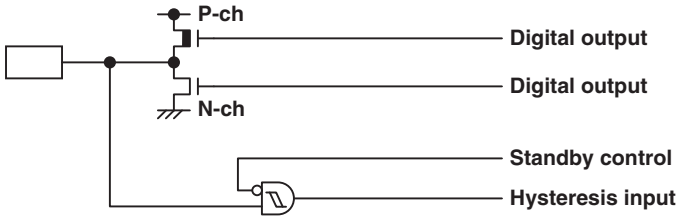
Type	Circuit	Remarks
M		• CMOS output • LCD output • Hysteresis input
N		• CMOS output • LCD output • Hysteresis input • CMOS input
Q		• CMOS output • LCD output • Hysteresis input
R		• CMOS output • LCD power supply • Hysteresis input

(Continued)

Type	Circuit	Remarks
S		• CMOS output • LCD output • Hysteresis input • Analog input
T		• CMOS output • Hysteresis input • Analog input • Pull-up control available
V		• CMOS output • LCD output • Hysteresis input • Analog input • CMOS input
W		• CMOS output • Hysteresis input • Analog input

(Continued)

(Continued)

Type	Circuit	Remarks
Y		• CMOS output • Hysteresis input

■ NOTES ON DEVICE HANDLING

• Preventing latch-ups

When using the device, ensure that the voltage applied does not exceed the maximum voltage rating.
In a CMOS IC, if a voltage higher than V_{CC} or a voltage lower than V_{SS} is applied to an input/output pin that is neither a medium-withstand voltage pin nor a high-withstand voltage pin, or if a voltage out of the rating range of power supply voltage mentioned in "1. Absolute Maximum Ratings" of "■ ELECTRICAL CHARACTERISTICS" is applied to the V_{CC} pin or the V_{SS} pin, a latch-up may occur.
When a latch-up occurs, power supply current increases significantly, which may cause a component to be thermally destroyed.

• Stabilizing supply voltage

Supply voltage must be stabilized.
A malfunction may occur when power supply voltage fluctuates rapidly even though the fluctuation is within the guaranteed operating range of the V_{CC} power supply voltage.
As a rule of voltage stabilization, suppress voltage fluctuation so that the fluctuation in V_{CC} ripple (p-p value) at the commercial frequency (50 Hz/60 Hz) does not exceed 10% of the standard V_{CC} value, and the transient fluctuation rate does not exceed 0.1 V/ms at a momentary fluctuation such as switching the power supply.

• Notes on using the external clock

When an external clock is used, oscillation stabilization wait time is required for power-on reset, wake-up from subclock mode or stop mode.

■ PIN CONNECTION

• Treatment of unused input pins

If an unused input pin is left unconnected, a component may be permanently damaged due to malfunctions or latch-ups. Always pull up or pull down an unused input pin through a resistor of at least 2 kΩ. Set an unused input/output pin to the output state and leave it unconnected, or set it to the input state and treat it the same as an unused input pin. If there is an unused output pin, leave it unconnected.

• Power supply pins

To reduce unnecessary electro-magnetic emission, prevent malfunctions of strobe signals due to an increase in the ground level, and conform to the total output current standard, always connect the V_{CC} pin and the V_{SS} pin to the power supply and ground outside the device. In addition, connect the current supply source to the V_{CC} pin and the V_{SS} pin with low impedance.
It is also advisable to connect a ceramic capacitor of approximately 0.1 µF as a bypass capacitor between the V_{CC} pin and the V_{SS} pin at a location close to this device.

• DBG pin

Connect the DBG pin directly to an external pull-up resistor.
To prevent the device from unintentionally entering the debug mode due to noise, minimize the distance between the DBG pin and the V_{CC} or V_{SS} pin when designing the layout of the printed circuit board.
The DBG pin should not stay at "L" level after power-on until the reset output is released.

• $\overline{RST}$ pin

Connect the $\overline{RST}$ pin directly to an external pull-up resistor.
To prevent the device from unintentionally entering the reset mode due to noise, minimize the distance between the $\overline{RST}$ pin and the V_{CC} or V_{SS} pin when designing the layout of the printed circuit board.
The PF2/$\overline{RST}$ pin functions as the reset input/output pin after power-on. In addition, the reset output function of the PF2/$\overline{RST}$ pin can be enabled by the RSTOE bit in the SYSC register, and the reset input function or the general purpose I/O function can be selected by the RSTEN bit in the SYSC register.

• Analog power supply

Always set the same potential to AV_{CC} and V_{CC} pins. When V_{CC} is larger than AV_{CC}, the current may flow through the AN00 to AN07 pins.

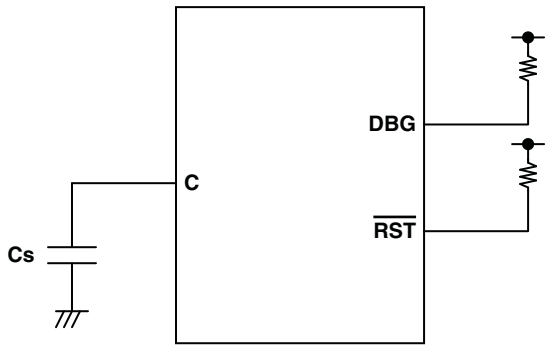
• Treatment of power supply pins on the A/D converter

Ensure that AV_{CC} is equal to V_{CC} and AV_{SS} equal to V_{SS} even when the A/D converter is not in use.
Noise riding on the AV_{CC} pin may cause accuracy degradation. Therefore, connect a ceramic capacitor of 0.1 µF (approx.) as a bypass capacitor between the AV_{CC} pin and the AV_{SS} pin in the vicinity of this device.

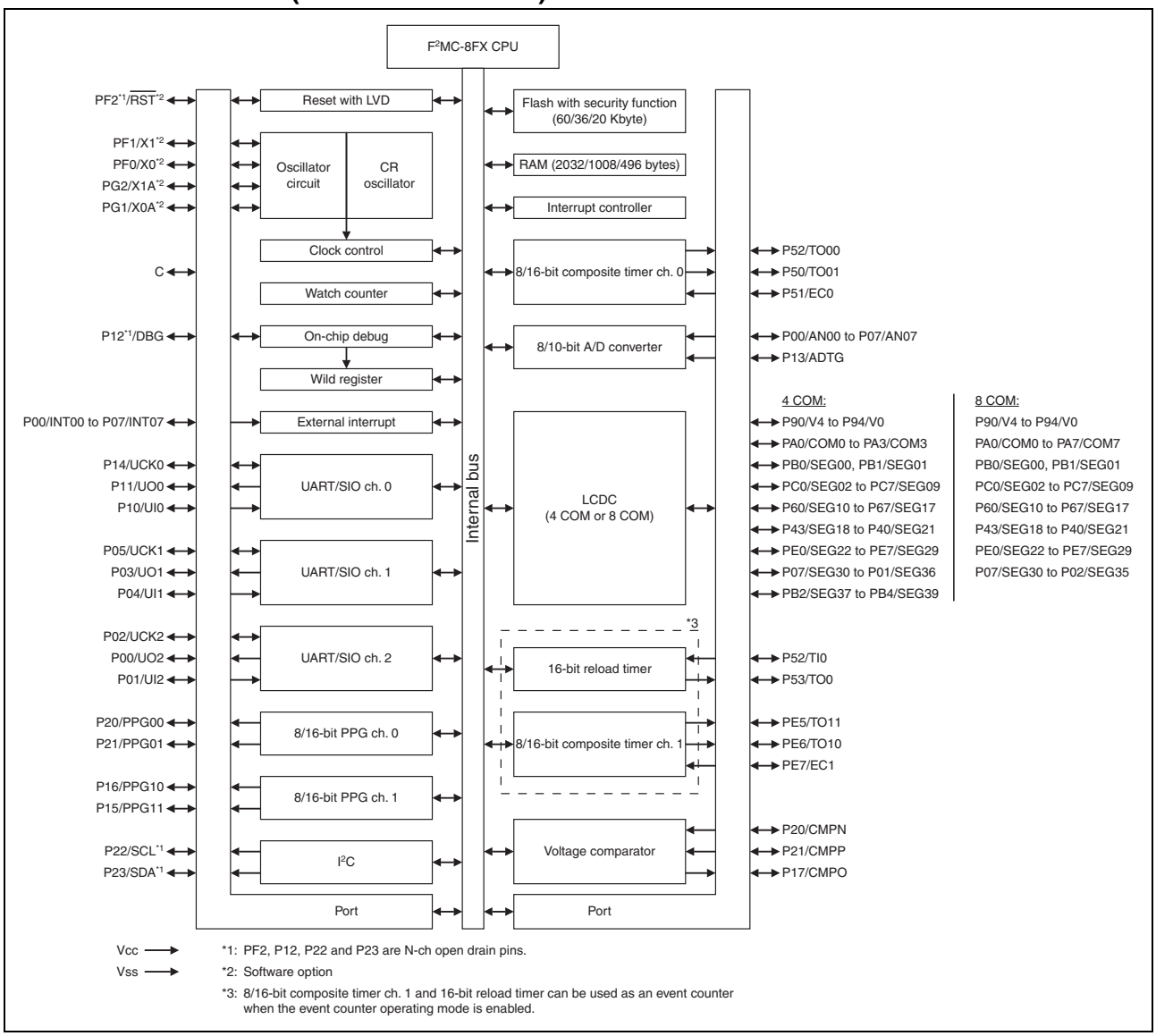
• C pin

Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. The bypass capacitor for the V_{CC} pin must have a capacitance larger than C_S. For the connection to a smoothing capacitor C_S, see the diagram below. To prevent the device from unintentionally entering an unknown mode due to noise, minimize the distance between the C pin and C_S and the distance between C_S and the V_{SS} pin when designing the layout of a printed circuit board.

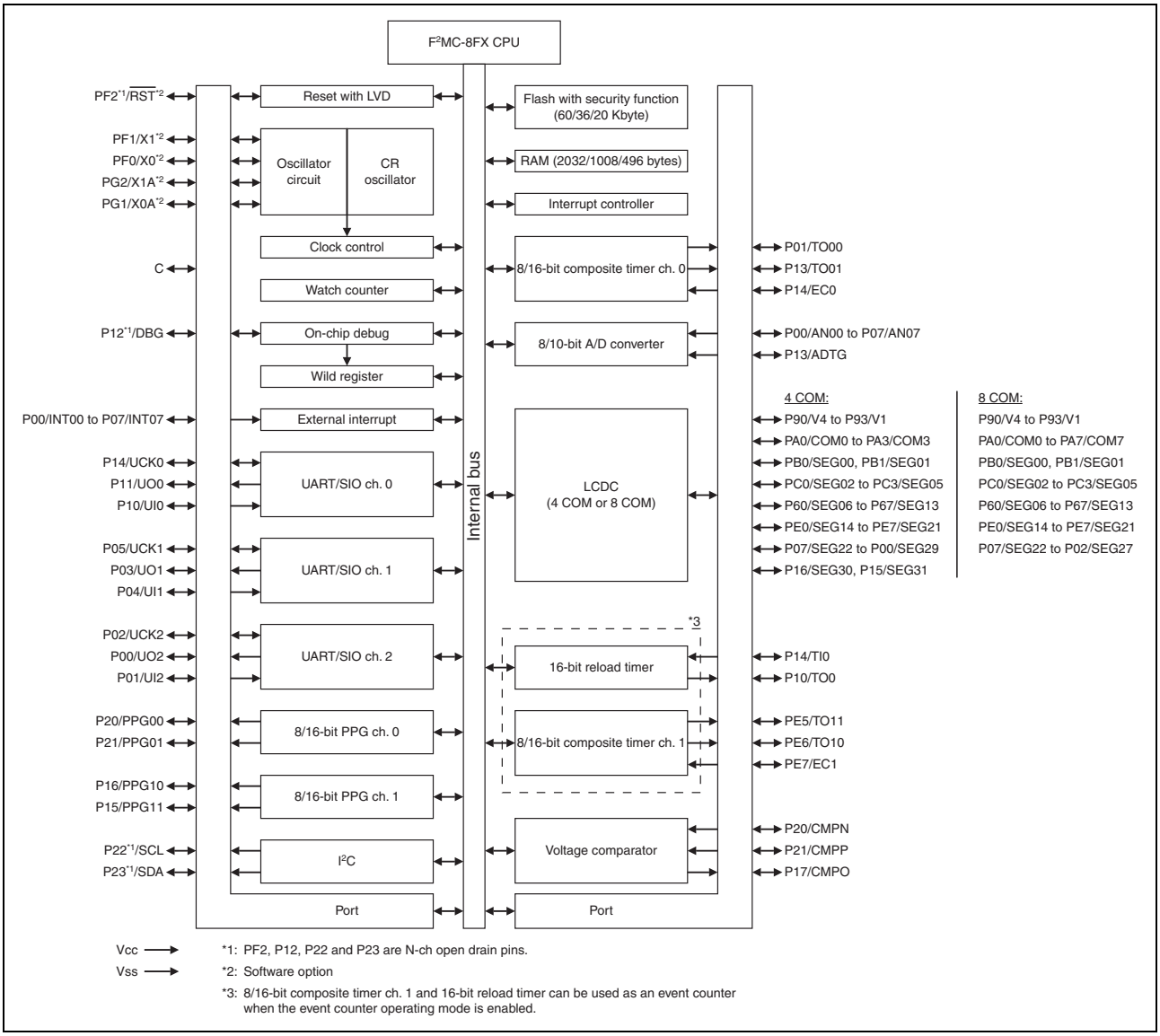
• DBG/$\overline{\text{RST}}$/C pins connection diagram



■ BLOCK DIAGRAM (MB95410H Series)



■ BLOCK DIAGRAM (MB95470H Series)



*1: PF2, P12, P22 and P23 are N-ch open drain pins.

*2: Software option

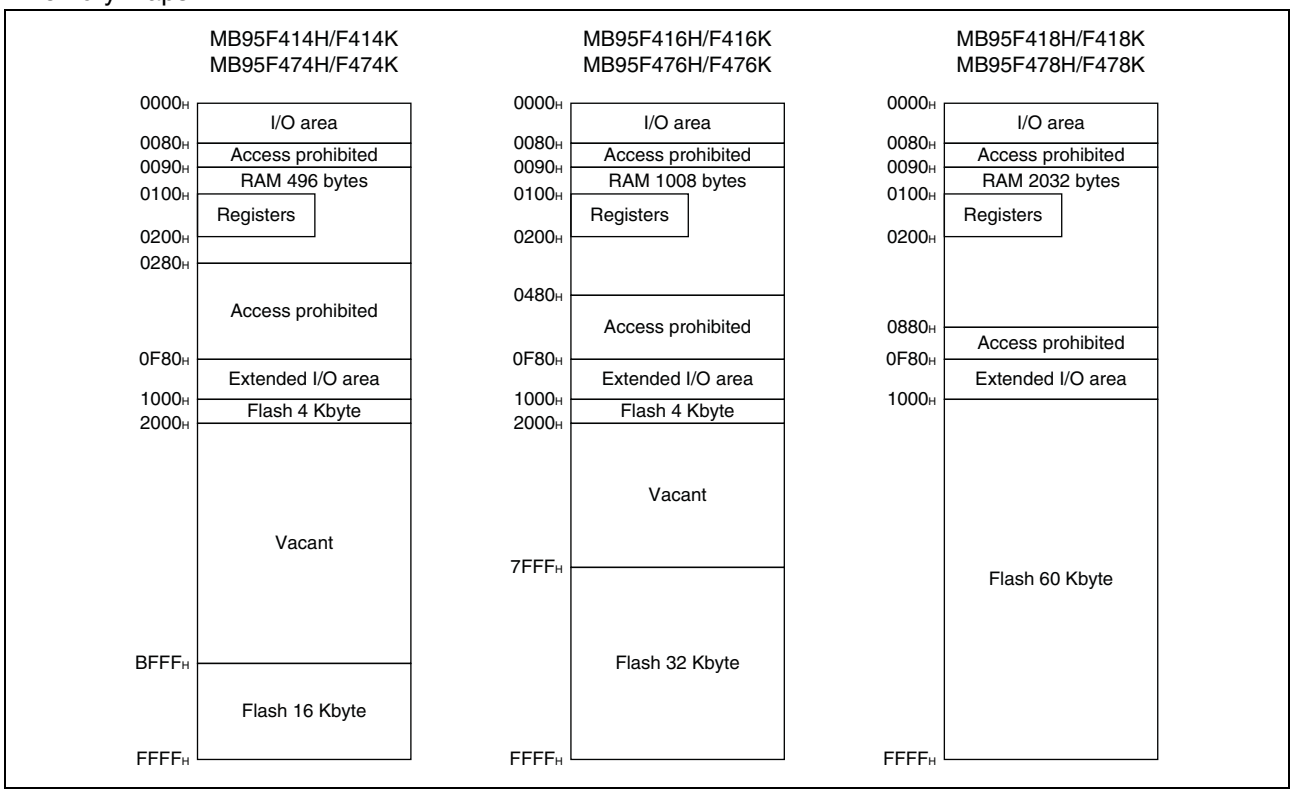
*3: 8/16-bit composite timer ch. 1 and 16-bit reload timer can be used as an event counter when the event counter operating mode is enabled.

■ CPU CORE

• Memory Space

The memory space of the MB95410H/470H Series is 64 Kbyte in size, and consists of an I/O area, a data area, and a program area. The memory space includes areas intended for specific purposes such as general-purpose registers and a vector table. The memory maps of the MB95410H/470H Series are shown below.

• Memory Maps



■ I/O MAP (MB95410H Series)

Address	Register abbreviation	Register name	R/W	Initial value
0000H	PDR0	Port 0 data register	R/W	00000000B
0001H	DDR0	Port 0 direction register	R/W	00000000B
0002H	PDR1	Port 1 data register	R/W	00000000B
0003H	DDR1	Port 1 direction register	R/W	00000000B
0004H	—	(Disabled)	—	—
0005H	WATR	Oscillation stabilization wait time setting register	R/W	11111111B
0006H	PLLC	PLL control register	R/W	00000000B
0007H	SYCC	System clock control register	R/W	XXXXXX11B
0008H	STBC	Standby control register	R/W	00000XXXB
0009H	RSRR	Reset source register	R/W	000XXXXXB
000AH	TBTC	Time-base timer control register	R/W	00000000B
000BH	WPCR	Watch prescaler control register	R/W	00000000B
000CH	WDTC	Watchdog timer control register	R/W	00000000B
000DH	SYCC2	System clock control register 2	R/W	XX100011B
000EH	PDR2	Port 2 data register	R/W	00000000B
000FH	DDR2	Port 2 direction register	R/W	00000000B
0010H, 0011H	—	(Disabled)	—	—
0012H	PDR4	Port 4 data register	R/W	00000000B
0013H	DDR4	Port 4 direction register	R/W	00000000B
0014H	PDR5	Port 5 data register	R/W	00000000B
0015H	DDR5	Port 5 direction register	R/W	00000000B
0016H	PDR6	Port 6 data register	R/W	00000000B
0017H	DDR6	Port 6 direction register	R/W	00000000B
0018H to 001BH	—	(Disabled)	—	—
001CH	PDR9	Port 9 data register	R/W	00000000B
001DH	DDR9	Port 9 direction register	R/W	00000000B
001EH	PDRA	Port A data register	R/W	00000000B
001FH	DDRA	Port A direction register	R/W	00000000B
0020H	PDRB	Port B data register	R/W	00000000B
0021H	DDRB	Port B direction register	R/W	00000000B
0022H	PDRC	Port C data register	R/W	00000000B
0023H	DDRC	Port C direction register	R/W	00000000B
0024H, 0025H	—	(Disabled)	—	—

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
0026H	PDRE	Port E data register	R/W	00000000B
0027H	DDRE	Port E direction register	R/W	00000000B
0028H	PDRF	Port F data register	R/W	00000000B
0029H	DDRF	Port F direction register	R/W	00000000B
002AH	PDRG	Port G data register	R/W	00000000B
002BH	DDRG	Port G direction register	R/W	00000000B
002CH	—	(Disabled)	—	—
002DH	PUL1	Port 1 pull-up register	R/W	00000000B
002EH	PUL2	Port 2 pull-up register	R/W	00000000B
002FH, 0030H	—	(Disabled)	—	—
0031H	PUL5	Port 5 pull-up register	R/W	00000000B
0032H to 0034H	—	(Disabled)	—	—
0035H	PULG	Port G pull-up register	R/W	00000000B
0036H	T01CR1	8/16-bit composite timer 01 status control register 1	R/W	00000000B
0037H	T00CR1	8/16-bit composite timer 00 status control register 1	R/W	00000000B
0038H	T11CR1	8/16-bit composite timer 11 status control register 1	R/W	00000000B
0039H	T10CR1	8/16-bit composite timer 10 status control register 1	R/W	00000000B
003AH	PC01	8/16-bit PPG01 control register	R/W	00000000B
003BH	PC00	8/16-bit PPG00 control register	R/W	00000000B
003CH	PC11	8/16-bit PPG11 control register	R/W	00000000B
003DH	PC10	8/16-bit PPG10 control register	R/W	00000000B
003EH	TMCSRH0	16-bit reload timer control status register upper	R/W	00000000B
003FH	TMCSRL0	16-bit reload timer control status register lower	R/W	00000000B
0040H to 0047H	—	(Disabled)	—	—
0048H	EIC00	External interrupt circuit control register ch. 0/ch. 1	R/W	00000000B
0049H	EIC10	External interrupt circuit control register ch. 2/ch. 3	R/W	00000000B
004AH	EIC20	External interrupt circuit control register ch. 4/ch. 5	R/W	00000000B
004BH	EIC30	External interrupt circuit control register ch. 6/ch. 7	R/W	00000000B
004CH to 004EH	—	(Disabled)	—	—
004FH	LCDCC2	LCDC control register 2	R/W	00010100B
0050H	CMR0	Voltage comparator control register	R/W	000X0001B
0051H to 0055H	—	(Disabled)	—	—

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
0056H	SMC10	UART/SIO serial mode control register 1 ch. 0	R/W	00000000B
0057H	SMC20	UART/SIO serial mode control register 2 ch. 0	R/W	00100000B
0058H	SSR0	UART/SIO serial status register ch. 0	R/W	00000001B
0059H	TDR0	UART/SIO serial output data register ch. 0	R/W	00000000B
005AH	RDR0	UART/SIO serial input data register ch. 0	R	00000000B
005BH	SMC11	UART/SIO serial mode control register 1 ch. 1	R/W	00000000B
005CH	SMC21	UART/SIO serial mode control register 2 ch. 1	R/W	00100000B
005DH	SSR1	UART/SIO serial status register ch. 1	R/W	00000001B
005EH	TDR1	UART/SIO serial output data register ch. 1	R/W	00000000B
005FH	RDR1	UART/SIO serial input data register ch. 1	R	00000000B
0060H	IBCR00	I²C bus control register 0	R/W	00000001B
0061H	IBCR10	I²C bus control register 1	R/W	00000000B
0062H	IBCR0	I²C bus status register	R	00000000B
0063H	IDDR0	I²C data register	R/W	00000000B
0064H	IAAR0	I²C address register	R/W	00000000B
0065H	ICCR0	I²C clock control register	R/W	00000000B
0066H	SMC12	UART/SIO serial mode control register 1 ch. 2	R/W	00000000B
0067H	SMC22	UART/SIO serial mode control register 2 ch. 2	R/W	00100000B
0068H	SSR2	UART/SIO serial status register ch. 2	R/W	00000001B
0069H	TDR2	UART/SIO serial output data register ch. 2	R/W	00000000B
006AH	RDR2	UART/SIO serial input data register ch. 2	R	00000000B
006BH	—	(Disabled)	—	—
006CH	ADC1	8/10-bit A/D converter control register 1	R/W	00000000B
006DH	ADC2	8/10-bit A/D converter control register 2	R/W	00000000B
006EH	ADDH	8/10-bit A/D converter data register upper	R/W	00000000B
006FH	ADDL	8/10-bit A/D converter data register lower	R/W	00000000B
0070H	WCSR	Watch counter status register	R/W	00000000B
0071H	FSR2	Flash memory status register 2	R/W	00000000B
0072H	FSR	Flash memory status register	R/W	000X0000B
0073H	SWRE0	Flash memory sector write control register 0	R/W	00000000B
0074H	FSR3	Flash memory status register 3	R	00000000B
0075H	—	(Disabled)	—	—
0076H	WREN	Wild register address compare enable register	R/W	00000000B
0077H	WROR	Wild register data test setting register	R/W	00000000B
0078H	—	Mirror of register bank pointer (RP) and direct bank pointer (DP)	—	—

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
0079H	ILR0	Interrupt level setting register 0	R/W	11111111B
007AH	ILR1	Interrupt level setting register 1	R/W	11111111B
007BH	ILR2	Interrupt level setting register 2	R/W	11111111B
007CH	ILR3	Interrupt level setting register 3	R/W	11111111B
007DH	ILR4	Interrupt level setting register 4	R/W	11111111B
007EH	ILR5	Interrupt level setting register 5	R/W	11111111B
007FH	—	(Disabled)	—	—
0F80H	WRARH0	Wild register address setting register (upper) ch. 0	R/W	00000000B
0F81H	WRARL0	Wild register address setting register (lower) ch. 0	R/W	00000000B
0F82H	WRDR0	Wild register data setting register ch. 0	R/W	00000000B
0F83H	WRARH1	Wild register address setting register (upper) ch. 1	R/W	00000000B
0F84H	WRARL1	Wild register address setting register (lower) ch. 1	R/W	00000000B
0F85H	WRDR1	Wild register data setting register ch. 1	R/W	00000000B
0F86H	WRARH2	Wild register address setting register (upper) ch. 2	R/W	00000000B
0F87H	WRARL2	Wild register address setting register (lower) ch. 2	R/W	00000000B
0F88H	WRDR2	Wild register data setting register ch. 2	R/W	00000000B
0F89H to 0F91H	—	(Disabled)	—	—
0F92H	T01CR0	8/16-bit composite timer 01 status control register 0	R/W	00000000B
0F93H	T00CR0	8/16-bit composite timer 00 status control register 0	R/W	00000000B
0F94H	T01DR	8/16-bit composite timer 01 data register	R/W	00000000B
0F95H	T00DR	8/16-bit composite timer 00 data register	R/W	00000000B
0F96H	TMCR0	8/16-bit composite timer 00/01 timer mode control register	R/W	00000000B
0F97H	T11CR0	8/16-bit composite timer 11 status control register 0	R/W	00000000B
0F98H	T10CR0	8/16-bit composite timer 10 status control register 0	R/W	00000000B
0F99H	T11DR	8/16-bit composite timer 11 data register	R/W	00000000B
0F9AH	T10DR	8/16-bit composite timer 10 data register	R/W	00000000B
0F9BH	TMCR1	8/16-bit composite timer 10/11 timer mode control register	R/W	00000000B
0F9CH	PPS01	8/16-bit PPG01 cycle setting buffer register	R/W	11111111B
0F9DH	PPS00	8/16-bit PPG00 cycle setting buffer register	R/W	11111111B
0F9EH	PDS01	8/16-bit PPG01 duty setting buffer register	R/W	11111111B
0F9FH	PDS00	8/16-bit PPG00 duty setting buffer register	R/W	11111111B
0FA0H	PPS11	8/16-bit PPG11 cycle setting buffer register	R/W	11111111B
0FA1H	PPS10	8/16-bit PPG10 cycle setting buffer register	R/W	11111111B
0FA2H	PDS11	8/16-bit PPG11 duty setting buffer register	R/W	11111111B
0FA3H	PDS10	8/16-bit PPG10 duty setting buffer register	R/W	11111111B

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
0FA4H	PPGS	8/16-bit PPG start register	R/W	00000000B
0FA5H	REVC	8/16-bit PPG output inversion register	R/W	00000000B
0FA6H	TMRH0	16-bit reload timer timer register upper	R/W	00000000B
	TMRLRH0	16-bit reload timer reload register upper	R/W	00000000B
0FA7H	TMRL0	16-bit reload timer timer register lower	R/W	00000000B
	TMRLRL0	16-bit reload timer reload register lower	R/W	00000000B
0FA8H	PSSR0	UART/SIO dedicated baud rate generator prescaler select register ch. 0	R/W	00000000B
0FA9H	BRSR0	UART/SIO dedicated baud rate generator baud rate setting register ch. 0	R/W	00000000B
0FAAH	PSSR1	UART/SIO dedicated baud rate generator prescaler select register ch. 1	R/W	00000000B
0FABH	BRSR1	UART/SIO dedicated baud rate generator baud rate setting register ch. 1	R/W	00000000B
0FACH	PSSR2	UART/SIO dedicated baud rate generator prescaler select register ch. 2	R/W	00000000B
0FADH	BRSR2	UART/SIO dedicated baud rate generator baud rate setting register ch. 2	R/W	00000000B
0FAEH	—	(Disabled)	—	—
0FAFH	AIDRL	A/D input disable register (lower)	R/W	00000000B
0FB0H	LCDCC1	LCDC control register 1	R/W	00000000B
0FB1H	—	(Disabled)	—	—
0FB2H	LCDCE1	LCDC enable register 1	R/W	00111110B
0FB3H	LCDCE2	LCDC enable register 2	R/W	00000000B
0FB4H	LCDCE3	LCDC enable register 3	R/W	00000000B
0FB5H	LCDCE4	LCDC enable register 4	R/W	00000000B
0FB6H	LCDCE5	LCDC enable register 5	R/W	00000000B
0FB7H	LCDCE6	LCDC enable register 6	R/W	00000000B
0FB8H	LCDCE7	LCDC enable register 7	R/W	00000000B
0FB9H	LCDCB1	LCDC blinking setting register 1	R/W	00000000B
0FBAH	LCDCB2	LCDC blinking setting register 2	R/W	00000000B
0FBBH, 0FBCH	—	(Disabled)	—	—
0FBDH to 0FE0H	LCDRAM	LCDC display RAM (36 bytes)	R/W	00000000B
0FE1H	—	(Disabled)	—	—
0FE2H	EVCR	Event counter control register	R/W	00000000B
0FE3H	WCDR	Watch counter data register	R/W	00111111B

(Continued)

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
0FE4H	CRTH	Main CR clock trimming register (upper)	R/W	0XXXXXXXB
0FE5H	CRTL	Main CR clock trimming register (lower)	R/W	00XXXXXXB
0FE6H, 0FE7H	—	(Disabled)	—	—
0FE8H	SYSC	System configuration register	R/W	11000011B
0FE9H	CMCR	Clock monitoring control register	R/W	XX000000B
0FEAH	CMDR	Clock monitoring data register	R	00000000B
0FEBH	WDTH	Watchdog timer selection ID register (upper)	R	XXXXXXXXB
0FECH	WDTL	Watchdog timer selection ID register (lower)	R	XXXXXXXXB
0FEDH	—	(Disabled)	—	—
0FEEH	ILSR	Input level select register	R/W	00000000B
0FEFH	WICR	Interrupt pin control register	R/W	01000000B
0FF0H to 0FFFH	—	(Disabled)	—	—

• R/W access symbols
  R/W : Readable / Writable
  R : Read only

• Initial value symbols
  0 : The initial value of this bit is “0”.
  1 : The initial value of this bit is “1”.
  X : The initial value of this bit is indeterminate.

Note: Do not write to an address that is “(Disabled)”. If a “(Disabled)” address is read, an indeterminate value is returned.

■ I/O MAP (MB95470H Series)

Address	Register abbreviation	Register name	R/W	Initial value
0000H	PDR0	Port 0 data register	R/W	00000000B
0001H	DDR0	Port 0 direction register	R/W	00000000B
0002H	PDR1	Port 1 data register	R/W	00000000B
0003H	DDR1	Port 1 direction register	R/W	00000000B
0004H	—	(Disabled)	—	—
0005H	WATR	Oscillation stabilization wait time setting register	R/W	11111111B
0006H	PLLC	PLL control register	R/W	00000000B
0007H	SYCC	System clock control register	R/W	XXXXXX11B
0008H	STBC	Standby control register	R/W	00000XXXB
0009H	RSRR	Reset source register	R/W	000XXXXXB
000AH	TBTC	Time-base timer control register	R/W	00000000B
000BH	WPCR	Watch prescaler control register	R/W	00000000B
000CH	WDTC	Watchdog timer control register	R/W	00000000B
000DH	SYCC2	System clock control register 2	R/W	XX100011B
000EH	PDR2	Port 2 data register	R/W	00000000B
000FH	DDR2	Port 2 direction register	R/W	00000000B
0010H to 0015H	—	(Disabled)	—	—
0016H	PDR6	Port 6 data register	R/W	00000000B
0017H	DDR6	Port 6 direction register	R/W	00000000B
0018H to 001BH	—	(Disabled)	—	—
001CH	PDR9	Port 9 data register	R/W	00000000B
001DH	DDR9	Port 9 direction register	R/W	00000000B
001EH	PDRA	Port A data register	R/W	00000000B
001FH	DDRA	Port A direction register	R/W	00000000B
0020H	PDRB	Port B data register	R/W	00000000B
0021H	DDRB	Port B direction register	R/W	00000000B
0022H	PDRC	Port C data register	R/W	00000000B
0023H	DDRC	Port C direction register	R/W	00000000B
0024H, 0025H	—	(Disabled)	—	—
0026H	PDRE	Port E data register	R/W	00000000B
0027H	DDRE	Port E direction register	R/W	00000000B
0028H	PDRF	Port F data register	R/W	00000000B
0029H	DDRF	Port F direction register	R/W	00000000B
002AH	PDRG	Port G data register	R/W	00000000B
002BH	DDRG	Port G direction register	R/W	00000000B
002CH	—	(Disabled)	—	—

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
002D$_H$	PUL1	Port 1 pull-up register	R/W	00000000$_B$
002E$_H$	PUL2	Port 2 pull-up register	R/W	00000000$_B$
002F$_H$ to 0034$_H$	—	(Disabled)	—	—
0035$_H$	PULG	Port G pull-up register	R/W	00000000$_B$
0036$_H$	T01CR1	8/16-bit composite timer 01 status control register 1	R/W	00000000$_B$
0037$_H$	T00CR1	8/16-bit composite timer 00 status control register 1	R/W	00000000$_B$
0038$_H$	T11CR1	8/16-bit composite timer 11 status control register 1	R/W	00000000$_B$
0039$_H$	T10CR1	8/16-bit composite timer 10 status control register 1	R/W	00000000$_B$
003A$_H$	PC01	8/16-bit PPG01 control register	R/W	00000000$_B$
003B$_H$	PC00	8/16-bit PPG00 control register	R/W	00000000$_B$
003C$_H$	PC11	8/16-bit PPG11 control register	R/W	00000000$_B$
003D$_H$	PC10	8/16-bit PPG10 control register	R/W	00000000$_B$
003E$_H$	TMCSRH0	16-bit reload timer control status register upper	R/W	00000000$_B$
003F$_H$	TMCSRL0	16-bit reload timer control status register lower	R/W	00000000$_B$
0040$_H$ to 0047$_H$	—	(Disabled)	—	—
0048$_H$	EIC00	External interrupt circuit control register ch. 0/ch. 1	R/W	00000000$_B$
0049$_H$	EIC10	External interrupt circuit control register ch. 2/ch. 3	R/W	00000000$_B$
004A$_H$	EIC20	External interrupt circuit control register ch. 4/ch. 5	R/W	00000000$_B$
004B$_H$	EIC30	External interrupt circuit control register ch. 6/ch. 7	R/W	00000000$_B$
004C$_H$ to 004E$_H$	—	(Disabled)	—	—
004F$_H$	LCDCC2	LCDC control register 2	R/W	00010100$_B$
0050$_H$	CMR0	Voltage comparator control register	R/W	000X0001$_B$
0051$_H$ to 0055$_H$	—	(Disabled)	—	—
0056$_H$	SMC10	UART/SIO serial mode control register 1 ch. 0	R/W	00000000$_B$
0057$_H$	SMC20	UART/SIO serial mode control register 2 ch. 0	R/W	00100000$_B$
0058$_H$	SSR0	UART/SIO serial status register ch. 0	R/W	00000001$_B$
0059$_H$	TDR0	UART/SIO serial output data register ch. 0	R/W	00000000$_B$
005A$_H$	RDR0	UART/SIO serial input data register ch. 0	R	00000000$_B$
005B$_H$	SMC11	UART/SIO serial mode control register 1 ch. 1	R/W	00000000$_B$
005C$_H$	SMC21	UART/SIO serial mode control register 2 ch. 1	R/W	00100000$_B$
005D$_H$	SSR1	UART/SIO serial status register ch. 1	R/W	00000001$_B$
005E$_H$	TDR1	UART/SIO serial output data register ch. 1	R/W	00000000$_B$

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
005F$_H$	RDR1	UART/SIO serial input data register ch. 1	R	00000000$_B$
0060$_H$	IBCR00	I^{2}C bus control register 0	R/W	00000001$_B$
0061$_H$	IBCR10	I^{2}C bus control register 1	R/W	00000000$_B$
0062$_H$	IBCR0	I^{2}C bus status register	R	00000000$_B$
0063$_H$	IDDR0	I^{2}C data register	R/W	00000000$_B$
0064$_H$	IAAR0	I^{2}C address register	R/W	00000000$_B$
0065$_H$	ICCR0	I^{2}C clock control register	R/W	00000000$_B$
0066$_H$	SMC12	UART/SIO serial mode control register 1 ch. 2	R/W	00000000$_B$
0067$_H$	SMC22	UART/SIO serial mode control register 2 ch. 2	R/W	00100000$_B$
0068$_H$	SSR2	UART/SIO serial status register ch. 2	R/W	00000001$_B$
0069$_H$	TDR2	UART/SIO serial output data register ch. 2	R/W	00000000$_B$
006A$_H$	RDR2	UART/SIO serial input data register ch. 2	R	00000000$_B$
006B$_H$	—	(Disabled)	—	—
006C$_H$	ADC1	8/10-bit A/D converter control register 1	R/W	00000000$_B$
006D$_H$	ADC2	8/10-bit A/D converter control register 2	R/W	00000000$_B$
006E$_H$	ADDH	8/10-bit A/D converter data register upper	R/W	00000000$_B$
006F$_H$	ADDL	8/10-bit A/D converter data register lower	R/W	00000000$_B$
0070$_H$	WCSR	Watch counter status register	R/W	00000000$_B$
0071$_H$	FSR2	Flash memory status register 2	R/W	00000000$_B$
0072$_H$	FSR	Flash memory status register	R/W	000X0000$_B$
0073$_H$	SWRE0	Flash memory sector write control register 0	R/W	00000000$_B$
0074$_H$	FSR3	Flash memory status register 3	R	00000000$_B$
0075$_H$	—	(Disabled)	—	—
0076$_H$	WREN	Wild register address compare enable register	R/W	00000000$_B$
0077$_H$	WROR	Wild register data test setting register	R/W	00000000$_B$
0078$_H$	—	Mirror of register bank pointer (RP) and direct bank pointer (DP)	—	—
0079$_H$	ILR0	Interrupt level setting register 0	R/W	11111111$_B$
007A$_H$	ILR1	Interrupt level setting register 1	R/W	11111111$_B$
007B$_H$	ILR2	Interrupt level setting register 2	R/W	11111111$_B$
007C$_H$	ILR3	Interrupt level setting register 3	R/W	11111111$_B$
007D$_H$	ILR4	Interrupt level setting register 4	R/W	11111111$_B$
007E$_H$	ILR5	Interrupt level setting register 5	R/W	11111111$_B$
007F$_H$	—	(Disabled)	—	—
0F80$_H$	WRARH0	Wild register address setting register (upper) ch. 0	R/W	00000000$_B$
0F81$_H$	WRARL0	Wild register address setting register (lower) ch. 0	R/W	00000000$_B$
0F82$_H$	WRDR0	Wild register data setting register ch. 0	R/W	00000000$_B$

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
0F83H	WRARH1	Wild register address setting register (upper) ch. 1	R/W	00000000B
0F84H	WRARL1	Wild register address setting register (lower) ch. 1	R/W	00000000B
0F85H	WRDR1	Wild register data setting register ch. 1	R/W	00000000B
0F86H	WRARH2	Wild register address setting register (upper) ch. 2	R/W	00000000B
0F87H	WRARL2	Wild register address setting register (lower) ch. 2	R/W	00000000B
0F88H	WRDR2	Wild register data setting register ch. 2	R/W	00000000B
0F89H to 0F91H	—	(Disabled)	—	—
0F92H	T01CR0	8/16-bit composite timer 01 status control register 0	R/W	00000000B
0F93H	T00CR0	8/16-bit composite timer 00 status control register 0	R/W	00000000B
0F94H	T01DR	8/16-bit composite timer 01 data register	R/W	00000000B
0F95H	T00DR	8/16-bit composite timer 00 data register	R/W	00000000B
0F96H	TMCR0	8/16-bit composite timer 00/01 timer mode control register	R/W	00000000B
0F97H	T11CR0	8/16-bit composite timer 11 status control register 0	R/W	00000000B
0F98H	T10CR0	8/16-bit composite timer 10 status control register 0	R/W	00000000B
0F99H	T11DR	8/16-bit composite timer 11 data register	R/W	00000000B
0F9AH	T10DR	8/16-bit composite timer 10 data register	R/W	00000000B
0F9BH	TMCR1	8/16-bit composite timer 10/11 timer mode control register	R/W	00000000B
0F9CH	PPS01	8/16-bit PPG01 cycle setting buffer register	R/W	11111111B
0F9DH	PPS00	8/16-bit PPG00 cycle setting buffer register	R/W	11111111B
0F9EH	PDS01	8/16-bit PPG01 duty setting buffer register	R/W	11111111B
0F9FH	PDS00	8/16-bit PPG00 duty setting buffer register	R/W	11111111B
0FA0H	PPS11	8/16-bit PPG11 cycle setting buffer register	R/W	11111111B
0FA1H	PPS10	8/16-bit PPG10 cycle setting buffer register	R/W	11111111B
0FA2H	PDS11	8/16-bit PPG11 duty setting buffer register	R/W	11111111B
0FA3H	PDS10	8/16-bit PPG10 duty setting buffer register	R/W	11111111B
0FA4H	PPGS	8/16-bit PPG start register	R/W	00000000B
0FA5H	REVC	8/16-bit PPG output inversion register	R/W	00000000B
0FA6H	TMRH0	16-bit reload timer timer register upper	R/W	00000000B
	TMRLRH0	16-bit reload timer reload register upper	R/W	00000000B
0FA7H	TMRL0	16-bit reload timer timer register lower	R/W	00000000B
	TMRLRL0	16-bit reload timer reload register lower	R/W	00000000B
0FA8H	PSSR0	UART/SIO dedicated baud rate generator prescaler select register ch. 0	R/W	00000000B
0FA9H	BRSR0	UART/SIO dedicated baud rate generator baud rate setting register ch. 0	R/W	00000000B
0FAAH	PSSR1	UART/SIO dedicated baud rate generator prescaler select register ch. 1	R/W	00000000B
0FABH	BRSR1	UART/SIO dedicated baud rate generator baud rate setting register ch. 1	R/W	00000000B

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
0FAC$_H$	PSSR2	UART/SIO dedicated baud rate generator prescaler select register ch. 2	R/W	00000000$_B$
0FAD$_H$	BRSR2	UART/SIO dedicated baud rate generator baud rate setting register ch. 2	R/W	00000000$_B$
0FAE$_H$	—	(Disabled)	—	—
0FAF$_H$	AIDRL	A/D input disable register (lower)	R/W	00000000$_B$
0FB0$_H$	LCDCC1	LCDC control register 1	R/W	00000000$_B$
0FB1$_H$	—	(Disabled)	—	—
0FB2$_H$	LCDCE1	LCDC enable register 1	R/W	00111100$_B$
0FB3$_H$	LCDCE2	LCDC enable register 2	R/W	00000000$_B$
0FB4$_H$	LCDCE3	LCDC enable register 3	R/W	00000000$_B$
0FB5$_H$	LCDCE4	LCDC enable register 4	R/W	00000000$_B$
0FB6$_H$	LCDCE5	LCDC enable register 5	R/W	00000000$_B$
0FB7$_H$	LCDCE6	LCDC enable register 6	R/W	00000000$_B$
0FB8$_H$	—	(Disabled)	—	—
0FB9$_H$	LCDCB1	LCDC blinking setting register 1	R/W	00000000$_B$
0FBA$_H$	LCDCB2	LCDC blinking setting register 2	R/W	00000000$_B$
0FBB$_H$, 0FBC$_H$	—	(Disabled)	—	—
0FBD$_H$ to 0FD8$_H$	LCDRAM	LCDC display RAM (28 bytes)	R/W	00000000$_B$
0FD9$_H$ to 0FE1$_H$	—	(Disabled)	—	—
0FE2$_H$	EVCR	Event counter control register	R/W	00000000$_B$
0FE3$_H$	WCDR	Watch counter data register	R/W	00111111$_B$
0FE4$_H$	CRTH	Main CR clock trimming register (upper)	R/W	0XXXXXXX$_B$
0FE5$_H$	CRTL	Main CR clock trimming register (lower)	R/W	00XXXXXX$_B$
0FE6$_H$, 0FE7$_H$	—	(Disabled)	—	—
0FE8$_H$	SYSC	System configuration register	R/W	11000011$_B$
0FE9$_H$	CMCR	Clock monitoring control register	R/W	XX000000$_B$
0FEA$_H$	CMDR	Clock monitoring data register	R	00000000$_B$
0FEB$_H$	WDTH	Watchdog timer selection ID register (upper)	R	XXXXXXXX$_B$
0FEC$_H$	WDTL	Watchdog timer selection ID register (lower)	R	XXXXXXXX$_B$

(Continued)

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
0FED$_H$	—	(Disabled)	—	—
0FEE$_H$	ILSR	Input level select register	R/W	00000000$_B$
0FEF$_H$	WICR	Interrupt pin control register	R/W	01000000$_B$
0FF0$_H$ to 0FFF$_H$	—	(Disabled)	—	—

• R/W access symbols
  R/W : Readable / Writable
  R : Read only

• Initial value symbols
  0 : The initial value of this bit is “0”.
  1 : The initial value of this bit is “1”.
  X : The initial value of this bit is indeterminate.

Note: Do not write to an address that is “(Disabled)”. If a “(Disabled)” address is read, an indeterminate value is returned.

■ INTERRUPT SOURCE TABLE

Interrupt source	Interrupt request number	Vector table address		Bit name of interrupt level setting register	Priority order of interrupt sources of the same level (occurring simultaneously)
		Upper	Lower		
External interrupt ch. 0	IRQ00	FFFA$_H$	FFFB$_H$	L00 [1:0]	High
External interrupt ch. 4					
External interrupt ch. 1	IRQ01	FFF8$_H$	FFF9$_H$	L01 [1:0]	
External interrupt ch. 5					
External interrupt ch. 2	IRQ02	FFF6$_H$	FFF7$_H$	L02 [1:0]	
External interrupt ch. 6					
External interrupt ch. 3	IRQ03	FFF4$_H$	FFF5$_H$	L03 [1:0]	
External interrupt ch. 7					
UART/SIO ch. 0	IRQ04	FFF2$_H$	FFF3$_H$	L04 [1:0]	
8/16-bit composite timer ch. 0 (lower)	IRQ05	FFF0$_H$	FFF1$_H$	L05 [1:0]	
8/16-bit composite timer ch. 0 (upper)	IRQ06	FFEE$_H$	FFEF$_H$	L06 [1:0]	
UART/SIO ch. 2	IRQ07	FFEC$_H$	FFED$_H$	L07 [1:0]	
LCD controller	IRQ08	FFEA$_H$	FFEB$_H$	L08 [1:0]	
8/16-bit PPG ch. 1 (lower)	IRQ09	FFE8$_H$	FFE9$_H$	L09 [1:0]	
UART/SIO ch. 1					
8/16-bit PPG ch. 1 (upper)	IRQ10	FFE6$_H$	FFE7$_H$	L10 [1:0]	
16-bit reload timer ch. 0	IRQ11	FFE4$_H$	FFE5$_H$	L11 [1:0]	
8/16-bit PPG ch. 0 (upper)	IRQ12	FFE2$_H$	FFE3$_H$	L12 [1:0]	
8/16-bit PPG ch. 0 (lower)	IRQ13	FFE0$_H$	FFE1$_H$	L13 [1:0]	
8/16-bit composite timer ch. 1 (upper)	IRQ14	FFDE$_H$	FFDF$_H$	L14 [1:0]	
Voltage comparator	IRQ15	FFDC$_H$	FFDD$_H$	L15 [1:0]	
I^{2}C	IRQ16	FFDA$_H$	FFDB$_H$	L16 [1:0]	
—	IRQ17	FFD8$_H$	FFD9$_H$	L17 [1:0]	
8/10-bit A/D converter	IRQ18	FFD6$_H$	FFD7$_H$	L18 [1:0]	
Time-base timer	IRQ19	FFD4$_H$	FFD5$_H$	L19 [1:0]	
Watch prescaler	IRQ20	FFD2$_H$	FFD3$_H$	L20 [1:0]	
Watch counter					
—	IRQ21	FFD0$_H$	FFD1$_H$	L21 [1:0]	
8/16-bit composite timer ch. 1 (lower)	IRQ22	FFCE$_H$	FFCF$_H$	L22 [1:0]	
Flash memory	IRQ23	FFCC$_H$	FFCD$_H$	L23 [1:0]	Low

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V_{CC}	V_{SS} – 0.3	V_{SS} + 6	V	
Input voltage*1	V_I	V_{SS} – 0.3	V_{SS} + 6	V	*2
Output voltage*1	V_O	V_{SS} – 0.3	V_{SS} + 6	V	*2
Maximum clamp current	I_{CLAMP}	–2	+2	mA	Applicable to specific pins*3
Total maximum clamp current	$\Sigma\lvert I_{CLAMP}\rvert$	—	20	mA	Applicable to specific pins*3
“L” level maximum output current	I_{CL}	—	15	mA	
“L” level average current	I_{CLAV}	—	4	mA	Average output current = operating current × operating ratio (1 pin)
“L” level total maximum output current	ΣI_{OL}	—	100	mA	
“L” level total average output current	ΣI_{OLAV}	—	50	mA	Total average output current = operating current × operating ratio (Total number of pins)
“H” level maximum output current	I_{CH}	—	–15	mA	
“H” level average current	I_{CHAV}	—	–4	mA	Average output current = operating current × operating ratio (1 pin)
“H” level total maximum output current	ΣI_{OH}	—	–100	mA	
“H” level total average output current	ΣI_{OHAV}	—	–50	mA	Total average output current = operating current × operating ratio (Total number of pins)
Power consumption	P_d	—	320	mW	
Operating temperature	T_A	–40	+85	°C	
Storage temperature	T_{stg}	–55	+150	°C	

*1: These parameters are based on the condition that V_{SS} = 0.0 V.

*2: V_I and V_O must not exceed V_{CC} + 0.3 V. V_I must not exceed the rated voltage. However, if the maximum current to/from an input is limited by means of an external component, the I_{CLAMP} rating is used instead of the V_I rating.

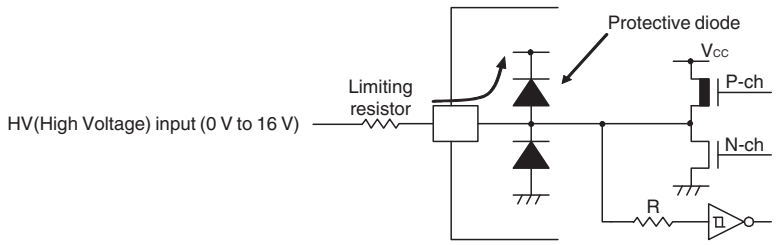
(Continued)

(Continued)

*3: Applicable to the following pins: P00 to P07, P10, P11, P13 to P16, P20 to P22, P40 to P43, P50 to P53, P60 to P67, P90 to P94, PA0 to PA7, PB0 to PB4, PC0 to PC7, PE0 to PE7, PF0, PF1, PG1 and PG2 (P40 to P43, P50 to P53, P94, PB2 to PB4 and PC4 to PC7 are only available on the MB95410H Series.)

- Use under recommended operating conditions.
- Use with DC voltage (current).
- The HV (High Voltage) signal is an input signal exceeding the V_{CC} voltage. Always connect a limiting resistor between the HV (High Voltage) signal and the microcontroller before applying the HV (High Voltage) signal.
- The value of the limiting resistance should be set so that when the HV (High Voltage) signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- When the microcontroller drive current is low, such as in low power consumption modes, the HV (High Voltage) input potential may pass through the protective diode to increase the potential of the V_{CC} pin, and thus affects other devices.
- If the HV (High Voltage) signal is input when the microcontroller power supply is off (not fixed at 0 V), since power is supplied from the pins, incomplete operations may be executed.
- If the HV (High Voltage) input is input after power-on, since power is supplied from the pins, the voltage of power supply may not be sufficient to enable a power-on reset.
- Do not leave the HV (High Voltage) input pin unconnected.
- Example of a recommended circuit

- Input/Output equivalent circuit



WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

(V_{SS} = 0.0 V)

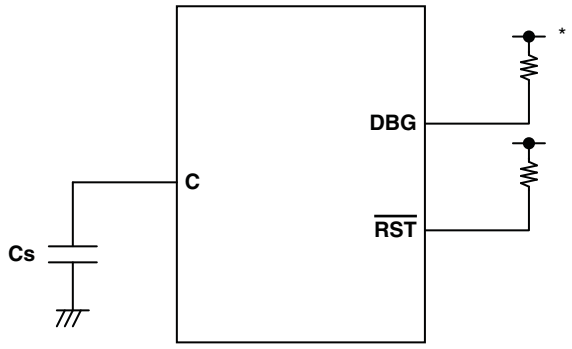
Parameter	Symbol	Value		Unit	Remarks	
		Min	Max			
Power supply voltage	V_{CC}, AV_{CC}	2.4*1*2	5.5*1	V	In normal operation	Other than on-chip debug mode
		2.3	5.5		Hold condition in stop mode	
		2.9	5.5		In normal operation	On-chip debug mode
		2.3	5.5		Hold condition in stop mode	
Smoothing capacitor	C_S	0.022	1	µF	*3	
Operating temperature	T_A	−40	+85	°C	Other than on-chip debug mode	
		+5	+35		On-chip debug mode	

*1: The value varies depending on the operating frequency, the machine clock and the analog guaranteed range.

*2: The value is initially 2.88 V when the low-voltage detection reset is used.

*3: Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. The bypass capacitor for the V_{CC} pin must have a capacitance larger than C_S. For the connection to a smoothing capacitor C_S, see the diagram below. To prevent the device from unintentionally entering an unknown mode due to noise, minimize the distance between the C pin and C_S and the distance between C_S and the V_{SS} pin when designing the layout of a printed circuit board.

• DBG / $\overline{RST}$ / C pins connection diagram



*: Since the DBG pin becomes a communication pin in on-chip debug mode, set a pull-up resistor value suiting the input/output specifications of P12/DBG.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

3. DC Characteristics

(V_{CC} = 5.0 V ±10%, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IHI}	P01, P04, P10, P22, P23	*1	0.7 V_{CC}	—	V_{CC} + 0.3	V	When CMOS input level (hysteresis input) is selected
	V_{IHS}	P00 to P07, P10 to P17, P20 to P23, P40 to P43*2, P50 to P53*2, P60 to P67, P90 to P93, P94*2, PA0 to PA7, PB0, PB1, PB2 to PB4*2, PC0 to PC3, PC4 to PC7*2, PE0 to PE7, PF0, PF1, PG1, PG2	*1	0.8 V_{CC}	—	V_{CC} + 0.3	V	Hysteresis input
	V_{IHM}	PF2	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	Hysteresis input
"L" level input voltage	V_{IL}	P01, P04, P10, P22, P23	*1	V_{SS} – 0.3	—	0.3 V_{CC}	V	When CMOS input level (hysteresis input) is selected
	V_{ILS}	P00 to P07, P10 to P17, P20 to P23, P40 to P43*2, P50 to P53*2, P60 to P67, P90 to P93, P94*2, PA0 to PA7, PB0, PB1, PB2 to PB4*2, PC0 to PC3, PC4 to PC7*2, PE0 to PE7, PF0, PF1, PG1, PG2	*1	V_{SS} – 0.3	—	0.2 V_{CC}	V	Hysteresis input
	V_{ILM}	PF2	—	V_{SS} – 0.3	—	0.3 V_{CC}	V	Hysteresis input
Open-drain output application voltage	V_D	P12, P22, P23, PF2	—	V_{SS} – 0.3	—	V_{SS} + 5.5	V	
"H" level output voltage	V_{OH1}	Output pins other than P12, P22, P23, PF2	I_{OH} = –4 mA	V_{CC} – 0.5	—	—	V	

(Continued)

(V_{CC} = 5.0 V ±10%, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ*4	Max		
"L" level output voltage	V_{OL1}	All output pins	I_{OL} = 4 mA	—	—	0.4	V	
Input leak current (Hi-Z output leak current)	I_{LI}	All input pins	0.0 V < V_I < V_{CC}	–5	—	+5	µA	When pull-up resistance is disabled
Pull-up resistance	R_{PULL}	P10, P11, P13, P14, P17, P20, P21, P50 to P53*2, PG1, PG2	V_I = 0 V	25	50	100	kΩ	When pull-up resistance is enabled
Input capacitance	C_{IN}	Other than V_{CC} and V_{SS}	f = 1 MHz	—	5	15	pF	
Power supply current*3	I_{CC}	V_{CC} (External clock operation)	V_{CC} = 5.5 V F_{CH} = 32 MHz F_{MP} = 16 MHz Main clock mode (divided by 2)	—	14.1	17	mA	Except during Flash memory programming and erasing
				—	20	39.5	mA	During Flash memory programming and erasing
	I_{CCS}		V_{CC} = 5.5 V F_{CH} = 32 MHz F_{MP} = 16 MHz Main sleep mode (divided by 2)	—	6.6	9	mA	
	I_{CCL}		V_{CC} = 5.5 V F_{CL} = 32 kHz F_{MPL} = 16 kHz Subclock mode (divided by 2) T_A = +25°C	—	60	153	µA	
	I_{CCLS}		V_{CC} = 5.5 V F_{CL} = 32 kHz F_{MPL} = 16 kHz Subsleep mode (divided by 2) T_A = +25°C	—	9	84	µA	
	I_{CCT}		V_{CC} = 5.5 V F_{CL} = 32 kHz Watch mode Main stop mode T_A = +25°C	—	4.3	30	µA	

(Continued)

(V_{CC} = 5.0 V ±10%, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ*4	Max		
Power supply current*3	I_{CCMPLL}	V_{CC} (External clock operation)	V_{CC} = 5.5 V F_{CH} = 4 MHz F_{MP} = 10 MHz Main PLL mode (multiplied by 2.5) T_A = +25°C	—	9.7	12.5	mA	
			V_{CC} = 5.5 V F_{CH} = 6.44 MHz F_{MP} = 16 MHz Main PLL mode (multiplied by 2.5) T_A = +25°C	—	13.9	20	mA	
	I_{CCMCR}	V_{CC}	V_{CC} = 5.5 V F_{CRH} = 12.5 MHz F_{MP} = 12.5 MHz Main CR clock mode	—	11	13.2	mA	
	I_{CCSCR}		V_{CC} = 5.5 V Sub-CR clock mode (multiplied by 2.5) T_A = +25°C	—	112	410	µA	
	I_{CCTS}	V_{CC} (External clock operation)	V_{CC} = 5.5 V F_{CH} = 32 MHz Time-base timer mode T_A = +25°C	—	1	3	mA	
	I_{CCH}		V_{CC} = 5.5 V Substop mode T_A = +25°C	—	3.1	22.5	µA	Main stop mode with one clock selected
	I_A	AV_{CC}	Current consumption for A/D conversion at 16 MHz	—	1.5	4.7	mA	
	I_{AH}		Current consumption for stopping A/D conversion at 16 MHz	—	1	5	µA	
	I_V		Current consumption of voltage comparator at 16 MHz	—	113	350	µA	

(Continued)

(Continued)

(V_{CC} = 5.0 V ±10%, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ*4	Max		
Power supply current*3	I_{LVD}	V_{CC}	Current consumption of the low-voltage detection circuit	—	31	54	µA	
	I_{CRH}		Current consumption of the main CR oscillator	—	0.5	0.6	mA	
	I_{CRL}		Current consumption of the sub-CR oscillator oscillating at 100 kHz	—	20	72	µA	
LCD internal division resistance	R_{LCD}	—	Between V4 and V_{SS}	—	400	—	kΩ	
				—	40	—	kΩ	
COM0 to COM7 output impedance	R_{VCOM}	COM0 to COM7	V1 to V4 = 4.1 V	—	—	5	kΩ	
SEG00 to SEG39 output impedance	R_{VSEG}	SEG00 to SEG39		—	—	7	kΩ	
LCD leakage current	I_{LCDL}	V0 to V4, COM0 to COM7, SEG00 to SEG39	—	–1	—	+1	µA	

*1: The input levels of P01, P04, P10, P22 and P23 can be switched between “CMOS input level” and “hysteresis input level”. The input level selection register (ILSR) is used to switch between the two input levels.

*2: P40 to P43, P50 to P53, P94, PB2 to PB4 and PC4 to PC7 are only available on the MB95410H Series.

*3:
- The power supply current is determined by the external clock. When the low-voltage detection option is selected, the power-supply current will be the sum of adding the current consumption of the low-voltage detection circuit (I_{LVD}) to one of the value from I_{CC} to I_{CCH}. In addition, when both the low-voltage detection option and the CR oscillator are selected, the power supply current will be the sum of adding up the current consumption of the low-voltage detection circuit, the current consumption of the CR oscillators (I_{CRH}, I_{CRL}) and a specified value. In on-chip debug mode, the CR oscillator (I_{CRH}) and the low-voltage detection circuit are always enabled, and current consumption therefore increases accordingly.
- See "4. AC Characteristics: (1) Clock Timing" for F_{CH} and F_{CL}.
- See "4. AC Characteristics: (2) Source Clock/Machine Clock" for F_{MP} and F_{MPL}.

*4: V_{CC} = 5.0 V, T_A = +25°C

4. AC Characteristics

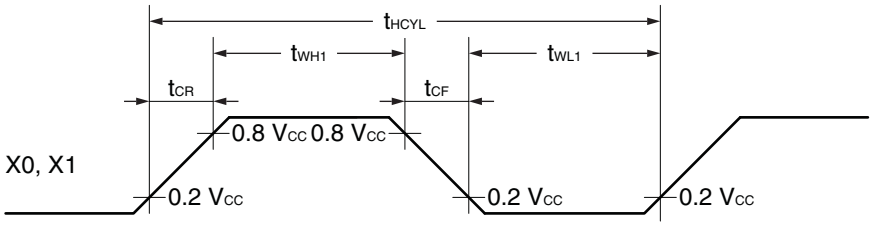
(1) Clock Timing

(V_{CC} = 2.4 V to 5.5 V, V_{SS} = 0.0 V, T_A = −40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Clock frequency	F_{CH}	X0, X1	—	1	—	16.25	MHz	When the main oscillation circuit is used
		X0	X1: open	1	—	12	MHz	When the main external clock is used
		X0, X1	*	1	—	32.5	MHz	
			—	3	—	8.13	MHz	Main PLL multiplied by 2
			—	3	—	6.5	MHz	Main PLL multiplied by 2.5
			—	3	—	4.06	MHz	Main PLL multiplied by 4
	F_{CRH}	—	—	12.25	12.5	12.75	MHz	Operating conditions: • The main CR clock is used. • T_A = −10°C to +85°C
				9.8	10	10.2	MHz	
				7.84	8	8.16	MHz	
				0.98	1	1.02	MHz	
		—	—	12.1875	12.5	12.8125	MHz	Operating conditions: • The main CR clock is used. • T_A = −40°C to −10°C
				9.75	10	10.25	MHz	
				7.8	8	8.2	MHz	
				0.975	1	1.025	MHz	
	F_{CL}	X0A, X1A	—	—	32.768	—	kHz	When the sub-oscillation circuit is used
				—	32.768	—	kHz	When the sub-external clock is used
	F_{CRL}	—	—	50	100	200	kHz	When the sub-CR clock is used
Clock cycle time	t_{HCYL}	X0, X1	—	61.5	—	1000	ns	When the main oscillation circuit is used
		X0	X1: open	83.4	—	1000	ns	When the external clock is used
		X0, X1	*	30.8	—	1000	ns	
	t_{LCYL}	X0A, X1A	—	—	30.5	—	µs	When the subclock is used
Input clock pulse width	t_{WH1} t_{WL1}	X0	X1: open	33.4	—	—	ns	When the external clock is used, the duty ratio should range between 40% and 60%.
		X0, X1	*	12.4	—	—	ns	
	t_{WH2} t_{WL2}	X0A	—	—	15.2	—	µs	
Input clock rise time and fall time	t_{CR} t_{CF}	X0	X1: open	—	—	5	ns	When the external clock is used
		X0, X1	*	—	—	5	ns	
CR oscillation start time	t_{CRHWK}	—	—	—	—	80	µs	When the main CR clock is used
	t_{CRLWK}	—	—	—	—	10	µs	When the sub-CR clock is used

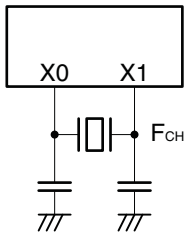
*: The external clock signal is input to X0 and the inverted external clock signal to X1.

- Input waveform generated when an external clock (main clock) is used

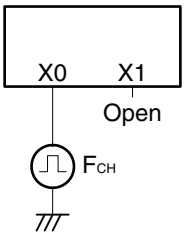


- Figure of main clock input port external connection

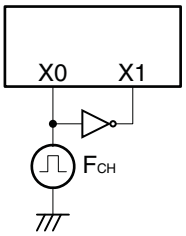
When a crystal oscillator or a ceramic oscillator is used



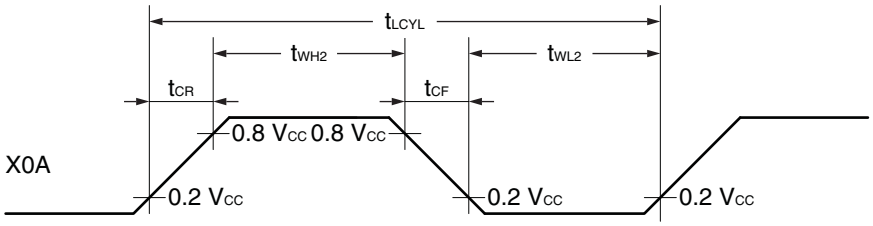
When the external clock is used (X1 is open)



When the external clock is used

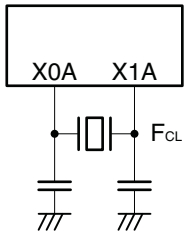


- Input waveform generated when an external clock (subclock) is used

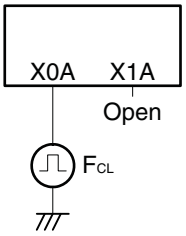


- Figure of subclock input port external connection

When a crystal oscillator or a ceramic oscillator is used



When the external clock is used



(2) Source Clock/Machine Clock

(V_{CC} = 5.0 V ±10%, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Source clock cycle time*1	t_{SCLK}	—	61.5	—	2000	ns	When the main oscillation clock is used Min: F_{CH} = 32.5 MHz, divided by 2 Max: F_{CH} = 1 MHz, divided by 2
			61.5	—	2000	ns	When the main oscillation clock is used Min: F_{CH} = 8.125 MHz, multiplied by the PLL multiplier of 2 Max: F_{CH} = 1 MHz, divided by 2
			80	—	1000	ns	When the main CR clock is used Min: F_{CRH} = 12.5 MHz Max: F_{CRH} = 1 MHz
			—	61	—	µs	When the sub-oscillation clock is used F_{CL} = 32.768 kHz, divided by 2
			—	20	—	µs	When the sub-CR clock is used F_{CRL} = 100 kHz, divided by 2
Source clock frequency	F_{SP}	—	0.50	—	16.25	MHz	When the main oscillation clock is used
			1	—	12.5	MHz	When the main CR clock is used
	F_{SPL}		—	16.384	—	kHz	When the sub-oscillation clock is used
			—	50	—	kHz	When the sub-CR clock is used F_{CRL} = 100 kHz, divided by 2
Machine clock cycle time*2 (minimum instruction execution time)	t_{MCLK}	—	61.5	—	32000	ns	When the main oscillation clock is used Min: F_{SP} = 16.25 MHz, no division Max: F_{SP} = 0.5 MHz, divided by 16
			80	—	16000	ns	When the main CR clock is used Min: F_{SP} = 12.5 MHz Max: F_{SP} = 1 MHz, divided by 16
			61	—	976.5	µs	When the sub-oscillation clock is used Min: F_{SPL} = 16.384 kHz, no division Max: F_{SPL} = 16.384 kHz, divided by 16
			20	—	320	µs	When the sub-CR clock is used Min: F_{SPL} = 50 kHz, no division Max: F_{SPL} = 50 kHz, divided by 16
Machine clock frequency	F_{MP}	—	0.031	—	16.25	MHz	When the main oscillation clock is used
			0.0625	—	12.5	MHz	When the main CR clock is used
	F_{MPL}		1.024	—	16.384	kHz	When the sub-oscillation clock is used
			3.125	—	50	kHz	When the sub-CR clock is used F_{CRL} = 100 kHz

*1: This is the clock before it is divided according to the division ratio set by the machine clock divide ratio select bits (SYCC:DIV1, DIV0). This source clock is divided to become a machine clock according to the division ratio set by the machine clock divide ratio select bits (SYCC:DIV1, DIV0). In addition, a source clock can be selected from the following.

- Main clock divided by 2
- PLL multiplication of main clock (select from 2, 2.5, 4 multiplication)
- Main CR clock divided by 2
- Subclock divided by 2
- Sub-CR clock divided by 2

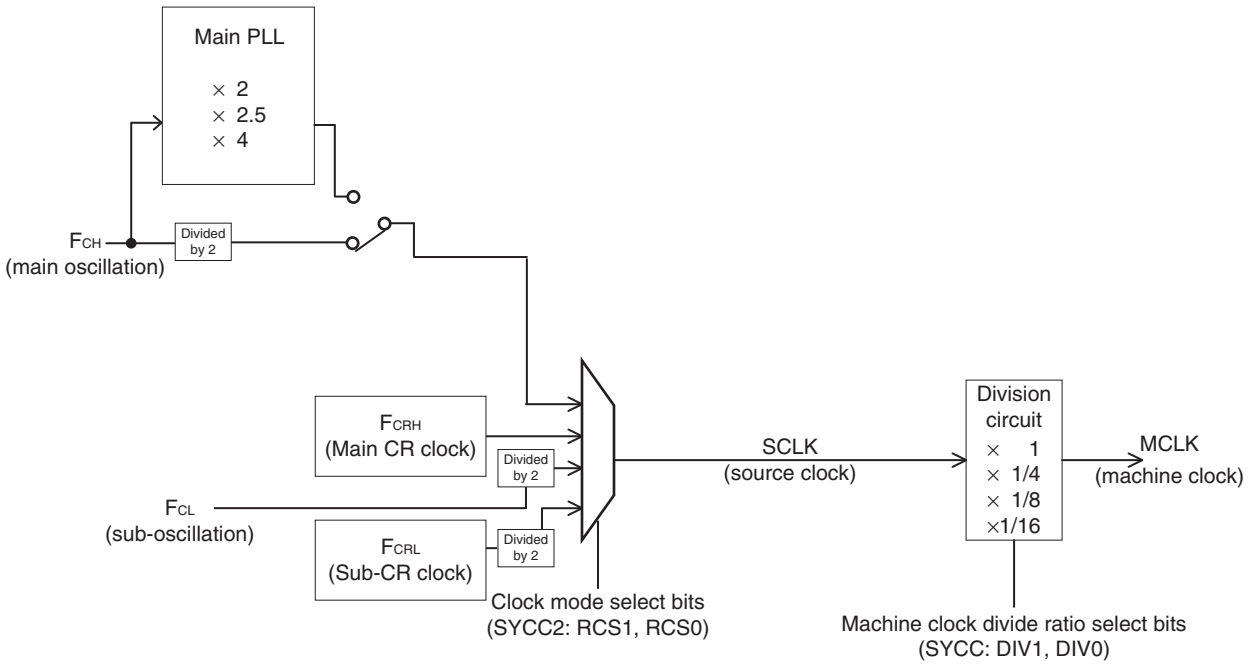
(Continued)

(Continued)

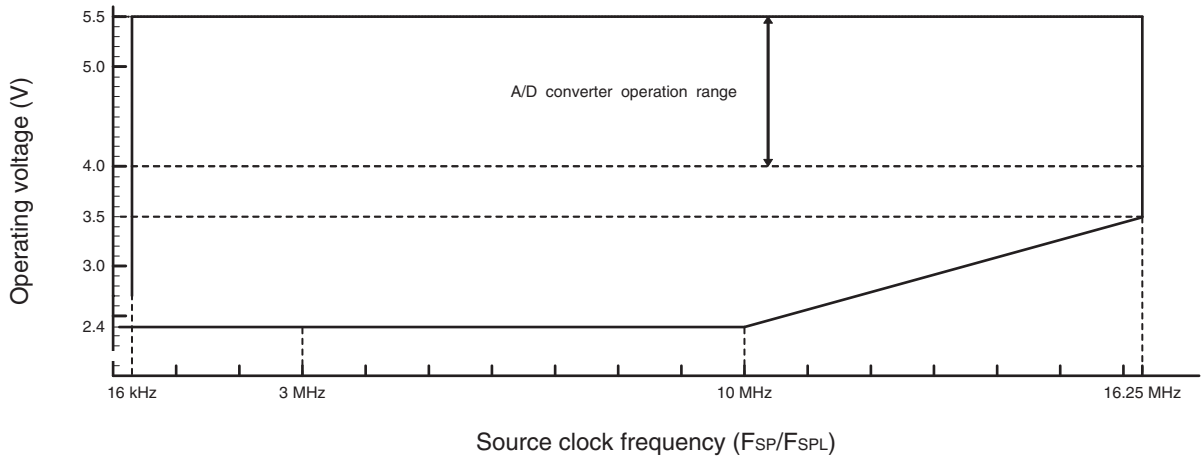
*2: This is the operating clock of the microcontroller. A machine clock can be selected from the following.

- Source clock (no division)
- Source clock divided by 4
- Source clock divided by 8
- Source clock divided by 16

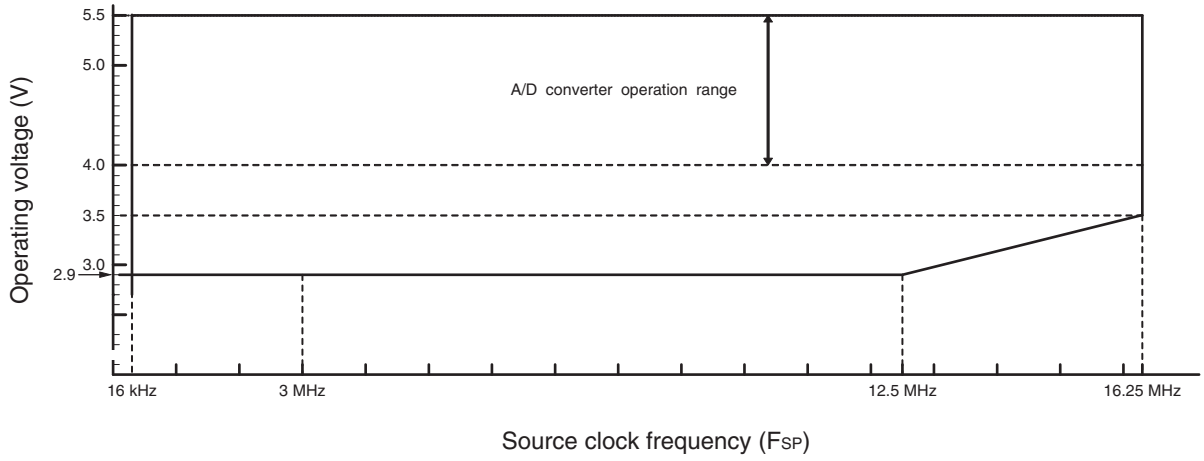
- Schematic diagram of the clock generation block



- Operating voltage - Operating frequency (When T_A = –40°C to +85°C)
  Without the on-chip debug function



- Operating voltage - Operating frequency (When T_A = –40°C to +85°C)
  With the on-chip debug function



(3) External Reset

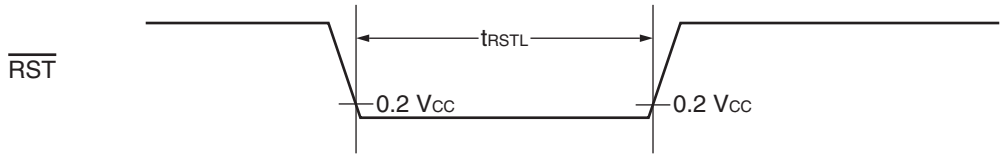
(V_{CC} = 5.0 V ±10%, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
$\overline{RST}$ "L" level pulse width	t_{RSTL}	2 t_{MCLK}*1	—	ns	In normal operation
		Oscillation time of the oscillator*2 + 100	—	µs	In stop mode, subclock mode, subsleep mode, watch mode, and power-on
		100	—	µs	In time-base timer mode

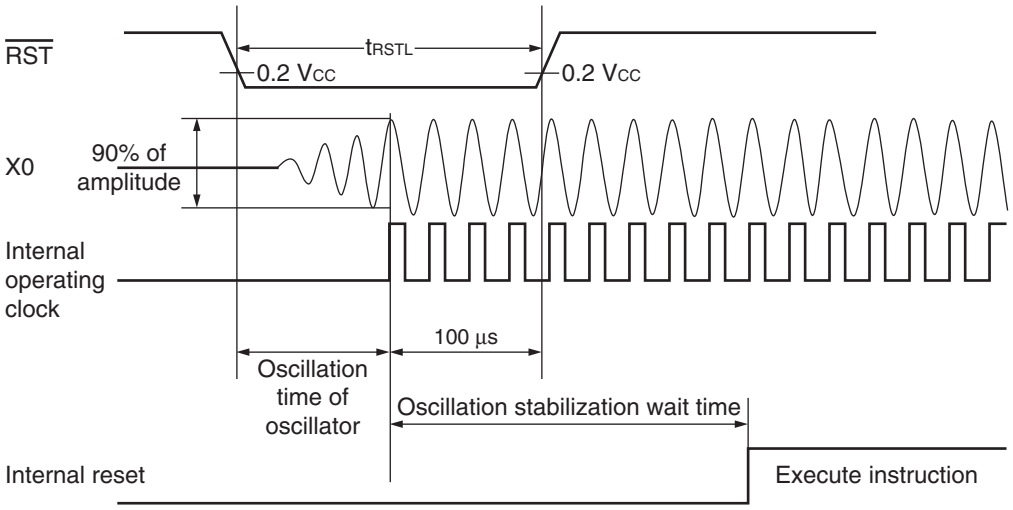
*1: See "(2) Source Clock/Machine Clock" for t_{MCLK}.

*2: The oscillation time of an oscillator is the time for it to reach 90% of its amplitude. The crystal oscillator has an oscillation time of between several ms and tens of ms. The ceramic oscillator has an oscillation time of between hundreds of µs and several ms. The external clock has an oscillation time of 0 ms. The CR oscillator clock has an oscillation time of between several µs and several ms.

- In normal operation



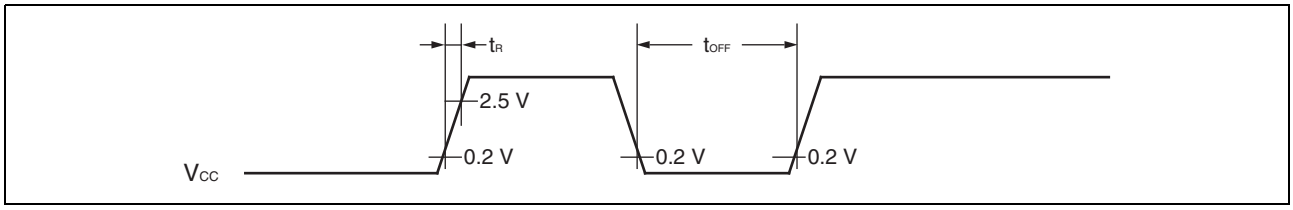
- In stop mode, subclock mode, subsleep mode, watch mode and power-on



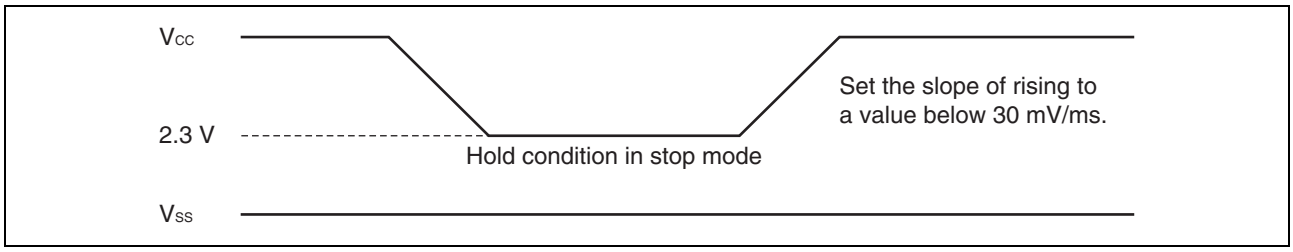
(4) Power-on Reset

(V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min	Max		
Power supply rising time	t_R	—	—	50	ms	
Power supply cutoff time	t_{OFF}	—	1	—	ms	Wait time until power-on



Note: A sudden change of power supply voltage may activate the power-on reset function. When changing the power supply voltage during the operation, set the slope of rising to a value below within 30 mV/ms as shown below.

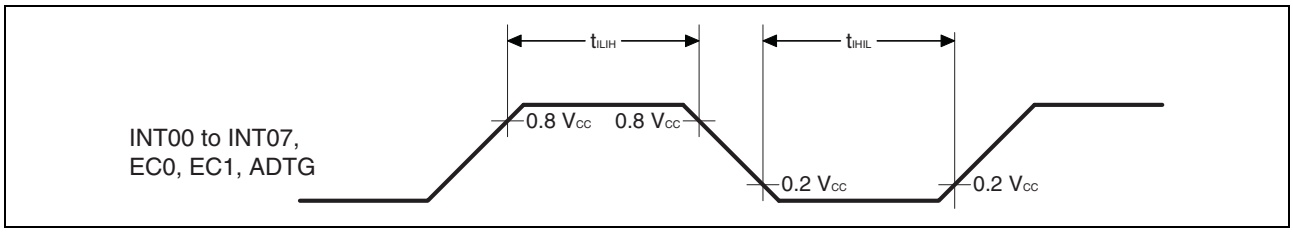


(5) Peripheral Input Timing

(V_{CC} = 5.0 V ±10%, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
Peripheral input “H” pulse width	t_{ILIH}	INT00 to INT07, EC0, EC1, ADTG	2 t_{MCLK}*	—	ns
Peripheral input “L” pulse width	t_{IHIL}		2 t_{MCLK}*	—	ns

*: See “(2) Source Clock/Machine Clock” for t_{MCLK}.



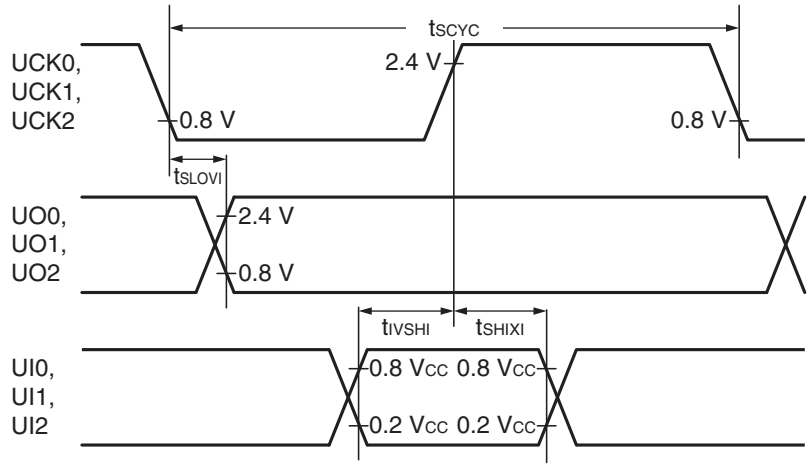
(6) UART/SIO, Serial I/O Timing

(V_{CC} = 5.0 V ±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = −40°C to +85°C)

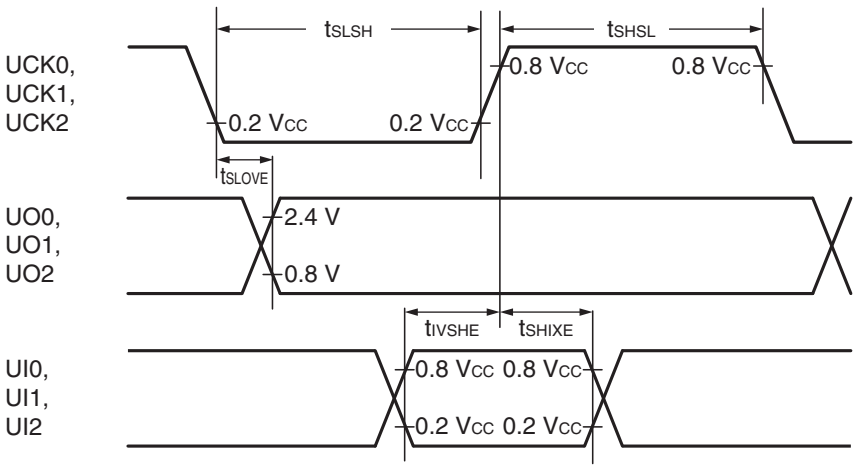
Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	UCK0, UCK1, UCK2	Internal clock operation output pin: C_L = 80 pF + 1 TTL	4 t_{MCLK}*	—	ns
UCK ↓→ UO time	t_{SLOVI}	UCK0, UCK1, UCK2, UO0, UO1, UO2		−190	+190	ns
Valid UI → UCK ↑	t_{IVSHI}	UCK0, UCK1, UCK2, UI0, UI1, UI2		2 t_{MCLK}*	—	ns
UCK ↑→ valid UI hold time	t_{SHIXI}	UCK0, UCK1, UCK2, UI0, UI1, UI2		2 t_{MCLK}*	—	ns
Serial clock “H” pulse width	t_{SHSL}	UCK0, UCK1, UCK2	External clock operation output pin: C_L = 80 pF + 1 TTL	4 t_{MCLK}*	—	ns
Serial clock “L” pulse width	t_{SLSH}	UCK0, UCK1, UCK2		4 t_{MCLK}*	—	ns
UCK ↓→ UO time	t_{SLOVE}	UCK0, UCK1, UCK2, UO0, UO1, UO2		—	190	ns
Valid UI → UCK ↑	t_{IVSHE}	UCK0, UCK1, UCK2, UI0, UI1, UI2		2 t_{MCLK}*	—	ns
UCK ↑→ valid UI hold time	t_{SHIXE}	UCK0, UCK1, UCK2, UI0, UI1, UI2		2 t_{MCLK}*	—	ns

*: See “(2) Source Clock/Machine Clock” for t_{MCLK}.

- Internal shift clock mode



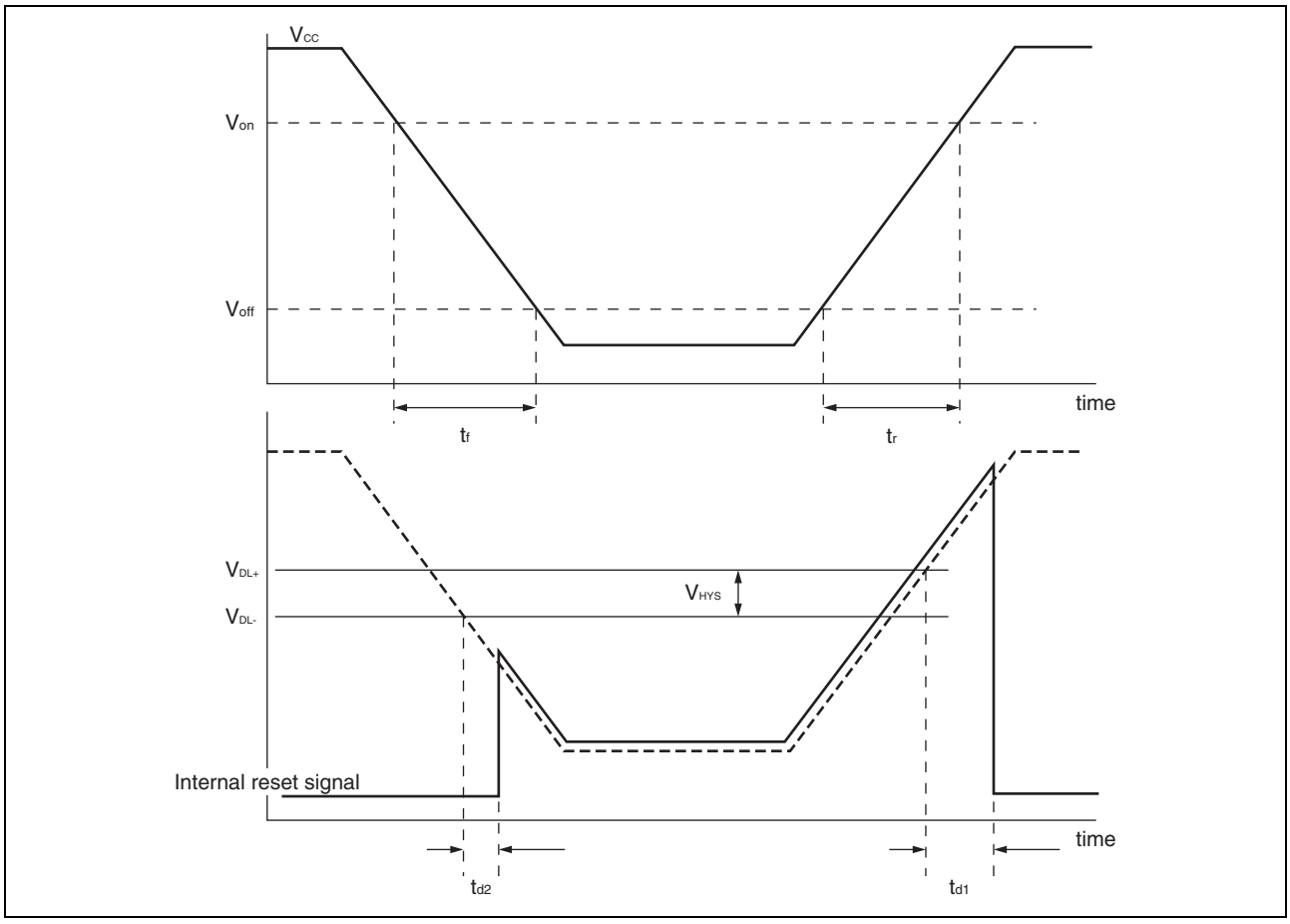
- External shift clock mode



(7) Low-voltage Detection

(V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Release voltage	V_{DL+}	2.52	2.7	2.88	V	At power supply rise
Detection voltage	V_{DL-}	2.42	2.6	2.78	V	At power supply fall
Hysteresis width	V_{HYS}	70	100	—	mV	
Power supply start voltage	V_{off}	—	—	2.3	V	
Power supply end voltage	V_{on}	4.9	—	—	V	
Power supply voltage change time (at power supply rise)	t_r	3000	—	—	µs	Slope of power supply that the reset release signal generates within the rating (V_{DL+})
Power supply voltage change time (at power supply fall)	t_f	300	—	—	µs	Slope of power supply that the reset detection signal generates within the rating (V_{DL-})
Reset release delay time	t_{d1}	—	—	300	µs	
Reset detection delay time	t_{d2}	—	—	20	µs	



(8) I²C Timing

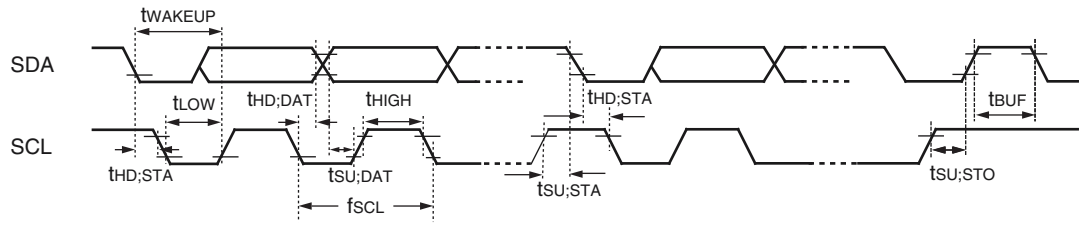
(V_{CC} = 5.0 V ±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Conditions	Value				Unit
				Standard-mode		Fast-mode		
				Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	SCL	R = 1.7 kΩ, C = 50 pF*1	0	100	0	400	kHz
(Repeat) Start condition hold time SDA ↓ → SCL ↓	$t_{HD;STA}$	SCL, SDA		4.0	—	0.6	—	µs
SCL clock “L” width	t_{LOW}	SCL		4.7	—	1.3	—	µs
SCL clock “H” width	t_{HIGH}	SCL		4.0	—	0.6	—	µs
(Repeat) Start condition setup time SCL ↑ → SDA ↓	$t_{SU;STA}$	SCL, SDA		4.7	—	0.6	—	µs
Data hold time SCL ↓ → SDA ↓ ↑	$t_{HD;DAT}$	SCL, SDA		0	3.45*2	0	0.9*3	µs
Data setup time SDA ↓ ↑ → SCL ↑	$t_{SU;DAT}$	SCL, SDA		0.25	—	0.1	—	µs
Stop condition setup time SCL ↑ → SDA ↑	$t_{SU;STO}$	SCL, SDA		4.0	—	0.6	—	µs
Bus free time between stop condition and start condition	t_{BUF}	SCL, SDA		4.7	—	1.3	—	µs

*1: R represents the pull-up resistor of the SCL and SDA lines, and C the load capacitor of the SCL and SDA lines.

*2: The maximum $t_{HD;DAT}$ in the Standard-mode is applicable only when the time during which the device is holding the SCL signal at “L” (t_{LOW}) does not extend.

*3: A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, provided that the condition of $t_{SU;DAT} \geq 250$ ns is fulfilled.



(Continued)

(V_{CC} = 5.0 V ±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Conditions	Value*2		Unit	Remarks
				Min	Max		
SCL clock “L” width	t_{LOW}	SCL	R = 1.7 kΩ, C = 50 pF*1	$(2 + nm / 2)t_{MCLK} – 20$	—	ns	Master mode
SCL clock “H” width	t_{HIGH}	SCL		$(nm / 2)t_{MCLK} – 20$	$(nm / 2)t_{MCLK} + 20$	ns	Master mode
Start condition hold time	$t_{HD;STA}$	SCL, SDA		$(– 1 + nm / 2)t_{MCLK} – 20$	$(– 1 + nm)t_{MCLK} + 20$	ns	Master mode Maximum value is applied when m, n = 1, 8. Otherwise, the minimum value is applied.
Stop condition setup time	$t_{SU;STO}$	SCL, SDA		$(1 + nm / 2)t_{MCLK} – 20$	$(1 + nm / 2)t_{MCLK} + 20$	ns	Master mode
Start condition setup time	$t_{SU;STA}$	SCL, SDA		$(1 + nm / 2)t_{MCLK} – 20$	$(1 + nm / 2)t_{MCLK} + 20$	ns	Master mode
Bus free time between stop condition and start condition	t_{BUF}	SCL, SDA		$(2 nm + 4)t_{MCLK} – 20$	—	ns	
Data hold time	$t_{HD;DAT}$	SCL, SDA		$3 t_{MCLK} – 20$	—	ns	Master mode
Data setup time	$t_{SU;DAT}$	SCL, SDA		$(– 2 + nm / 2)t_{MCLK} – 20$	$(– 1 + nm / 2)t_{MCLK} + 20$	ns	Master mode When assuming that “L” of SCL is not extended, the minimum value is applied to first bit of continuous data. Otherwise, the maximum value is applied.
Setup time between clearing interrupt and SCL rising	$t_{SU;INT}$	SCL		$(nm / 2)t_{MCLK} – 20$	$(1 + nm / 2)t_{MCLK} + 20$	ns	Minimum value is applied to interrupt at 9th SCL↓. Maximum value is applied to interrupt at 8th SCL↓.
SCL clock “L” width	t_{LOW}	SCL		$4 t_{MCLK} – 20$	—	ns	At reception
SCL clock “H” width	t_{HIGH}	SCL		$4 t_{MCLK} – 20$	—	ns	At reception

(Continued)

(Continued)

(V_{CC} = 5.0 V ±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Conditions	Value*2		Unit	Remarks
				Min	Max		
Start condition detection	$t_{HD;STA}$	SCL, SDA	R = 1.7 kΩ, C = 50 pF*1	2 t_{MCLK} – 20	—	ns	Not detected when 1 t_{MCLK} is used at reception
Stop condition detection	$t_{SU;STO}$	SCL, SDA		2 t_{MCLK} – 20	—	ns	Not detected when 1 t_{MCLK} is used at reception
Restart condition detection condition	$t_{SU;STA}$	SCL, SDA		2 t_{MCLK} – 20	—	ns	Not detected when 1 t_{MCLK} is used at reception
Bus free time	t_{BUF}	SCL, SDA		2 t_{MCLK} – 20	—	ns	At reception
Data hold time	$t_{HD;DAT}$	SCL, SDA		2 t_{MCLK} – 20	—	ns	At slave transmission mode
Data setup time	$t_{SU;DAT}$	SCL, SDA		t_{LOW} – 3 t_{MCLK} – 20	—	ns	At slave transmission mode
Data hold time	$t_{HD;DAT}$	SCL, SDA		0	—	ns	At reception
Data setup time	$t_{SU;DAT}$	SCL, SDA		t_{MCLK} – 20	—	ns	At reception
SDA↓→SCL↑ (at wakeup function)	t_{WAKEUP}	SCL, SDA		Oscillation stabilization wait time + 2 t_{MCLK} – 20	—	ns	

*1: R represents the pull-up resistor of the SCL and SDA lines, and C the load capacitor of the SCL and SDA lines.

*2:
- See “(2) Source Clock/Machine Clock” for t_{MCLK}.
- m represents the CS4 bit and CS3 bit (bit4 and bit3) in the I²C clock control register (ICCR0).
- n represents the CS2 bit to CS0 bit (bit2 to bit0) in the I²C clock control register (ICCR0).
- The actual timing of I²C is determined by the values of m and n set by the machine clock (t_{MCLK}) and the CS4 to CS0 bits in the ICCR0 register.
- Standard-mode:
  m and n can be set to values in the following range: 0.9 MHz < t_{MCLK} (machine clock) < 16.25 MHz.
  The usable frequencies of the machine clock are determined by the settings of m and n as shown below.
  (m, n) = (1, 8) : 0.9 MHz < t_{MCLK} ≤ 1 MHz
  (m, n) = (1, 22), (5, 4), (6, 4), (7, 4), (8, 4) : 0.9 MHz < t_{MCLK} ≤ 2 MHz
  (m, n) = (1, 38), (5, 8), (6, 8), (7, 8), (8, 8) : 0.9 MHz < t_{MCLK} ≤ 4 MHz
  (m, n) = (1, 98), (5, 22), (6, 22), (7, 22) : 0.9 MHz < t_{MCLK} ≤ 10 MHz
  (m, n) = (8, 22) : 0.9 MHz < t_{MCLK} ≤ 16.25 MHz
- Fast-mode:
  m and n can be set to values in the following range: 3.3 MHz < t_{MCLK} (machine clock) < 16.25 MHz.
  The usable frequencies of the machine clock are determined by the settings of m and n as shown below.
  (m, n) = (1, 8) : 3.3 MHz < t_{MCLK} ≤ 4 MHz
  (m, n) = (1, 22), (5, 4) : 3.3 MHz < t_{MCLK} ≤ 8 MHz
  (m, n) = (1, 38), (6, 4), (7, 4), (8, 4) : 3.3 MHz < t_{MCLK} ≤ 10 MHz
  (m, n) = (5, 8) : 3.3 MHz < t_{MCLK} ≤ 16.25 MHz

(9) Voltage Comparator Timing

(AV_{CC} = 4.0 V to 5.5 V, AV_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Pin name	Value			Unit	Remarks
		Min	Typ	Max		
Voltage range	CMPP, CMPN	0	—	AV_{CC} – 1.3	V	
Offset voltage	CMPP, CMPN	–10	—	+10	mV	
Delay time	CMPO	—	650	1210	ns	5 mV overdrive
		—	140	420	ns	50 mV overdrive
Power down delay	CMPO	—	—	1210	ns	Power down recovery PD: 1 → 0
		0	—	—	ns	Power down effective PD: 0 → 1 Output: “H” level
Power up stabilization time	CMPO	—	—	1210	ns	Output stabilization time at power up
Bandgap reference voltage	—	1.17	1.22	1.27	V	

5. A/D Converter

(1) A/D Converter Electrical Characteristics

(AV_{CC} = V_{CC} = 4.0 V to 5.5 V, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

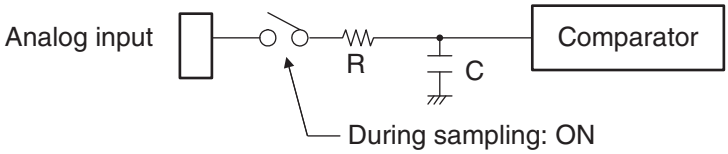
Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Resolution	—	—	—	10	bit	
Total error		–3	—	+3	LSB	
Linearity error		–2.5	—	+2.5	LSB	
Differential linear error		–1.9	—	+1.9	LSB	
Zero transition voltage	V_{OT}	AV_{SS} – 1.5 LSB	AV_{SS} + 0.5 LSB	AV_{SS} + 2.5 LSB	V	
Full-scale transition voltage	V_{FST}	AV_{CC} – 4.5 LSB	AV_{CC} – 2 LSB	AV_{CC} + 0.5 LSB	V	
Compare time	—	0.9	—	16500	µs	4.5 V ≤ V_{CC} ≤ 5.5 V
		1.8	—	16500	µs	4.0 V ≤ V_{CC} < 4.5 V
Sampling time	—	0.6	—	∞	µs	4.5 V ≤ V_{CC} ≤ 5.5 V, with external impedance < 5.4 kΩ
		1.2	—	∞	µs	4.0 V ≤ V_{CC} < 4.5 V, with external impedance < 2.4 kΩ
Analog input current	I_{AIN}	–0.3	—	+0.3	µA	
Analog input voltage	V_{AIN}	AV_{SS}	—	AV_{CC}	V	

(2) Notes on Using the A/D Converter

• External impedance of analog input and its sampling time

- The A/D converter has a sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the capacitor of the internal sample and hold circuit is insufficient, adversely affecting A/D conversion precision. Therefore, to satisfy the A/D conversion precision standard, considering the relationship between the external impedance and minimum sampling time, either adjust the register value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value. In addition, if sufficient sampling time cannot be secured, connect a capacitor of about 0.1 µF to the analog input pin.

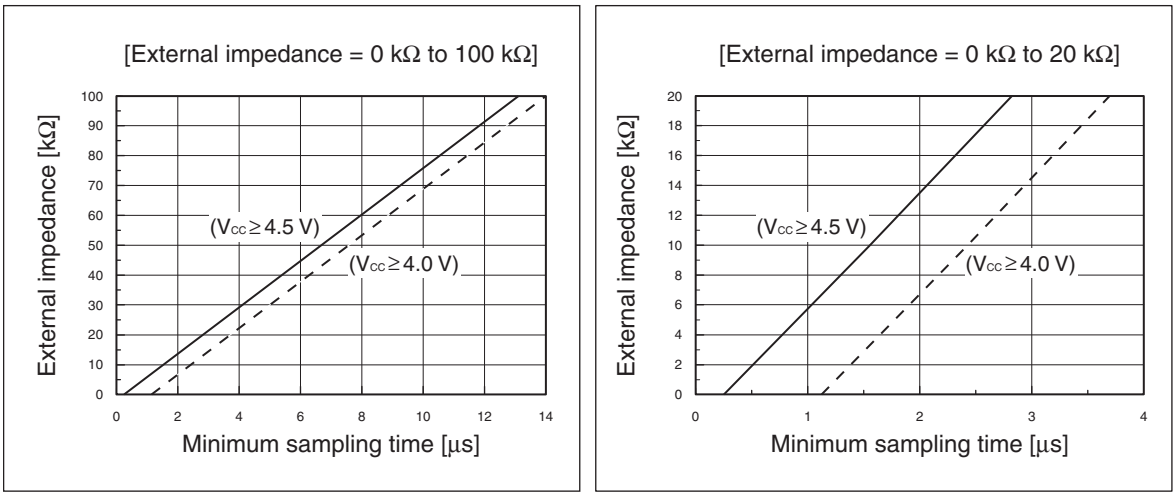
- Analog input equivalent circuit



V_{CC}	R	C
4.5 V ≤ V_{CC} ≤ 5.5 V	1.95 kΩ (Max)	17 pF (Max)
4.0 V ≤ V_{CC} < 4.5 V	8.98 kΩ (Max)	17 pF (Max)

Note: The values are reference values.

- Relationship between external impedance and minimum sampling time

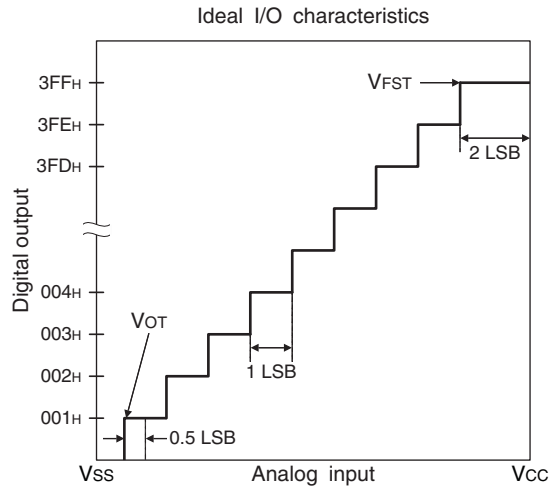


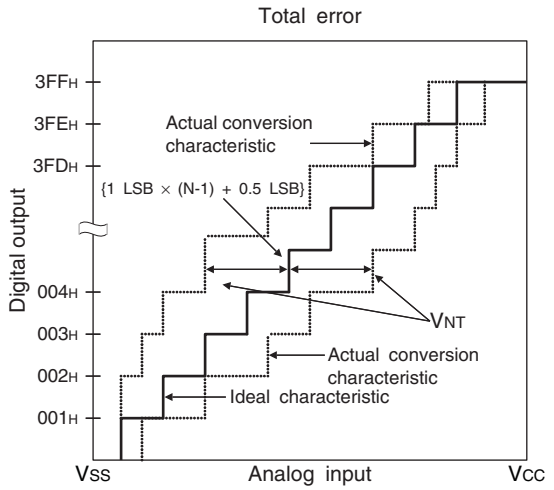
• A/D conversion error

As |V_{CC}–V_{SS}| decreases, the A/D conversion error increases proportionately.

(3) Definitions of A/D Converter Terms

- Resolution
  It indicates the level of analog variation that can be distinguished by the A/D converter.
  When the number of bits is 10, analog voltage can be divided into 2^{10} = 1024.
- Linearity error (unit: LSB)
  It indicates how much an actual conversion value deviates from the straight line connecting the zero transition point (“00 0000 0000” ← → “00 0000 0001”) of a device to the full-scale transition point (“11 1111 1111” ← → “11 1111 1110”) of the same device.
- Differential linear error (unit: LSB)
  It indicates how much the input voltage required to change the output code by 1 LSB deviates from an ideal value.
- Total error (unit: LSB)
  It indicates the difference between an actual value and a theoretical value. The error can be caused by a zero transition error, a full-scale transition errors, a linearity error, a quantum error, or noise.





$$1\ \text{LSB} = \frac{V_{CC} - V_{SS}}{1024}\ (\text{V})$$

$$\text{Total error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

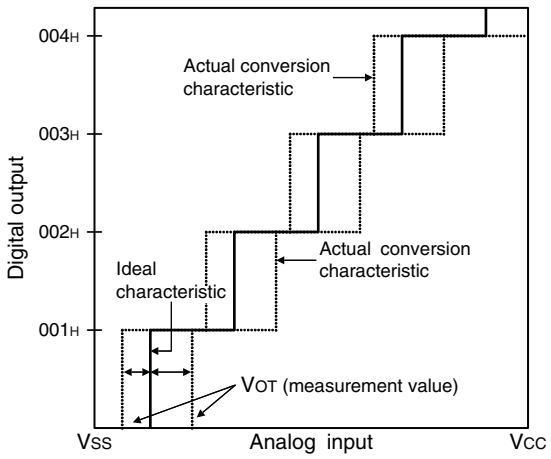
N : A/D converter digital output value

V_{NT} : Voltage at which the digital output transits from $(N - 1)_H$ to N_H

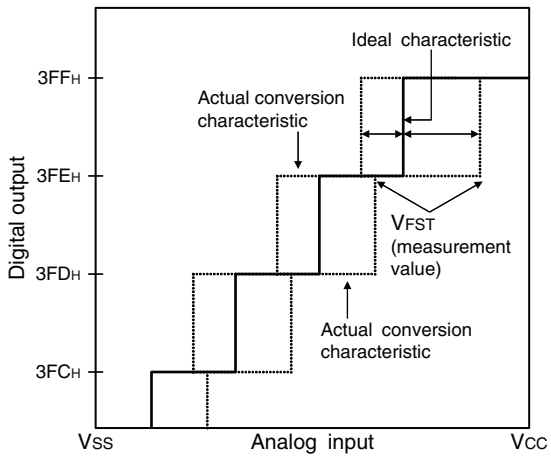
(Continued)

(Continued)

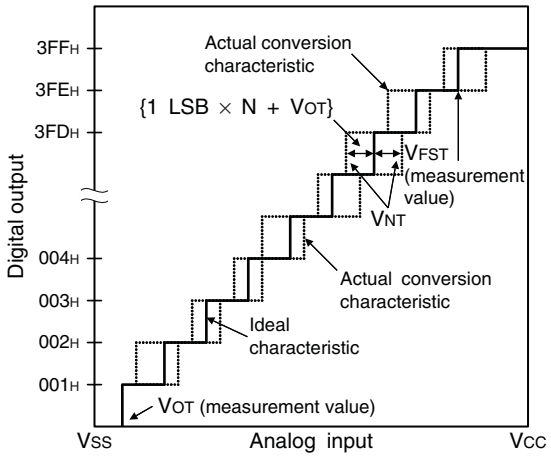
Zero transition error



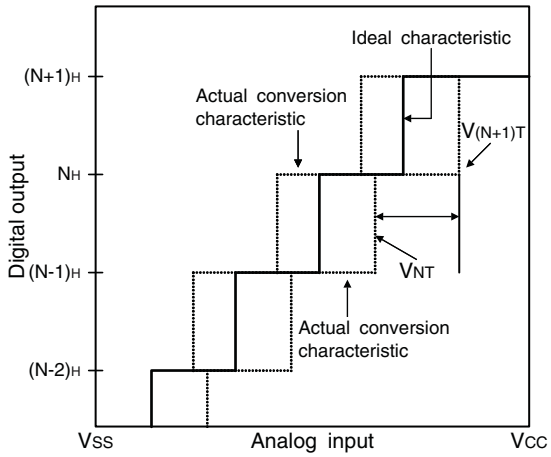
Full-scale transition error



Linearity error



Differential linearity error



$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times N + V_{OT}\}}{1\ \text{LSB}}$$

$$\text{Differential linear error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1$$

N : A/D converter digital output value

V_{NT} : Voltage at which the digital output transits from $(N - 1)_H$ to N_H

V_{OT} (ideal value) = V_{SS} + 0.5 LSB [V]

V_{FST} (ideal value) = V_{CC} - 2 LSB [V]

6. Flash Memory Program/Erase Characteristics

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time (2 Kbyte sector)	—	0.2*1	0.5*2	s	The time of writing 00_H prior to erasure is excluded.
Sector erase time (16 Kbyte sector)	—	0.5*1	7.5*2	s	The time of writing 00_H prior to erasure is excluded.
Byte writing time	—	21	6100*2	µs	System-level overhead is excluded.
Program/erase cycle	100000	—	—	cycle	
Power supply voltage at program/erase	3.0	—	5.5	V	
Flash memory data retention time	20*3	—	—	year	Average T_A = +85°C

*1: T_A = +25°C, V_{CC} = 5.0 V, 100000 cycles

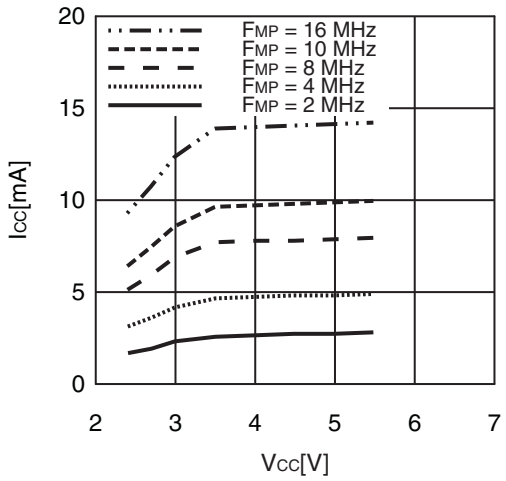
*2: T_A = +85°C, V_{CC} = 3.0 V, 100000 cycles

*3: This value is converted from the result of a technology reliability assessment. (The value is converted from the result of a high temperature accelerated test using the Arrhenius equation with the average temperature being +85°C).

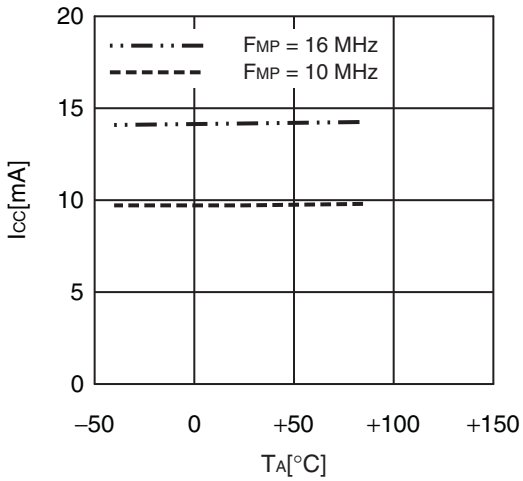
■ SAMPLE CHARACTERISTICS

- Power supply current temperature characteristics

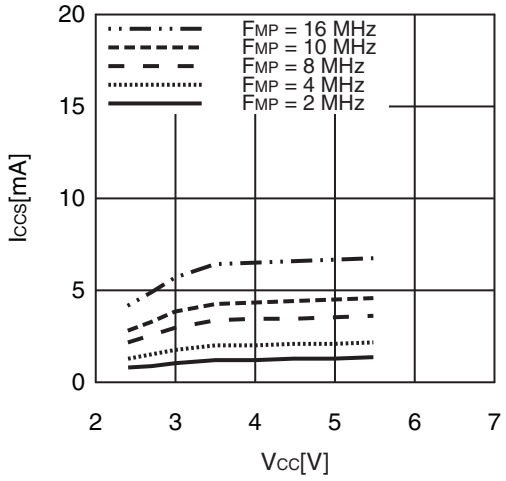
I_{CC} – V_{CC}
T_A = +25°C, F_{MP} = 2, 4, 8, 10, 16 MHz (divided by 2)
Main clock mode with the external clock operating



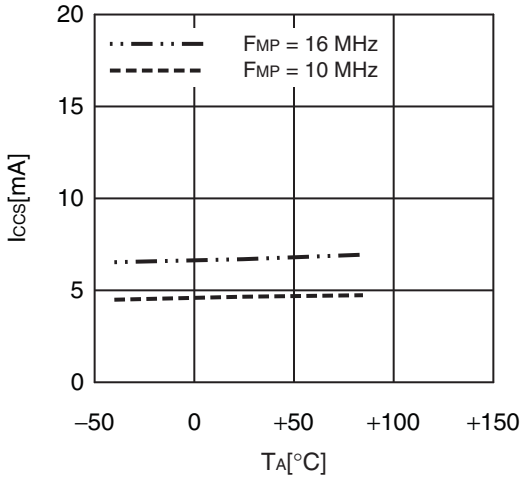
I_{CC} – T_A
V_{CC} = 5.5 V, F_{MP} = 10, 16 MHz (divided by 2)
Main clock mode with the external clock operating



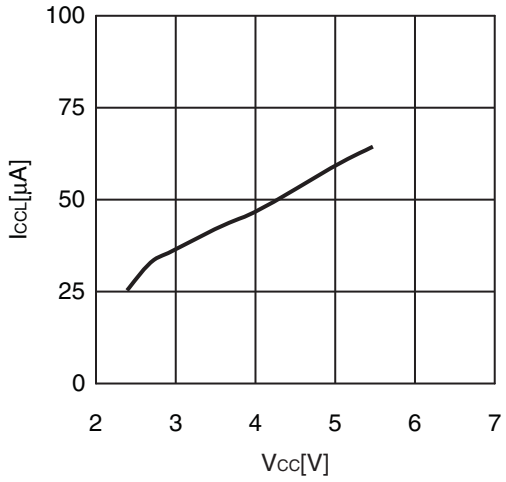
I_{CCS} – V_{CC}
T_A = +25°C, F_{MP} = 2, 4, 8, 10, 16 MHz (divided by 2)
Main sleep mode with the external clock operating



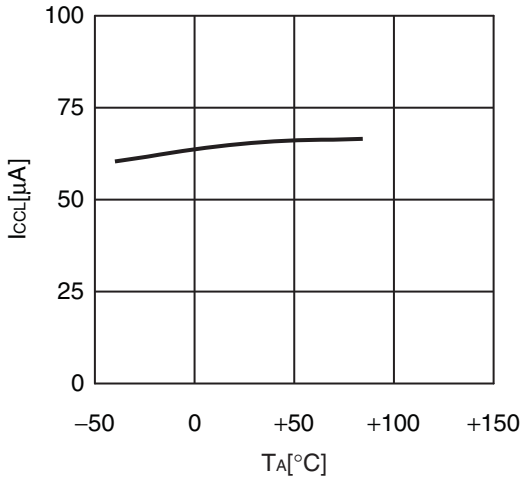
I_{CCS} – T_A
V_{CC} = 5.5 V, F_{MP} = 10, 16 MHz (divided by 2)
Main sleep mode with the external clock operating



I_{CCL} – V_{CC}
T_A = +25°C, F_{MPL} = 16 kHz (divided by 2)
Subclock mode with the external clock operating



I_{CCL} – T_A
V_{CC} = 5.5 V, F_{MPL} = 16 kHz (divided by 2)
Subclock mode with the external clock operating

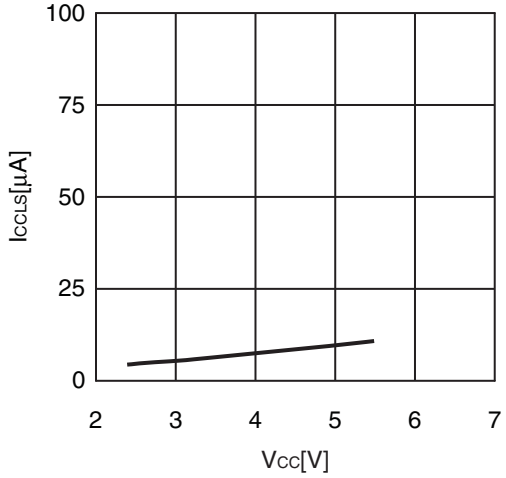


(Continued)

I_{CCLS} – V_{CC}

T_A = +25°C, F_{MPL} = 16 kHz (divided by 2)

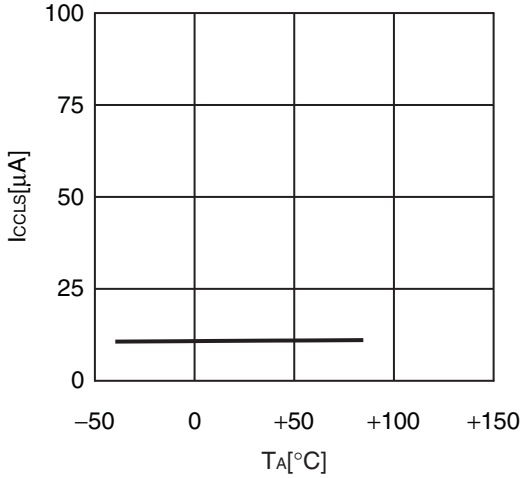
Subsleep mode with the external clock operating



I_{CCLS} – T_A

V_{CC} = 5.5 V, F_{MPL} = 16 kHz (divided by 2)

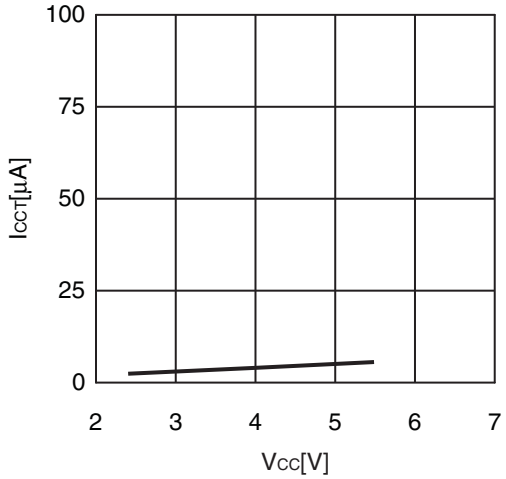
Subsleep mode with the external clock operating



I_{CCT} – V_{CC}

T_A = +25°C, F_{MPL} = 16 kHz (divided by 2)

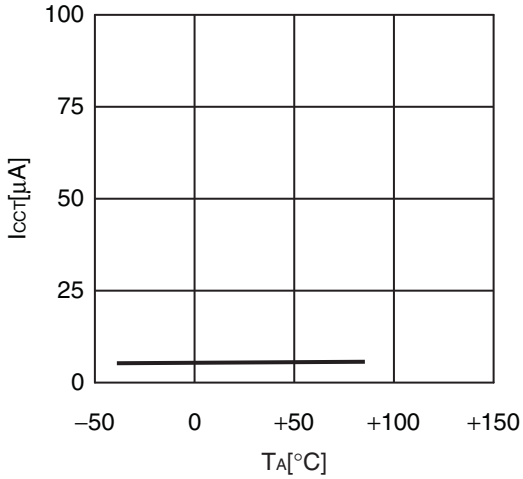
Watch mode with the external clock operating



I_{CCT} – T_A

V_{CC} = 5.5 V, F_{MPL} = 16 kHz (divided by 2)

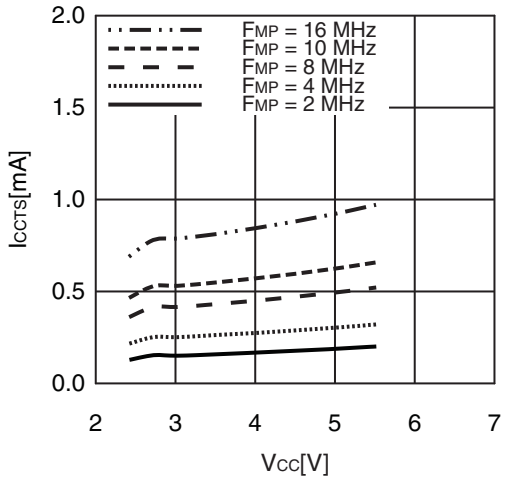
Watch mode with the external clock operating



I_{CCTS} – V_{CC}

T_A = +25°C, F_{MP} = 2, 4, 8, 10, 16 MHz (divided by 2)

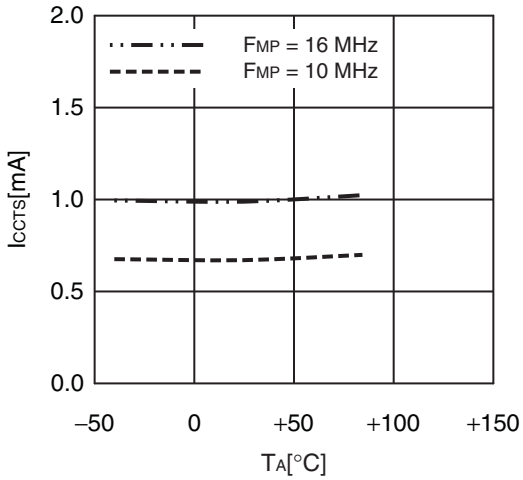
Time-base timer mode with the external clock operating



I_{CCTS} – T_A

V_{CC} = 5.5 V, F_{MP} = 10, 16 MHz (divided by 2)

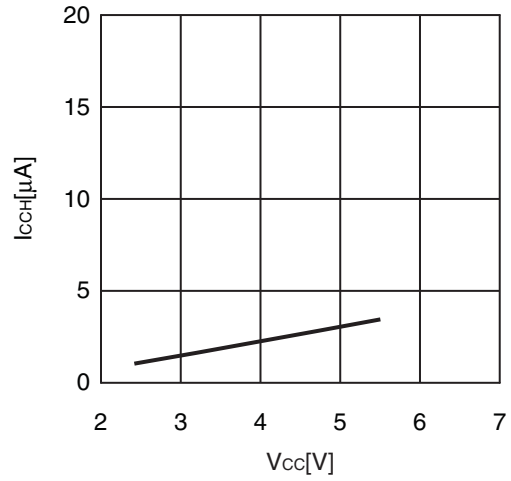
Time-base timer mode with the external clock operating



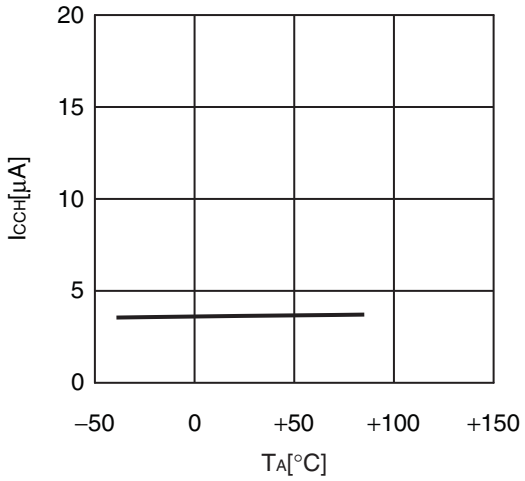
(Continued)

(Continued)

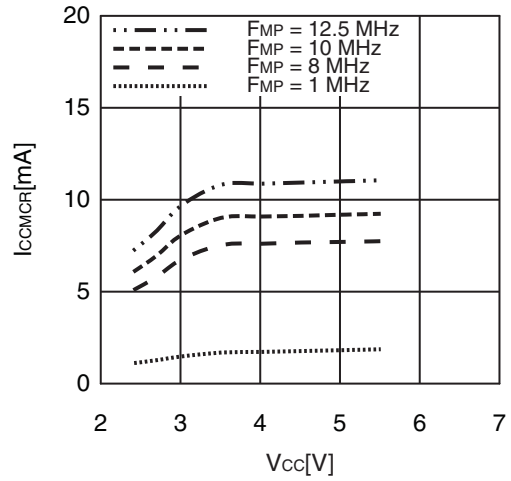
I_{CCH} – V_{CC}
T_A = +25°C, F_{MPL} = (stop)
Substop mode with the external clock stopping



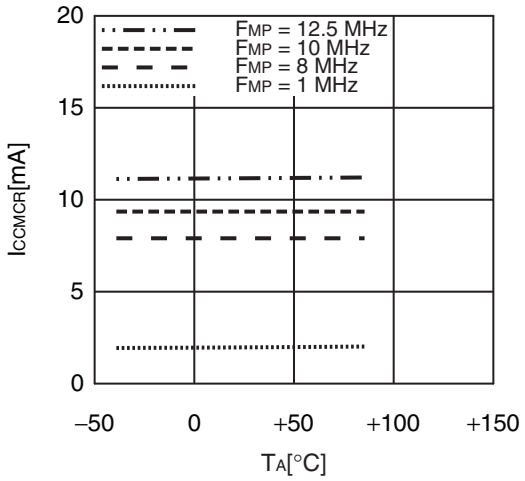
I_{CCH} – T_A
V_{CC} = 5.5 V, F_{MPL} = (stop)
Substop mode with the external clock stopping



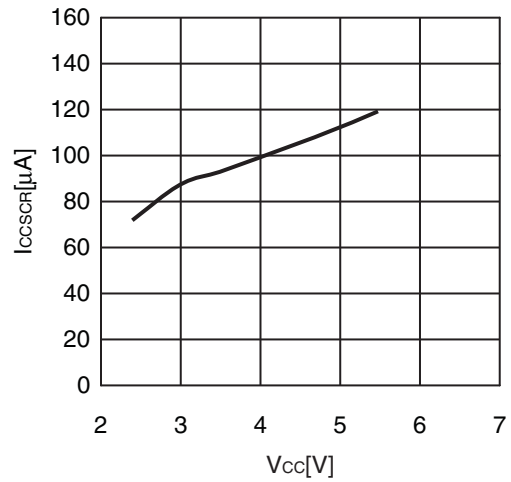
I_{CCMCR} – V_{CC}
T_A = +25°C, F_{MP} = 1, 8, 10, 12.5 MHz (no division)
Main clock mode with the main CR clock operating



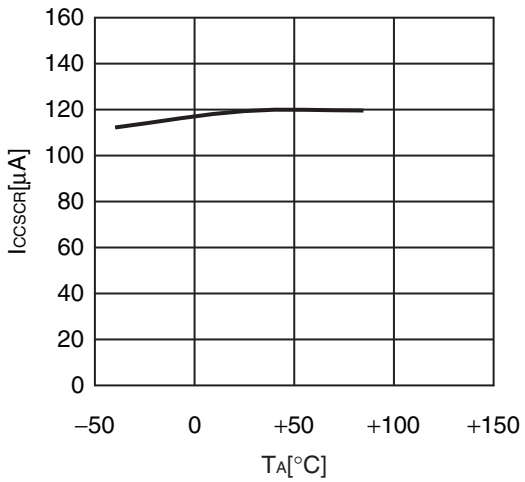
I_{CCMCR} – T_A
V_{CC} = 5.5 V, F_{MP} = 1, 8, 10, 12.5 MHz (no division)
Main clock mode with the main CR clock operating



I_{CCSCR} – V_{CC}
T_A = +25°C, F_{MPL} = 50 kHz (divided by 2)
Subclock mode with the sub-CR clock operating

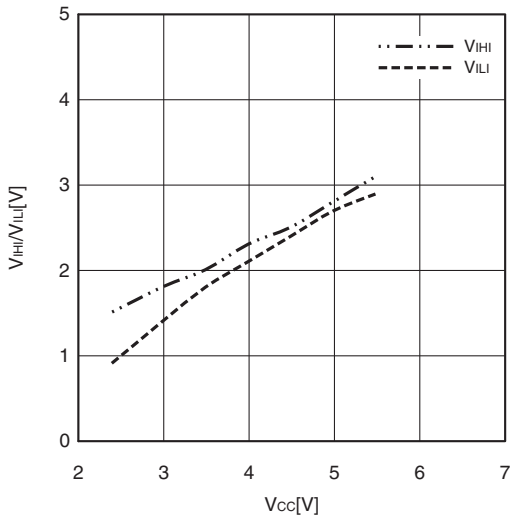


I_{CCSCR} – T_A
V_{CC} = 5.5 V, F_{MPL} = 50 kHz (divided by 2)
Subclock mode with the sub-CR clock operating

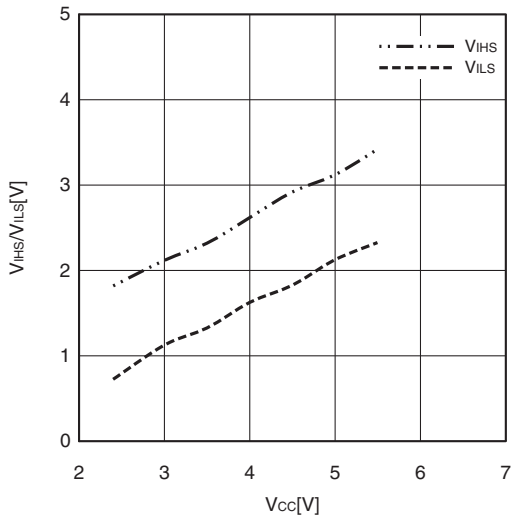


- Input voltage characteristics

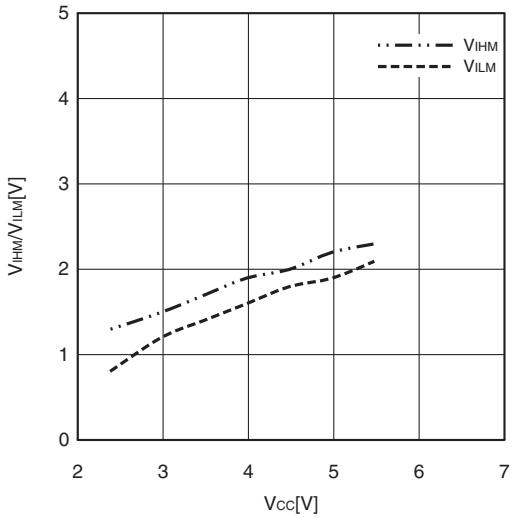
V_{IHI} – V_{CC} and V_{ILI} – V_{CC}
T_A = +25°C



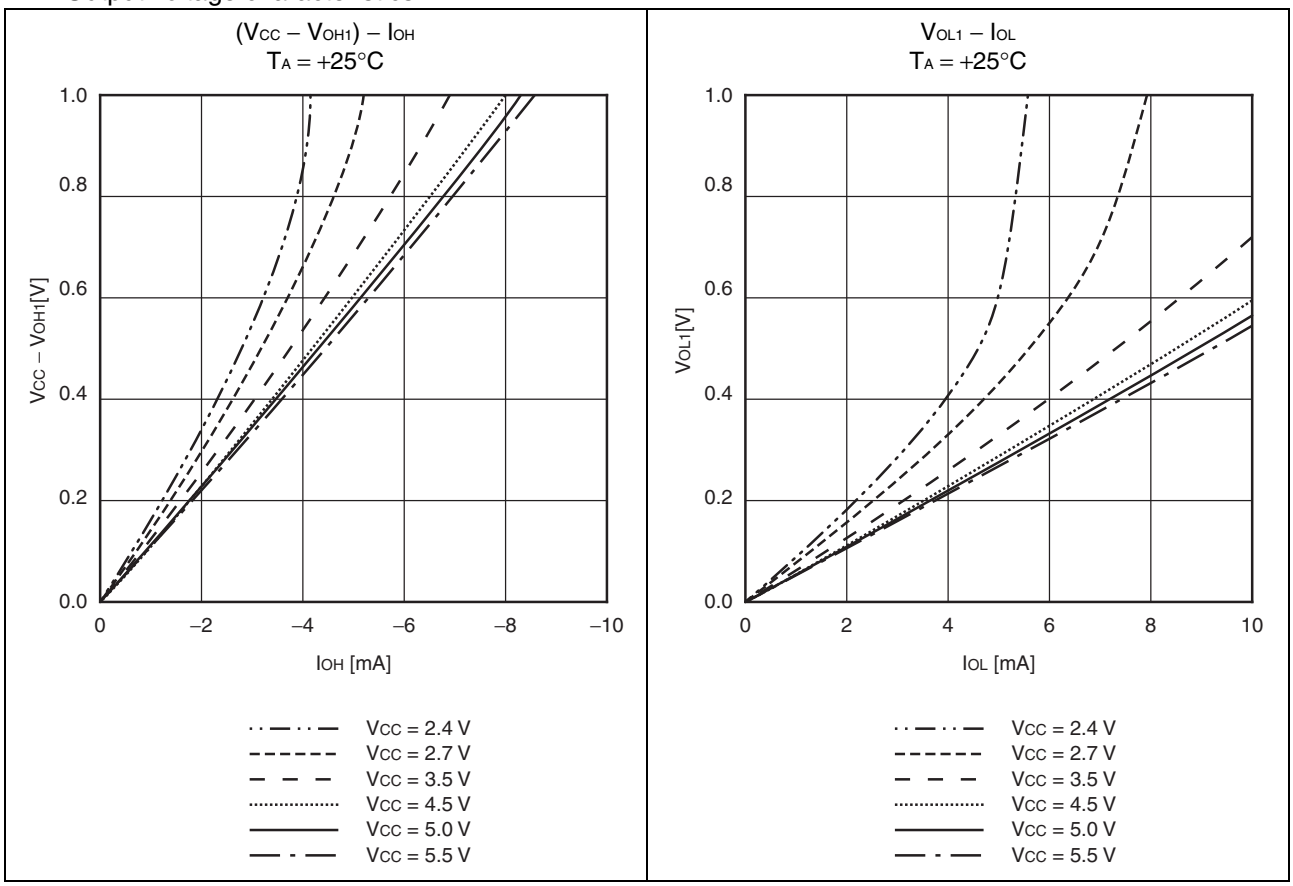
V_{IHS} – V_{CC} and V_{ILS} – V_{CC}
T_A = +25°C



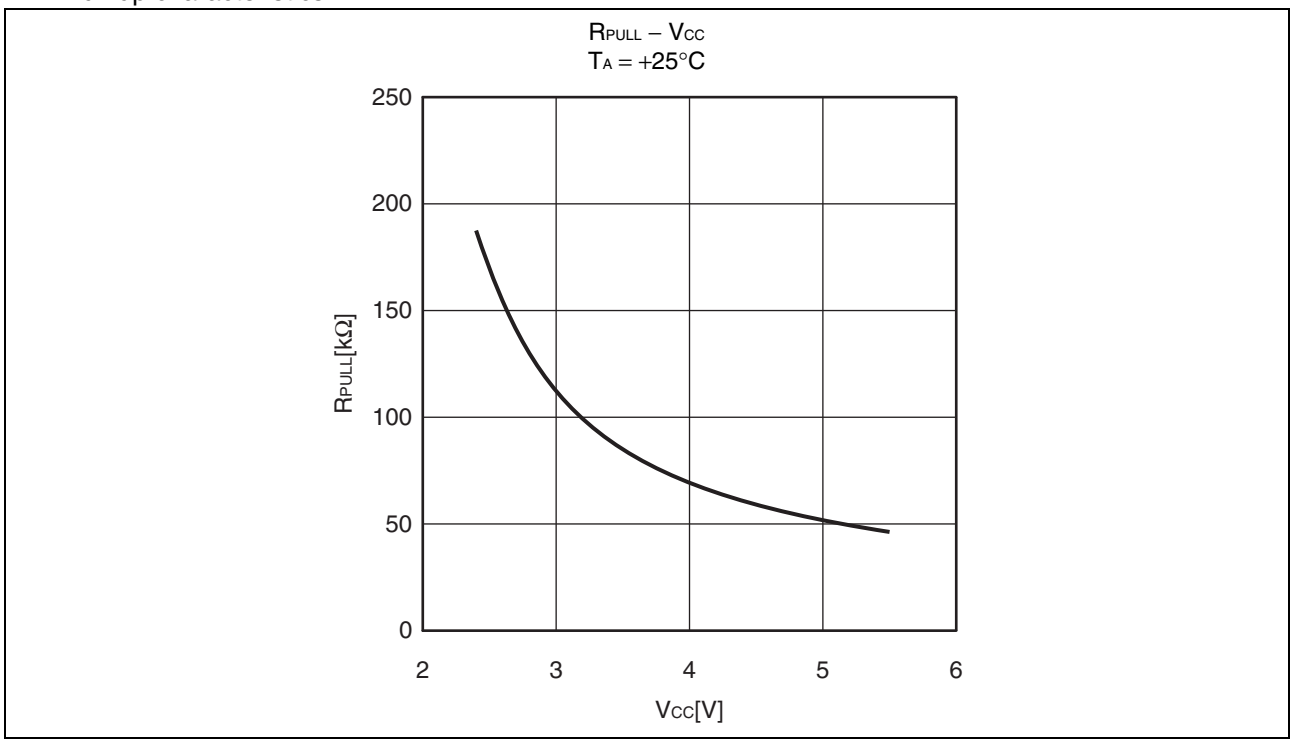
V_{IHM} – V_{CC} and V_{ILM} – V_{CC}
T_A = +25°C



- Output voltage characteristics



- Pull-up characteristics



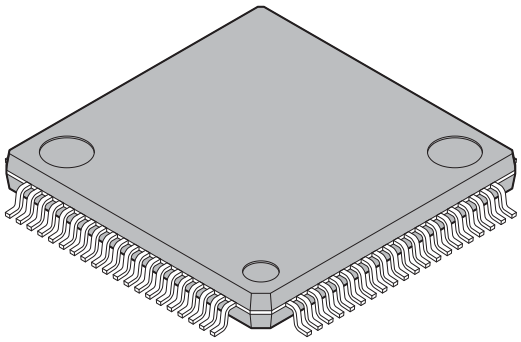
■ MASK OPTIONS

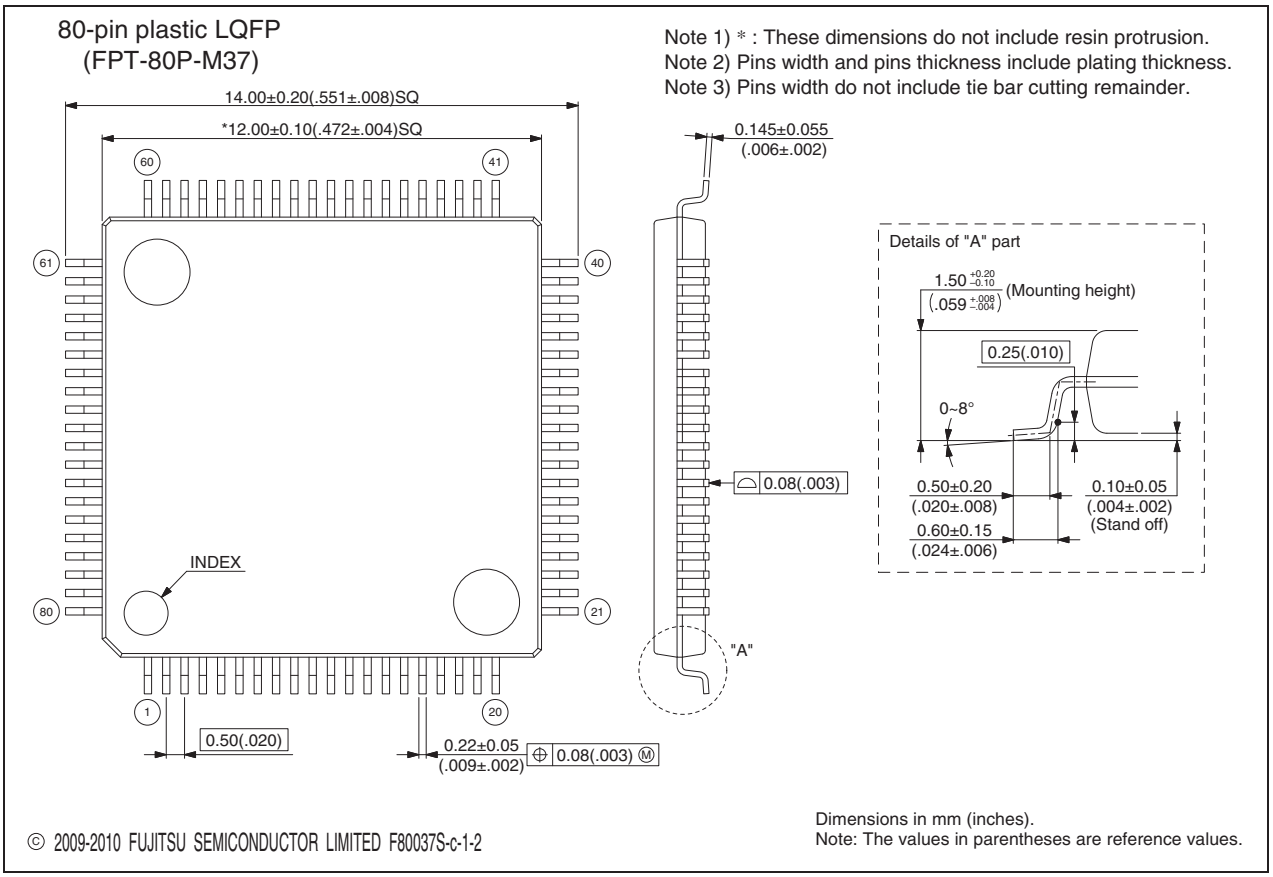
No.	Part Number	MB95F414H MB95F416H MB95F418H MB95F474H MB95F476H MB95F478H	MB95F414K MB95F416K MB95F418K MB95F474K MB95F476K MB95F478K
	Selectable/Fixed	Fixed	
1	Low-voltage detection reset	Without low-voltage detection reset	With low-voltage detection reset
2	Reset	With dedicated reset input	Without dedicated reset input

■ ORDERING INFORMATION

Part Number	Package
MB95F414HPMC-G-SNE2 MB95F414KPMC-G-SNE2 MB95F416HPMC-G-SNE2 MB95F416KPMC-G-SNE2 MB95F418HPMC-G-SNE2 MB95F418KPMC-G-SNE2	80-pin plastic LQFP (FPT-80P-M37)
MB95F474HPMC1-G-SNE2 MB95F474KPMC1-G-SNE2 MB95F476HPMC1-G-SNE2 MB95F476KPMC1-G-SNE2 MB95F478HPMC1-G-SNE2 MB95F478KPMC1-G-SNE2	64-pin plastic LQFP (FPT-64P-M38)
MB95F474HPMC2-G-SNE2 MB95F474KPMC2-G-SNE2 MB95F476HPMC2-G-SNE2 MB95F476KPMC2-G-SNE2 MB95F478HPMC2-G-SNE2 MB95F478KPMC2-G-SNE2	64-pin plastic LQFP (FPT-64P-M39)

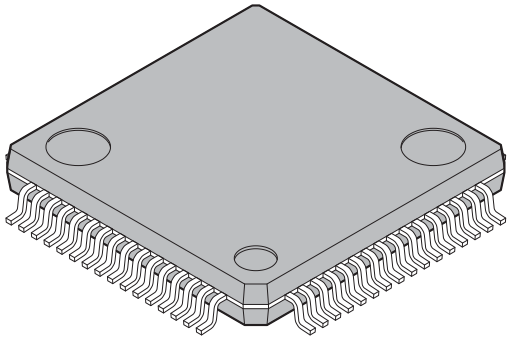
■ PACKAGE DIMENSION

80-pin plastic LQFP		
 (FPT-80P-M37)	Lead pitch	0.50 mm
	Package width × package length	12.00 mm × 12.00 mm
	Lead shape	Gullwing
	Lead bend direction	Normal bend
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.47 g



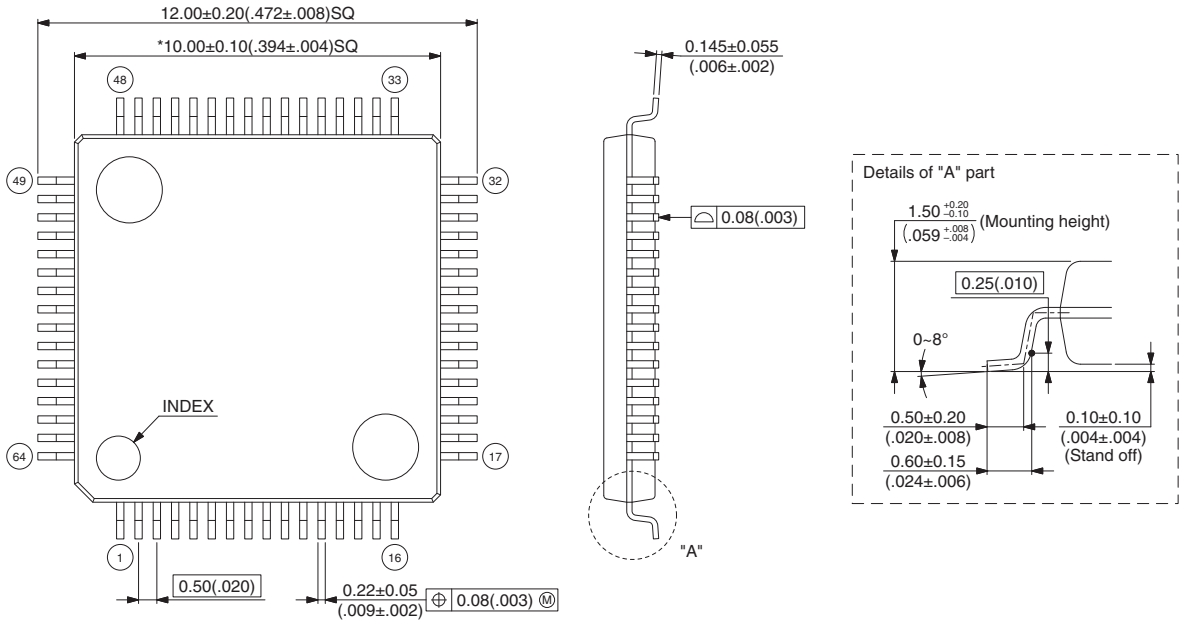
Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

(Continued)

64-pin plastic LQFP		
	Lead pitch	0.50 mm
	Package width × package length	10.00 mm × 10.00 mm
	Lead shape	Gullwing
	Lead bend direction	Normal bend
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
(FPT-64P-M38)	Weight	0.32 g

64-pin plastic LQFP
(FPT-64P-M38)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



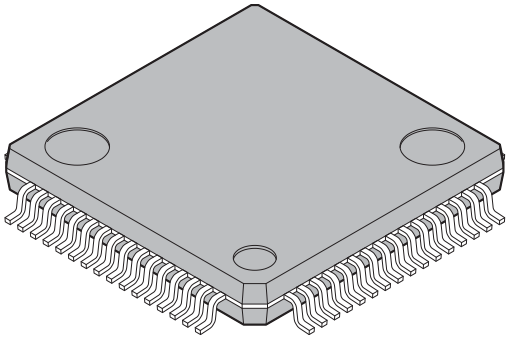
© 2010 FUJITSU SEMICONDUCTOR LIMITED F64038S-c-1-2

Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

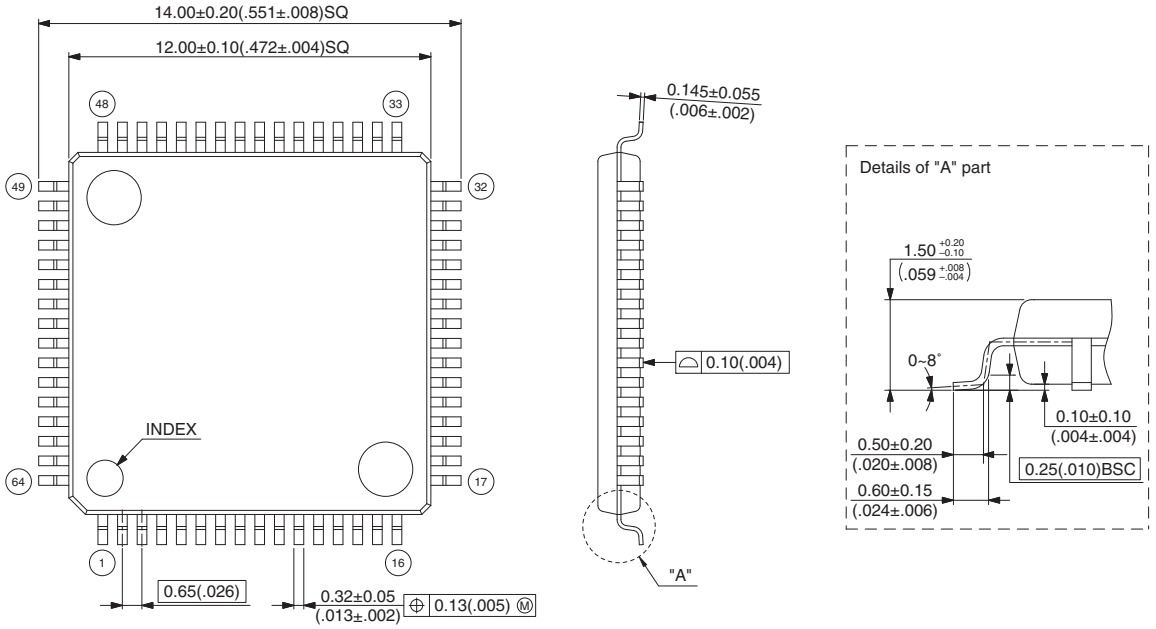
(Continued)

(Continued)

64-pin plastic LQFP		
 (FPT-64P-M39)	Lead pitch	0.65 mm
	Package width × package length	12.00 mm × 12.00 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.47 g

64-pin plastic LQFP
(FPT-64P-M39)

Note 1) Pins width and pins thickness include plating thickness.



© 2010-2011 FUJITSU SEMICONDUCTOR LIMITED HMbF64-39Sc-2-2

Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

■ MAJOR CHANGES IN THIS EDITION

A change on a page is indicated by a vertical line drawn on the left side of that page.

Page	Section	Details
1	—	Changed the family name. F²MC-8FX → New 8FX
49 to 51	■ ELECTRICAL CHARACTERISTICS 3. DC Characteristics	Changed the values of the following power supply current parameters: I_{CC}, I_{CCS}, I_{CCL}, I_{CCLS}, I_{CCT}, I_{CCMPLL}, I_{CCMCR}, I_{CCSCR}, I_{CCTS}, I_{CCH}, I_A, I_V, I_{LVD}.
52	■ ELECTRICAL CHARACTERISTICS 4. AC Characteristics (1) Clock Timing	Changed the values of the clock frequency (F_{CRH}).
64	■ ELECTRICAL CHARACTERISTICS 4. AC Characteristics (8) I²C Timing	Changed the settings related to the machine clock shown in *2.
71 to 76	■ SAMPLE CHARACTERISTICS	Added “■ SAMPLE CHARACTERISTICS”.

MEMO

FUJITSU SEMICONDUCTOR LIMITED

Nomura Fudosan Shin-yokohama Bldg. 10-23, Shin-yokohama 2-Chome,
Kohoku-ku Yokohama Kanagawa 222-0033, Japan
Tel: +81-45-415-5858
http://jp.fujitsu.com/fsl/en/

For further information please contact:

North and South America
FUJITSU SEMICONDUCTOR AMERICA, INC.
1250 E. Arques Avenue, M/S 333
Sunnyvale, CA 94085-5401, U.S.A.
Tel: +1-408-737-5600 Fax: +1-408-737-5999
http://us.fujitsu.com/micro/

Europe
FUJITSU SEMICONDUCTOR EUROPE GmbH
Pittlerstrasse 47, 63225 Langen, Germany
Tel: +49-6103-690-0 Fax: +49-6103-690-122
http://emea.fujitsu.com/semiconductor/

Korea
FUJITSU SEMICONDUCTOR KOREA LTD.
902 Kosmo Tower Building, 1002 Daechi-Dong,
Gangnam-Gu, Seoul 135-280, Republic of Korea
Tel: +82-2-3484-7100 Fax: +82-2-3484-7111
http://kr.fujitsu.com/fsk/

Asia Pacific
FUJITSU SEMICONDUCTOR ASIA PTE. LTD.
151 Lorong Chuan,
#05-08 New Tech Park 556741 Singapore
Tel : +65-6281-0770 Fax : +65-6281-0220
http://www.fujitsu.com/sg/services/micro/semiconductor/

FUJITSU SEMICONDUCTOR SHANGHAI CO., LTD.
Rm. 3102, Bund Center, No.222 Yan An Road (E),
Shanghai 200002, China
Tel : +86-21-6146-3688 Fax : +86-21-6335-1605
http://cn.fujitsu.com/fss/

FUJITSU SEMICONDUCTOR PACIFIC ASIA LTD.
10/F., World Commerce Centre, 11 Canton Road,
Tsimshatsui, Kowloon, Hong Kong
Tel : +852-2377-0226 Fax : +852-2376-3269
http://cn.fujitsu.com/fsp/

Specifications are subject to change without notice. For further information please contact each office.

All Rights Reserved.
The contents of this document are subject to change without notice.
Customers are advised to consult with sales representatives before ordering.
The information, such as descriptions of function and application circuit examples, in this document are presented solely for the purpose of reference to show examples of operations and uses of FUJITSU SEMICONDUCTOR device; FUJITSU SEMICONDUCTOR does not warrant proper operation of the device with respect to use based on such information. When you develop equipment incorporating the device based on such information, you must assume any responsibility arising out of such use of the information.
FUJITSU SEMICONDUCTOR assumes no liability for any damages whatsoever arising out of the use of the information.
Any information in this document, including descriptions of function and schematic diagrams, shall not be construed as license of the use or exercise of any intellectual property right, such as patent right or copyright, or any other right of FUJITSU SEMICONDUCTOR or any third party or does FUJITSU SEMICONDUCTOR warrant non-infringement of any third-party's intellectual property right or other right by using such information. FUJITSU SEMICONDUCTOR assumes no liability for any infringement of the intellectual property rights or other rights of third parties which would result from the use of information contained herein.
The products described in this document are designed, developed and manufactured as contemplated for general use, including without limitation, ordinary industrial use, general office use, personal use, and household use, but are not designed, developed and manufactured as contemplated (1) for use accompanying fatal risks or dangers that, unless extremely high safety is secured, could have a serious effect to the public, and could lead directly to death, personal injury, severe physical damage or other loss (i.e., nuclear reaction control in nuclear facility, aircraft flight control, air traffic control, mass transport control, medical life support system, missile launch control in weapon system), or (2) for use requiring extremely high reliability (i.e., submersible repeater and artificial satellite).
Please note that FUJITSU SEMICONDUCTOR will not be liable against you and/or any third party for any claims or damages arising in connection with above-mentioned uses of the products.
Any semiconductor devices have an inherent chance of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.
Exportation/release of any products described in this document may require necessary procedures in accordance with the regulations of the Foreign Exchange and Foreign Trade Control Law of Japan and/or US export control laws.
The company names and brand names herein are the trademarks or registered trademarks of their respective owners.

Edited: Sales Promotion Department