

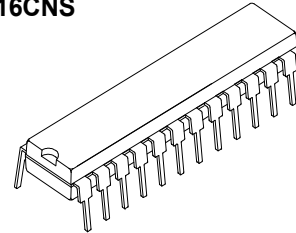
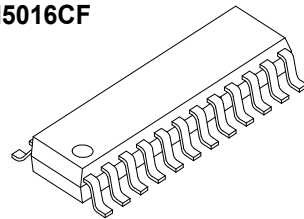
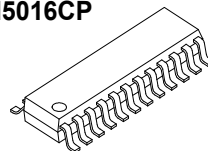
**16-bit Constant Current LED Sink Driver****Features**

- 16 constant-current output channels
- Output current adjustable through an external resistor
- Serial data in/parallel data out
- Output current: 5-90 mA
- 20MHz clock frequency

Product Description

MBI5016, utilizing the most advanced silicon technology, is targeted for LED panel display. MBI5016 contains CMOS shift registers and latch functions, converting serial input data into parallel output format. At the output stage, sixteen regulated current sources, implemented in Bipolar Junction Transistor, were designed to provide 5-90 mA constant current for driving LEDs.

MBI5016 provides users with great flexibility and device performance while using MBI5016 in their LED panel system design. Users may adjust the output current of MBI5016 through an external resistor, R_{ext} , which gives users flexibility in controlling the light intensity of LEDs. MBI5016 guarantees to endure 17V at the output port, allowing users to connect more LEDs in series. The high clock frequency, 20 MHz, also satisfies the system requirement of high volume data transmission.

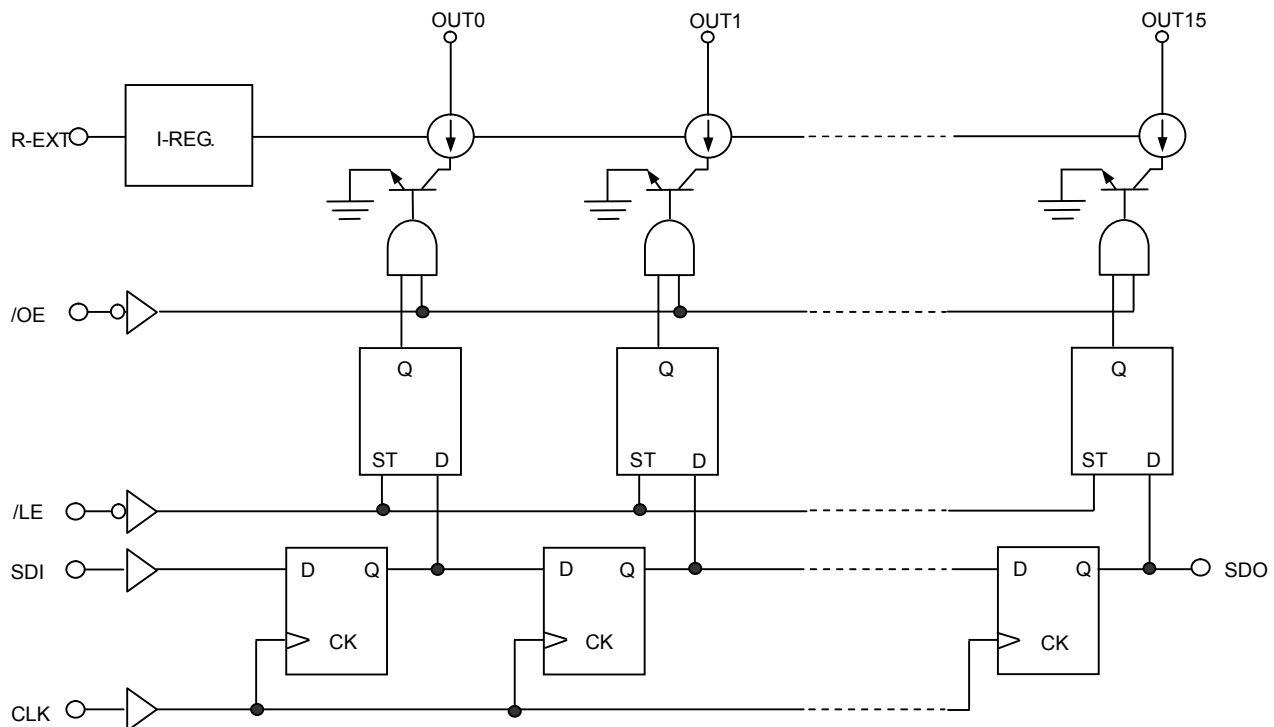
MBI5016CNS**SDIP24-P-300-1.78****Weight: 1.11g(typ)****MBI5016CF****SOP24-P-300-1.00****Weight: 0.28g(typ)****MBI5016CP****SSOP24-P-150-0.64****Weight: 0.11g(typ)**

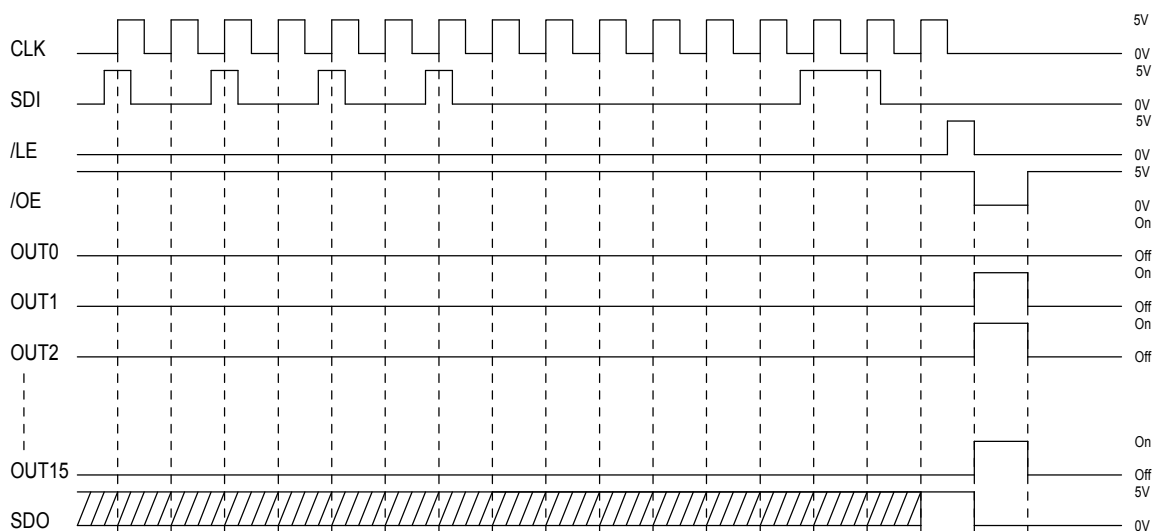
Terminal Description

PIN NO.	PIN NAME	FUNCTION
1	GND	Ground terminal for control logic and current sink
2	SDI	Serial-data input to the shift register
3	CLK	Clock input terminal for data shift on rising edge
4	/LE	Data strobe input terminal Serial data is transferred to the output latch when /LE is high. The data is latched when /LE goes low.
5~20	OUT0~OUT15	Constant current output terminals
21	/OE	Output enable terminal When (active) low, the output drivers are enabled; when high, all output drivers are turned OFF (blanked).
22	SDO	Serial-data output to the following SDI of next driver IC
23	R-EXT	Input terminal used to connect an external resistor for setting up output current for all output channels
24	VDD	5V supply voltage terminal

Pin Description

GND	1	24	VDD
SDI	2	23	R-EXT
CLK	3	22	SDO
/LE	4	21	/OE
OUT0	5	20	OUT15
OUT1	6	19	OUT14
OUT2	7	18	OUT13
OUT3	8	17	OUT12
OUT4	9	16	OUT11
OUT5	10	15	OUT10
OUT6	11	14	OUT9
OUT7	12	13	OUT8

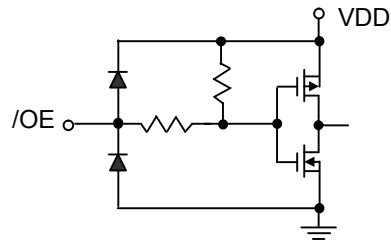
Block Diagram

Timing Diagram**Truth Table**

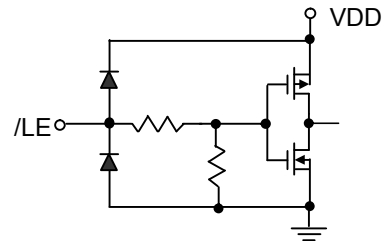
CLK	/LE	/OE	SDI	OUT0...OUT7...OUT15	SDO
UP	H	L	D_n	D_n D_{n-7} D_{n-15}	D_{n-15}
UP	L	L	D_{n+1}	No Change	D_{n-14}
UP	H	L	D_{n+2}	D_{n+2} D_{n-5} D_{n-13}	D_{n-13}
DOWN	X	L	D_{n+3}	D_{n+2} D_{n-5} D_{n-13}	D_{n-13}
DOWN	X	H	D_{n+3}	Off	D_{n-13}

Equivalent Circuits of Inputs and Outputs

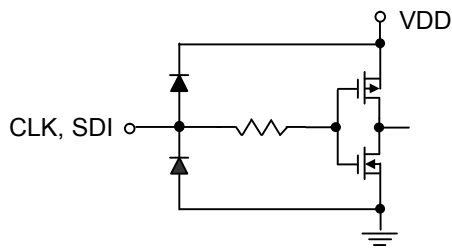
/OE terminal



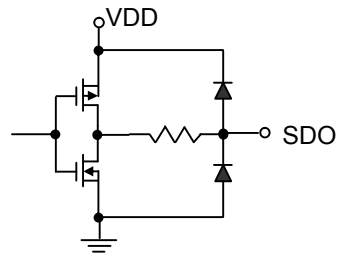
/LE terminal



CLK, SDI terminal



SDO terminal



Maximum Ratings

CHARACTERISTIC		SYMBOL	RATING	UNIT
Supply Voltage		V_{DD}	0~+7.0	V
Output Voltage		V_{CE}	-0.5~+17.0	V
Output Current		I_{OUT}	+90	mA
Input Voltage		V_{IN}	-0.4~ V_{DD} +0.4	V
GND Terminal Current		I_{GND}	1440	mA
Clock Frequency		F_{CLK}	20	MHz
Power Dissipation (ON PCB, $T_a=25^{\circ}\text{C}$)	CNS – type	P_D	1.52	W
	CF – type		1.30	
	CP – type		1.11	
Thermal Resistance (ON PCB, $T_a=25^{\circ}\text{C}$)	CNS – type	$R_{th(j-a)}$	82	$^{\circ}\text{C/W}$
	CF – type		96	
	CP – type		112	
Operating Temperature		T_{opr}	-40~+85	$^{\circ}\text{C}$
Storage Temperature		T_{stg}	-55~+150	$^{\circ}\text{C}$

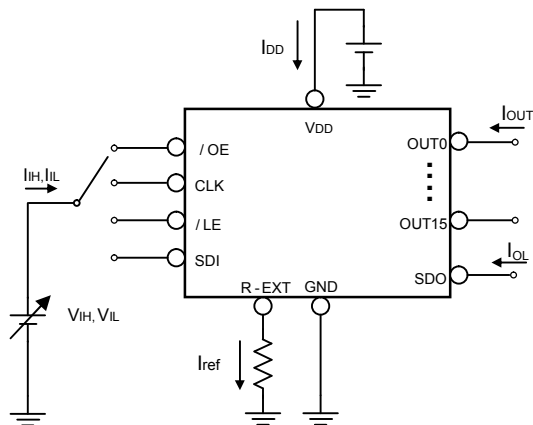
Recommended Operating Condition

CHARACTERISTIC		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage		V_{DD}	-	4.5	5.0	5.5	V
Output Voltage		V_{CE}	-	-	-	17.0	V
Output Current		I_{OUT}	DC Test Circuit	5	-	90	mA
		I_{OH}	SDO	-	-	-1.0	mA
		I_{OL}	SDO	-	-	1.0	mA
Input Voltage		V_{IH}	-	$0.7V_{DD}$	-	$V_{DD}+0.3$	V
		V_{IL}	-	-0.3	-	$0.3V_{DD}$	V
/LE Pulse Width		$t_{w(L)}$	$V_{DD}=4.5\sim 5.5\text{V}$	25	-	-	ns
CLK Pulse Width		$t_{w(CLK)}$		25	-	-	ns
/OE Pulse Width		$t_{w(OE)}$		400	-	-	ns
Setup Time for DATA		$t_{su(D)}$		20	-	-	ns
Hold Time for DATA		$t_{h(D)}$		15	-	-	ns
Setup Time for LATCH		$t_{su(L)}$		60	-	-	ns
Hold Time for LATCH		$t_{h(L)}$		20	-	-	ns
Clock Frequency		F_{CLK}	Cascade Operation	-	-	20.0	MHz
Power Dissipation	CNS – type	P_D	$T_a=85^{\circ}\text{C}$	-	-	0.79	W
	CF – type					0.67	
	CP – type					0.57	

Electrical Characteristics

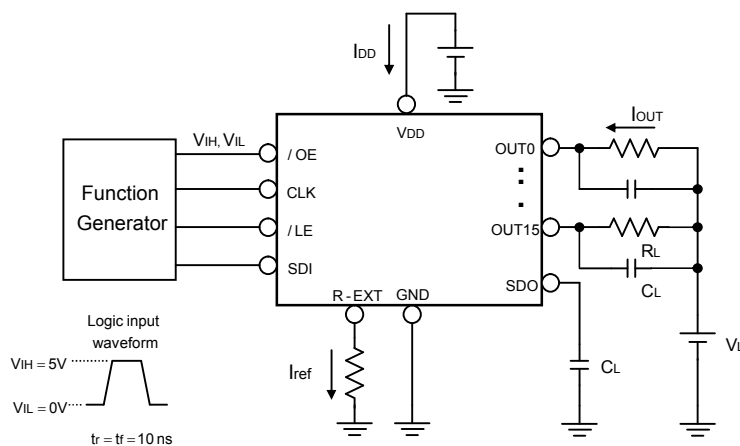
CHRACTERISTIC		SYMBOL	CONDITION		MIN.	TYP.	MAX.	UNIT
Input Voltage	“H” level	V _{IH}	-		0.7V _{DD}	-	V _{DD}	V
	“L” level	V _{IL}	-		GND	-	0.3V _{DD}	
Output Leakage Current		I _{OH}	V _{OH} =17.0V		-	-	10	μA
Output Voltage	SDO	V _{OL}	I _{OL} =+1.0mA		-	-	0.4	V
		V _{OH}	I _{OH} =-1.0mA		4.6	-	-	V
Output Current 1		I _{OUT1}	V _{CE} =0.8V	R _{ext} = 865 Ω (Include Skew)	-	40.0	-	mA
Current Skew		dI _{OUT1}	I _{OL} =40mA V _{CE} =0.8V	R _{ext} = 865 Ω	-	±1.5	±6.0	%
Output Current 2		I _{OUT2}	V _{CE} =1.2V	R _{ext} = 330 Ω (Include Skew)	-	80.0	-	mA
Current Skew		dI _{OUT2}	I _{OL} =80mA V _{CE} =1.2V	R _{ext} = 330 Ω	-	±1.5	±6.0	%
Pull-up Resistor		R _{IN} (up)	-		150	300	600	KΩ
Pull-down Resistor		R _{IN} (down)	-		85	200	400	KΩ
Supply Current	“OFF”	I _{DD} (off) 1	R _{ext} = OPEN, OUT0~15=Off		-	0.1	1.0	mA
		I _{DD} (off) 2	R _{ext} = 865 Ω, OUT0~15=Off		0.1	0.2	1.0	
		I _{DD} (off) 3	R _{ext} = 330 Ω, OUT0~15=Off		0.1	0.2	1.0	
	“ON”	I _{DD} (on) 1	R _{ext} = 865 Ω, OUT0~15=On		10	16	22	
		I _{DD} (on) 2	R _{ext} = 330 Ω, OUT0~15=On		18	24.3	38.5	

Test Circuit for Electrical Characteristic



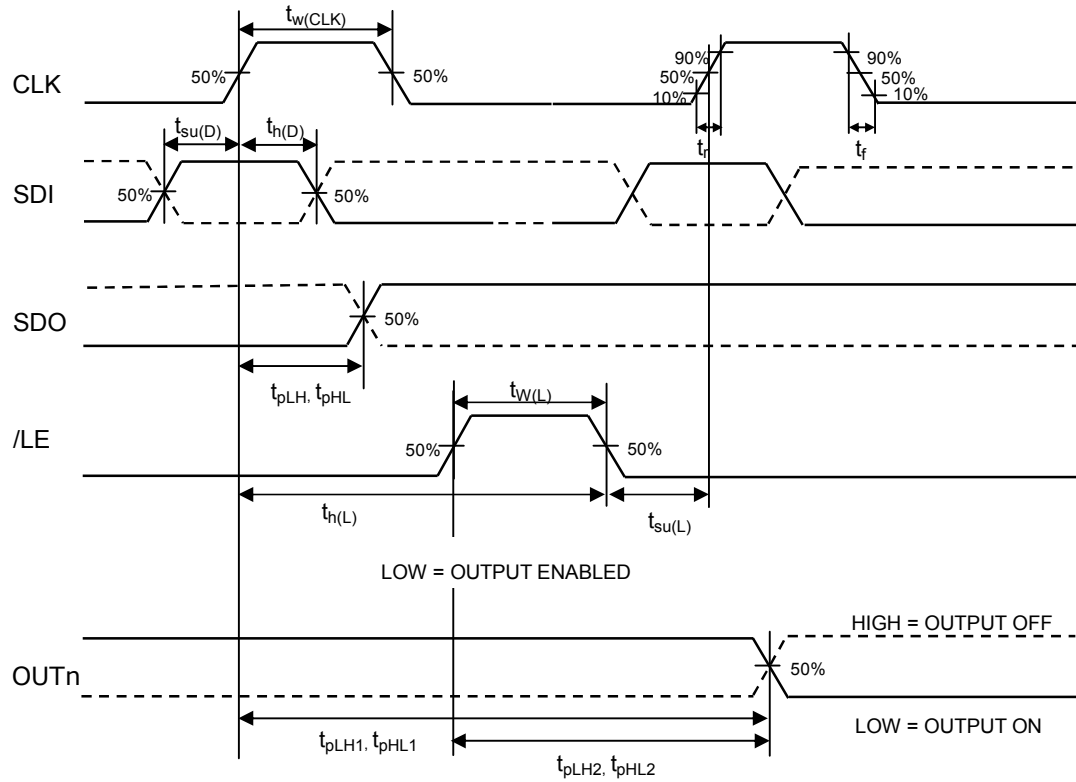
Switching Characteristics

CHARACTERISTIC		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay Time ("L" to "H")	CLK - OUTn	t_{pLH1}	$V_{DD}=5.0V$ $V_{CE}=0.8V$ $V_{IH}=V_{DD}$ $V_{IL}=GND$ $R_{ext} = 865 \Omega$ $V_L=3.4V$ $R_L=65 \Omega$ $C_L=10.5pF$	-	200	300	ns
	/LE - OUTn	t_{pLH2}		-	200	300	ns
	/OE - OUTn	t_{pLH3}		-	200	300	ns
	CLK - SDO	t_{pLH}		20	50	70	ns
Propagation Delay Time ("H" to "L")	CLK - OUTn	t_{pHL1}		-	200	300	ns
	/LE - OUTn	t_{pHL2}		-	200	300	ns
	/OE - OUTn	t_{pHL3}		-	200	300	ns
	CLK - SDO	t_{pHL}		20	50	70	ns
Pulse Width	CLK	$t_{w(CLK)}$		15	-	-	ns
	/LE	$t_{w(L)}$		20	-	-	ns
Set-up Time for LATCH		$t_{su(L)}$		10	-	-	ns
Hold Time for LATCH		$t_{h(L)}$		10	-	-	ns
Maximum CLK Rise Time		t_r		-	-	500	us
Maximum CLK Fall Time		t_f		-	-	500	us
Output Rise Time		t_{or}		-	150	200	ns
Output Fall Time		t_{of}		-	150	200	ns

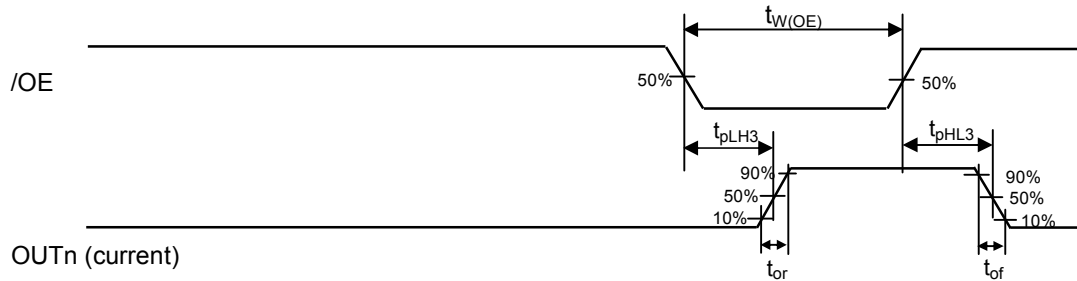
Test Circuit for Switching Characteristic

Timing Waveform

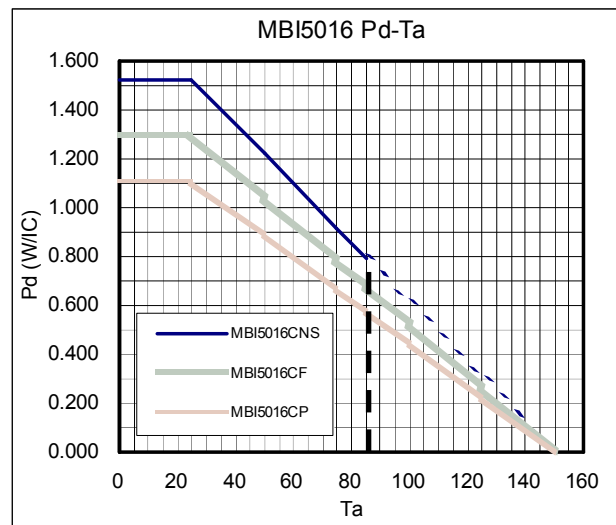
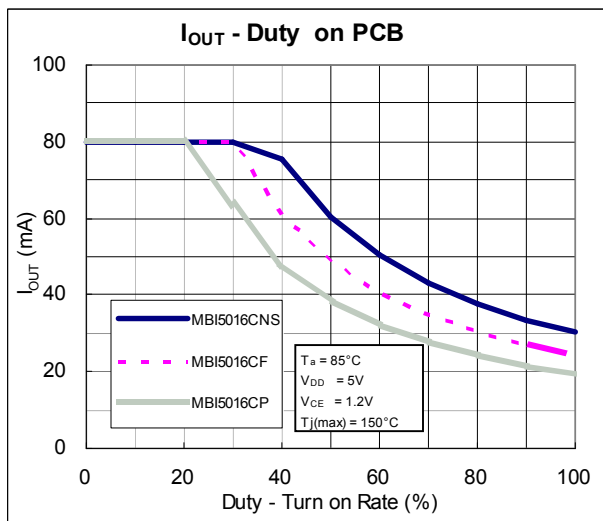
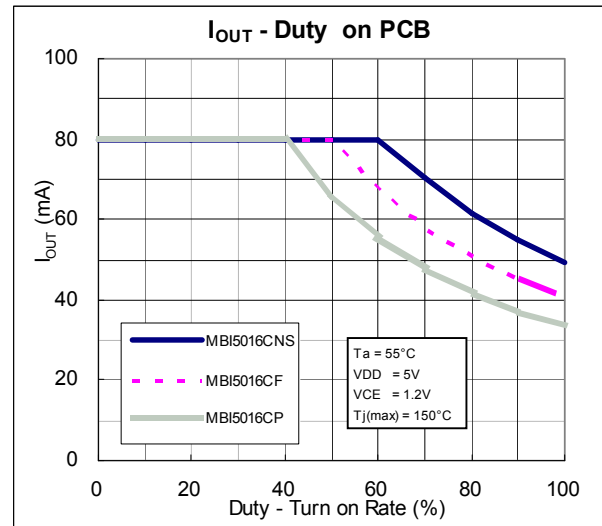
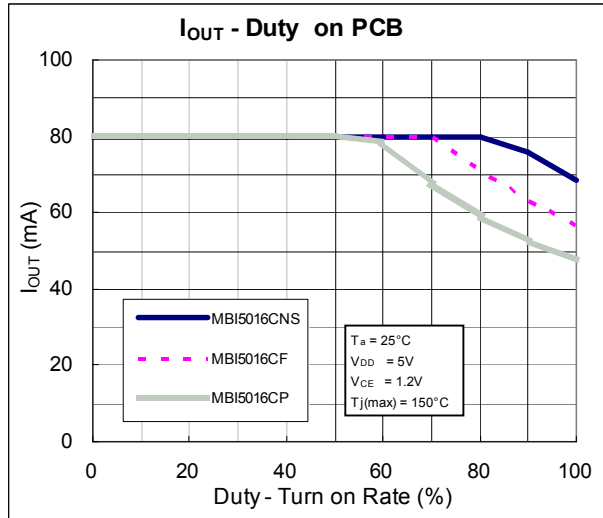
1. CLK, SDO, /LE, OUTn



2. /OE, OUTn

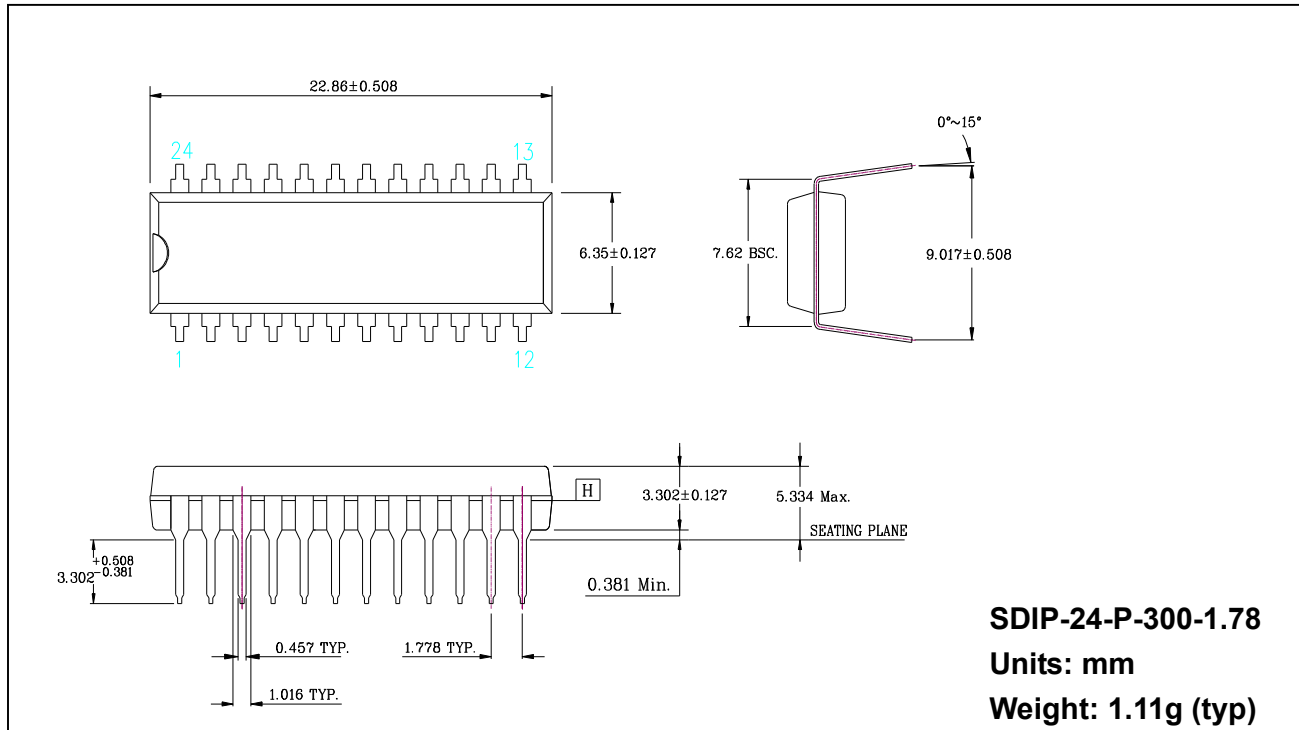


Graphs

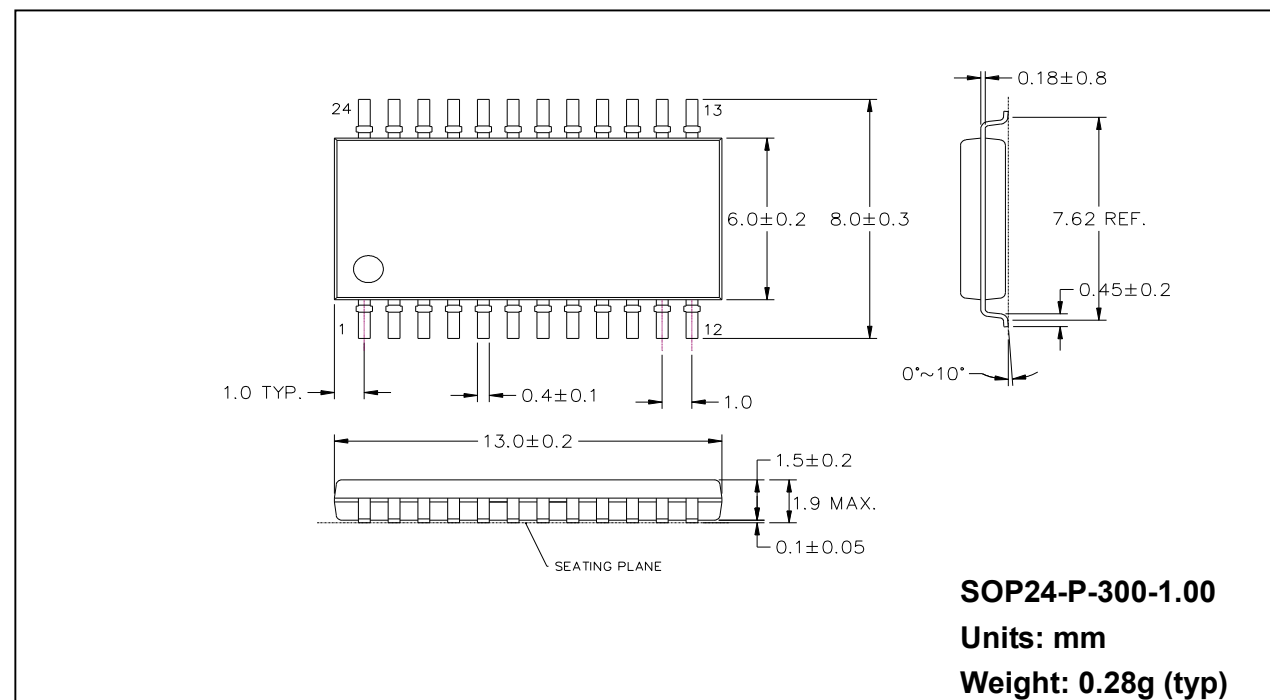


Outline Drawings

MBI5016CNS



MBI5016CF



MBI5016CP

