

**16-Channel Constant Current LED Sink Driver****Features**

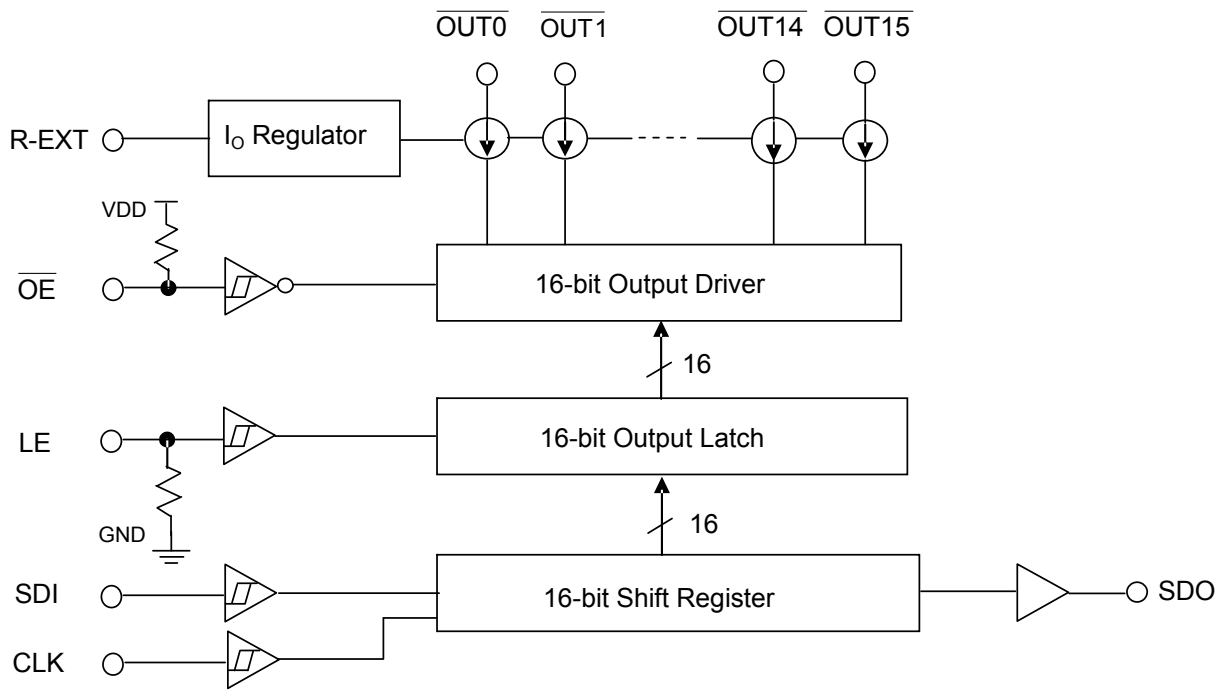
- 16 constant-current output channels
- Constant output current invariant to load voltage change:  
Constant output current range:  
3-30mA@ $V_{DD}=5V$ ;  
3-15mA@ $V_{DD}=3.3V$
- Excellent output current accuracy  
between channels:  $\pm 1.5\%$  (typ.) and  $\pm 2.5\%$  (max.)  
between ICs:  $\pm 1.5\%$  (typ.) and  $\pm 3.0\%$  (max.)
- Output current adjusted through an external resistor
- Fast response of output current,  $\overline{OE}$  (min.): 45ns with good uniformity  
between output channels
- 25MHz clock frequency
- Schmitt trigger input
- 3.3V/ 5V supply voltage
- Package MSL Level:3
- RoHS compliant package

**Product Description**

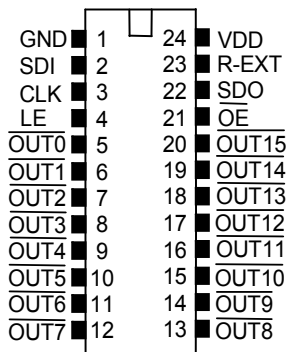
With PrecisionDrive™ technology, MBI5020 is designed for LED displays which require to operate at low current and to match the luminous intensity of each channel. It provides supply voltage and accepts CMOS logic input at 3.3V and 5.0V to meet the trend of low power consumption. MBI5020 contains a serial buffer and data latches which convert serial input data into parallel output format. At MBI5020 output stage, sixteen regulated current ports are designed to provide uniform and constant current sinks for driving LEDs within a large range of  $V_F$  variations.

MBI5020 provides users with great flexibility and device performance while using MBI5020 in their system design for LED display applications, e.g. LED panels. It accepts an input voltage range from 3V to 5.5V and maintains a constant current up from 3mA to 30mA determined by an external resistor,  $R_{ext}$ , which gives users flexibility in controlling the light intensity of LEDs. MBI5020 guarantees to endure maximum 17V at the output port. The high clock frequency, 25 MHz, also satisfies the system requirements of high volume data transmission.

Block Diagram



**Pin Configuration**



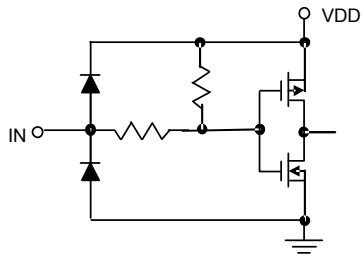
MBI5020GP

**Terminal Description**

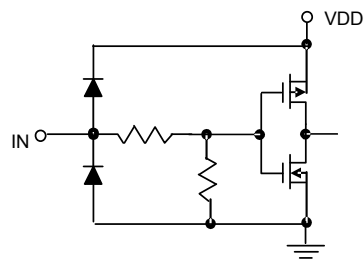
Pin Name	Function
GND	Ground terminal for control logic and current sink
SDI	Serial-data input to the shift register
CLK	Clock input terminal for data shift on rising edge
LE	Data strobe input terminal Serial data is transferred to the output latch when LE is high. The data is latched when LE goes low.
OUT0 ~ OUT15	Constant current output terminals
OE	Output enable terminal When OE (active) low $\overline{OUT0} \sim \overline{OUT15}$ are enabled. When OE high $\overline{OUT0} \sim \overline{OUT15}$ are turned OFF (blanked).
SDO	Serial-data output to the following SDI of next driver IC
R-EXT	Input terminal used to connect an external resistor for setting up output current for all output channels
VDD	3.3V/5V supply voltage terminal

**Equivalent Circuits of Inputs and Outputs**

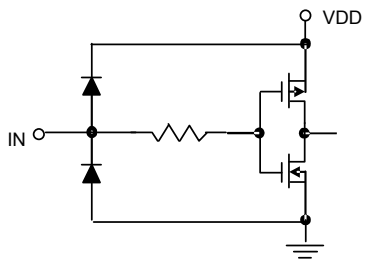
**OE terminal**



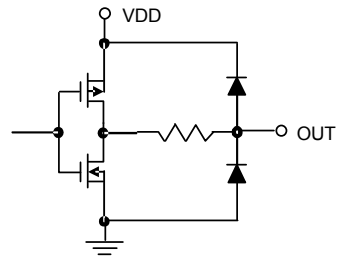
**LE terminal**



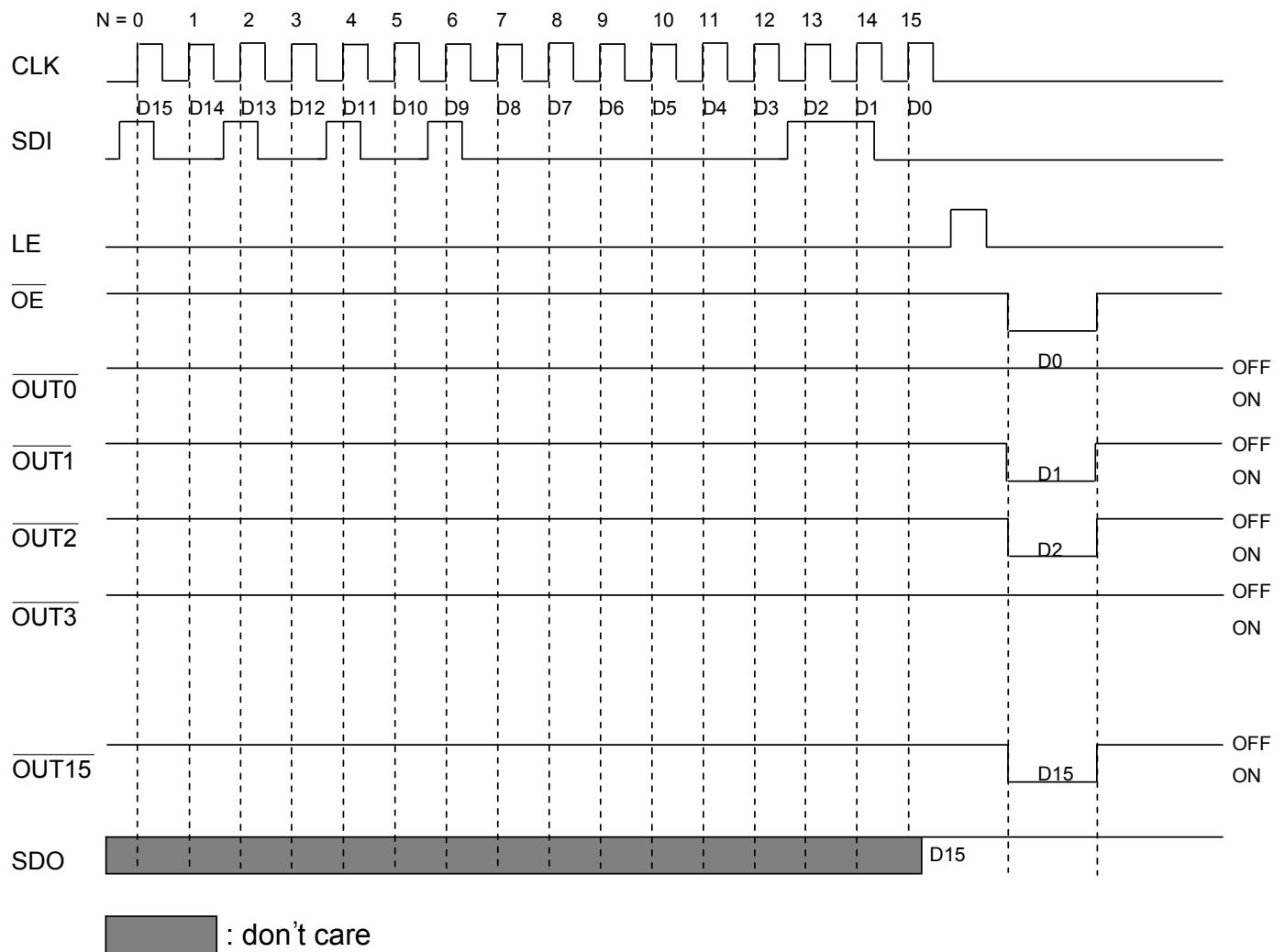
**CLK, SDI terminal**



**SDO terminal**



**Timing Diagram**



**Truth Table**

CLK	LE	OE	SDI	OUT0 ... OUT7 ... OUT15	SDO
	H	L	D <sub>n</sub>	$\overline{D_n} \dots \overline{D_{n-7}} \dots \overline{D_{n-15}}$	D <sub>n-15</sub>
	L	L	D <sub>n+1</sub>	No Change	D <sub>n-14</sub>
	H	L	D <sub>n+2</sub>	$\overline{D_{n+2}} \dots \overline{D_{n-5}} \dots \overline{D_{n-13}}$	D <sub>n-13</sub>
	X	L	D <sub>n+3</sub>	$\overline{D_{n+2}} \dots \overline{D_{n-5}} \dots \overline{D_{n-13}}$	D <sub>n-13</sub>
	X	H	D <sub>n+3</sub>	Off	D <sub>n-13</sub>

Maximum Ratings

Characteristic		Symbol	Rating	Unit
Supply Voltage		$V_{DD}$	0~7.0	V
Input Voltage (SDI, CLK, LE, GCLK)		$V_{IN}$	-0.4~ $V_{DD}+0.4$	V
Output Current		$I_{OUT}$	+35	mA
Sustaining Voltage at OUT Port		$V_{DS}$	-0.5~+17.0	V
GND Terminal Current		$I_{GND}$	560	mA
Power Dissipation (On PCB, Ta= 25°C)*	GP-type	$P_D$	1.76	W
Thermal Resistance(On PCB, Ta= 25°C)*	GP-type	$R_{th(j-a)}$	70.90	°C/W
Operating Junction Temperature		$T_{j,max}$	150**	°C
Operating Ambient Temperature		$T_{opr}$	-40~+85	°C
Storage Temperature		$T_{stg}$	-55 ~ +150	°C
ESD Rating	HBM (MIL-STD-883G Method 3015.8, Human Body Mode)	-	Class 3A (6KV)	-
	MM (ANSI/ ESD S5.2-2009, Machine Mode)	-	Class M4 (500V)	-

\* The PCB size is 76.2mm\*114.3mm in simulation. Please refer to JEDEC JESD51.

\*\* Operation at the maximum rating for extended periods may reduce the device reliability; therefore, the suggested junction temperature of the device is under 125°C.

Note: The performance of thermal dissipation is strongly related to the size of thermal pad, thickness and layer numbers of the PCB. The empirical thermal resistance may be different from simulative value. Users should plan for expected thermal dissipation performance by selecting package and arranging layout of the PCB to maximize the capability.

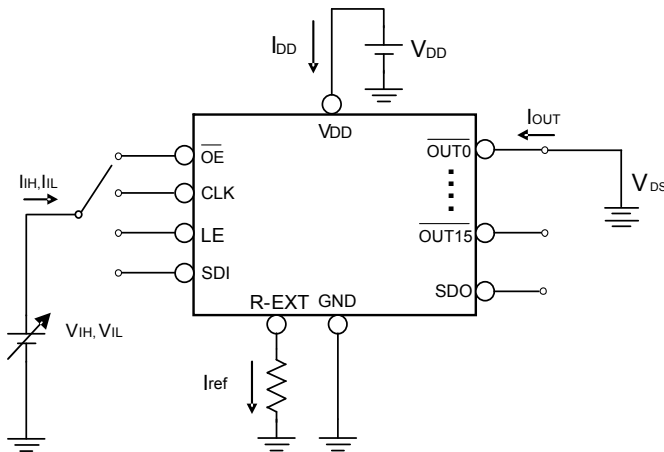
**Electrical Characteristics (V<sub>DD</sub> = 5.0V)**

Characteristics		Symbol	Condition		Min.	Typ.	Max.	Unit
Supply Voltage		V <sub>DD</sub>	-		4.5	5.0	5.5	V
Output Voltage		V <sub>DS</sub>	$\overline{\text{OUT0}} \sim \overline{\text{OUT15}}$		-	-	17	V
Output Current		I <sub>OUT</sub>	Refer to „Test Circuit for Electrical Characteristics”		3.0	-	30	mA
		I <sub>OH</sub>	SDO		-	-1.0	-	mA
		I <sub>OL</sub>	SDO		-	1.0	-	mA
Input Voltage	„H” level	V <sub>IH</sub>	T <sub>a</sub> =-40~85°C		0.7 x V <sub>DD</sub>	-	V <sub>DD</sub>	V
	„L” level	V <sub>IL</sub>	T <sub>a</sub> =-40~85°C		GND	-	0.3 x V <sub>DD</sub>	V
Output Leakage Current		I <sub>OH</sub>	V <sub>DS</sub> =17.0V		-	-	0.5	μA
Output Voltage	SDO	V <sub>OL</sub>	I <sub>OL</sub> =+1.0mA		-	-	0.4	V
		V <sub>OH</sub>	I <sub>OH</sub> =-1.0mA		V <sub>DD</sub> -0.4	-	-	V
Output Current 1		I <sub>OUT1</sub>	V <sub>DS</sub> =1.0V	R <sub>ext</sub> =1240 Ω	-	15	-	mA
Current Skew		dI <sub>OUT1</sub>	I <sub>OL</sub> =15mA V <sub>DS</sub> =1.0V	R <sub>ext</sub> =1240 Ω	-	±1.5	±2.5	%
Current Skew		dI <sub>OUT2</sub>	I <sub>OL</sub> =15mA V <sub>DS</sub> =1.0V	R <sub>ext</sub> =1240 Ω	-	±1.5	±3.0	%
Output Current vs. Output Voltage Regulation		%/dV <sub>DS</sub>	V <sub>DS</sub> within 1.0V and 3.0V		-	±0.1	±0.3	%/V
Output Current vs. Supply Voltage Regulation		%/dV <sub>DD</sub>	V <sub>DD</sub> within 4.5V and 5.5V		-	-	±1.0	%/V
Pull-up Resistor		R <sub>IN(up)</sub>	$\overline{\text{OE}}$		200	460	700	KΩ
Pull-down Resistor		R <sub>IN(down)</sub>	LE		200	460	700	KΩ
Supply Current	“OFF”	I <sub>DD(off) 1</sub>	R <sub>ext</sub> = Open , $\overline{\text{OUT0}} \sim \overline{\text{OUT15}}$ =Off		-	2.7	3.7	mA
		I <sub>DD(off) 2</sub>	R <sub>ext</sub> =1240Ω, $\overline{\text{OUT0}} \sim \overline{\text{OUT15}}$ =Off		-	9.7	10.7	
	“ON”	I <sub>DD(on) 1</sub>	R <sub>ext</sub> =1240Ω, $\overline{\text{OUT0}} \sim \overline{\text{OUT15}}$ =On		-	8.5	9.5	

**Electrical Characteristics (V<sub>DD</sub> = 3.3V)**

Characteristics		Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage		V <sub>DD</sub>	-	3.0	3.3	3.6	V
Output Voltage		V <sub>DS</sub>	$\overline{\text{OUT0}} \sim \overline{\text{OUT15}}$	-	-	17	V
Output Current		I <sub>OUT</sub>	Refer to „Test Circuit for Electrical Characteristics”	3.0	-	15	mA
		I <sub>OH</sub>	SDO	-	-1.0	-	mA
		I <sub>OL</sub>	SDO	-	1.0	-	mA
Input Voltage	„H” level	V <sub>IH</sub>	T <sub>a</sub> =-40~85°C	0.7 x V <sub>DD</sub>	-	V <sub>DD</sub>	V
	„L” level	V <sub>IL</sub>	T <sub>a</sub> =-40~85°C	GND	-	0.3 x V <sub>DD</sub>	V
Output Leakage Current		I <sub>OH</sub>	V <sub>DS</sub> =17.0V	-	-	0.5	μA
Output Voltage	SDO	V <sub>OL</sub>	I <sub>OL</sub> =+1.0mA	-	-	0.4	V
		V <sub>OH</sub>	I <sub>OH</sub> =-1.0mA	V <sub>DD</sub> -0.4	-	-	V
Output Current 1		I <sub>OUT1</sub>	V <sub>DS</sub> =1.0V    R <sub>ext</sub> =1240 Ω	-	15	-	mA
Current Skew		dI <sub>OUT1</sub>	I <sub>OL</sub> =15mA V <sub>DS</sub> =1.0V    R <sub>ext</sub> =1240 Ω	-	±1.5	±2.5	%
Current Skew		dI <sub>OUT2</sub>	I <sub>OL</sub> =15mA V <sub>DS</sub> =1.0V    R <sub>ext</sub> =1240 Ω	-	±1.5	±3.0	%
Output Current vs. Output Voltage Regulation		%/dV <sub>DS</sub>	V <sub>DS</sub> within 1.0V and 3.0V	-	±0.1	±0.3	%/V
Output Current vs. Supply Voltage Regulation		%/dV <sub>DD</sub>	V <sub>DD</sub> within 3.0V and 3.6V	-	-	±1.0	%/V
Pull-up Resistor		R <sub>IN(up)</sub>	$\overline{\text{OE}}$	200	460	700	KΩ
Pull-down Resistor		R <sub>IN(down)</sub>	LE	200	460	700	KΩ
Supply Current	“OFF”	I <sub>DD(off) 1</sub>	R <sub>ext</sub> =Open, $\overline{\text{OUT0}} \sim \overline{\text{OUT15}}$ =Off	-	2.5	3.5	mA
		I <sub>DD(off) 2</sub>	R <sub>ext</sub> =1240Ω, $\overline{\text{OUT0}} \sim \overline{\text{OUT15}}$ =Off	-	9.2	10.2	
	“ON”	I <sub>DD(on) 1</sub>	R <sub>ext</sub> =1240Ω, $\overline{\text{OUT0}} \sim \overline{\text{OUT15}}$ =On	-	8.8	9.8	

**Test Circuit for Electrical Characteristics**





**Switching Characteristics (V<sub>DD</sub>= 5.0V)**

Characteristics		Symbol	Condition	Min.	Typ.	Max.	Unit
Propagation Delay Time („L” to „H”)	CLK- $\overline{\text{OUT}}_{2n}$ *	$t_{pLH1}$	V <sub>DD</sub> =5.0V V <sub>DS</sub> =1.0V V <sub>IH</sub> =V <sub>DD</sub> V <sub>IL</sub> =GND R <sub>ext</sub> =930Ω V <sub>L</sub> =4.0V R <sub>L</sub> =150Ω C <sub>L</sub> =10pF	-	37	52	ns
	CLK- $\overline{\text{OUT}}_{2n+1}$ *			-	35	50	ns
	LE- $\overline{\text{OUT}}_{2n}$	$t_{pLH2}$		-	37	52	ns
	LE- $\overline{\text{OUT}}_{2n+1}$			-	35	50	ns
	OE - $\overline{\text{OUT}}_{2n}$	$t_{pLH3}$		-	37	52	ns
	OE - $\overline{\text{OUT}}_{2n+1}$			-	35	50	ns
	CLK-SDO	$t_{pLH}$		-	25	35	ns
Propagation Delay Time („H” to „L”)	CLK- $\overline{\text{OUT}}_{2n}$	$t_{pHL1}$		-	27	37	ns
	CLK- $\overline{\text{OUT}}_{2n+1}$			-	25	35	ns
	LE- $\overline{\text{OUT}}_{2n}$	$t_{pHL2}$		-	22	32	ns
	LE- $\overline{\text{OUT}}_{2n+1}$			-	20	30	ns
	OE - $\overline{\text{OUT}}_{2n}$	$t_{pHL3}$		-	22	32	ns
	OE - $\overline{\text{OUT}}_{2n+1}$			-	20	30	ns
	CLK-SDO	$t_{pHL}$		-	25	35	ns
Pulse Width	CLK	$t_{w(\text{CLK})}$	20	-	-	ns	
	LE	$t_{w(L)}$	20	-	-	ns	
	OE **	$t_{w(\text{OE})}$	45	60	-	ns	
Hold Time for LE		$t_{h(L)}$	30	-	-	ns	
Setup Time for LE		$t_{su(L)}$	5	-	-	ns	
Hold Time for SDI		$t_{h(D)}$	5	-	-	ns	
Setup Time for SDI		$t_{su(D)}$	3	-	-	ns	
Maximum CLK Rise Time		$t_r$	-	-	500	ns	
Maximum CLK Fall Time		$t_f$	-	-	500	ns	
SDO Rise Time		$t_{r,\text{SDO}}$	-	10	-	ns	
SDO Fall Time		$T_{f,\text{SDO}}$	-	10	-	ns	
Output Rise Time of Output Ports		$t_{or}$	-	30	40	ns	
Output Fall Time of Output Ports		$t_{of}$	-	35	45	ns	

\*The staggered delay between odd channels,  $\overline{\text{OUT}}_{2n+1}$  (e.g. OUT1, OUT3, OUT5, etc.) and even channels  $\overline{\text{OUT}}_{2n}$  (e.g. OUT2, OUT4, OUT6, etc.) is 2ns. MBI5020 has a built-in staggered circuit to perform delay mechanism, by which the even and odd output ports will be turned on at a different time so that the instant current from the power line will be lowered.

\*\* With uniform output current.

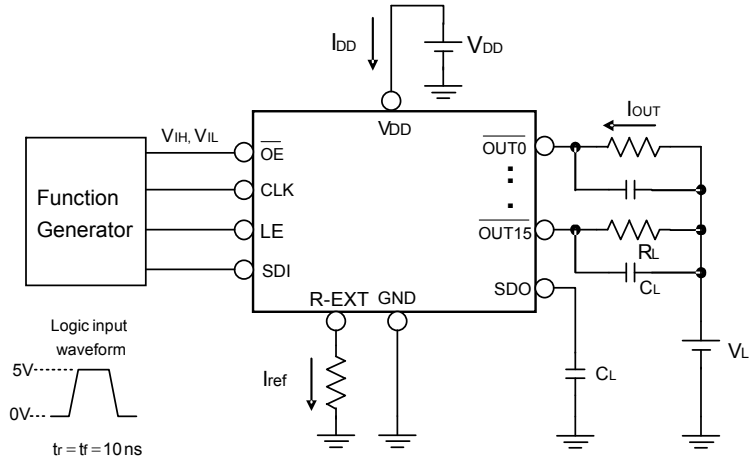
**Switching Characteristics (V<sub>DD</sub>= 3.3V)**

Characteristics		Symbol	Condition	Min.	Typ.	Max.	Unit
Propagation Delay Time („L” to „H”)	CLK-OUT 2n *	t <sub>pLH1</sub>	V <sub>DD</sub> =3.3V V <sub>DS</sub> =1.0V V <sub>IH</sub> =V <sub>DD</sub> V <sub>IL</sub> =GND R <sub>ext</sub> =930Ω V <sub>L</sub> =4.0V R <sub>L</sub> =150Ω C <sub>L</sub> =10 pF	-	52	72	ns
	CLK-OUT 2n + 1 *			-	50	70	ns
	LE-OUT 2n	t <sub>pLH2</sub>		-	52	72	ns
	LE-OUT 2n + 1			-	50	70	ns
	OE - OUT 2n	t <sub>pLH3</sub>		-	52	72	ns
	OE - OUT 2n + 1			-	50	70	ns
	CLK-SDO	t <sub>pLH</sub>		-	35	45	ns
Propagation Delay Time („H” to „L”)	CLK-OUT 2n	t <sub>pHL1</sub>		-	27	37	ns
	CLK-OUT 2n + 1			-	25	35	ns
	LE-OUT 2n	t <sub>pHL2</sub>		-	27	37	ns
	LE-OUT 2n + 1			-	25	35	ns
	OE - OUT 2n	t <sub>pHL3</sub>		-	27	37	ns
	OE - OUT 2n + 1			-	25	35	ns
	CLK-SDO	t <sub>pHL</sub>		-	35	45	ns
Pulse Width	CLK	t <sub>w(CLK)</sub>	20	-	-	ns	
	LE	t <sub>w(L)</sub>	20	-	-	ns	
	OE **	t <sub>w(OE)</sub>	50	65	-	ns	
Hold Time for LE		t <sub>h(L)</sub>	30	-	-	ns	
Setup Time for LE		t <sub>su(L)</sub>	5	-	-	ns	
Hold Time for SDI		t <sub>h(D)</sub>	5	-	-	Ns	
Setup Time for SDI		t <sub>su(D)</sub>	3	-	-	Ns	
Maximum CLK Rise Time		t <sub>r</sub>	-	-	500	Ns	
Maximum CLK Fall Time		t <sub>f</sub>	-	-	500	Ns	
SDO Rise Time		t <sub>r,SDO</sub>	-	10	-	Ns	
SDO Fall Time		T <sub>f,SDO</sub>	-	10	-	Ns	
Output Rise Time of Output Ports		t <sub>or</sub>	-	55	70	Ns	
Output Fall Time of Output Ports		t <sub>of</sub>	-	40	55	ns	

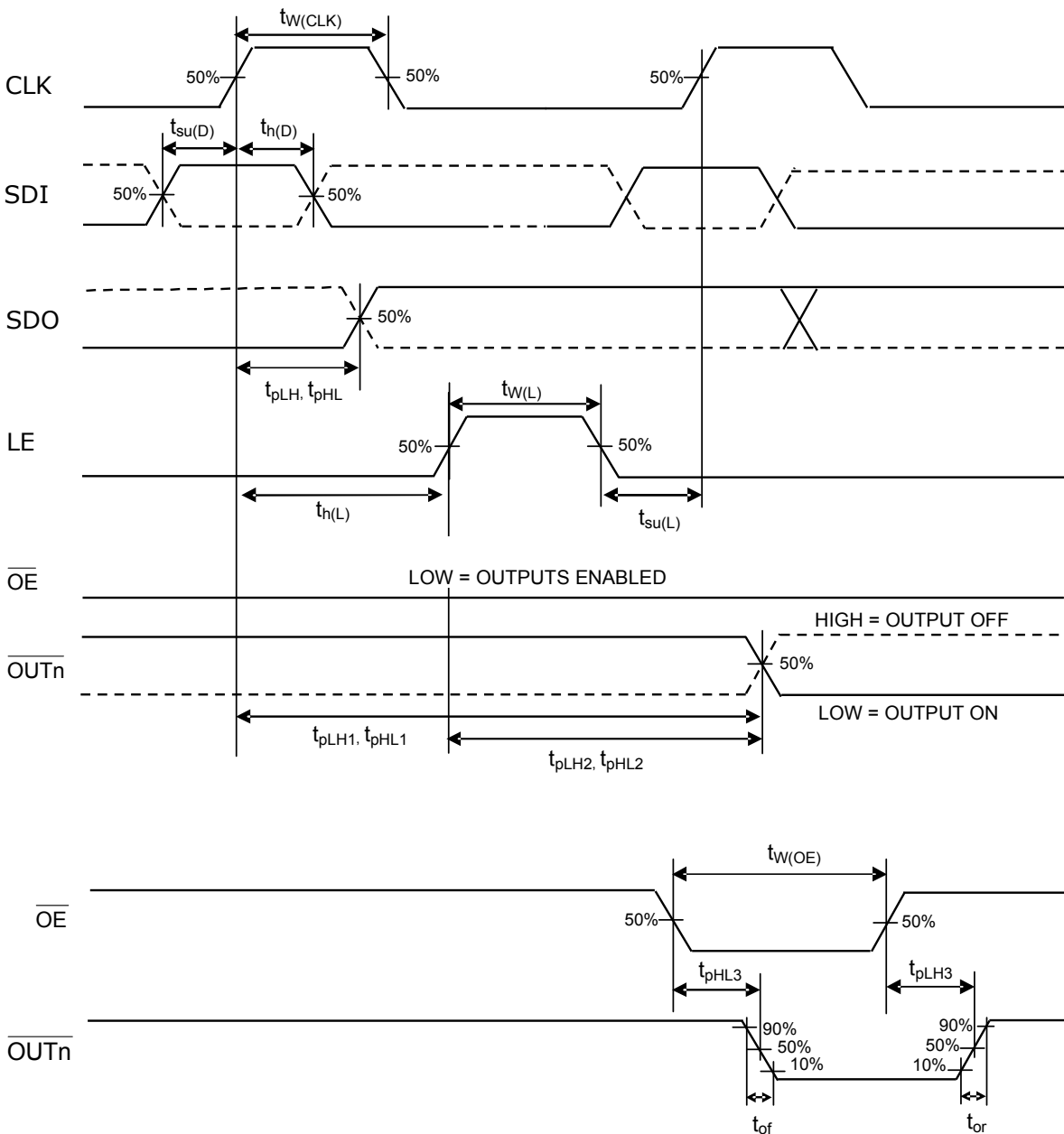
\*The staggered delay between odd channels,  $\overline{OUT2n + 1}$  (e.g. OUT1, OUT3, OUT5, etc.) and even channels  $\overline{OUT2n}$  (e.g. OUT2, OUT4, OUT6, etc.) is 2ns. MBI5020 has a built-in staggered circuit to perform delay mechanism, by which the even and odd output ports will be turned on at a different time so that the instant current from the power line will be lowered.

\*\* With uniform output current.

Test Circuit for Switching Characteristics



Timing Waveform



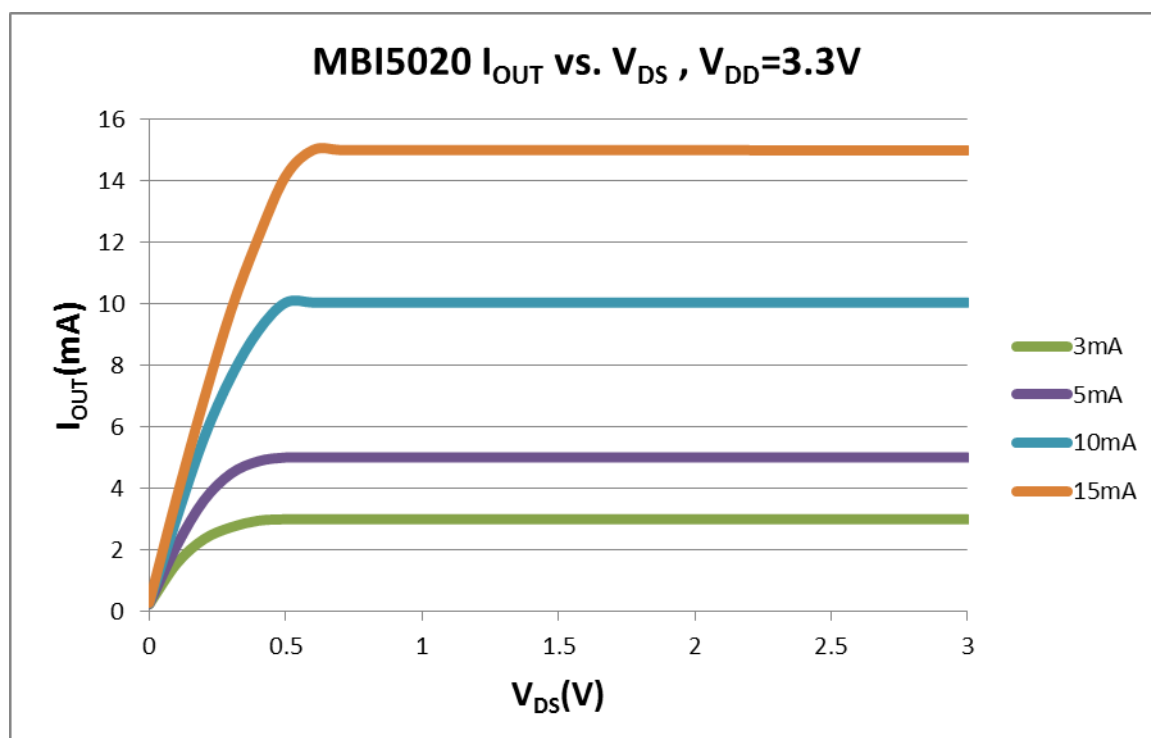
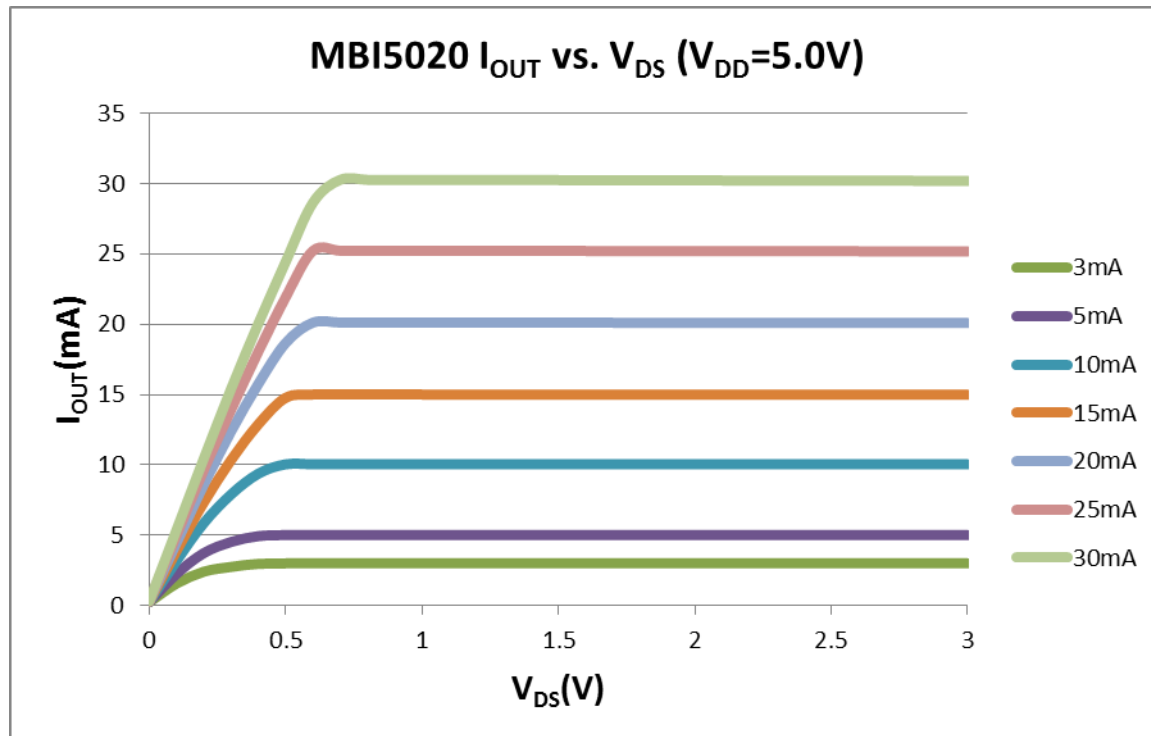
**Application Information**

**Constant Current**

To design LED displays, MBI5020 provides nearly no variations in current from channel to channel and from IC to IC.

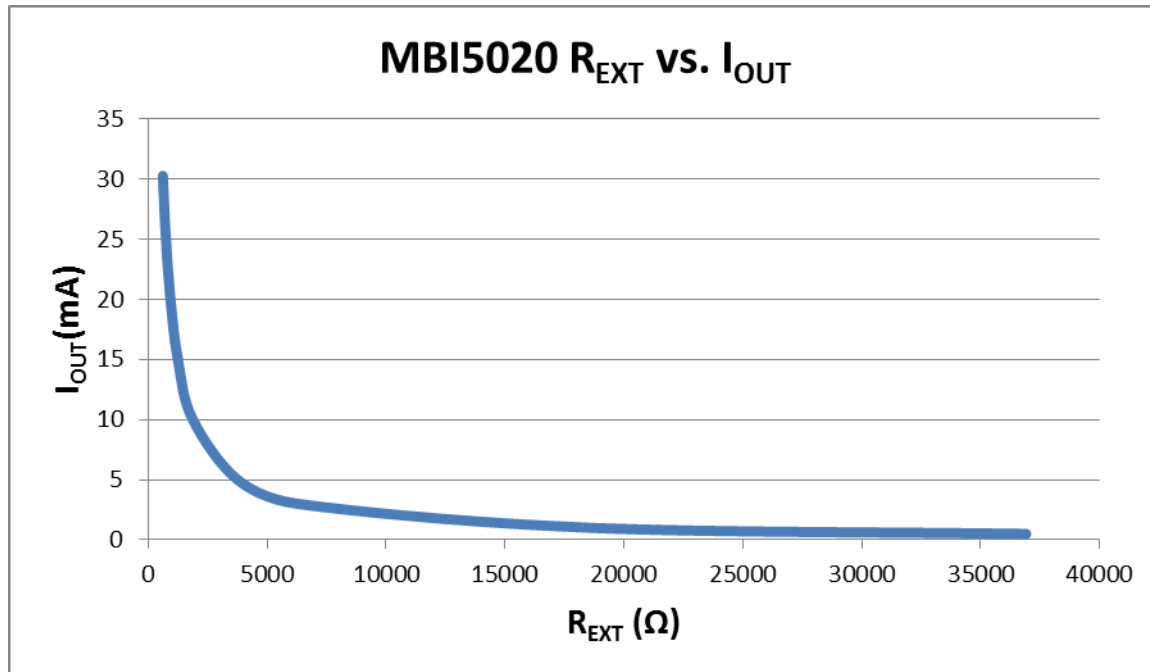
This can be achieved by:

- 1) The maximum current variation between channels is less than  $\pm 2.5\%$ , and that between ICs is less than  $\pm 3\%$ .
- 2) In addition, the current characteristic of output stage is flat and users can refer to the figure as shown below. The output current can be kept constant regardless of the variations of LED forward voltages ( $V_F$ ). This performs as a perfection of load regulation.



**Adjusting Output Current**

The output current of each channel ( $I_{OUT}$ ) is set by an external resistor,  $R_{EXT}$ . The relationship between  $I_{OUT}$  and  $R_{EXT}$  is shown in the following figure.



Also, the output current can be calculated from the equation:

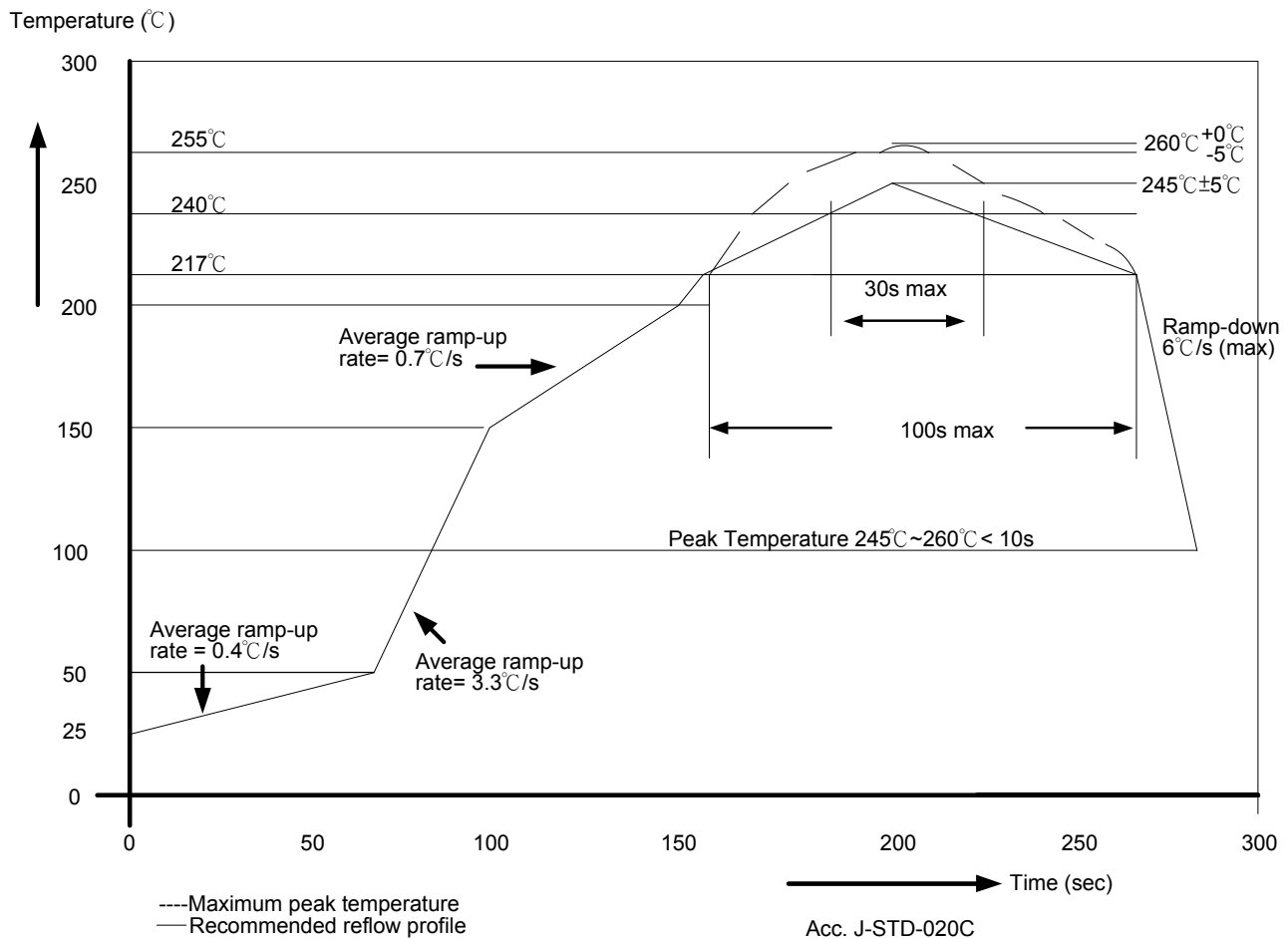
$$V_{R-EXT}=1.24V; I_{OUT}=V_{R-EXT} \cdot (1/R_{EXT}) \times 15; R_{EXT}=(V_{R-EXT}/I_{OUT}) \times 15$$

where  $R_{EXT}$  is the resistance of the external resistor connected to R-EXT terminal and  $V_{R-EXT}$  is the voltage of R-EXT terminal. The magnitude of current (as a function of  $R_{EXT}$ ) is around 25mA at 744Ω and 10mA at 1860Ω.

**Soldering Process of “Pb-free & Green” Package Plating\***

Macroblock has defined "Pb-Free & Green" to mean semiconductor products that are compatible with the current RoHS requirements and selected 100% pure tin (Sn) to provide forward and backward compatibility with both the current industry-standard SnPb-based soldering processes and higher-temperature Pb-free processes. Pure tin is widely accepted by customers and suppliers of electronic devices in Europe, Asia and the US as the lead-free surface finish of choice to replace tin-lead. Also, it adopts tin/lead (SnPb) solder paste, and please refer to the JEDEC J-STD-020C for the temperature of solder bath. However, in the whole Pb-free soldering processes and materials, 100% pure tin (Sn) will all require from 245°C to 260°C for proper soldering on boards, referring to JEDEC J-STD-020C as shown below.

For managing MSL3 Package, it should refer to JEDEC J-STD-0 20C about floor life management & refer to JEDEC J-STD-033C about re-bake condition while IC's floor life exceeds MSL3 limitation.



Package Thickness	Volume mm <sup>3</sup> <350	Volume mm <sup>3</sup> 350-2000	Volume mm <sup>3</sup> ≥ 2000
<1.6mm	260 +0 °C	260 +0 °C	260 +0 °C
1.6mm – 2.5mm	260 +0 °C	250 +0 °C	245 +0 °C
≥2.5mm	250 +0 °C	245 +0 °C	245 +0 °C

\* For details, please refer to Macroblock's “Policy on Pb-free & Green Package”.

**Package Power Dissipation (P<sub>D</sub>)**

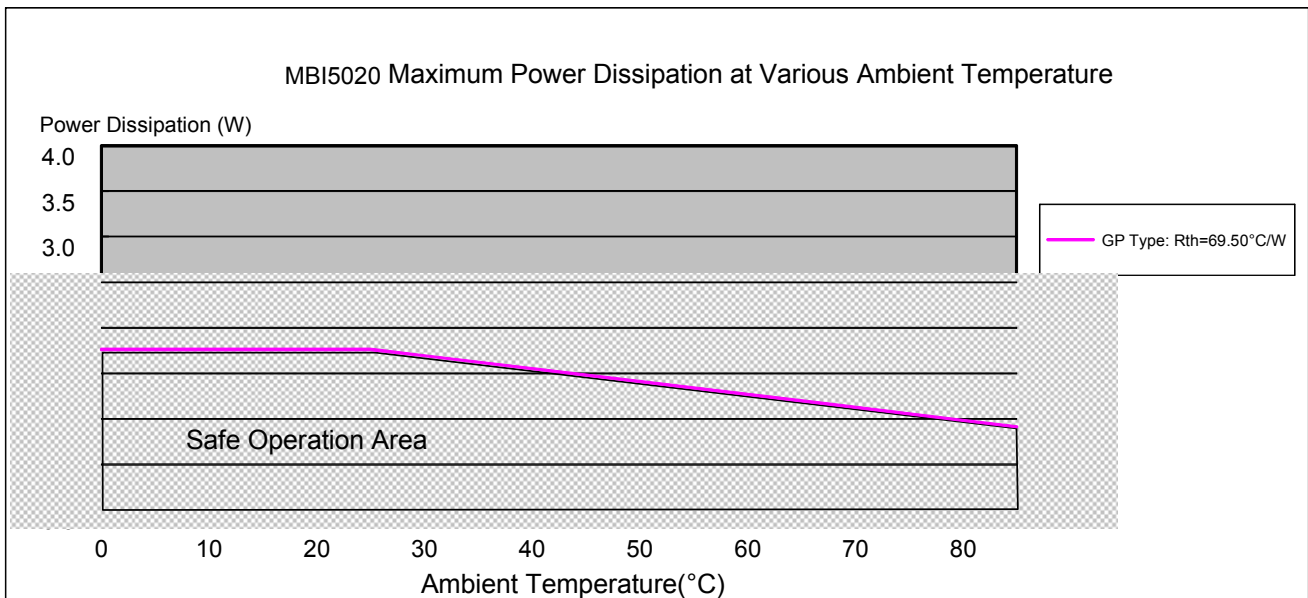
The maximum allowable package power dissipation is determined as  $P_D(max)=(T_j-T_a)/R_{th(j-a)}$ . When 16 output channels are turned on simultaneously, the actual package power dissipation is

$P_D(act)=(I_{DD} \times V_{DD})+(I_{OUT} \times Duty \times V_{DS} \times 16)$ . Therefore, to keep  $P_D(act) \leq P_D(max)$ , the allowable maximum output current as a function of duty cycle is:

$$I_{OUT} = \{[(T_j - T_a) / R_{th(j-a)}] - (I_{DD} \times V_{DD})\} / V_{DS} / Duty / 16, \text{ where } T_j = 150^\circ\text{C}.$$

Condition: I <sub>OUT</sub> =30mA, 16 output channels active		
Package	R <sub>th(j-a)</sub> (°C/W)	P <sub>D</sub> (W)
GP	70.90	1.76

The maximum power dissipation,  $P_D(max)=(T_j-T_a)/R_{th(j-a)}$ , decreases as the ambient temperature increases.

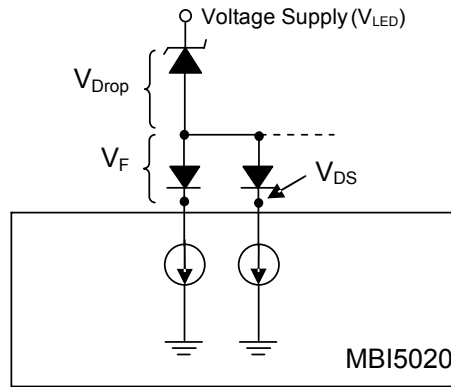
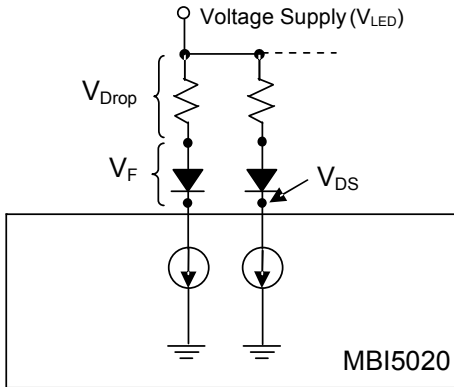


**Load Supply Voltage ( $V_{LED}$ )**

MBI5020 are designed to operate with  $V_{DS}$  ranging from 0.4V to 0.8V (depending on  $I_{OUT}=1\sim 35mA$ ) considering the package power dissipating limits.  $V_{DS}$  may be higher enough to make  $P_{D(act)} > P_{D(max)}$  when  $V_{LED}=5V$  and  $V_{DS}=V_{LED}-V_F$ , in which  $V_{LED}$  is the load supply voltage. In this case, it is recommended to use the lowest possible supply voltage or to set an external voltage reducer,  $V_{DROP}$ .

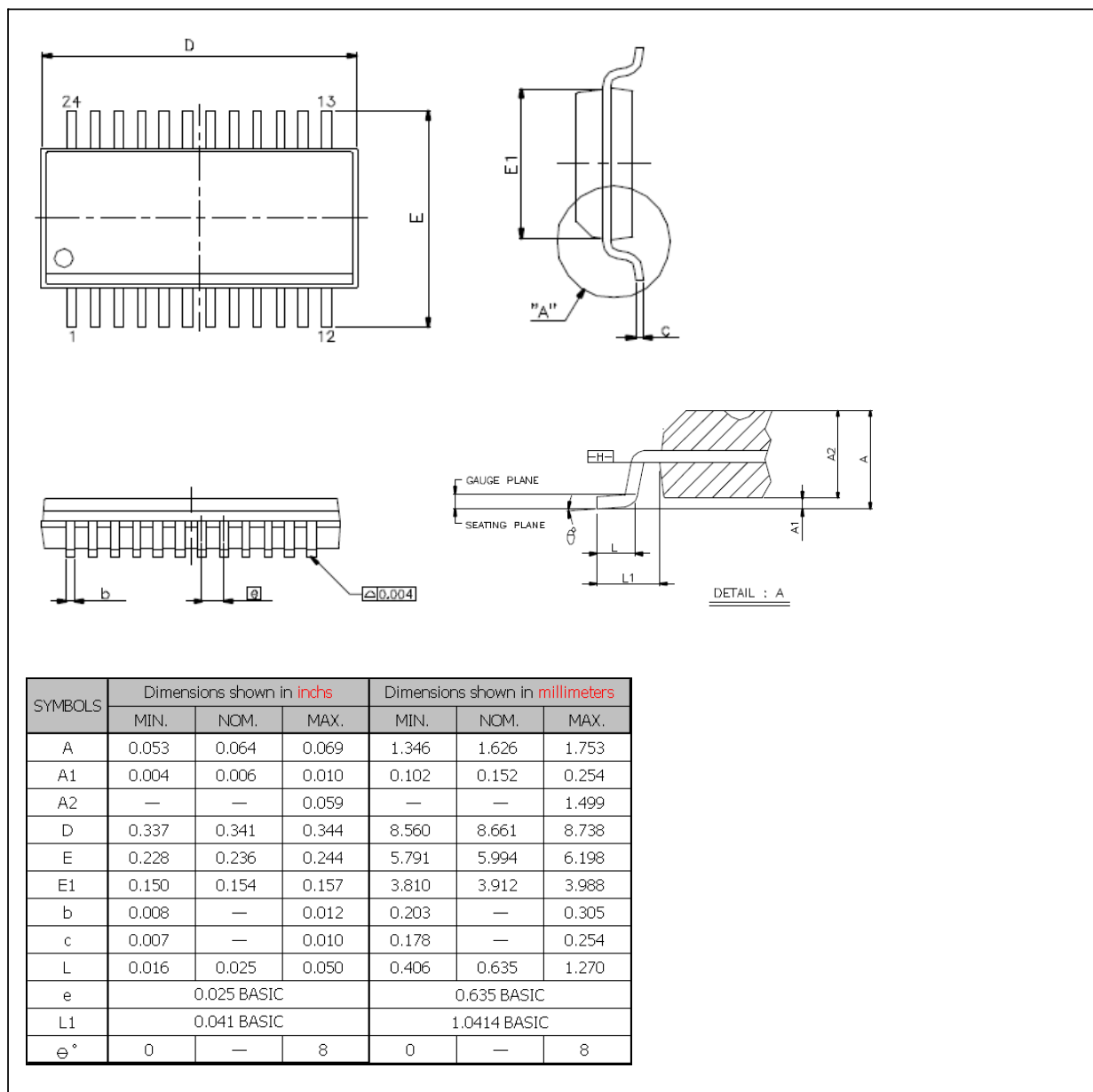
A voltage reducer lets  $V_{DS}=(V_{LED}-V_F)-V_{DROP}$ .

Resistors or Zener diode can be used in the applications as shown in the following figures.



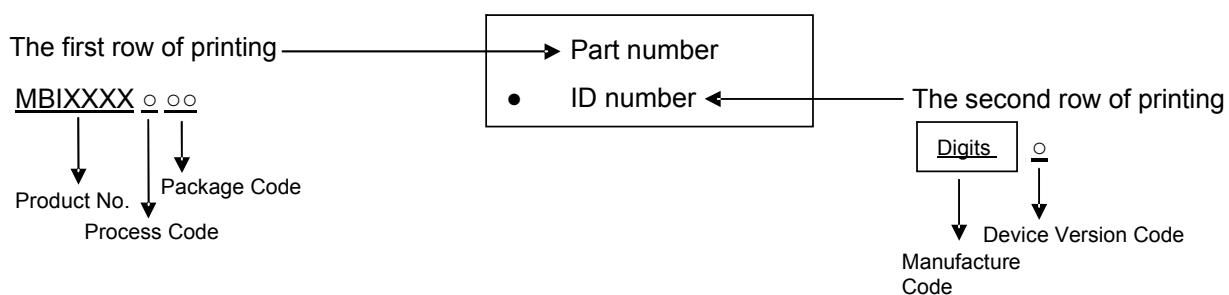


Package Outline



MBI5020GP Outline Drawing

### Product Top-mark Information



### Product Revision History

Datasheet Version	Device Version Code
V1.00	A
V1.10	A

### Product Ordering Information

Part Number *	RoHS Package Type	Weight (g)
MBI5020GP-A	SSOP24L-150-0.64	0.11

\*Please place your order with the „Part Number” information on your purchase order (PO).

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