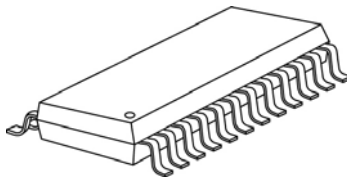
16-Channel Constant Current LED Driver With 16-bit PWM Control

Features

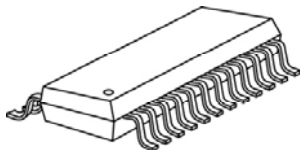
- Backward compatible with MBI5026 in package
- 16 constant-current output channels
- 16-bit/12-bit color depth PWM control
- Scrambled-PWM technology to improve refresh rate
- Compulsory open circuit detection to detect individual LED errors
  Full panel, data independent
  Silent error detection with 0.1mA
- 8-bit programmable output current gain
- Over temperature warning/protection
- Constant output current range: 3~90mA
  3~70mA at 3.3V supply voltage
  8~ 90mA at 5.0V supply voltage
- Output current accuracy:
  Between channels: <±1.5% (typ.), and
  Between ICs: <±3% (typ.)
- Staggered delay of output, preventing from current surge
- Maximum data clock frequency: 30MHz
- Schmitt trigger input
- 3.0V-5.5V supply voltage

Small Outline Package



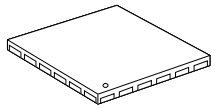
GF: SOP24L-300-1.00

Thin Shrink SOP



GTS: TSSOP24L-173-0.65

Quad Flat No-Lead



GFN: QFN24L-4*4-0.5

Product Description

MBI5030 is designed for LED video applications using internal Pulse Width Modulation (PWM) control with selectable 16-bit or 12-bit color depth. MBI5030 features a 16-bit shift register which converts serial input data into each pixel gray scale of output port. At MBI5030 output port, sixteen regulated current ports are designed to provide uniform and constant current sinks for driving LEDs with a wide range of V_F variations. The output current can be preset through an external resistor. Moreover, the preset current of MBI5030 can be further programmed to 256 gain steps for LED global brightness adjustment.

With Scrambled-PWM (S-PWM) technology, MBI5030 enhances Pulse Width Modulation by scrambling the “on” time into several “on” periods. The enhancement equivalently increases the visual refresh rate. When building a 16-bit color depth video, S-PWM reduces the flickers and improves the fidelity. MBI5030 offloads the signal timing generation of the host controller which just needs to feed data into drivers. MBI5030 drives the corresponding LEDs to the brightness specified by image data. With MBI5030, all output channels can be built with 16-bit color depth (65,536 gray scales). Each LED’s brightness can be calibrated enough from minimum to maximum brightness with compensated gamma correction or LED deviation information inside the 16-bit image data.

Floor 6-4, No.18, Pu-Ting Rd., Hsinchu, Taiwan 30077, ROC.
TEL: +886-3-579-0068, FAX: +886-3-579-7534 E-mail: info@mblock.com.tw

Block Diagram

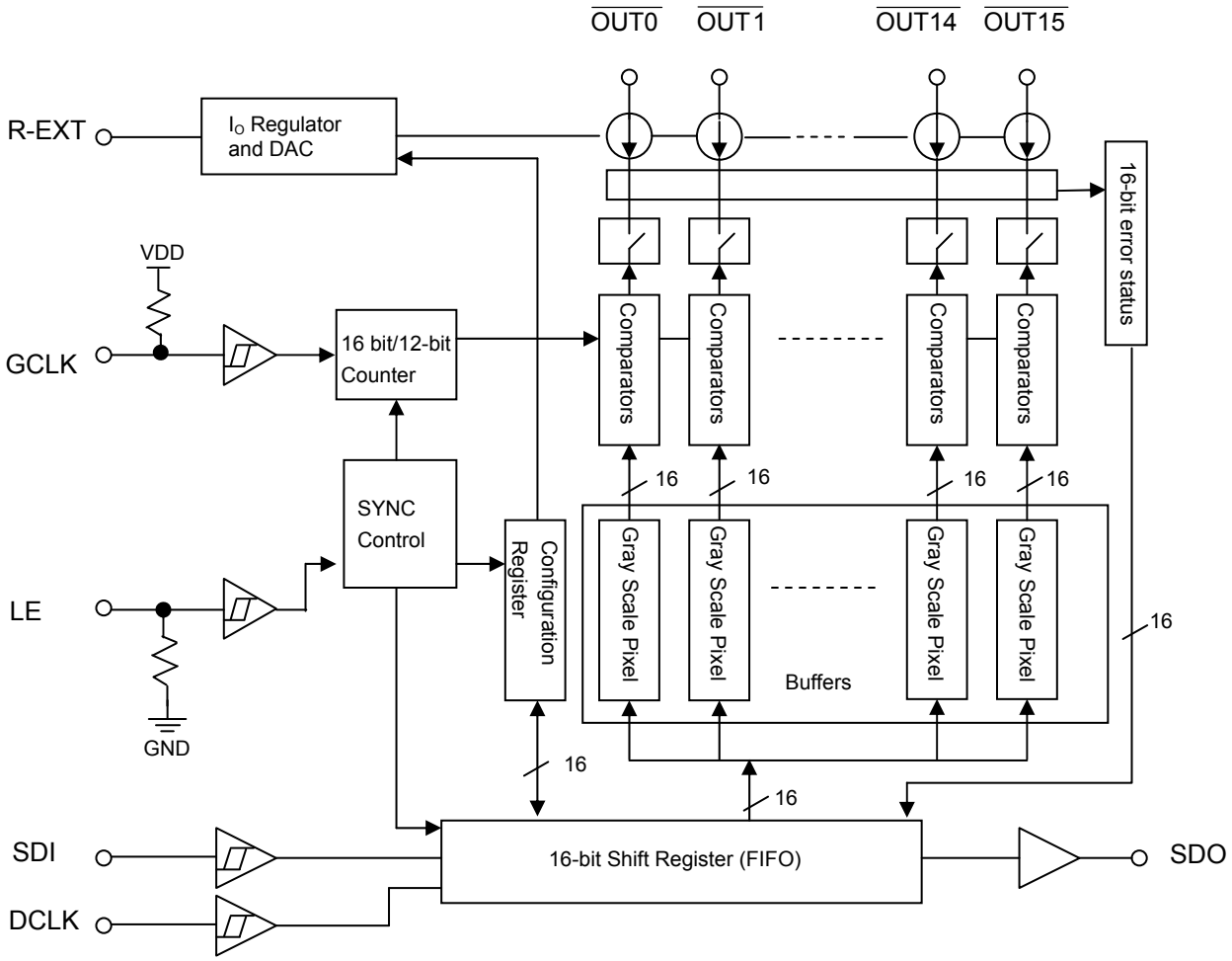
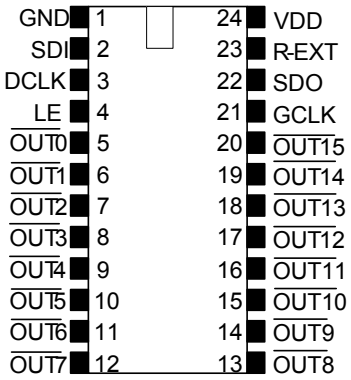
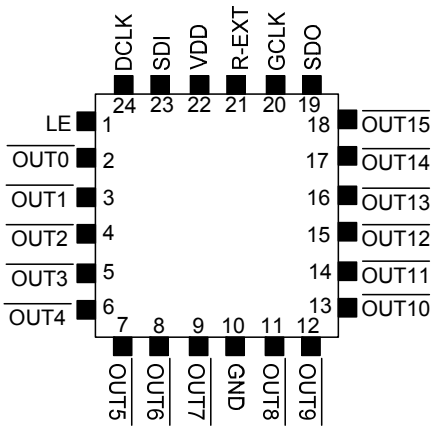


Figure 1

Pin Configuration



MBI5030GF/GTS



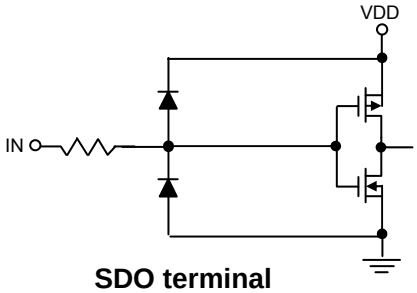
MBI5030GFN

Terminal Description

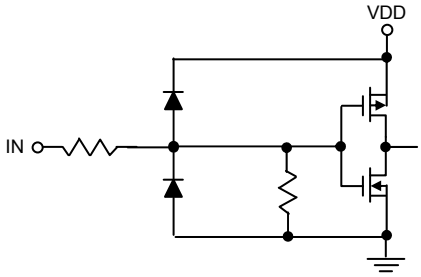
Pin Name	Function
GND	Ground terminal for control logic and current sink
SDI	Serial-data input to the shift register
DCLK	Clock input terminal used to shift data on rising edge and carries command information when LE is asserted.
LE	Data strobe terminal and controlling command with DCLK
$\overline{OUT0}$ ~ $\overline{OUT15}$	Constant current output terminals
GCLK	Gray scale clock terminal Clock input for gray scale. The gray scale display is counted by gray scale clock comparing with input data.
SDO	Serial-data output to the receiver-end SDI of next driver IC
R-EXT	Input terminal used to connect an external resistor for setting up output current for all output channels
VDD	3.3V/5V supply voltage terminal

Equivalent Circuits of Inputs and Outputs

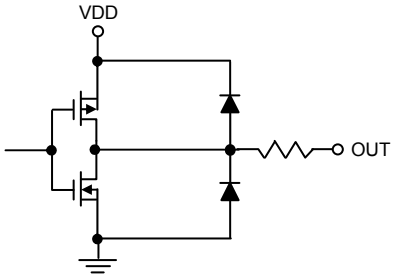
GCLK, DCLK, SDI terminal



LE terminal



SDO terminal



Maximum Rating

Characteristic		Symbol	Rating	Unit
Supply Voltage		V_{DD}	7	V
Input Pin Voltage (SDI)		V_{IN}	-0.4~V_{DD}+0.4	V
Output Current		I_{OUT}	+100	mA
Sustaining Voltage at OUT Port		V_{DS}	17	V
GND Terminal Current		I_{GND}	+1600	mA
Power Dissipation (On PCB, Ta=25°C)*	GF Type	P_D	2.39	W
	GTS Type		3.87	
	GFN Type		3.49	
Thermal Resistance (On PCB, Ta=25°C)*	GF Type	$R_{th(j-a)}$	52.37	°C/W
	GTS Type		32.34	
	GFN Type		35.85	
Junction Temperature		$T_{j,max}$	150**	°C
Operating Ambient Temperature		T_{opr}	-40~+85	°C
Storage Temperature		T_{stg}	-55~+150	°C
ESD Rating	Human Body Mode (MIL-STD-883G Method 3015.7)	HBM	Class 3B (≧8000V)	-
	Machine Mode (JEDEC EIA/JESD22-A115)	MM	Class C (≧400V)	-

*The PCB size is 76.2mm*114.3mm in simulation. Please refer to JEDEC JESD51.

** Operation at the maximum rating for extended periods may reduce the device reliability; therefore, the suggested operation temperature of the device is under 125°C.

Note: The performance of thermal dissipation is strongly related to the size of thermal pad, thickness and layer numbers of the PCB. The empirical thermal resistance may be different from simulative value. User should plan for expected thermal dissipation performance by selecting package and arranging layout of the PCB to maximize the capability.

Electrical Characteristics (V_{DD}=5.0V, Ta=25°C)

Characteristics		Symbol	Condition		Min.	Typ.	Max.	Unit
Supply Voltage		V_{DD}	-		4.5	5.0	5.5	V
Sustaining Voltage at OUT Ports		V_{DS}	$\overline{OUT0}$ ~ $\overline{OUT15}$		-	-	17.0	V
Output Current		I_{OUT}	Refer to "Test Circuit for Electrical Characteristics"		8	-	90	mA
		I_{OH}	SDO		-	-	-1.0	mA
		I_{OL}	SDO		-	-	1.0	mA
Input Voltage	"H" level	V_{IH}	Ta=-40~85ºC		0.7xV_{DD}	-	V_{DD}	V
	"L" level	V_{IL}	Ta=-40~85ºC		GND	-	0.3xV_{DD}	V
Output Leakage Current		I_{OH}	V_{DS}=17.0V		-	-	0.5	µA
Output Voltage	SDO	V_{OL}	I_{OL}=+1.0mA		-	-	0.4	V
		V_{OH}	I_{OH}=-1.0mA		V_{DD}-0.4	-	-	V
Current Skew (Channel)		dI_{OUT}	I_{OUT}=25.7mA V_{DS}=1.0V	R_{ext}=560Ω	-	±1.5	±3.0	%
			I_{OUT}=64.5mA V_{DS}=1.0V	R_{ext}=220Ω	-	±1.5	±3.0	%
Current Skew (IC)		dI_{OUT2}	I_{OUT}=25.7mA V_{DS}=1.0V	R_{ext}=560Ω	-	±3.0	±6.0	%
			I_{OUT}=64.5mA V_{DS}=1.0V	R_{ext}=220Ω	-	±3.0	±6.0	%
Output Current vs. Output Voltage Regulation*		%/dV_{DS}	V_{DS} within 1.0V and 3.0V, R_{ext}=700Ω@21mA		-	±0.1	±0.3	% / V
Output Current vs. Supply Voltage Regulation*		%/dV_{DD}	V_{DD} within 4.5V and 5.5V		-	±1.0	±2.0	% / V
LED Error Detection Threshold		$V_{DS,TH}$	-		-	0.30	0.35	V
Pull-down Resistor		R_{IN}(down)	LE		250	450	800	KΩ
Supply Current	"Off"	I_{DD}(off) 1	R_{ext}=Open, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off		-	3.0	6.0	mA
		I_{DD}(off) 2	R_{ext}=700Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off		-	7.0	10.0	
		I_{DD}(off) 3	R_{ext}=230Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off		-	9.0	12.0	
	"On"	I_{DD}(on) 1	R_{ext}=700Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =On		-	8.0	11.0	
		I_{DD}(on) 2	R_{ext}=230Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =On		-	10.0	13.0	
Thermal Flag Temperature		T_{TF}	Junction Temperature		135	150	165	°C

*One channel on.

Electrical Characteristics (V_{DD}=3.3V, Ta=25°C)

Characteristics		Symbol	Condition		Min.	Typ.	Max.	Unit
Supply Voltage		V_{DD}	-		3.0	3.3	3.6	V
Sustaining Voltage at OUT Ports		V_{DS}	$\overline{OUT0}$ ~ $\overline{OUT15}$		-	-	17.0	V
Output Current		I_{OUT}	Refer to "Test Circuit for Electrical Characteristics"		3	-	70	mA
		I_{OH}	SDO		-	-	-1.0	mA
		I_{OL}	SDO		-	-	1.0	mA
Input Voltage	"H" level	V_{IH}	Ta=-40~85ºC		0.7xV_{DD}	-	V_{DD}	V
	"L" level	V_{IL}	Ta=-40~85ºC		GND	-	0.3xV_{DD}	V
Output Leakage Current		I_{OH}	V_{DS}=17.0V		-	-	0.5	μA
Output Voltage	SDO	V_{OL}	I_{OL}=+1.0mA		-	-	0.4	V
		V_{OH}	I_{OH}=-1.0mA		V_{DD}-0.4	-	-	V
Current Skew (Channel)		dI_{OUT}	I_{OUT}=25.7mA V_{DS}=1.0V	R_{ext}=560Ω	-	±1.5	±3.0	%
		dI_{OUT}	I_{OUT}=64.5mA V_{DS}=1.0V	R_{ext}=220Ω	-	±1.5	±3.0	%
Current Skew (IC)		dI_{OUT2}	I_{OUT}=25.7mA V_{DS}=1.0V	R_{ext}=560Ω	-	±3.0	±6.0	%
		dI_{OUT2}	I_{OUT}=64.5mA V_{DS}=1.0V	R_{ext}=220Ω	-	±3.0	±6.0	%
Output Current vs. Output Voltage Regulation		%/dV_{DS}	V_{DS} within 1.0V and 3.0V, R_{ext}=700Ω@20mA		-	±0.1	±0.3	% / V
Output Current vs. Supply Voltage Regulation		%/dV_{DD}	V_{DD} within 3.0V and 3.6V		-	±1.0	±2.0	% / V
LED Error Detection Threshold		$V_{DS,TH}$	-		-	0.30	0.35	V
Pull-down Resistor		R_{IN}(down)	LE		250	450	800	KΩ
Supply Current	"Off"	I_{DD}(off) 1	R_{ext}=Open, $\overline{OUT0}$~$\overline{OUT15}$ = Off		-	2.5	4.5	mA
		I_{DD}(off) 2	R_{ext}=700Ω, $\overline{OUT0}$~$\overline{OUT15}$ = Off		-	6.5	9.5	
		I_{DD}(off) 3	R_{ext}=230Ω, $\overline{OUT0}$~$\overline{OUT15}$ = Off		-	8.5	11.5	
	"On"	I_{DD}(on) 1	R_{ext}=700Ω, $\overline{OUT0}$~$\overline{OUT15}$ = On		-	8.0	11.0	
		I_{DD}(on) 2	R_{ext}=230Ω, $\overline{OUT0}$~$\overline{OUT15}$ = On		-	10.0	13.0	
Thermal Flag Temperature		T_{TF}	Junction Temperature		135	150	165	°C

*One channel on.

Test Circuit for Electrical Characteristics

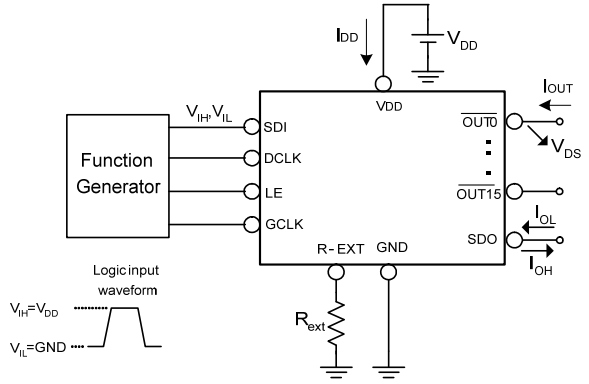


Figure 2

Switching Characteristics (V_{DD}=5.0V, Ta=25°C)

Characteristics		Symbol	Condition	Min.	Typ.	Max.	Unit
Setup Time	SDI - DCLK ↑	t_{SU0}	V_{DD}=5.0V V_{IH}=V_{DD} V_{IL}=GND R_{ext}=700Ω V_{DS}=1V R_L=200Ω C_L=10pF C_1=100nF C_2=10μF C_{SDO}=10pF	1	-	-	ns
	LE ↑ – DCLK ↑	t_{SU1}		1	-	-	ns
	LE ↓ – DCLK ↑	t_{SU2}		5	-	-	ns
Hold Time	DCLK ↑ - SDI	t_{H0}		3	-	-	ns
	DCLK ↑ - LE ↓	t_{H1}		7	-	-	ns
Propagation Delay Time	DCLK - SDO	t_{PD0}		-	25	33	ns
	GCLK – $\overline{OUT4n}$ *	t_{PD1}		-	50	-	ns
	LE – SDO**	t_{PD2}**		-	30	40	ns
Staggered Delay of Output	$\overline{OUT4n+1}$ *	t_{DL1}		-	2	-	ns
	$\overline{OUT4n+2}$ *	t_{DL2}		-	4	-	ns
	$\overline{OUT4n+3}$ *	t_{DL3}		-	6	-	ns
Pulse Width	LE	$t_{w(L)}$		5	-	-	ns
	DCLK	$t_{w(DCLK)}$		15	-	-	ns
	GCLK	$t_{w(GCLK)}$		15	-	-	ns
Output Rise Time of Output Ports		t_{OR}		15	25	-	ns
Output Fall Time of Output Ports		t_{OF}		10	15	-	ns
Error Detection Duration		t_{EDD}***		425	500	575	ns
Data Clock Frequency		F_{DCLK}		-	-	30	MHz
Gray Scale Clock Frequency****		F_{GCLK}		-	-	33	MHz

* Refer to the Timing Waveform, where n=0, 1, 2, 3.

**In timing of “Read Configuration” and “Read Error Status Code”, the next DCLK rising edge should be t_{PD2} after the falling edge of LE.

***Refer to Figure 5.

****With uniform output current.

Switching Characteristics (V_{DD}=3.3V, Ta=25°C)

Characteristics		Symbol	Condition	Min.	Typ.	Max.	Unit
Setup Time	SDI - DCLK ↑	t_{SU0}	V_{DD}=3.3V V_{IH}=V_{DD} V_{IL}=GND R_{ext}=700Ω V_{DS}=1V R_L=200Ω C_L=10pF C_1=100nF C_2=10μF C_{SDO}=10pF	1	-	-	ns
	LE ↑ – DCLK ↑	t_{SU1}		1	-	-	ns
	LE ↓ – DCLK ↑	t_{SU2}		5	-	-	ns
Hold Time	DCLK ↑ - SDI	t_{H0}		3	-	-	ns
	DCLK ↑ - LE ↓	t_{H1}		7	-	-	ns
Propagation Delay Time	DCLK – SDO	t_{PD0}		-	30	40	ns
	GCLK – $\overline{OUT4n}$ *	t_{PD1}		-	60	-	ns
	LE – SDO	t_{PD2}**		-	40	50	ns
Staggered Delay of Output	$\overline{OUT4n+1}$ *	t_{DL1}		-	2	-	ns
	$\overline{OUT4n+2}$ *	t_{DL2}		-	4	-	ns
	$\overline{OUT4n+3}$ *	t_{DL3}		-	6	-	ns
Pulse Width	LE	$t_{w(L)}$		5	-	-	ns
	DCLK	$t_{w(DCLK)}$		20	-	-	ns
	GCLK	$t_{w(GCLK)}$		20	-	-	ns
Output Rise Time of Output Ports		t_{OR}		20	30	-	ns
Output Fall Time of Output Ports		t_{OF}		30	40	-	ns
Error Detection Duration		t_{EDD}***		425	500	575	ns
Data Clock Frequency		F_{DCLK}		-	-	25	MHz
Gray Scale Clock Frequency****		F_{GCLK}		-	-	20	MHz

* Refer to the Timing Waveform, where n=0, 1, 2, 3.

**In timing of “Read Configuration” and “Read Error Status Code”, the next DCLK rising edge should be t_{PD2} after the falling edge of LE.

***Refer to Figure 5.

****With uniform output current.

Test Circuit for Switching Characteristics

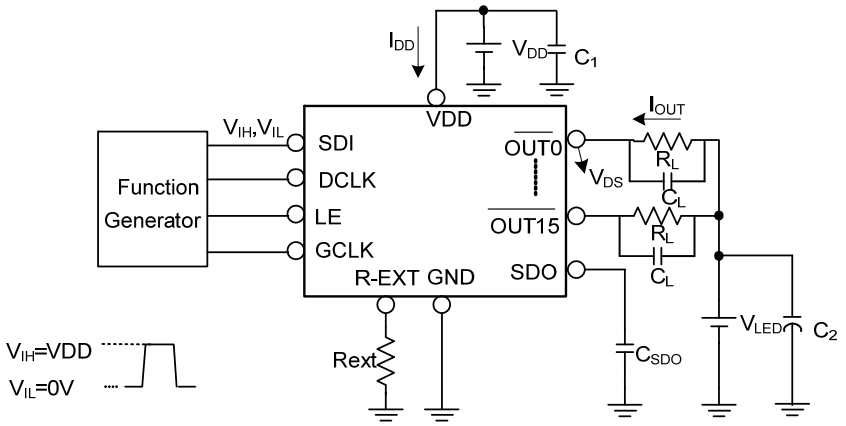
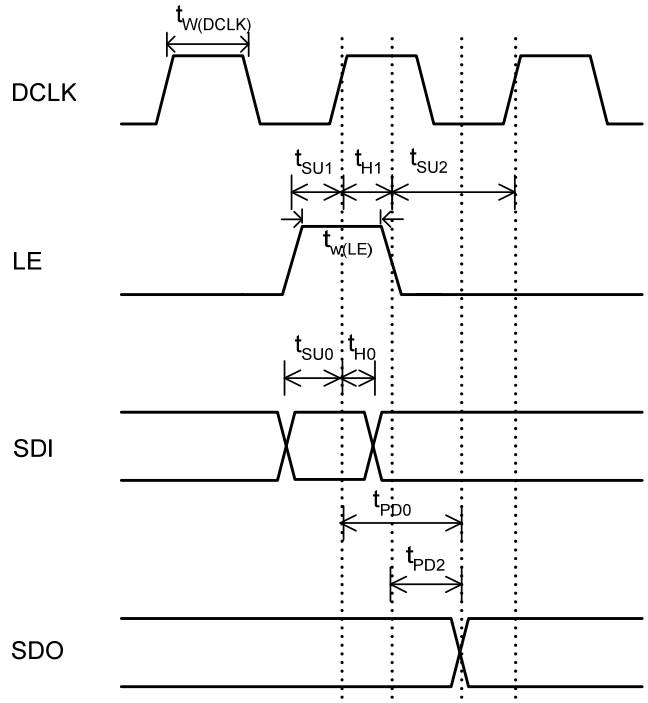


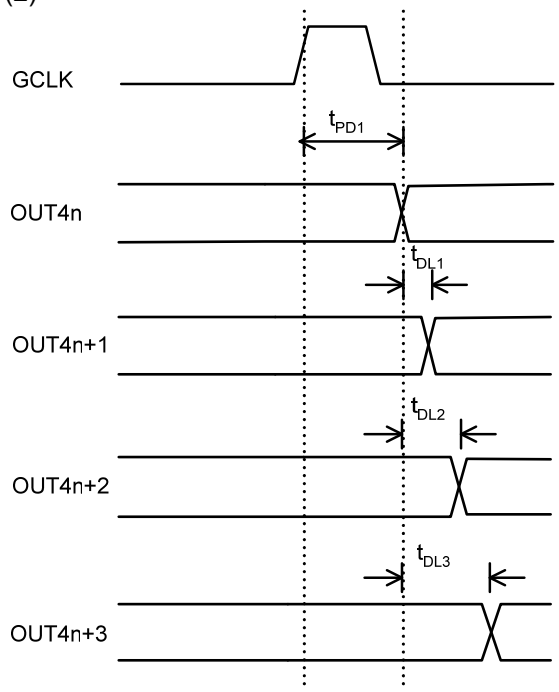
Figure 3

Timing Waveform

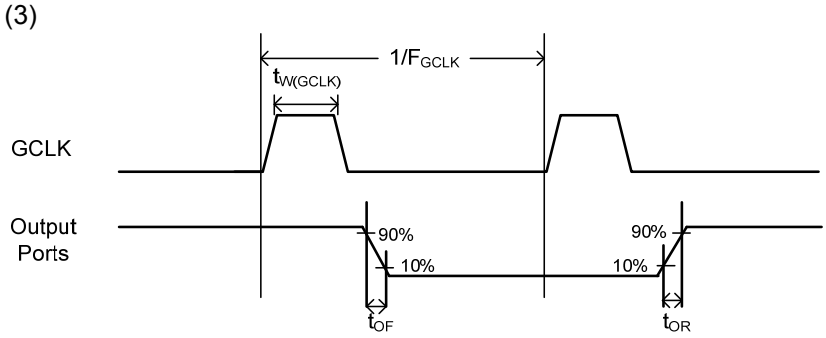
(1)



(2)



(3)

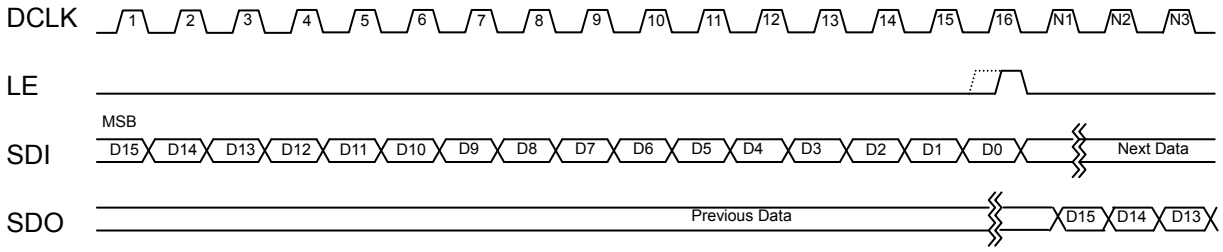


Principle of Operation

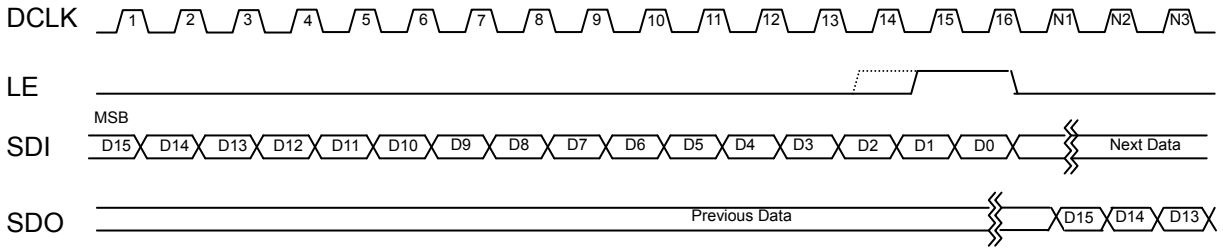
Control Command

	Signals Combination		Description
Command Name	**LE**	**Number of DCLK Rising Edge when LE is asserted**	**The Action after a Falling Edge of LE**
Data Latch	High	0 or 1	Serial data are transferred to the buffers
Global Latch	High	2 or 3	Buffer data are transferred to the comparators
Read Configuration	High	4 or 5	Move out “configuration register” to the shift registers
Enable “Error Detection”	High	6 or 7	Detect the status of each output’s LED
Read “Error Status Code”	High	8 or 9	Move out “error status code” of 16 outputs to the shift registers
Write Configuration	High	10 or 11	Serial data are transferred to the “configuration register”
Reset PWM Counter	High	12 or 13	If bit “B” of the configuration register is set to “1”, this command will reset PWM counter.

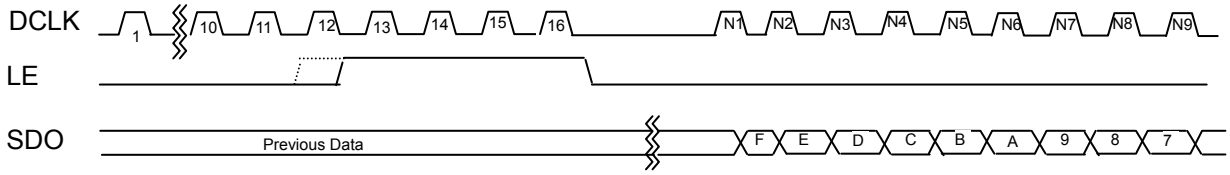
Data Latch



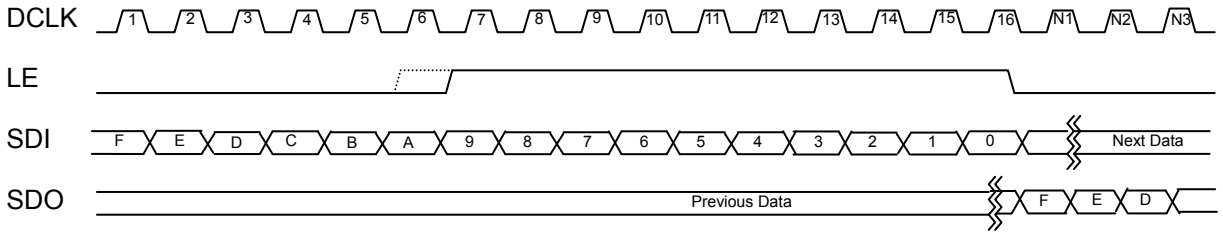
Global Latch



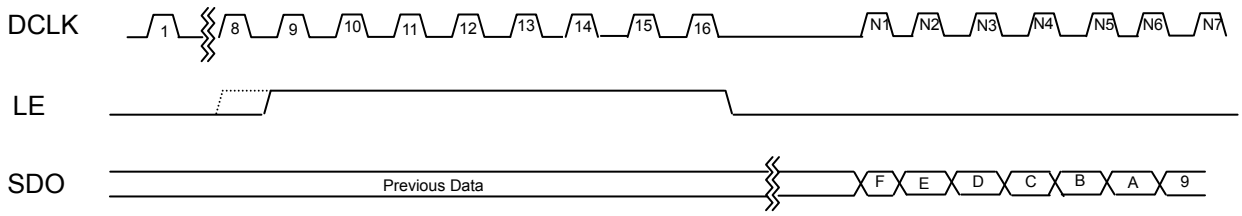
Read Configuration



Write Configuration



Read Error Status



Setting Gray Scales of Pixels

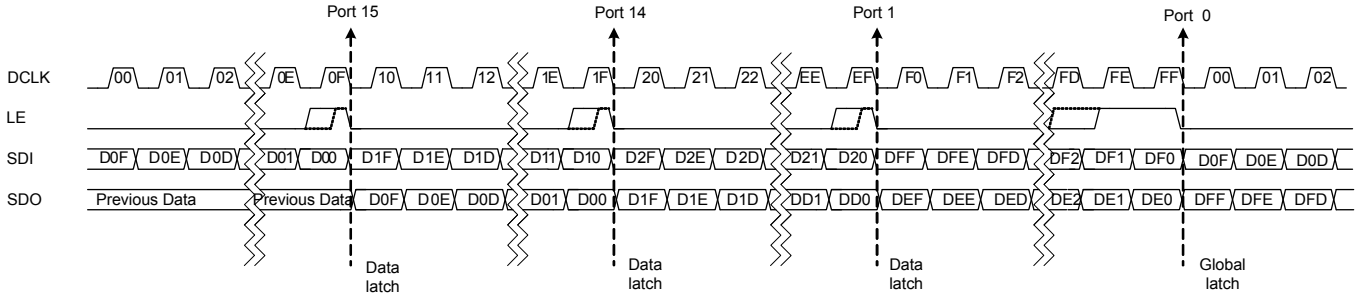
MBI5030 implements the gray level of each output port using the S-PWM control algorithm. With the 16-bit data, all output channels can be built with 65,536 gray scales.

There are two methods to issue the “global latch” command.

1. When configuration bit “F” is set to “0” (Default), the 16-bit input shift register latches 15 times of the gray scale data into each data buffer with a “data latch” command sequentially. With a “global latch” command for the 16th gray scale data, the 256-bit data buffers will be clocked in with the MSB first, loading the data from port 15 to port 0.
2. When configuration bit “F” is set to “1”, the 16-bit input shift register latches 16 times of the gray scale data into each data buffer with a “data latch” command sequentially. With a “global latch” command for additional latch, the 256-bit data buffers will be clocked in with the MSB first, loading the data from port 15 to port 0.

Full Timing for Data Loading

When bit “F” = “0”



When bit “F” = “1”

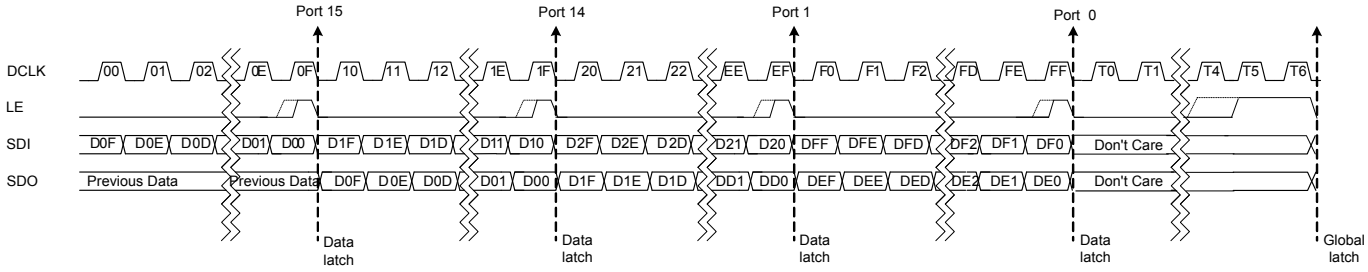


Figure 4

Error Detection Principle

The principle of MBI5030 LED open-circuit detection is based on the fact that the LED loading status is judged by comparing the effective voltage value (V_{DS}) of each output port with the target voltage ($V_{DS,TH}$) = 0.3V. Thus, after the command of “error detection”, the output ports of MBI5030 will be turned on with current 0.1mA for open-circuit detection. While receive the “read error status code” command, the LED driver will put the error status into the shift register and could be read out through the SDO pin bit by bit. Then, the error status of open-circuit saved in the built-in register would be shifted out through SDO pin bit by bit after coming new data.

The error detection time (t_{EDD}) is from the LE falling edge of “enable error detection” command to the LE falling edge of “read error status code” command. The detection time shall be controlled within a suitable length. If the error detection time is too long, flickers may occur. If the error detection time is too short, the detection result may not be stable. In general case, to get the correct error report without flickers, it is recommended to issue the “read error status code” command right after the “enable error detection” command under the normal speed of DCLK.

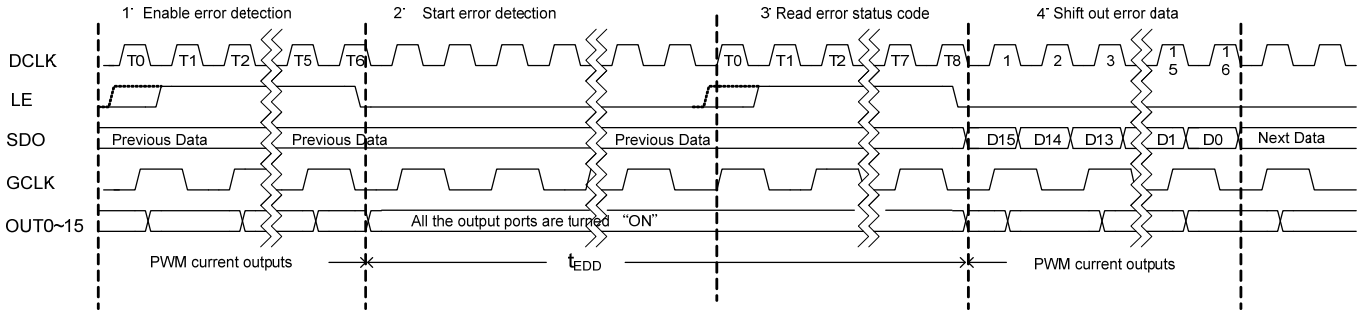


Figure 5

The relationship between the error status code and the effective output point is shown below:

State of Output Port	Condition of Effective Output Point		Detected Error Status Code	Meaning
On / Off	I_{OUT}=0.1mA,	$V_{DS}<V_{DS,TH}$	“0”	Error
		$V_{DS}\geqq V_{DS,TH}$	“1”	Normal

Definition of Configuration Register

MSB LSB

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0

e.g.. Default Value

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	8'b10101011								0	0

Bit	Attribute	Definition	Value	Function	
F	Read/Write	Data loading	0 (Default)	15 times of "data latch" + 1 "global latch"	
			1	16 times of "data latch" + 1 "global latch"	
E	Read	Thermal error flag	0 (Default)	Safe (OK)	
			1	Over temperature (>150°C typ.)	
D	Read/Write	PWM gray scale counter	0 (Default)	16 bits	
			1	12 bits	
C	Read/Write	PWM counting mode selection	0 (Default)	When bit D is set to "0", 64 times of MSB* 10-bit PWM counting and once of LSB* 6-bit PWM counting*	When bit D is set to "1", 64 times of MSB 6-bit* PWM counting and once of LSB 6-bit PWM counting*
			1	16-bit PWM counting	12-bit PWM counting
B	Read/Write	PWM counter reset	0(Default)	Disable	
			1	Enable with 12 or 13 DCLKs (rising edge) when LE is asserted	
A	Read/Write	PWM data synchronization mode	0 (Default)	Auto-synchronization	
			1	Manual synchronization	
9~2	Read/Write	Current gain adjustment	00000000 ~ 11111111	8'b10101011 (Default)	
1	Read/Write	Thermal protection	0 (Default)	Disable	
			1	Enable** , 25% of setting output current if T_{TF} > 150°C	
0	Read/Write	Time-out alert of GCLK disconnection	0 (Default)	Enable***	
			1	Disable	

*Please refer to "Setting the PWM Counting Mode" section.

**Please refer to "TP Function (Thermal Protection)" section.

***Please refer to "Time-Out Shutdown of GCLK Disconnection" section.

Thermal Error Flag

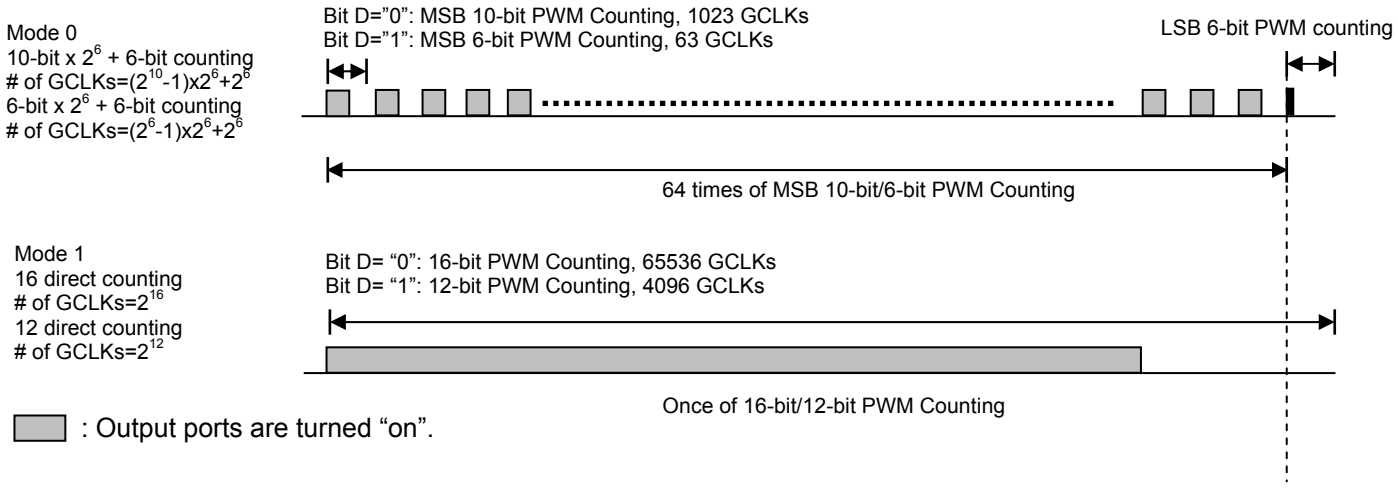
The thermal error flag indicates an overheating condition. When IC's junction temperature is over 150°C (typ.), the bit "E" is set to "1". The bit "E" can be read out through "Read Configuration" command.

Setting the PWM Gray Scale Counter

MBI5030 provides a selectable 16-bit or 12-bit color depth. The value of 16-bit image data of each output will be only implemented according 16-bit or 12-bit PWM counter. The default bit "D" is set to "0" for 16-bit color depth.

Setting the PWM Counting Mode

MBI5030 defines the different counting algorithms that support S-PWM, scrambled PWM, technology. With S-PWM, the total PWM cycles can be broken down into MSB (Most Significant Bits) and LSB (Least Significant Bits) of gray scale cycles, and the MSB information can be dithered across many refresh cycles to achieve overall same high bit resolution. MBI5030 also allows changing different counting algorithms and provides the better output linearity when there are fewer transitions of output.



Synchronization for PWM Counting

Between the data frame and the video frame, when the bit “A” is set to “0” (Default), MBI5030 will automatically handle the synchronization of previous data and next data for PWM counting. The next image data will be updated to output buffers and start PWM counting when the previous data has finished one internal PWM cycle. It will prevent the lost count of image data resolution and guarantee the data accuracy. In this mode, system controller only needs to provide a continuous running GCLK for PWM counter. The output will be renewed after finishing one of MSB PWM cycles.

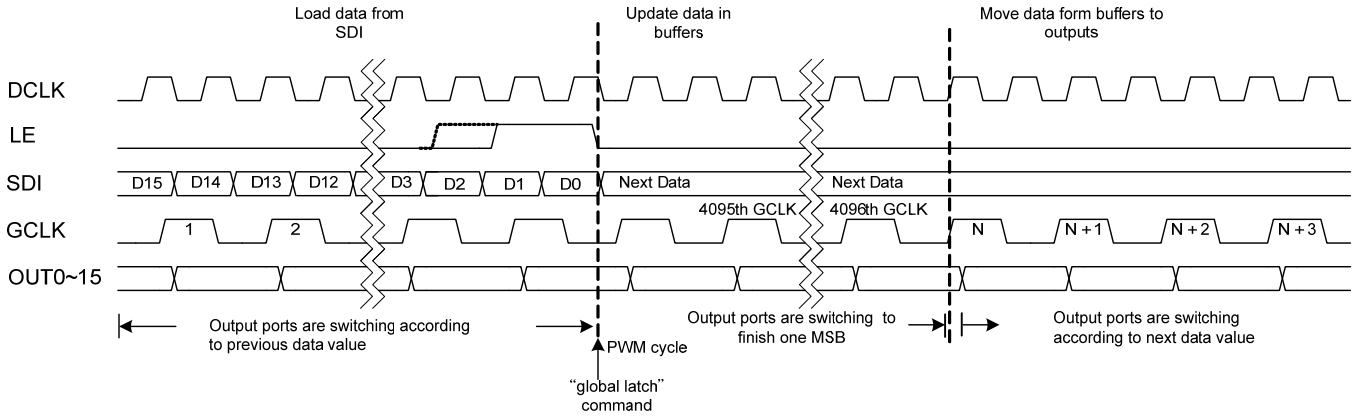


Figure 6

When the bit “A” is set to “1”, MBI5030 will update the next image data into output buffer immediately, no matter the counting status of previous image data is. In this mode, system controller will synchronize the GCLK according image data outside MBI5030 by itself. Otherwise, the conflict of previous image data and next image data will cause the data lost.

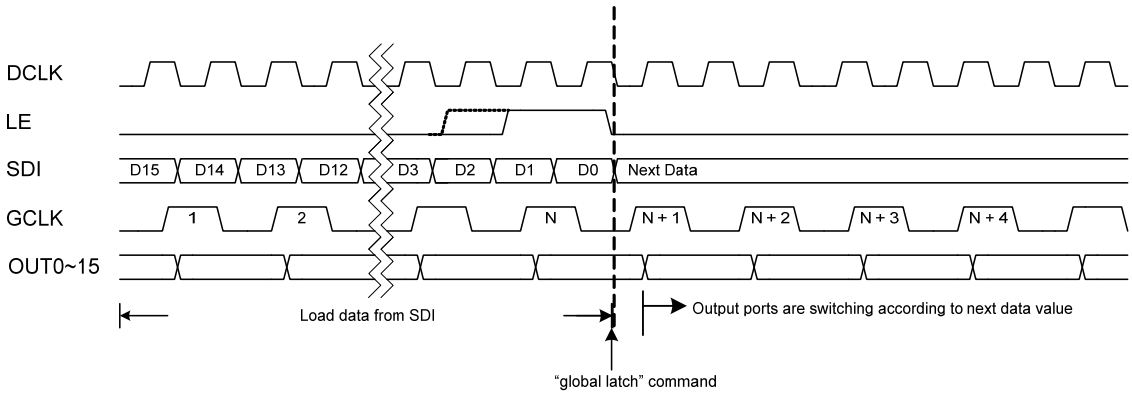


Figure 7

Time-Out Shutdown of GCLK Disconnection

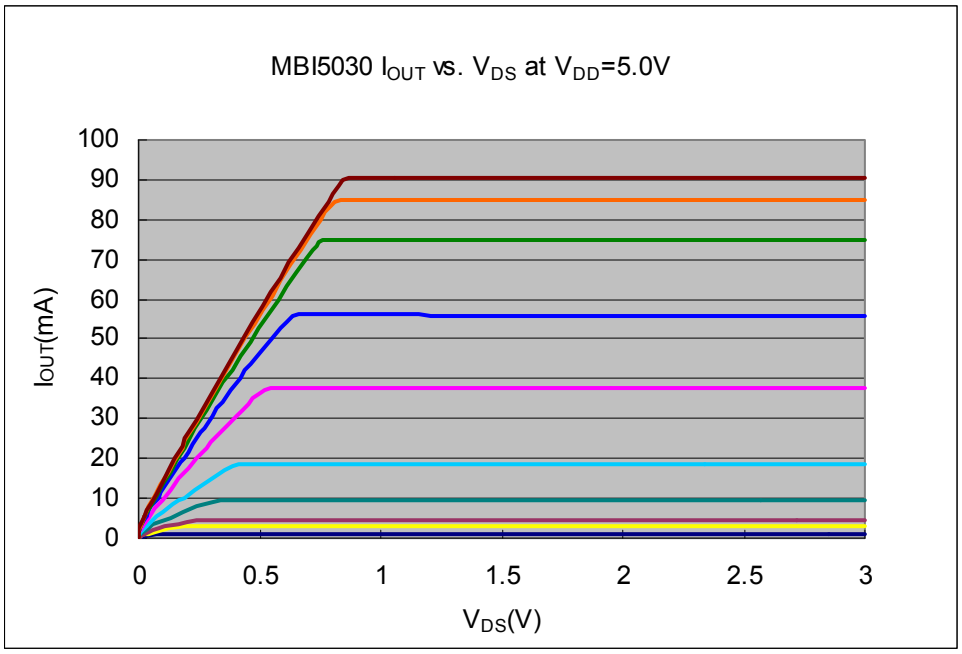
When the signal of GCLK is disconnected for around 1 second period, all output ports will be turned off automatically. This function will protect the LED display system from staying on always and prevent the large current from damaging the power system. The default is set to ‘enable” when bit “0” is 0. When the GCLK is active again and new serial data are moved in, the driver resumes to work after resetting the internal counters and comparators.

Constant Current

In LED display application, MBI5030 provides nearly no variation in current from channel to channel and from IC to IC. This can be achieved by:

1) The typical current variation between channels is less than 1.5%, and that between ICs is less than ±3%.

2) In addition, the current characteristic of output stage is flat and users can refer to the figure as shown below. The output current can be kept constant regardless of the variations of LED forward voltages (V_F). This guarantees LED to be performed on the same brightness as user's specification.



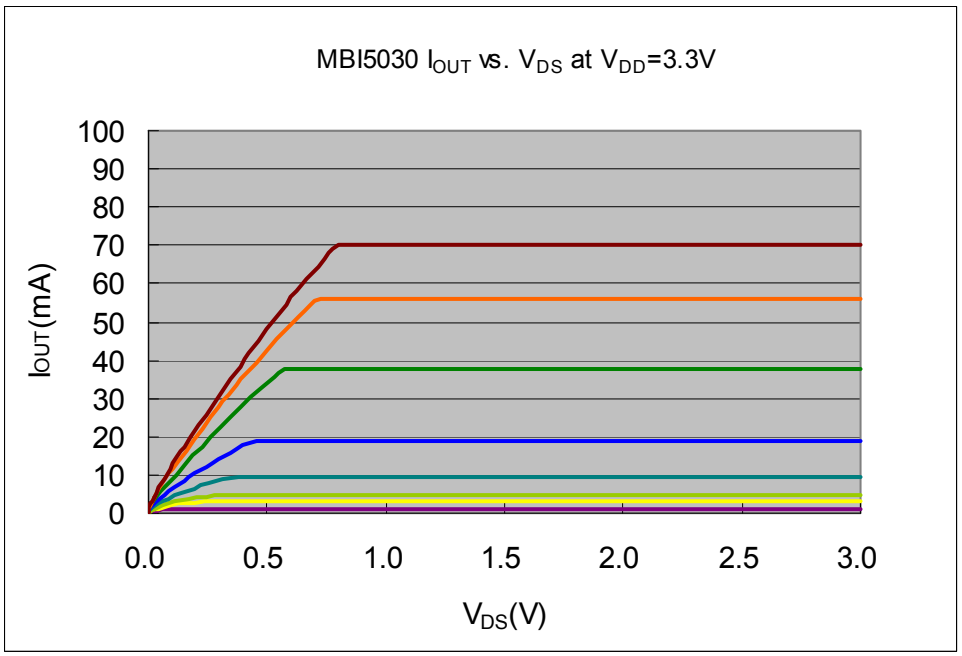


Figure 8

Setting Output Current

The output current (I_{OUT}) is set by an external resistor, R_{ext}. The default relationship between I_{OUT} and R_{ext} is shown in the following figure.

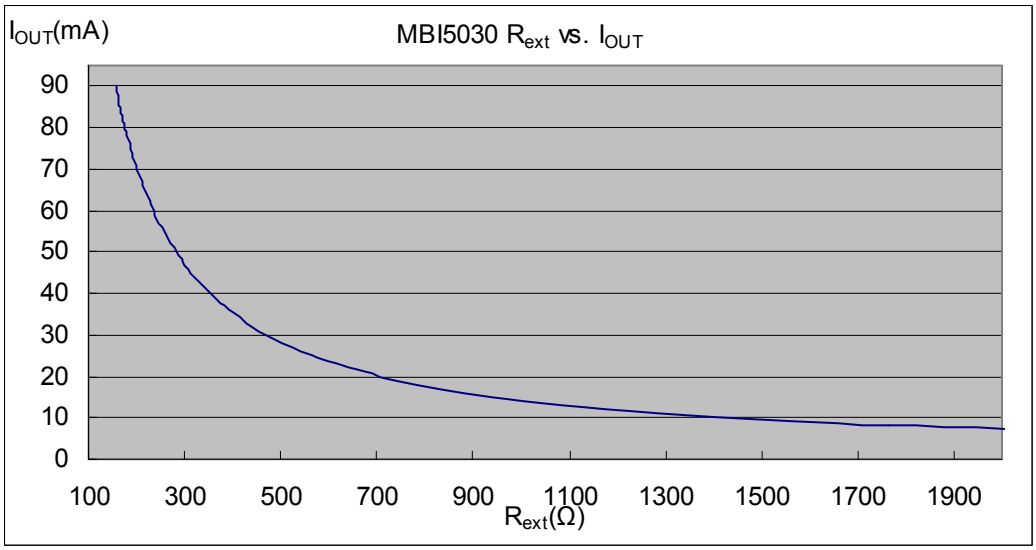


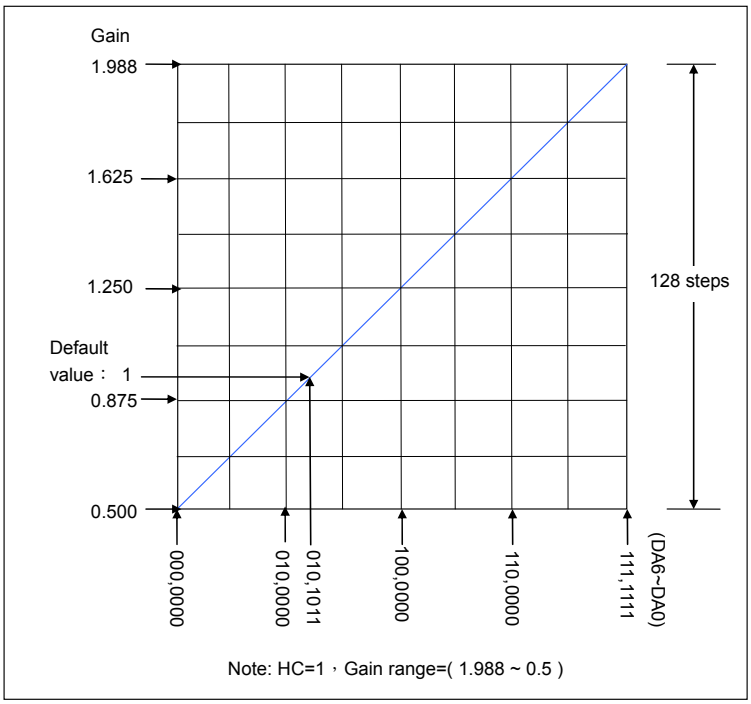
Figure 9

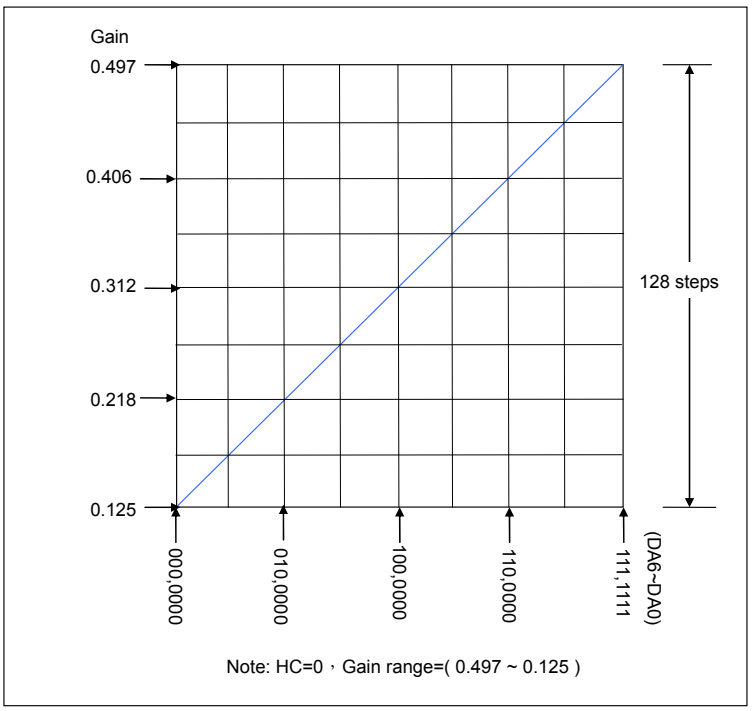
Also, the output current can be calculated from the equation:

VR-EXT=0.61Volt x G; IOUT=(VR-EXT/Rext)x23.3

Whereas Rext is the resistance of the external resistor connected to R-EXT terminal and VR-EXT is its voltage. G is the digital current gain, which is set by the bit9 – bit2 of the configuration register. The default value of G is 1. For your information, the output current is about 20mA when R_{ext}=700Ω and 60mA when R_{ext}=230Ω if G is set to default value 1. The formula and setting for G are described in next section.

Current Gain Adjustment





The bit 9 to bit 2 of the configuration register set the gain of output current, i.e., G. As totally 8-bit in number, i.e., ranged from 8'b00000000 to 8'b11111111, these bits allow the user to set the output current gain up to 256 levels. These bits can be further defined inside Configuration Register as follows:

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	HC	DA6	DA5	DA4	DA3	DA2	DA1	DA0	-	-

1. Bit 9 is HC bit. The setting is in low current band when HC=0, and in high current band when HC=1.
2. Bit 8 to bit 2 are DA6 ~ DA0.

The relationship between these bits and current gain G is:

HC=1, D=(256G-128)/3

HC=0, D=(1024G-128)/3

and D in the above decimal numeration can be converted to its equivalent in binary form by the following equation:

$D=DA6x2^6+DA5x2^5+DA4x2^4+DA3x2^3+DA2x2^2+DA1x2^1+DA0x2^0$

In other words, these bits can be looked as a floating number with 1-bit exponent HC and 7-bit mantissa DA6~DA0.

For example,

HC=1, G=1.25, D=(256x1.25-128)/3=64

the D in binary form would be:

$D=64=1x2^6+0x2^5+0x2^4+0x2^3+0x2^2+0x2^1+0x2^0$

The bit 9 to bit 2 of the configuration register are set to 8'b1100,0000.

Staggered Delay of Output

MBI5030 has a built-in staggered circuit to perform delay mechanism. Among output ports exist a graduated 2ns delay time among $\overline{OUT4n}$, $\overline{OUT4n+1}$, $\overline{OUT4n+2}$, and $\overline{OUT4n+3}$, by which the output ports will be divided to four groups at a different time so that the instant current from the power line will be lowered.

Package Power Dissipation (PD)

The maximum allowable package power dissipation is determined as $P_D(max)=(Tj–Ta)/R_{th(j-a)}$. When 16 output channels are turned on simultaneously, the actual package power dissipation is $P_D(act)=(I_{DD}xV_{DD})+(I_{OUT}xDutyxV_{DS}x16)$. Therefore, to keep $P_D(act)\leq P_D(max)$, the allowable maximum output current as a function of duty cycle is:

$I_{OUT}=\{[(Tj–Ta)/R_{th(j-a)}]–(I_{DD}xV_{DD})\}/V_{DS}/Duty/16$, where Tj=150°C.

The maximum power dissipation, $P_D(max)=(Tj–Ta)/R_{th(j-a)}$, decreases as the ambient temperature increases.

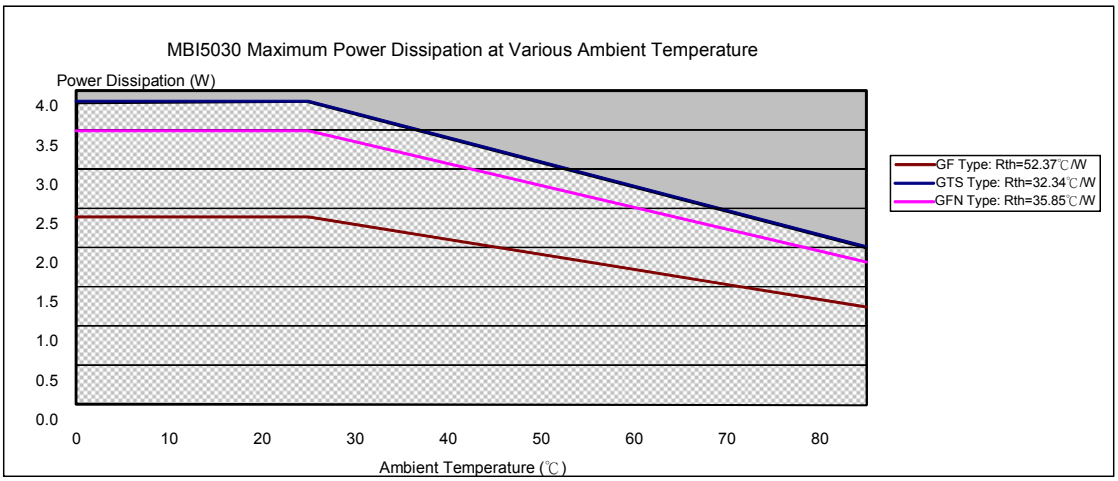


Figure 10

Usage of Thermal Pad

The PCB area L2xW2 is 4 times of the IC's area L1xW1.The thickness of the PCB is 1.6mm, copper foil 1 Oz. The thermal pad on the IC's bottom has to be mounted on the copper foil.

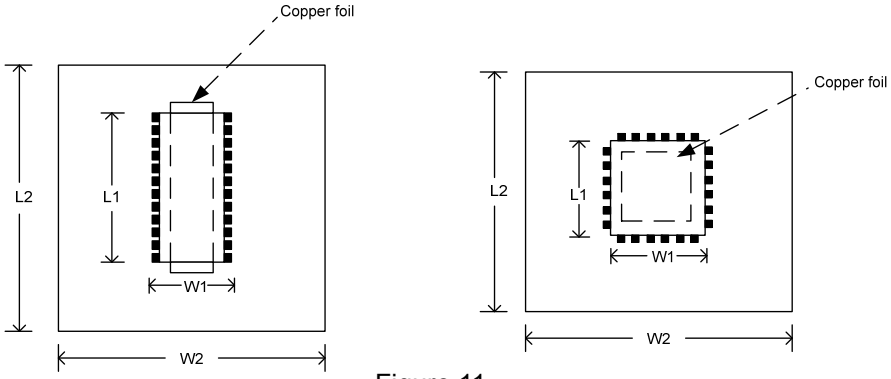


Figure 11

TP Function (Thermal Protection)

The TP function is disable by default when bit "1" is set to "0". If this bit is set to "1" and the junction temperature exceeds the threshold, T_X (150°C typ.), the thermal error flag will be turned on and the TP function will be simultaneously enabled. When the TP function is enabled, the output current will decrease to 25%. As soon as the temperature is below (125°C typ.), the thermal error flag will return to the default value "0" and the output current will recover from the 25% current. The average output current is limited, and therefore, the driver is protected from being overheated, however, it will degrade the gray scale.

LED Supply Voltage (V_{LED})

MBI5030 are designed to operate with V_{DS} ranging from 0.4V to 1.0V (depending on I_{OUT}=5~90mA) considering the package power dissipating limits. V_{DS} may be higher enough to make $P_{D\,(act)} > P_{D\,(max)}$ when V_{LED}=5V and $V_{DS}=V_{LED}-V_F$, in which V_{LED} is the load supply voltage. In this case, it is recommended to use the lowest possible supply voltage or to set an external voltage reducer, V_{DROP}.

A voltage reducer lets $V_{DS}=(V_{LED}-V_F)-V_{DROP}$.

Resistors or Zener diode can be used in the applications as shown in the following figures.

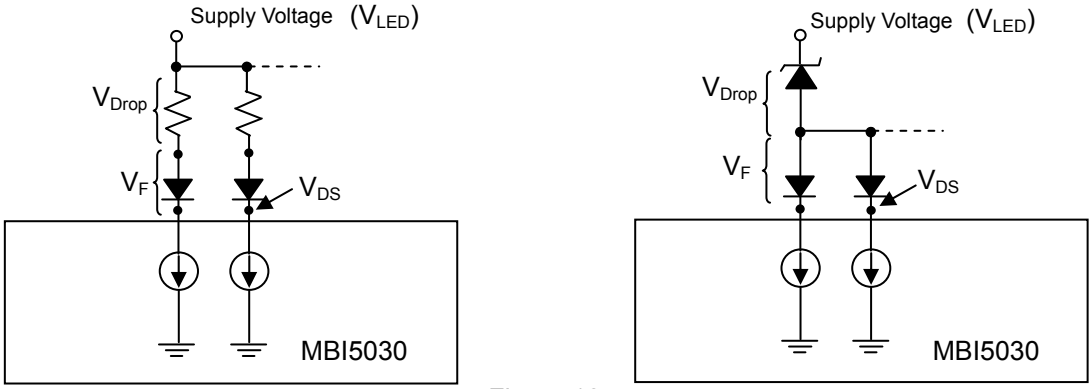


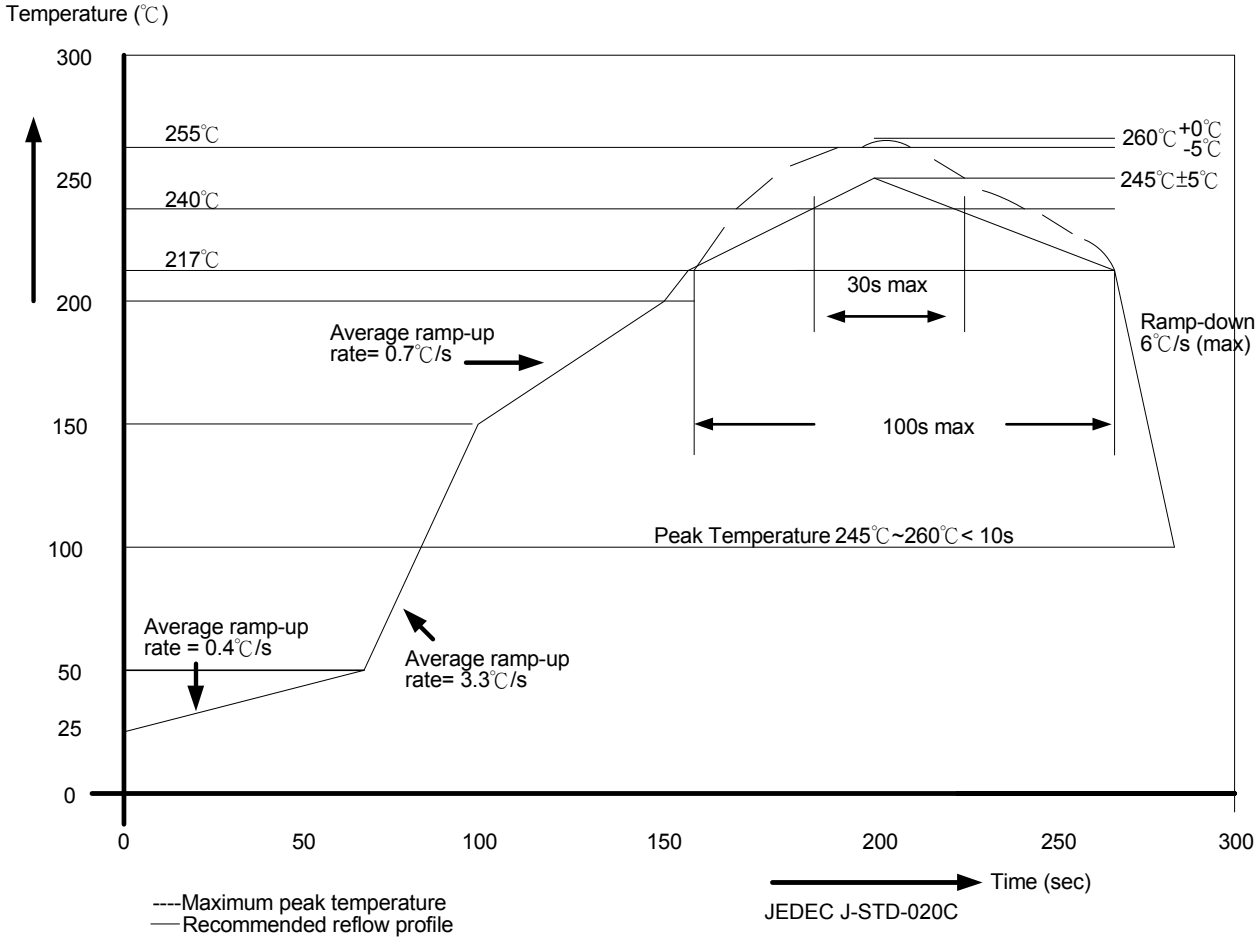
Figure 12

Switching Noise Reduction

LED drivers are frequently used in switch-mode applications which always behave with switching noise due to the parasitic inductance on PCB. To eliminate switching noise, refer to "Application Note for 8-bit and 16-bit LED Drivers- Overshoot".

Soldering Process of "Pb-free & Green" Package Plating*

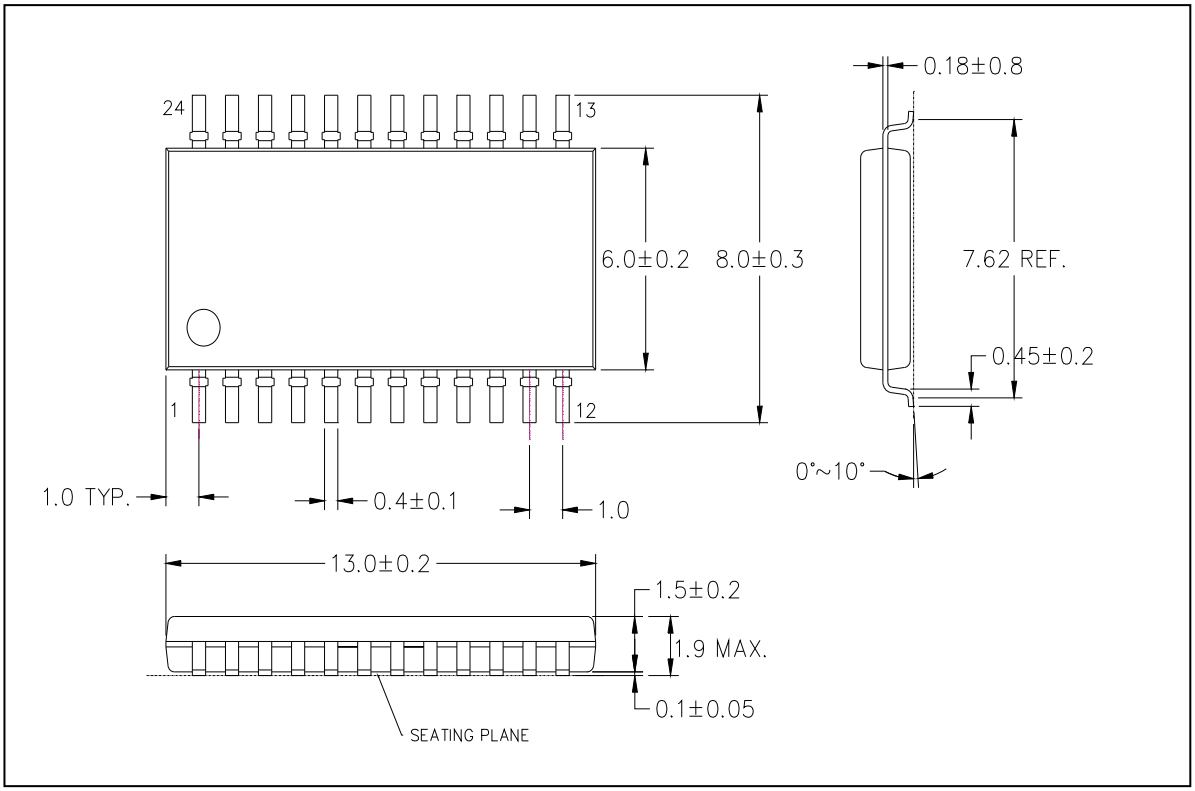
Macroblock has defined "Pb-Free & Green" to mean semiconductor products that are compatible with the current RoHS requirements and selected 100% pure tin (Sn) to provide forward and backward compatibility with both the current industry-standard SnPb-based soldering processes and higher-temperature Pb-free processes. Pure tin is widely accepted by customers and suppliers of electronic devices in Europe, Asia and the US as the lead-free surface finish of choice to replace tin-lead. Also, it adopts tin/lead (SnPb) solder paste, and please refer to the JEDEC J-STD-020C for the temperature of solder bath. However, in the whole Pb-free soldering processes and materials, 100% pure tin (Sn) will all require from 245 °C to 260°C for proper soldering on boards, referring to JEDEC J-STD-020C as shown below. .



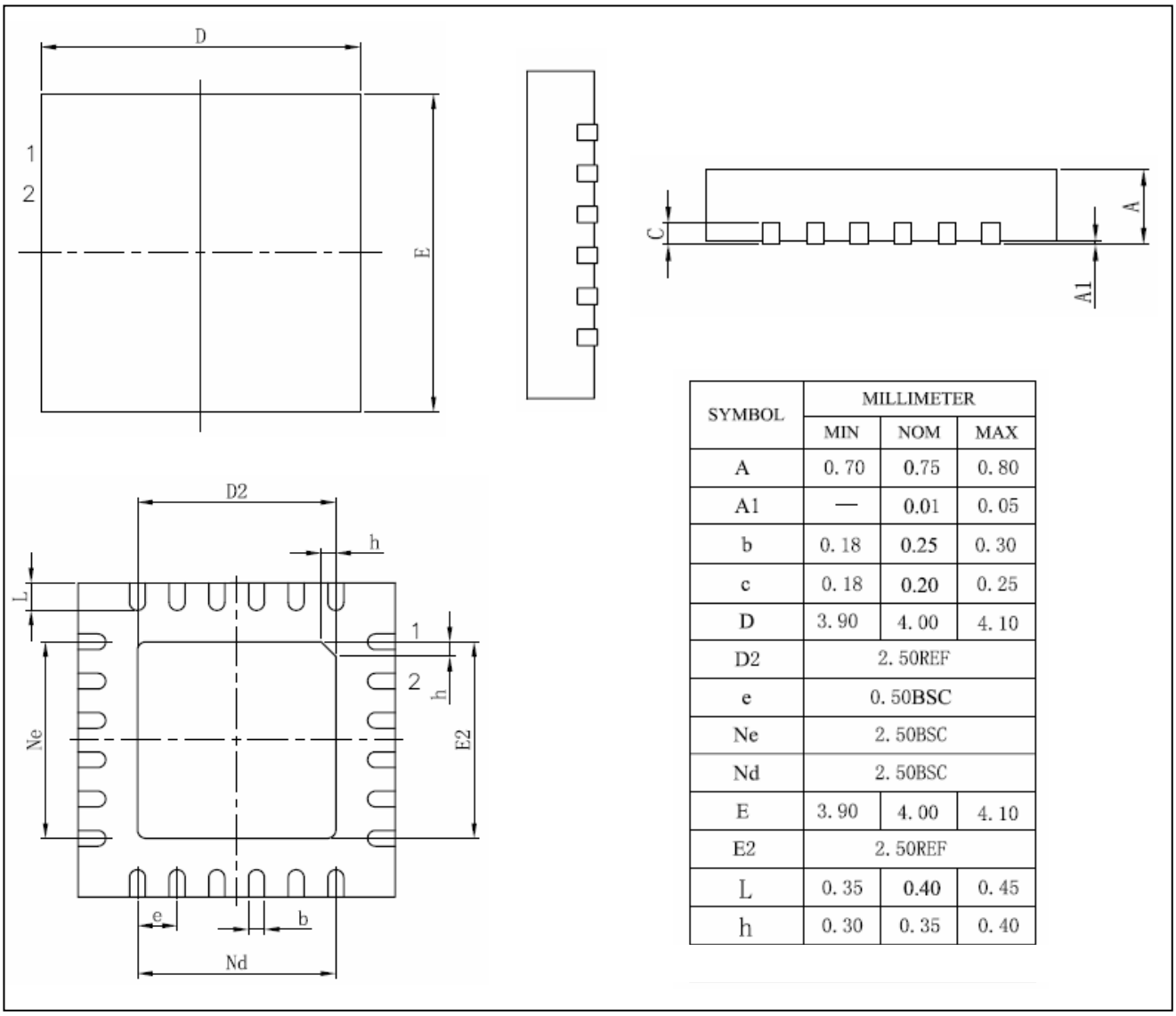
Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 ≧2000
<1.6mm	260 +0 °C	260 +0 °C	260 +0 °C
1.6mm – 2.5mm	260 +0 °C	250 +0 °C	245 +0 °C
≧2.5mm	250 +0 °C	245 +0 °C	245 +0 °C

*Note: For details, please refer to Macroblock's "Policy on Pb-free & Green Package".

Package Outline



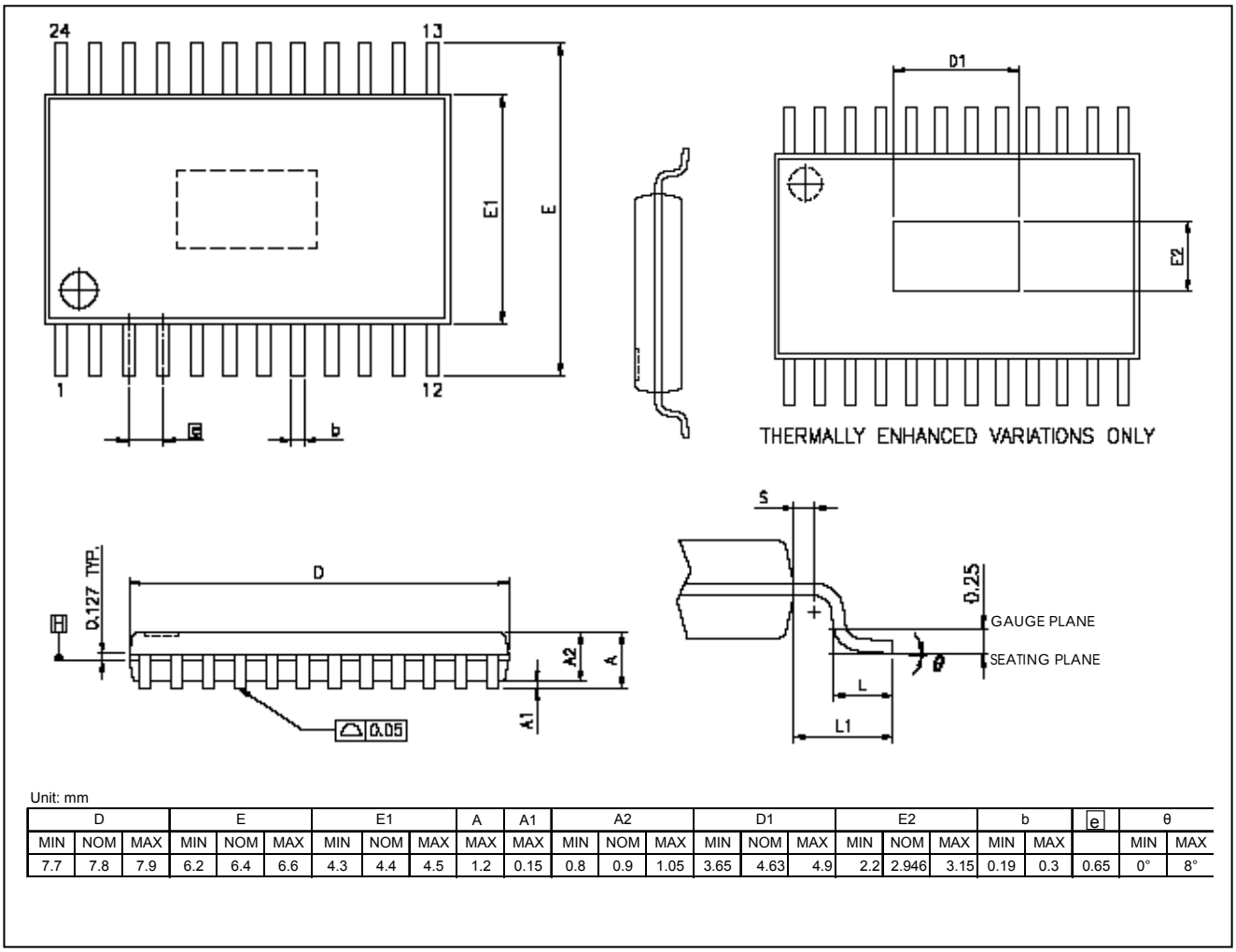
MBI5030GF Outline Drawing



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0. 70	0.75	0. 80
A1	—	0.01	0. 05
b	0. 18	0.25	0. 30
c	0. 18	0.20	0. 25
D	3. 90	4. 00	4. 10
D2	2. 50REF		
e	0. 50BSC		
Ne	2. 50BSC		
Nd	2. 50BSC		
E	3. 90	4. 00	4. 10
E2	2. 50REF		
L	0. 35	0.40	0. 45
h	0. 30	0. 35	0. 40

MBI5030GFN Outline Drawing

Remark: The thermal pad size may exist a tolerance due to the manufacturing process, please use the maximum dimensions-D2(max. 2.50mm) x E2(max. 2.50mm) for the thermal pad layout. In addition, to avoid the short circuit risk, the vias or circuit traces shall not pass through the maximum area of thermal pad.
Note: The unit of the outline drawing is millimeter (mm).



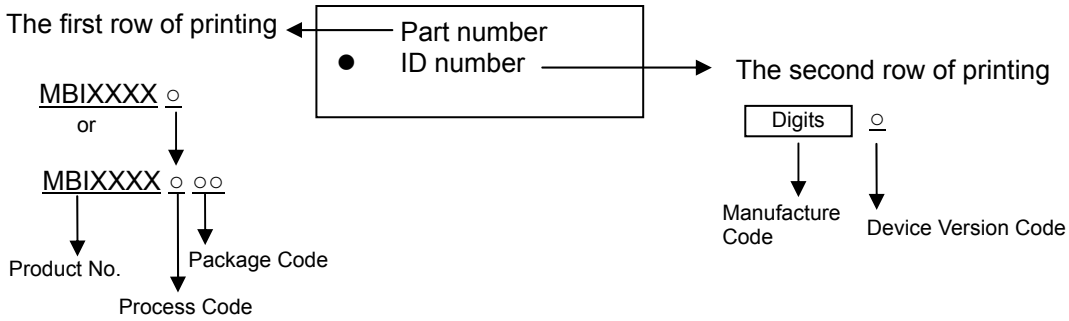
Unit: mm

D			E			E1			A	A1	A2			D1			E2			b		e	θ	
MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MAX	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	MAX		MIN	MAX
7.7	7.8	7.9	6.2	6.4	6.6	4.3	4.4	4.5	1.2	0.15	0.8	0.9	1.05	3.65	4.63	4.9	2.2	2.946	3.15	0.19	0.3	0.65	0°	8°

MBI5030 GTS Outline Drawing

Note: The unit for the outline drawing is mm.

Product Top Mark Information



Product Revision History

Datasheet version	Device Version Code
VA.00	C
VA.01	C
VA.02	C

Product Ordering Information

Product Ordering Number*	RoHS Compliant Package Type	Weight (g)
MBI5030GF-C	SOP24L-300-1.00	0.30
MBI5030GTS-C	TSSOP24L-173 -0.65	0.0967
MBI5030GFN-C	QFN24L-4*4- 0.5	0.0379

*Please place your order with the ***"product ordering number"*** information on your purchase order (PO).

Disclaimer

Macroblock reserves the right to make changes, corrections, modifications, and improvements to their products and documents or discontinue any product or service without notice. Customers are advised to consult their sales representative for the latest product information before ordering. All products are sold subject to the terms and conditions supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

Macroblock's products are not designed to be used as components in device intended to support or sustain life or in military applications. Use of Macroblock's products in components intended for surgical implant into the body, or other applications in which failure of Macroblock's products could create a situation where personal death or injury may occur, is not authorized without the express written approval of the Managing Director of Macroblock. Macroblock will not be held liable for any damages or claims resulting from the use of its products in medical and military applications.