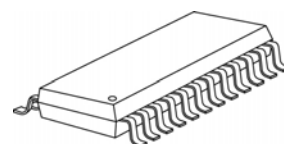# 16-Channel SPWM Constant Current LED Driver

Features

- 16 constant-current output channels
- 16-bit color depth PWM control
- Scrambled-PWM technology to improve refresh rate
- 6-bit programmable output current gain
- Constant output current range: 2~45mA
  2~ 45mA at 5.0V supply voltage
  2~30mA at 3.3V supply voltage
- Output current accuracy:
  Between channels: <±1.5% (typ.), and
  Between ICs: <±3% (typ.)
- Staggered delay of output, preventing from current surge
- Maximum data clock frequency: 30MHz
- Maximum gray scale clock frequency: 33MHz
  Refresh rate doubled by innovative rising/falling edge trigger GCLK
- Schmitt trigger input
- 3.0V-5.5V supply voltage

Small Outline Package

GF: SOP24L-300-1.00

Shrink SOP

GP: SSOP24L-150-0.64

Thin Shrink SOP

GTS: TSSOP24L-173-0.65

QFN

GFN: QFN24L-4*4-0.5

Product Description

MBI5042 is designed for LED video applications using internal Pulse Width Modulation (PWM) control with selectable 16-bit color depth which features a 16-bit shift register which converts serial input data into each pixel gray scale of output port. The output current can be preset through an external resistor. Moreover, the preset current of MBI5042 can be further programmed to 64 gain steps for LED global brightness adjustment.
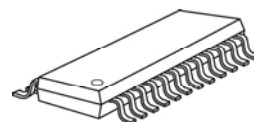
With Scrambled-PWM (S-PWM) technology, MBI5042 enhances Pulse Width Modulation by scrambling the "on" time into several "on" periods. The enhancement equivalently increases the visual refresh rate. When building a 16-bit color depth video, S-PWM reduces the flickers and improves the fidelity. MBI5042 offloads the signal timing generation of the host controller which just needs to feed data into drivers. MBI5042 drives the corresponding LEDs to the brightness specified by image data. With MBI5042, all output channels can be built with 16-bit color depth (65,536 gray scales). Each LED's brightness can be calibrated enough from minimum to maximum brightness with compensated gamma correction or LED deviation information inside the 16-bit image data.
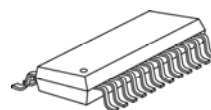
Block Diagram

Pin Configuration

MBI5042GF/GP/GTS

MBI5042GFN

Terminal Description

Pin Name	Function
GND	Ground terminal for control logic and current sink
SDI	Serial-data input to the shift register
DCLK	Clock input terminal used to shift data on rising edge and carries command information when LE is asserted.
LE	Data strobe terminal and controlling command with DCLK
$\overline{OUT0} \sim \overline{OUT15}$	Constant current output terminals
GCLK	Gray scale clock terminal Clock input for gray scale. The gray scale display is counted by gray scale clock comparing with input data.
SDO	Serial-data output to the receiver-end SDI of next driver IC
R-EXT	Input terminal used to connect an external resistor for setting up output current for all output channels
VDD	3.3V/5V supply voltage terminal

Equivalent Circuits of Inputs and Outputs

GCLK, DCLK, SDI terminal
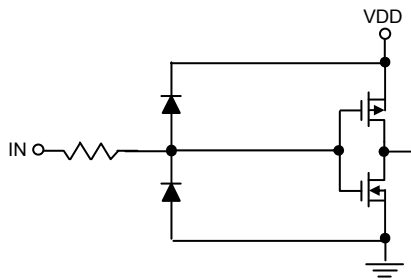
LE terminal
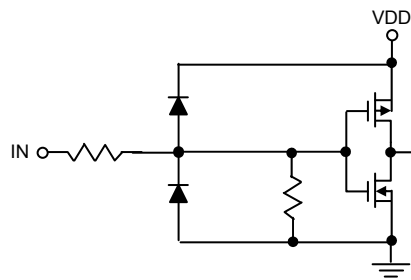
SDO terminal

Maximum Rating

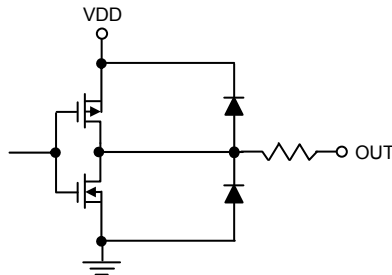| Characteristic		Symbol	Rating	Unit
Supply Voltage		V_{DD}	-0.5~+7	V
Input Pin Voltage (SDI)		V_{IN}	$-0.4~V_{DD}+0.4$	V
Output Current		I_{OUT}	+45	mA
Sustaining Voltage at OUT Port		V_{DS}	-0.5~+17	V
GND Terminal Current		I_{GND}	+720	mA
Power Dissipation (On PCB, Ta=25°C)*	GF Type	P_D	2.52	W
	GPType		2.03	
	GTS Type		3.53	
	GFN Type		3.12	
Thermal Resistance (On PCB, Ta=25°C)*	GF Type	$R_{th(j-a)}$	49.69	°C/W
	GPType		61.56	
	GTS Type		35.45	
	GFN Type		40.01	
Junction Temperature		$T_{j,max}$	150**	°C
Operating Temperature		T_{opr}	-40~+85	°C
Storage Temperature		T_{stg}	-55~+150	°C
ESD Rating	Human Body Mode (MIL-STD-883G Method 3015.7)	HBM	Class 2 (2000V ~ 3999V)	-
	Machine Mode (JEDEC EIA/JESD22-A115)	MM	Class B (200V ~ 399V)	-

* The PCB size is 76.2mm*114.3mm in simulation. Please refer to JEDEC JESD51.

** Operation at the maximum rating for extended periods may reduce the device reliability; therefore, the suggested operation temperature of the device is under 125°C.

Note: The performance of thermal dissipation is strongly related to the size of thermal pad, thickness and layer numbers of the PCB. The empirical thermal resistance may be different from simulative value. User should plan for expected thermal dissipation performance by selecting package and arranging layout of the PCB to maximize the capability.
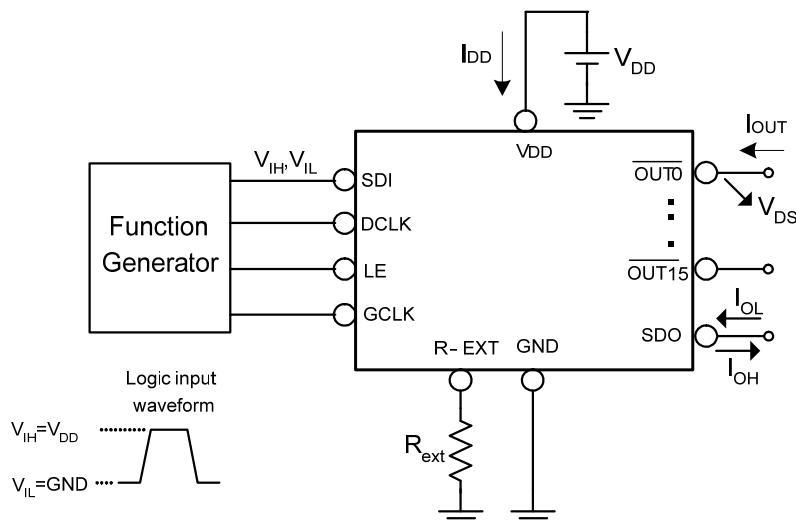
Electrical Characteristics (V_{DD}=5.0V)

Characteristics		Symbol	Condition		Min.	Typ.	Max.	Unit
Supply Voltage		V_{DD}	-		4.5	5.0	5.5	V
Sustaining Voltage at OUT Ports		V_{DS}	$\overline{OUT0}$ ~ $\overline{OUT15}$		-	-	17.0	V
Output Current		I_{OUT}	Refer to "Test Circuit for Electrical Characteristics"		2	-	45	mA
		I_{OH}	SDO		-	-	-1.0	mA
		I_{OL}	SDO		-	-	1.0	mA
Input Voltage	"H" level	V_{IH}	Ta=-40~85ºC		$0.7 \times V_{DD}$	-	V_{DD}	V
	"L" level	V_{IL}	Ta=-40~85ºC		GND	-	$0.3 \times V_{DD}$	V
Output Leakage Current		I_{OH}	V_{DS}=17.0V		-	-	0.5	µA
Output Voltage	SDO	V_{OL}	I_{OL}=+1.0mA		-	-	0.4	V
		V_{OH}	I_{OH}=-1.0mA		V_{DD}-0.4	-	-	V
Current Skew (Channel)		dI_{OUT}	I_{OUT}=20mA V_{DS}=1.0V	R_{ext}=700Ω	-	±1.5	±3.0	%
Current Skew (IC)		dI_{OUT2}	I_{OUT}=20mA V_{DS}=1.0V	R_{ext}=700Ω	-	±3.0	±6.0	%
Output Current vs. Output Voltage Regulation*		%/dV_{DS}	V_{DS} within 1.0V and 3.0V, R_{ext}=700Ω@20mA		-	±0.1	±0.3	% / V
Output Current vs. Supply Voltage Regulation*		%/dV_{DD}	V_{DD} within 4.5V and 5.5V		-	±1.0	±2.0	% / V
Pull-down Resistor		R_{IN}(down)	LE		250	450	800	KΩ
Supply Current	"Off"	I_{DD}(off) 1	R_{ext}=Open, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off		-	2.0	4.0	mA
		I_{DD}(off) 2	R_{ext}=6KΩ, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off		-	3.0	5.0	
		I_{DD}(off) 3	R_{ext}=700Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off		-	5.0	7.0	
		I_{DD}(off) 4	R_{ext}=348Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off		-	7.5	10.5	
	"On"	I_{DD}(on) 1	R_{ext}=6KΩ, $\overline{OUT0}$ ~ $\overline{OUT15}$ =On		-	3.0	5.0	
		I_{DD}(on) 2	R_{ext}=700Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =On		-	5.0	7.0	
		I_{DD}(on) 3	R_{ext}=348Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =On		-	8.0	11.0	

*One channel on.

Electrical Characteristics (V_{DD}=3.3V)

Characteristics		Symbol	Condition		Min.	Typ.	Max.	Unit
Supply Voltage		V_{DD}	-		3.0	3.3	3.6	V
Sustaining Voltage at OUT Ports		V_{DS}	$\overline{OUT0}$ ~ $\overline{OUT15}$		-	-	17.0	V
Output Current		I_{OUT}	Refer to "Test Circuit for Electrical Characteristics"		2	-	30	mA
		I_{OH}	SDO		-	-	-1.0	mA
		I_{OL}	SDO		-	-	1.0	mA
Input Voltage	"H" level	V_{IH}	Ta=-40~85ºC		$0.7 \times V_{DD}$	-	V_{DD}	V
	"L" level	V_{IL}	Ta=-40~85ºC		GND	-	$0.3 \times V_{DD}$	V
Output Leakage Current		I_{OH}	V_{DS}=17.0V		-	-	0.5	µA
Output Voltage	SDO	V_{OL}	I_{OL}=+1.0mA		-	-	0.4	V
		V_{OH}	I_{OH}=-1.0mA		V_{DD}-0.4	-	-	V
Current Skew (Channel)		dI_{OUT}	I_{OUT}=20mA V_{DS}=1.0V	R_{ext}=700Ω	-	±1.5	±30	%
Current Skew (IC)		dI_{OUT2}	I_{OUT}=20mA V_{DS}=1.0V	R_{ext}=700Ω	-	±3.0	±6.0	%
Output Current vs. Output Voltage Regulation		$\%/dV_{DS}$	V_{DS} within 1.0V and 3.0V, R_{ext}=700Ω@20mA		-	±0.1	±0.3	% / V
Output Current vs. Supply Voltage Regulation		$\%/dV_{DD}$	V_{DD} within 3.0V and 3.6V		-	±1.0	±2.0	% / V
Pull-down Resistor		R_{IN}(down)	LE		250	450	800	KΩ
Supply Current	"Off"	I_{DD}(off) 1	R_{ext}=Open, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off		-	2.0	4.0	mA
		I_{DD}(off) 2	R_{ext}=6KΩ, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off		-	3.0	5.0	
		I_{DD}(off) 3	R_{ext}=700Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off		-	4.5	6.5	
		I_{DD}(off) 4	R_{ext}=460Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off		-	5.0	7.0	
	"On"	I_{DD}(on) 1	R_{ext}=6KΩ, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off		-	3.0	5.0	
		I_{DD}(on) 2	R_{ext}=700Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off		-	4.5	6.5	
		I_{DD}(on) 3	R_{ext}=460Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off		-	5.5	7.5	

Test Circuit for Electrical Characteristics

Switching Characteristics (V_{DD}=5.0V), Test condition: Ta=25°C

Characteristics		Symbol	Condition	Min.	Typ.	Max.	Unit
Setup Time	SDI - DCLK ↑	t_{SU0}		7	-	-	ns
	LE ↑ – DCLK ↑	t_{SU1}		7	-	-	ns
	LE ↓ – DCLK ↑	t_{SU2}		7	-	-	ns
Hold Time	DCLK ↑ - SDI	t_{H0}		7	-	-	ns
	DCLK ↑ - LE ↓	t_{H1}		7	-	-	ns
Propagation Delay Time	DCLK - SDO	t_{PD0}	V_{DD}=5.0V $V_{IH}=V_{DD}$ V_{IL}=GND R_{ext}=700Ω V_{DS}=1.0V R_L=200Ω C_L=10pF C_1=100nF C_2=10µF C_{SDO}=10pF	-	25	30	ns
	GCLK – $\overline{OUT2n}$ [*]	t_{PD1}		-	30	60	ns
	LE – SDO [**]	t_{PD2}		-	30	60	ns
Staggered Delay of Output	$\overline{OUT2n}$ - $\overline{OUT2n+1}$ [*]	t_{DL1}		-	5	8	ns
Pulse Width	LE	$t_{w(L)}$		15	-	-	ns
	DCLK	$t_{w(DCLK)}$		10	-	-	ns
	GCLK	$t_{w(GCLK)}$		10	-	-	ns
	GCLK,2x	$t_{w(GCLK, 2x)}$		15	-	-	ns
Output Rise Time of Output Ports (High speed)		$t_{OR,HIGH}$		-	15	25	ns
Output Rise Time of Output Ports (Low speed)		$t_{OF,LOW}$		-	35	60	ns
Output Fall Time of Output Ports (High speed)		$t_{OF,HIGH}$		-	15	25	ns
Output Fall Time of Output Ports (Low speed)		$t_{OF,LOW}$			35	60	ns
Data Clock Frequency		F_{DCLK}		-	-	30	MHz
Gray Scale Clock Frequency [***]		F_{GCLK}		-	-	33	MHz
2x Gray Scale Clock Frequency [***]		$F_{GCLK, 2x}$		-	-	16.5	MHz

[*] Refer to the Timing Waveform, where n=0~7

[**] In timing of "Read Configuration", the next DCLK rising edge should be t_{PD2} after the falling edge of LE.

[***] With uniform output current.

Switching Characteristics (V_{DD}=3.3V), Test condition: Ta=25°C

| Characteristics		Symbol	Condition	Min.	Typ.	Max.	Unit
Setup Time	SDI - DCLK ↑	t_{SU0}		10	-	-	ns
	LE ↑ – DCLK ↑	t_{SU1}		10	-	-	ns
	LE ↓ – DCLK ↑	t_{SU2}		10	-	-	ns
Hold Time	DCLK ↑ - SDI	t_{H0}		10	-	-	ns
	DCLK ↑ - LE ↓	t_{H1}		10	-	-	ns
Propagation Delay Time	DCLK – $\overline{SDO}$	t_{PD0}	V_{DD}=3.3V V_{IH}=V_{DD} V_{IL}=GND R_{ext}=700Ω V_{DS}=1.0V R_L=200Ω C_L=10pF C_1=100nF C_2=10µF C_{SDO}=10pF	-	30	35	ns
	GCLK – $\overline{OUT2n}$ *	t_{PD1}		-	50	80	ns
	LE – SDO**	t_{PD2}		-	40	50	ns
Staggered Delay of Output	$\overline{OUT2n}$ - $\overline{OUT2n+1}$ *	t_{DL1}		-	8	10	ns
Pulse Width	LE	$t_{w(L)}$		15	-	-	ns
	DCLK	$t_{w(DCLK)}$		15	-	-	ns
	GCLK	$t_{w(GCLK)}$		15	-	-	ns
	GCLK,2x	$t_{w(GCLK, 2x)}$		25	-	-	ns
Output Rise Time of Output Ports (High speed)		$t_{OR,HIGH}$		-	25	35	ns
Output Rise Time of Output Ports (Low speed)		$t_{OF,LOW}$		-	45	70	ns
Output Fall Time of Output Ports (High speed)		$t_{OF,HIGH}$		-	25	35	ns
Output Fall Time of Output Ports (Low speed)		$t_{OF,LOW}$			45	70	ns
Data Clock Frequency		F_{DCLK}		-	-	25	MHz
Gray Scale Clock Frequency***		F_{GCLK}		-	-	20	MHz
2x Gray Scale Clock Frequency ***		$F_{GCLK, 2x}$		-	-	10	MHz

* Refer to the Timing Waveform, where n=0~7

** In timing of "Read Configuration", the next DCLK rising edge should be t_{PD2} after the falling edge of LE.
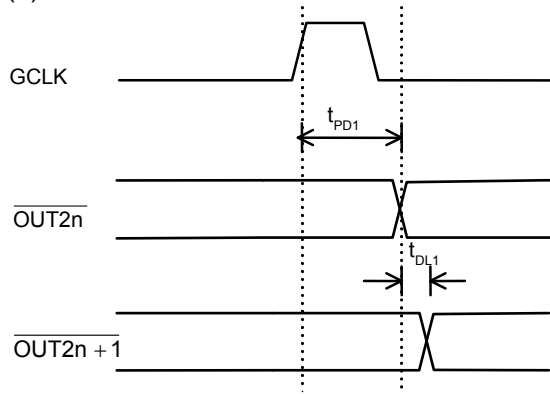
*** With uniform output current.

Test Circuit for Switching Characteristics
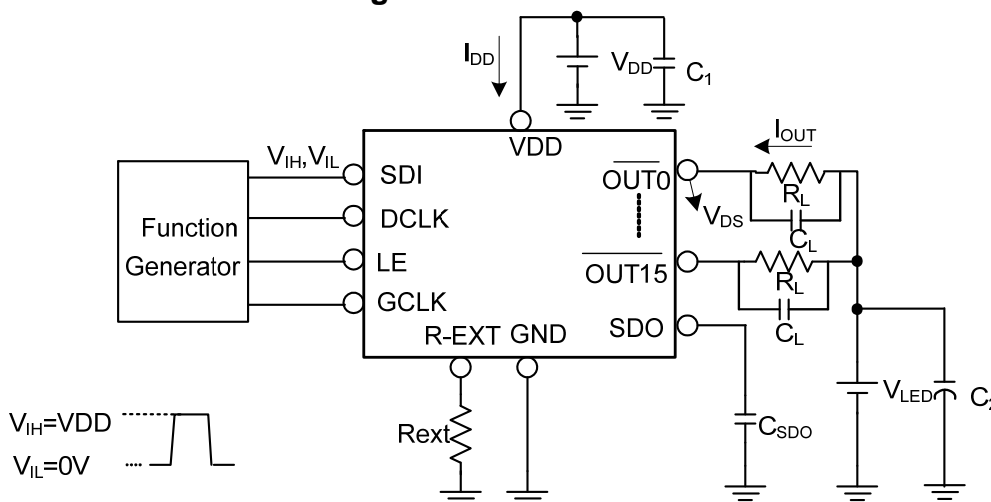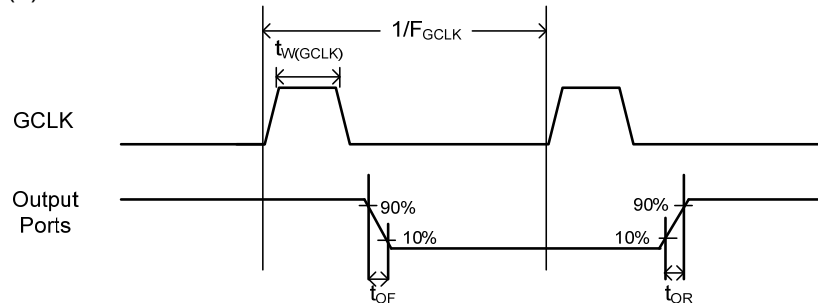
## Timing Waveform

(1)
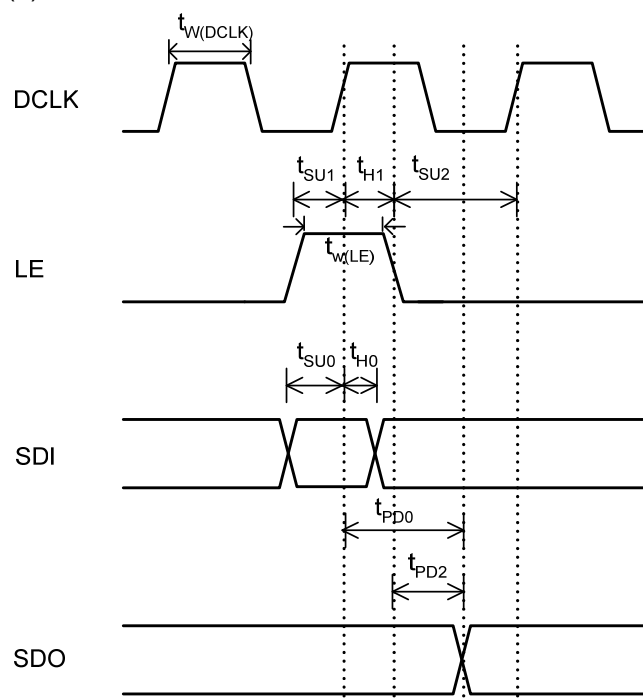
(2)

(3)

Principle of Operation

Control Command

| Command Name	Signals Combination		Description
	LE	**Number of DCLK Rising Edge when LE is asserted**	**The Action after a Falling Edge of LE**
Data Latch	High	1	Serial data are transferred to the buffers
Global Latch	High	3	Buffer data are transferred to the comparators
Read Configuration	High	5	Move out "configuration register" to the shift registers
Write Configuration	High	11	Serial data are transferred to the "configuration register"
Enable Write Configuration	High	15	To enable "Write Configuration"

Data Latch
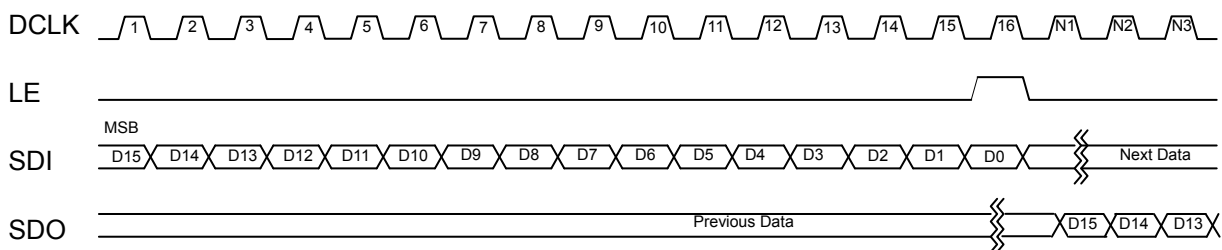
Global Latch
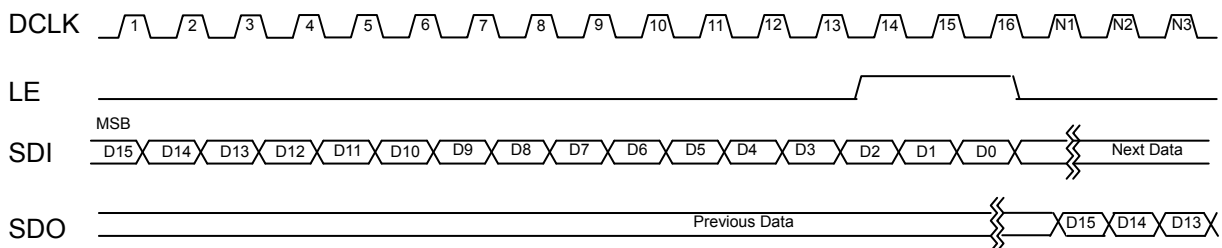
Read Configuration
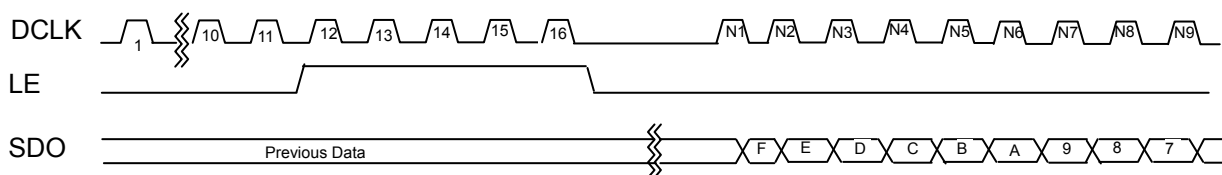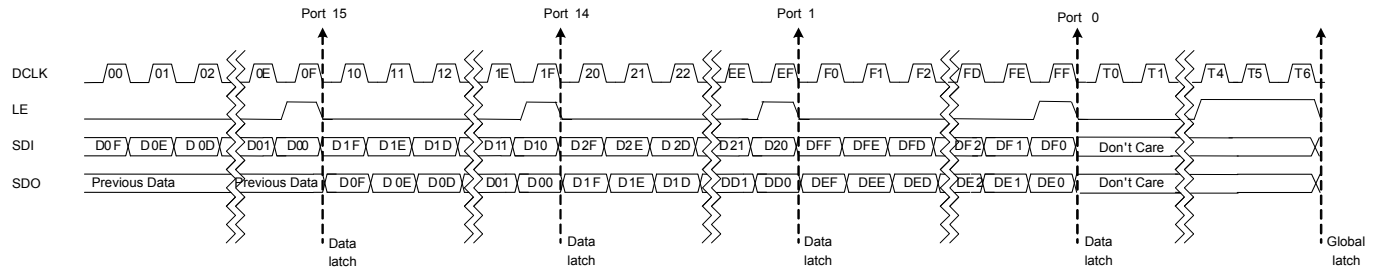

Write Configuration
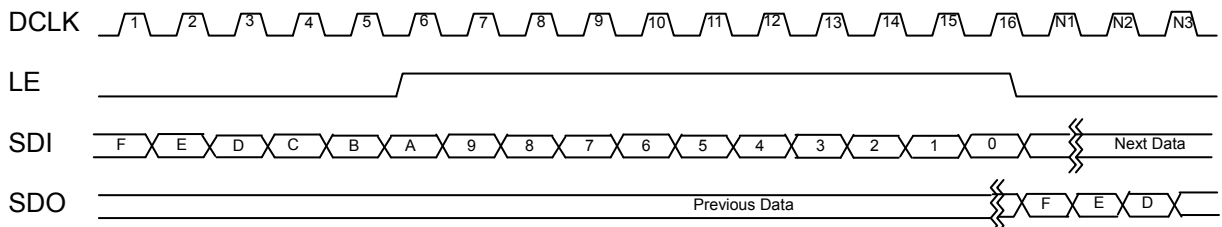
Setting Gray Scales of Pixels

MBI5042 implements the gray level of each output port using the S-PWM control algorithm. With the 16-bit data, all output channels can be built with 65,536 gray scales.

The 16-bit input shift register latches 16 times of the gray scale data into each data buffer with a "data latch" command sequentially. With a "global latch" command for additional latch, the 256-bit data buffers will be clocked in with the MSB first, loading the data from port 15 to port 0.

Full Timing for Data Loading

Definition of Configuration Register

MSB   LSB

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0

e.g.. Default Value

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	6'b101011						0	0	0	0

Bit	Attribute	Definition	Value	Function
F~E	Read/Write	GCLK shift	00	00: shift 0 GCLK 01: shift 2 GCLK 10: shift 4 GCLK 11: shift 8 GCLK
D	Read	Reserved	0	Please keep "0"
C	Read/Write	Stagger delay	0	0: enable 1: disable
A~B	Read	Reserved	00	Please keep "0"
9~4	Read/Write	Current gain adjustment	000000~ 111111	6'b101011 (Default, 100%) 000000:12.5% …. 111111:200%
3	Read/Write	GCLK rising/falling edge trigger	0	0: disable 1: enable
2	Read/Write	t_{OR} / t_{OF} speed switch	0	0: high speed 1: low speed
1~0	Read	Reserved	00	Please keep "00"

The PWM Counting Mode

MBI5042 supports S-PWM, scrambled PWM, technology. With S-PWM , the total PWM cycles can be broken down into MSB (Most Significant Bits) and LSB (Least Significant Bits) of gray scale cycles, and the MSB information can be dithered across many refresh cycles to achieve overall same high bit resolution.

MSB 10-bit PWM Counting, 1023 GCLKs

LSB 6-bit PWM counting

10-bit x 2^6 + 6-bit counting
# of GCLKs=$(2^{10}$-1$)$x2^6+2^6

64 times of MSB 10-bit PWM Counting
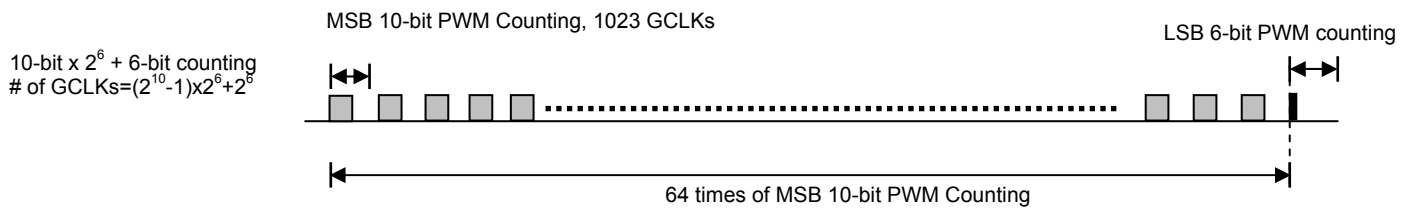
☐ : Output ports are turned "on".

Synchronization for PWM Counting

MBI5042 updates the next image data into output buffer immediately, no matter the counting status of previous image data is. In this mode, system controller will synchronize the GCLK according image data outside MBI5030 by itself. Otherwise, the conflict of previous image data and next image data will cause the data lost.

GCLK rising/falling edge trigger

Compared to output channel triggered by traditional rising edge, MBI5042 provides a feature in rising/falling edge trigger that can realize higher refresh rate at lower GCLK frequency to lower the impact of EMI. In rising/falling edge trigger mode, a 16-bit PWM cycle can be accomplished in 32,768 GCLK counts.
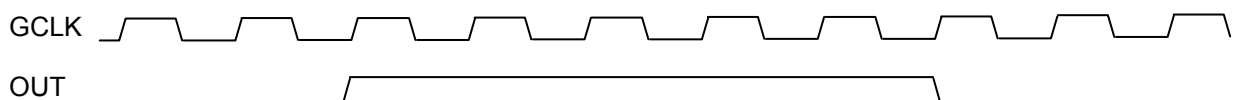
Rising edge trigger
GCLK=20Mhz, PWM=10

GCLK

OUT
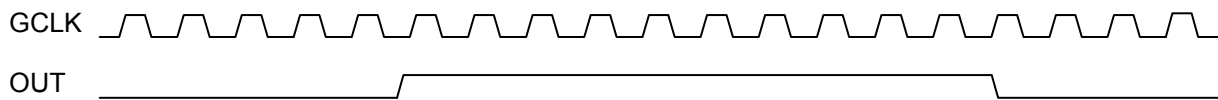
Rising/falling edge trigger
GCLK=10Mhz, PWM=10

GCLK

OUT

Please be noted, in rising/falling edge trigger mode, maximum GCLK frequency should be less 16.5Mhz to make sure of getting a uniform output because of t_{OR} and t_{OF} of output ports.

Constant Current

In LED display application, MBI5042 provides nearly no variation in current from channel to channel and from IC to IC. This can be achieved by:

1) The typical current variation between channels is less than 3.0%, and that between ICs is less than ±6.0%.

2) In addition, the current characteristic of output stage is flat and users can refer to the figure as shown below. The output current can be kept constant regardless of the variations of LED forward voltages (V_F). This guarantees LED to be performed on the same brightness as user's specification.
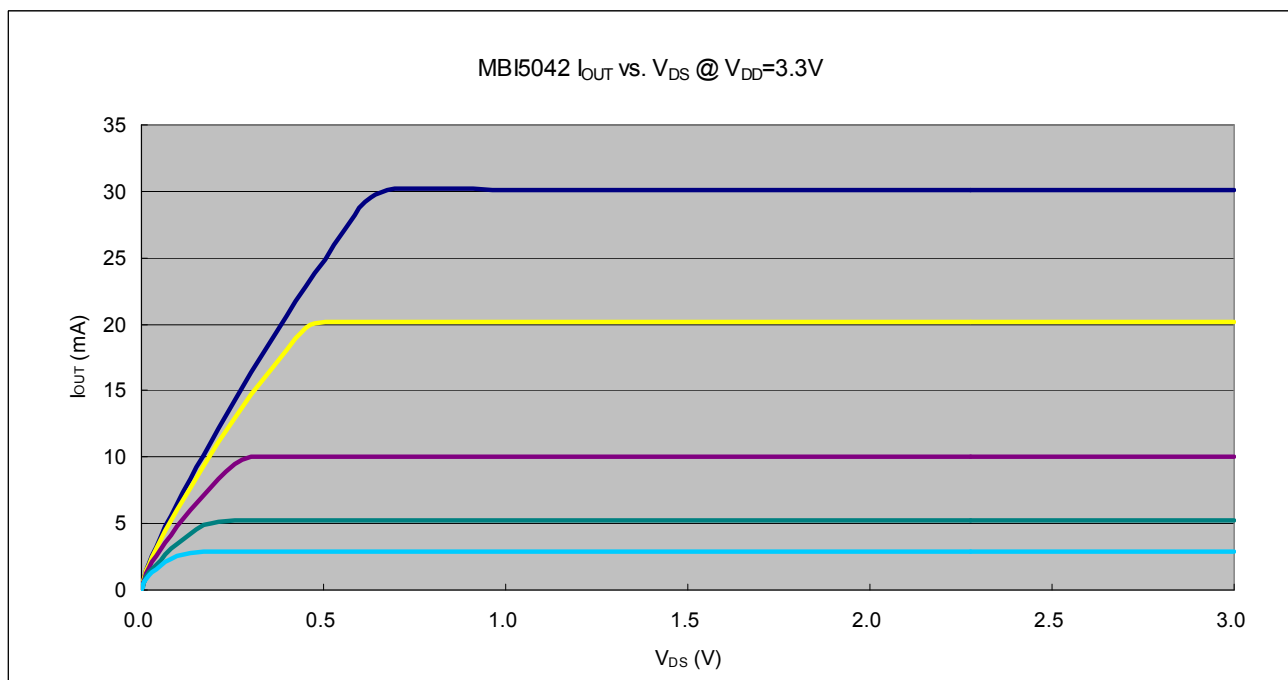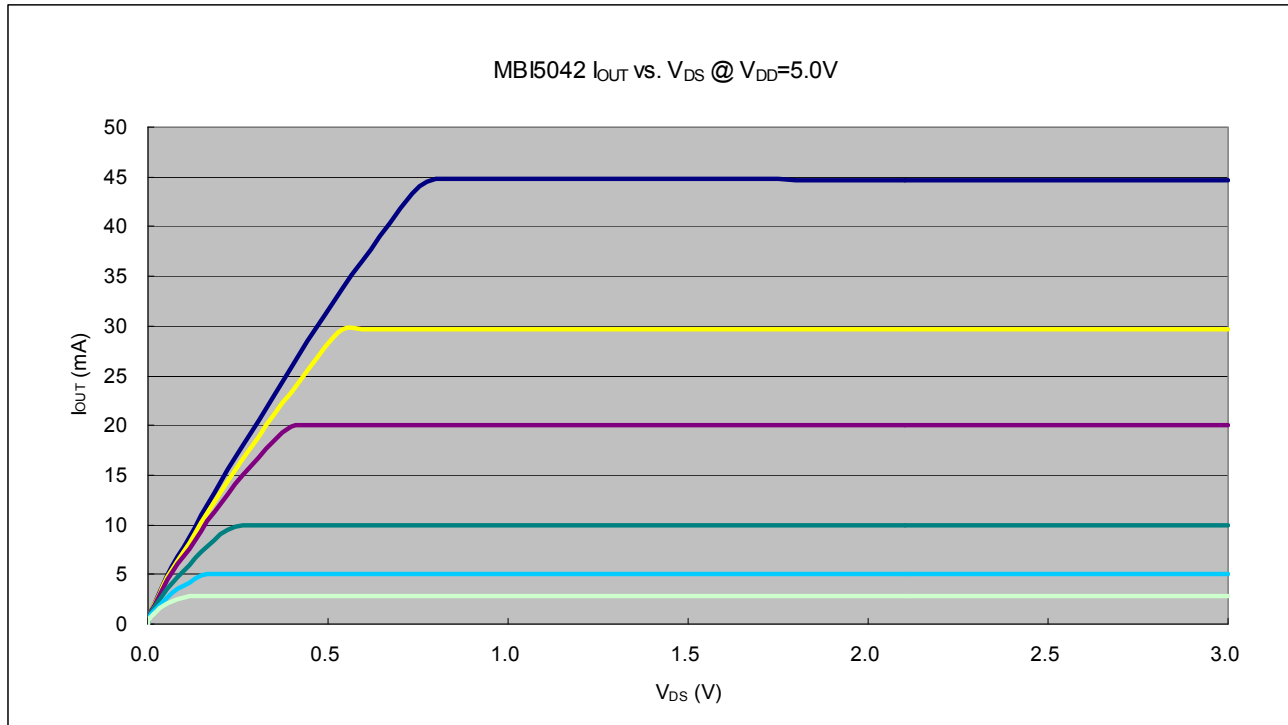
Setting Output Current

The output current (I_{OUT}) is set by an external resistor, R_{ext}. The default relationship between I_{OUT} and R_{ext} is shown in the following figure.
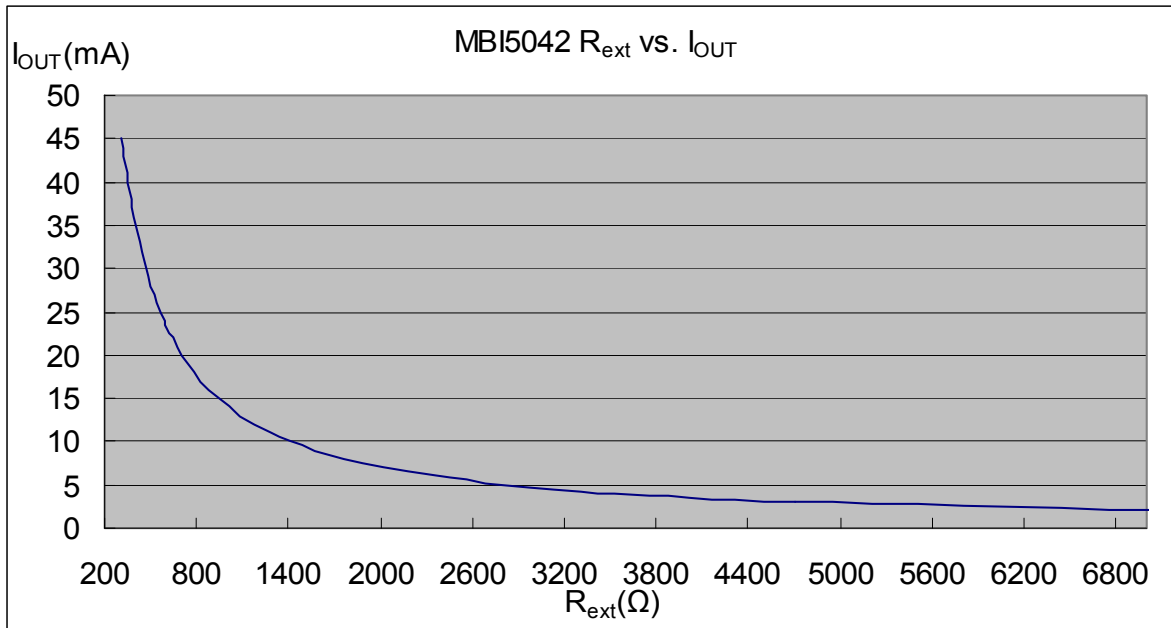
Also, the output current can be calculated from the equation:

V_{R-EXT}=0.61Volt x G; I_{OUT}=(V_{R-EXT}/R_{ext})x23

Whereas R_{ext} is the resistance of the external resistor connected to R-EXT terminal and V_{R-EXT} is its voltage. G is the digital current gain, which is set by the bit9 – bit4 of the configuration register. The default value of G is 1. For your information, the output current is about 20mA when R_{ext}=700Ω if G is set to default value The formula and setting for G are described in next section.

Current Gain Adjustment

Left graph:

Gain
1.938
1.615
1.246
Default value : 1
0.877
0.508
32 steps
0,0000 0,1000 0,1011 1,0000 1,1000 1,1111 (DA4~DA0)
Note: HC=1，Gain range=(1.938 ~ 0.508)

Right graph:

Gain
0.488
0.406
0.312
0.218
0.125
32 steps
0,0000 0,1000 1,0000 1,1000 1,1111 (DA4~DA0)
Note: HC=0，Gain range=(0.488 ~ 0.125)
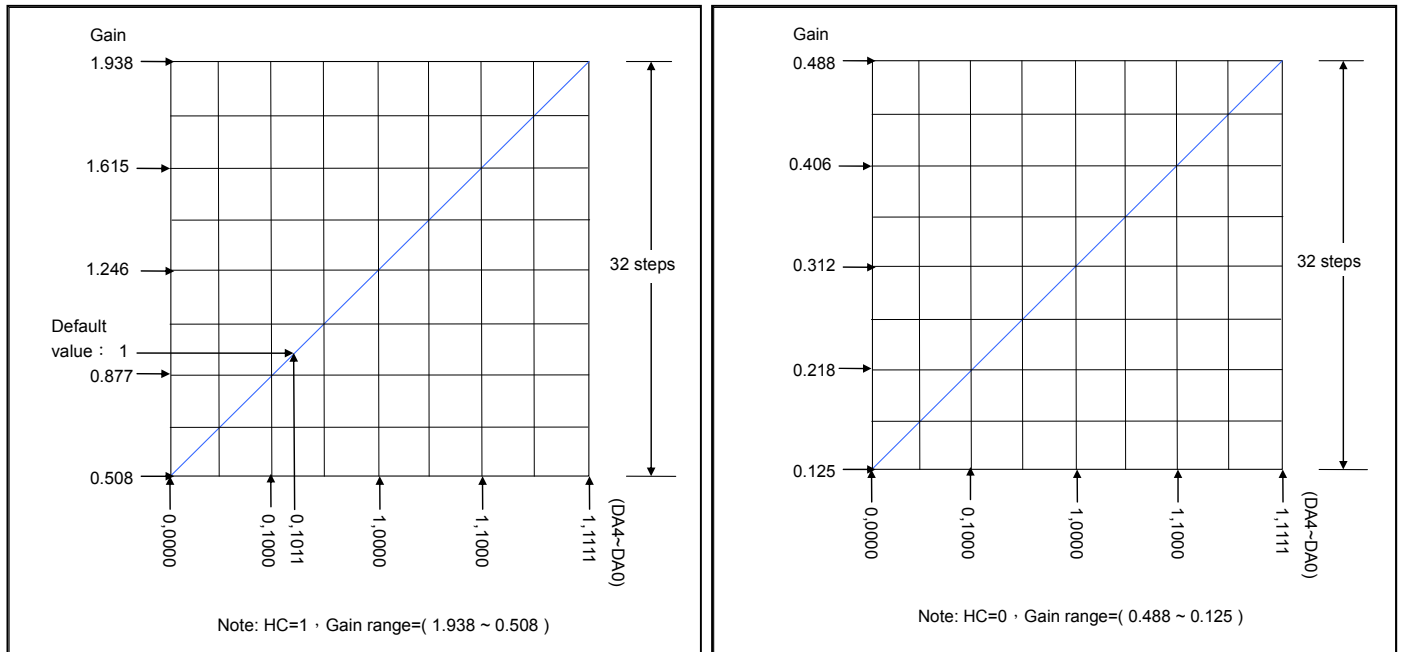
The bit 9 to bit 4 of the configuration register set the gain of output current, i.e., G. As totally 6-bit in number, i.e., ranged from 6'b000000 to 6'b111111, these bits allow the user to set the output current gain up to 64 levels. These bits can be further defined inside Configuration Register as follows:

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	HC	DA4	DA3	DA2	DA1	DA0	-	-	-	-

1. Bit 9 is HC bit. The setting is in low current band when HC=0, and in high current band when HC=1.
2. Bit 8 to bit 4 are DA4 ~ DA0.

The relationship between these bits and current gain G is:

HC=1, D=(65xG-33)/3

HC=0, D=(256xG-32)/3

and D in the above decimal numeration can be converted to its equivalent in binary form by the following equation:

D= $DA4 \times 2^4 + DA3 \times 2^3 + DA2 \times 2^2 + DA1 \times 2^1 + DA0 \times 2^0$

In other words, these bits can be looked as a floating number with 1-bit exponent HC and 5-bit mantissa DA4~DA0. For example,

HC=1, G=1.246, D=(65x1.246-33)/3=16

the D in binary form would be:

D=16= $1 \times 2^4 + 0 \times 2^3 + 0 \times 2^2 + 0 \times 2^1 + 0 \times 2^0$

The 6 bits (bit 5~bit 0) of the configuration register are set to 6'b110000.

Staggered Delay of Output

MBI5042 has a built-in staggered circuit to perform delay mechanism. Among output ports exist a graduated 5ns delay time among $\overline{OUT2n}$, and $\overline{OUT2n+1}$, by which the output ports will be divided to two groups at a different time so that the instant current from the power line will be lowered.

Soldering Process of "Pb-free & Green" Package Plating*

Macroblock has defined "Pb-Free & Green " to mean semiconductor products that are compatible with the current RoHS requirements and selected 100% pure tin (Sn) to provide forward and backward compatibility with both the current industry-standard SnPb-based soldering processes and higher-temperature Pb-free processes. Pure tin is widely accepted by customers and suppliers of electronic devices in Europe, Asia and the US as the lead-free surface finish of choice to replace tin-lead. Also, it is backward compatible to reflow processes which adopt tin/lead (SnPb) solder paste. Please refer to JEDEC J-STD-020C for temperature setting. However, in the whole Pb-free soldering processes and materials, 100% pure tin (Sn) will all require from 245 ^{o}C to 260°C for proper soldering on boards, referring to JEDEC J-STD-020C as shown below.
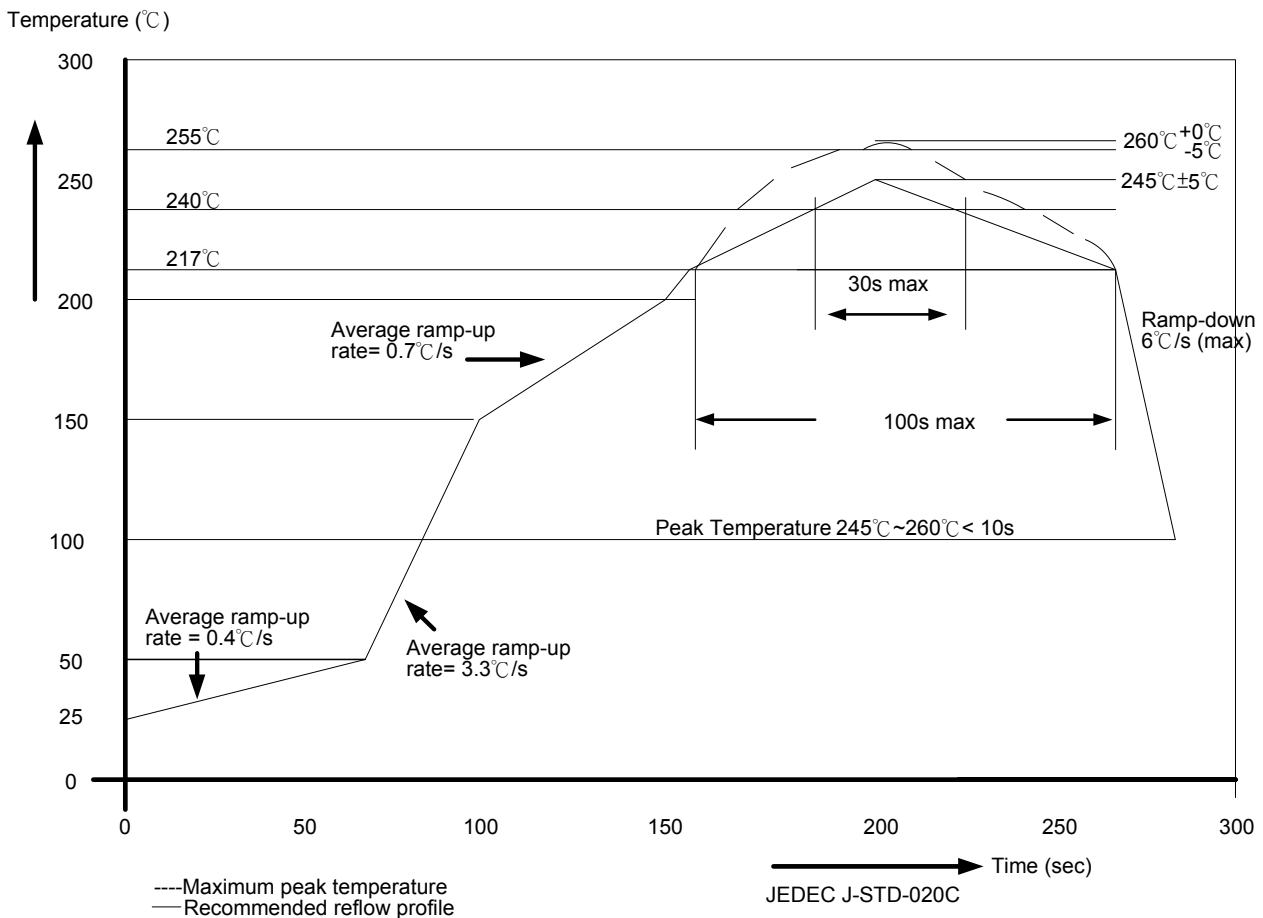
Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 $\geqq$2000
<1.6mm	260 +0 ^{o}C	260 +0 ^{o}C	260 +0 ^{o}C
1.6mm – 2.5mm	260 +0 ^{o}C	250 +0 ^{o}C	245 +0 ^{o}C
$\geqq$2.5mm	250 +0 ^{o}C	245 +0 ^{o}C	245 +0 ^{o}C

*Note: For details, please refer to Macroblock's "Policy on Pb-free & Green Package".

Package Power Dissipation (PD)

The maximum allowable package power dissipation is determined as $P_D(max)=(Tj–Ta)/R_{th(j-a)}$. When 16 output channels are turned on simultaneously, the actual package power dissipation is

$P_D(act)=(I_{DD}xV_{DD})+(I_{OUT}xDutyxV_{DS}x16)$. Therefore, to keep $P_D (act){\leq}P_D (max)$, the allowable maximum output current as a function of duty cycle is:

$I_{OUT}=\{[(Tj–Ta)/R_{th(j-a)}]–(I_{DD}xV_{DD})\}/V_{DS}$ /Duty/16, where Tj=150°C.

Device Type	$R_{th(j-a)}$ (°C/W)	P_D (W)
GF	49.69	2.52
GP	61.56	2.03
GTS	35.45	3.53
GFN	40.01	3.12

The maximum power dissipation, $P_D(max)=(Tj–Ta)/R_{th(j-a)}$, decreases as the ambient temperature increases.
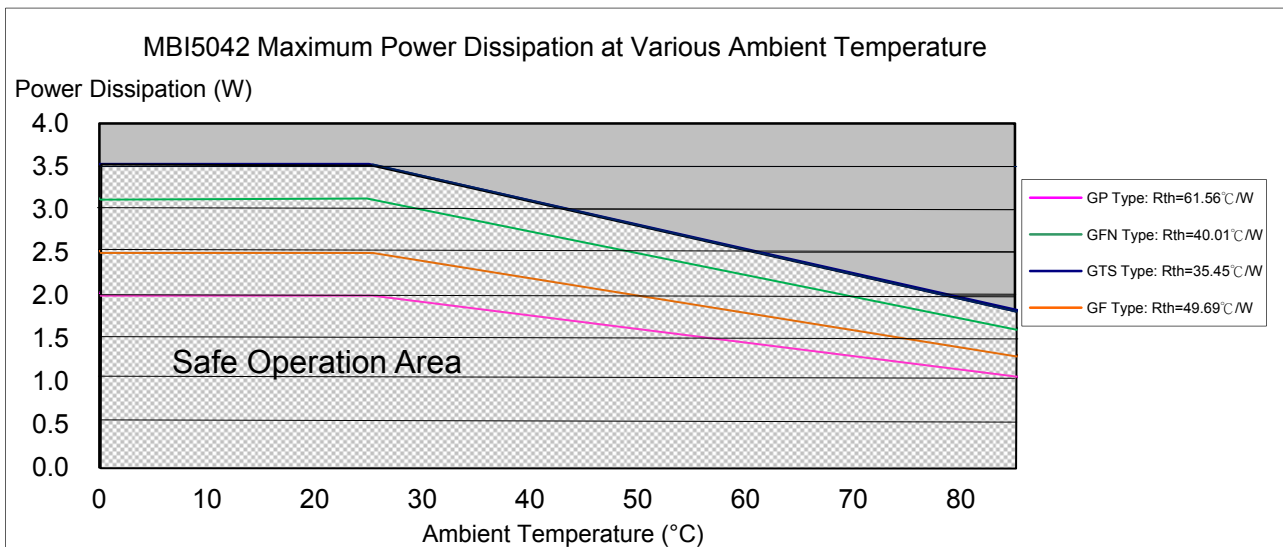
Usage of Thermal Pad

The PCB area L2xW2 is 4 times of the IC's area L1xW1.The thickness of the PCB is 1.6mm, copper foil 1 Oz. The thermal pad on the IC's bottom has to be mounted on the copper foil.
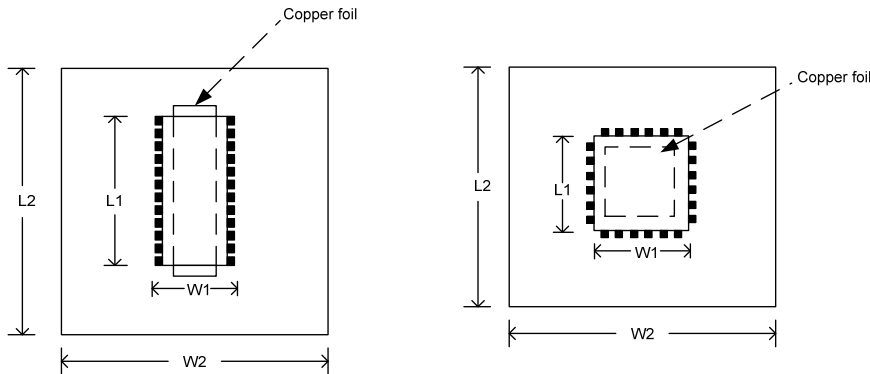
LED Supply Voltage (V_{LED})

MBI5042 are designed to operate with V_{DS} ranging from 0.4V to 1.0V (depending on I_{OUT}=2~45mA) considering the package power dissipating limits. V_{DS} may be higher enough to make $P_{D\ (act)}$ >$P_{D\ (max)}$ when V_{LED}=5V and V_{DS}=V_{LED}–V_F, in which V_{LED} is the load supply voltage. In this case, it is recommended to use the lowest possible supply voltage or to set an external voltage reducer, V_{DROP}.

A voltage reducer lets V_{DS}=(V_{LED}–V_F)–V_{DROP}.

Resistors or Zener diode can be used in the applications as shown in the following figures.
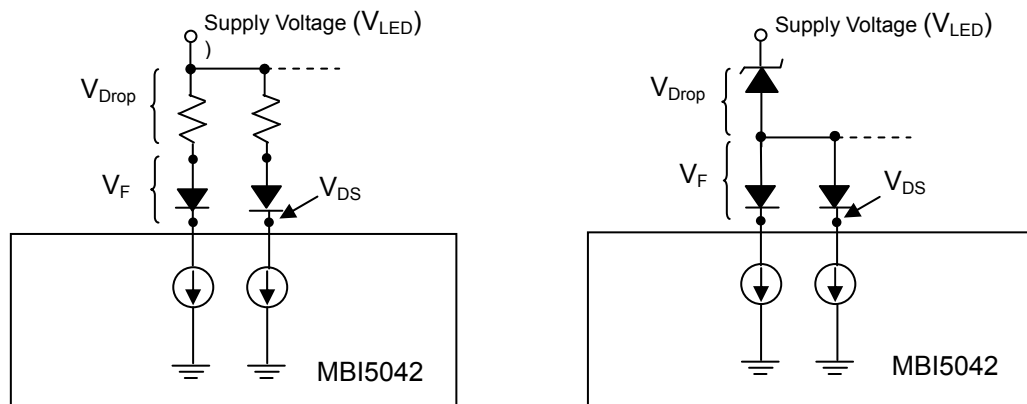
Switching Noise Reduction

LED drivers are frequently used in switch-mode applications which always behave with switching noise due to the parasitic inductance on PCB. To eliminate switching noise, refer to "Application Note for 8-bit and 16-bit LED Drivers- Overshoot".

Package Outline

MBI5042GF Outline Drawing

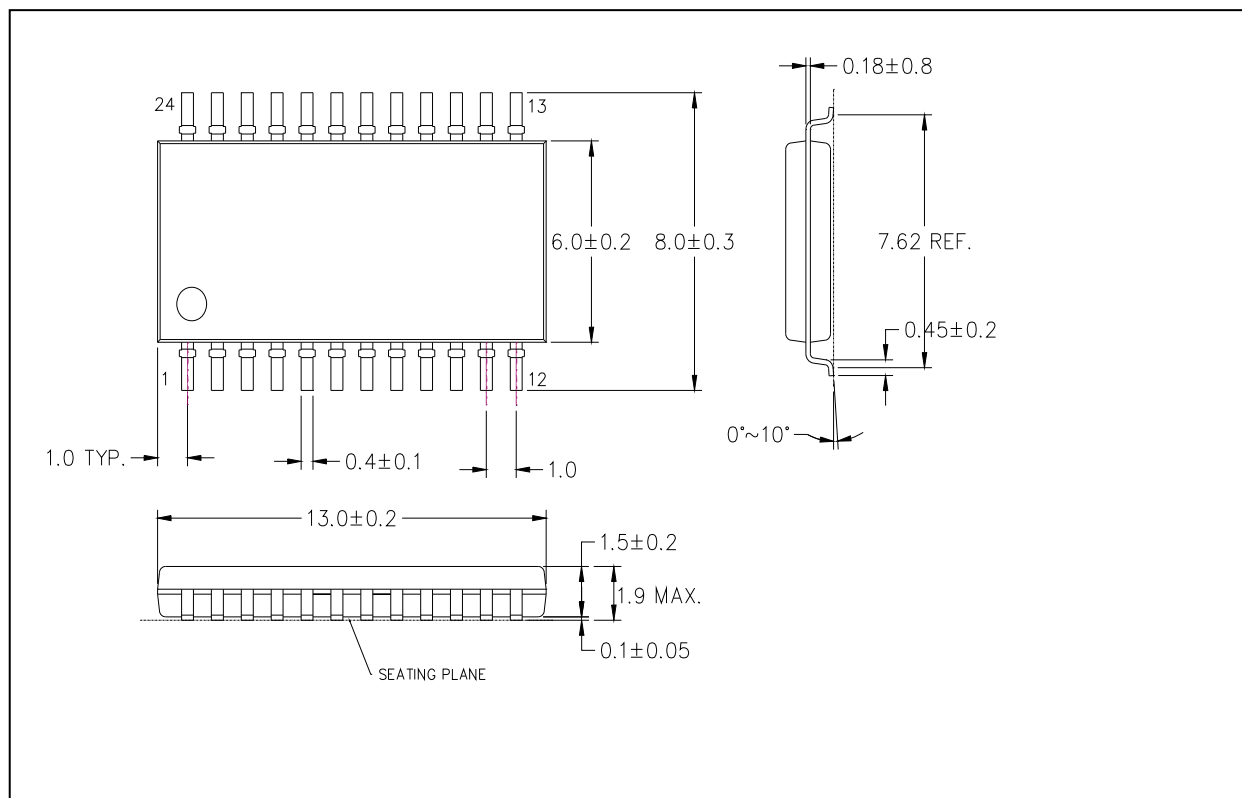| SYMBOLS	Dimensions shown in inchs			Dimensions shown in millimeters		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.053	0.064	0.069	1.346	1.626	1.753
A1	0.004	0.006	0.010	0.102	0.152	0.254
A2	—	—	0.059	—	—	1.499
D	0.337	0.341	0.344	8.560	8.661	8.738
E	0.228	0.236	0.244	5.791	5.994	6.198
E1	0.150	0.154	0.157	3.810	3.912	3.988
b	0.008	—	0.012	0.203	—	0.305
c	0.007	—	0.010	0.178	—	0.254
L	0.016	0.025	0.050	0.406	0.635	1.270
e	0.025 BASIC			0.635 BASIC		
L1	0.041 BASIC			1.0414 BASIC		
θ°	0	—	8	0	—	8

MBI5042GP Outline Drawing

Note: The unit for the outline drawing is mm.

THERMALLY ENHANCED VARIATIONS ONLY

Unit: mm

D			E			E1			A	A1	A2			D1			E2			b		e	θ	
MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MAX	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	MAX		MIN	MAX
7.7	7.8	7.9	6.2	6.4	6.6	4.3	4.4	4.5	1.2	0.15	0.8	0.9	1.05	3.65	4.63	4.9	2.2	2.946	3.15	0.19	0.3	0.65	0°	8°
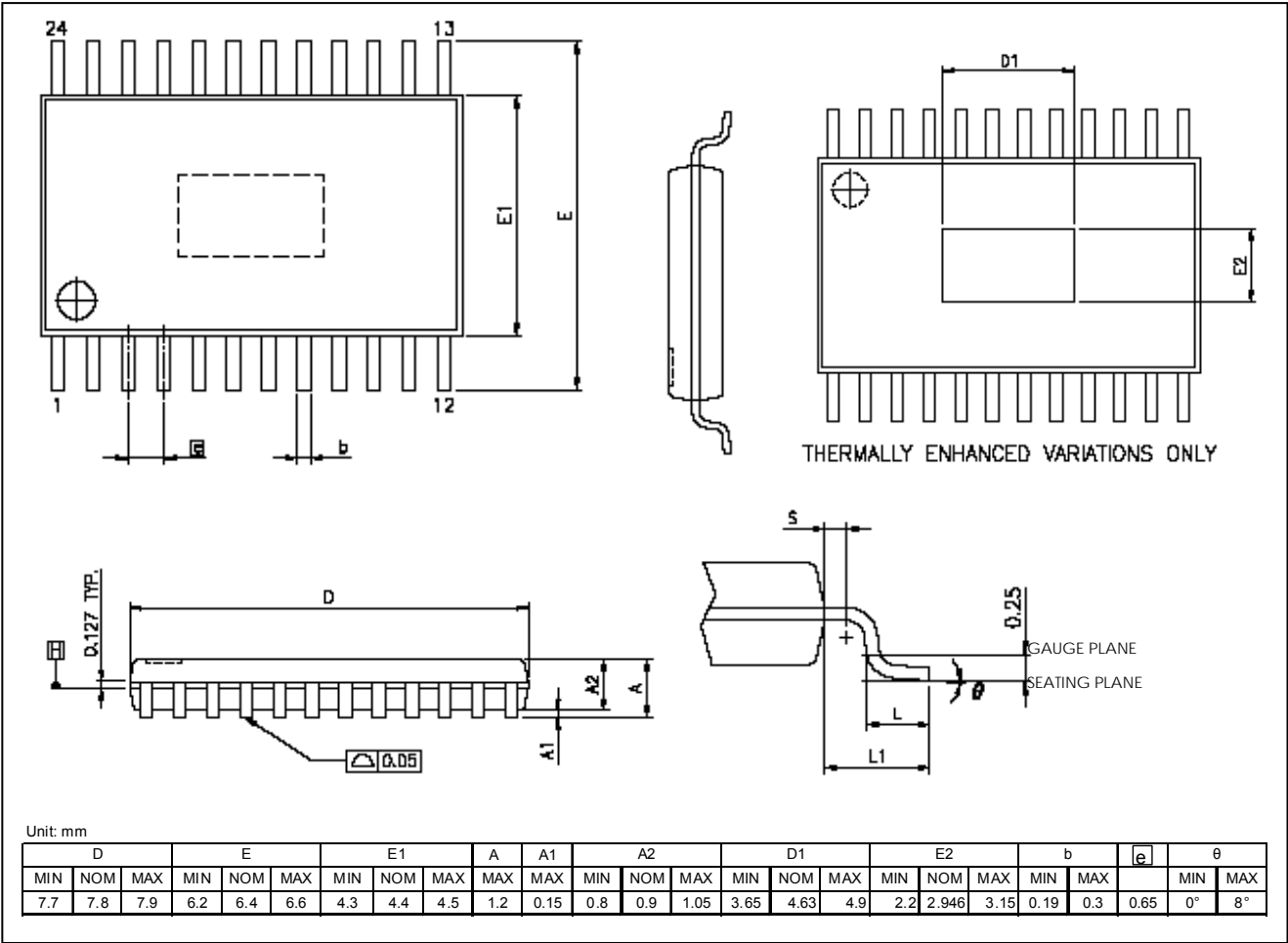
MBI5042 GTS Outline Drawing

| SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.01	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	3.90	4.00	4.10
D2	2.50REF		
e	0.50BSC		
Ne	2.50BSC		
Nd	2.50BSC		
E	3.90	4.00	4.10
E2	2.50REF		
L	0.35	0.40	0.45
h	0.30	0.35	0.40
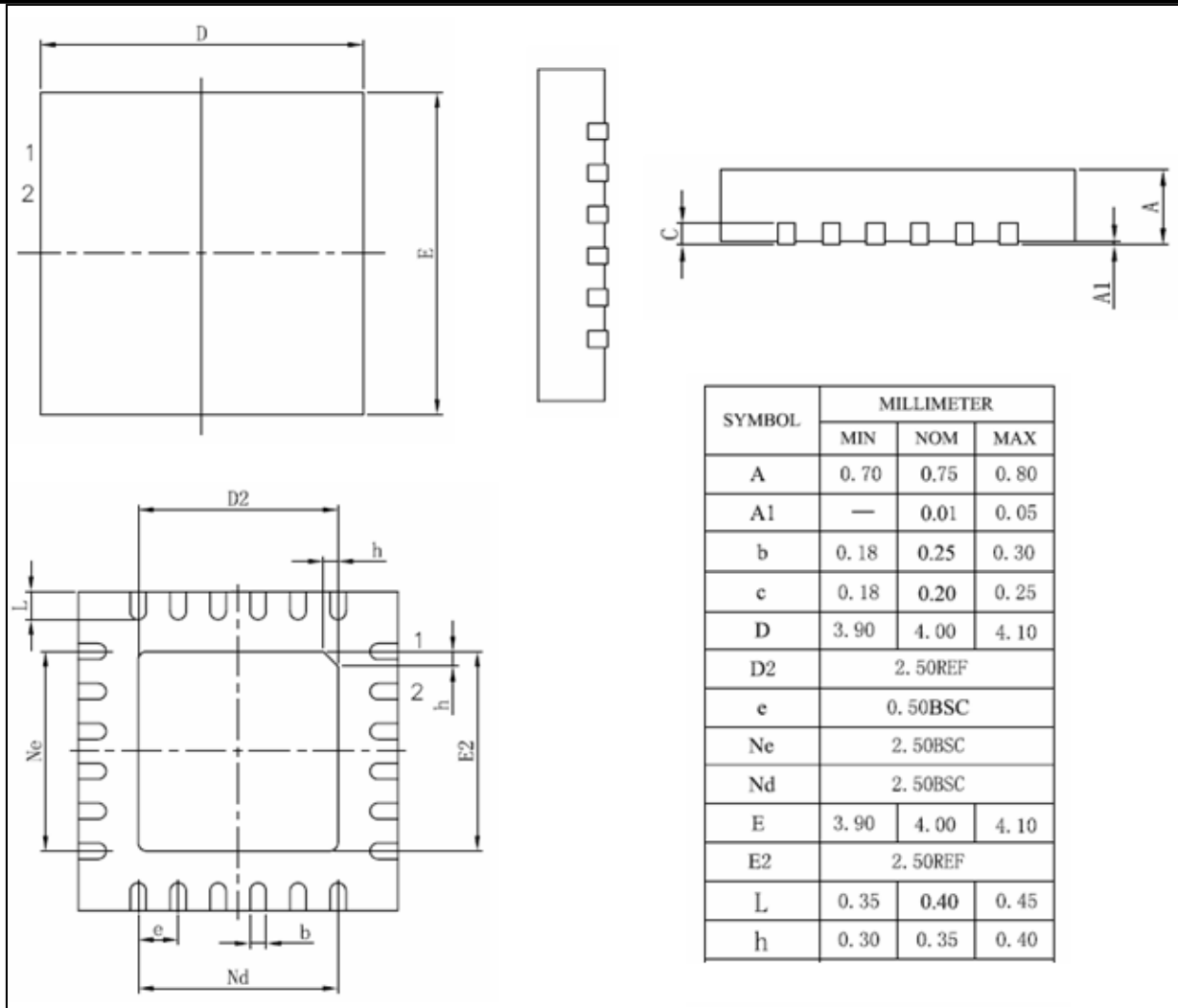
MBI5042 GFN Outline Drawing

Note 1: The unit of the outline drawing is millimeter (mm).
Note 2: The thermal pad size may exist a tolerance due to the manufacturing process, please use the maximum dimensions-D2(max. 2.50mm) x E2(max. 2.50mm) for the thermal pad layout. In addition, to avoid the short circuit risk, the vias or circuit traces shall not pass through the maximum area of thermal pad.

Product Top Mark Information
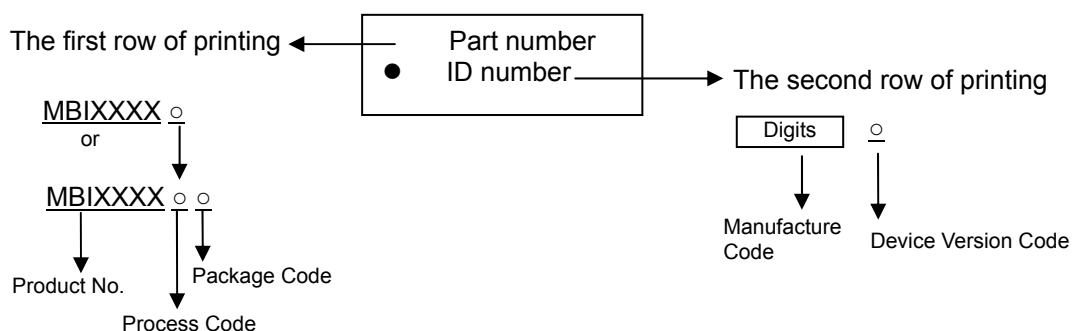
Product Revision History

Datasheet version	Device Version Code
VA.00	A
VA.01	A
VB.00	B
VB.01	B
VB.02	B

Product Ordering Information

Product Ordering Number*	"Pb-free & Green" Package Type	Weight (g)
MBI5042GF-B	SOP24L-300-1.00	0.28
MBI5042GP-B	SSOP24L-150-0.64	0.11
MBI5042GTS-B	TSSOP24L-173 -0.65	0.0967
MBI5042GFN-B	QFN24-4*4L-0.5	0.0379

*Please place your order with the *"product ordering number"* information on your purchase order (PO).

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