FUJITSU

October 1986
Edition 2.0

■ MBL8042H/N

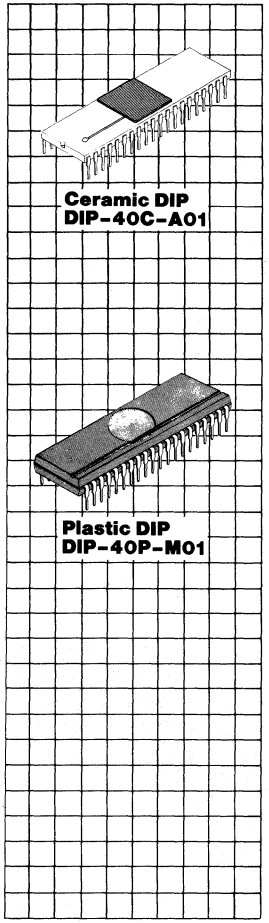
NMOS Universal Peripheral Interface 8-Bit Microcomputer

Description

The MBL8042 Universal Peripheral Interface is a single-chip 8-bit microcomputer based on an 8-bit parallel microprocessor chip.

The MBL8042 is fabricated with an N-channel silicon-gate MOS process. The MBL8042 has a 2K x 8-bit ROM for program memory, a 128 x 8-bit RAM for data memory, 18 I/O ports, an 8-bit timer/counter and clock generator on the chip, and is powered by single +5V.supply.

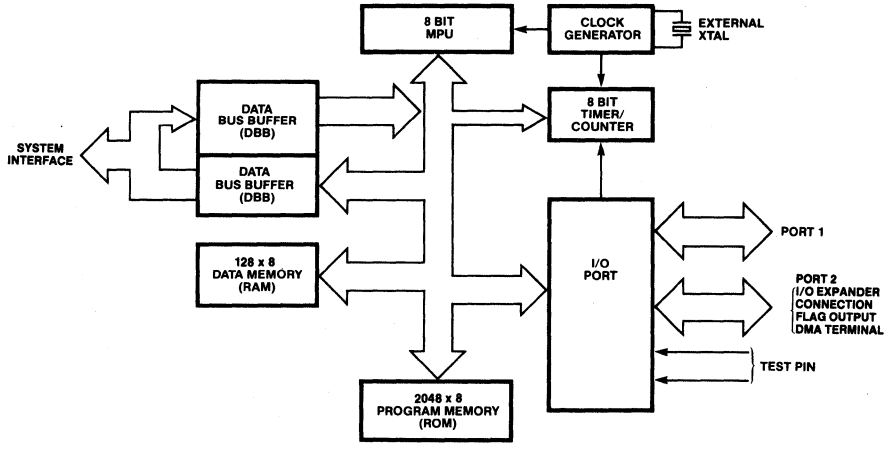
The MBL8042 is designed to operate as a slave processor, which receives commands and data from the master processor, controls peripheral devices and transfers input data from peripheral devices to the master processor. By using the MBL8042 an intelligent peripheral controller can be designed freely.



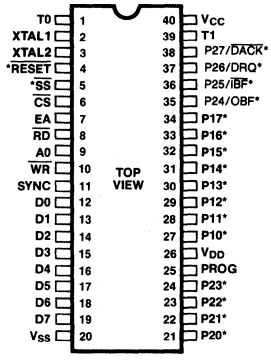
Features

- **Processor:**
  8-bit parallel processing
- **Register:**
  One 8-bit Status Register (for Interface with master processor)
  Two 8-bit Data Bus Buffer Registers (for Input/Output)
- **Memory**
  — 2K x 8 bit ROM (for program memory)
  — 128 x 8 bit RAM (for data memory)
- **I/O:**
  One 8-bit Bidirectional Data Bus
  Two 8-bit Bidirectional I/O Ports
  Two Test Inputs
- **Clock Source:**
  Clock Generator (with External Crystal Resonator) or External Clock
- **8-Bit Interval Timer/Event Counter**
- **Low-power Standby Operation Capability**
- **Power-on Reset Capability (with External Capacitor)**
- **Instruction Set:**
  93 Instructions (217 Instruction Codes)
  — 1-byte Instruction (about 70%), 2-byte Instruction (about 30%)
  — 1-cycle or 2-cycle Instruction (1 cycle = 2.5μs at 6MHz XTAL)
- **Technology:**
  N-channel Silicon-gate E/D MOS Process
- **Two Package Options:**
  Standard 40-pin Ceramic (Suffix-C) or Plastic DIP (Suffix-P)
- **Equivalent:**
  Intel 8042

Block Diagram



Pin Assignment



*These pins are internally pulled up

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Pin Descriptions

Pin No.	Name	Symbol	Description
1	Test 0	T_0	Conditional Input for Conditional Branch
2	Crystal 1	XTAL 1	Input pin for an internal Clock Generator connected to external crystal. Also, this pin can be used as input from an external clock source.
3	Crystal 2	XTAL 2	Input pin for an internal Clock Generater connected to external crystal. (Note: The XTAL 1 and XTAL 2 input levels are not TTL compatible).
4	Reset	$\overline{RESET}$	Resets and forces the MPU to be initialized. (Note: This input level is not TTL compatible).
5	Single Step	$\overline{SS}$	Input pin used for single step operation.
6	Chip Select	$\overline{CS}$	Input pin used for the master processor to select the UPI.
7	External Address	EA	Input pin used for controlling program memory access. Holding EA high forces all program memory fetches to reference external memory. Useful for emulation and debug, and essential for testing and program verification.
8	Read Strobe	$\overline{RD}$	Strobe input enables the MBL8042 to read contents of the Data Bus Buffer register or Status register.
9	Address "0"	A_0	Address input to read/write data or read/write commands. A_0 = "L" indicates data read or write. A_0 = "H" indicates status read or command write.
10	Write Strobe	$\overline{WR}$	Strobe input enables the MBL8042 to write data into its Data Buffer register.
11	Sync	SYNC	A clock output pin indicating the MBL8042 instruction cycle. This pin is used when a synchronization signal is required for external circuits.
12 thru 19	Data Bus	DB_0 thru DB_7	8-bit bidirectional I/O port used to interface the MBL8042 to the master processor.
20	Ground	V_{SS}	Ground terminal.
21 thru 24	Port 2	$P2_0$ thru $P2_3$	Lower 4 bits of the quasi-bidirectional I/O port (Port 2). These function as interface port with the I/O expander (MBL8243) when an expansion I/O executes instruction. During single step operation upper 3 bits of the program fetch address are output on P20, P21, P22.
25	Program	PROG	A strobe signal output pin for an I/O expander (MBL8243) used, when performing an expansion I/O instruction.
26	Power Supply	V_{DD}	Power supply pin (+5V) for internal RAM.
27 thru 34	Port 1	$P1_0$ thru $P1_7$	Quasi-bidirectional I/O ports (Port 1). During single step operation, the next program fetch address (Lower 8 bits) is output.
35 thru 38	Port 2	$P2_4$ thru $P2_7$	Upper 4 bits of the quasi-bidirectional I/O port (port 2). These function as the flag output pins ($P2_4$ and $P2_5$) and DMA pins ($P2_6$ and $P2_7$) according to instructions.
39	Test 1	T_1	This pin has the following functions according to instruction: 1. Event Input pin for the Event Counter. 2. Condition Input pin for Conditional Branch.
40	Power Supply	V_{CC}	Power supply pin (+5V).

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System Interface

The master processor and MBL8042 are interfaced through the data bus buffer.

MBL8042 has 2 internal DBB (Data Bus Buffer) registers. The register to be accessed is determined by the address line and strobe signal.

Flag 1 (F1) is set when a command is written (A_0 = 1), and reset when data is written (A_0 = 0).

The master processor can read only data from the output DBB register, and cannot read and check data or commands which the master processor has written itself.

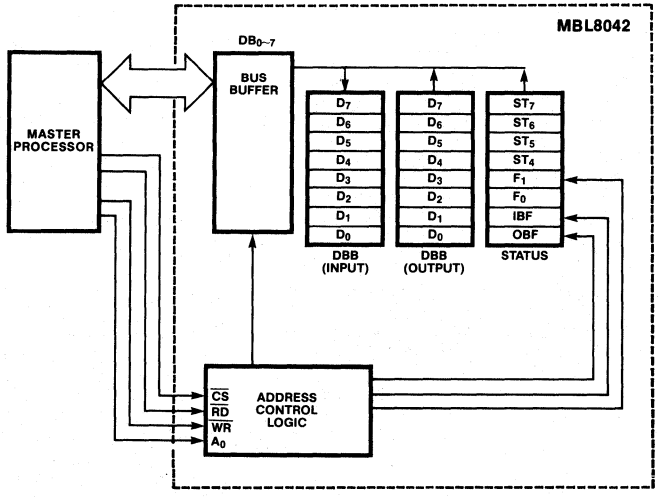
When MBL8042 writes data to the output DBB with the OUT DBB, A instruction, OBF is set.

When DBB is read ($\overline{CS}$ = RD = A_0 = 0, $\overline{WR}$ = 1) by the master processor, OBF is reset. IBF is set when the master processor writes to the DBB, and reset when MBL8042 reads data from the DBB with IN A, DBB instruction.

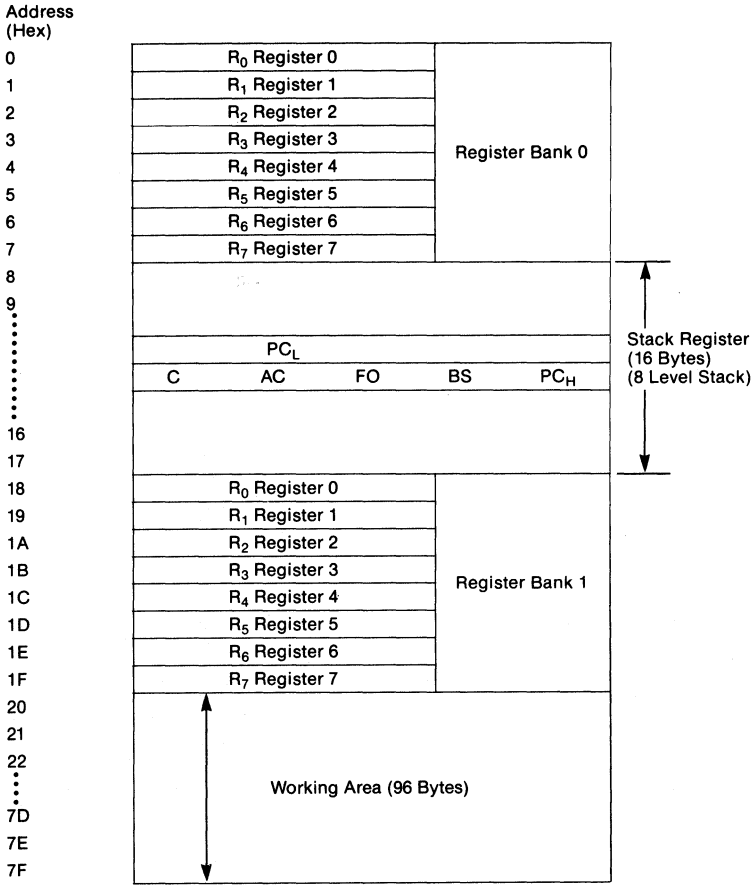
The internal status of the MBL8042 does not change when the status register contents are read out.

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A_0	Description
0	0	1	0	Read DBB (Output) register.
0	0	1	1	Read Status Register.
0	1	0	0	Write DBB (Input) register (Data).
0	1	0	1	Write DBB (Input) register (Command).
1	x	x	x	Invalid.

Interface between MBL8042 and Master Processor

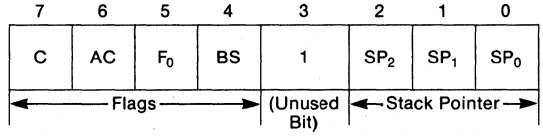


Resident Data Memory Map (RAM)



Status Register (PSW)

The Status Register is an 8-bit register configured as shown in the following figure. The upper four bits are used for flags to indicate the status of the MPU and when a sub-routine call or an interrupt occurs, the contents of the program counter is transferred to one of the 8 register pairs of the Stack Register as determined by the lower three bits of the Status Register. The remaining one bit is an unused bit.



Flags

C (Carry): When an overflow occurs in the Accumulator, this bit is set to "1".

AC (Auxiliary Carry): When an overflow occurs from Bit 3 to Bit 4 in the accumulator, this bit is set to "1".

F_0 (User Flag): This flag can be controlled as a user flag by the proper instruction.

BS (Bank Select): This flag can be controlled to select a Register Bank by an instruction. When BS = 0, Register Bank 0 is selected. When BS = 1, the Register Bank 1 is selected.

Stack Register (8 Level Capability)

The Stack Register has 16 bytes of memory area in the built-in RAM. The stack Register consists of eight levels, i.e. a Stack level consists of two bytes as shown below.

SP (Stack Pointer): In the diagram below, "SP" indicates a Stack Pointer address to be used for the next sub-routine call or interrupt. "SP" is given an 8-bit code from the lower three bits of Status Register as follows:

$SP = 00001SP_2SP_1SP_0$

$SP_2SP_1SP_0$ → Status Register Bits 0 to 2.

PC_n (Program Counter): "PC_n" indicates the contents of the n-th bit in the Program Counter.

Interrupt Processing (IBF Interrupt, Timer/Counter Interrupt)

There are two types of interrupt: the IBF interrupt and Timer/Counter interrupt.

If an interrupt occurs when the system is in "interrupt enable" status, the interrupt flag is set as soon as the current instruction is completed.

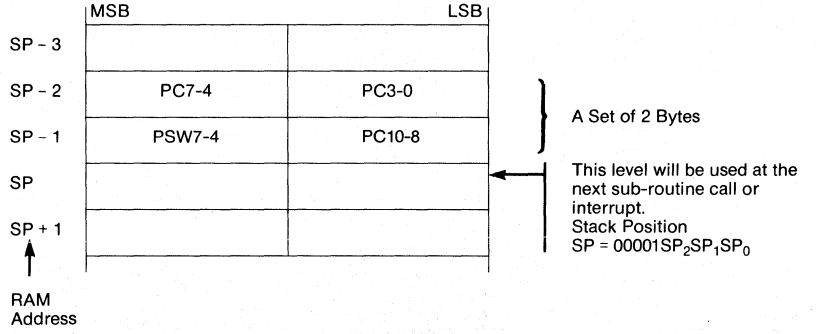
When the interrupt processing begins, the Status and Program Counter contents are first stored in the stack. Then, operation jumps to Address 3 in the case of the IBF interrupt and Address 7 in the case of a timer interrupt.

After the interrupt has been processed by a user program and RETR (Return and Restore Status) instruction has been executed, the Status and Program Counter contents stored in the stack are restored, the interrupt flag is reset and the system is ready to accept the next interrupt request.

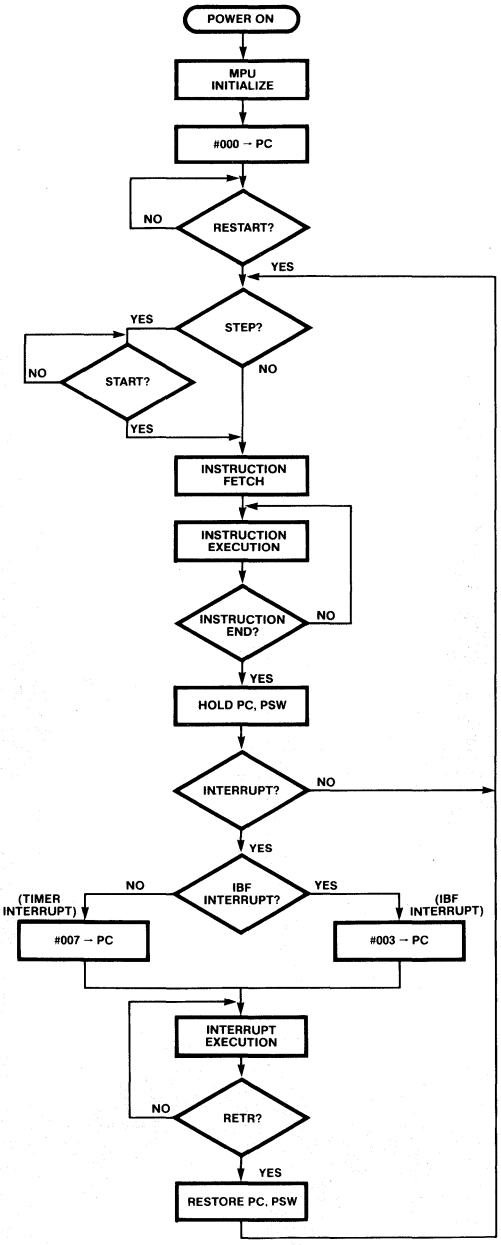
A Timer/Counter interrupt request occurs when the Timer/Counter overflow flag is set due to Timer/Counter overflow.

However, since the Timer/Counter interrupt request is masked by the IBF interrupt request, IBF interrupt has first priority.

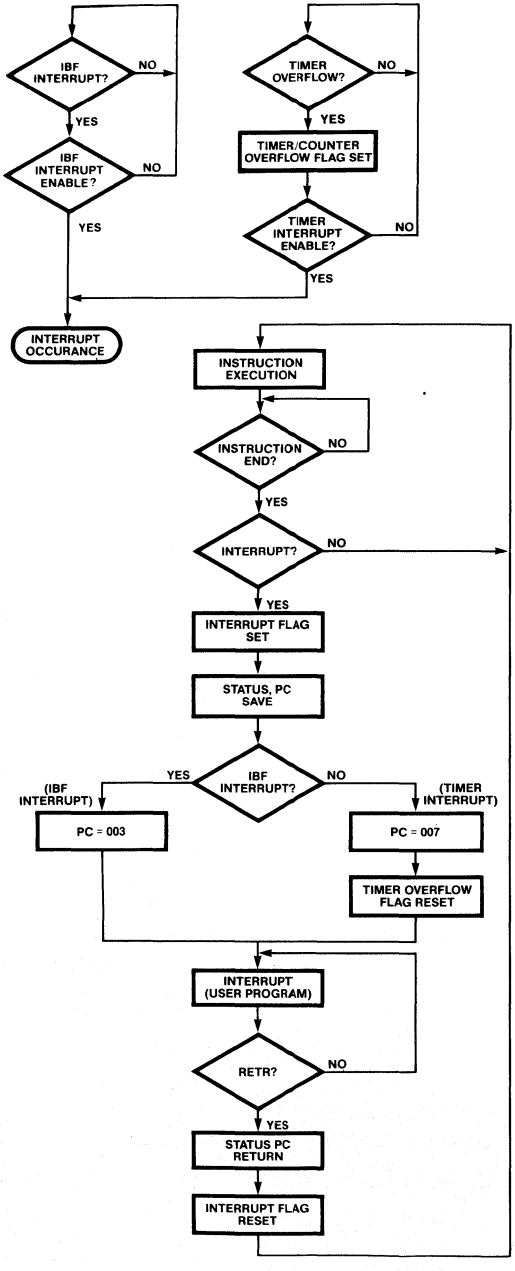
The Timer/Counter interrupt is enabled after the IBF interrupt has been executed and the system has become ready to receive the next interrupt request.



Operation Flow Chart



Interrupt Flow Chart



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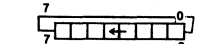
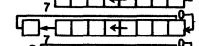
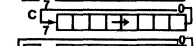
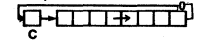
Instruction Set Summary

Accumulator

Operation	Mnemonic	OP Code	Byte	Cycle	Flag C	Flag AC	Note
Add register to A	ADD A, Rr	6X	1	1	*	*	(A) ← (A) + (Rr)
Add data memory to A	ADD A, @R0	60	1	1	*	*	(A) ← (A) + ((R0))
	ADD A, @R1	61	1	1	*	*	(A) ← (A) + ((R1))
Add immediate to A	ADD A, #data	03	2	2	*	*	(A) ← (A) + data
Add register to A with Carry	ADDC A, Rr	7X	1	1	*	*	(A) ← (A) + (Rr) + C
Add data memory to A with Carry	ADDC A, @R0	70	1	1	*	*	(A) ← (A) + ((R0)) + C
	ADDC A, @R1	71	1	1	*	*	(A) ← (A) + ((R1)) + C
Add immediate to A with Carry	ADDC A, #data	13	2	2	*	*	(A) ← (A) + data + C
AND register to A	ANL A, Rr	5X	1	1	—	—	(A) ← (A) AND (Rr)
AND data memory to A	ANL A, @R0	50	1	1	—	—	(A) ← (A) AND (R0)
	ANL A, @R1	51	1	1	—	—	(A) ← (A) AND (R1)
AND immediate to A	ANL A, #data	53	2	2	—	—	(A) ← (A) AND data
OR register to A	ORL A, Rr	4X	1	1	—	—	(A) ← (A) OR (Rr)
OR data memory to A	ORL A, @R0	40	1	1	—	—	(A) ← (A) OR ((R0))
	ORL A, @R1	41	1	1	—	—	(A) ← (A) OR ((R1))
OR immediate to A	ORL A, #data	43	2	2	—	—	(A) ← (A) OR data
Exclusive OR register to A	XRL A, Rr	DX	1	1	—	—	(A) ← (A) XOR (Rr)
Exclusive OR data memory to A	XRL A, @R0	D0	1	1	—	—	(A) ← (A) XOR ((R0))
	XRL A, @R1	D1	1	1	—	—	(A) ← (A) XOR ((R1))
Exclusive OR immediate to A	XRL A, #data	D3	2	2	—	—	(A) → (A) XOR data
Increment A	INC A	17	1	1	—	—	(A) ← (A) + 1
Decrement A	DEC A	07	1	1	—	—	(A) ← (A) - 1
Clear A	CLR A	27	1	1	—	—	(A) ← 0
Complement A	CPL A	37	1	1	—	—	(A) ← ($\bar{A}$)
Decimal Adjust A	DA A	57	1	1	*	—	Note (1)
Swap nibbles of A	SWAP A	47	1	1	—	—	(A7~4) ⇄ (A3~0)
Rotate A Left	RL A	E7	1	1	—	—	
Rotate A Left through Carry	RLC A	F7	1	1	*	—	
Rotate A Right	RR A	77	1	1	—	—	
Rotate A Right through Carry	RRC A	67	1	1	*	—	

Note 1: The accumulator value is adjusted to form BCD digits following the binary addition of BCD numbers.
Operation Code X: Table 1
Flag*: This flag is set or reset in the state after executed instruction.

Input/Output

Operation	Mnemonic	OP Code	Byte	Cycle	Flag C	Flag AC	Note
Input port to A	IN A, P1	09	1	2	—	—	(A) ← (P1)
	IN A, P2	0A	1	2	—	—	(A) ← (P2)
Output A to port	OUTL P1, A	39	1	2	—	—	(P1) ← (A)
	OUTL P2, A	3A	1	2	—	—	(P2) ← (A)
AND immediate to port	ANL P1, #data	99	2	2	—	—	(P1) ← (P1) AND data
	ANL P2, #data	9A	2	2	—	—	(P2) ← (P2) AND data
OR immediate to port	ORL P1, #data	89	2	2	—	—	(P1) ← (P1) OR data
	ORL P2, #data	8A	2	2	—	—	(P2) ← (P2) OR data
Input DBB to A, clear IBF	IN A, DBB	22	1	1	—	—	(A) ← (DBB), (IBF) ← 0
Output A to DBB, set OBF	OUT DBB, A	02	1	1	—	—	(DBB) ← (A), (OBF) ← 1
A7~4 to bits 7~4 of Status	MOV STS, A	90	1	1	—	—	(STS7~4) ← (A7~4)
Input Expander port to A	MOVD A, P_p	0X	1	2	—	—	(A3~0) ← (P_p), (A7~4) ← 0
Output A to Expander port	MOVD P_p, A	3X	1	2	—	—	(P_p) ← (A3~0)
AND A to Expander port	ANLD P_p, A	9X	1	2	—	—	(P_p) ← (P_p) AND (A3~0)
OR A to Expander port	ORLD P_p, A	8X	1	2	—	—	(P_p) ← (P_p) OR (A3~0)

Operation Code X: Table 2

Instruction Set Summary
(Continued)

Data Moves

Operation	Mnemonic	OP Code	Byte	Cycle	Flag C	Flag AC	Note
Move register to A	MOV A, Rr	FX	1	1	—	—	(A) ← (Rr)
Move data memory to A	MOV A, @R0	F0	1	1	—	—	(A) ← ((R0))
	MOV A, @R1	F1	1	1	—	—	(A) ← ((R1))
Move immediate to A	MOV A, #data	23	2	2	—	—	(A) ← data
Move A to register	MOV Rr, A	AX	1	1	—	—	(Rr) ← (A)
Move A to data memory	MOV @R0, A	A0	1	1	—	—	((R0)) ← (A)
	MOV @R1, A	A1	1	1	—	—	((R1)) ← (A)
Move immediate to register	MOV Rr, #data	BX	2	2	—	—	(Rr) ← data
Move immediate to data memory	MOV @R0, #data	B0	2	2	—	—	((R0)) ← data
	MOV @R1, #data	B1	2	2	—	—	((R1)) ← data
Move PSW to A	MOV A, PSW	C7	1	1	—	—	(A) ← (PSW)
Move A to PSW	MOV PSW, A	D7	1	1	*	*	(PSW) ← (A)
Exchange A and register	XCH A, Rr	2X	1	1	—	—	(A) ⇄ (Rr)
Exchange A and data memory	XCH A, @R0	20	1	1	—	—	(A) ⇄ ((R0))
	XCH A, @R1	21	1	1	—	—	(A) ⇄ ((R1))
Exchange digit of A and data memory	XCHD A, @R0	30	1	1	—	—	(A3~0) ⇄ ((R0)3~0)
	XCHD A, @R1	31	1	1	—	—	(A3~0) ⇄ ((R1)3~0)
Move to A from current page	MOVP A, @A	A3	1	2	—	—	(A) ← ((A)) within page
Move to A from Page 3	MOVP3 A, @A	E3	1	2	—	—	(A) ← ((A)) within page 3

Operation Code X: Table 1
Flag*: This flag is set or reset in the state after executed instruction.

Timer/Counter

Operation	Mnemonic	OP Code	Byte	Cycle	Flag C	Flag AC	Note
Read Timer/Counter	MOV A, T	42	1	1	—	—	(A) ← (T)
Load Timer/Counter	MOV T, A	62	1	1	—	—	(T) ← (A)
Start Timer	STRT T	55	1	1	—	—	
Start Counter	STRT CNT	45	1	1	—	—	
Stop Timer/Counter	STOP TCNT	65	1	1	—	—	
Enable Timer/ Counter Interrupt	EN TCNTI	25	1	1	—	—	
Disable Timer/ Counter Interrupt	DIS TCNTI	35	1	1	—	—	

Control

Operation	Mnemonic	OP Code	Byte	Cycle	Flag C	Flag AC	Note
Enable DMA Handshake Lines	EN DMA	E5	1	1	—	—	
Enable IBF Interrupt	EN I	05	1	1	—	—	
Disable IBF Interrupt	DIS I	15	1	1	—	—	
Enable Master Interrupts	EN FLAGS	F5	1	1	—	—	
Select register bank 0	SEL RB0	C5	1	1	—	—	(BS) ← 0
Select register bank 1	SEL RB1	D5	1	1	—	—	(BS) ← 1
No Operation	NOP	00	1	1	—	—	

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Instruction Set Summary
(Continued)

Register

Operation	Mnemonic	OP Code	Byte	Cycle	Flag C	Flag AC	Note
Increment register	INC Rr	1X	1	1	—	—	(Rr) ← (Rr) + 1
Increment data memory	INC @R0	10	1	1	—	—	((R0)) ← ((R0)) + 1
	INC @R1	11	1	1	—	—	((R1)) ← ((R1)) + 1
Decrement register	DEC Rr	CX	1	1	—	—	(Rr) ← (Rr) - 1

Operation Code X: Table 1

Subroutine

Operation	Mnemonic	OP Code	Byte	Cycle	Flag C	Flag AC	Note
Jump to Subroutine	CALL addr	%4	2	2	—	—	Note (2)
Return	RET	83	1	2	—	—	Note (3)
Return and restore status	RETR	93	1	2	*	*	Note (4)

Operation Code %: Table 3
Flag*: This flag is set or reset in the state after executed instruction.

Flags

Operation	Mnemonic	OP Code	Byte	Cycle	Flag C	Flag AC	Note
Clear Carry	CLR C	97	1	1	Z	—	(C) ← 0
Complement Carry	CPL C	A7	1	1	CP	—	(C) ← $(\overline{C})$
Clear Flag 0	CLR F0	85	1	1	—	—	(F0) ← 0
Complement Flag 0	CPL F0	95	1	1	—	—	(F0) ← $(\overline{F0})$
Clear Flag 1	CLR F1	A5	1	1	—	—	(F1) ← 0
Complement Flag 1	CPL F1	B5	1	1	—	—	(F1) ← $(\overline{F1})$

Flag Z: Reset CP: Invert

Branch

Operation	Mnemonic	OP Code	Byte	Cycle	Flag C	Flag AC	Note
Jump unconditional	JMP addr	%4	2	2	—	—	Unconditional Branch
Jump indirect	JMPP @A	B3	1	2	—	—	Unconditional Branch Note (5)
Decrement register and jump	DJNZ Rr,addr	EX	2	2	—	—	(Rr) ≠ 0 Note (6)
Jump on Carry = 1	JC addr	F6	2	2	—	—	(C) = 1
Jump on Carry = 0	JNC addr	E6	2	2	—	—	(C) = 0
Jump on A Zero	JZ addr	C6	2	2	—	—	(A) = 0
Jump on A not Zero	JNZ addr	96	2	2	—	—	(A) ≠ 0
Jump on T0 = 1	JT0 addr	36	2	2	—	—	(T0) = H
Jump on T0 = 0	JNT0 addr	26	2	2	—	—	(T0) = L
Jump on T1 = 1	JT1 addr	56	2	2	—	—	(T1) = H
Jump on T1 = 0	JNT1 addr	46	2	2	—	—	(T1) = L
Jump on F0 = 1	JF0 addr	B6	2	2	—	—	(F0) = 1
Jump on F1 = 1	JF1 addr	76	2	2	—	—	(F1) = 1
Jump on Timer Flag = 1, Clear Flag	JTF addr	16	2	2	—	—	(TF) = 1
Jump on IBF Flag = 0	JNIBF addr	D6	2	2	—	—	(IBF) = 0
Jump on OBF Flag = 1	JOBF addr	86	2	2	—	—	(OBF) = 1
Jump on Accumulator Bit	JBb addr	%2	2	2	—	—	(Ab) = 1

Operation Code X: Table 1
%: Table 3

Note 2: Call addr
((SP)) ← (PC), (PSW7~4)
(SP) ← (SP) + 1
(PC10 ~ 8) ← A_H
(PC7~0) ← A_L

Note 3: RET
(SP) ← (SP) - 1
(PC) ← ((SP))

Note 4: RETR
(SP) ← (SP) - 1
(PC) ← ((SP))
(PSW7~4) ← ((SP))

Note 5: JMPP @
(PC7~0) ← ((A))

Note 6: DJNZ Rr, addr
(Rr) ← (Rr) - 1
if (Rr) ≠ 0 (PC7~0) ← addr
if (Rr) = 0 Execute next instruction

Instruction Set Summary
(Continued)

OP Code Of Register Access (Table 1)

Mnemonic	Rr	R0	R1	R2	R3	R4	R5	R6	R7
ADD A,Rr		63	69	6A	6B	6C	6D	6E	6F
ADDC A,Rr		78	79	7A	7B	7C	7D	7E	7F
ANL A,Rr		58	59	5A	5B	5C	5D	5E	5F
DEC Rr		C8	C9	CA	CB	CC	CD	CE	CF
DJNZ Rr, addr		E8	E9	EA	EB	EC	ED	EE	EF
INC Rr		18	19	1A	1B	1C	1D	1E	1F
MOV A,Rr		F8	F9	FA	FB	FC	FD	FE	FF
MOV Rr,A		A8	A9	AA	AB	AC	AD	AE	AF
MOV Rr, #data		B8	B9	BA	BB	BC	BD	BE	BF
ORL A, Rr		48	49	4A	4B	4C	4D	4E	4F
XCH A,Rr		28	29	2A	2B	2C	2D	2E	2F
XRL A,Rr		D8	D9	DA	DB	DC	DD	DE	DF

bit

7	6	5	4	3	2	1	0
					r_2	r_1	r_0

OP Code Of Expander (Table 2)

Mnemonic	PP	P4	P5	P6	P7
ANLD P_P, A		9C	9D	9E	9F
MOVD A, P_P		0C	0D	0E	0F
MOVD P_P, A		3C	3D	3E	3F
ORLD P_P, A		8C	8D	8E	8F

bit

7	6	5	4	3	2	1	0
						P_1	P_0

OP Code Of JMP, CALL, JBb (Table 3)

	First Byte								Second Byte							
bit	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
JMP	A_H			0	0	1	0	0	A_L							
CALL	A_H			1	0	1	0	0	A_L							
JB_b	B_b			1	0	0	1	0	A_L							

A_H; Address A_{10}, A_9, A_8
A_L; Address A_7 to A_0
B_b; b-th Bit on Accumulator

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Instruction Codes

H \ L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP		OUT DBB,A	ADD A, #	JMP 0 x x	EN I		DEC A		IN A, P1	IN A, P2		MOVD A, P4	MOVD A, P5	MOVD A, P6	MOVD A, P7
1	INC @R0	INC @R1	JB0 addr	ADDC A, #	CALL 0 x x	DIS I	JTF addr	INC A	INC R0	INC R1	INC R2	INC R3	INC R4	INC R5	INC R6	INC R7
2	XCH A, @R0	XCH A, @R1	IN A, DBB	MOV A, #	JMP 1 x x	EN TCNTI	JNT0 addr	CLR A	XCH A, R0	XCH A, R1	XCH A, R2	XCH A, R3	XCH A, R4	XCH A, R5	XCH A, R6	XCH A, R7
3	XCHD A, @R0	XCHD A, @R1	JB1 addr		CALL 1 x x	DIS TCNTI	JT0 addr	CPL A		OUTL P1, A	OUTL P2, A		MOVD P4, A	MOVD P5, A	MOVD P6, A	MOVD P7, A
4	ORL A, @R0	ORL A, @R1	MOV A, T	ORL A, #	JMP 2 x x	STRT CNT	JNT1 addr	SWAP A	ORL A, R0	ORL A, R1	ORL A, R2	ORL A, R3	ORL A, R4	ORL A, R5	ORL A, R6	ORL A, R7
5	ANL A, @R0	ANL A, @R1	JB2 addr	ANL A, #	CALL 2 x x	STRT T	JT1 addr	DA A	ANL A, R0	ANL A, R1	ANL A, R2	ANL A, R3	ANL A, R4	ANL A, R5	ANL A, R6	ANL A, R7
6	ADD A, @R0	ADD A, @R1	MOV T, A		JMP 3 x x	STOP TCNT		RRC A	ADD A, R0	ADD A, R1	ADD A, R2	ADD A, R3	ADD A, R4	ADD A, R5	ADD A, R6	ADD A, R7
7	ADDC A, @R0	ADDC A, @R1	JB3 addr		CALL 3 x x		JF1 addr	RR A	ADDC A, R0	ADDC A, R1	ADDC A, R2	ADDC A, R3	ADDC A, R4	ADDC A, R5	ADDC A, R6	ADDC A, R7
8				RET	JMP 4 x x	CLR F0	JOBF addr			ORL P1, #	ORL P2, #		ORLD P4, A	ORLD P5, A	ORLD P6, A	ORLD P7, A
9	MOV STS, A		JB4 addr	RETR	CALL 4 x x	CPL F0	JNZ addr	CLR C		ANL P1, #	ANL P2, #		ANLD P4, A	ANLD P5, A	ANLD P6, A	ANLD P7, A
A	MOV @R0, A	MOV @R1, A		MOVP A, @A	JMP 5 x x	CLR F1		CPL C	MOV R0, A	MOV R1, A	MOV R2, A	MOV R3, A	MOV R4, A	MOV R5, A	MOV R6, A	MOV R7, A
B	MOV @R0, #	MOV @R1, #	JB5 addr	JMPP @A	CALL 5 x x	CPL F1	JF0 addr		MOV R0, #	MOV R1, #	MOV R2, #	MOV R3, #	MOV R4, #	MOV R5, #	MOV R6, #	MOV R7, #
C					JMP 6 x x	SEL RB0	JZ addr	MOV A, PSW	DEC R0	DEC R1	DEC R2	DEC R3	DEC R4	DEC R5	DEC R6	DEC R7
D	XRL A, @R0	XRL A, @R1	JB6 addr	XRL A, #	CALL 6 x x	SEL RB1	JNIBF addr	MOV PSW, A	XRL A, R0	XRL A, R1	XRL A, R2	XRL A, R3	XRL A, R4	XRL A, R5	XRL A, R6	XRL A, R7
E				MOVP3 A,@A	JMP 7 x x	EN DMA	JNC addr	RL A	DJNZ R0, addr	DJNZ R1, addr	DJNZ R2, addr	DJNZ R3, addr	DJNZ R4, addr	DJNZ R5, addr	DJNZ R6, addr	DJNZ R7, addr
F	MOV A, @R0	MOV A, @R1	JB7 addr		CALL 7 x x	EN FLAGS	JC addr	RLC A	MOV A, R0	MOV A, R1	MOV A, R2	MOV A, R3	MOV A, R4	MOV A, R5	MOV A, R6	MOV A, R7

#: Immediate data

1 Byte, 1 Cycle Instruction

1 Byte, 2 Cycle Instruction

2 Byte, 2 Cycle Instruction

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}, V_{DD}	-0.3 to +7.0	V
Input Voltage	V_{IN}	-0.3 to +7.0	V
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	-55 to +150	°C
Power Dissipation	P_D	1.5	W

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational specifications of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}, V_{DD}	+5.0 ±10%	V
	V_{SS}	0	V
Operating Temperature		0 to +70	°C

DC Characteristics

(T_A = 0° C to +70° C, V_{CC} = V_{DD} = 5.0V ± 10%, V_{SS} = 0V)

Parameter		Symbol	Test Conditions	Value Min.	Value Max.	Unit
Input Low Voltage	All Except XTAL1, 2, $\overline{RESET}$	V_{IL}		-0.3	0.8	V
	XTAL1,2, $\overline{RESET}$	V_{IL1}		-0.3	0.6	V
Input High Voltage	All Except XTAL1, 2, $\overline{RESET}$	V_{IH}		2.0	V_{CC}	V
	XTAL1,2, $\overline{RESET}$	V_{IH1}		3.8	V_{CC}	V
Output Low Voltage	DB_0 to DB_7	V_{OL}	I_{OL} = 2.0mA		0.45	V
	P10-P17, P20-P27 SYNC	V_{OL1}	I_{OL} = 1.6mA		0.45	V
	PROG	V_{OL2}	I_{OL} = 1.0mA		0.45	V
Output High Voltage	DB_0 to DB_7	V_{OH}	I_{OH} = -400μA	2.4		
	All other outputs	V_{OH1}	I_{OH} = -50μA	2.4		
Input Leakage Current	T_0, T_1, $\overline{RD}$, $\overline{WR}$, $\overline{CS}$, A_0, EA	I_{IL}	$V_{SS} \leqq V_{IN} \leqq V_{CC}$		±10	μA
Output Leakage Current	DB_0 to DB_7 (High Z State)	I_{OL}	V_{SS}+0.45V$\leqq$ $V_{IN} \leqq V_{CC}$		±10	μA
Input Low Current	$P1_0$ to $P1_7$ $P2_0$ to $P2_7$	I_{LI}	V_{IL} = 0.8V		0.5	mA
	$\overline{RESET}$, $\overline{SS}$	I_{LI1}	V_{IL} = 0.8V		0.2	mA
V_{DD} Supply Current		I_{DD}			15	mA
Supply Current		I_{CC} + I_{DD}			125	mA

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AC Characteristics

(T_A = 0°C to +70°C, V_{CC} = V_{DD} = 5.0V ± 10%, V_{SS} = 0V)

Data Bus Buffer Register Read (Refer to the Fig. 1)

Parameter		Symbol	Test Conditions	Value Min.	Value Max.	Unit
$\overline{CS}$, A_0 Setup Time (to $\overline{RD}$)		t_{AR}		0		ns
$\overline{CS}$, A_0 Hold Time (from $\overline{RD}$)		t_{RA}		0		ns
$\overline{RD}$ Pulse Width		t_{RR}		160		ns
Data Delay Time (from $\overline{CS}$, A_0)		t_{AD}	C_L = 150pF		130	ns
Data Delay Time (from $\overline{RD}$)		t_{RD}	C_L = 150pF		130	ns
Data Floating Time (from $\overline{RD}$)		t_{DF}			85	ns
Cycle Time	MBL8042N	t_{CY}	*	2.5	15.0	μs
	MBL8042H		**	1.25	15.0	μs

*t_{CY} = 2.50μs at 6MHz XTAL (N version)
**t_{CY} = 1.25μs at 12MHz XTAL (H version)

Data Bus Buffer Register Write (Refer to the Fig. 2)

Parameter	Symbol	Test Conditions	Value Min.	Value Max.	Unit
$\overline{CS}$, A_0 Setup Time (to $\overline{WR}$)	t_{AW}		0		ns
$\overline{CS}$, A_0 Hold Time (from $\overline{WR}$)	t_{WA}		0		ns
$\overline{WR}$ Pulse Width	t_{WW}		160		ns
Data Setup Time (to $\overline{WR}$)	t_{DW}		130		ns
Data Hold Time (from $\overline{WR}$)	t_{WD}		0		ns

Port 2 (Refer to the Fig. 3)*

Parameter	Symbol	MBL8042N Min.	MBL8042N Max.	MBL8042H Min.	MBL8042H Max.	Unit
Port Control Setup before Falling Edge of PROG Time (to PROG)	t_{CP}	100		110		ns
Port Control Hold after Falling Edge of PROG Time (from PROG)	t_{PC}	60		100		ns
Output Data Setup Time (to PROG)	t_{DP}	200		250		ns
Output Data Hold Time (from PROG)	t_{PD}	20		65		ns
Input Data Hold Time (from PROG)	t_{PF}	0	150	0	150	ns
PROG Time P2 Input Must be Valid	t_{PR}		650		810	ns
PROG Pulse Width	t_{PP}	700		1200		ns

*at 6MHz XTAL for N version
at 12MHz XTAL for H version

AC Characteristics
(Continued)

DMA Characteristics (Refer to the Fig. 4)

Parameter	Symbol	Test Conditions	Value Min.	Value Max.	Unit
DACK Setup Time (to RD, WR)	t_{ACC}		0		ns
DACK Hold Time (from RD, WR)	t_{CAC}		0		ns
Input Data Delay Time (from DACK)	t_{ACD}	C_L = 150pF		130	ns
DRQ Clear Time (from RD, WR)	t_{CRQ}			100	ns

AC Test Conditions
V_{IL} = 0.8V (All except XTAL1, 2, RESET)
= 0.6V (XTAL1, 2, RESET)
V_{IH} = 2.0V (All except XTAL1, 2, RESET)
= 3.8V (XTAL1, 2, RESET)
V_{OL} = 0.45V
V_{OH} = 2.4V

Output Load
D0–D7 : C_L = 150pF
All other outputs: C_L = 80pF

Timing Diagram

Figure 1. Data Bus Buffer (DBB) Read Operation

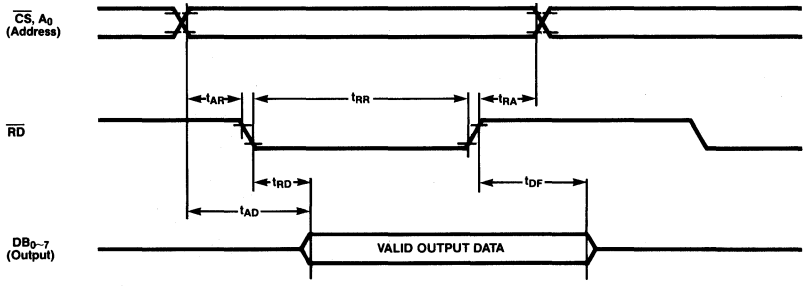
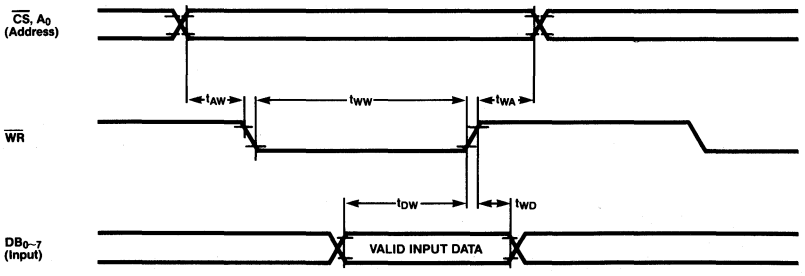


Figure 2. Data Bus Buffer (DBB) Write Operation



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Timing Diagram
(Continued)

Figure 3. Port 2 (Lower 4 Bits) Operation in Connection with I/O Expander

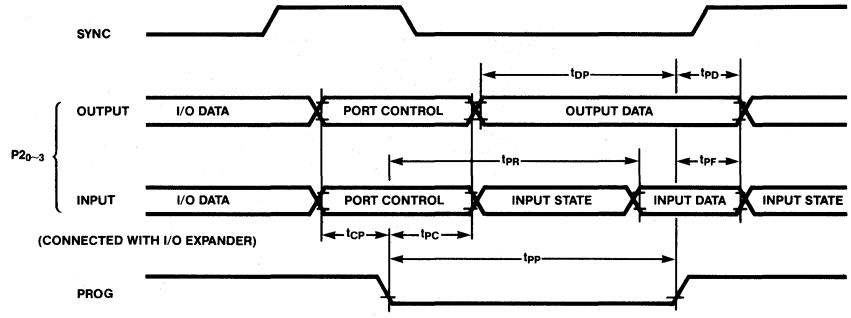
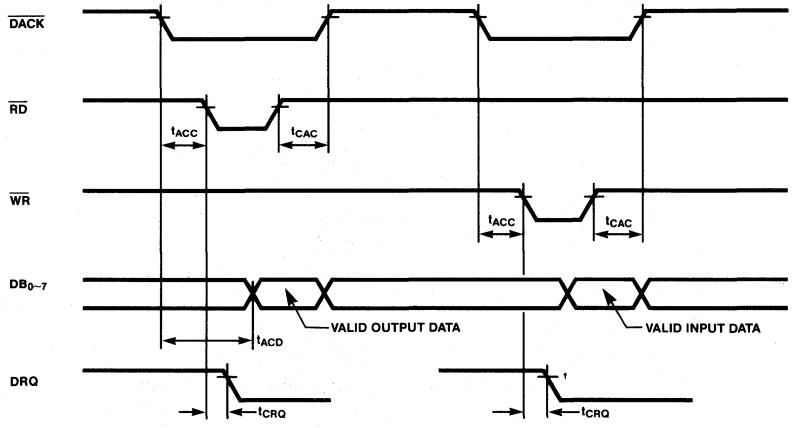
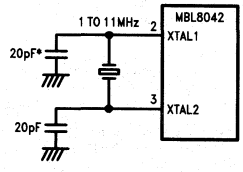


Figure 4. DMA Operation



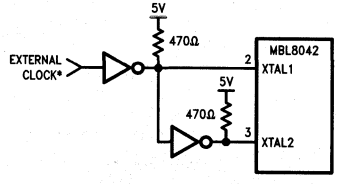
Oscillation Circuits

Crystal Oscillator



* Including stray capacitances

External Clock Driver

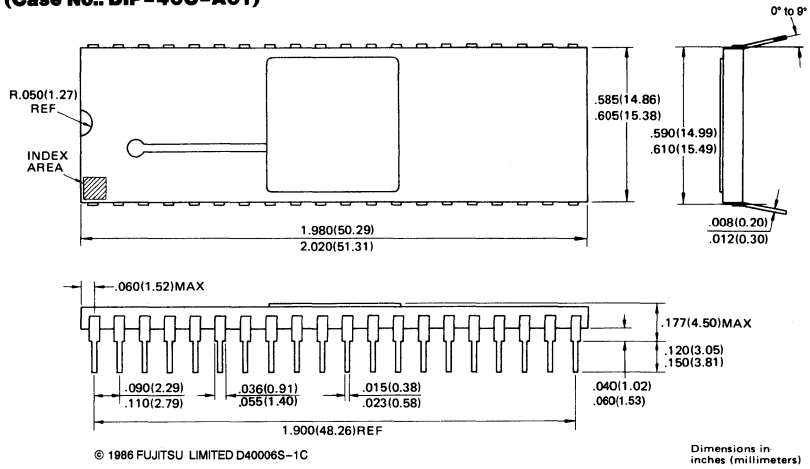


* Both high and low times should be more than 35% of the cycle time, and rise and fall times should be less than 20 ns.

Package Dimensions

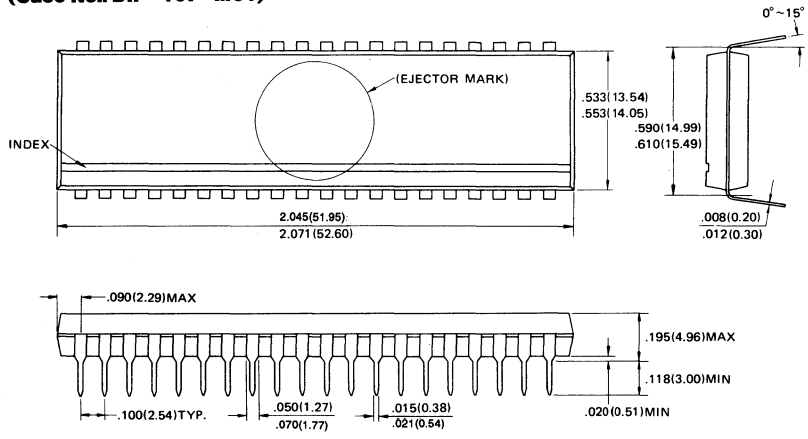
Dimensions in inches (millimeters)

40-Lead Ceramic (Metal Seal) Dual In-Line Package (Case No.: DIP-40C-A01)



Dimensions in inches (millimeters)

40-Lead Plastic Dual In-Line Package (Case No.: DIP-40P-M01)



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