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Edition 3.0

MBL8051AH, MBL8031AH

NMOS Single-Chip 8-Bit Microcomputer

Description

The Fujitsu MBL8051AH/8031AH are single-chip 8-bit microcomputers developed as members of the MBL8051 Series. These microcomputers have powerful architecture and instruction set designed for controller applications.

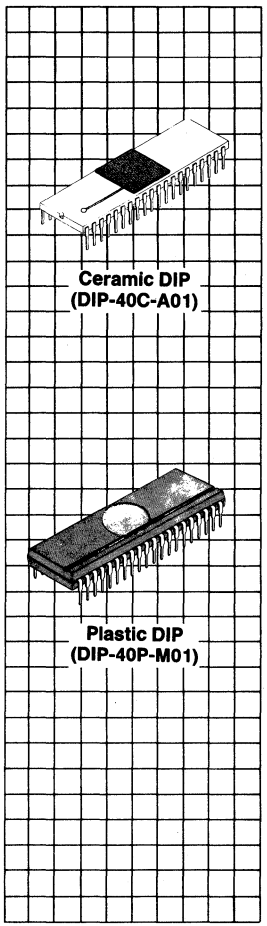
The MBL8051AH contains a 4K x 8-bit program memory (mask ROM), a 128 x 8-bit data memory (static RAM), 32 I/O lines configured as four 8-bit parallel ports, two programmable 16-bit timer/counters, a programmable serial I/O port, a five-source two-priority-level multi-interrupt function, and on-chip oscillator with clock circuitry. The MBL8031AH has all of these features except the on-chip memory.

The MBL8051AH/MBL8031AH can have up to 64K x 8-bit program memory and up to (64K + 128) x 8-bit data memory in expanded system configuration. Both microcomputers can use standard TTL compatible memories and most byte-oriented Intel MCS-80* and MCS-85* peripherals for additional memory and I/O capability.

As a control-oriented feature, the MBL8051AH/MBL8031AH have a bit handling hardware: 128 bit-locations in the data memory and the special function registers can be directly addressable by the user with bit manipulation instructions. This is very useful for control type applications.

The instruction set is designed for efficient use of the program memory space: consisting of 44% one-byte, 41% two-byte, and 15% three-byte instructions. At 12MHz clock, over half of the instructions execute in just 1.0μs, while the longest instructions, multiply and divide, require only 4μs.

The MBL8051AH/MBL8031AH are fabricated by Fujitsu's N-channel poly-silicon-gate E/D MOS process, and packaged in a 40-pin ceramic or plastic DIP. They have TTL compatible inputs/outputs and operate with a single +5V power supply and a 12MHz to 3.5MHz clock.



Ceramic DIP (DIP-40C-A01)

Plastic DIP (DIP-40P-M01)

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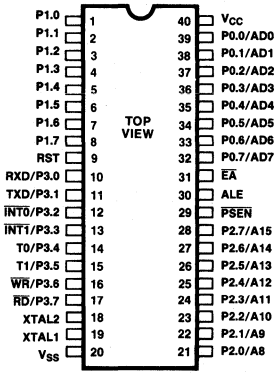
Features and Pin Assignment

- Control-Oriented 8-Bit CPU
- 4K x 8-Bit Program Memory (ROM for MBL8051AH Only)
- 128 x 8-Bit Data Memory (RAM)
- 32 I/O Lines (Four 8-Bit Ports)
- 128 x 8-Bit Special Function Registers
- Two Programmable 16-Bit Timer/Counters
- Programmable Full-Duplex Serial Channel
- Five-Source Maskable Two-Priority-Level Multi-Interrupt
- Expandability:
  - —Program Memory: Up to 64K x 8-Bits
  - —Data Memory, —I/O Ports: Up to (64K + 128) x 8 Bits
- Boolean Processor:
  - —218 User Bit-Addressable Locations
  - —Bit Manipulation Instructions
- Minimum Instruction Execution Time: 1μs (at 12MHz)
- 4μs (at 12MHz) Multiply and Divide
- On-chip Oscillator (3.5MHz–12MHz)
- Power-Down Mode: 10mA at V_{PD}=5V
- TTL Compatible I/O
- Single +5V Power Supply
- N-Channel Silicon-Gate E/D MOS Process
- Two Package Options:
  - —40-Pin Ceramic DIP (Suffix C)
  - —40-Pin Plastic DIP (Suffix P)
- Compatible with Intel MCS-80*/MCS-85* Peripherals
- MBL8048 Series (equivalent to Intel MCS-48*) Architecture Enhanced with:
  - —Non-Paged Jumps
  - —Direct Addressing
  - —Four 8-Register Banks
  - —Stack Depth up to 128 Bytes
  - —Multiply, Divide, Subtract, Compare



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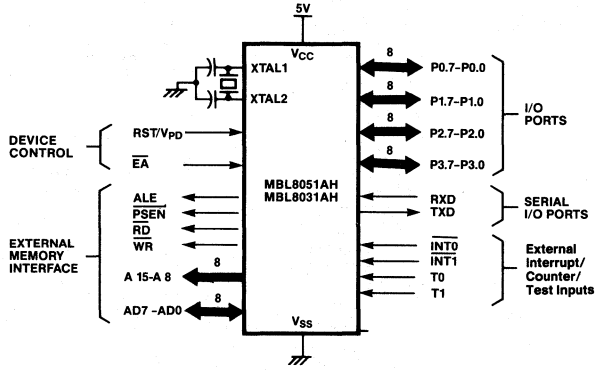
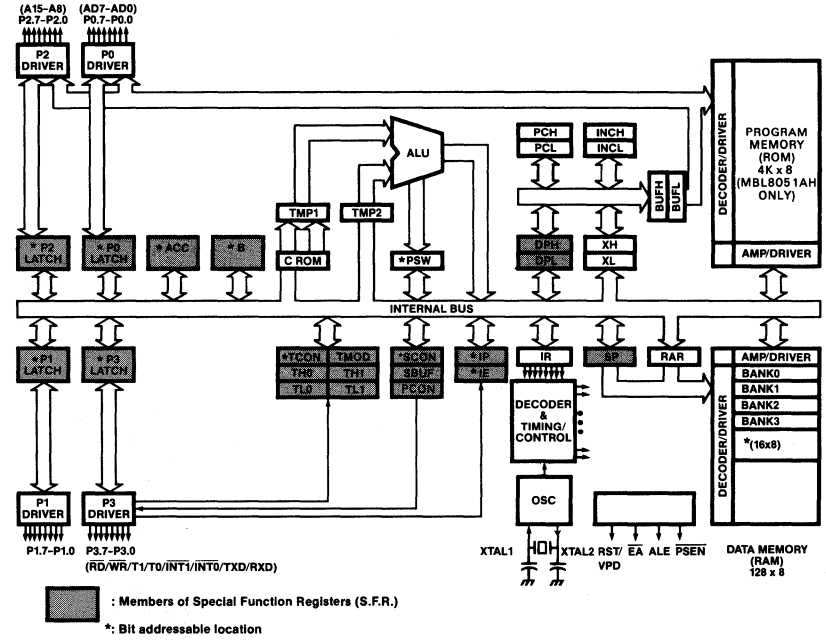
Logic Symbol



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Block Diagram



Pin Description

	Symbol	Pin No.	Type	Name & Function
Power Supply	V_{CC}	40	—	+5V power supply pin.
	V_{SS}	20	—	Ground pin.
Clock	XTAL1	19	I	Crystal 1: Input to the inverting amplifier that forms part of the oscillator. This pin should be connected to ground when an external oscillator is used.
	XTAL2	18	O	Crystal 2: Output of the inverting amplifier, and input to internal clock generator. This pin receives the oscillator signal when an external oscillator is used.
I/O Ports	P0.7/AD7-P0.0/AD0	32-39	I/O	Port 0: Port 0 is an 8-bit open-drain bidirectional I/O port. As an open-drain output port, each pin can sink 8 LS-TTL loads. Port 0 pins that have 1s written to them float, and in that state will function as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external memory. In this application it uses strong internal pullups when emitting 1s.
	P1.7-P1.0	8-1	I/O	Port 1: Port 1 is an 8-bit quasi-bidirectional I/O port with internal pullups. The Port 1 output buffers can sink/source 4 LS-TTL loads. Port 1 pins that have 1s written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups.

Pin Description
(continued)

	Symbol	Pin No.	Type	Name & Function
I/O Ports (Continued)	P2.7/A15- P2.0/A8	28-21	I/O	Port 2: Port 2 is an 8-bit quasi-bidirectional I/O port with internal pullups. The Port 2 output buffers can sink/source 4 LS-TTL loads. Port 2 emits the high-order address byte during accesses to external memory that use 16-bit addresses. In this application it uses the strong internal pullups when emitting 1s. Port 2 also receives the high-order address and control bits during program verification.
	P3.7-P3.0	17-10	I/O	Port 3: Port 3 is an 8-bit bidirectional I/O port with internal pullups. It also serves the functions of various special features of the MBL8051AH, as listed below: **Port Pin** — **Alternate Function** P3.0 — RXD (Serial input port) P3.1 — TXD (Serial output port) P3.2 — INT0 (External interrupt 0) P3.3 — INT1 (External interrupt 1) P3.4 — T0 (Timer 0 external input) P3.5 — T1 (Timer 1 external input) P3.6 — WR (External data memory write strobe) P3.7 — RD (External data memory read strobe) The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. The Port 3 output buffers can source/sink 4 LS-TTL loads.
Other Ports	RST	9	I	Reset input: A high on this pin for two machine cycles while the oscillator is running resets the device. A small external pulldown resistor ($\approx$8.2kΩ) from RST to V_{SS} permits power-on reset when a capacitor ($\approx$10pF) is also connected from RST to V_{CC}.
	ALE	30	O	Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory: ALE is emitted at a constant rate of 1/6 of the oscillator frequency, for external timing or clocking purposes, even when there are no accesses to external memory. However, one ALE pulse is skipped during each access to external data memory. ALE can sink/source 8 LS-TTL inputs.
	$\overline{PSEN}$	29	O	Program Store Enable is the read strobe to external program memory. When the device is executing out of external program memory, PSEN is activated twice each machine cycle (except that two PSEN activations are skipped during accesses to external data memory). PSEN is not activated; remaining high, during internal program memory execution.
	$\overline{EA}$	31	I	External Address Enable input: When $\overline{EA}$ is held high the CPU executes out of internal program memory (unless the program counter exceeds OFFFH). Holding $\overline{EA}$ low forces the CPU to execute out of external memory regardless of the program counter value. In the MBL8031AH, $\overline{EA}$ must be externally wired low.

Instruction Set Description

The MBL8051AH instruction set includes 111 instructions, 49 of which are single-byte, 45 two-byte and 17 three-byte. The instruction op code format consists of a function mnemonic followed by a "destination, source" operand field. This field specifies the data type and addressing method(s) to be used.

The MBL8051AH instruction set is divided into five functional groups:

- Arithmetic Operations
- Logical Operations
- Data Transfer
- Boolean Variable Manipulation
- Program & Machine Control (subroutine control/branch)

The following table summarizes the MBL8051AH instruction set.

Instruction Set Summary (1)

	Mnemonic + Operand	Operation	Op Code (Hex)	Byte/ Cycle	Program Status Word C	AC	F0	RS1	RS0	OV	—	P
Arithmetic Operations	ADD A, Rn	Add register to accumulator	2X	1/1	↕	↕	•	•	•	↕		↕
	ADD A, direct	Add direct byte to accumulator	25	2/1	↕	↕	•	•	•	↕		↕
	ADD A, @Ri	Add indirect RAM to accumulator	26 27	1/1	↕	↕	•	•	•	↕		↕
	ADD A, #data	Add immediate data to accumulator	24	2/1	↕	↕	•	•	•	↕		↕
	ADDC A, Rn	Add register to accumulator with carry	3X	1/1	↕	↕	•	•	•	↕		↕
	ADDC A, direct	Add direct byte to accumulator with carry	35	2/1	↕	↕	•	•	•	↕		↕
	ADDC A, @Ri	Add indirect RAM to accumulator with carry	36 37	1/1	↕	↕	•	•	•	↕		↕
	ADDC A, #data	Add immediate data to accumulator with carry	34	2/1	↕	↕	•	•	•	↕		↕
	SUBB A, Rn	Subtract register from accumulator with borrow	9X	1/1	↕	↕	•	•	•	↕		↕
	SUBB A, direct	Subtract direct byte from accumulator with borrow	95	2/1	↕	↕	•	•	•	↕		↕
	SUBB A, @Ri	Subtract indirect RAM from accumulator with borrow	96 97	1/1	↕	↕	•	•	•	↕		↕
	SUBB A, #data	Subtract immediate data from accumulator with borrow	94	2/1	↕	↕	•	•	•	↕		↕
	INC A	Increment accumulator	04	1/1	•	•	•	•	•	•		↕
	INC Rn	Increment register	0X	1/1	•	•	•	•	•	•		•

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Instruction Set Summary (1)(Continued)

Arithmetic Operations (continued)

Mnemonic + Operand	Operation	Op Code (Hex)	Byte/ Cycle	Program Status Word C	AC	F0	RS1	RS0	OV	—	P
INC direct	Increment direct byte	05	2/1	•	•	•	•	•	•		•
INC @Ri	increment indirect RAM	06 07	1/1	•	•	•	•	•	•		•
INC DPTR	Increment data pointer	A3	1/2	•	•	•	•	•	•		•
DEC A	Decrement accumulator	14	1/1	•	•	•	•	•	•		↕
DEC Rn	Decrement register	1X	1/1	•	•	•	•	•	•		•
DEC direct	Decrement direct byte	15	2/1	•	•	•	•	•	•		•
DEC @Ri	Decrement indirect RAM	16 17	1/1	•	•	•	•	•	•		•
MUL AB	Multiply A and B	A4	1/4	↕	•	•	•	•	↕		↕
DIV AB	Divide A by B	84	1/4	↕	•	•	•	•	↕		↕
DA A	Decimal adjust accumulator	D4	1/1	↕	•	•	•	•	•		↕

Instruction Set Summary (2)

Logical Operations

Mnemonic + Operand	Operation	Op Code (Hex)	Byte/ Cycle	Program Status Word C	AC	F0	RS1	RS0	OV	—	P
ANL A, Rn	AND register to accumulator	5X	1/1	•	•	•	•	•	•		↕
ANL A, direct	AND direct byte to accumulator	55	2/1	•	•	•	•	•	•		↕
ANL A, @Ri	AND indirect RAM to accumulator	56 57	1/1	•	•	•	•	•	•		↕
ANL A, #data	AND immediate data to accumulator	54	2/1	•	•	•	•	•	•		↕
ANL direct, A	AND accumulator to direct byte	52	2/1	•	•	•	•	•	•		•
ANL direct, #data	AND immediate data to a direct byte	53	3/2	•	•	•	•	•	•		•
ORL A, Rn	OR register to accumulator	4X	1/1	•	•	•	•	•	•		↕
ORL A, direct	OR direct byte to accumulator	45	2/1	•	•	•	•	•	•		↕
ORL A, @Ri	OR indirect RAM to accumulator	46 47	1/1	•	•	•	•	•	•		↕
ORL A, #data	OR immediate data to accumulator	44	2/1	•	•	•	•	•	•		↕
ORL direct, A	OR accumulator to direct byte	42	2/1	•	•	•	•	•	•		•
ORL direct, #data	OR immediate data to direct byte	43	3/2	•	•	•	•	•	•		•
XRL A, Rn	Exclusive-OR register to accumulator	6X	1/1	•	•	•	•	•	•		↕
XRL A, direct	Exclusive-OR direct byte to accumulator	65	2/1	•	•	•	•	•	•		↕

Instruction Set Summary (2)(Continued)

Logical Operations (continued)

Mnemonic + Operand	Operation	Op Code (Hex)	Byte/ Cycle	Program Status Word C	AC	F0	RS1	RS0	OV	—	P
XRL A, @Ri	Exclusive-OR indirect RAM to accumulator	65 67	1/1	•	•	•	•	•	•		↕
XRL A, #data	Exclusive-OR immediate data to accumulator	64	2/1	•	•	•	•	•	•		↕
XRL direct, A	Exclusive-OR accumulator to direct byte	62	2/1	•	•	•	•	•	•		•
XRL direct, #data	Exclusive-OR immediate data to direct byte	63	3/2	•	•	•	•	•	•		•
CLR A	Clear accumulator	E4	1/1	•	•	•	•	•	•		↕
CPL A	Complement accumulator	F4	1/1	•	•	•	•	•	•		•
RL A	Rotate accumulator left	23	1/1	•	•	•	•	•	•		•
RLC A	Rotate accumulator left through carry	33	1/1	↕	•	•	•	•	•		↕
RR A	Rotate accumulator right	03	1/1	•	•	•	•	•	•		•
RRC A	Rotate accumulator right through carry	13	1/1	↕	•	•	•	•	•		↕
SWAP A	Swap nibbles within accumulator	C4	1/1	•	•	•	•	•	•		•

Instruction Set Summary (3)

Data Transfer

Mnemonic + Operand	Operation	Op Code (Hex)	Byte/ Cycle	Program Status Word C	AC	F0	RS1	RS0	OV	—	P
MOV A, Rn	Move register to accumulator	EX	1/1	•	•	•	•	•	•		↕
*MOV A, direct	Move direct byte to accumulator	E5	2/1	•	•	•	•	•	•		↕
MOV A, @Ri	Move indirect RAM to accumulator	E6 E7	1/1	•	•	•	•	•	•		↕
MOV A, #data	Move immediate data to accumulator	74	2/1	•	•	•	•	•	•		↕
MOV Rn, A	Move accumulator to register	FX	1/1	•	•	•	•	•	•		•
MOV Rn, direct	Move direct byte to register	AX	2/2	•	•	•	•	•	•		•
MOV Rn, #data	Move immediate data to register	7X	2/1	•	•	•	•	•	•		•
MOV direct, A	Move accumulator to direct byte	F5	2/1	•	•	•	•	•	•		•
MOV direct, Rn	Move register to to direct byte	8X	2/2	•	•	•	•	•	•		•
MOV direct, direct	Move direct byte to direct byte	85	3/2	•	•	•	•	•	•		•

* MOV A, ACC is not a valid instruction

Instruction Set Summary (3)(Continued)

	Mnemonic + Operand	Operation	Op Code (Hex)	Byte/ Cycle	Program Status Word C	AC	F0	RS1	RS0	OV	—	P
Data Transfer (continued)	MOV direct, @Ri	Move indirect RAM to direct byte	86 87	2/2	•	•	•	•	•	•		•
	MOV direct, #data	Move immediate data to direct byte	75	3/2	•	•	•	•	•	•		•
	MOV @Ri, A	Move accumulator to indirect RAM	F6 F7	1/1	•	•	•	•	•	•		•
	MOV @Ri, direct	Move direct byte to indirect RAM	A6 A7	2/2	•	•	•	•	•	•		•
	MOV @Ri, #data	Move immediate data to indirect RAM	76 77	2/1	•	•	•	•	•	•		•
	MOV DPTR, #data 16	Load data pointer with a 16-bit constant	90	3/2	•	•	•	•	•	•		•
	MOVC A, @A+DPTR	Move code byte relative to data pointer to accumulator	93	1/2	•	•	•	•	•	•		↕
	MOVC A, @A+PC	Move code byte relative to program counter to accumulator	83	1/2	•	•	•	•	•	•		↕
	MOVX A, @Ri	Move external RAM (8-bit addr) to accumulator	E2 E3	1/2	•	•	•	•	•	•		↕
	MOVX A, @DPTR	Move external RAM (16-bit addr) to accumulator	E0	1/2	•	•	•	•	•	•		↕
	MOVX @Ri, A	Move accumulator to external RAM (8-bit addr)	F2 F3	1/2	•	•	•	•	•	•		•
	MOVX @DPTR, A	Move accumulator to external RAM (16-bit addr)	F0	1/2	•	•	•	•	•	•		•

Instruction Set Summary (3)(Continued)

	Mnemonic + Operand	Operation	Op Code (Hex)	Byte/ Cycle	Program Status Word C	AC	F0	RS1	RS0	OV	—	P
Data Transfer (continued)	PUSH direct	Push direct byte onto stack	C0	2/2	•	•	•	•	•	•		•
	POP direct	Pop direct byte from stack	D0	2/2	•	•	•	•	•	•		•
	XCH A, Rn	Exchange register with accumulator	CX	1/1	•	•	•	•	•	•		↕
	XCH A, direct	Exchange direct byte with accumulator	C5	2/1	•	•	•	•	•	•		↕
	XCH A, @Ri	Exchange indirect RAM with accumulator	C6 C7	1/1	•	•	•	•	•	•		↕
	XCHD A, @Ri	Exchange low-order digit indirect RAM with A	D6 D7	1/1	•	•	•	•	•	•		↕
Boolean Variable Manipulation	CLR C	Clear carry flag	C3	1/1	↕	•	•	•	•	•		•
	CLR bit	Clear direct bit	C2	2/1	•	•	•	•	•	•		•
	SETB C	Set carry flag	D3	1/1	↕	•	•	•	•	•		•
	SETB bit	Set direct bit	D2	2/1	•	•	•	•	•	•		•
	CPL C	Complement carry flag	B3	1/1	↕	•	•	•	•	•		•
	CPL bit	Complement direct bit	B2	2/1	•	•	•	•	•	•		•
	ANL C, bit	AND direct bit to carry flag	82	2/2	↕	•	•	•	•	•		•
	ANL C, 1 bit	AND complement of direct bit to carry flag	B0	2/2	↕	•	•	•	•	•		•
	ORL C/bit	OR direct bit to carry flag	72	2/2	↕	•	•	•	•	•		•
	ORL C, 1 bit	OR complement of direct bit to carry flag	A0	2/2	↕	•	•	•	•	•		•
	MOV C/bit	Move direct bit to carry flag	A2	2/1	↕	•	•	•	•	•		•
	MOV bit, C	Move carry flag to direct bit	92	2/2	•	•	•	•	•	•		•

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Instruction Set Summary (4)

	Mnemonic + Operand	Operation	Op Code (Hex)	Byte/ Cycle	Program Status Word C	AC	F0	RS1	RS0	OV	–	P
Program and Machine Control	ACALL addr 11	Absolute subroutine call	*1	2/2	•	•	•	•	•	•		•
	CALL addr	ACALL addr 11 or LCALL addr 16			•	•	•	•	•	•		•
	LCALL addr 16	Long subroutine call	12	3/2	•	•	•	•	•	•		•
	RET	Return from subroutine	22	1/2	•	•	•	•	•	•		•
	RETI	Return from interrupt	32	1/2	•	•	•	•	•	•		•
	AJMP addr 11	Absolute jump	*1	2/2	•	•	•	•	•	•		•
	LJMP addr 16	Long jump	02	3/2	•	•	•	•	•	•		•
	SJMP rel	Short jump (relative addr)	80	2/2	•	•	•	•	•	•		•
	JMP @A+DPTR	Jump indirect relative to data pointer	73	1/2	•	•	•	•	•	•		•
	JZ rel	Jump if accumulator is zero	60	2/2	•	•	•	•	•	•		•
	JNZ rel	Jump if accumulator is not zero	70	2/2	•	•	•	•	•	•		•
	JC rel	Jump if carry flag is set	40	2/2	•	•	•	•	•	•		•
	JNC rel	Jump if carry flag is not set	50	2/2	•	•	•	•	•	•		•
	JB bit, rel	Jump if direct bit is set	20	3/2	•	•	•	•	•	•		•
	JNB bit, rel	Jump if direct bit is not set	30	3/2	•	•	•	•	•	•		•
	JBC bit, rel	Jump if direct bit is set & clear bit	10	3/2	•	•	•	•	•	•		•
	CJNE A, direct, rel	Compare direct to accumulator & jump if not equal	B5	3/2	↕	•	•	•	•	•		•
	CJNE A, #data, rel	Compare immediate data to A & jump if not equal	B4	3/2	↕	•	•	•	•	•		•
	CJNE Rn, #data, rel	Compare immediate data to reg. & jump if not equal	B6 B7	3/2	↕	•	•	•	•	•		•
	CJNE @Ri, #data, rel	Compare immediate data to indirect RAM & jump if not equal	BX	3/2	↕	•	•	•	•	•		•
	DJNZ Rn, rel	Decrement register & jump if not zero	DX	2/2	•	•	•	•	•	•		•
	DJNZ direct, rel	Decrement direct byte & jump if not zero	D5	3/2	•	•	•	•	•	•		•
	NOP	No operation	00	1/1	•	•	•	•	•	•		•

Instruction Set Description (Continued)

Notes on Data Addressing Modes:

Rn	— Working register R0-R7 (See Table 1 below)
direct	— 128 internal RAM locations, any I/O port, control status register
@Ri	— Indirect internal RAM location addressed by register R0 or R1
#data	— 8-bit constant included in instruction
#data 16	— 16-bit constant included as bytes 2 & 3 of instruction
bit	— 128 software flags, any I/O pin, control status bit

Notes on Program Addressing Modes:

addr 16	— Destination address for LCALL & LJMP may be anywhere within the 64K program memory address space.
addr 11	— Destination address for ACALL & AJMP will be within the same 2K page of program memory as the first byte of the following instruction.
rel	— SJMP and all conditional jumps include an 8-bit offset byte. Range is +127 to −128 bytes relative to first byte of the following instruction.

Notes on Affecting Flag Setting:

↕ — Affected (set or reset)
• — Not affected

Notes on Instruction Set Op Codes:
1. See Table 1 for op code X.
2. *The first 3 bits of op code are determined by operand (addr 11).

Table 1 Op codes of Register Access Instructions

Mnemonic + Operand	Rn	R0	R1	R2	R3	R4	R5	R6	R7
ADD A, Rn		28	29	2A	2B	2C	2D	2E	2F
ADDC A, Rn		38	39	3A	3B	3C	3D	3E	3F
SUBB A, Rn		98	99	9A	9B	9C	9D	9E	9F
INC Rn		08	09	0A	0B	0C	0D	0E	0F
DEC Rn		18	19	1A	1B	1C	1D	1E	1F
ANL A, Rn		58	59	5A	5B	5C	5D	5E	5F
ORL A, Rn		48	49	4A	4B	4C	4D	4E	4F
XRL A, Rn		68	69	6A	7B	6C	6D	6E	6F
MOV A, Rn		E8	E9	EA	EB	EC	ED	EE	EF
MOV Rn, A		F8	F9	FA	FB	FC	FD	FE	FF
MOV Rn, #data		78	79	7A	7B	7C	7D	7E	7F
MOV Rn, direct		A8	A9	AA	AB	AC	AD	AE	AF
MOV direct, Rn		88	89	8A	8B	8C	8D	8E	8F
XCH A, Rn		C8	C9	CA	CB	CC	CD	CE	CF

Instruction Set Description (Continued)

Instruction Code Summary

L \ H	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	JBC bit, rel	JB bit, rel	JNB bit, rel	JC rel	JNC rel	JZ rel	JNZ rel	SJMP rel	MOV DPTR, # data 16	ORL C, /bit	ANL C, /bit	PUSH dir	POP dir	MOVX A, @DPTR	MOVX @ DPTR, A
1	AJMP (P0)	ACALL (P0)	AJMP (P1)	ACALL (P1)	AJMP (P2)	ACALL (P2)	AJMP (P3)	ACALL (P3)	AJMP (P4)	ACALL (P4)	AJMP (P5)	ACALL (P5)	AJMP (P6)	ACALL (P6)	AJMP (P7)	ACALL (P7)
2	LJMP addr16	LCALL addr16	RET	RETI	ORL dir, A	ANL dir, A	XRL dir, A	ORL C, bit	ANL C, bit	MOV bit, C	MOV C, bit	CPL bit	CLR bit	SETB bit	MOVX A, @R0	MOVX @R0, A
3	RR A	RRC A	RL A	RLC A	ORL dir, #data	ANL dir, #data	XRL dir, #data	JMP @A+DPTR	MOVCA, @A+PC	MOVCA, @A+DPTR	INC DPTR	CPL C	CLR C	SETB C	MOVX A, @R1	MOVX @R1, A
4	INC A	DEC A	ADD A, #data	ADDC A, #data	ORL A, #data	ANL A, #data	XRL A, #data	MOV A, #data	DIV AB	SUBB A, #data	MUL AB	CJNE, A, #data, rel	SWAP A	DA A	CLR A	CPL A
5	INC dir	DEC dir	ADD A, dir	ADDC A, dir	ORL A, dir	ANL A, dir	XRL A, dir	MOV dir, #data	MOV dir, dir	SUBB A, dir		CJNE A, dir, rel	XCH A, dir	DJNZ dir, rel	MOV A, dir	MOV dir, A
6	INC @R0	DEC @R0	ADD A, @R0	ADDC A, @R0	ORL A, @R0	ANL A, @R0	XRL A, @R0	MOV @R0, #data	MOV dir, @R0	SUBB A, @R0	MOV @R0, dir	CJNE @R0, #data, rel	XCH A, @R0	XCHD A, @R0	MOV A, @R0	MOV @ R0, A
7	INC @R1	DEC @R1	ADD A, @R1	ADDC A, @R1	ORL A, @R1	ANL A, @R1	XRL A, @R1	MOV @R1, # data	MOV dir, @R1	SUBB A, @R1	MOV @R1, dir	CJNE @R1, #data, rel	XCH A, @R1	XCHD A, @R1	MOV A, @R1	MOV @ R1, A
8	INC R0	DEC R0	ADD A, R0	ADDC A, R0	ORL A, R0	ANL A, R0	XRL A, R0	MOV R0, #data	MOV dir, R0	SUBB A, R0	MOV R0, dir	CJNE R0, #data, rel	XCH A, R0	DJNZ R0, rel	MOV A, R0	MOV R0, A
9	INC R1	DEC R1	ADD A, R1	ADDC A, R1	ORL A, R1	ANL A, R1	XRL A, R1	MOV R1, #data	MOV dir, R1	SUBB A, R1	MOV R1, dir	CJNE R1, #data, rel	XCH A, R1	DJNZ R1, rel	MOV A, R1	MOV R1, A
A	INC R2	DEC R2	ADD A, R2	ADDC A, R2	ORL A, R2	ANL A, R2	XRL A, R2	MOV R2, #data	MOV dir, R2	SUBB A, R2	MOV R2, dir	CJNE R2, #data, rel	XCH A, R2	DJNZ R2, rel	MOV A, R2	MOV R2, A
B	INC R3	DEC R3	ADD A, R3	ADDC A, R3	ORL A, R3	ANL A, R3	XRL A, R3	MOV R3, #data	MOV dir, R3	SUBB A, R3	MOV R3, dir	CJNE R3, #data, rel	XCH A, R3	DJNZ R3, rel	MOV A, R3	MOV R3, A
C	INC R4	DEC R4	ADD A, R4	ADDC A, R4	ORL A, R4	ANL A, R4	XRL A, R4	MOV R4, #data	MOV dir, R4	SUBB A, R4	MOV R4, dir	CJNE R4, #data, rel	XCH A, R4	DJNZ R4, rel	MOV A, R4	MOV R4, A
D	INC R5	DEC R5	ADD A, R5	ADDC A, R5	ORL A, R5	ANL A, R5	XRL A, R5	MOV R5, #data	MOV dir, R5	SUBB A, R5	MOV R5, dir	CJNE R5, #data, rel	XCH A, R5	DJNZ R5, rel	MOV A, R5	MOV R5, A
E	INC R6	DEC R6	ADD A, R6	ADDC A, R6	ORL A, R6	ANL A, R6	XRL A, R6	MOV R6, #data	MOV dir, R6	SUBB A, R6	MOV R6, dir	CJNE R6, #data, rel	XCH A, R6	DJNZ R6, rel	MOV A, R6	MOV R6, A
F	INC R7	DEC R7	ADD A, R7	ADDC A, R7	ORL A, R7	ANL A, R7	XRL A, R7	MOV R7, #data	MOV dir, R7	SUBB A, R7	MOV R7, dir	CJNE R7, #data, rel	XCH A, R7	DJNZ R7, rel	MOV A, R7	MOV R7, A

2Byte		3Byte
2Cycle	Boolean Manipulation	4Cycle

Absolute Maximum Ratings

Parameter	Symbol	Rating Min.	Rating Max.	Unit
Supply Voltage	V_{CC}	V_{SS}-0.3	V_{SS}+7.0	V
Input Voltage	V_{IN}	V_{SS}-0.3	V_{SS}+7.0	V
Output Voltage	V_{OUT}	V_{SS}-0.3	V_{SS}+7.0	V
Power Dissipation	P_D		1.5	W
Operating Ambient Temperature	T_A	0	+70	°C
Storage Temperature	Tstg	-55	+150	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Value Min.	Value Typ.	Value Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}		0		V
Operating Ambient Temperature	T_A	0		+70	°C

2

DC Characteristics

(V_{CC} = 5V ±10%,
V_{SS} = 0V, T_A = 0°C to 70°C)

Parameter	Pin	Symbol	Value Min.	Value Max.	Unit	Test Conditions
Input High Voltage	All Inputs except RST and XTAL2	V_{IH}	2.0	V_{CC}+0.5	V	
	RST and XTAL2	V_{IH1}	2.5	V_{CC}+0.5	V	XTAL1=0V
Input Low Voltage		V_{IL}	V_{SS}-0.3	0.8	V	
Power-Down Voltage	VPD	V_{PD}	4.5	5.5	V	V_{CC}=0V
Output High Voltage	Ports 1, 2, 3	V_{OH}	2.4		V	I_{OH}=-80μA
	Port 0, ALE, $\overline{PSEN}$	V_{OH1}	2.4		V	I_{OH}=-400μA
Output Low Voltage	Ports 1, 2, 3	V_{OL}		0.45	V	I_{OL}=1.6mA
	Port 0, ALE, $\overline{PSEN}$	V_{OL1}		0.45	V	I_{OL}=3.2mA
Low Level Input Leakage Current	Ports 1, 2, 3	I_{IL}		-500	μA	V_{IN}=0.45V
	XTAL2	I_{IL2}		-3.2	mA	XTAL1=0V, VIN=0.45V
High Level Input Leakage Current	RST	I_{IH1}		500	μA	$V_{IN} < V_{CC}$-1.5V
Input Leakage Current	Port 0, $\overline{EA}$	I_{LI}	-10	+10	μA	0.45V<V_{IN}<V_{CC}
Power Supply Current	V_{CC}	I_{CC}		125	mA	All outputs open; $\overline{EA}$ = V_{CC}
Power-Down Current	VPD	I_{PD}		10	mA	V_{CC}=0V, V_{PD}=5V
Capacitance of I/O Buffer		C_{IO}		10	pF	f_C=1.0MHz,

Note: Capacitive loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the VOLs of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases, the noise pulse on the ALE line may exceed 0.8V. In such cases it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input.

AC Characteristics
(V_{CC} = 5V ± 10%, V_{SS} = 0V; T_A = 0°C to 70°C, C_L = 100pF for Port 0, ALE and $\overline{PSEN}$ outputs, C_L = 80pF for all other outputs)

External Program Memory Characteristics

Parameter	Symbol	fc = 12 MHz Min.	fc = 12 MHz Max.	Unit	fc = 3.5MHz to 12 MHz Min.	fc = 3.5MHz to 12 MHz Max.	Unit
Oscillation Period	TCLCL	83		ns	1/fc (Max.)	1/fc (Min.)	
Cycle Time	TCY	1.0		μs	12TCLCL (Min.)	12TCLCL (Max.)	
ALE Pulse Width	TLHLL	127		ns	2TCLCL-40		ns
Address Setup Time (To ALE)	TAVLL	43		ns	TCLCL-40		ns
Address Hold Time (After ALE)	TLLAX	48		ns	TCLCL-35		ns
Instr In Delay Time (After ALE)	TLLIV		233	ns		4TCLCL-100	ns
ALE to $\overline{PSEN}$	TLLPL	58		ns	TCLCL-25		ns
$\overline{PSEN}$ Pulse Width	TPLPH	215		ns	3TCLCL-35		ns
Instr In Delay Time (After $\overline{PSEN}$)	TPLIV		125	ns		3TCLCL-125	ns
Input Instr Hold Time (After $\overline{PSEN}$)	TPXIX	0		ns	0		ns
Input Instr Float Time (After $\overline{PSEN}$)	TPXIZ		63	ns		TCLCL-20	ns
Address Delay Time (After $\overline{PSEN}$)	TPXAV	75		ns	TCLCL-8		ns
Input Instr Delay Time (After Address)	TAVIV		302	ns		5TCLCL-115	ns
Address Float Time (To $\overline{PSEN}$)	TPLAZ		20	ns		20	ns

External Data Memory Characteristics

$\overline{RD}$ Pulse Width	TRLRH	400		ns	6TCLCL-100		ns
$\overline{WR}$ Pulse Width	TWLWH	400		ns	6TCLCL-100		ns
Address Hold Time (After ALE)	TLLAX	48		ns	TCLCL-35		ns
Data In Delay Time (After $\overline{RD}$)	TRLDV		252	ns		5TCLCL-165	ns
Data Hold Time (After $\overline{RD}$)	TRHDX	0		ns	0		ns
Data Float Time (After $\overline{RD}$)	TRHDZ		97	ns		2TCLCL-70	ns
Data In Delay Time (After ALE)	TLLDV		517	ns		8TCLCL-150	ns
Data In Delay Time (After Address)	TAVDV		585	ns		9TCLCL-165	ns
ALE To $\overline{RD}$ or $\overline{WR}$	TLLWL	200	300	ns	3TCLCL-50	3TCLCL+50	ns
Address Setup Time (To $\overline{RD}$ or $\overline{WR}$)	TAVWL	203		ns	4TCLCL-130		ns
$\overline{RD}$ or $\overline{WR}$ High To ALE High	TWHLH	43	123	ns	TCLCL-40	TCLCL+40	ns

2

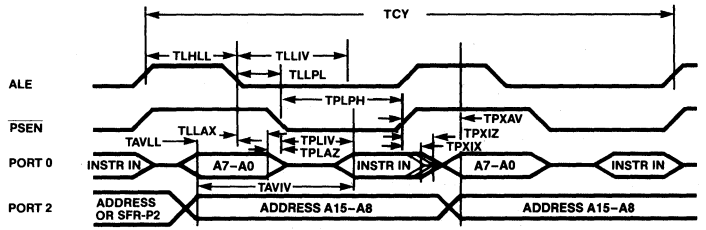
AC Characteristics

(V_{CC} = 5V ±10%, V_{SS} = 0V; T_A = 0°C to 70°C, C_L = 100pF for Port 0, ALE and $\overline{PSEN}$ outputs, C_L = 80pF for all other outputs)

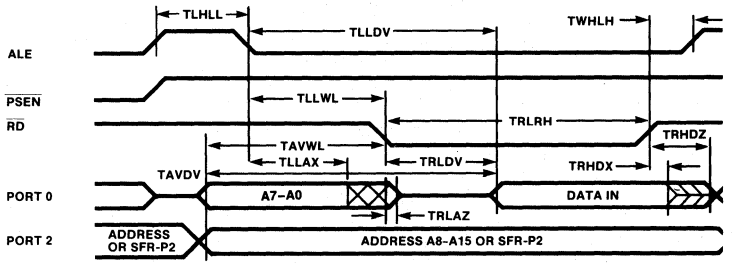
External Data Memory Characteristics (Continued)

Parameter	Symbol	fc = 12 MHz Min.	Max.	Unit	fc = 3.5MHz to 12 MHz Min.	Max.	Unit
Data Valid To WR Transition	TQVWX	23		ns	TCLCL-60		ns
Data Setup Time (Before WR)	TQVWH	433		ns	7TCLCL-150		ns
Data Hold Time (After WR)	TWHQX	33		ns	TCLCL-50		ns
Address Float Time (After RD)	TRLAZ		20	ns		20	ns

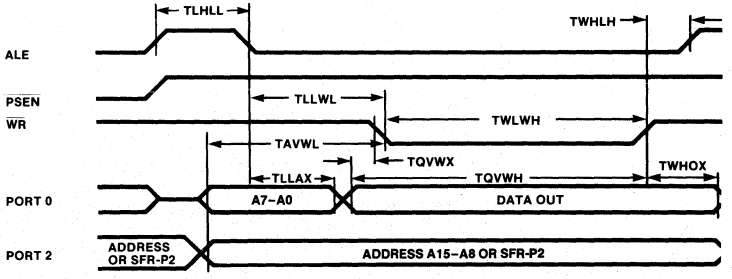
External Program Memory Read Cycle Timing Diagram



External Data Memory Read Cycle Timing Diagram



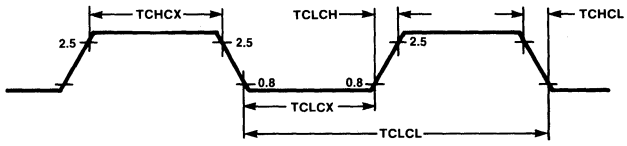
External Data Memory Write Cycle Timing Diagram



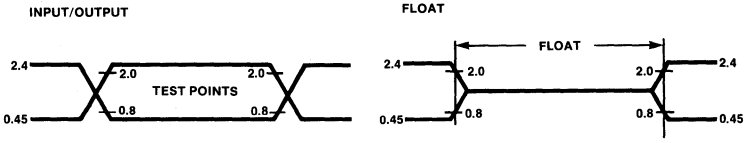
External Clock Drive Characteristics

Parameter	Symbol	fc = 3.5 MHz to 12 MHz Min.	Max.	Unit
Oscillation Frequency	1/TCLCL	3.5	12	ns
High Time	TCHCX	20		ns
Low Time	TCLCX	20		ns
Rise Time	TCLCH		20	ns
Fall Time	TCHCL		20	ns

External Clock Timing Diagram

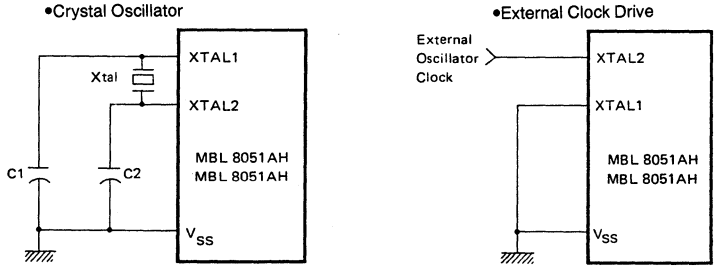


AC Testing Input/Output and Float Waveforms



AC inputs during testing are driven at 2.4V for a logic "1" and 0.45V for a logic "0". Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0". For timing purposes, the float state is defined as the point at which a P0 pin sinks 3.2mA or sources 400μA at the voltage test levels.

Oscillator Configurations



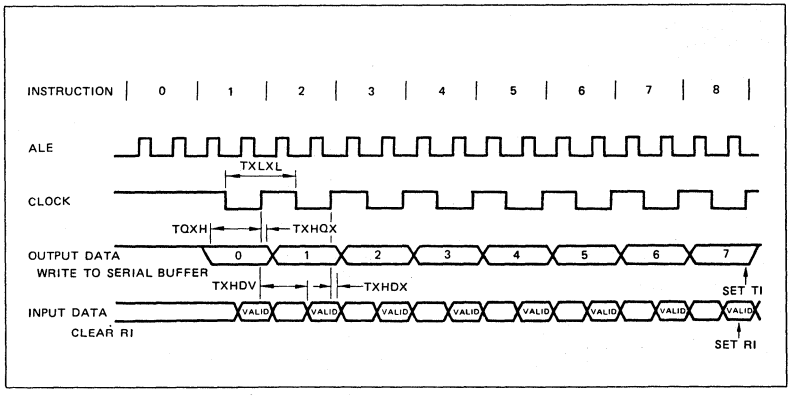
C1 = C2 = 30pF ± 10pF
Xtal = Crystal Resonator

Serial Port Timing— Shift Register Mode

(Test Conditions: V_{CC} = 5V ±10%, V_{SS} = 0V, T_A = 0°C to 70°C, C_L = 80 pF)

Symbol	Parameter	f_C = 12MHz		f_c = 3.5MHz to 12MHz		Units
		Min	Max	Min	Max	
TXLXL	Serial Port Clock Cycle Time	1.0		12TCLCL		μs
TQVXH	Output Data Setup to Clock Rising Edge	700		10TCLCL-133		ns
TXHQX	Output Data Hold After Clock Rising Edge	50		2TCLCL-117		ns
TXHDX	Input Data Hold After Clock Rising Edge	0		0		ns
TXHDV	Clock Rising Edge to Input Data Valid		700		10TCLCL-133	ns

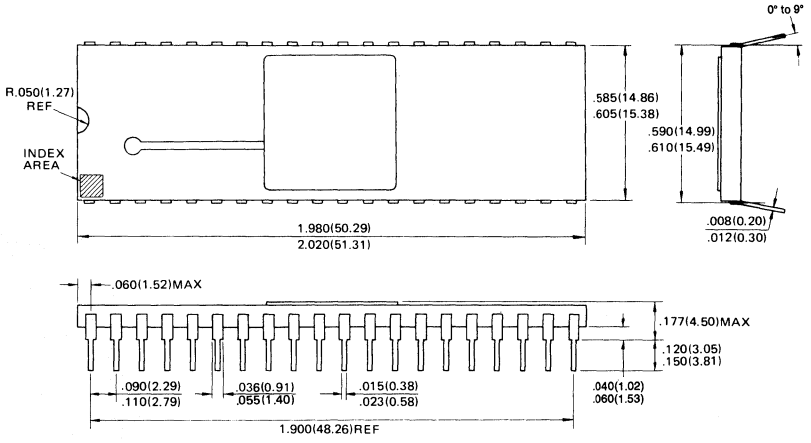
Serial Port Timing Diagram



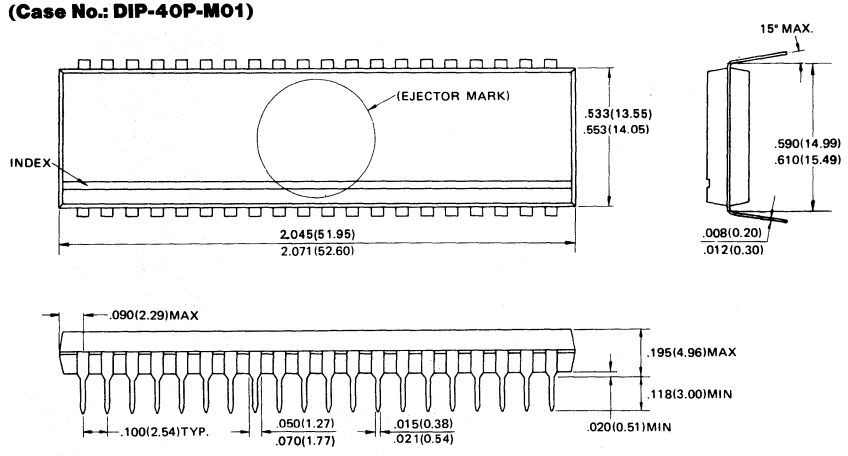
Package Dimensions

Dimensions in inches
(millimeters)

40-Lead Ceramic
(Metal Seal)
Dual In-Line Package
(Case No.: DIP-40C-A01)



40-Lead Plastic
Dual In-Line Package
(Case No.: DIP-40P-M01)



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